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COMPARISON OF DIFFERENT MICRO-COMPUTER ARCHITECTURES

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Abstract: Theaim of this paper is to represent an insightful comparison between four of the most popular and widely used architectures that are Advanced RISC Machine (ARM), Microprocessor without Interlocked Pipelined Stages (MIPS), Performance Optimization with Enabled RISC – Performance Computing (PowerPC) and Scalable Processor Architecture(SPARC). All these four architecture belongs to the Reduced Instruction Set Architecture (RISC) processor family. In order to acknowledge the user about the differences between these ISA's and impact of each individual of them, a contrastamong these architectures is extremely necessary. As these architectures are used in several applications, this paper attempts to cover some ofsoftware and hardware applications that will help in identifying the differences between them. This paper provides enough information that will help the reader to select the best suited ISA for his required application.

Key words:ARM, MIPS, PowerPC, SPARC, computer architectures

I. INTRODUCTION

Unlike Complex Instruction Set Computer (CISC), which has complex and variable size instructions, the Reduced Instruction Set Computer Architecture (RISC) has simple as well as fixed length instructions, few addressing modes that are easy for the hardware to manipulate [1-12]. The only instructions in RISC processors that deal with the memory are the Load/Store instructions.This paper covers fourpopular RISC family architectures including ARM, MIPS, PowerPC and SPARC.Many applications of these four architectures exist [13-19].This paper presents different features like registers, addressing modes and operating modes of MIPS, ARM, POWERPC and SPARC that will give the reader a better understanding of how different architectures works and how they use the different kind of addressing modes.

ARM is the most popular ISA among the others with over 50 billion ARM processors produced as of 2014. ARM is highly valued in the mobiles and tablets world. MIPS fall slightly behind ARM but still is a popular RISC architecture. MIPS was initially used for embedded system but it has now stepped into the mobile market as well.PowerPC is a joint invention of Apple-IBM-Motorola shortly known as AIM. Initially PowerPC was intended to support Personal Computers. But since then PowerPC CPUs has evolved a lot and has become popular as embedded and high performance processors.In1987 Sun Microsystems introduced the SPARCarchitecture [20-33]. Sun Microsystems owned SPARCfor almost 25 years but later was acquired by ORACLE Corporation.

This section provides a brief history about the four ISA's (ARM, MIPS, PowerPC and SPARC).

II. Overview of Various Architecture

i. **ARM:**The ARM, initially was known as Acorn RISC Machine but later it changed to Advanced RISC Machine, was invented by a British company called Acorn Computer in 1985. The main aim of the company was to produce low cost PCs. Now ARM is

leading the mobile market. With over 50 billion ARM processors produced as of 2014, ARM is the most widely used Instruction Set Architecture.

ii. **MIPS:** The MIPS, stands for Microprocessor without Interlocked Pipelined Stages, is one of the members of the RISC family.The MIPS was invented in the early 1980's in Stanford University. The MIPS was initially developed with the idea to support embeddedsystemsbut currently it has started to support the mobile market as well. Many versions of MIPS have been introduced into the market so far that are MIPS I, MIPS II, MIPS III, MIPS IV, MIPS V.MIPS has also developed a MIPS32 (for 32-bit implementations) and MIPS64 (for 64-bit implementations).

iii. **PowerPC:** PowerPC, stands for Performance Optimization with Enabled RISC – Performance Computing, is a RISC ISA created in 1991 by the Apple-IBM-Motorola alliance known as AIM. PowerPCISA is an evolving instruction set. Initially PowerPC was intended for personal computers. PowerPC CPUs have since become popular as embedded and high performance processors.

iv. **SPARC:**The Scalable Processor Architecture was developed by Sun Microsystems in 1987. SPARC CPUs are considered as high performance CPUs. There are many CPU implementation of SPARC with features likeimplementation compatibility, graphical user interface (GUI), many compiler tools and many other.

III. Applications

There are many applications of ARM, MIPS, PowerPC and SPARC. This section provides some information about the applications of the four processors.

I. **ARM:** ARM is one of the most popular RISC processor. ARM is widely used in all areas of technology, especially in mobile and tablets devices. It's because of the key features of ARM like high performance, low power consumption and low implementation cost that make it the most favorable ISA for mobile technology. ARM has developed two main profile architectures that are ARMv8-A and ARMv8-R. ARMv8-A architecture is used in mobile and enterprise while ARMv8-R architecture is used for embedded applications in automotive and industrial control.Besides this ARM has developed a Cortex series: the Cortex-M series which is used widely in embedded applications and the Cortex-A series which is widely used in avionics, security and telemedicine.

ARM these days is a widely used architecture. Because of its popularity many universities are now using ARM'sISAto teach their students about assembly language and to acquire the necessary up-to-date knowledge.

II. **MIPS:**MIPS is also a widely used architecture and has many applications. MIPS implementations are primarily used in embedded systems and networking areas like routers, residential gateways, video game consoles such as Sony Play Station, Nintendoand Play Station Portable.MIPS implementations were also used by Digital Equipment Corporation, Pyramid Technology, Tandem Computers and many others during the late 1980s and 1990s. One of the reasons of MIPS popularity is that it has many open source implementations. Beginners who are

willing to learn how to code in assembly language uses MIPS.

MIPS has an application, known as MIPS Management (MM) that ensures the efficient running of the programs running on MIPS. MM, nowadays, reduces the amount of CPU resources, lowers thecost of applications running on MIPS that are not in use which makes it very beneficial in avoiding faults (for example, it is useful in coding online transactions).To ensure efficient utilization of memory, MIPS has a Memory Management Unit (MMU) that helps in reduction of unnecessary memory loss and cost of memory consumption.

III. **PowerPC:**PowerPC was originally intended for Personal Computers but since then it has become popular as embedded and high performance processors. PowerPC has been used by iMac, iBook, Apple's Power Macintosh, PowerBook and Xserve line. Apple is not using PowerPC any more instead it is using Intel. PowerPC is also used in video game consoles and embedded applications. AmigaOne (a series of computers) and third party AmigaOS-4 (an operating system which runs on PowerPC) personal computers still use PowerPC CPUs. PowerPC family includes PowerPC e200 which is ideal for embedded applications with a speed ranging up to 600 MHz, PowerPC e300 similar to e200 but with an increased speedofup to 667 MHz, PowerPC e600 speed of up to 2GHz, ideal for high performance routing and telecommunication where complex computation takes place, POWER5 a dual core version, POWER6 executes instruction in order instead of out-of-order and a lot of other PowerPC implementations.

IV. **SPARC:** SPARC was initially owned by Sun Microsystems for almost 25 years but later in 2010 it was acquired by ORACLE Corporation. In those 25 years, Sun Microsystems publishes many applications for the SPARCbasedComputers. The initial versions of SPARC include SPARC-v7 (1986) a 32-bit processor, SPARC-v8 (1990) also 32-bit, SPARC-v9 (1993) a 64-bit processor. SPARC processors were used in Symmetric Multi-Processing (SMP) server produced by SPARC, SolbourneComputer and Fujitsu. There are many implementations of SPARC like SPARC station1, the Dual-Core UltraSPARC IV was first the multi-core SPARC processor. ORACLE introduced the M-Series and T-series of SPARC.

Addressing Modes: This section compares different addressing modes of different ISA architecture [33-44].

I. **ARM:**ARM supports multiple addressing modes. There are four main addressing modes to calculate the effective address:
   a. **Pre-indexed Addressing:** Source/destination address is stored in a register offset by another value.
   b. **Pre-indexed Addressing with Write Back:** In this mode, it is sometimes useful to save the new address in a register. To indicate that this effective address is being written back, add an exclamation mark (!) at the end of the load instruction.
   c. **Post-Indexed Addressing:** This mode is identical to Pre-Indexed Addressing with Write back. But, the address is reformed and saved only after the load/store operation.

d. **Program Counter Relative Addressing:** This mode allows the ARM architecture designers to address memory relative to the Program Counter (r15).

II. **MIPS:**MIPS have only a small number of ways that is computes addresses in memory. The address can be an address of an instruction (for branch and jump instructions) or it can be an address of data (for load and store instructions).

a. **Register Addressing:** This is used in the jr (jump register) instruction.

b. **Immediate Addressing:**This mode does not access memory and thus is relatively faster than other modes. The immediate is of size equal to 16-bits.

c. **PC-Relative Addressing:** This is used in the beq and bne (branch equal, branch not equal) instructions.

d. **Pseudo-direct Addressing:** This is used in the j (jump) instruction.

e. **Base Addressing:** This is used in the lw and sw (load word, store word) instructions.

III. **PowerPC:**The PowerPC processor architecture has only one addressing mode for load and store instructions.

IV. **SPARC:** SPARC supports two addressing modes.

a. The Register indirect with index: This mode computes the effective address by adding the contents of the base register to those of the index register. The effective address cannot be equal to only the base register but the index register could be made equal to zero and by that the effective address will be equal to the base register. E.g.: Ld [%o1], %o2.

b. The Register indirect with immediate: This mode computes the effective address by sign extending the 13-bit immediate to 64 bits and then adds the contents of the base register to it . The effective address could be made equal to the base register by making the constant equal to zero. E.g.: Ld [%o1+30], %o2

Registers: This section covers the different types of register of ARM, MIPS, PowerPC and SPARC.

Architectures	Number of Registers	Classification of Registers
ARM	37 registers/32-bits	Registers are divided into groups: • 31 General-purpose Registers: ✓ Unbanked registers: fromr0 to r7 ✓ Banked registers: from r8to r14 • Status Registers: 1) Current Program StatusRegister (CPSR) 2) the last five are calledsaved program status register (SPSR)
MIPS	32 registers/32-bits	Registers are reserved for special operations. • Two-special purpose registers: Hi/LO: they stock the results ofthe integer multiply and divideinstructions • 30-General Purpose registers:from $0 to $31. ✓ $0: hardwired to zero ✓ $31: link registers. ✓ $29: stack pointer.
POWERPC	101 register/32-bits	Registers are divided into groups: • 32(0-31) General Purpose Registers (GPRs or rX) • 32 Floating point registers (FPRs or fX) • Special Purpose registers (SPRs) ✓ Program counter PC or IAR (instruction address register) ✓ Link register (LR) which can hold the address of a procedure for branch instructions ✓ Condition register (CR) which has eight (0-7) 4 bit fields holding the result of e.g. a compare instruction ✓ Count register for loops is called CTR ✓ XER is the fixed-point exception register ✓ FPSCR is the floating point status and control register ✓ Vector Registers (AltiVec specific) (v0–v31)
SPARC	37 registers/32-bits	Registers are divided into four groups: • In Registers: from %i0 to %i7. • Global Registers: from %g0to %g7. %g0 is alwayshardwired to zero. • Local Registers: from %l0 to%l7. They are user freely inany code. • Out Registers: from %o0 to%o7

Operating Modes: In this section different operating modes for four different ISAs architecture are cover. Each operating mode is allowed to access certain register and to use certain instruction.

I. ARM:

The ARM has seven basic operating modes:

i. User : unprivileged mode under which most tasks run

ii. FIQ : entered when a high priority (fast) interrupt is raised

iii. IRQ : entered when a low priority (normal) interrupt is raised
iv. Supervisor : entered on reset and when a Software Interrupt instruction is executed
v. Abort : used to handle memory access violations
vi. Undef : used to handle undefined instructions

ARM Architecture Version 4 adds a seventh mode:

i. System : privileged mode using the same registers as user mode

II. MIPS:

MIPS have only two operating modes:

i. Kernel (supervisor): when the status bit is set to 0, the operating mode is switched to the kernel mode and can access and change all registers. This mode has the opportunity over other modes and gets switched to in case of an error, interruption, exception or at power up.
ii. User Mode: when the status bit is 1, the operating mode switches to the user mode. This mode is accessed by users and has a lower privilege than that of the kernel mode. It also prevents different users from interfering with one another.

III. SPARC:

SPARC executes the instructions in only two modes:

i. Supervisor mode: The supervisor mode is used to access the processor state registers, such as the Window Invalid Mask (WIM), and the input/output devices. Also, in the supervisor mode, there is a complete access to the memory and its system tables making it privileged in almost all architectures.
ii. User mode: The User mode is used to write to and read from the processor state register and has a limited access to the memory since a load or a store instruction cannot be executed in it.

Conclusion:

The computer world is changing at a rapid pace. The demands of the software world are forcing the computer architectures to change the technology according to the software requirements. This paper was written to compare the four RISC architectures and highlights some of the key differences in ARM, MIPS, PowerPC and the SPARC architectures that will help the reader in selection of a better architecture for the required task.

References:

[1]. **Sarah El Kady, Mai Khater, and MerihanAlhafnawi. MIPS, ARM and SPARC- an Architecture Comparison. 2014**

[2]. **C.Corporation,BestPracticesForImprovingApplicationPerformance and Lowering Cost by Managing MIPS., 2012**

[3]. **L. Kwiatkowski and C. Verhoef, Reducing operational costs through MIPS management. Department of Computer Science, VrijeUniver- siteit Amsterdam, 2012.**

[4]. **O.CORPORATION,ORACLESPARC 25YearsofSPARCInnovation., 2014.**

[5]. Khan, F., & Nakagawa, K. (2013). Comparative study of spectrum sensing techniques in cognitive radio networks. In *Computer and Information Technology (WCCIT), 2013 World Congress on* (pp. 1-8). IEEE.

[6]. Khan, F., Bashir, F., & Nakagawa, K. (2012). Dual head clustering scheme in wireless sensor networks. In *Emerging Technologies (ICET), 2012 International Conference on* (pp. 1-5). IEEE.

[7]. M. A. Jan, P. Nanda, X. He, and R. P. Liu, "A Lightweight Mutual Authentication Scheme for IoT Objects," *Future Generation Computer Systems*

(FGCS), "Submitted", 2016.

[8]. Khan, F., Kamal, S. A., &Arif, F. (2013). Fairness improvement in long chain multihop wireless ad hoc networks. In *2013 International Conference on Connected Vehicles and Expo (ICCVE)* (pp. 556-561). IEEE.

[9]. Khan, F. (2014). Secure communication and routing architecture in wireless sensor networks. In *2014 IEEE 3rd Global Conference on Consumer Electronics (GCCE)* (pp. 647-650). IEEE.

[10]. M. A. Jan, P. Nanda, X. He and R. P. Liu, "PASCCC: Priority-based application-specific congestion control clustering protocol" Computer Networks, Vol. 74, PP-92-102, 2014.

[11]. Khan, S., & Khan, F. (2015). Delay and Throughput Improvement in Wireless Sensor and Actor Networks. In *5th National Symposium on Information Technology: Towards New Smart World (NSITNSW)* (pp. 1-8).

[12]. Khan, F., Jan, S. R., Tahir, M., Khan, S., &Ullah, F. (2016). Survey: Dealing Non-Functional Requirements at Architecture Level. *VFAST Transactions on Software Engineering*, *9*(2), 7-13.

[13]. Khan, F., & Nakagawa, K. (2012). Performance Improvement in Cognitive Radio Sensor Networks. *the IEICE Japan.*

[14]. Khan, F., Khan, S., & Khan, S. A. (2015, October). Performance improvement in wireless sensor and actor networks based on actor repositioning. In *2015 International Conference on Connected Vehicles and Expo (ICCVE)* (pp. 134-139). IEEE.

[15]. M. A. Jan, P. Nanda, X. He and R. P. Liu, "A Sybil Attack Detection Scheme for a Centralized Clustering-based Hierarchical Network" in Trustcom/BigDataSE/ISPA, Vol.1, PP-318-325, 2015, IEEE.

[16]. Jabeen, Q., Khan, F., Khan, S., & Jan, M. A. (2016). Performance Improvement in Multihop Wireless Mobile Adhoc Networks. *the Journal Applied, Environmental, and Biological Sciences (JAEBS)*, *6(4S)*, 82-92.

[17]. Khan, F. (2014, May). Fairness and throughput improvement in multihop wireless ad hoc networks. In *Electrical and Computer Engineering (CCECE), 2014 IEEE 27th Canadian Conference on* (pp. 1-6). IEEE.

[18]. Khan, S., Khan, F., Arif, F., Q., Jan, M. A., & Khan, S. A. (2016). Performance Improvement in Wireless Sensor and Actor Networks. *Journal of Applied Environmental and Biological Sciences*, *6(4S)*, 191-200.

[19]. Khan, F., & Nakagawa, K. (2012). B-8-10 Cooperative Spectrum Sensing Techniques in Cognitive Radio Networks. *電子情報通信学会ソサイエティ大会講演論文集*, *2012*(2), 152.

[20]. M. A. Jan, P. Nanda, X. He, and R. P. Liu, "A Lightweight Mutual Authentication Scheme for IoT Objects," *Elsevier Future Generation Computer Systems (FGCS)*, "Submitted", 2016.

[21]. Khan, F., Jan, S. R., Tahir, M., & Khan, S. (2015, October). Applications, limitations, and improvements in visible light communication systems. In*2015 International Conference on Connected Vehicles and Expo (ICCVE)*(pp. 259-262). IEEE.

[22]. Jabeen, Q., Khan, F., Hayat, M. N., Khan, H., Jan, S. R., &Ullah, F. (2016). A Survey: Embedded Systems Supporting By Different Operating Systems. *International Journal of Scientific Research in Science, Engineering and Technology (IJSRSET), Print ISSN*, 2395-1990.

[23]. Jan, S. R., Ullah, F., Ali, H., & Khan, F. (2016). Enhanced and Effective Learning through Mobile Learning an Insight into Students Perception of Mobile Learning at University Level. *International Journal of Scientific Research in Science, Engineering and Technology (IJSRSET), Print ISSN*, 2395-1990.

[24]. Jan, S. R., Khan, F., &Zaman, A. The perception of students about mobile learning at University level.

[25]. M. A. Jan, P. Nanda, X. He, and R. P. Liu, "A Sybil Attack Detection Scheme for a Forest Wildfire Monitoring Application," *Elsevier Future Generation Computer Systems (FGCS)*, "Accepted", 2016.

[26]. Jan, S. R., Shah, S. T. U., Johar, Z. U., Shah, Y., & Khan, F. (2016). An Innovative Approach to Investigate Various Software Testing Techniques and Strategies. *International Journal of Scientific Research in Science, Engineering and Technology (IJSRSET), Print ISSN*, 2395-1990.

[27]. Khan, I. A., Safdar, M., Ullah, F., Jan, S. R., Khan, F., & Shah, S. (2016). Request-Response Interaction Model in Constrained Networks. *In International Journal of Advance Research and Innovative Ideas in Education, Online ISSN-2395-4396*

[28]. Azeem, N., Ahmad, I., Jan, S. R., Tahir, M., Ullah, F., & Khan, F. (2016). A New Robust Video Watermarking Technique Using H. 264/AAC Codec Luma Components Based On DCT. *In International Journal of Advance Research and Innovative Ideas in Education, Online ISSN-2395-4396*

[29]. Jan, S. R., Khan, F., Ullah, F., Azim, N., &Tahir, M. (2016). Using CoAP Protocol for Resource Observation in IoT. *International Journal of Emerging Technology in Computer Science & Electronics, ISSN: 0976-1353*

[30]. Azim, N., Majid, A., Khan, F., Jan, S. R., Tahir, M., &Jabeen, Q. (2016). People Factors in Agile Software Development and Project Management. *In International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE)* ISSN: 0976-1353

[31]. Azim, N., Majid, A., Khan, F., Tahir, M., Safdar, M., &Jabeen, Q. (2016). Routing of Mobile Hosts in Adhoc Networks. *In International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE)* ISSN: 0976-1353.

[32]. *Azim, N., Khan, A., Khan, F., Majid, A., Jan, S. R., &Tahir, M. (2016) Offsite 2-Way Data Replication toward Improving Data Refresh Performance. In International Journal of Engineering Trends and Applications,* ISSN: 2393 – 9516

[33]. Tahir, M., Khan, F., Jan, S. R., Azim, N., Khan, I. A., &Ullah, F. (2016) EEC: Evaluation of Energy Consumption in Wireless Sensor Networks. . *In International Journal of Engineering Trends and Applications,* ISSN: 2393 – 9516

[34]. Rehman, A. U., Yang, L. L., &Hanzo, L. (2016, May). Performance of Cognitive Hybrid Automatic Repeat reQuest: Go-Back-N. In 2016 IEEE 83rd Vehicular Technology Conference (VTC Spring) (pp. 1-5).IEEE.

[35]. M. A. Jan, P. Nanda, M. Usman, and X. He, "PAWN: A Payload-based mutual Authentication scheme for Wireless Sensor Networks," *Concurrency and Computation: Practice and Experience*, "accepted", 2016.

[36]. Azim, N., Qureshi, Y., Khan, F., Tahir, M., Jan, S. R., &Majid, A. (2016) Offsite One Way Data Replication towards Improving Data Refresh Performance. *In International Journal of Computer Science Trends and Technology,* ISSN: 2347-8578

[37]. Safdar, M., Khan, I. A., Ullah, F., Khan, F., & Jan, S. R. (2016) Comparative Study of Routing Protocols in Mobile Adhoc Networks. *In International Journal of Computer Science Trends and Technology,* ISSN: 2347-8578

[38]. Tahir, M., Khan, F., Babar, M., Arif, F., Khan, F., (2016) Framework for Better Reusability in Component Based Software Engineering.*In the Journal of Applied Environmental and Biological Sciences (JAEBS), 6(4S),* 77-81.

[39]. Khan, S., Babar, M., Khan, F., Arif, F., Tahir, M. (2016). Collaboration Methodology for Integrating Non-Functional Requirements in Architecture. *In the Journal of Applied Environmental and Biological Sciences (JAEBS), 6(4S),* 63-67

[40]. Rehman, Ateeq Ur, Lie-Liang Yang, and LajosHanzo. "Performance of Cognitive Hybrid Automatic Repeat reQuest: Stop-and-Wait." *2015 IEEE 81st Vehicular Technology Conference (VTC Spring)*.IEEE, 2015.

[41]. Jan, S.R., Ullah, F., Khan, F., Azim, N., Tahir, M., Khan, S., Safdar, M. (2016). Applications and Challenges Faced by Internet of Things- A Survey. *In the International Journal of Engineering*

Trends and Applications,ISSN: 2393 – 9516

[42]. Tahir, M., Khan, F., Jan, S.R., Khan, I.A., Azim, N. (2016). Inter-Relationship between Energy Efficient Routing and Secure Communication in WSN. *In International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE)* ISSN: 0976-1353.

[43]. J.Bae,ImaginationTechnologiesbringsMIPSArchitecturetothefore., 2013.