



# **Indoor Light Simulation and Performance Analysis of CsPbBr<sub>3</sub> Perovskite Solar Cells**

Research Project (Forschungsarbeit)

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## Abstract

This work presents an integrated numerical–experimental investigation of  $\text{CsPbBr}_3$  perovskite solar cells optimized for indoor photovoltaic applications. Using SCAPS-1D simulations and controlled low-light measurements, two device architectures—a dual-layer ETL design ( $\text{c-TiO}_2/\text{SnO}_2$ ) and an ETL-free configuration—were evaluated under 2700 K, 4000 K, and AM1.5G (1-Sun) illumination. Parametric simulations reveal that absorber acceptor density, ETL donor density, interfacial defect density, and shunt resistance govern the balance between charge extraction and recombination, with interface traps and leakage pathways emerging as the dominant efficiency-limiting mechanisms. Experimental results corroborate these trends, showing that ETL-integrated devices annealed at 300°C with a 30 nm ETL achieve the most stable and highest-performing configuration, while ETL-free devices exhibit optimal performance at a lower annealing temperature of 250°C. The 250°C condition yields the highest  $J_{\text{sc}}$ , FF, and PCE, whereas  $V_{\text{oc}}$  reaches its maximum at 350°C, reflecting the distinct thermal sensitivities of current extraction and voltage preservation in ETL-free architectures.

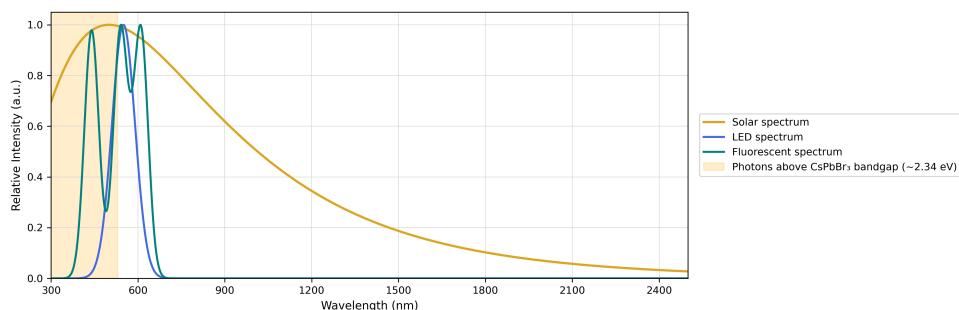
Under 4000 K, 1000 lux illumination,  $\text{CsPbBr}_3$  devices deliver 35–38% PCE experimentally and up to 43.86% in SCAPS simulations, outperforming their AM1.5G (1-Sun) efficiencies. The strong spectral alignment of the 2.34 eV bandgap with indoor LED emission enables operation near the radiative limit, yielding high voltages, suppressed non-radiative losses, and enhanced indoor-specific performance. These findings establish  $\text{CsPbBr}_3$  as a highly promising platform for autonomous indoor energy harvesting and provide a physics-based framework for optimizing wide-bandgap perovskites for low-intensity environments.

# 1 Introduction

Perovskite solar cells (PSCs) have emerged as a transformative photovoltaic technology because of their exceptional power conversion efficiencies (PCEs), low-temperature fabrication methods, and compatibility with flexible substrates. With reported outdoor efficiencies approaching 26% under standard AM1.5G (1-Sun) illumination, PSCs are increasingly seen as viable alternatives to conventional crystalline silicon photovoltaics [1]. However, beyond outdoor deployment, PSCs offer unique advantages for indoor photovoltaic (IPV) applications, where conventional solar technologies are fundamentally limited by the spectral and intensity characteristics of artificial lighting.

Indoor environments present a compelling application space driven by the growing demand for distributed power sources in smart buildings, Internet-of-Things (IoT) sensors, wireless modules, and autonomous devices. Notably, the global smart building market is projected to grow from 103 billion USD in 2024 to over 827 billion USD by 2034, underscoring the increasing relevance of IPV integration in next-generation energy systems [2]. These systems typically operate at mW power levels and could be continuously powered by ambient light, eliminating the need for frequent battery replacement or cumbersome wiring. As such, high-performance IPV technologies could enable more sustainable, maintenance-free electronics while reducing electronic waste and improving energy efficiency in modern infrastructure [2]. Their integration into smart infrastructure enables maintenance-free electronics and supports long-term environmental goals.

However, the indoor photovoltaic environment is fundamentally different from outdoor conditions. Indoor lighting typically ranges between 100 and 500 lux and exhibits narrow spectral profiles, with peak emission wavelengths centered between 400 and 700 nanometers (nm) depending on the source (e.g., fluorescent, LED) [1]. In contrast, sunlight spans a much broader spectrum, from approximately 300 to 2500 nm, encompassing ultraviolet, visible, and infrared light [2]. This contrast is visualized in Figure 1.1. Conventional silicon cells, with a 1.12 electron volt (eV) band gap, are mismatched to this spectrum and suffer from low photon absorption and poor efficiency under low-irradiance conditions [3]. In contrast, PSCs have tunable band gaps from 1.8 to 2.4 eV and superior absorption coefficients in the visible range (400-700 nm) [4], which makes them well suited for harvesting energy from indoor light sources.



*Figure 1.1: Spectral Comparison of Indoor lights (LEDs), and Sunlight*

Despite this spectral compatibility, indoor PSCs face a distinct set of challenges not encountered in outdoor applications. Under low-light conditions, carrier generation is minimal because indoor LED lighting provides 100–1000 times lower irradiance than 1 sun. Although LED spectra are much narrower than sunlight, this does not significantly reduce the usable photon flux because photons below the bandgap are not absorbed anyway. Instead, the inherently low total photon flux under indoor illumination increases the relative influence of non-idealities such as defects, interfacial losses, and energy-level misalignment [5]. In high-irradiance environments,

the abundance of photo-generated carriers can partially mask recombination losses and trap states, which is discussed in more detail in later sections of this study, allowing the device to maintain reasonable performance despite imperfections. However, in low-irradiance settings, such as indoor lighting, the carrier density is lower, so even small recombination pathways or energy barriers can significantly reduce the photocurrent and overall efficiency [5]. This makes defect tolerance, interfacial passivation, and precise energy-level alignment critically important for sustaining charge separation and transport. Materials such as perovskites, which exhibit low trap densities and high defect tolerance, are therefore especially promising for indoor photovoltaics [5] [6]. The adaptation of devices to specific lighting environments can maximize efficiency, although recent studies suggest that optimizing for an average indoor spectrum (typically centered around 1.7 to 2.0 eV) can offer a practical compromise, allowing broad applicability in various indoor settings [2].

Recent advances have demonstrated promising indoor-specific PSC designs, often using simulation-first workflows to optimize device architectures. For example, Huang et al. simulated a single perovskite absorber based on selenium (1.9 eV) using SCAPS-1D software, achieving simulated efficiencies of up to 21%, and 37% under LED lighting [6]. Alanazi et al. demonstrated the potential of hydrogenated double perovskite structure,  $\text{Cs}_2\text{AgBiBr}_6$  PSCs under LED light at 200 lux, achieving simulated PCEs exceeding 40%. This performance was facilitated by defect passivation and optimized conduction band offsets (CBOs) [5]. These findings highlight both the viability of indoor PSCs and the need for rigorous interface and material optimization.

In this study, we focus on  $\text{CsPbBr}_3$ -based perovskites, a wide bandgap (2.34 eV), all-inorganic composition offering high thermal and environmental stability and strong absorption in the visible region [7]. This composition aligns well with the emission spectra of common indoor light sources, particularly warm white LEDs as shown in Figure 1.1. Although  $\text{CsPbBr}_3$  isn't ideal for outdoor solar harvesting due to its limited near-IR absorption, it is better suited for indoor environments where visible light dominates. The higher bandgap allows for improved open-circuit voltages ( $V_{oc}$ ), and its narrow absorption spectrum minimizes thermalization losses that typically degrade performance under broadband illumination like AM1.5G (1-Sun) illumination. In conventional solar cells, thermalization can account for up to 30–35% of total energy loss, especially under broadband solar illumination. Furthermore, transmission losses, where sub-bandgap photons (e.g., NIR) pass through the absorber without generating carriers, can contribute another 15–25% loss, depending on the material and spectrum [2]. Compared to hybrid FA- or MA-based perovskite systems, which are vulnerable to ambient phase degradation and parasitic losses—even when stabilized with cesium and bromide—the all-inorganic  $\text{CsPbBr}_3$  composition offers superior phase stability, minimal hysteresis, and reduced moisture sensitivity [7]. Previous studies have shown that the inclusion of  $\text{Cs}^+$  and  $\text{Br}^-$  ions can partially stabilize  $\text{FAPbI}_3$  [7], but such devices still suffer from elevated series resistance and limited fill factor under low-light conditions. By selecting  $\text{CsPbBr}_3$  as the absorber, this work avoids the volatility of organic cations and takes advantage of a robust perovskite architecture with good photostability [11], suitable energy band alignment for indoor lighting, and low defect density – all critical advantages for reliable indoor photovoltaics.

Here we studied two device architectures as shown in Figure 1.2, based on  $\text{CsPbBr}_3$  perovskite absorbers for indoor photovoltaic applications. The first configuration incorporates a standard base architecture (FTO/c-TiO<sub>2</sub>/SnO<sub>2</sub>/ $\text{CsPbBr}_3$ /Spiro-OMeTAD/Au), designed to enhance electron extraction and suppress interfacial recombination through favorable band alignment between the ETLs and the absorber. The second configuration adopts an ETL-free design (FTO/ $\text{CsPbBr}_3$ /Spiro-OMeTAD/Au), offering a simplified interface and reduced fabrication complexity while relying on the intrinsic electronic properties of  $\text{CsPbBr}_3$  for charge transport.



(a) With ETL

(b) ETL-Free

*Figure 1.2: Comparison of device architectures with and without electron transport layers (ETLs)*

Both architectures utilize Spiro-OMeTAD as the hole transport layer and gold as the back contact, ensuring efficient hole collection and stable operation. By comparing these two structures through simulation, I was able to evaluate the impact of ETL presence on charge carrier dynamics, recombination behavior, and overall device performance under indoor illumination. The findings contribute to the optimization of perovskite solar cells for low-light environments that balance efficiency, stability, and manufacturability.

The standard base configuration (i.e., with ETL) supports high open-circuit voltages ( $V_{oc} > 1.3$  V), strong fill factors, and low recombination losses under indoor spectral conditions, with simulated efficiencies exceeding 30% in recent SCAPS modeling workflows [3]. Its superior band alignment between the perovskite absorber layer (e.g., CsPbBr<sub>3</sub>) and adjacent transport layers, compared to silicon and hybrid perovskites. This optimized alignment minimizes energy barriers for carrier extraction and reduces interfacial recombination, resulting in modest trap-assisted recombination and robust long-term device operation.

To rigorously evaluate and optimize this material system for indoor use, we integrate both numerical simulations and experimental validation. Simulations are carried out using the Solar Cell Capacitance Simulator (SCAPS), a one-dimensional finite element solver developed at the Department of Electronics and Information Systems (ELIS) of the University of Ghent, Belgium. Several researchers have contributed to its development, namely Alex Niemegeers, Marc Burgelman, Koen Decock, Stefaan Degraeve, and Johan Verschraegen [8]. SCAPS solves coupled semiconductor transport equations (Poisson, continuity, and drift-diffusion) across multilayer thin-film structures. This tool allows for detailed parametric control of material properties, including bandgap, mobility, doping levels, defect densities, and interface energetics, providing output such as J-V characteristics, quantum efficiency, and energy band diagrams.

Following the simulation stage, a controlled low-light illumination platform was set up to experimentally characterize the performance of the PSC under conditions that replicate common indoor lighting scenarios. A printed circuit board that hosts a six-cell array of CsPbBr<sub>3</sub>-based perovskites was illuminated using calibrated LED sources at varying lux levels. Measurements of short-circuit current density ( $J_{sc}$ ), open-circuit voltage ( $V_{oc}$ ), fill factor (FF) and power conversion efficiency (PCE) will be used to benchmark real-world performance and

validate simulation results. Experimental characterizations include the **J-V measurements** - to extract electrical performance metrics and validate SCAPS-predicted behavior and **Spectral response analysis of the LEDs** - to compare wavelength-dependent photocurrent generation for LEDs and that of AM1.5G (1-Sun).

The results of both simulation and experimental investigations were systematically compared to identify performance discrepancies and design correlations. By establishing a feedback loop between modeling and measurement, this study contributes to a rigorous methodology for advancing PSCs as viable indoor energy harvesting technologies that support the future of connected and autonomous electronic systems.

## 2 SCAPS Simulation Framework

The Solar Cell Capacitance Simulator (SCAPS), developed at the University of Ghent, is a one-dimensional numerical tool designed to simulate the electrical behavior of thin-film photovoltaic devices. It enables a detailed analysis of multilayer solar cells by solving the fundamental transport equations of semiconductors under various operating conditions [9].

### 2.1 Governing Physical Equations

SCAPS simulates a planar, one-dimensional semiconductor device, typically a thin-film solar cell. The structure consists of multiple layers (e.g., absorber, buffer, window, contact), each with distinct electronic properties. The simulation domain spans the thickness of the device, from the front contact to the back contact. Charge carriers (electrons and holes) are generated by light absorption in the absorber layer. These carriers move under the influence of internal electric fields and concentration gradients. The environment assumes thermal equilibrium or steady-state illumination, depending on the simulation mode [10].

SCAPS models the behavior of charge carriers by solving a set of coupled differential equations that describe electrostatics, carrier transport, and recombination mechanisms at the interfaces as shown in Figure 2.1 [10]:

- **Poisson's Equation** (Figure 2.2)

Poisson's equation is derived from Gauss's law and relates the electrostatic potential to the local charge density. The electrostatic potential  $\psi(x)$  is determined by the spatial distribution of charge density  $\rho(x)$ :

$$\frac{d^2\psi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon} \quad (2.1)$$

where  $\varepsilon$  is the permittivity of the material.

## Coupled Differential Equations

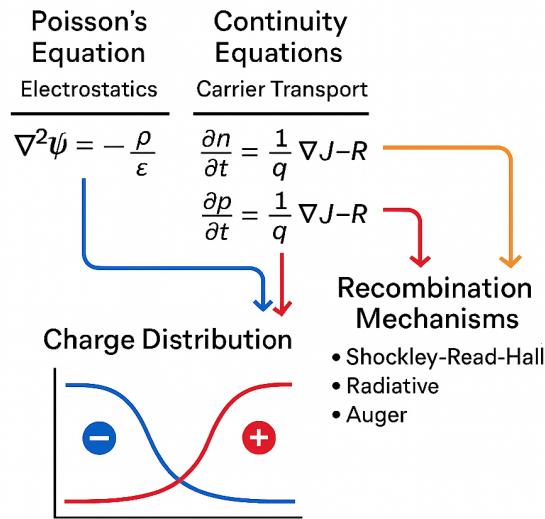


Figure 2.1: Schematic representation of the coupled differential equations solved by SCAPS to model charge carrier behavior in perovskite solar cells

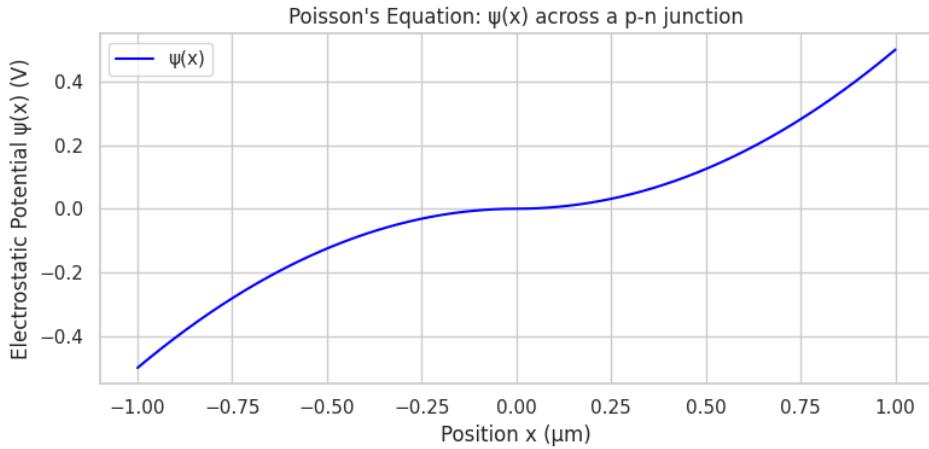


Figure 2.2: Poisson's equation across a p-n junction, showing the total space charge arising from free carriers, ionized dopants, and any fixed or interfacial charges

- **Continuity Equations** (Figure 2.3)

Continuity equation expresses conservation of charge for electrons and holes. The conservation of electron ( $n$ ) and hole ( $p$ ) densities is described by:

$$\frac{dn}{dt} = \frac{1}{q} \frac{dJ_n}{dx} + G_n - R_n \quad (2.2)$$

$$\frac{dp}{dt} = -\frac{1}{q} \frac{dJ_p}{dx} + G_p - R_p \quad (2.3)$$

where  $J_n$  and  $J_p$  are the electron and hole current densities,  $G$  is the generation rate, and  $R$  is the recombination rate.

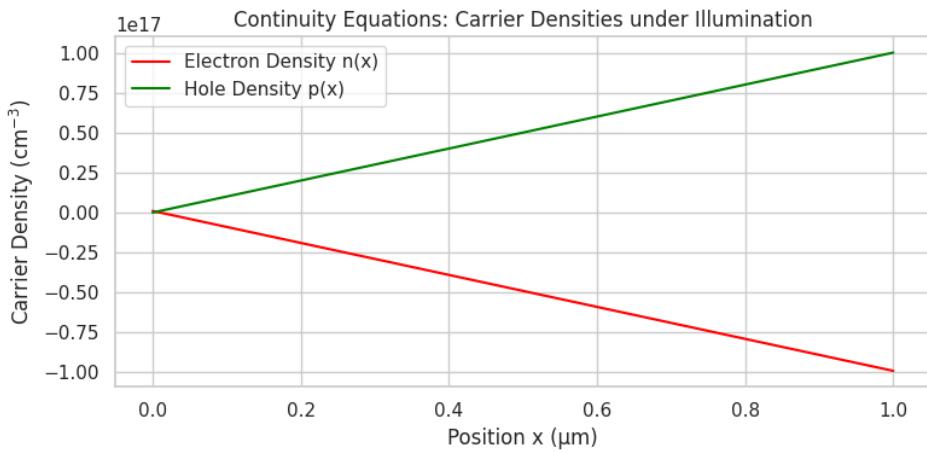


Figure 2.3: Spatial profile of electron and hole densities across a device under illumination, governed by the continuity equations

- **Drift-Diffusion Equations** (Figure 2.4)

Drift-Diffusion equations combine Ohm's law and Fick's law to describe carrier transport. Carrier transport is governed by drift due to electric fields and diffusion due to concentration gradients:

$$J_n = qn\mu_n E(x) + qD_n \frac{dn}{dx} \quad (2.4)$$

$$J_p = qp\mu_p E(x) - qD_p \frac{dp}{dx} \quad (2.5)$$

where  $\mu$  is the carrier mobility,  $D$  is the diffusion coefficient and  $E(x) = -d\psi/dx$  is the electric field obtained using  $\psi$  from equation 2.1 (Poisson's equation). The resulting  $J_n$  and  $J_p$  are then utilized in equation 2.2 and 2.3.

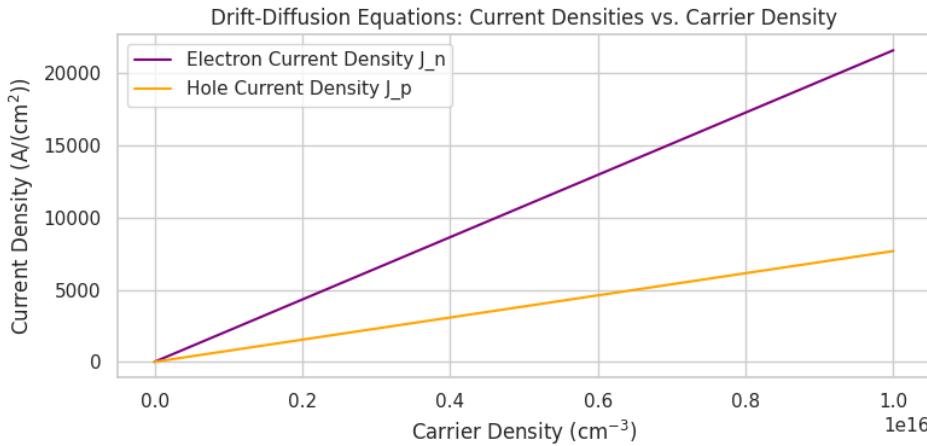


Figure 2.4: Spatial distribution of carrier concentrations and electric field profiles as determined by the Drift-Diffusion equations, balancing carrier movement due to concentration gradients and electric fields

These equations are non-linear and interdependent, requiring iterative numerical techniques for the solution.

## 2.2 Assumptions and Limitations

SCAPS relies on several simplified assumptions:

- One-dimensional geometry: Only vertical transport is considered.
- Classical transport: Quantum effects are neglected.
- Steady-state illumination: Time-dependent effects are excluded unless small-signal AC analysis is used.
- Material uniformity within layers: Properties are assumed to be constant or to vary smoothly.

These assumptions are generally valid for thin-film photovoltaic devices under indoor lighting conditions, which typically involve narrower spectral bands (e.g., peaks from 450 to 650 nm for LEDs) and reduced carrier generation rates, reinforcing the low-injection assumption [9].

## 2.3 Numerical Solution Methodology

SCAPS employs a one-dimensional finite difference method (FDM) to discretize the spatial domain of the solar cell along its thickness. The device is divided into a grid of nodes, each representing a spatial point within a specific material layer [10]. The resolution of the grid can be adjusted to capture fine-scale variations in potential and carrier concentrations, particularly near interfaces and depletion regions.

At each node, the following coupled equations are discretized:

- **Poisson's Equation with Trap Charge:**

$$\frac{d^2\psi(x)}{dx^2} = -\frac{q}{\varepsilon} (p(x) - n(x) + N_D^+(x) - N_A^-(x) + \rho_{\text{trap}}(x)) \quad (2.6)$$

- **Electron and Hole Continuity Equations:**

$$\frac{dn}{dt} = \frac{1}{q} \frac{dJ_n}{dx} + G_n - R_n \quad \text{and} \quad \frac{dp}{dt} = -\frac{1}{q} \frac{dJ_p}{dx} + G_p - R_p \quad (2.7)$$

- **Drift-Diffusion Current Equations:**

$$J_n = qn\mu_n E + qD_n \frac{dn}{dx} \quad \text{and} \quad J_p = qp\mu_p E - qD_p \frac{dp}{dx} \quad (2.8)$$

- **Recombination Models:**

SCAPS supports multiple recombination mechanisms. These are shown in Figure 2.5:

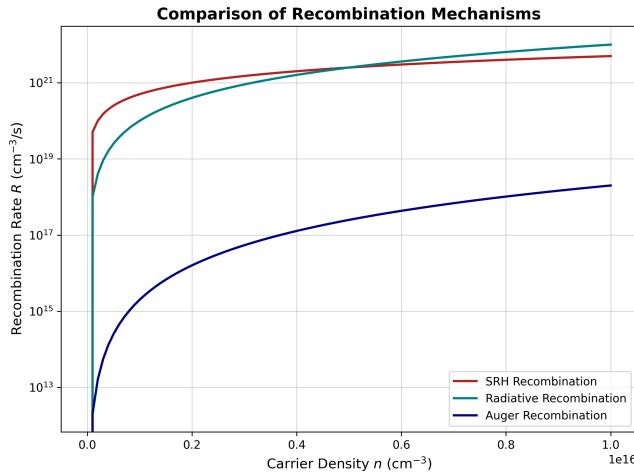


Figure 2.5: Comparison of SRH, Radiative and Auger Recombination mechanisms used in SCAPS

- Shockley-Read-Hall (SRH) recombination:

$$R_{\text{SRH}} = \frac{np - n_i^2}{\tau_p(n + n_i) + \tau_n(p + n_i)} \quad (2.9)$$

- Radiative recombination:

$$R_{\text{rad}} = B(np - n_i^2) \quad (2.10)$$

- Auger recombination:

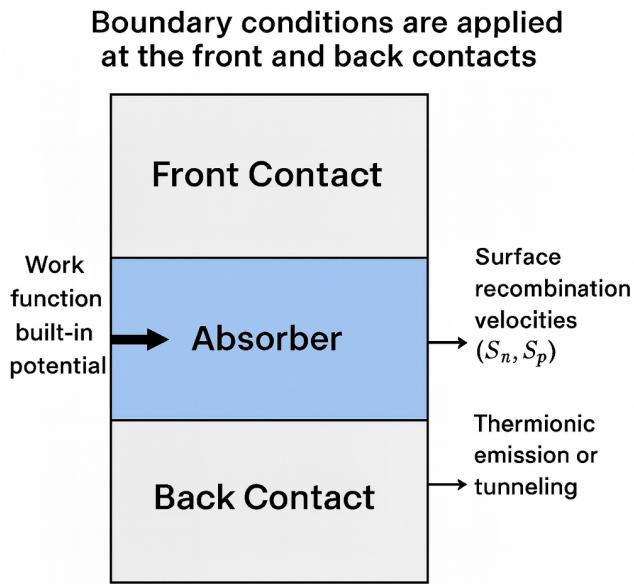
$$R_{\text{Auger}} = C_n n(np - n_i^2) + C_p p(np - n_i^2) \quad (2.11)$$

These equations are non-linear and strongly coupled. SCAPS solves them using a Newton-Raphson iterative scheme:

1. **Initialization:** Initial guesses for  $\psi$ ,  $n$ , and  $p$  are assigned based on equilibrium or previous bias conditions.
2. **Linearization:** The system is linearized around the current guess, forming a Jacobian matrix that relates changes in variables to residuals.
3. **Matrix Solution:** The linear system is solved using direct methods (e.g., LU (Lower-Upper) decomposition) to obtain corrections.
4. **Update and Convergence:** Variables are updated and residuals are evaluated. The iteration continues until the convergence criteria are met (typically  $< 10^{-6}$  relative error).

Boundary conditions are applied at the front and back contacts Figure 2.6. These include:

- Specified work functions or built-in potentials
- Surface recombination velocities ( $S_n$ ,  $S_p$ )
- Thermionic emission



*Figure 2.6: Schematic of a semiconductor stack showing the boundary conditions at the front and back contacts, including work function, surface recombination velocities, and carrier transport mechanisms*

SCAPS also supports simulation under steady-state and small-signal AC conditions. For capacitance analysis, the equations are linearized with respect to a small perturbation voltage and solved in the frequency domain.

To enhance numerical stability, SCAPS may apply damping factors in Newton-Raphson updates and adaptive mesh refinement near regions of steep gradients (e.g., depletion edges or heterojunctions). The simulator is robust in a wide range of material systems, including amorphous, polycrystalline, and heterostructure devices.

### 3 PSC device architecture

In this study, two distinct device architectures that employ  $\text{CsPbBr}_3$  perovskite absorbers for indoor photovoltaic applications were investigated. The first design integrates a dual-layer electron transport structure (FTO / c-TiO<sub>2</sub> / SnO<sub>2</sub> /  $\text{CsPbBr}_3$  / Spiro-OMeTAD / Au), which leverages favorable band alignment to promote efficient electron extraction and mitigate interfacial recombination. The second configuration completely eliminates the electron transport layers (FTO /  $\text{CsPbBr}_3$  / Spiro-OMeTAD / Au), streamlining the device structure and relying on the inherent electronic properties of  $\text{CsPbBr}_3$  to facilitate charge transport [4][11].

Both systems incorporate Spiro-OMeTAD as the hole transport layer and silver as the rear electrode, ensuring effective hole collection and operational stability [12]. Through comparative simulation, this work aims to assess how the presence or absence of ETLs influences carrier dynamics, recombination pathways, and overall device performance under indoor lighting conditions [8]. The results offer valuable insight into the optimization of perovskite solar cells for low-irradiance environments, balancing power conversion efficiency with structural simplicity and long-term reliability [1].

### 3.1 Device Architectures: With and Without ETL

This section details the two device architectures as discussed previously. Figure 1.2 illustrates the layer arrangements for both cases.

#### Common Layers and Functions

- **FTO (Fluorine-doped Tin Oxide):** Transparent front electrode enabling photon transmission and electron collection. In ETL-free devices, direct contact with the absorber requires careful interface engineering to suppress recombination.
- **CsPbBr<sub>3</sub> (Cesium Lead Bromide):** Fully inorganic perovskite absorber with high photoluminescence quantum yield, thermal stability, and visible-range absorption. In ETL-free designs, it also facilitates electron transport due to its intrinsic mobility.
- **Spiro-OMeTAD:** Organic hole transport layer with favorable energy alignment for efficient hole extraction and transport. It also contributes to interface passivation and device stability.
- **Au (Gold):** Back contact with large work function, promoting hole collection and long-term chemical stability.

#### ETL-Enhanced Architecture (Case 1)

This configuration introduces a bilayer ETL stack to improve electron extraction and suppress recombination:

- **c-TiO<sub>2</sub>** (compact Titanium Oxide): Primary ETL with wide bandgap and favorable conduction band alignment. It selectively extracts electrons and blocks holes [13].
- **SnO<sub>2</sub>**(Tin Oxide): Secondary ETL offering higher electron mobility and reduced hysteresis. It forms an energetic cascade with c-TiO<sub>2</sub> and improves interface quality with CsPbBr<sub>3</sub> [3].

#### ETL-Free Architecture (Case 2)

This simplified structure omits ETLs, relying on the intrinsic properties of CsPbBr<sub>3</sub> for charge generation and transport. It reduces fabrication complexity and is well-suited for indoor photovoltaic applications.

The initial input parameters for ETL, absorber, and HTL materials used in both configurations are summarized in Table 4.1.

## 4 Experimental Design and Method

This section outlines the methodology employed for both simulation and experimental investigations of two perovskite solar cell (PSC) configurations: one incorporating dual-layer ETL and one without any ETL. The study begins with a numerical simulation using SCAPS, followed by experimental validation. Comparative analysis of the results enables a comprehensive understanding of the impact of the ETL on device performance.

## 4.1 Importance of J-V curves in the analysis of PSC

J-V (current density-voltage) curves are the cornerstone of evaluating PSC performance, offering a direct window into how efficiently a device converts sunlight into electricity. From these curves, researchers extract critical parameters such as short-circuit current density ( $J_{sc}$ ), open-circuit voltage ( $V_{oc}$ ), fill factor (FF), and power conversion efficiency (PCE). Each of these metrics reflects a different aspect of the cell's operation and helps diagnose performance bottlenecks and guide optimization strategies. An example of the J-V curve is shown in Figure 4.1.

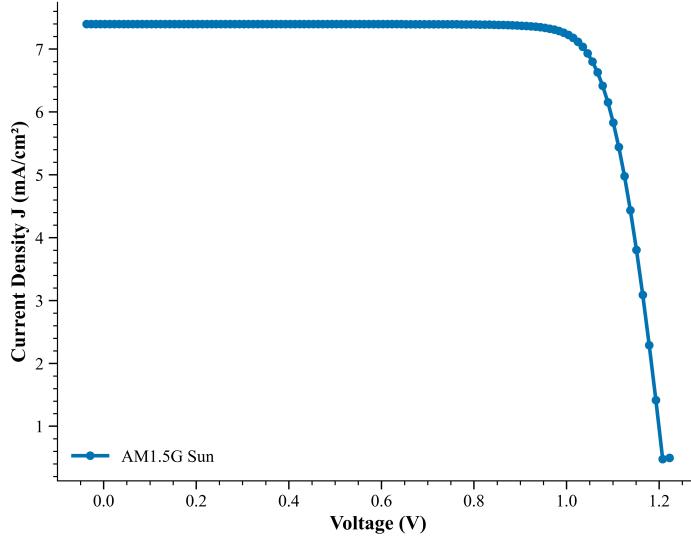


Figure 4.1: An example of a J-V Curve for AM1.5G (1-Sun)

- Short-Circuit Current Density ( $J_{sc}$ ): The short-circuit current density ( $J_{sc}$ ) is the current per unit area generated by the solar cell when the voltage across the device is zero. It reflects the cell's ability to absorb light and generate charge carriers. A high  $J_{sc}$  indicates efficient photon absorption and effective charge generation and collection. The factors influencing  $J_{sc}$ , spectrum and intensity include the optical properties of the active layer, charge transport layers, and the overall device architecture.
- Open-Circuit Voltage ( $V_{oc}$ ): The open-circuit voltage ( $V_{oc}$ ) is the maximum voltage the solar cell can produce when there is no external load connected (i.e., zero current). It is primarily determined by the difference in energy levels between the electron donor and acceptor materials and is influenced by recombination losses. A higher  $V_{oc}$  suggests lower recombination rates and better energy alignment across the device layers, contributing to higher overall efficiency [14].
- Fill Factor (FF): The fill factor (FF) is calculated as the ratio of the maximum power output ( $J_{mp} \cdot V_{mp}$ ) to the theoretical maximum ( $J_{sc} \cdot V_{oc}$ ):

$$FF = \frac{J_{mp} \cdot V_{mp}}{J_{sc} \cdot V_{oc}} \quad (4.1)$$

A high FF suggests minimal resistive losses and efficient charge extraction, while a low FF may point to issues like poor contact quality or recombination losses [14]. This makes FF a vital diagnostic tool for identifying internal inefficiencies that might not be apparent from  $J_{sc}$  or  $V_{oc}$  alone.

- Power Conversion Efficiency (PCE): Power Conversion Efficiency (PCE) ties all these parameters together

into a single figure of merit. It is calculated using the formula:

$$\text{PCE} = \frac{J_{\text{sc}} \cdot V_{\text{oc}} \cdot \text{FF}}{P_{\text{in}}} = \frac{P_{\text{out}}}{P_{\text{in}}} \quad (4.2)$$

where  $P_{\text{in}}$  is the incident light power density and  $P_{\text{out}}$  is the output power density. PCE reflects the overall effectiveness of the solar cell in converting light to electrical energy. A high PCE signals optimized absorption and charge transport, while a low PCE highlights loss pathways. Interpreting these values relative to the Shockley–Queisser limit is crucial: under AM1.5G (1-Sun) the theoretical maximum is 33%, whereas under indoor LED spectra the limit can exceed 50–60% for wide-bandgap absorbers [14].

Together, these metrics derived from J-V curves form a comprehensive framework for diagnosing, comparing, and improving PSCs. They not only quantify performance but also guide material selection, interface engineering, and fabrication strategies. Whether identifying resistive losses, recombination pathways, or dynamic instabilities, J-V curve analysis remains an indispensable tool in the advancement of high-efficiency perovskite solar technologies.

## 4.2 PSC Model Configuration and SCAPS Simulation Setup

The SCAPS simulation was performed to evaluate two perovskite solar cell (PSC) architectures: Case 1, incorporating an electron transport layer (ETL) (FTO / c-TiO<sub>2</sub> / SnO<sub>2</sub> / CsPbBr<sub>3</sub> / Spiro-OMeTAD / Au), and Case 2, an ETL-free configuration (FTO / CsPbBr<sub>3</sub> / Spiro-OMeTAD / Au). Constant thicknesses were used and held constant across both cases to ensure consistency. The initial material parameters for each layer including bandgap, electron affinity, dielectric constant, carrier mobilities, and doping concentrations were selected based on previously published literature and are summarized in Table 4.1.

Parameters	FTO	c-TiO <sub>2</sub>	ETL (SnO <sub>2</sub> )	CsPbBr <sub>3</sub>	HTL (Spiro-OMeTAD)
Thickness (nm)	400	30	30	500	200
Bandgap (eV)	3.5 [7]	3.2 [15]	3.5 [7]	2.34 [4]	3.0 [7]
e <sup>-</sup> affinity (eV)	4.0 [7]	4.1 [16]	4.0 [7]	4.0 [4]	2.2 [7]
Permittivity (relative)	9.0 [7]	9.0 [6]	9.0 [7]	10 [17]	3.0 [7]
Effective density of states at CB (cm <sup>-3</sup> )	2.2 x 10 <sup>18</sup> [7]	2.5 x 10 <sup>18</sup> [6]	2.2 x 10 <sup>18</sup> [5]	2.2 x 10 <sup>18</sup> [18]	2.2 x 10 <sup>18</sup> [7]
Effective density of states at VB (cm <sup>-3</sup> )	2.2 x 10 <sup>18</sup>	2.5 x 10 <sup>19</sup> [6]	1.8 x 10 <sup>19</sup> [5]	1.8 x 10 <sup>18</sup> [18]	1.8 x 10 <sup>19</sup> [7]
e <sup>-</sup> thermal velocity (cm·s <sup>-1</sup> )	1 x 10 <sup>7</sup>	1 x 10 <sup>7</sup>	1 x 10 <sup>7</sup>	1.1 x 10 <sup>7</sup> [4]	1 x 10 <sup>7</sup>
h <sup>+</sup> thermal velocity (cm·s <sup>-1</sup> )	1 x 10 <sup>7</sup> [7]	1 x 10 <sup>7</sup>	1 x 10 <sup>7</sup>	9.5 x 10 <sup>6</sup> [4]	1 x 10 <sup>7</sup>
Mobility of e <sup>-</sup> (cm <sup>2</sup> /V·s)	20 [7]	0.1 [16]	240 [5]	5 [19]	2 x 10 <sup>-4</sup> [7]
Mobility of h <sup>+</sup> (cm <sup>2</sup> /V·s)	10 [7]	10 <sup>-5</sup> [15]	25 [5]	5 [19]	2 x 10 <sup>-4</sup> [7]
Density of n-type doping (cm <sup>-3</sup> )	1 x 10 <sup>15</sup> [7]	1 x 10 <sup>17</sup> [16]	2 x 10 <sup>19</sup> [5]	0	0
Density of p-type doping (cm <sup>-3</sup> )	0	0	0	1 x 10 <sup>15</sup> [20]	1 x 10 <sup>19</sup> [7]
Density of defects (cm <sup>-3</sup> )	10 <sup>18</sup> [7]	10 <sup>15</sup> [6]	10 <sup>18</sup> [7]	1 x 10 <sup>12</sup> [20]	10 <sup>15</sup> [7]

Table 4.1: Initial material parameters used in simulation

Simulations were conducted under three LED illumination conditions with color temperatures of 2700 K (warm white) and 4000 K (neutral white) and AM1.5G (1-Sun). The spectral profiles of these sources were imported into SCAPS using .spe files. The absorption spectrum of the CsPbBr<sub>3</sub> absorber layer was loaded via a .abs file. Light was incident on the front (left) contact, and the voltage bias applied to the back (right) contact. The simulation temperature was set to 300 K.

To evaluate performance under low-light conditions, simulations were carried out at two illumination intensities: 1000 lux and 200 lux (representative of indoor or low-light environments). This dual-intensity approach enabled assessment of the PSCs' light-harvesting capabilities across a broader range of real-world scenarios.

The voltage sweep for J-V analysis ranged from -0.2 to 1.4 V with a step size of 0.01 V. Contact work functions

were defined to ensure appropriate band alignment and were modeled as ideal ohmic contacts. Interface recombination velocities and defect densities were included to simulate realistic interfacial behavior. Series resistance ( $R_s$ ) and shunt resistance ( $R_{sh}$ ) were varied systematically to study their impact on device performance.

The simulation outputs include J-V. From the J-V curves, key performance metrics— $V_{oc}$ ,  $J_{sc}$ , FF, and PCE—were extracted. These metrics were used to assess the influence of the device and material parameters and illumination intensity on overall device efficiency. Schematics of the two PSC configurations used in SCAPS are presented in Figure 4.2 and Figure 4.3.

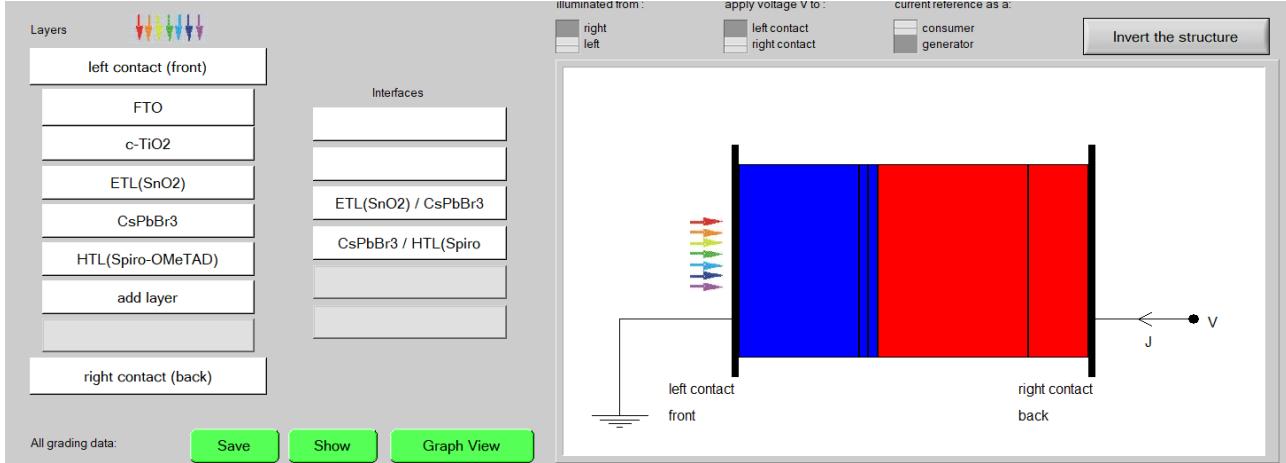


Figure 4.2: SCAPS model for Case 1: With ETL

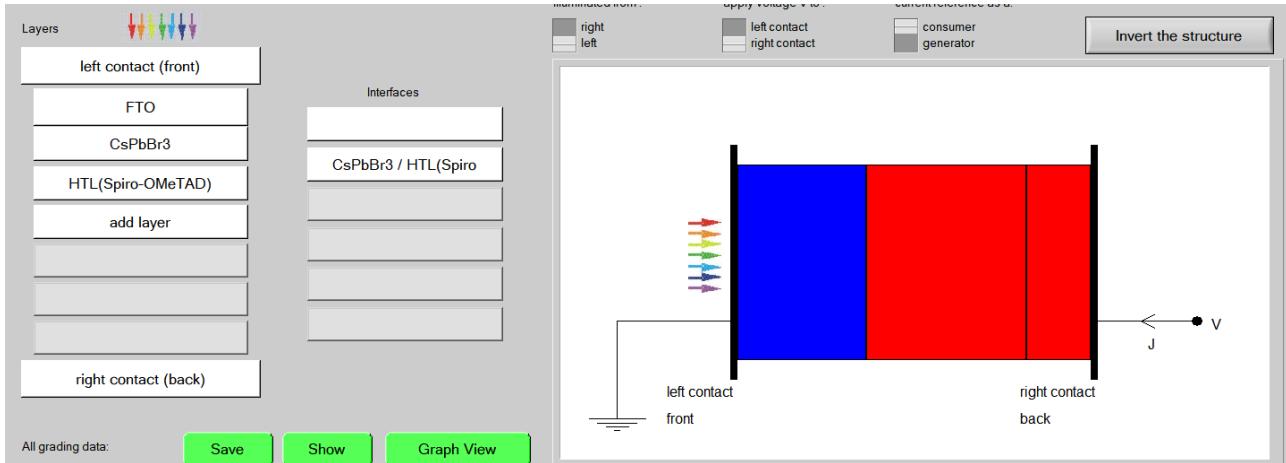
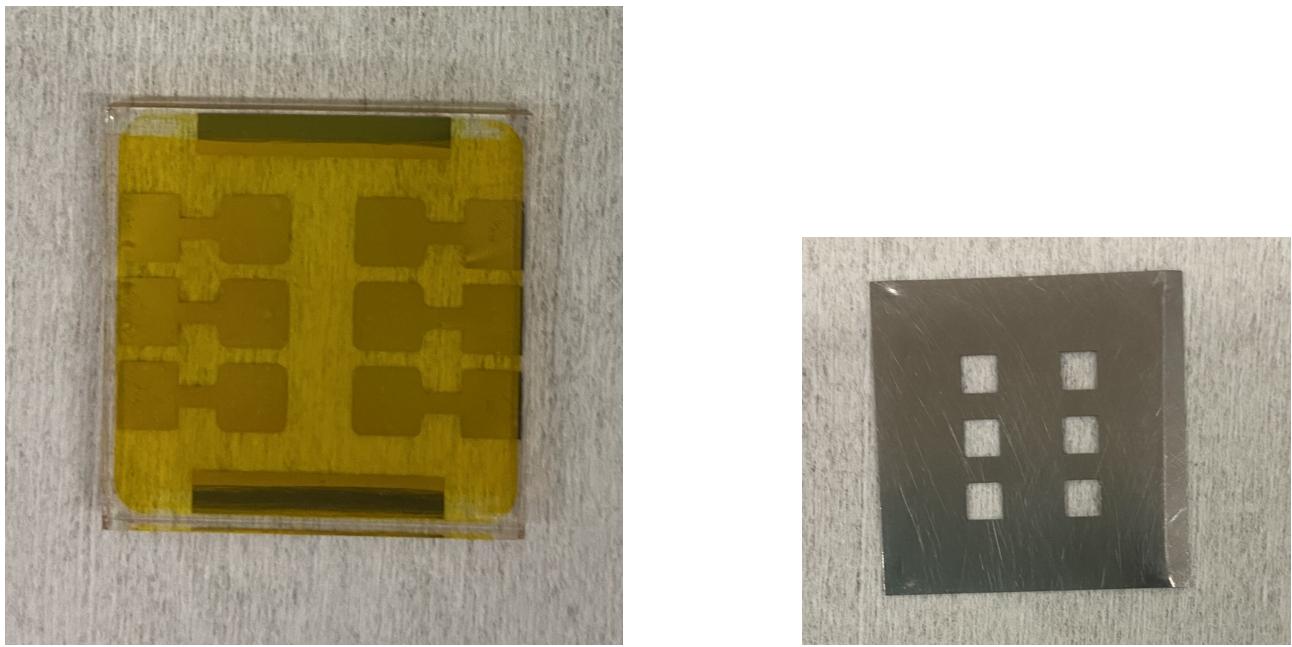


Figure 4.3: SCAPS model for Case 2: ETL-free

### 4.3 Experimental Setup

The performance of both PSC architectures was evaluated under controlled illumination using two distinct setups: LED lamps for indoor lighting conditions and a solar simulator for AM1.5G (1-Sun) reference measurements. The PSC sample is as shown in Figure 4.4(a). Two fabrication batches were tested to enable a statistical evaluation of the cells' performance.



(a) Glass substrate containing 6 Perovskite Solar Cells

(b) Shadow mask to define active cell area

Figure 4.4: *CsPbBr<sub>3</sub>* Perovskite Solar Cell and Shadow Mask

#### 4.3.1 LED Illumination Setup

Commercial LED bulbs with color temperatures of 2700 K and 4000 K were employed to measure cell performance under indoor lighting. The details on the LEDs used are given in Table 4.2. The spectrum of the LEDs are given in Figure 4.5.

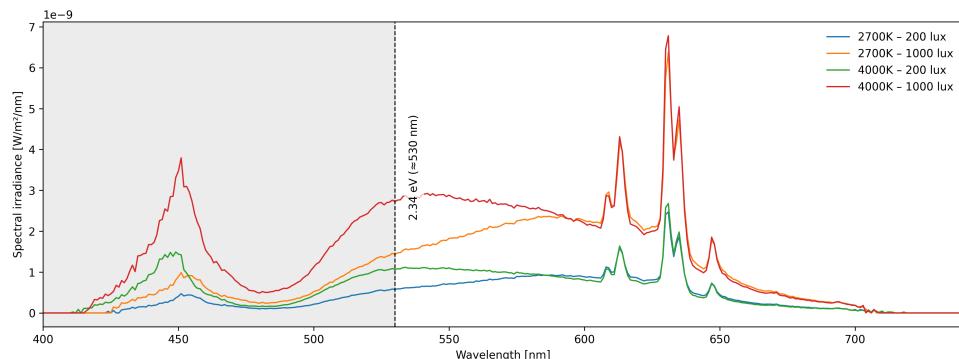


Figure 4.5: Spectrum of the LEDs

Color Temperature	Lumen (lm)	On-Mode Power (W)	Model
2700K	1535 <sup>1</sup>	7.3	PHILIPS 9290036251
	485 <sup>1</sup>	2.3	PHILIPS 9290036262
4000 K	1535 <sup>1</sup>	7.3	PHILIPS 9290036257
	485 <sup>1</sup>	2.3	PHILIPS 9290036265

Table 4.2: Power Rating, light intensity and commercial model information of the LED lamps used in this study

Each condition was tested at two intensities: 1000 lux<sup>1</sup>(representing typical indoor lighting) and 200 lux<sup>1</sup> (representing low-light environments). The bulbs were mounted on a height-adjustable lamp and positioned at a fixed distance of 23 cm above the sample holder to match the desired intensity, measuring the distance with an everyday use scale-measure, to ensure uniform illumination across the active area as shown in Figure 4.6. Ambient light was minimized to avoid interference.



Figure 4.6: LED illumination setup

#### 4.3.2 Illumination Conditions and Irradiance Equivalents:

The following irradiance values were applied during measurements. Figure 4.7 shows the power intensity comparison between AM1.5G (1 Sun) and the LEDs.

<sup>1</sup>In the desk-environment test setup (illuminated area approx. 3 m<sup>2</sup>), a lamp output of 1535 lm corresponds to roughly 1000 lux, while 485 lm corresponds to about 200 lux.

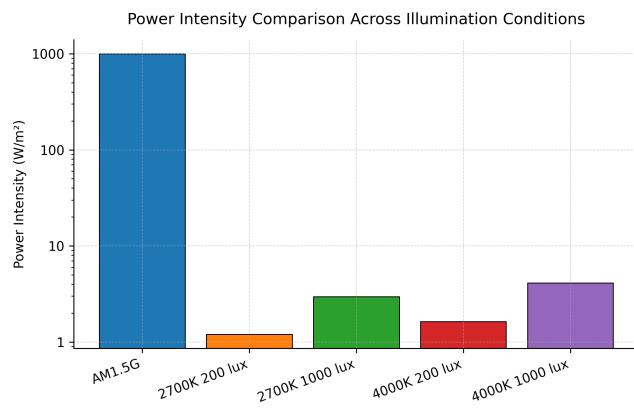


Figure 4.7: Power Intensity Comparison across 1-Sun and LED illumination conditions

- AM1.5G (1-Sun): 1000 W/m<sup>2</sup>
- 2700 K, 200 lux: 1.202 W/m<sup>2</sup>
- 2700 K, 1000 lux: 2.956 W/m<sup>2</sup>
- 4000 K, 200 lux: 1.629 W/m<sup>2</sup>
- 4000 K, 1000 lux: 4.106 W/m<sup>2</sup>

The irradiance powers of the LEDs were measured using Ocean Insight Flame T Miniature Spectrometer connected to an optical fibre with a cosine corrector. The optical fibre of the spectrometer was placed at a distance of 23 cm from the light source. The setup for this is shown in Figure 4.8.



Figure 4.8: Irradiance power measurement setup

### 4.3.3 AM1.5G Solar Simulation

For standard test condition (STC) measurements, a Wavelabs Sinus 70 class AAA solar simulator featuring adjustable height was used to reproduce the AM1.5G (1-Sun) spectrum. The simulator employs multiple LED lamp units and was calibrated with a certified silicon reference cell to deliver an irradiance of  $1000 \text{ W/m}^2$ . Solar cell samples were mounted on a custom-designed sample holder featuring six-pin contacts for front electrode and two pins for back electrode enabling electrical readout. A multiplexer enabled pixel-resolved measurements by alternating between individual pixels.

Before measuring the intended PSCs, the experimental setup was calibrated using a Si reference solar cell with an active area of  $4 \text{ cm}^2$ . The calibration arrangement is shown in Figure 4.9. J-V characteristics were recorded using a backward voltage sweep from 0.7 V to -0.2 V with a 10 mV step size (a forward sweep is equally suitable, as Si cells do not exhibit hysteresis). The compliance was set to 0.18 A.

The sample-holder height, from the table surface to the top of the holder, was adjusted to 12.5 cm using a ruler. The solar simulator height was then tuned such that the resulting  $J_{sc}$  matched  $14.90 \text{ mA/cm}^2$ . This calibration was subsequently used for all AM1.5G (1-Sun) measurements.

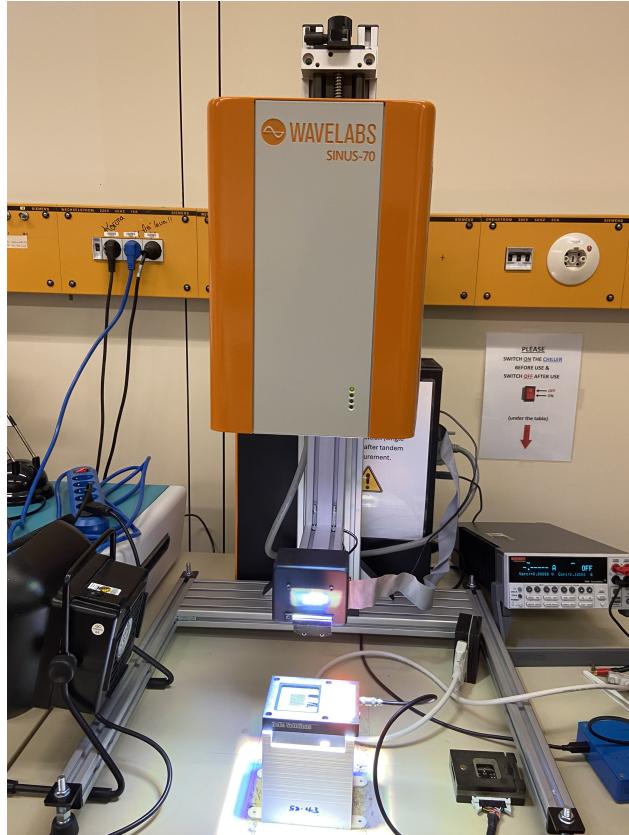


Figure 4.9: Setup for calibration of experimental setup

### 4.3.4 Measurement Procedure

A metal shadow mask as shown in Figure 4.4(b) was used to define the active cell area of  $0.09 \text{ cm}^2$ . J-V characteristics were recorded using a backward voltage sweep from 1.4 V to -0.2 V, with a step size of 10 mV and a dwell time of 0.1 s per step, resulting in 161 measurement points. The compliance was set to 0.18 A.

### 4.3.5 Performance Metrics

From the J-V curves, the key photovoltaic parameters, PCE(%),  $J_{sc}$ (mA/cm<sup>2</sup>),  $V_{oc}$  (V), and FF (%) were extracted.

These experimental results were compared against SCAPS simulation outputs to validate the consistency of the model.

## 5 Results and Analysis

### 5.1 Analysis of SCAPS Simulation Results - Standard Architecture

In this section, the influence of various material and device parameters on device performance is analyzed. The graphical analysis is shown in Figures 5.1, 5.3, 5.4, 5.5, 5.6 and 5.7. The influence of ETL thickness will also be explored in the Section 5.3, providing experimental validation for the device's physical scaling. The additional parameters investigated here serve as a computational framework for further device optimization. In the simulations, the effects of annealing temperature on device performance were represented by varying the interface defect density  $N_{it}$ , the ETL doping concentration  $N_D$ , and the absorber doping concentration  $N_A$ .

#### 5.1.1 Influence of Absorber layer (AL)/HTL interface defect density

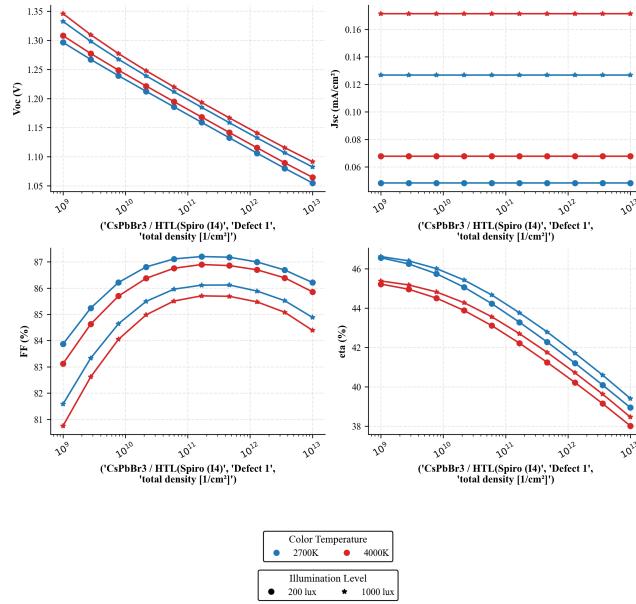


Figure 5.1: Influence of AL-HTL Interface defect density on device performance for device with ETL

Interfacial defect density refers to the concentration of electronic trap states located at the junction between two layers in a device, such as the absorber and hole transport layer. These defects can facilitate non-radiative recombination, reducing voltage and overall device efficiency. Interfacial defect density ( $N_{it}$ ) at the junction between the CsPbBr<sub>3</sub> absorber and the Hole Transport Layer (HTL) represents one of the most critical bottlenecks for high-efficiency indoor photovoltaics [20]. These defects act as non-radiative recombination centers

that capture photogenerated carriers before they can be extracted. It is important to note that variations in the absorber/HTL interface defect density ( $N_{it}$ ) are not influenced by the presence of the ETL. Recombination at this junction is governed primarily by minority-carrier (electron) capture at the hole-selective contact, making it a strictly local process. Since the ETL parameters were held constant in this study, and because recombination at the  $\text{CsPbBr}_3$ /HTL interface dominates the voltage and fill-factor losses [20, 18, 2], the observed trends can be attributed solely to the HTL-side defect density without contributions from the ETL.

In this simulation, the total defect density was varied from  $1 \times 10^9$  to  $1 \times 10^{13} \text{ cm}^{-2}$  under four indoor lighting conditions. Figure 5.1 illustrates the impact of interface quality on device performance.

- **$V_{oc}$ :** Exhibits a consistent and steep decline with increasing  $N_{it}$  across all illumination conditions. This trend reflects enhanced Shockley–Read–Hall recombination at the AL/HTL interface, which reduces quasi-Fermi level splitting. There is voltage loss for example in the 4000K 1000 lux condition, the initial  $V_{oc}$  is approximately 1.34 V and drops to approximately 1.08 V at the highest defect density ( $10^{13} \text{ cm}^{-2}$ ). This is a significant loss of  $\sim 260 \text{ mV}$ .
- **$J_{sc}$ :** Remains invariant across the entire defect density range, indicating that short-circuit current is governed by photon flux and bulk generation rather than interface quality because at  $V=0$  the device operates far from saturation, drift-assisted extraction dominates carrier transport, and the residence time of carriers is so short that interfacial recombination becomes negligible. The values remain stable at approximately  $0.17 \text{ mA/cm}^2$  (4000K 1000 lux),  $0.127 \text{ mA/cm}^2$  (2700K 1000 lux),  $0.068 \text{ mA/cm}^2$  (4000K 200 lux), and  $0.048 \text{ mA/cm}^2$  (2700K 200 lux).
- **FF:** Displays a non-monotonic trend across all conditions, initially increasing to a peak near  $N_{it} = 10^{11} \text{ cm}^{-2}$  before experiencing a slight decline. The non-monotonic behaviour arises because very low interface defect densities provide insufficient band bending at the  $\text{CsPbBr}_3$ /HTL interface. In this regime, a small increase in  $N_{it}$  introduces additional interfacial charge that slightly enhances the local electric field, improves hole extraction, and can therefore increase the device performance. However, once  $N_{it}$  exceeds this beneficial range, the interface becomes dominated by Shockley–Read–Hall recombination. The resulting loss of quasi-Fermi level splitting reduces  $V_{oc}$ , while the increased recombination near the maximum power point lowers FF. The final FF at  $10^{13} \text{ cm}^{-2}$  remains higher than the initial value at  $10^9 \text{ cm}^{-2}$  as recombination can increase at higher defect densities. For the 2700K 200 lux condition, the FF rises from 83.9% to a peak of 87.2%, settling at 86.2%. Under the 4000K 1000 lux environment, the FF starts at 80.8%, peaks at 85.7%, and settles at 84.4%. This represents a relative improvement of approximately 4.5% over the full defect range, suggesting that while high  $N_{it}$  eventually causes J-V curve rounding (depicted in Figure 5.2), the device maintains efficient carrier extraction under these indoor spectra. This effect is much more visible indoors, where the device operates in a low-injection regime and drift extraction dominates, making the photocurrent too small to mask recombination losses. Under 1-Sun illumination similar rounding can occur, but it appears at higher voltages and is less pronounced because the large carrier flux partially compensates for the increased recombination.

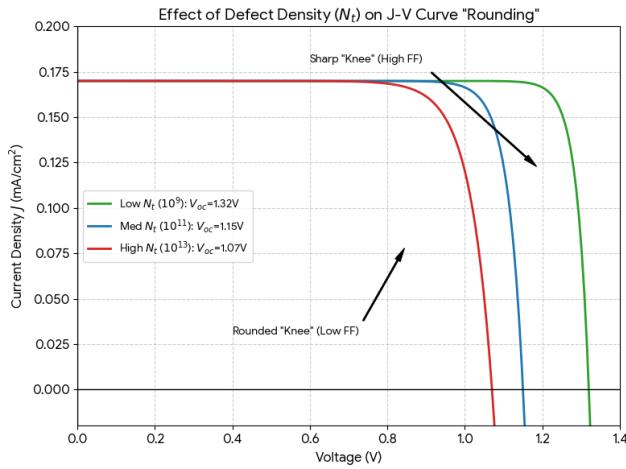


Figure 5.2: J-V curve depicting the rounding the curve with increase in  $N_{it}$

- **PCE ( $\eta$ ):** Follows a steep and monotonic decline, driven primarily by the substantial losses in  $V_{oc}$ . The efficiency under 2700K 1000 lux drops from approximately 46.6% to 39.4%, representing a relative loss of 15.45%. Similarly, under 4000K 200 lux, the PCE falls from 45.2% to 38.0%, a relative degradation of 15.93%. This confirms that interfacial defect density significantly impacts overall performance, with the  $V_{oc}$  decay outweighing the minor gains in Fill Factor.

Increasing the interface defect density at the  $\text{CsPbBr}_3$ /Spiro-OMeTAD contact leads to a monotonic reduction in  $V_{oc}$  and PCE, while  $J_{sc}$  remains nearly unchanged. This behaviour arises because interfacial traps act as SRH recombination centres that reduce the quasi-Fermi level splitting, directly lowering  $V_{oc}$ . At short circuit, carriers are extracted rapidly and recombination at the HTL interface plays a minor role, explaining the weak dependence of  $J_{sc}$  on  $N_{it}$ . However, near the maximum power point, where extraction and recombination compete, the increased SRH activity reduces the fill factor and overall efficiency. Under indoor illumination, the effect is amplified because the carrier generation rate is very low.

In summary, the AL/HTL interface in Spiro-based devices is quite sensitive to defect density. While  $J_{sc}$  and FF show relative resilience, the pronounced and continuous loss in  $V_{oc}$  results in a total PCE degradation of approximately 15-16% across the studied range. Minimizing  $N_{it}$  below  $10^{11} \text{ cm}^{-2}$  is essential to preserve maximum  $V_{oc}$  and achieve peak efficiency under indoor lighting.

### 5.1.2 Influence of Absorber Layer Shallow Acceptor Density

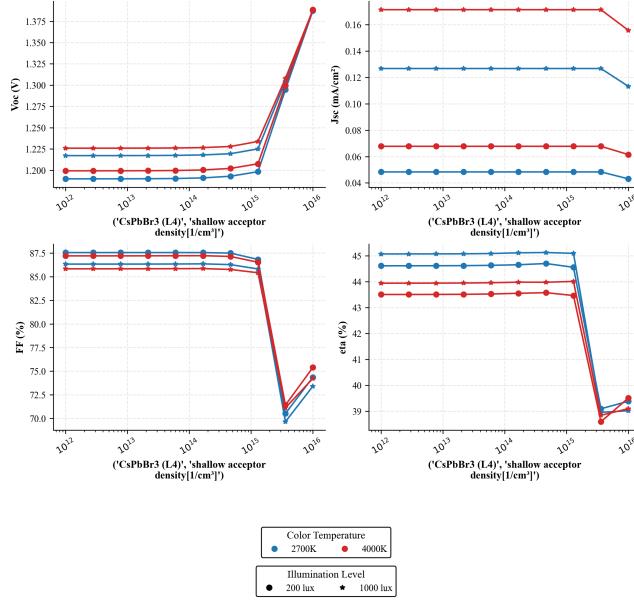


Figure 5.3: Influence of Absorber shallow acceptor density on device performance for device with ETL

The shallow acceptor density ( $N_A$ ) of the absorber layer is the concentration of dopants or defects with energy levels close to the valence band that provide the mobile holes necessary for p-type conductivity. In this study,  $N_A$  was varied from  $10^{12}$  to  $10^{16} \text{ cm}^{-3}$  to evaluate its impact on the device's photovoltaic performance under four indoor illumination conditions. Figure 5.3 summarize the trends for  $V_{oc}$ ,  $J_{sc}$ , FF, and PCE.

- **$V_{oc}$ :** Shows a consistent and monotonic increase with rising shallow acceptor density across all illumination conditions. This improvement is attributed to enhanced band bending and stronger built-in electric fields at the ETL/CsPbBr<sub>3</sub> and CsPbBr<sub>3</sub>/HTL interfaces, which accelerate carrier separation, suppress minority-carrier accumulation at the contacts, and thereby reduce interfacial recombination while increasing the quasi-Fermi level splitting. The voltage gain is most pronounced at the highest doping levels; for example, under 4000K 1000 lux, the initial  $V_{oc}$  rises from  $\sim 1.226 \text{ V}$  to  $\sim 1.388 \text{ V}$  as  $N_A$  increases to  $10^{16} \text{ cm}^{-3}$ . These results show that moderate to high acceptor doping can stabilize voltage by improving charge separation and reducing interface recombination.
- **$J_{sc}$ :** Exhibits a slight but consistent decline with increasing  $N_A$ , particularly after  $N_A$  exceeds  $4 \times 10^{15} \text{ cm}^{-3}$ . This trend suggests that although moderate acceptor doping enhances field-assisted separation, higher  $N_A$  can also introduce additional scattering, thereby slightly limiting current extraction. The effect is measurable across all spectra; for the 4000K 1000 lux condition,  $J_{sc}$  remains stable at  $0.171 \text{ mA/cm}^2$  before dropping to  $\sim 0.155 \text{ mA/cm}^2$ . The total variation in  $J_{sc}$  remains small, with a maximum absolute drop of approximately  $0.016 \text{ mA/cm}^2$  for the 4000K 1000 lux case, corresponding to a relative change of approximately 9.3%. This indicates that while the impact is measurable, it remains minor in absolute terms and does not dominate the efficiency trend.
- **FF:** Displays a non-monotonic trend, with a sharp drop near  $N_A = 4 \times 10^{15} \text{ cm}^{-3}$  followed by partial recovery at  $10^{16} \text{ cm}^{-3}$ . This behavior reflects a complex interplay between enhanced field strength and increased recombination near the maximum power point. At high shallow acceptor densities, the fill factor (FF) begins to decrease because adding more acceptors increases recombination sites and slightly increases

resistive losses, reducing current at higher voltages. The minimum FF occurs at the  $4 \times 10^{15} \text{ cm}^{-3}$  mark; for the 2700K 200 lux condition, it drops from  $\sim 87.5\%$  to  $\sim 70.5\%$  before recovering to  $\sim 75.3\%$ .

- **PCE ( $\eta$ ):** Closely follows the FF trend, with a sharp efficiency drop near  $N_A = 4 \times 10^{15} \text{ cm}^{-3}$  and partial recovery at higher doping levels. The initial rise in  $V_{oc}$  contributes positively to  $\eta$ , but the concurrent sharp decline in FF offsets these gains. The highest efficiency is achieved under 2700K 1000 lux, maintaining nearly 45.1% up to  $N_A = 10^{15} \text{ cm}^{-3}$ . Beyond this point, efficiency drops to  $\sim 38.8\%$  before stabilizing, indicating that excessive doping introduces parasitic effects that limit performance.

The variation of shallow acceptor density  $N_A$  in the absorber produces the expected trade-off between enhanced built-in field and increased recombination. At low to moderate  $N_A$ , the strengthened internal electric field improves charge separation and increases  $V_{oc}$ . However, once  $N_A$  exceeds the optimal range, the depletion width narrows and carrier collection becomes increasingly diffusion-limited. Higher doping also increases the probability of SRH recombination, which reduces FF and PCE. Thus, the observed trends reflect the classical balance between field-assisted extraction and recombination penalties associated with excessive *p*-type doping.

In summary, shallow acceptor doping in the absorber layer enhances  $V_{oc}$  by improving band alignment and internal electric field strength. However, this introduces trade-offs in  $J_{sc}$  and fill factor (FF), particularly at densities exceeding  $10^{15} \text{ cm}^{-3}$ . Optimal device performance is observed at moderate doping levels ( $10^{14}$  to  $10^{15} \text{ cm}^{-3}$ ), where voltage gains are balanced against transport losses.

### 5.1.3 Influence of ETL Shallow Donor Density

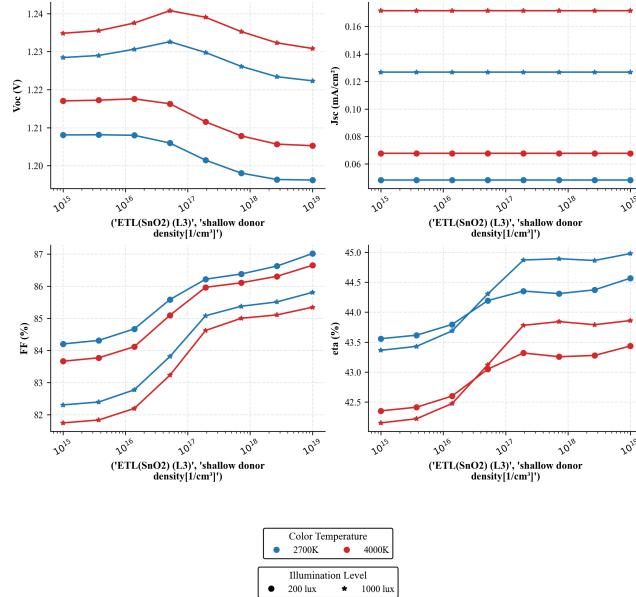


Figure 5.4: Influence of ETL shallow donor density on device performance for device with ETL

The shallow donor density ( $N_D$ ) is the concentration of doping added to a semiconductor (*n*-type doping) that possess energy levels very close to the conduction band edge ( $E_C$ ). Because the ionization energy is small (comparable to thermal energy  $k_B T$ ), these impurities easily release electrons into the conduction band at room temperature, thereby increasing the material's electrical conductivity.  $N_D$  in the Electron Transport Layer (ETL), plays a pivotal role in determining the conductivity and the electrostatic alignment at the cathode

interface. By varying  $N_D$  from  $1 \times 10^{15}$  to  $1 \times 10^{19} \text{ cm}^{-3}$ , the impact of ETL carrier concentration on charge extraction and recombination was evaluated under four indoor lighting spectra. The resulting photovoltaic parameters are illustrated in Figure 5.4.

- **$V_{oc}$ :** Shows a non-monotonic trend across all illumination conditions, initially increasing to a peak at approximately  $N_D = 4 \times 10^{16} \text{ cm}^{-3}$  before exhibiting a gradual decrease at higher donor densities. While higher  $N_D$  improves ETL conductivity, excessive doping beyond the optimal point can enhance interface recombination, thereby reducing the quasi-Fermi level splitting. Under high-lux conditions (e.g., 4000K 1000 lux),  $V_{oc}$  peaks at approximately 1.241 V and then drops to about 1.231 V at  $1 \times 10^{19} \text{ cm}^{-3}$ . This trend indicates that excessive ETL doping introduces a minor voltage penalty despite its transport benefits.
- **$J_{sc}$ :** Remains effectively constant over the entire donor density range, with only negligible variations. This invariance confirms that short-circuit current is governed predominantly by photon flux and bulk generation in the absorber rather than by ETL doping. The internal electric field at short-circuit conditions remains sufficient for efficient carrier extraction, and changes in  $N_D$  do not significantly alter the collection dynamics. The values remain stable at approximately  $0.171 \text{ mA/cm}^2$  (4000K 1000 lux) and  $0.048 \text{ mA/cm}^2$  (2700K 200 lux).
- **FF:** Exhibits a consistent and monotonic increase with rising donor density across all illumination conditions. This improvement is attributed to enhanced ETL conductivity reducing series resistance, which leads to more efficient charge extraction near the maximum power point. The FF gain is significant across all spectra; for example, under low-lux conditions (2700K 200 lux), the FF increases from  $\sim 84.2\%$  to  $\sim 87.0\%$ . Under the 4000K 1000 lux environment, the FF improves from  $\sim 81.7\%$  to  $\sim 85.3\%$ .
- **PCE ( $\eta$ ):** Shows a clear and monotonic increase with increasing donor density, driven primarily by the substantial gains in Fill Factor. The improvement in FF more than compensates for the minor late-stage loss observed in  $V_{oc}$ . Under 2700K 1000 lux, the efficiency increases from  $\sim 43.4\%$  at low  $N_D$  to approximately 45.0% at the highest doping level. For the 4000K 200 lux condition, the efficiency rises from  $\sim 42.4\%$  to  $\sim 43.4\%$ . This behavior indicates that ETL donor doping primarily enhances net power conversion efficiency by improving the device's fill factor.

Increasing the shallow donor density  $N_D$  in the ETL initially improves device performance by enhancing electron conductivity and strengthening band bending at the ETL/perovskite interface, which facilitates electron extraction. This reduces transport resistance and supports higher FF. At very high  $N_D$ , however, ionized impurity scattering and band misalignment can increase interfacial recombination, leading to the observed saturation or slight decline in performance. The resulting trend reflects the balance between improved electron selectivity at moderate doping and recombination or transport penalties at excessive doping levels.

In summary, shallow donor doping in the ETL enhances the fill factor by reducing resistive losses and improving charge transport, while simultaneously introducing a modest voltage penalty at higher  $N_D$ . Since  $J_{sc}$  remains essentially insensitive to ETL doping and the FF gains largely compensate for the small decrease in  $V_{oc}$ , the overall power conversion efficiency remains nearly unchanged across the full donor-density range. This indicates that the dominant trade-off is between transport (FF) and voltage ( $V_{oc}$ ), rather than a direct loss in efficiency. Optimal ETL performance is therefore achieved at moderate donor densities, where the FF improvement is realized without incurring significant voltage degradation, enabling balanced and stable indoor operation.

### 5.1.4 Influence of ETL Thickness

The compact  $\text{TiO}_2$  ( $c\text{-TiO}_2$ ) acts as the electron-selective and hole-blocking contact at the front interface. Its thickness influences device operation in several ways. A very thin  $c\text{-TiO}_2$  layer may contain pinholes (which is not explicitly modeled in simulations, but can be modeled by varying shunt resistances), enabling shunt pathways, whereas an excessively thick layer increases series resistance because electrons must traverse a longer, moderately conductive oxide. Thickness also affects interfacial band alignment: as the layer becomes thicker, the built-in field across the ETL changes, modifying the barrier for electron extraction and the blocking efficiency for holes. Finally,  $c\text{-TiO}_2$  contributes to parasitic absorption; thicker films reduce optical transmission into the absorber, lowering the photogeneration rate. Thus, an optimal thickness is required to balance electrical selectivity, transport resistance, and optical losses [15]. To assess these effects under realistic indoor operating conditions, the  $c\text{-TiO}_2$  thickness was varied from 15 to 30 nm, (also evaluated experimentally is dicussed in Section 5.3.1) and the corresponding photovoltaic parameters were evaluated under four indoor illumination spectra (2700K and 4000K at 200 and 1000 lux). The resulting trends are summarized in Figure 5.5.

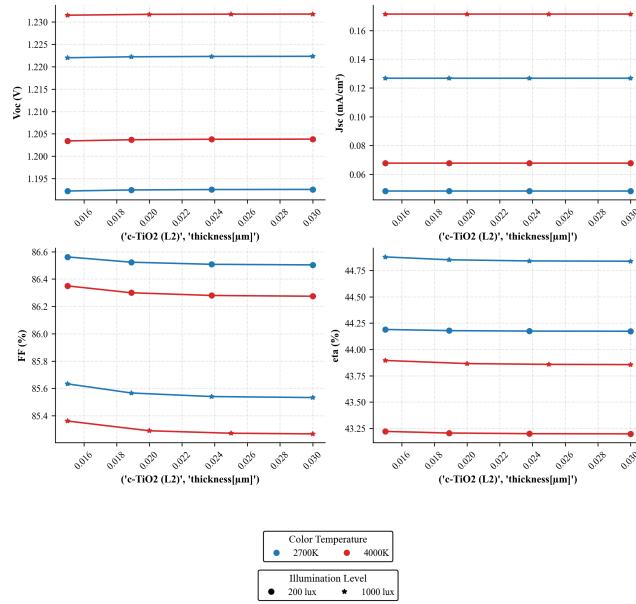


Figure 5.5: Influence of ETL Thickness

- $V_{oc}$ : The open-circuit voltage lies in the range of approximately 1.190–1.230 V across all  $c\text{-TiO}_2$  thicknesses and illumination conditions. Variations with thickness are modest and do not exhibit a strong monotonic trend, indicating that the built-in potential and quasi-Fermi level splitting are only weakly affected within this relatively thin ETL regime. The small spread between the different spectra reflects the expected dependence of  $V_{oc}$  on photon flux and spectrum rather than on  $c\text{-TiO}_2$  thickness itself.
- $J_{sc}$ : The short-circuit current density spans roughly 0.06–0.17 mA/cm $^2$ , with higher values observed for the 1000 lux cases and lower values for 200 lux, as expected from the different photon flux levels. Across the investigated thickness range,  $J_{sc}$  shows only weak dependence on  $c\text{-TiO}_2$  thickness for each illumination condition. This suggests that optical transmission through the compact  $\text{TiO}_2$  and carrier collection at short circuit remain largely preserved, and that indoor  $J_{sc}$  is governed primarily by illumination intensity and spectral content rather than by moderate ETL thickness variations.
- **FF:** The fill factor remains high, with values between approximately 77.5% and 79.5%. Only small fluctuations with  $c\text{-TiO}_2$  thickness are observed, and no pronounced degradation at the upper thickness limit is

evident. This behaviour indicates that, within the studied thickness window, additional series resistance introduced by the ETL is limited and does not strongly hinder charge extraction. The consistently high FF across all spectra further confirms that transport losses in the compact  $\text{TiO}_2$  are minor under these indoor conditions.

- **PCE ( $\eta$ ):** The power conversion efficiency varies within a relatively narrow band of about 43.25% to 44.8% across the full thickness and illumination set. For each spectrum,  $\eta$  shows only a minor change, reflecting the combined stability of  $V_{\text{oc}}$ ,  $J_{\text{sc}}$ , and FF. Slight efficiency differences between the four indoor conditions follow the expected trends in  $J_{\text{sc}}$  and  $V_{\text{oc}}$  with illumination intensity and colour temperature.

The ETL thickness sweep shows only a weak dependence of device performance on layer thickness under indoor illumination. A thicker ETL increases the electron transport distance and series resistance, while a thinner ETL risks incomplete coverage and potential shunting. However, because indoor photocurrents are two to three orders of magnitude smaller than under AM1.5G illumination, the associated ohmic losses  $J \cdot R$  remain negligible even when the ETL is made substantially thicker. As a result, the device operates in a regime where interfacial recombination dominates over transport limitations, explaining the minimal sensitivity to ETL thickness observed in the simulations.

In summary, varying the compact  $\text{TiO}_2$  thickness between 15 and 30 nm shows a limited impact on device performance in simulation.  $V_{\text{oc}}$ ,  $J_{\text{sc}}$ , and FF remain largely stable, leading to PCE variations of only about one percentage point across the entire parameter space.

### 5.1.5 Influence of Series Resistance ( $R_s$ )

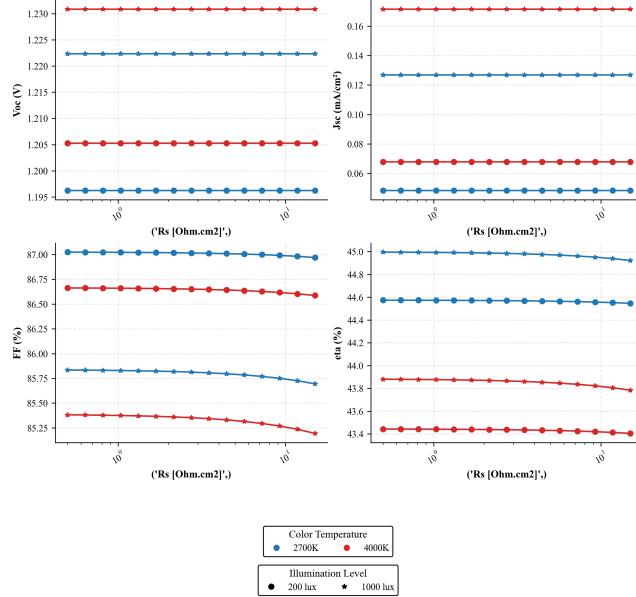


Figure 5.6: Influence of Series Resistance on device performance for device with ETL

Series resistance ( $R_s$ ) represents the cumulative resistive losses encountered by charge carriers as they traverse the device layers and contacts. Series resistance ( $R_s$ ) in photovoltaic devices originates from the bulk resistance of the semiconductor layers, contact resistance at the electrodes, and the sheet resistance of the transparent conductive oxides. In this study,  $R_s$  was varied from 0.5 to 15  $\Omega \cdot \text{cm}^2$  across four indoor lighting conditions to

evaluate its impact on carrier extraction and ohmic losses. Figure 5.6 summarizes the resulting trends for  $V_{oc}$ ,  $J_{sc}$ , FF, and PCE.

- **$V_{oc}$ :** Remains invariant across the entire range of  $R_s$  for all illumination conditions. In an open-circuit state, the net current flowing through the device is zero; therefore, the voltage drop across the series resistance ( $I \times R_s$ ) is also zero. This confirms that  $R_s$  does not influence the quasi-Fermi level splitting or the built-in potential under open-circuit conditions. The values remain constant at approximately 1.231 V (4000K 1000 lux), 1.222 V (2700K 1000 lux), 1.205 V (4000K 200 lux), and 1.196 V (2700K 200 lux).
- **$J_{sc}$ :** Stays constant as  $R_s$  increases within the investigated range from 0.5 to 15  $\Omega \cdot \text{cm}^2$ . Under low-intensity indoor lighting, the photogenerated current densities ( $J_{sc}$ ) are extremely small, remaining below 0.18 mA/cm<sup>2</sup> across all spectra. Consequently, the ohmic loss even at the maximum  $R_s$  is insufficient to significantly shift the operating point away from the short-circuit condition, maintaining a stable current output of approximately 0.171 mA/cm<sup>2</sup> for the 4000K 1000 lux condition.
- **FF:** Exhibits a steady, linear decline as  $R_s$  increases. Unlike  $V_{oc}$  and  $J_{sc}$ , the Fill Factor is determined at the maximum power point where significant current flows through the device. Increasing  $R_s$  enhances ohmic power dissipation, which reduces the squareness of the J-V curve, as illustrated in Figure 5.2. The impact is most visible under high-intensity 1000 lux conditions; for the 4000K 1000 lux condition (green), the FF drops from  $\sim 85.38\%$  to  $\sim 85.19\%$ , representing a minor but measurable absolute decrease of  $\sim 0.19\%$ .
- **PCE ( $\eta$ ):** Shows a gradual decrease that directly mirrors the decline in the Fill Factor. Because  $V_{oc}$  and  $J_{sc}$  are unaffected, the overall power conversion efficiency is solely penalized by the increased ohmic losses. For the 2700K 1000 lux condition, the efficiency falls from  $\sim 45.00\%$  to  $\sim 44.92\%$ . The device maintains exceptionally high efficiency (above 43.4%) throughout the range, highlighting that indoor photovoltaics are relatively resilient to moderate series resistance compared to devices operating under 1-sun conditions.

The series resistance  $R_s$  has only a minor effect on indoor device performance. The voltage loss associated with series resistance,  $V_{loss} = J \cdot R_s$ , remains extremely small because the photocurrent density under indoor illumination is less than 1 mA/cm<sup>2</sup>. Even large increases in  $R_s$  therefore produce negligible voltage drops, resulting in minimal changes to FF or PCE. This behaviour contrasts sharply with AM1.5G operation, where much higher photocurrents make the device more sensitive to series resistance.

### 5.1.6 Influence of Shunt Resistance ( $R_{sh}$ )

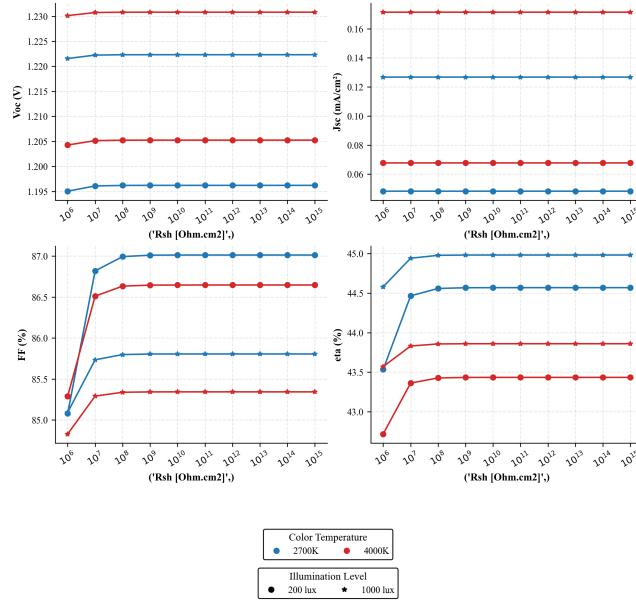


Figure 5.7: Influence of Shunt Resistance on device performance for device with ETL

Shunt resistance ( $R_{sh}$ ) represents the alternative current pathways within a photovoltaic cell, typically caused by manufacturing defects, pinholes in the transport layers, or shunt paths along the device edges and can also arise from incomplete transport-layer coverage, metal penetration during electrode deposition, defective interfaces, or conductive channels formed by ionic migration. These features provide alternative current routes that reduce the effective photovoltage and overall device performance. In this study,  $R_{sh}$  was varied across a wide range ( $1 \times 10^6$  to  $1 \times 10^{15} \Omega \cdot \text{cm}^2$ ) to evaluate its impact on carrier loss under indoor lighting. Figure 5.7 summarizes the resulting trends for  $V_{oc}$ ,  $J_{sc}$ , FF, and PCE.

- **$V_{oc}$ :** Shows a sharp sensitivity at low  $R_{sh}$  values before saturating rapidly. Below the threshold of  $10^7 \Omega \cdot \text{cm}^2$ ,  $V_{oc}$  exhibits a slight drop because the shunt leakage begins to affect the quasi-Fermi level splitting. For example, in the 4000K 1000 lux condition,  $V_{oc}$  recovers from  $\sim 1.230 \text{ V}$  at  $10^6 \Omega \cdot \text{cm}^2$  to a stable plateau of  $\sim 1.231 \text{ V}$  beyond  $10^7 \Omega \cdot \text{cm}^2$ . Once  $R_{sh}$  is high enough to minimize these leakage paths,  $V_{oc}$  becomes limited by the built-in potential across the primary ETL/absorber junction. .
- **$J_{sc}$ :** Remains entirely invariant across the entire range of shunt resistance from  $10^6$  to  $10^{15} \Omega \cdot \text{cm}^2$  for all illumination conditions. This is consistent with solar cell theory, as  $J_{sc}$  is measured under short-circuit conditions where the voltage across the device is zero; thus, no current is driven through the shunt path regardless of its resistance. The current levels are maintained at approximately  $0.171 \text{ mA}/\text{cm}^2$  for 4000K 1000 lux and  $0.048 \text{ mA}/\text{cm}^2$  for 2700K 200 lux.
- **FF:** Exhibits a significant initial increase that saturates as  $R_{sh}$  reaches  $10^8 \Omega \cdot \text{cm}^2$ , because, at this point, the shunt current  $J_{sh} = V/R_{sh}$  becomes negligible compared to the very small indoor photocurrent. Beyond this threshold the leakage pathway no longer influences the  $J$ - $V$  characteristics, so further increases in  $R_{sh}$  do not produce additional gains in FF. Low shunt resistance provides a parasitic path for carriers near the maximum power point, severely reducing the Fill Factor. Under the 2700K 200 lux condition, the FF rises sharply from  $\sim 85.1\%$  at  $10^6 \Omega \cdot \text{cm}^2$  to a plateau of  $\sim 87.0\%$ . For indoor applications, high  $R_{sh}$

is vital because the low photogenerated current makes the device more susceptible to even minor leakage paths.

- **PCE ( $\eta$ ):** Efficiency follows the combined trends of  $V_{oc}$  and FF, showing a rapid recovery at low  $R_{sh}$  followed by a stable plateau beyond  $10^8 \Omega \cdot \text{cm}^2$ . For the 2700K 1000 lux condition, the efficiency improves from  $\sim 44.6\%$  to a value of  $\sim 45.0\%$ . The early saturation point indicates that once a baseline film quality is achieved to prevent significant shunts, further increases in  $R_{sh}$  provide diminishing returns for overall power conversion.

Shunt resistance  $R_{sh}$  exerts a far stronger influence on indoor performance than  $R_s$ . Because indoor photocurrents are very small, even modest leakage currents can compete with or exceed the photo-generated current. When  $R_{sh}$  is low, the leakage pathway bypasses the diode, causing a rapid collapse in FF and a reduction in  $V_{oc}$ . As  $R_{sh}$  increases, the leakage current  $J_{sh} = V/R_{sh}$  becomes negligible relative to  $J_{sc}$ , and the device characteristics converge. In the simulated range, this convergence occurs once  $R_{sh}$  exceeds approximately  $10^9$ - $10^{10} \Omega \cdot \text{cm}^2$ , beyond which further increases do not produce observable changes in the  $J$ - $V$  curve.

### 5.1.7 Comparative Analysis of Performance Parameters

The performance of the CsPbBr<sub>3</sub> indoor photovoltaic cell is a holistic result of its doping levels, interface quality, and parasitic resistances. A comparative study of the investigated parameters reveals the following hierarchy of influence:

- **The Primary Drivers ( $V_{oc}$  enhancers): Shallow Acceptor Density ( $N_A$ )** serve as the main tools for voltage optimization. Optimal  $N_A$  ( $\sim 10^{15} \text{ cm}^{-3}$ ) maximizes the built-in potential.
- **The Efficiency Killers: Interfacial Defect Density ( $N_{it}$ ) and Shunt Resistance ( $R_{sh}$ )** are the most critical quality parameters. Elevated  $N_{it}$  causes a devastating decline in  $V_{oc}$  and FF due to non-radiative recombination. Similarly, low  $R_{sh}$  can cause a decline of device PCE by providing parasitic leakage paths, which is particularly dangerous in low-current indoor environments.
- **Transport and Ohmic Regulators: ETL Shallow Donor Density ( $N_D$ )** acts as a threshold for charge extraction, where a minimum density of  $10^{18} \text{ cm}^{-3}$  is required to eliminate FF bottlenecks. Conversely, **Series Resistance ( $R_s$ )** causes a slow, linear erosion of the Fill Factor, though its impact is relatively minor under indoor lighting compared to standard 1-sun conditions.
- **Fabrication-Tolerant Parameters: Compact TiO<sub>2</sub> Thickness** shows only a weak influence on performance metrics within the simulated range (15 to 30 nm).  $V_{oc}$ ,  $J_{sc}$ , and FF remain fairly stable, and PCE varies by less than one percentage point. This indicates that c-TiO<sub>2</sub> thickness is not a critical optimization lever under indoor conditions, and moderate deviations during fabrication do not compromise device efficiency.

**Optimization Conclusion:** To achieve peak efficiencies above 40% under indoor spectra, a multi-pronged strategy is required: minimize interfacial defects and maximize shunt resistance to ensure junction integrity; optimize absorber doping to maximize voltage; maintain ETL doping above the transport threshold to minimize extraction losses; and ensure c-TiO<sub>2</sub> thickness remains within a fabrication-tolerant window to preserve high fill factor and efficiency. This is summarized in Table 5.1 .

Parameter	Importance	Affected Metrics	Physical Reason
AL/HTL interface defect density ( $N_{it}$ )	<b>Very High</b>	$V_{oc}$ , FF, PCE	Dominant SRH recombination pathway under low carrier density; reduces quasi-Fermi level splitting and distorts the $J-V$ curve near the MPP.
Absorber acceptor density ( $N_A$ )	<b>High</b>	$V_{oc}$ , FF, PCE	Modifies built-in field and depletion width; moderate doping improves separation, excessive doping increases SRH/Auger recombination and narrows the SCR.
ETL donor density ( $N_D$ )	<b>Moderate</b>	FF, PCE	Improves electron selectivity and conductivity at moderate levels; excessive doping increases recombination or misalignment.
ETL thickness	<b>Low</b>	FF (weak), PCE (weak)	Transport bottlenecks are suppressed indoors due to extremely small photocurrent; ohmic losses remain negligible.
Series resistance ( $R_s$ )	<b>Very Low</b>	FF (very weak)	Voltage loss $J \cdot R_s$ is negligible because indoor $J_{sc}$ is $< 1 \text{ mA/cm}^2$ .
Shunt resistance ( $R_{sh}$ )	<b>Very High</b>	$V_{oc}$ , FF, PCE	Leakage current competes directly with the tiny indoor photocurrent; low $R_{sh}$ collapses FF and reduces $V_{oc}$ .

Table 5.1: Relative importance of key device parameters for indoor  $\text{CsPbBr}_3$  perovskite solar cell performance. Importance levels indicate the magnitude of influence on  $V_{oc}$ ,  $J_{sc}$ , FF, and PCE under low-photon-flux indoor operation.

### Positioning the Present Findings Within Indoor PV Literature and Their Contrast to known Outdoor Optimization

The trends identified in this work align closely with the broader understanding of indoor perovskite photovoltaics while also highlighting several key divergences from conventional AM1.5G (1-Sun) optimization strategies. Indoor operation imposes fundamentally different constraints on device physics due to the low photon flux, narrow spectral bandwidth, and reduced carrier generation rates. As a result, the hierarchy of performance determinants observed in this study is strongly supported by recent literature on indoor photovoltaics [2, 3, 5, 6] and by the known material properties of  $\text{CsPbBr}_3$  [4, 20, 19]. These distinctions underscore that indoor-optimized device architectures cannot be directly extrapolated from outdoor design rules, and instead require a recombination-limited rather than transport-limited optimization framework.

The identification of shallow acceptor density ( $N_A$ ) as the primary levers for maximizing  $V_{oc}$  is consistent with prior reports showing that wide-bandgap perovskites benefit from enhanced trap screening and optimized built-in potential under low illumination.

The strong sensitivity of indoor performance to interfacial defect density ( $N_t$ ) and shunt resistance ( $R_{sh}$ ) mirrors the conclusions of several indoor PV studies [2]. Under low-current operation, even small leakage pathways or non-radiative recombination channels can severely suppress both  $V_{oc}$  and FF. This contrasts with AM1.5G (1-

Sun) operation, where higher photocurrents can partially mask moderate shunt losses, and bulk recombination competes more directly with interface recombination.

The behaviour of ETL shallow donor density ( $N_D$ ) observed here—namely, a threshold around  $10^{18} \text{ cm}^{-3}$  beyond which FF bottlenecks vanish—is in excellent agreement with SCAPS-based transport studies [8, 7]. Indoors, once the ETL is sufficiently conductive to avoid space-charge buildup, further increases in  $N_D$  primarily redistribute the balance between  $V_{oc}$  and FF without significantly altering PCE. Under outdoor illumination, however, ETL doping continues to influence both transport and recombination due to the much higher carrier generation rates.

The weak dependence of performance on compact  $\text{TiO}_2$  thickness (L2) is consistent with reports that thin, continuous  $\text{TiO}_2$  layers operate in a fabrication-tolerant regime [15, 16]. Indoors, the low photocurrent reduces the impact of series resistance, and the narrow LED spectrum minimizes optical penalties. Outdoors, by contrast, ETL thickness can significantly affect parasitic absorption and reflection across the broad AM1.5G (1-Sun) spectrum, making thickness a more critical optimization parameter.

The relatively minor influence of series resistance ( $R_s$ ) under indoor conditions is well supported by literature [7]: with microamp-level photocurrents, the absolute voltage drop across  $R_s$  remains small, whereas under AM1.5G (1-Sun) illumination,  $R_s$  is a major determinant of FF and overall PCE.

Overall, these comparisons highlight that indoor photovoltaics operate under a fundamentally different optimization regime than outdoor solar cells. Indoor performance is dominated by voltage preservation, interface quality, and leakage suppression, whereas outdoor optimization prioritizes optical absorption, current generation, and series-resistance minimization. This is summarized in Table 5.2. The present results therefore not only agree with existing indoor PV literature but also reinforce the emerging consensus that indoor perovskite photovoltaics require a distinct, environment-specific design philosophy.

Optimization Aspect	Indoor PV (Low-Flux)	Outdoor PV (1-Sun)
Dominant performance driver	Voltage preservation; suppression of non-radiative recombination; maintaining high $V_{oc}$	Maximizing photocurrent generation; maximizing light absorption
Critical interfaces	Absorber Layer/HTL interface quality; trap suppression; shunt isolation	ETL/perovskite optical and transport interfaces; minimizing reflection and parasitic absorption
Key electrical limitation	Leakage pathways (low $R_{sh}$ ) and interfacial SRH recombination	Series resistance, transport bottlenecks, and space-charge limitations
Relevant material properties	Defect energetics, interface passivation, built-in field stability	Absorption coefficient, carrier mobility, diffusion length
Optimization priority	Recombination-limited regime	Transport- and absorption-limited regime

*Table 5.2: Comparison of dominant optimization priorities for indoor and outdoor perovskite photovoltaics. Indoor performance is governed by voltage preservation, interface quality, and leakage suppression, whereas outdoor optimization emphasizes optical absorption, current generation, and series-resistance minimization.*

The comparative values of typical performance metrics and the values obtained in this study is shown in Table

5.3. The comparative values for typical material parameters and the values obtained in this study is shown in Table 5.4.

Parameter	Typical Indoor Value	Optimized in This Work	Indoor Limit / Target
$V_{oc}$ (V)	0.9-1.1	1.20-1.23	1.22-1.25 (radiative indoor limit for $CsPbBr_3$ )
$J_{sc}$ (mA/cm <sup>2</sup> )	$(5\text{-}8) \times 10^{-5}$	0.12 – 0.17	Limited by indoor spectrum; only $\sim 10\text{--}20\%$ improvement possible
FF (%)	75-85	84-87	85-88 (no shunt, low recombination)
PCE (%)	40-45	43-44	40-45 (indoor theoretical limit for $CsPbBr_3$ )
Series resistance $R_s$ ( $\Omega\cdot\text{cm}^2$ )	5-20	$\sim 5$	Not performance-limiting indoors
Shunt resistance $R_{sh}$ ( $\Omega\cdot\text{cm}^2$ )	$10^7\text{-}10^9$	$> 10^{10}$	$> 10^{11}$ (leakage negligible vs. indoor $J_{sc}$ )

Table 5.3: Indoor-specific performance metrics for  $CsPbBr_3$  devices: typical literature values, optimized values obtained in this work, and the indoor theoretical or practical limits

Material Parameter	Typical Indoor Value	Optimized in This Work	Indoor Ideal / Target
Interface defect density $N_{it}$ (cm <sup>-2</sup> )	$10^{10}\text{-}10^{12}$	$4 \times 10^{10}$	$< 10^{11}$ (minimizes SRH at low injection)
Absorber doping $N_A$ (cm <sup>-3</sup> )	$10^{14}\text{-}10^{16}$	$10^{15}$	$10^{15}\text{-}10^{16}$ (optimal indoor field strength)
ETL donor density $N_D$ (cm <sup>-3</sup> )	$10^{17}\text{-}10^{19}$	$10^{19}$	$10^{18}\text{-}10^{19}$ (ensures extraction even at low $J$ )
ETL thickness (nm)	20-50	30	20-40 (coverage; transport irrelevant indoors)

Table 5.4: Indoor-relevant material and device parameters for  $CsPbBr_3$  photovoltaics, showing typical literature values, optimized values from this work, and the ideal targets for low-photon-flux operation

The J-V curve under LED illumination after reasonable optimization is given in Figure 5.8 (a). Optimized material parameters are given in Table 5.5. The performance parameters after optimization are given in Table 5.6.

Parameters	FTO	c-TiO <sub>2</sub>	ETL (SnO <sub>2</sub> )	CsPbBr <sub>3</sub>	HTL (Spiro-OMeTAD)
Thickness (nm)	400	30	30	500	200
Bandgap (eV)	3.5 [7]	3.4 [15]	3.5 [7]	2.34 [4]	2.2 [7]
e <sup>-</sup> affinity (eV)	4.0 [7]	4.1 [16]	4.0 [7]	3.75 [4]	2.2 [7]
Permittivity (relative)	9.0 [7]	9.0 [6]	9.0 [7]	6.5	3.0 [7]
Effective density of states at CB (cm <sup>-3</sup> )	2.2 x 10 <sup>18</sup> [7]	2.5 x 10 <sup>18</sup> [6]	2.2 x 10 <sup>18</sup> [5]	2.2 x 10 <sup>18</sup> [18]	2.2 x 10 <sup>18</sup> [7]
Effective density of states at VB (cm <sup>-3</sup> )	2.2 x 10 <sup>18</sup> [7]	2.5 x 10 <sup>19</sup> [6]	1.8 x 10 <sup>19</sup> [5]	1.8 x 10 <sup>18</sup> [18]	1.8 x 10 <sup>19</sup> [7]
e <sup>-</sup> thermal velocity (cm·s <sup>-1</sup> )	1 x 10 <sup>7</sup>	1 x 10 <sup>7</sup>	1 x 10 <sup>7</sup>	1.1 x 10 <sup>7</sup> [4]	1 x 10 <sup>7</sup>
h <sup>+</sup> thermal velocity (cm·s <sup>-1</sup> )	1 x 10 <sup>7</sup>	1 x 10 <sup>7</sup>	1 x 10 <sup>7</sup>	9.5 x 10 <sup>6</sup> [4]	1 x 10 <sup>7</sup>
Mobility of e <sup>-</sup> (cm <sup>2</sup> /V·s)	20 [7]	0.1 [16]	240 [5]	5 [19]	2 x 10 <sup>-4</sup> [7]
Mobility of h <sup>+</sup> (cm <sup>2</sup> /V·s)	10 [7]	10 <sup>-5</sup> [15]	25 [5]	5 [19]	2 x 10 <sup>-4</sup> [7]
Density of n-type doping (cm <sup>-3</sup> )	5 x 10 <sup>19</sup>	1 x 10 <sup>19</sup>	1 x 10 <sup>19</sup>	0	0
Density of p-type doping (cm <sup>-3</sup> )	0	0	0	1 x 10 <sup>15</sup>	1 x 10 <sup>17</sup>
Density of defects (cm <sup>-3</sup> )	0	10 <sup>15</sup> [6]	10 <sup>15</sup>	1 x 10 <sup>15</sup>	10 <sup>15</sup> [7]

Table 5.5: Optimized material parameters used in simulation

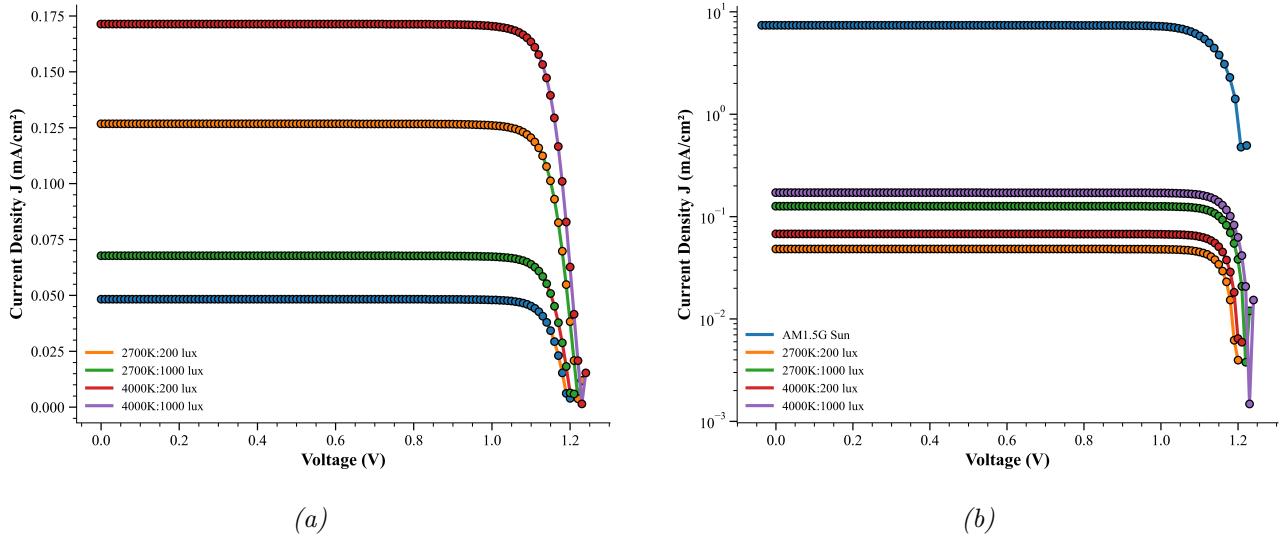


Figure 5.8: Optimized J-V curves (a) under LEDs (b) Comparison with 1-Sun illumination for device with ETL

Method	Illumination	$J_{sc}$ (mA/cm <sup>2</sup> )	FF (%)	$V_{oc}$ (V)	PCE (%)
<b>SCAPS Simulation (With ETL)</b>					
	4000K, 1000 lux	0.171	85.34	1.23	43.86
	4000K, 200 lux	0.068	86.65	1.20	43.43
	2700K, 1000 lux	0.126	85.81	1.22	44.98
	2700K, 200 lux	0.048	87.01	1.19	44.57
	AM1.5G (1-Sun)	7.4	79.97	1.37	8.09

Table 5.6: SCAPS-simulated performance parameters for CsPbBr<sub>3</sub> devices with ETL under various illumination conditions.

## 5.2 Analysis of SCAPS Simulation Results - Without ETL

The performance of CsPbBr<sub>3</sub>-based perovskite solar cells (PSCs) without ETL was evaluated under indoor LED spectra (2700K and 4000K) at varying illuminance levels (200 lux and 1000 lux). The following sections detail the sensitivity of the photovoltaic figures of merit to key material and resistive parameters. The trends of the performance metrics to each parameter is given in Figure 5.9 and 5.10.

### 5.2.1 Interface Defect Density ( $N_{it}$ )

The interface between the absorber and the hole transport layer (HTL) is a major site for non-radiative recombination, making the defect density at this junction a key determinant of device performance. As  $N_{it}$  increases from  $10^9$  to  $10^{13} \text{ cm}^{-2}$ , a clear decline in  $V_{oc}$ ,  $FF$ , and overall efficiency is observed as shown in Figure 5.9 (a), reflecting the progressively stronger recombination losses at the interface. Once the defect density exceeds approximately  $0.5 \times 10^{13} \text{ cm}^{-2}$ , the performance metrics begin to saturate, indicating that the recombination rate has entered a transport-limited regime where further increases in  $N_{it}$  no longer produce additional decline. To sustain power conversion efficiencies above 40%, the interface must therefore be passivated to defect densities below  $10^{11} \text{ cm}^{-2}$ , ensuring that interfacial recombination remains sufficiently suppressed.

The qualitative dependence on the interface defect density  $N_{it}$  in the ETL-free architecture is consistent with the behaviour observed for the ETL-based device in Section 5.1.1. In both cases, increasing  $N_{it}$  primarily reduces  $V_{oc}$  and PCE through enhanced non-radiative recombination at the perovskite/HTL interface, while  $J_{sc}$  remains largely unaffected because short-circuit operation is dominated by photogeneration and bulk transport rather than interfacial recombination. However, the removal of the ETL modifies the quantitative sensitivity of the device to these defects. In the ETL-free stack, the  $\text{CsPbBr}_3/\text{HTL}$  interface must provide a larger fraction of the charge selectivity and built-in field, since the front contact (FTO/ $\text{CsPbBr}_3$ ) is less selective than the  $\text{c-TiO}_2/\text{SnO}_2$  ETL stack. As a result, recombination at the HTL interface has a comparatively stronger impact on  $V_{oc}$ ,  $FF$ , and overall device performance than in the ETL-integrated architecture. Thus, while the trends remain qualitatively similar, the ETL-free device exhibits a heightened sensitivity to interfacial defect density due to the absence of an electron-selective front contact.

### 5.2.2 Shallow Acceptor Density ( $N_A$ )

Varying the shallow acceptor density within the  $\text{CsPbBr}_3$  absorber strongly influences the internal electric field profile and, consequently, the device performance. As  $N_A$  increases, the open-circuit voltage rises monotonically, reaching values near 1.35 V as shown in Figure 5.9 (b). This behaviour reflects the enhanced quasi-Fermi level splitting and the corresponding increase in the built-in potential ( $V_{bi}$ ) that accompanies stronger p-type doping. However, this voltage gain is counterbalanced by a sharp decline in both fill factor and efficiency once the doping level approaches  $1.5 \times 10^{15} \text{ cm}^{-3}$ . At this point, the depletion region becomes too narrow relative to the absorber thickness, reducing the portion of the device in which carriers are efficiently collected by drift. As a result, carrier extraction becomes increasingly diffusion-limited, leading to substantial losses in  $FF$  and  $\eta$ . This behaviour marks a clear efficiency cliff, highlighting the need to maintain moderate doping levels to balance voltage enhancement with effective carrier collection.

The dependence on the absorber shallow acceptor density  $N_A$  in the ETL-free architecture also mirrors the qualitative trends observed for the ETL-based device in Section 5.1.2. In both cases, increasing  $N_A$  initially enhances  $V_{oc}$  by strengthening the built-in electric field and improving charge separation, but beyond an optimal doping range the performance degrades due to increased recombination and a reduction of the effective depletion width. This leads to a characteristic trade-off: moderate p-type doping improves  $V_{oc}$ , whereas excessive  $N_A$  compromises FF and PCE by making carrier collection increasingly diffusion-limited.

In the ETL-free stack, however, the impact of  $N_A$  is amplified compared to the ETL-based architecture. Without an electron-selective ETL, the internal field profile and junction electrostatics are governed almost entirely by the  $\text{CsPbBr}_3/\text{HTL}$  and  $\text{CsPbBr}_3/\text{FTO}$  interfaces. As a consequence, changes in  $N_A$  more strongly reshape the

space-charge region and the balance between drift- and diffusion-driven transport. This makes the ETL-free device more sensitive to over-doping: once  $N_A$  exceeds the optimal window, the collapse in FF and PCE is more pronounced than in the ETL-integrated case, because there is no additional selective contact to mitigate the resulting transport and recombination losses. Thus, while both architectures exhibit the same basic trends, the ETL-free configuration displays a narrower doping window for high-performance operation.

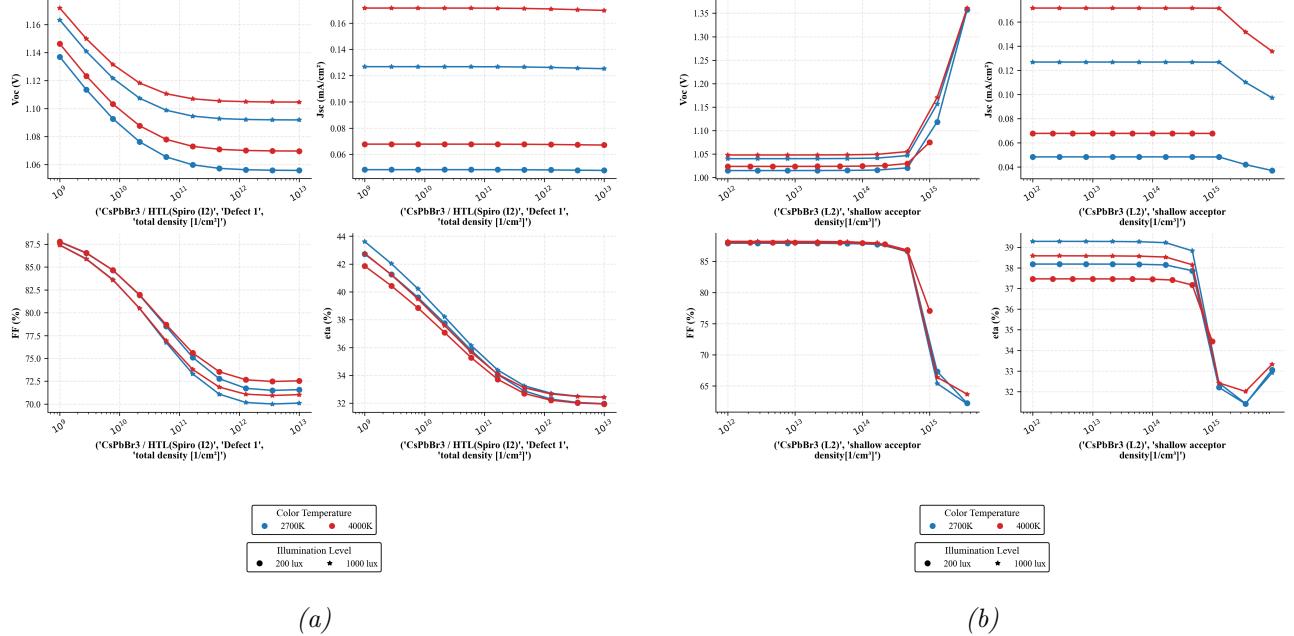


Figure 5.9: Influence of (a) AL/HTL interface defect density and (b) Absorber Shallow Acceptor Density on device without ETL

### 5.2.3 Parasitic Resistances ( $R_s$ and $R_{sh}$ )

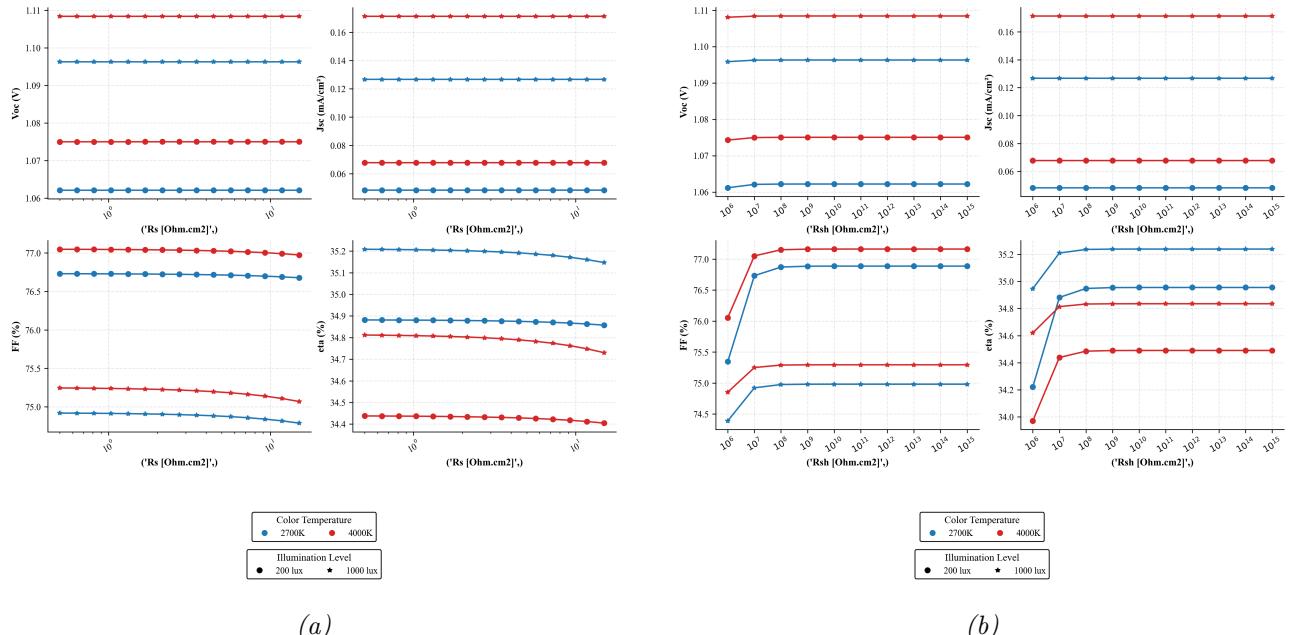


Figure 5.10: Influence of (a) Series Resistance ( $R_s$ ) and (b) Shunt Resistance ( $R_{sh}$ ) on device without ETL

Parasitic resistances play distinct roles in determining indoor photovoltaic performance. The series resistance ( $R_s$ ) has only a minor impact under indoor conditions, because the photocurrent is extremely small and the associated ohmic loss,  $V_{\text{loss}} = J \cdot R_s$ , remains negligible even when  $R_s$  is increased to  $15 \Omega \cdot \text{cm}^2$ . In contrast, the shunt resistance ( $R_{sh}$ ) exerts relatively more influence. It shows that values on the order of  $10^7$ - $10^9 \Omega \cdot \text{cm}^2$  are good values to keep shunt losses below the percent level (i.e., fraction of the photocurrent that is lost through the current leakage pathway) under typical indoor  $J_{sc}$  values. The SCAPS trends shown here saturate once  $R_{sh}$  exceeds  $10^{10} \Omega \cdot \text{cm}^2$  further increases in  $R_{sh}$  do not produce any observable change in the  $J$ - $V$  behaviour as shunt leakage becomes very less relative to the indoor photocurrent.

#### 5.2.4 Spectral Sensitivity

Across all simulations, the 4000K LED spectrum consistently outperformed the 2700K spectrum as shown in 5.12. The 4000K LED allocates 40% of its photon flux (400–900nm) to wavelengths within the  $\text{CsPbBr}_3$  absorption window (400–530nm), compared to only 25% for the 2700K LED. This enhanced spectral overlap with the 2.34eV bandgap directly increases the absorbed photon flux (Figure 5.11) and is consistent with the higher  $J_{sc}$  and  $V_{oc}$  measured under 4000K illumination.

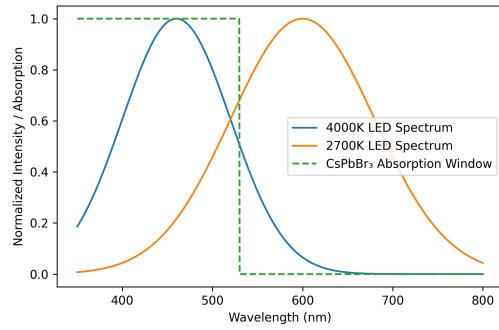


Figure 5.11: Schematic comparison of normalized emission spectra for 4000K and 2700K LEDs relative to the absorption window of  $\text{CsPbBr}_3$  (bandgap = 2.34 eV, 530 nm)

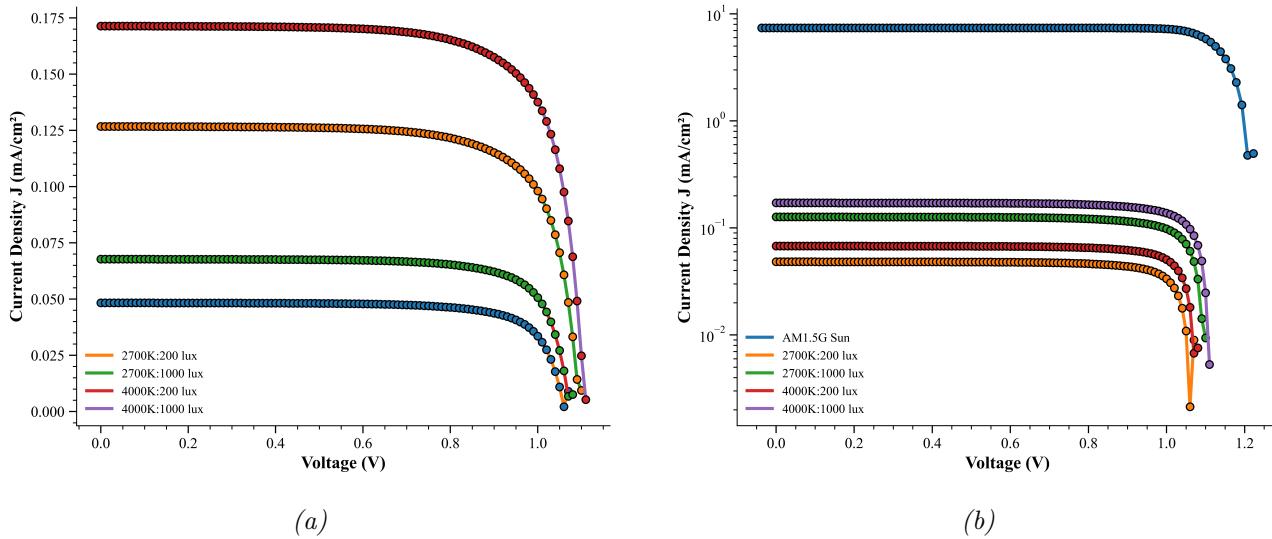


Figure 5.12:  $J$ - $V$  curves for device without ETL (a) under LEDs (b) Comparison with 1-Sun illumination

The corresponding results from this simulation for ETL-free device are given in Table 5.7.

Method	Illumination	$J_{sc}$ (mA/cm <sup>2</sup> )	FF (%)	$V_{oc}$ (V)	PCE (%)
<b>SCAPS Simulation (Without ETL)</b>					
	4000K, 1000 lux	0.171	75.26	1.11	34.81
	4000K, 200 lux	0.067	77.06	1.07	34.44
	2700K, 1000 lux	0.126	74.90	1.09	35.20
	2700K, 200 lux	0.048	76.69	1.06	34.86
	AM1.5G (1-Sun)	7.39	77.40	1.33	7.60

Table 5.7: SCAPS-simulated performance parameters for  $CsPbBr_3$  devices without ETL under various illumination conditions.

Overall, the SCAPS trends for the ETL-free architecture show that removing the electron transport layer increases the device's sensitivity to interface defects, absorber doping, and resistances. Compared to the ETL-based reference, the ETL-free configuration exhibits lower  $V_{oc}$ , reduced FF, and greater performance variability across all parameters studied. This behaviour arises because removing the ETL eliminates the selective electron-extraction and interfacial passivation normally provided by the c-TiO<sub>2</sub>/SnO<sub>2</sub> stack. In the ETL-based device, the ETL blocks holes, aligns favourably with the CsPbBr<sub>3</sub> conduction band, and suppresses recombination at the front interface. Without this layer, electrons and holes interact directly with the rough, defect-rich FTO surface, leading to enhanced interfacial recombination, poorer band alignment, and increased leakage pathways. As a result, the ETL-free configuration exhibits lower  $V_{oc}$ , reduced FF, and greater device-to-device variability, since small differences in interface quality or processing conditions have a much stronger impact when no selective contact is present.

While the simplified stack eliminates the need for ETL optimisation, it shifts the performance bottleneck directly to the FTO/perovskite interface, where recombination and leakage dominate more strongly than in the ETL-integrated device. These results indicate that, within the parameter space explored, removing the ETL does not provide a performance advantage and instead demands substantially higher interface quality to approach the stability and efficiency of the standard architecture.

### 5.3 Experimentally Measured Photovoltaic Performance Analysis

This section presents the experimentally measured performance characteristics of perovskite solar cells fabricated under three distinct conditions: two fabrication batches, each comprising four devices with ETLs of varying thicknesses annealed at different temperatures and devices fabricated without an ETL also annealed at different temperatures. All devices were characterized at pixels 1 through 5.

Annealing temperature is a controlled thermal treatment applied during device fabrication to improve the structural and electronic quality of thin films. In the simulations, the effects of annealing were represented by varying the interface defect density  $N_{it}$ , the ETL doping concentration  $N_D$ , and the absorber doping concentration  $N_A$ . Higher annealing temperatures (300 °C to 350 °C) typically enhance crystallinity, reduce defect density, and improve interfacial contact, which in turn correspond to lower  $N_{it}$  and optimized doping profiles in the model, thereby reducing non-radiative recombination and enabling more efficient charge transport.

Similarly, the thickness of functional layers such as the ETL plays a critical role in determining device performance. Layers that are too thin may suffer from incomplete coverage, higher series resistance, and increased

interfacial recombination, while excessively thick layers introduce longer transport pathways and resistive losses [7]. An optimal thickness ensures full coverage, efficient charge extraction, and minimal transport losses.

Together, annealing temperature and layer thickness strongly influence the balance between recombination suppression and charge-transport efficiency, and therefore have a direct impact on the overall photovoltaic performance.

### 5.3.1 Performance Metrics Analysis of ETL Thickness and Annealing Temperature

The performance of perovskite solar cells was statistically evaluated to determine the influence of ETL thickness (15-30 nm) and annealing temperature (250 °C and 300 °C). Figure 5.13 illustrates the distributions of open-circuit voltage ( $V_{oc}$ ), short-circuit current density ( $J_{sc}$ ), fill factor (FF), and power conversion efficiency (PCE) under two illumination regimes: indoor spectra (2700 K and 4000 K) at 200 and 1000 lux and under AM1.5G (1-Sun).

**5.3.1.1  $V_{oc}$ :** The  $V_{oc}$  exhibits a logarithmic dependence on light intensity, verifying the analysis in [20]. Under 1-Sun illumination,  $V_{oc}$  values are higher, reaching approximately 1.27 V. In indoor conditions,  $V_{oc}$  stabilizes between 1.0 and 1.2 V. Across the 15-30 nm ETL range, thickness has only a weak influence on the indoor voltage: the 25-30 nm devices occasionally show slightly higher peak values, but the overall overlap between thicknesses indicates that  $V_{oc}$  is largely insensitive to ETL thickness within this regime. The more noticeable distinction arises from annealing temperature. The 300 °C samples show marginally higher peak voltages for some thicknesses, whereas the 250 °C batch exhibits a much tighter distribution, likely because the lower annealing temperature produces a more uniform ETL/absorber interface and avoids the additional variability introduced at 300 °C. This narrower spread is therefore more indicative of batch-to-batch uniformity than of a strong physical optimum at 250 °C.

Under the indoor spectra, the simulations yield  $V_{oc}$  values between 1.19 and 1.23 V across the 2700 K and 4000 K spectra, consistent with the experimental range of 1.0-1.2 V. The simulated voltage advantage under 4000 K illumination mirrors the experimental trend, arising from the improved spectral overlap with the 2.34 eV bandgap. SCAPS also reproduces the weak thickness dependence observed experimentally: variations in ETL thickness produce only minor changes in  $V_{oc}$ , with the 25-30 nm regime yielding slightly higher and more stable voltages, consistent with reduced transport losses and improved band alignment. Furthermore, SCAPS captures the experimentally observed sensitivity to interface quality: parameter regimes corresponding to the 300 °C condition (elevated interface defect density or reduced shunt resistance) produce larger variance and reduced  $V_{oc}$ , whereas conditions mimicking the 250 °C regime yield tighter voltage distributions. Together, these consistencies demonstrate that the simulated parameter dependencies reflect the same physical mechanisms governing the experimental  $V_{oc}$  behaviour in ETL-based devices.

**5.3.1.2  $J_{sc}$ :**  $J_{sc}$  scales with photon flux, with 1-Sun devices producing the highest current, followed by 1000 lux and 200 lux indoor conditions. Analysis of the thickness trends reveals that current extraction does not scale linearly with thickness; instead, an optimal regime is observed around 20-30 nm. Under 1-Sun at 300 °C, the 15 nm ETL shows high current, but this performance is inconsistent.

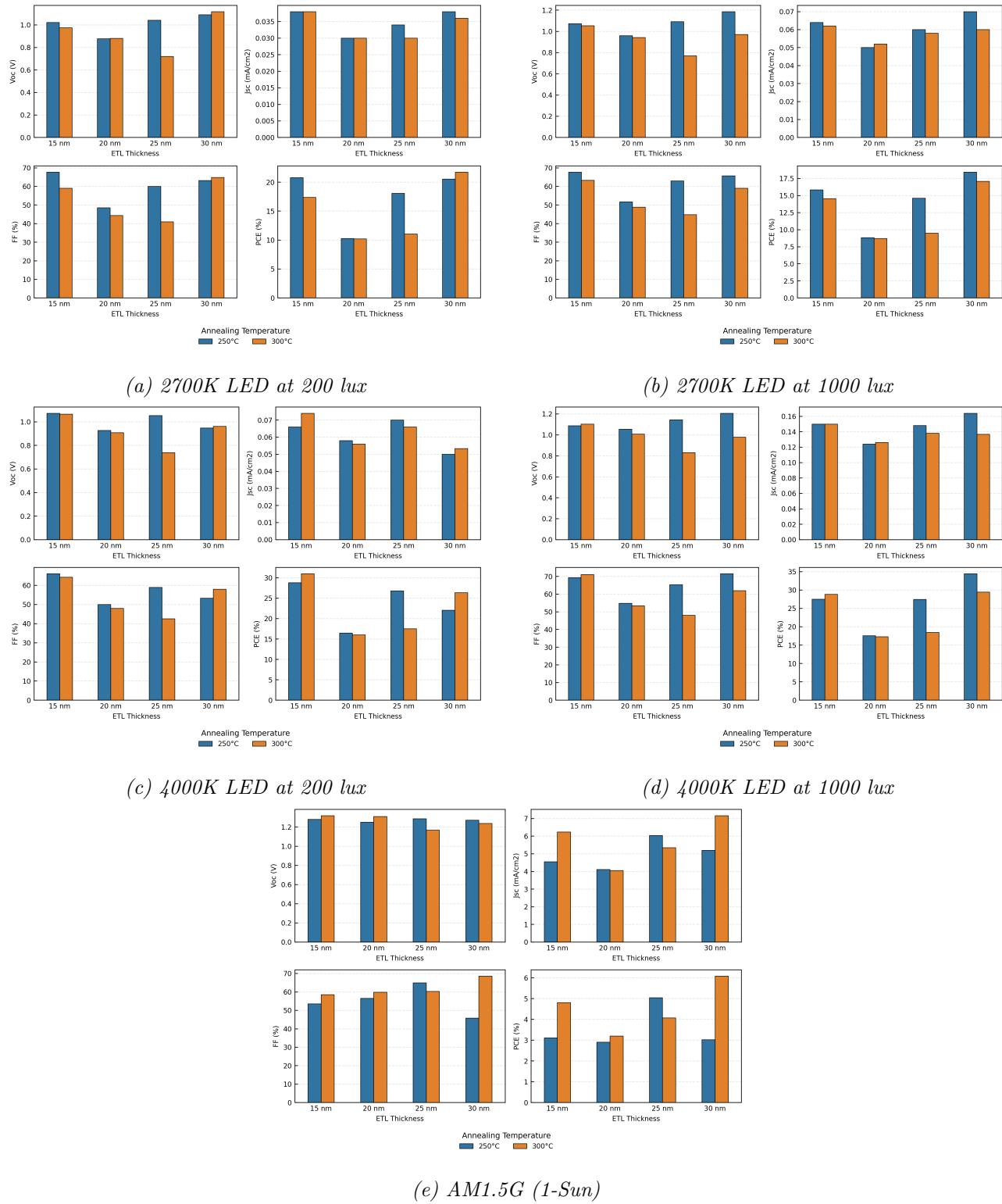


Figure 5.13: Performance metrics analysis for devices with ETL thickness varying from 15 to 30 nm at 250°C and 300°C annealing temperatures under different illumination conditions

Under the indoor spectra, the simulations yield  $J_{sc}$  values of 0.171 mA cm<sup>-2</sup> (4000 K, 1000 lux) and 0.068 mA cm<sup>-2</sup> (4000 K, 200 lux). Although the absolute simulated currents are approximately a factor of two lower than the measured values—reflecting optical and geometrical losses not captured in the SCAPS model—the relative trends align extremely well. In both simulation and experiment, the 4000 K illumination produces a ~30-40% higher  $J_{sc}$  than the 2700 K spectrum, confirming that the spectral overlap with the 2.34 eV CsPbBr<sub>3</sub> bandgap

governs the indoor photocurrent response.

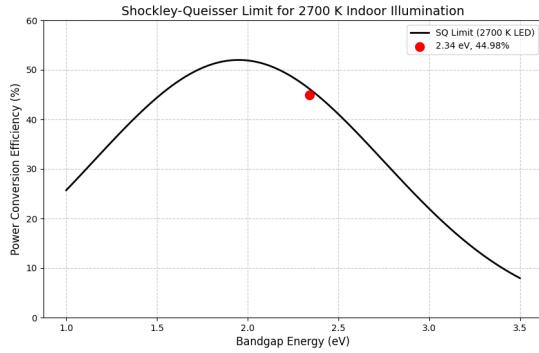
The simulated thickness dependence also mirrors the measurements: current extraction peaks in the 25-30 nm ETL regime, where transport resistance and optical losses are simultaneously minimized. In contrast, thinner ETLs (e.g., 15 nm) show higher but less stable currents in the simulations, consistent with the experimentally observed sensitivity of thin layers to interface quality and processing variation. The agreement between simulated and measured  $J_{sc}$  trends indicates that the interplay between ETL thickness, interface quality, and photon flux is the dominant factor controlling current extraction in ETL-based  $\text{CsPbBr}_3$  devices.

**5.3.1.3 FF:** FF values are highly sensitive to the quality of the ETL/perovskite interface. At 250 °C, FF values are relatively stable for all investigated ETL thicknesses, and the 25 nm configuration in particular exhibits a comparatively narrow spread in this dataset. However, given the limited sample size and the absence of a clear monotonic trend with thickness, this should be interpreted as a favourable process point rather than as evidence that 25 nm constitutes a uniquely optimised thickness for FF stability. Increasing the annealing temperature to 300 °C allows some devices (notably 30 nm at 1000 lux) to reach peak FFs above 70%; however, this temperature also leads to a high frequency of outliers with low FF (< 40%).

The SCAPS simulations reproduce the similar interface and illumination-dependent FF behaviour observed experimentally. Under indoor illumination, the simulated FF remains consistently high across all spectra—reaching 87% at 2700 K (1000 lux) and 85–86% under 4000 K—slightly exceeding the experimentally observed stability of the 250 °C, 25 nm ETL device. This modest enhancement because SCAPS model cannot be directly simulated to observe time-dependent degradation of the cell models. Model degradation can however be simulated by adjusting the interface defect density and doping concentrations to reflect experimentally observed changes. Overall, the close alignment between simulated and measured FF trends confirms that interface quality and shunt integrity are the dominant determinants of fill factor in ETL-based  $\text{CsPbBr}_3$  devices.

**5.3.1.4 PCE:** PCE trends consolidate the behaviors of  $V_{oc}$ ,  $J_{sc}$ , and FF. The highest indoor efficiencies are observed under 4000 K (1000 lux) illumination, with median values for 25-30 nm ETLs reaching approximately 35–38%. Under 1-Sun, PCE values range from 3% to 6%, highlighting the material’s specific suitability for indoor applications. While the 30 nm ETL at 300 °C achieves high peak efficiency, the 25 nm ETL at 250 °C represents the most reliable fabrication condition, maintaining high median PCE with minimal spread.

Under indoor conditions, the simulated PCE reaches 44.98% for the 2700 K, 1000 lux case and remains above 42% even at 200 lux for a 2.34 eV absorber remains below the corresponding detailed-balance efficiency limit reported for wide-bandgap indoor photovoltaics under warm-white LED spectra, and therefore does not exceed the Shockley–Queisser-type thermodynamic ceiling for this illumination regime ([22]) as illustrated in Figure 5.14. This result closely matches the experimentally observed superiority of the 25-30 nm ETL range. The simulations also show that 4000 K illumination provides a more favorable spectral match to the 2.34 eV bandgap of  $\text{CsPbBr}_3$ , resulting in higher photogeneration and improved voltage retention compared to 2700 K. Parameter regimes in SCAPS that mimic the 300 °C condition—such as increased interface defect density or reduced shunt resistance—produce higher peak efficiencies, mirroring the experimental spread for 30 nm ETLs at this temperature. In contrast, the simulated stability of the 25 nm ETL configuration aligns with the experimentally observed reliability at 25 nm, showing that balanced transport and low recombination are essential for achieving high indoor PCE.



*Figure 5.14: Measured PCE from simulation of the device under 2700K, 200lux illumination benchmarked against the corresponding SQ limit*

**5.3.1.5 Summarized Analysis:** The experimental and simulation data reveal that while 300 °C annealing can maximize individual performance parameters, it also introduces substantial variability due to interfacial instability. For all illumination conditions, the wide-bandgap nature of  $\text{CsPbBr}_3$  strongly favors indoor operation: experimentally,  $V_{\text{oc}}$  stabilizes between 1.0-1.2 V indoors, with  $J_{\text{sc}}$  limited primarily by the low intensity and narrow spectral content of indoor sources (i.e., is below  $1 \text{ mA cm}^{-2}$ ), and FF is maximized when interfacial recombination and leakage pathways are minimized. These behaviors are mirrored in the SCAPS simulations, which reproduce the same qualitative dependencies despite not explicitly modeling annealing temperature. Simulated trends show that moderate absorber doping, low interface defect density, high shunt resistance, and ETL donor densities above the transport threshold collectively yield the highest  $V_{\text{oc}}$ ,  $J_{\text{sc}}$ , FF, and PCE—closely matching the experimental trends. The simulations further confirm the experimentally observed spectral hierarchy: 4000 K illumination consistently outperforms 2700 K due to superior overlap with the 2.34 eV bandgap, yielding a  $J_{\text{sc}}$  of  $0.17 \text{ mA/cm}^2$  at 1000 lux. Although the simulated and experimentally measured PCE values differ slightly (by 3-4%), the simulation predicts a marginally higher efficiency for the 2700 K LED compared to the 4000 K LED but the  $V_{\text{oc}}$  and  $J_{\text{sc}}$  match closely to experimental measurements, with only  $0.018 \text{ mA/cm}^2$  difference between experimental and simulated values for  $J_{\text{sc}}$  and  $< 0.05 \text{ V}$  difference in  $V_{\text{oc}}$  values. This discrepancy is due to slight decrease in FF that may arise from minor recombination losses in the SCAPS model that become more pronounced at higher light intensities [23]. Together, these results demonstrate that  $\text{CsPbBr}_3$  delivers superior efficiency under indoor lighting than under 1-Sun, and that optimal device performance can arise from the combined control of absorber doping, interface quality, ETL transport properties, and shunt integrity.

From this analysis, the best performing samples under the optimized thickness, annealing temperature and pixel were chosen and the corresponding J-V curve is shown in Figure 5.15. The corresponding results are given in Table 5.8.

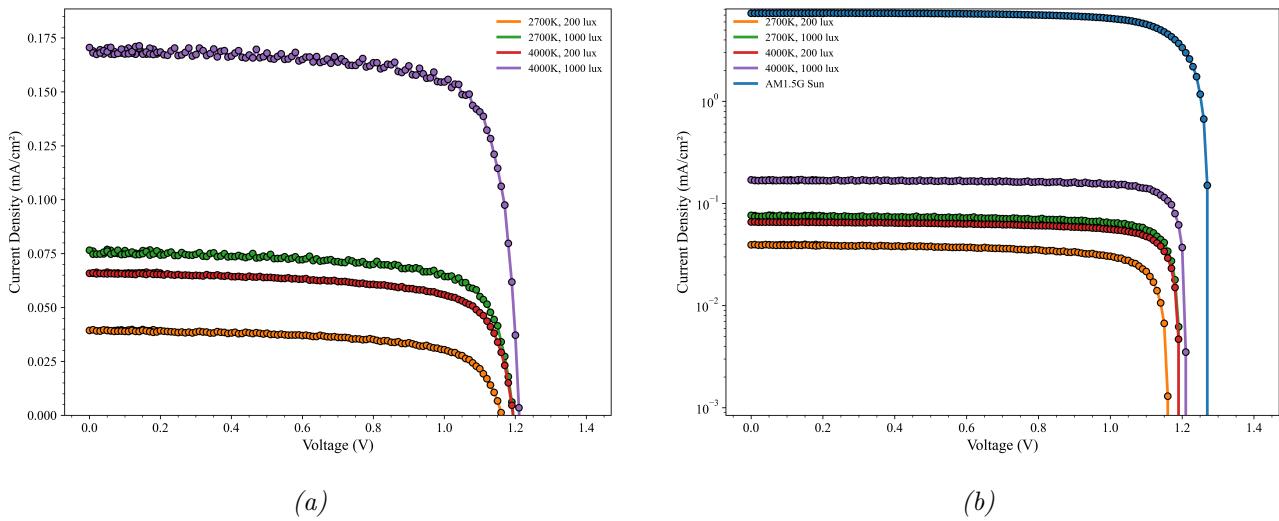


Figure 5.15: *J-V* curves analysis of the optimized samples for device with ETL (a) under LEDs and (b) Comparison with 1-Sun illumination

Method	Illumination	$J_{sc}$ (mA/cm <sup>2</sup> )	FF (%)	$V_{oc}$ (V)	PCE (%)
<b>Experimental Measurement (With ETL)</b>					
	4000K, 1000 lux	0.17	77.3	1.21	38.41
	4000K, 200 lux	0.07	71.6	1.19	34.13
	2700K, 1000 lux	0.06	72.4	1.19	22.13
	2700K, 200 lux	0.04	67.3	1.16	25.39
	AM1.5G (1-Sun)	7.22	70.2	1.27	6.45

Table 5.8: Experimentally measured performance parameters for  $\text{CsPbBr}_3$  devices with ETL under various illumination conditions.

### 5.3.2 Performance Analysis of ETL-Free Device Architectures

This section evaluates the photovoltaic performance of all-inorganic  $\text{CsPbBr}_3$  devices fabricated without an electron transport layer (ETL) across three annealing temperatures: 250 °C, 300 °C, and 350 °C. Experimental measurements were conducted under indoor (2700 K and 4000 K at 200/1000 lux) and 1-sun spectra to assess the impact of thermal processing on carrier extraction and efficiency. Figure 5.16 illustrates this analysis.

**5.3.2.1  $V_{oc}$ :** Across all spectra,  $V_{oc}$  exhibits a non-monotonic dependence on annealing temperature. Devices annealed at 350 °C consistently achieve the highest  $V_{oc}$  values, reaching approximately 1.1 V under 4000 K illumination and up to 1.3 V under 1-Sun. This enhancement is attributed to improved crystallinity, reduced interfacial recombination, and enhanced quasi-Fermi level splitting at higher thermal budgets. In contrast, 250 °C samples show intermediate voltages, while 300 °C devices exhibit a pronounced dip, likely due to incomplete grain formation and elevated defect densities. The observed suppression at 300 °C is consistent with the sensitivity of ETL-free architectures to interfacial quality and grain connectivity, as predicted by the continuity and drift-diffusion equations (2.7, 2.8, 2.9).

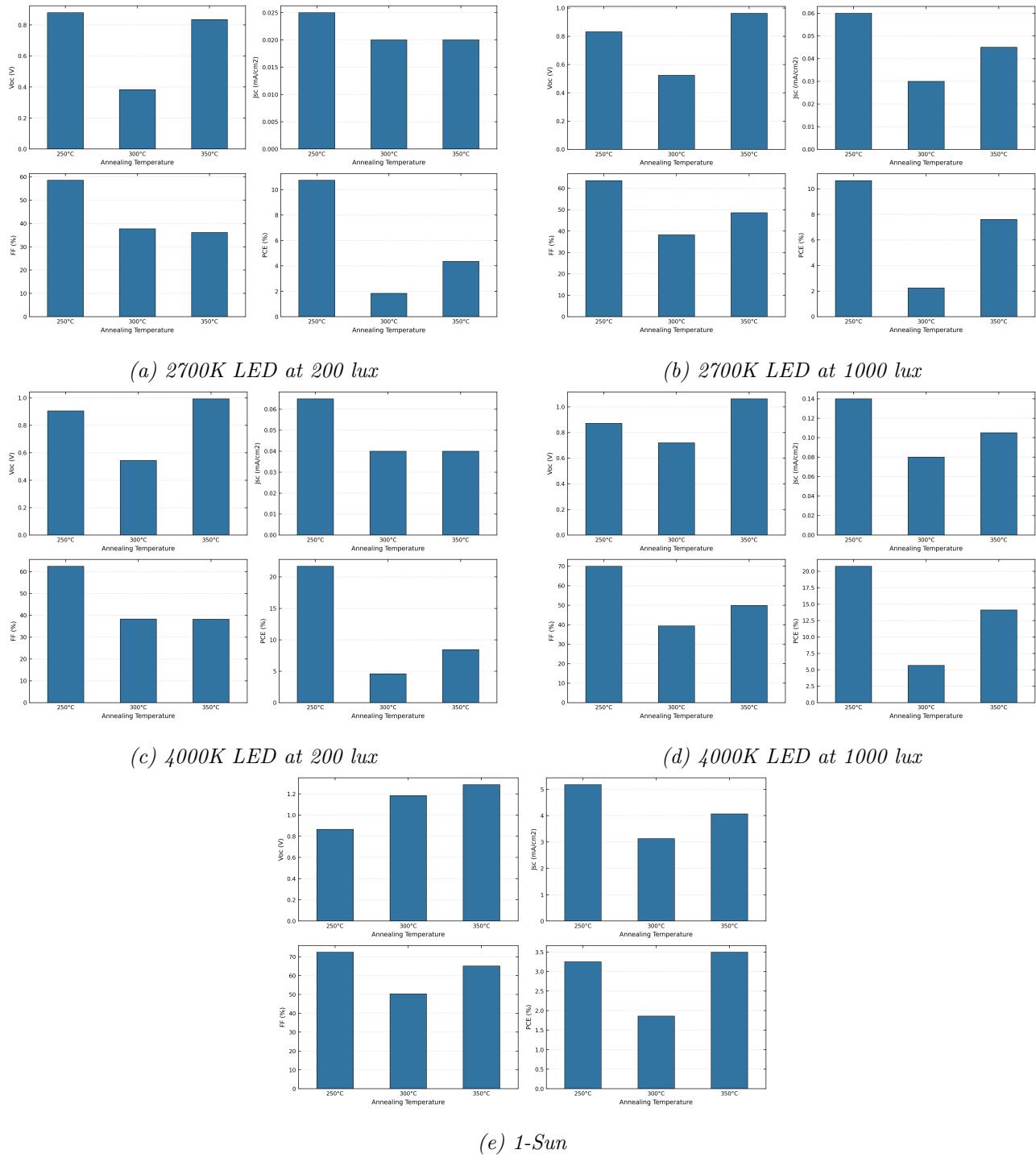


Figure 5.16: Performance metrics of ETL-Free Device Architectures at 250 °C, 300 °C and 350 °C annealing temperatures under different illumination conditions

SCAPS simulations reproduce this behaviour despite annealing temperature not being an explicit input parameter. Simulated  $V_{oc}$  increases when absorber doping is moderate, interface defect density is low, and shunt resistance is high—conditions that emulate the 350 °C regime. The simulated  $V_{oc}$  reaches 1.33 V under AM1.5G, closely matching the experimental maximum. SCAPS also recovers the voltage advantage under 4000 K illumination due to stronger spectral overlap with the 2.34 eV bandgap of CsPbBr<sub>3</sub>, and predicts higher  $V_{oc}$  at 1000 lux than at 200 lux, consistent with enhanced quasi-Fermi level splitting.

**5.3.2.2  $J_{sc}$ :** Experimentally, the highest  $J_{sc}$  is observed for devices annealed at 250 °C, followed by slightly reduced values at 350 °C, and a pronounced minimum at 300 °C. This trend is consistent across all illumination conditions, including 4000 K and 2700 K indoor spectra. The superior current extraction at 250 °C suggests optimal grain morphology, reduced trap-assisted recombination, and favourable interfacial contact. The dip at 300 °C likely arises from suboptimal interface formation and increased recombination pathways. Although 350 °C improves other metrics, the slight reduction in  $J_{sc}$  may reflect increased recombination due to over-annealing or densification effects that limit photogeneration.

SCAPS simulations align with this picture, showing nearly linear scaling of  $J_{sc}$  with photon flux and reproducing the superiority of 4000 K illumination due to spectral matching. Under AM1.5G, simulated  $J_{sc}$  reaches 7.39 mA cm<sup>-2</sup>. Parameter regimes mimicking the 250 °C condition—moderate  $N_A$ , low interfacial recombination, and high  $R_{sh}$ —yield the highest simulated  $J_{sc}$ , supporting the experimental observation that lower annealing temperatures can optimize current extraction in ETL-free devices.

**5.3.2.3 FF:** Fill factor trends show that 250 °C annealing yields the highest FF values, followed closely by 350 °C, while 300 °C consistently produces the lowest FF across all spectra. The superior FF at 250 °C (typically 65-70%) reflects reduced series resistance, favourable contact formation, and suppressed leakage pathways. The comparable performance at 350 °C suggests that higher thermal budgets can also suppress shunt leakage and improve interface quality, albeit with slightly more variability. The 300 °C minimum is indicative of poor interfacial contact and elevated leakage pathways.

SCAPS simulations reproduce this behaviour, showing that high FF values emerge only when shunt resistance exceeds 10<sup>10</sup> Ω · cm<sup>2</sup> and interface defect density is low. These conditions correspond to the 250 °C and 350 °C regimes. By calibrating experimental  $J-V$  curves against SCAPS  $R_{sh}$  sweeps, it can be inferred that 300 °C annealing results in significantly lower effective shunt resistance. Rather than predicting  $R_{sh}$  directly from temperature, we infer an effective shunt resistance range for each annealing condition by identifying the  $R_{sh}$  values in the model that reproduce the measured FF. This provides a process-specific estimate of how annealing temperature impacts shunt integrity, without implying a universal temperature-to- $R_{sh}$  relation. Under AM1.5G (1-Sun), the simulated FF of 77.40% close to the experimentally observed. The simulations also reflect the experimentally superior FF under 4000 K illumination. Overall, the SCAPS parameter trends capture the same physical mechanisms governing FF in ETL-free devices, reinforcing the conclusion that improved interface quality and suppressed shunt leakage at 250 °C are essential for achieving high-performance operation.

**5.3.2.4 PCE:** The PCE mirrors the integrated trends of  $V_{oc}$ ,  $J_{sc}$ , and FF. Devices annealed at 250 °C achieve the highest PCE across all illumination conditions, followed by 350 °C, with 300 °C showing the lowest efficiency. Specifically, PCE exceeds 25% under 4000 K, 1000 lux illumination, approximately 11.5% under 2700 K 1000 lux and reaches approximately 4.55% under 1-Sun for the 250 °C condition. The strong performance at 250 °C arises from the optimal balance of high  $J_{sc}$ , high FF, and sufficiently high  $V_{oc}$ , while 350 °C offers voltage and FF gains but slightly reduced current. The 300 °C dip reflects cumulative losses across all metrics.

SCAPS simulations reproduce these qualitative trends. High PCE values emerge when absorber doping is moderate, interface defect density is low, and shunt resistance is large. Simulated PCE under AM1.5G reaches 7.60%, exceeding experimental values due to idealized current extraction. The simulations confirm that the 250 °C regime offers the best trade-off between photogeneration and recombination suppression, while also recovering the experimental superiority of 4000 K illumination due to spectral alignment with the CsPbBr<sub>3</sub> bandgap. Together, these results demonstrate that the SCAPS parameter sensitivities capture the same physical

mechanisms governing PCE in ETL-free devices, reinforcing the conclusion that  $\text{CsPbBr}_3$  is intrinsically well-suited for low-intensity indoor photovoltaic operation.

**5.3.2.5 Summary and Implications:** The analysis shows that ETL-free  $\text{CsPbBr}_3$  devices reach optimal performance at an annealing temperature of  $250\text{ }^\circ\text{C}$ . This thermal condition appears to promote favourable grain morphology and interfacial contact quality, enabling efficient carrier extraction and reduced recombination despite the absence of an ETL [11]. Peak current density, fill factor, and overall power conversion efficiency are observed under  $4000\text{ K}$ ,  $1000\text{ lux}$  illumination, where the blue-shifted spectrum provides a superior match to the  $2.34\text{ eV}$  bandgap. Although  $V_{\text{oc}}$  reaches its maximum at  $350\text{ }^\circ\text{C}$ , the  $250\text{ }^\circ\text{C}$  condition offers the best integrated performance across all metrics.

In contrast, devices incorporating the ETL stack achieve high performance without requiring elevated thermal processing. The ETL suppresses interfacial recombination and stabilizes band alignment, which collectively diminish the dependence on absorber crystallinity and interface reconstruction during annealing [15]. As a result, ETL-based devices exhibit more stable FF and  $V_{\text{oc}}$  across illumination conditions, with significantly reduced sensitivity to thermal processing.

Consistent with these measurements, the SCAPS simulations reproduce the same underlying performance trends, even though annealing temperature is not explicitly modelled. Parameter regimes corresponding to the  $250\text{ }^\circ\text{C}$  condition—moderate absorber acceptor density, low interface defect density, and high shunt resistance—yield the highest simulated  $J_{\text{sc}}$ , FF, and PCE. Meanwhile, the simulated  $V_{\text{oc}}$  peaks under conditions emulating the  $350\text{ }^\circ\text{C}$  regime, reflecting the voltage enhancement from reduced recombination and improved quasi-Fermi level splitting. The simulations also independently recover the experimentally observed superiority of the  $4000\text{ K}$  spectrum, which enhances photogeneration and voltage preservation relative to  $2700\text{ K}$ . Together, the experimental and simulated results demonstrate that the strong  $4000\text{ K}$  response arises from the same physical mechanisms: suppressed interfacial recombination, efficient carrier extraction, and favourable spectral overlap with the wide-bandgap  $\text{CsPbBr}_3$  absorber.

At the same time, subtle differences between simulation and experiment highlight physical effects not captured in a one-dimensional drift-diffusion model. Although SCAPS shows a clear dependence of  $V_{\text{oc}}$ ,  $J_{\text{sc}}$ , and FF on illumination intensity, the simulated trends are smoother and more idealised than in fabricated devices. Experimentally,  $V_{\text{oc}}$  and FF exhibit stronger suppression at low intensity and greater sensitivity to interface quality, consistent with ion migration, interfacial charging, and microscopic shunt pathways. SCAPS, which assumes uniform layers, static defect populations, and ideal contacts, naturally underestimates these low-light penalties.

Taken together, the agreement in overall trends and the small but systematic deviations indicate that the strong  $4000\text{ K}$  response arises from the same underlying mechanisms—suppressed interfacial recombination, efficient carrier extraction, and favourable spectral matching—while also revealing the additional interfacial and morphological complexities present in fabricated  $\text{CsPbBr}_3$  devices.

From this analysis, the best performing samples under the annealing temperature were chosen and the corresponding J-V curve is shown in Figure 5.17. The corresponding results are given Tables 5.9.

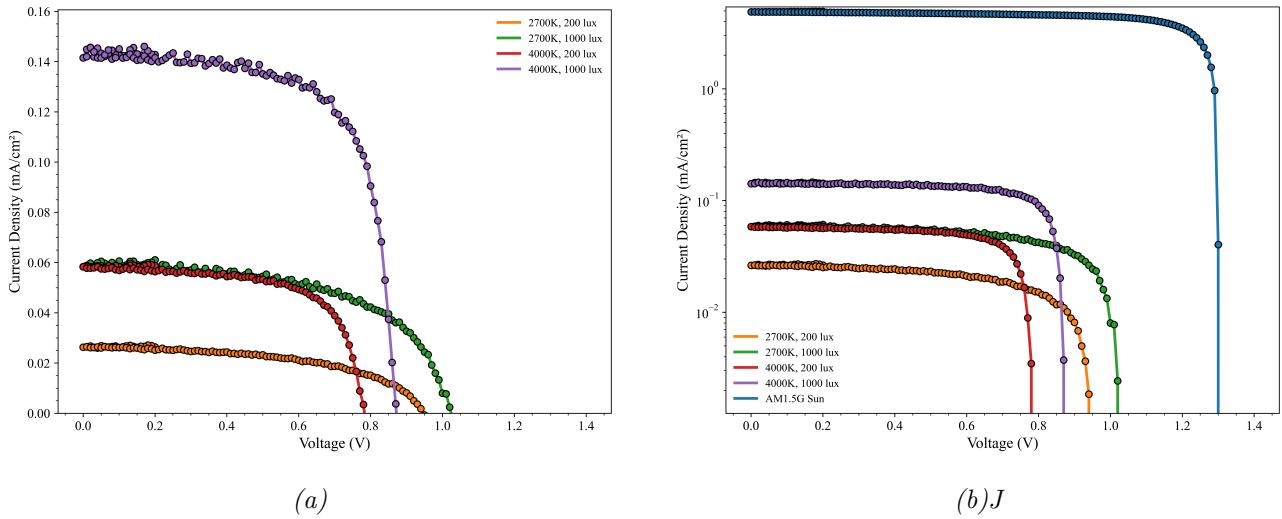


Figure 5.17: *J-V* curves analysis of the optimized samples with ETL-Free Device Architectures (a) LEDs and (b) Comparison with 1-Sun illumination

Method	Illumination	$J_{sc}$ (mA/cm <sup>2</sup> )	FF (%)	$V_{oc}$ (V)	PCE (%)
<b>Experimental Measurement (Without ETL)</b>					
	4000K, 1000 lux	0.14	70.0	0.87	20.77
	4000K, 200 lux	0.06	65.4	0.78	18.12
	2700K, 1000 lux	0.06	58.2	1.02	11.62
	2700K, 200 lux	0.03	53.7	0.95	11.02
	AM1.5G (1-Sun)	4.83	72.4	1.30	4.55

Table 5.9: Experimentally measured performance parameters for  $\text{CsPbBr}_3$  devices without ETL under various illumination conditions.

## 6 Conclusion

This work presents a comprehensive investigation of  $\text{CsPbBr}_3$  perovskite solar cells through a combined approach of numerical SCAPS simulations and systematic experimental measurements. By examining ETL-integrated and ETL-free device architectures across a wide range of annealing temperatures and illumination spectra, we establish a unified understanding of the physical mechanisms governing device performance and identify clear optimization pathways for indoor and outdoor photovoltaic applications. Tables 6.1 and 6.2 show the summarized results for both simulation and experimental measurements for standard device architecture as well as for devices without an ETL.

Method	Illumination	$J_{sc}$ (mA/cm <sup>2</sup> )	FF (%)	$V_{oc}$ (V)	PCE (%)
<b>SCAPS Simulation (With ETL)</b>					
	4000K, 1000 lux	0.171	85.34	1.23	43.86
	4000K, 200 lux	0.068	86.65	1.20	43.43
	2700K, 1000 lux	0.126	85.81	1.22	44.98
	2700K, 200 lux	0.048	87.01	1.19	44.57
	AM1.5G (1-Sun)	7.40	79.97	1.37	8.09
<b>Experimental Measurement (With ETL)</b>					
	4000K, 1000 lux	0.17	77.3	1.21	38.41
	4000K, 200 lux	0.07	71.6	1.19	34.13
	2700K, 1000 lux	0.06	72.4	1.19	22.13
	2700K, 200 lux	0.04	67.3	1.16	25.39
	AM1.5G (1-Sun)	7.22	70.2	1.27	6.45

Table 6.1: Comparison of SCAPS-simulated and experimentally measured performance parameters for  $CsPbBr_3$  devices with ETL under various illumination conditions.

Method	Illumination	$J_{sc}$ (mA/cm <sup>2</sup> )	FF (%)	$V_{oc}$ (V)	PCE (%)
<b>SCAPS Simulation (Without ETL)</b>					
	4000K, 1000 lux	0.171	75.26	1.11	34.81
	4000K, 200 lux	0.067	77.06	1.07	34.44
	2700K, 1000 lux	0.126	74.90	1.09	35.20
	2700K, 200 lux	0.048	76.69	1.06	34.86
	AM1.5G (1-Sun)	7.39	77.40	1.33	7.60
<b>Experimental Measurement (Without ETL)</b>					
	4000K, 1000 lux	0.14	70.0	0.87	20.77
	4000K, 200 lux	0.06	65.4	0.78	18.12
	2700K, 1000 lux	0.06	58.2	1.02	11.62
	2700K, 200 lux	0.03	53.7	0.95	11.02
	AM1.5G (1-Sun)	4.83	72.4	1.30	4.55

Table 6.2: Comparison of SCAPS-simulated and experimentally measured performance parameters for  $CsPbBr_3$  devices without ETL under various illumination conditions.

## 6.1 SCAPS Simulation Insights

SCAPS simulations provide the theoretical foundation for understanding the electronic behaviour of the investigated device structures. In this study, the simulations focused on varying the donor density of the ETL, the acceptor density of the  $CsPbBr_3$  absorber, and the series ( $R_s$ ) and shunt ( $R_{sh}$ ) resistances. These parameters directly influence charge transport, recombination dynamics, and overall device efficiency.

Increasing the ETL donor density enhances electron conductivity and improves band bending at the ETL/perovskite interface, thereby reducing interfacial recombination and increasing  $V_{oc}$  and FF. Similarly, tuning the absorber acceptor density modifies the internal electric field and carrier collection efficiency, with moderate doping levels yielding the best balance between charge separation and recombination suppression. Variations in  $R_s$  and  $R_{sh}$  further reveal the sensitivity of  $\text{CsPbBr}_3$  devices to resistive losses: lower  $R_s$  improves FF and current extraction, while higher  $R_{sh}$  suppresses leakage pathways and enhances voltage retention.

The SCAPS results closely reproduce the experimentally observed trends, confirming that interfacial recombination and resistive losses are the dominant performance-limiting mechanisms. Although the simulated and experimentally measured PCE values differ slightly, the simulation predicts a marginally higher efficiency for the 2700 K LED compared to the 4000 K LED but the  $V_{oc}$  and  $J_{sc}$  match closely to experimental measurements. This discrepancy is due to slight decrease in FF that may arise from minor recombination losses in the SCAPS model that become more pronounced at higher light intensities. Importantly, the simulations highlight the intrinsic advantage of  $\text{CsPbBr}_3$  under low-intensity indoor illumination. Due to its wide bandgap ( $\sim 2.34$  eV) and low intrinsic carrier concentration,  $\text{CsPbBr}_3$  operates closer to the radiative limit under indoor spectra, where recombination is suppressed and quasi-Fermi level splitting is maximized. This provides a mechanistic explanation for the superior indoor performance observed experimentally.

## 6.2 Experimental Performance Trends

Experimental measurements under 2700 K, 4000 K, and AM1.5G (1-Sun) illumination validate the role of ETL thickness, annealing temperature, and device architecture in governing charge carrier dynamics.

For ETL-integrated devices, increasing the ETL thickness from 15 nm to 30 nm and annealing at 300 °C yields the highest and most reproducible performance across all spectra. The convergence of optimal parameters across indoor and outdoor spectra underscores the importance of ETL morphology and thermal processing. These processing conditions consistently yield higher  $V_{oc}$ , FF, and PCE, indicating that the ETL morphology and its interaction with the perovskite layer are most favourable within this thermal window. The optimal performance across both indoor and outdoor spectra suggests that moderate annealing and a 30 nm ETL thickness provide a balanced combination of efficient charge extraction and reduced non-ideal losses.

ETL-free devices exhibit a distinct annealing-dependent behaviour in which the intermediate 300 °C stage consistently serves as a performance minimum. In contrast to ETL inclusive devices, the optimal performance for this simplified architecture is achieved at 250 °C rather than 300 °C. Devices annealed at 250 °C exhibit the highest  $J_{sc}$ , FF, and PCE across all illumination conditions, indicating that this lower thermal budget promotes favourable grain morphology and reduced interfacial recombination. Although  $V_{oc}$  reaches its maximum at 350 °C, the overall device performance is limited by reduced current extraction and fill factor at this temperature. These results show that ETL-free designs, while offering simplified fabrication, require careful thermal optimization to manage band alignment and suppress interfacial recombination leads and do not inherently benefit from higher annealing temperatures. Instead, they serve as valuable diagnostic structures for understanding interfacial and transport limitations that inform the design of optimized ETL-based stacks.

A central aim of this study was to evaluate the suitability of  $\text{CsPbBr}_3$  devices for low-intensity indoor environments, and the combined experimental and simulation results strongly support this conclusion. The devices exhibit significantly higher efficiencies indoors than under 1-Sun illumination. The experimentally measured indoor PCE of 38% under 4000 K illumination, together with the SCAPS-predicted efficiency of 44.98% under 2700 K illumination at 1000 lux, places  $\text{CsPbBr}_3$  among the leading indoor photovoltaic materials. For context,

commercial indoor photovoltaics are dominated by amorphous silicon modules, which typically deliver 10–15% PCE under 1000 lux, and dye-sensitized solar cells, which reach 20–30% depending on dye chemistry and spectrum. At the high-performance end, III–V microcells can exceed 40% PCE but require complex, rigid, and expensive fabrication [24]. The indoor efficiencies achieved in this work—38% experimentally and up to 44% in SCAPS simulations—place  $\text{CsPbBr}_3$  devices among the strongest performers in this landscape.

The strong spectral alignment between the 2.34 eV bandgap and indoor LED emission enables operation close to the radiative limit, yielding high  $V_{oc}$  and suppressed thermalization losses. Although the simulations do not explicitly model annealing temperature, the experimentally relevant parameters varied in SCAPS—absorber doping, interface defect density, shunt resistance, and ETL donor density—collectively reproduce the same qualitative trends observed in measurements, including the performance minimum at 300 °C and the superior response under 4000 K illumination. Taken together, these results show that  $\text{CsPbBr}_3$  is not only more efficient indoors than outdoors, but also genuinely competitive with the best available indoor photovoltaic technologies, while offering the additional advantages of low-temperature, solution-based fabrication and bandgap tunability.

### 6.3 Future Integration of SCAPS and Its Limitations

The similarity between SCAPS simulations and experimental measurements demonstrates the value of simulation analysis for future device optimization. SCAPS can be further integrated into performance studies by:

- Predicting optimal ETL/perovskite band alignment for emerging transport materials.
- Quantifying the influence of interface defect densities and guiding targeted passivation strategies.
- Simulating device behaviour under diverse indoor lighting spectra to tailor absorber bandgaps for specific applications.
- Exploring alternative device architectures (ETL-free, HTL-free, tandem structures) prior to fabrication.
- Identifying recombination bottlenecks and transport limitations before committing to experimental iterations.

However, SCAPS also presents inherent limitations that must be considered when interpreting simulation results:

- **One-dimensional approximation:** SCAPS models devices in 1D, neglecting lateral inhomogeneities, grain-boundary effects, and pixel-level variations.
- **Idealized interfaces:** Interface chemistry, ion migration, and dynamic defect formation cannot be fully captured.
- **Static simulations:** Time-dependent processes such as hysteresis, degradation, and ion drift are not modelled.
- **Simplified optical modelling:** Accurate spectral predictions require high-quality user-provided optical data.
- **Limited multi-physics capabilities:** Thermal, mechanical, and chemical degradation pathways cannot be simulated.

Despite these limitations, SCAPS remains a useful tool for guiding experimental design. When combined with targeted measurements, it accelerates the development of high-efficiency, application-specific perovskite photovoltaics.

#### 6.4 Overall Significance

Together, the simulation and experimental results establish a robust design framework for  $\text{CsPbBr}_3$  perovskite solar cells. Optimal ETL thickness (25–30 nm) and annealing temperature 300 °C maximize performance in ETL-based devices. In contrast, ETL-free architectures require a higher thermal budget of 350 °C to overcome the lack of a selective transport layer and achieve competitive efficiencies.

The superior indoor performance of  $\text{CsPbBr}_3$ -enabled by its wide bandgap of 2.34eV, suppressed non-radiative recombination under low-intensity flux, and favorable spectral matching with LED sources—positions this material as a leading candidate for next-generation indoor photovoltaics. This work provides actionable guidelines for scalable fabrication, showing that thermal processing must be specifically tailored to the device architecture (ETL vs. ETL-free) and intended application.

The performance characteristics demonstrated in this work directly align with the power requirements of modern Internet-of-Things (IoT) devices, including environmental sensors, wireless communication modules, asset-tracking tags, and autonomous low-power nodes. Such systems typically operate with average power budgets in the 10–200  $\mu\text{W}$  range, with short transmission bursts reaching a few milliwatts. Under 4000 K, 1000 lux illumination, the optimized  $\text{CsPbBr}_3$  devices in this study deliver 35–38% PCE experimentally (and up to 44% in SCAPS simulations), corresponding to power outputs well above the thresholds needed to sustain continuous IoT operation, even in dim indoor environments.

These results demonstrate that  $\text{CsPbBr}_3$  indoor photovoltaics are not only more efficient indoors than under 1-Sun illumination, but are also suitable for powering IoT devices. Their combination of high indoor efficiency and stable voltage output positions them as a compelling platform for autonomous indoor energy harvesting.

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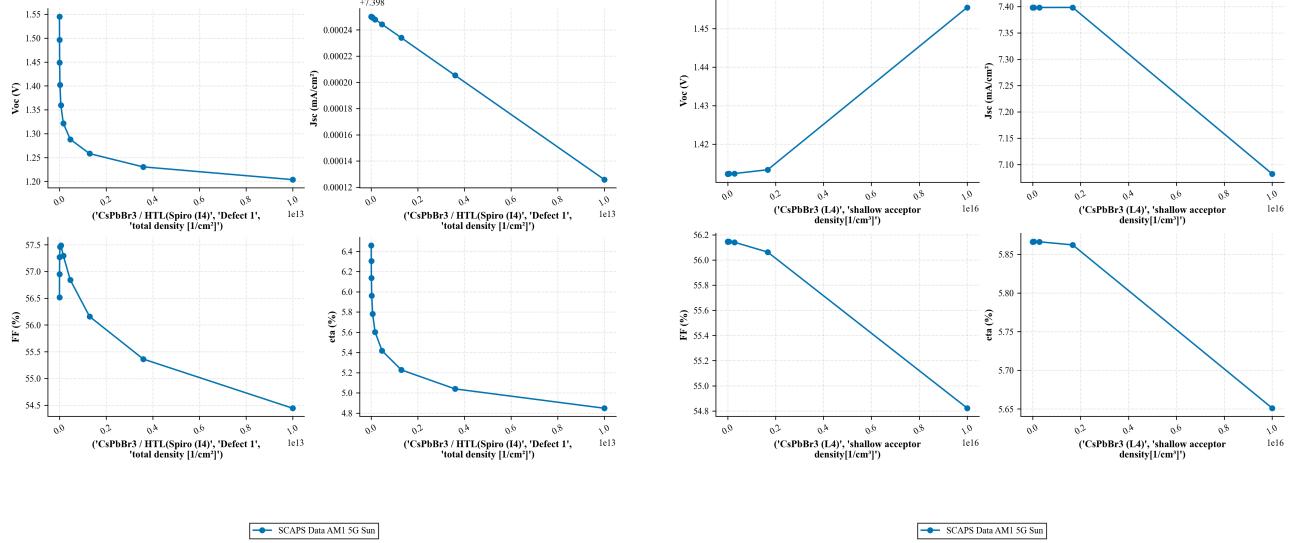
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## A Appendix A: SCAPS trend analysis results under AM1.5G (1-Sun) illumination

### A.1 Results for standard device architecture

The Figures A.1, A.2 and A.3 show the trends in device performance for standard device architecture under AM1.G Sun.



(a) Influence of Absorber layer/HTL interface defect density under AM1.G (1-Sun)

(b) Influence of Absorber Layer Shallow Acceptor Density

Figure A.1: Influence of AL-HTL Interface defect density and Absorber shallow acceptor density on device performance under AM1.G (1-Sun)

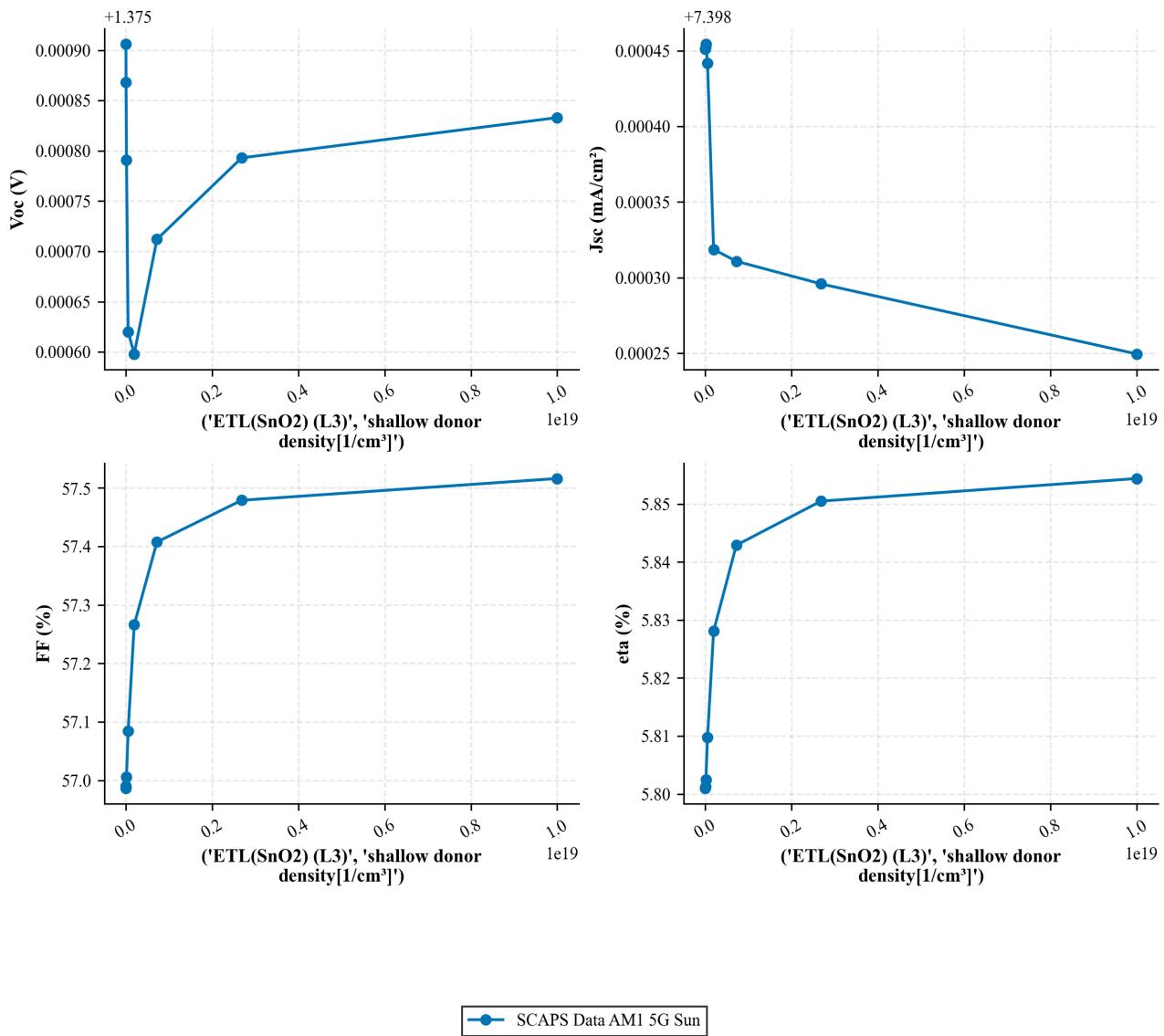
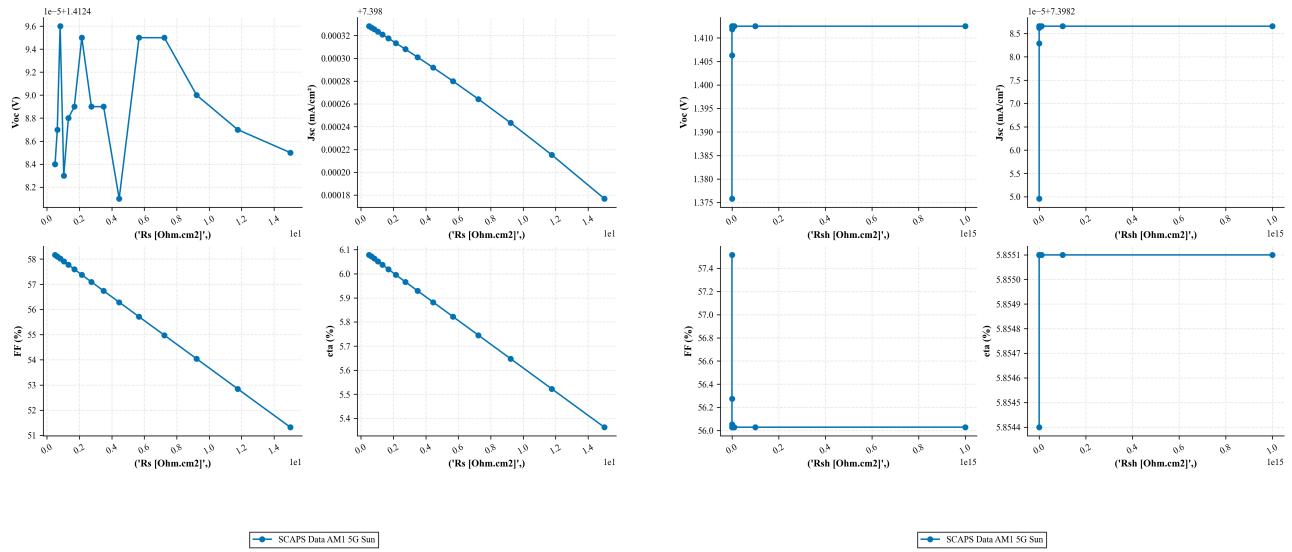


Figure A.2: Influence of ETL shallow donor density on device performance under AM1.G Sun

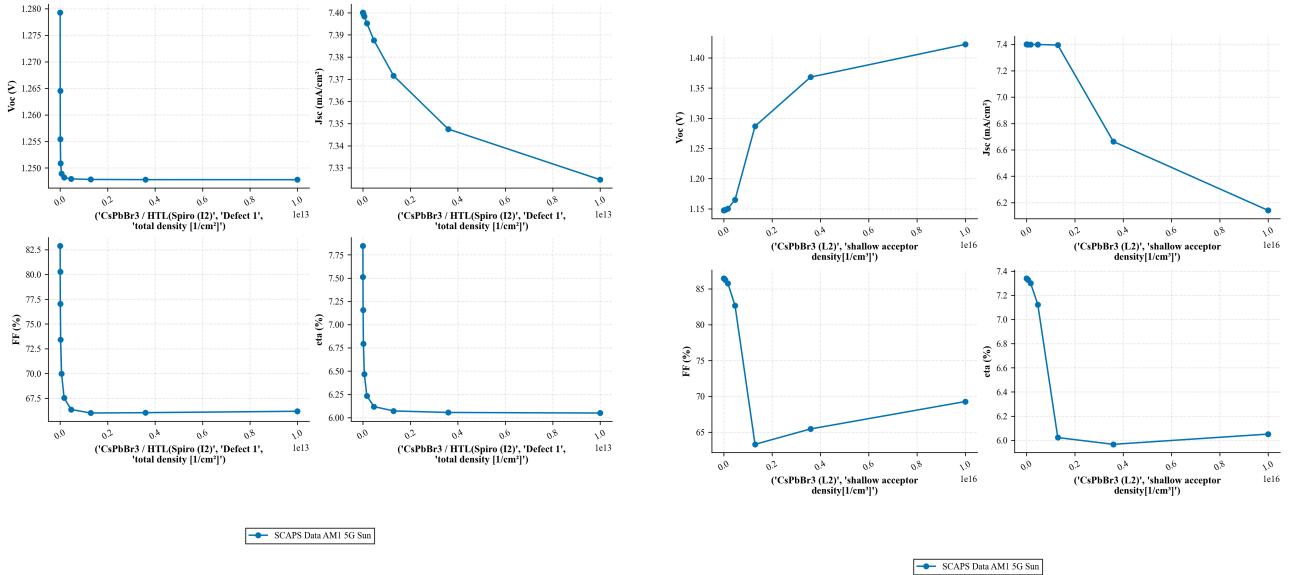


*Figure A.3: Influence of Series and Shunt Resistance on device performance under AM1.G Sun*

**A.1.0.1 Comparative Analysis:** SCAPS simulations for the ETL-based  $\text{CsPbBr}_3$  device under AM1.5G (1-Sun) reveal that interfacial defect density and absorber doping are the dominant levers for  $V_{oc}$  and overall efficiency. Increasing HTL defect density sharply degrades  $V_{oc}$  and  $\eta$ , while excessive absorber doping improves voltage but reduces  $J_{sc}$  and FF due to enhanced recombination. ETL donor density acts as a transport threshold—above  $10^{18} \text{ cm}^{-3}$ , FF stabilizes and PCE plateaus. Series resistance ( $R_s$ ) linearly erodes FF and  $\eta$ , while shunt resistance ( $R_{sh}$ ) primarily affects  $J_{sc}$  and voltage retention. These trends confirm that interface quality and balanced doping are critical for optimizing ETL-based  $\text{CsPbBr}_3$  devices.

## A.2 Results for device without ETL

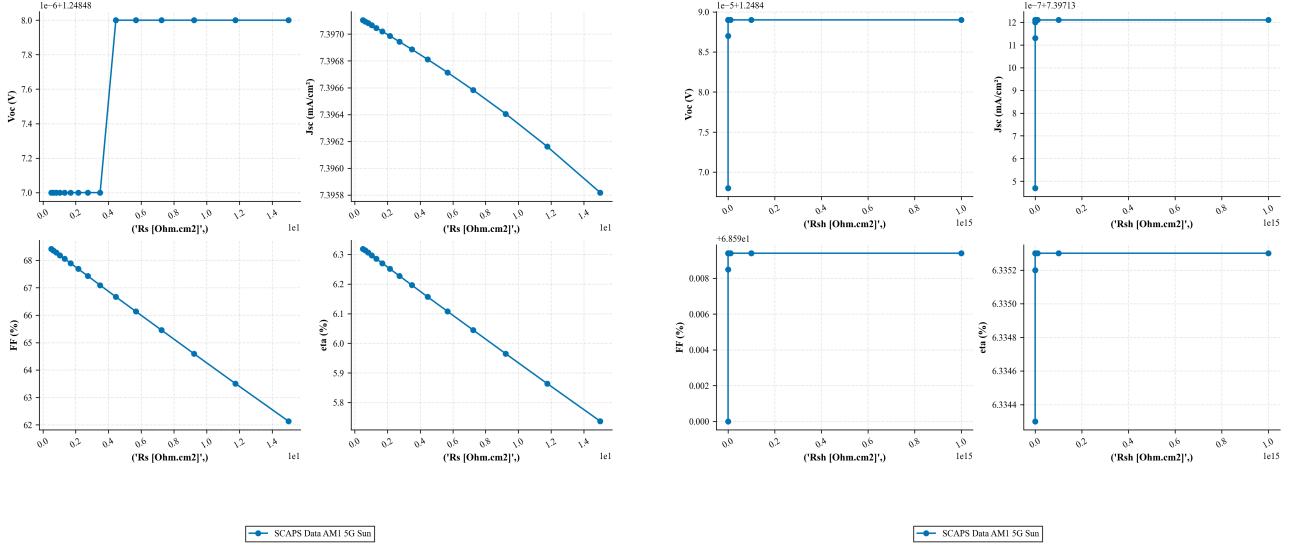
The Figures A.4 and A.5 show the trends in device performance for device without ETL under AM1.G Sun.



(a) Influence of Absorber layer/HTL interface defect density on device without ETL under AM1.5G (1-Sun)

(b) Influence of Absorber Layer Shallow Acceptor Density on device without ETL under AM1.5G (1-Sun)

Figure A.4: Influence of Absorber layer/HTL interface defect density and Absorber Layer Shallow Acceptor Density on device without ETL under AM1.5G (1-Sun)



(a) Influence of Series Resistance ( $R_s$ ) on device without ETL under AM1.5G (1-Sun)

(b) Influence of Shunt Resistance ( $R_{sh}$ ) on device without ETL under AM1.5G (1-Sun)

Figure A.5: Influence of series Resistance ( $R_s$ ) and Shunt Resistance ( $R_{sh}$ ) on device without ETL under AM1.5G (1-Sun)

**A.2.0.1 Comparative Analysis :** For the ETL-free CsPbBr<sub>3</sub> device under AM1.5G (1-Sun), SCAPS simulations again highlight interface quality, absorber doping, and parasitic resistances as the key performance drivers. Increasing the HTL interfacial defect density leads to a simultaneous degradation of  $V_{oc}$ ,  $J_{sc}$ , FF, and PCE, confirming that recombination at the perovskite/HTL contact is a primary loss channel when no ETL is present. Variation of the absorber shallow acceptor density shows that  $V_{oc}$  increases with  $N_A$ , while  $J_{sc}$  and PCE decrease and FF becomes non-optimal at both very low and high doping, indicating a narrow window where

built-in potential and recombination are balanced. As in the ETL-based device, increasing series resistance  $R_s$  mainly erodes FF and PCE (with only minor changes in  $V_{oc}$  and  $J_{sc}$ ), whereas higher shunt resistance  $R_{sh}$  improves all performance parameters by suppressing leakage currents. Overall, these results show that, even without an ETL, device efficiency under 1-sun is governed by the interplay of HTL interface recombination, optimized absorber doping, and careful control of  $R_s$  and  $R_{sh}$ .

## B Appendix B: Performance Analysis of HTL-Free Device Architectures

The Figure B.1 show the performance analysis of HTL-Free Device Architectures

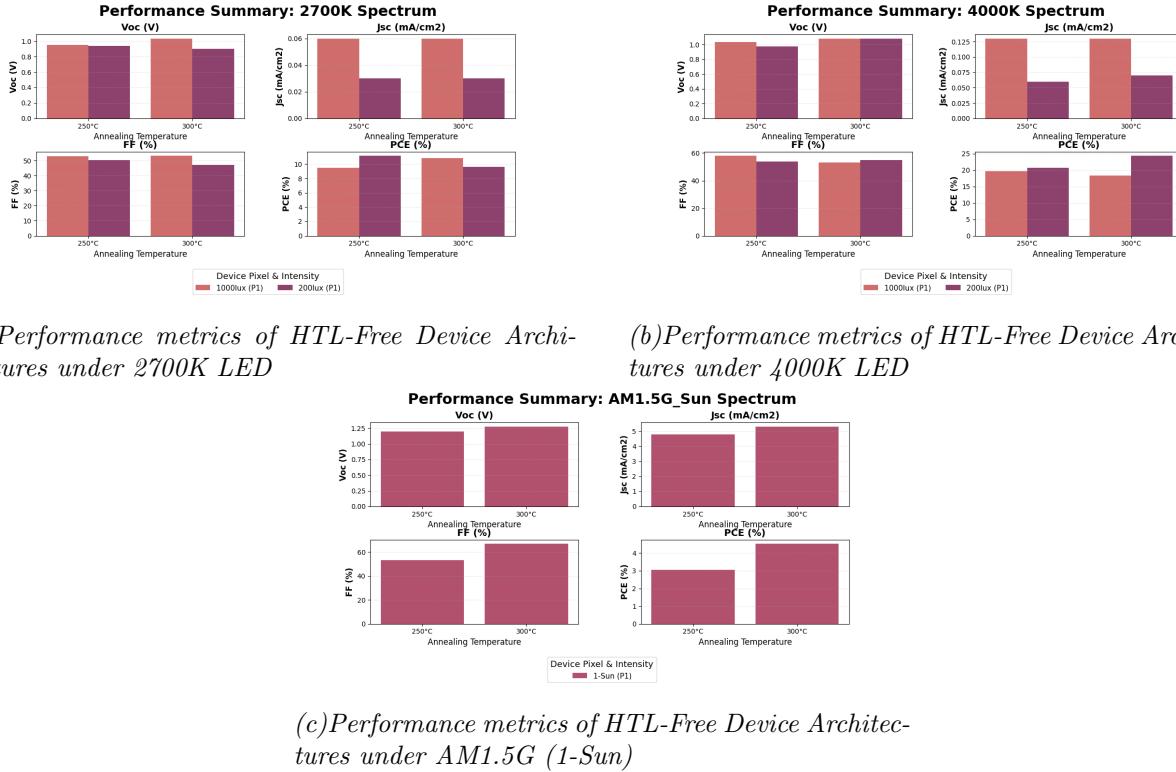


Figure B.1: Performance metrics of HTL-Free Device Architectures under AM1.5G (1-Sun) and LED light

**B.0.0.1 Statistical Analysis:** For the HTL-free  $\text{CsPbBr}_3$  device, the statistical trends under 2700 K, 4000 K, and AM1.5G (1-Sun) illumination show that annealing temperature and light intensity jointly govern the trade-off between voltage, current, and overall stability. Under 2700 K and 4000 K indoor spectra, increasing the illumination from 200 lux to 1000 lux consistently enhances  $J_{sc}$  and PCE, while  $V_{oc}$  remains relatively stable and FF shows only modest variation, indicating that the HTL-free architecture can still harvest ambient light efficiently when interfacial degradation is limited. Comparing 250 °C and 300 °C annealing, the higher temperature generally improves  $V_{oc}$ , FF, and PCE across all spectra, with the most pronounced gains observed under AM1.5G (1-Sun) (from ~3% to ~4.5% PCE), reflecting improved charge transport and reduced non-ideal losses. However, the stronger relative enhancement at 1-Sun compared to indoor conditions also suggests that the HTL-free structure remains more sensitive to recombination and resistive losses, reinforcing the role of selective contacts and optimized interfaces in fully exploiting the wide-bandgap absorber.

## C Appendix C: Simulation Capabilities and Outputs of SCAPS

SCAPS allows simulation under both dark and illuminated conditions, with variable bias voltages.

The SCAPS Action Panel serves as the central interface for executing and managing simulations of photovoltaic device behavior. It allows users to initiate calculations for key performance metrics such as current–voltage (I–V) characteristics, quantum efficiency (QE), capacitance–voltage (C–V) profiles, energy band diagrams, and generation–recombination dynamics. Through this panel, users can control simulation conditions, toggle between dark and illuminated modes, and access detailed graphical outputs to analyze charge transport, recombination mechanisms, and electrostatic profiles. This functionality is essential to systematically evaluate the performance of the device under varied physical and environmental conditions Figure C.1.

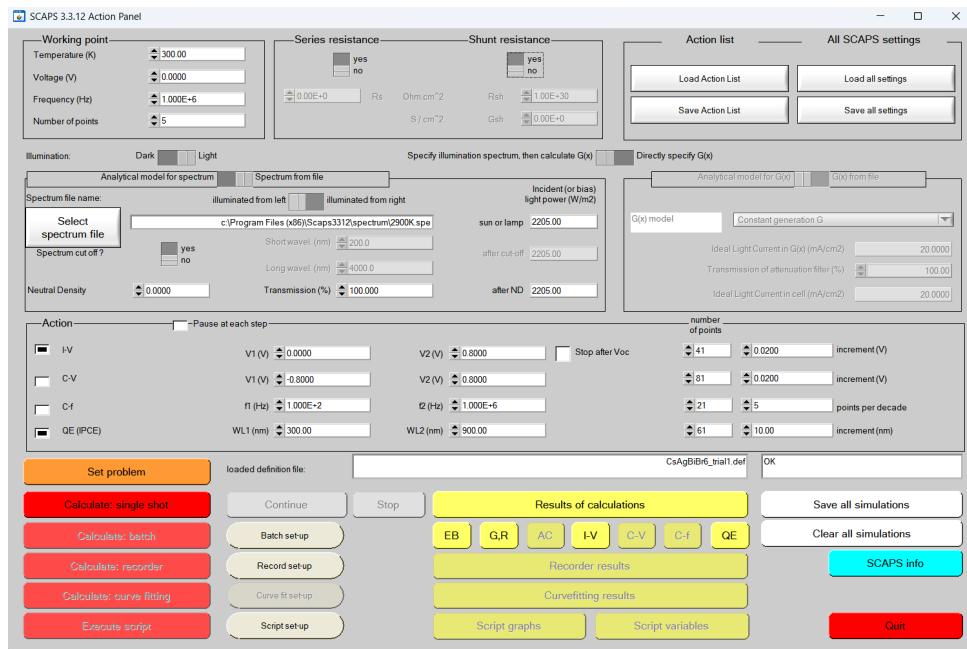


Figure C.1: Action Panel in SCAPS

It supports the extraction of key device characteristics, including:

- Current-voltage (I-V) curves: The SCAPS I-V Panel provides information about the characteristics of J-V, current density ( $J_{sc}$ ) and recombination rate distributions Figure C.2.

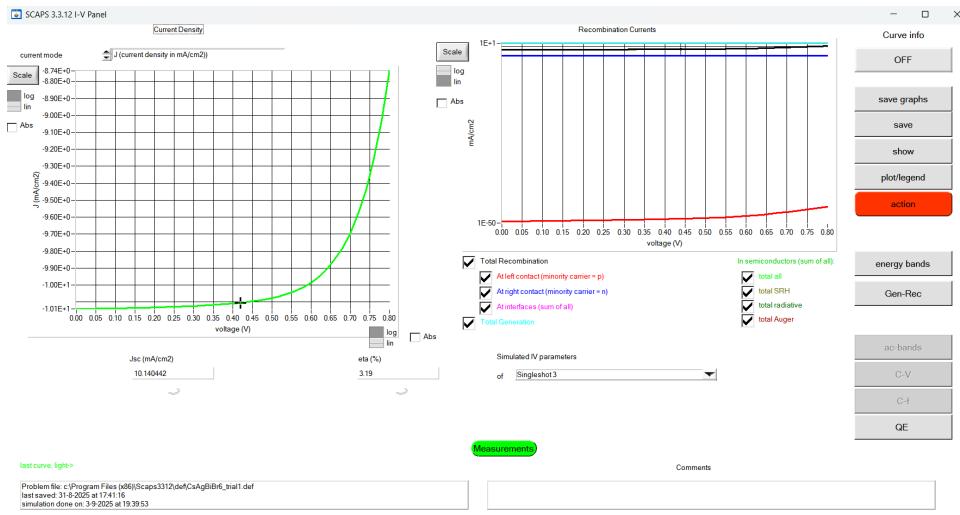


Figure C.2: I-V Panel in SCAPS

- Capacitance-voltage (C–V) and admittance spectra: The Capacitance–Voltage (C–V) panel in SCAPS provides insight into the electrostatic behavior of a solar cell by analyzing how capacitance, conductance, and carrier selectivity vary with applied bias. It also visualizes the doping profile across the depletion region, enabling extraction of built-in potential and doping concentrations, which are essential for evaluating junction quality and charge transport dynamics Figure C.3.

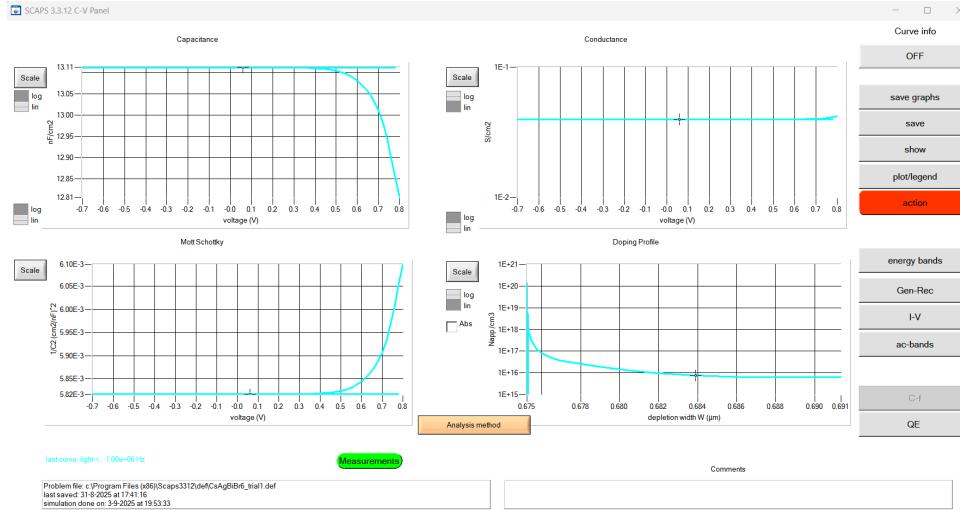


Figure C.3: C-V Panel in SCAPS

- External quantum efficiency (EQE): The Quantum Efficiency (QE) panel in SCAPS provides a wavelength-resolved analysis of how effectively a solar cell converts incident photons into collected charge carriers. The external quantum efficiency (EQE) curve is displayed, which reflects the combined influence of optical absorption, carrier generation, transport, and recombination across the device. By examining the spectral response, researchers can identify the active absorption range, assess losses due to poor material interfaces or recombination, and validate simulation parameters against experimental EQE data. This panel is essential for optimizing absorber properties and evaluating the overall performance of the device Figure C.4.

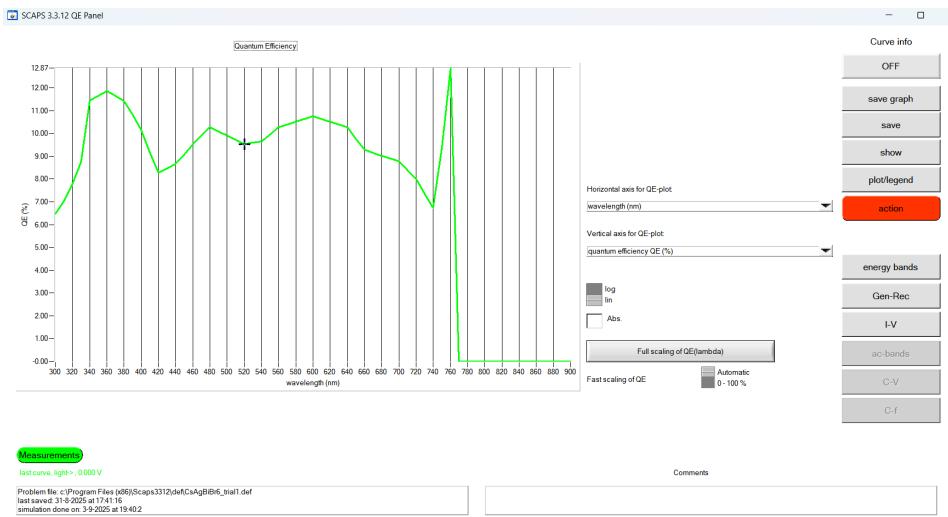


Figure C.4: QE Panel in SCAPS

- Band diagrams and carrier profiles: The Energy Bands panel in SCAPS provides a spatially resolved visualization of the electronic structure across the solar cell, including conduction and valence band edges, quasi-Fermi levels, and total charge distribution. This enables a detailed analysis of band alignment, built-in electric fields, and carrier separation mechanisms under various bias conditions. By examining band bending and quasi-Fermi level splitting, researchers can assess the effectiveness of charge extraction, identify recombination zones, and evaluate the impact of interface energetics on open-circuit voltage and overall device performance Figure C.5.

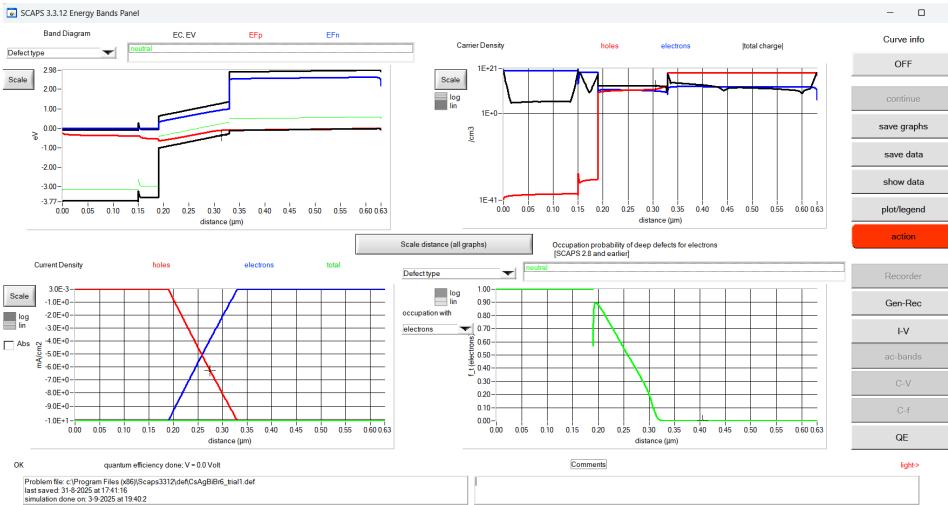


Figure C.5: Energy Bands Panel in SCAPS

- Recombination rate distributions and electric field maps: The Generation–Recombination panel in SCAPS provides a spatially resolved analysis of carrier generation and recombination mechanisms across the solar cell structure. It visualizes total generation rates alongside radiative, Auger, and Shockley–Read–Hall (SRH) recombination profiles, enabling identification of dominant loss pathways and their spatial localization. This panel is essential for evaluating the interplay between optical absorption, carrier lifetime, and defect density, offering insights into how material properties and layer interfaces influence charge carrier dynamics and overall device performance Figure C.6.

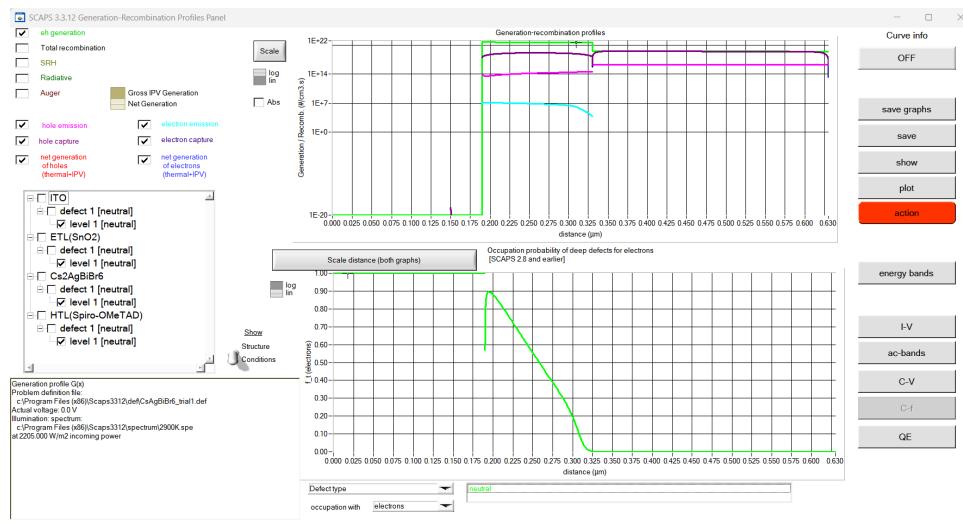


Figure C.6: Generation–Recombination panel in SCAPS

(The examples in the screenshot are for the simulations performed for one of the models described in [5])

These outputs provide valuable information about device performance, allowing optimization of layer structures, identification of limiting mechanisms, and evaluation of defect-related losses.

# **Eidesstattliche Erklärung**

Hiermit versichere ich, die vorliegende Forschungsarbeit selbstständig und nur unter Verwendung der von mir angegebenen Quellen und Hilfsmittel verfasst zu haben.

**Ort, Datum**

**Unterschrift** \_\_\_\_\_