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MICROCHIP

PIC - Microcontrollers and Embedded Systems



PIC16F877A Architecture-Configuration & PCB

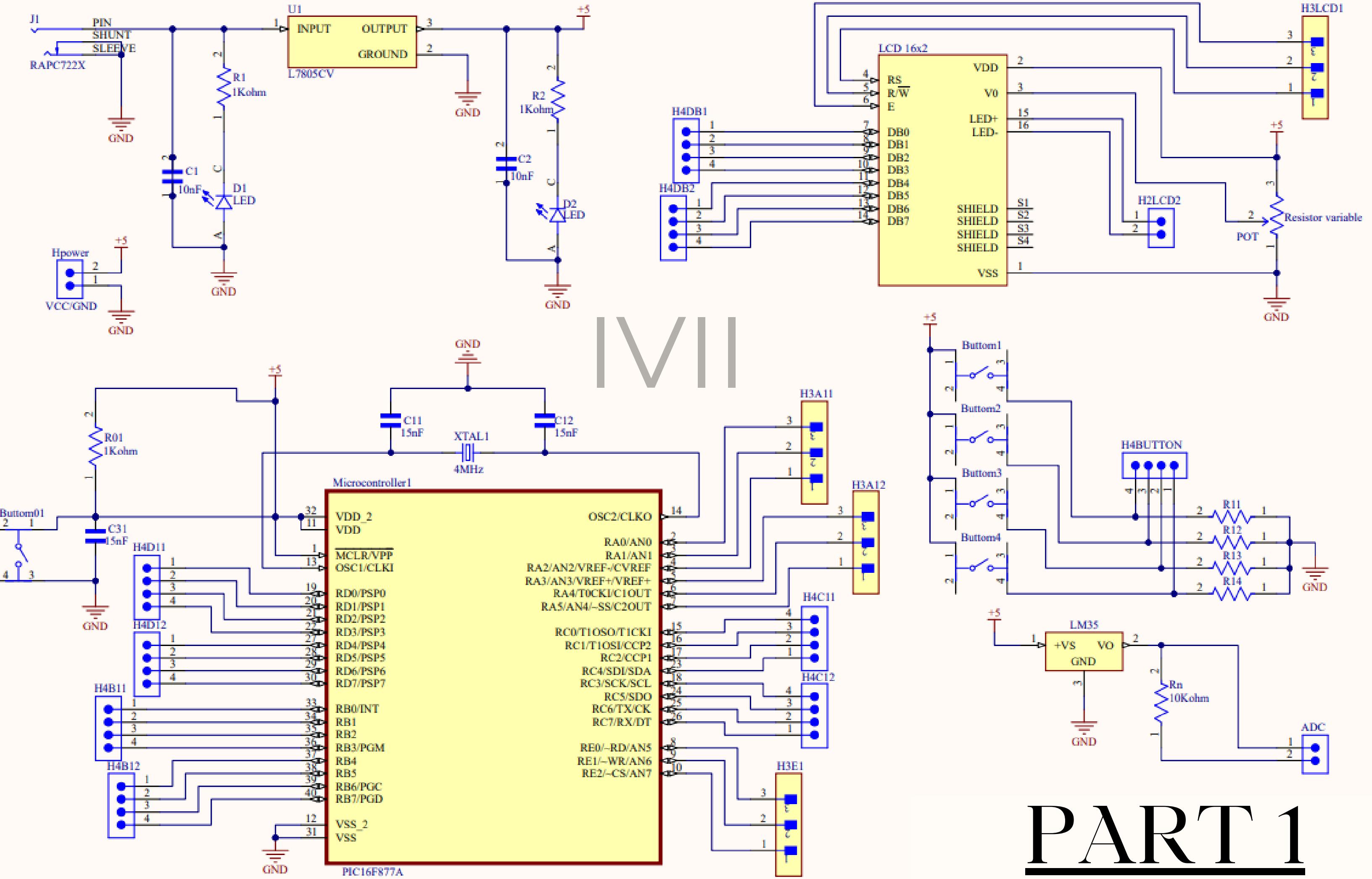
SOULAYMANE AZZOUZ

Prof.TAJEDDIN ELHAMAD APPLICATIONS



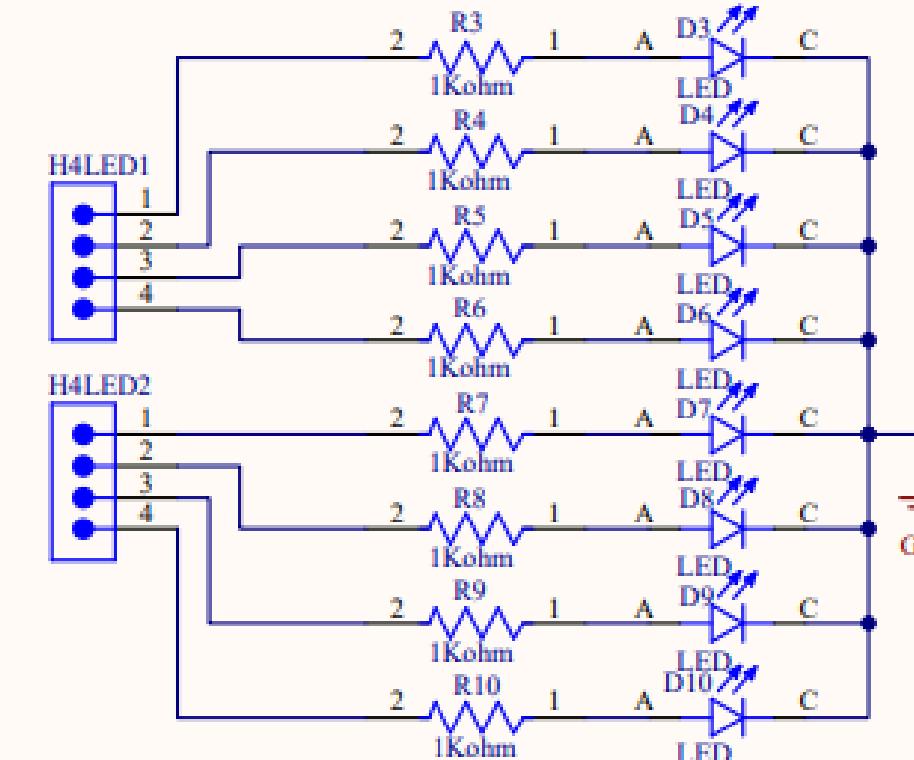
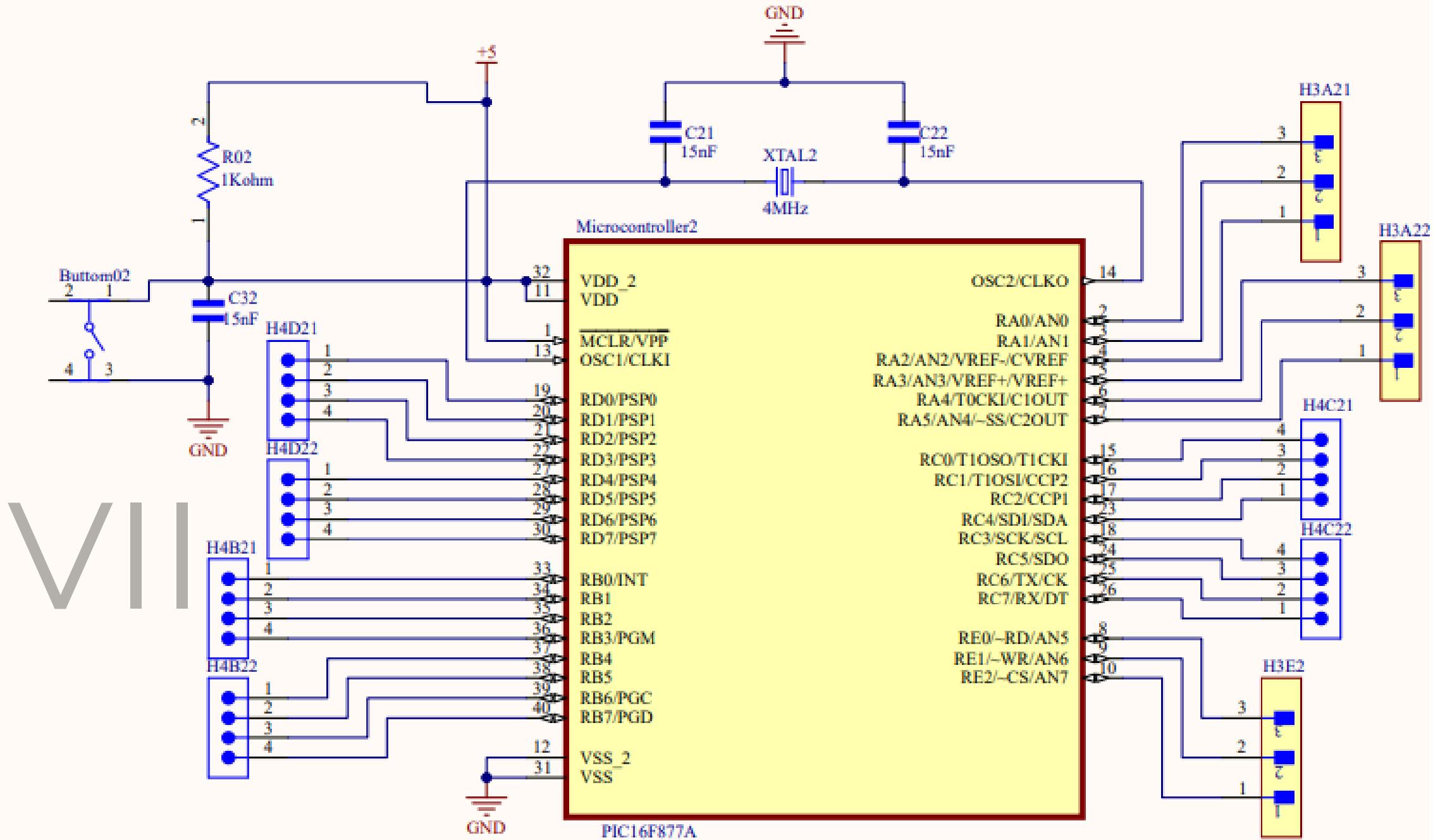
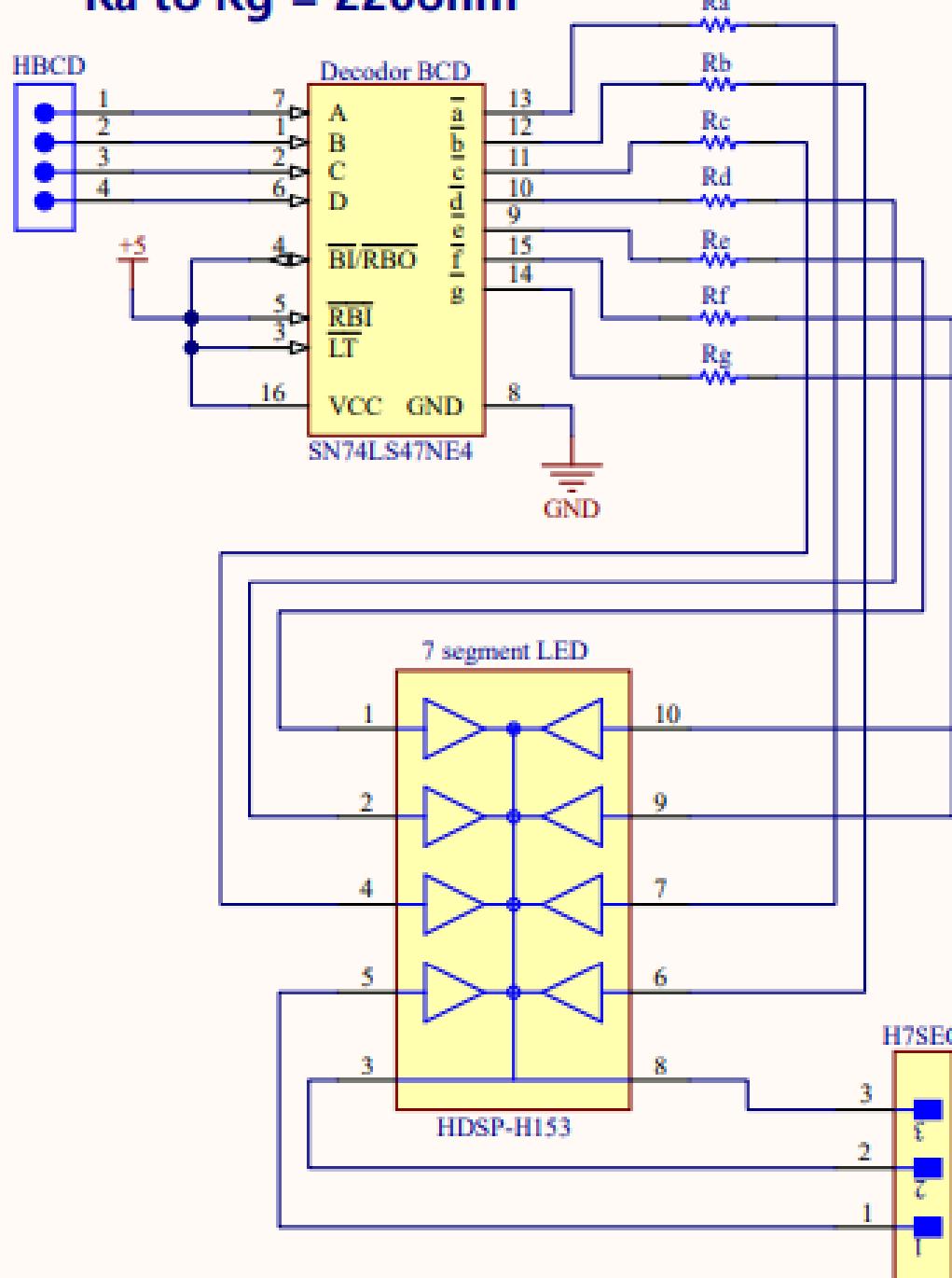
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PCB DESIGN





R_a to R_g = 220ohm

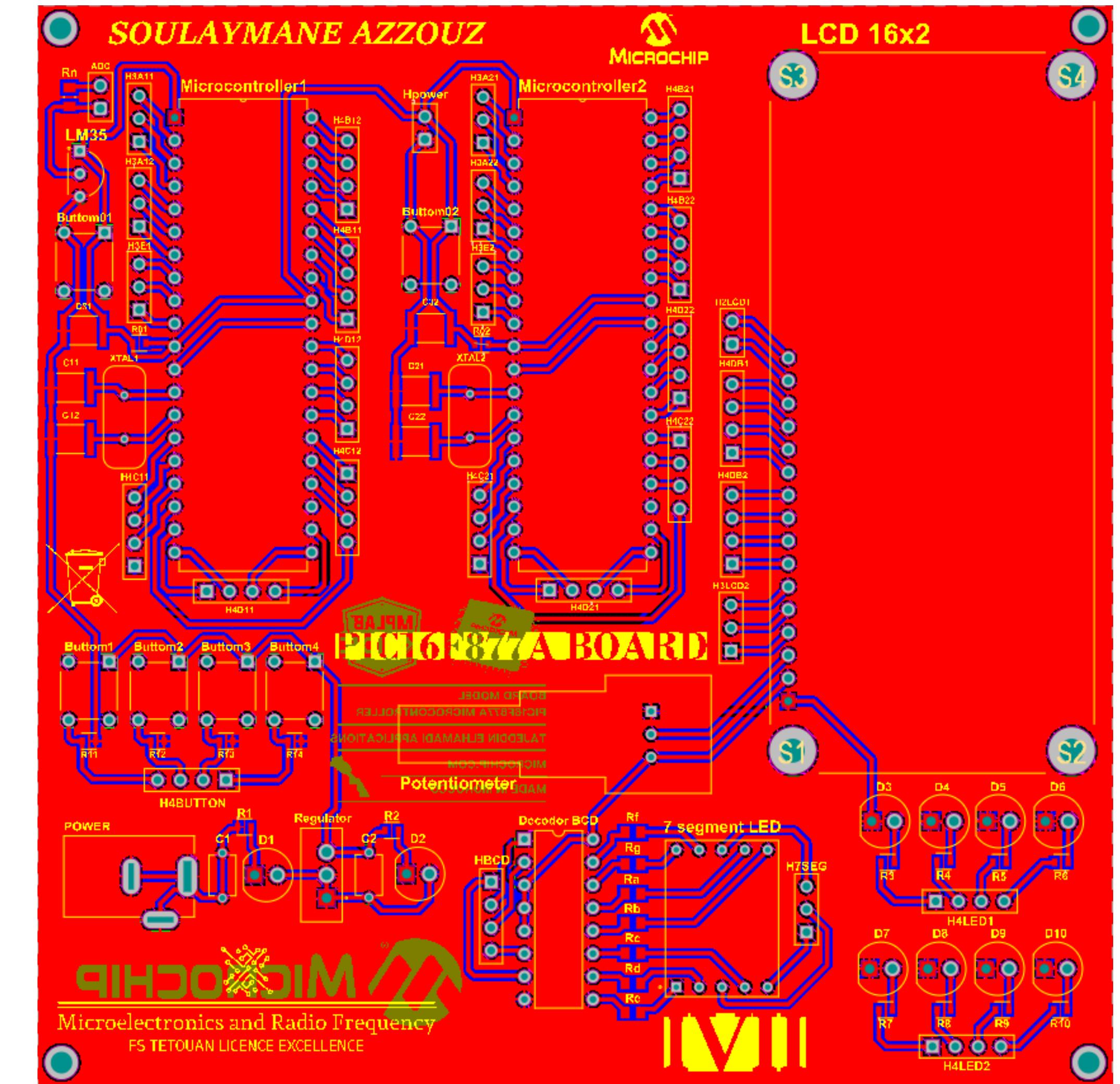


PART 2



2D VIEW

PIC16F877A PCB BOARD





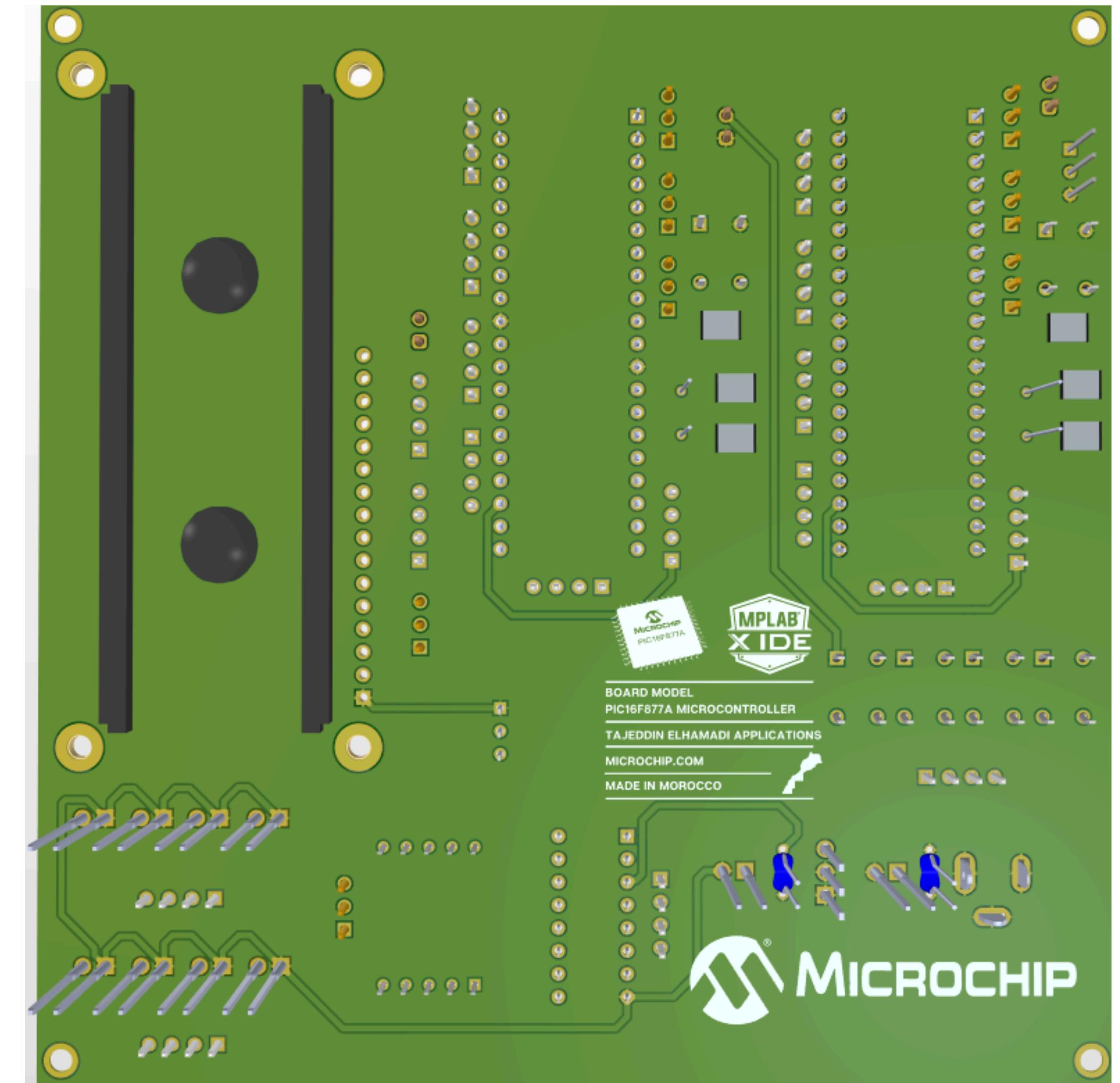
3D VIEW

PIC16F877A

PCB BOARD

BOTTOM

LAYER



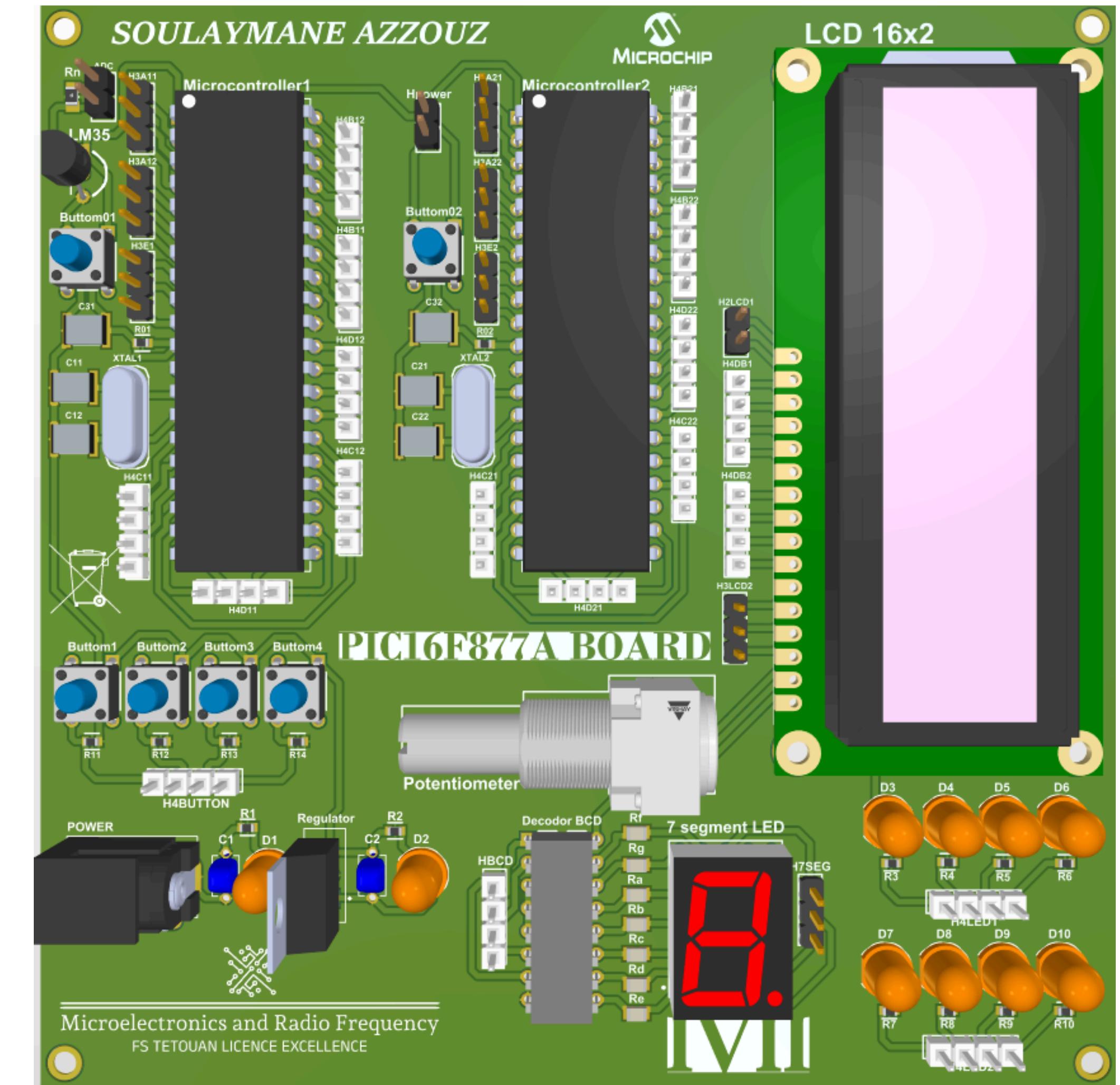


3D VIEW

PIC16F877A

PCB BOARD

TOP LAYER





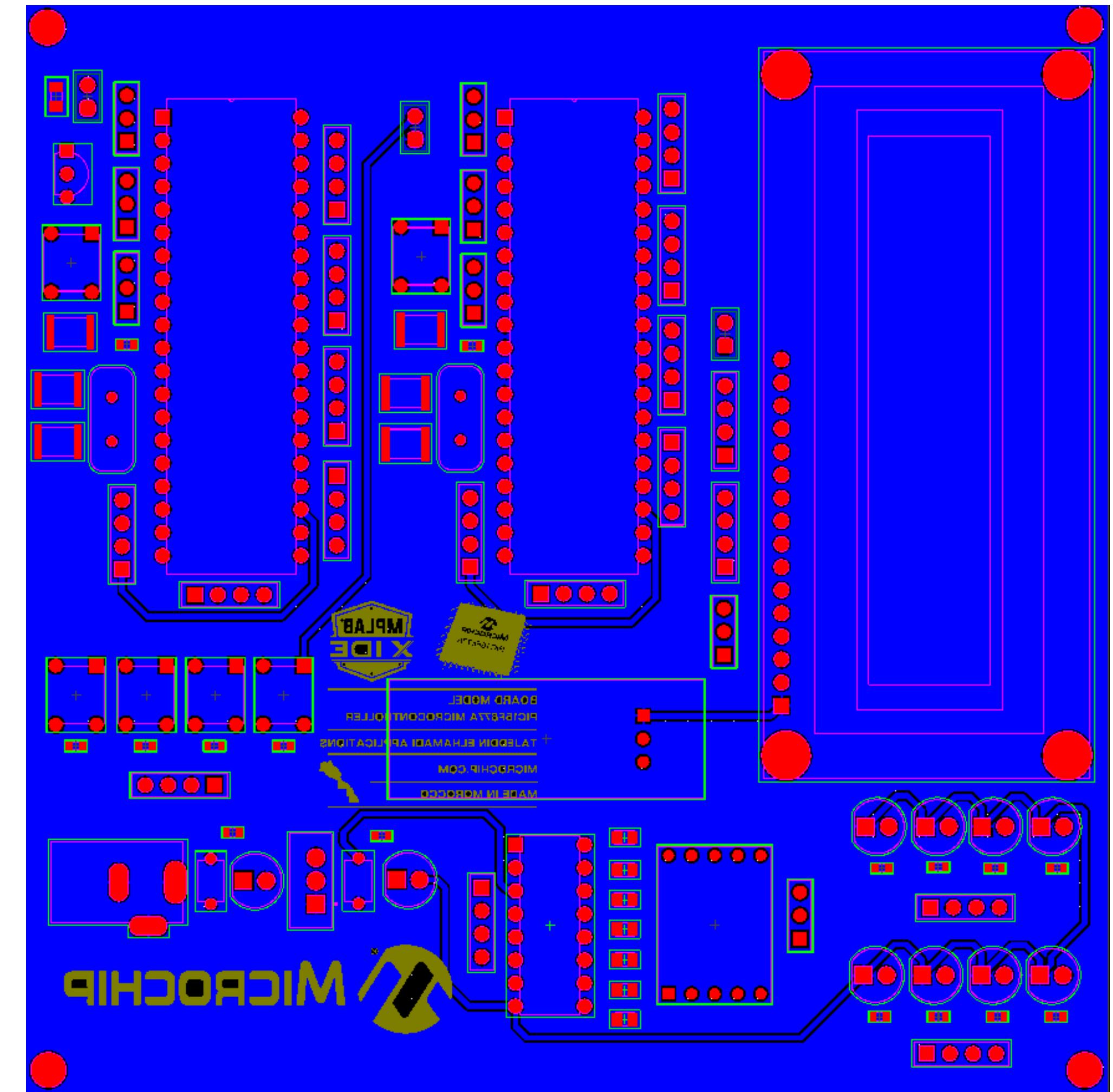
MANUFACTURING

PIC16F877A

PCB BOARD

GERBER

FILE





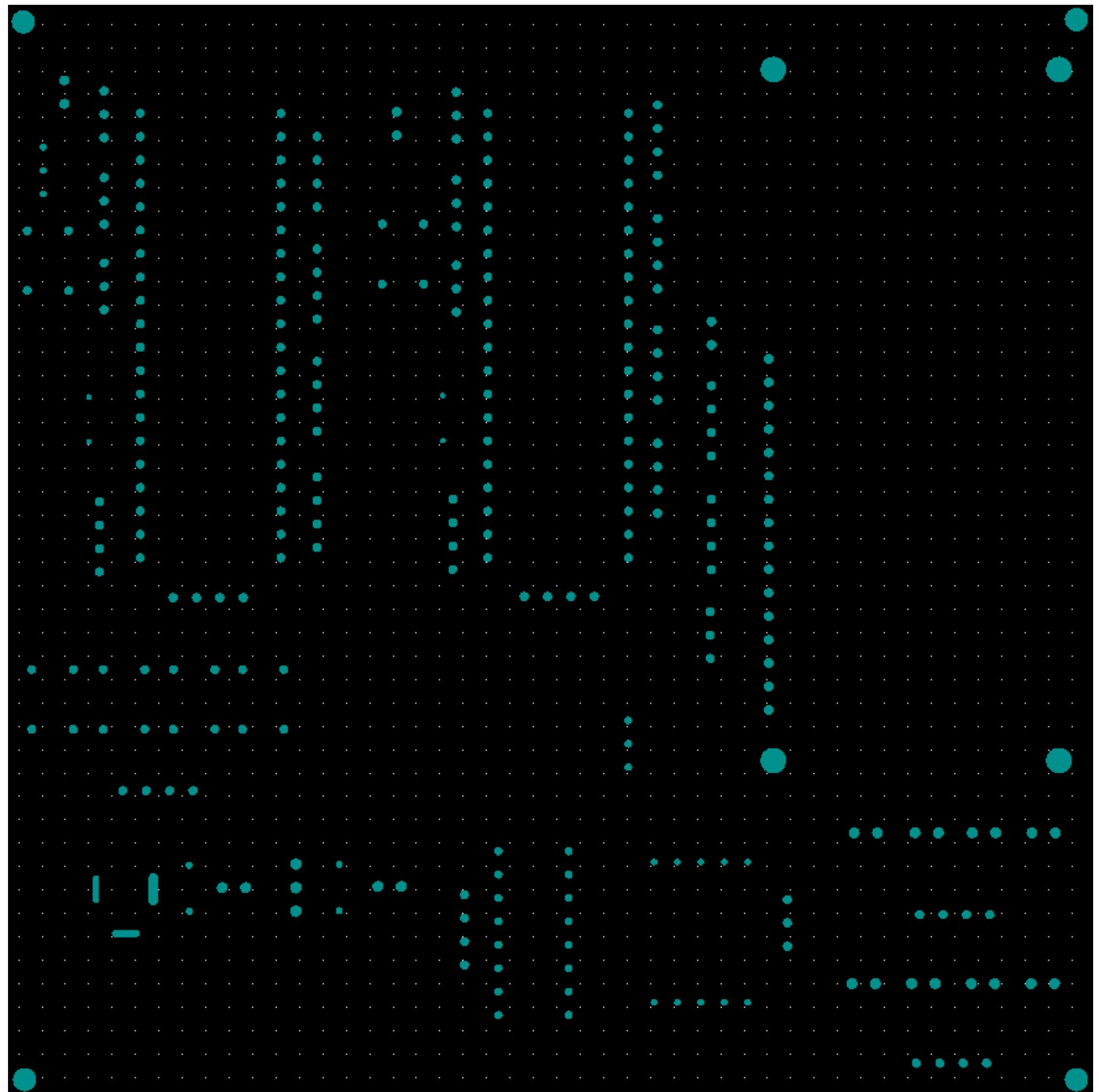
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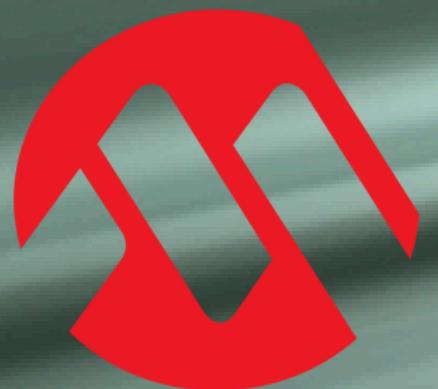
PIC16F877A

PCB BOARD

NC DRILL

FILE





MICROCHIP

PIC16F877A ARCHITECTURE



PINS DIAGRAM

1- The PIC16F877A is an 8-bit microcontroller from Microchip Technology, part of the PIC16 family, widely used for embedded applications due to its versatility, ease of use, and robust features. It is based on the Harvard architecture, meaning it has separate memory spaces for program instructions and data, allowing for more efficient processing.

2- The PIC16F877A microcontroller has a RISC (Reduced Instruction Set Computing) architecture, which simplifies the instruction set, making it easier to learn and use. It contains 35 single-word instructions, which are executed in one cycle (except for program branches).

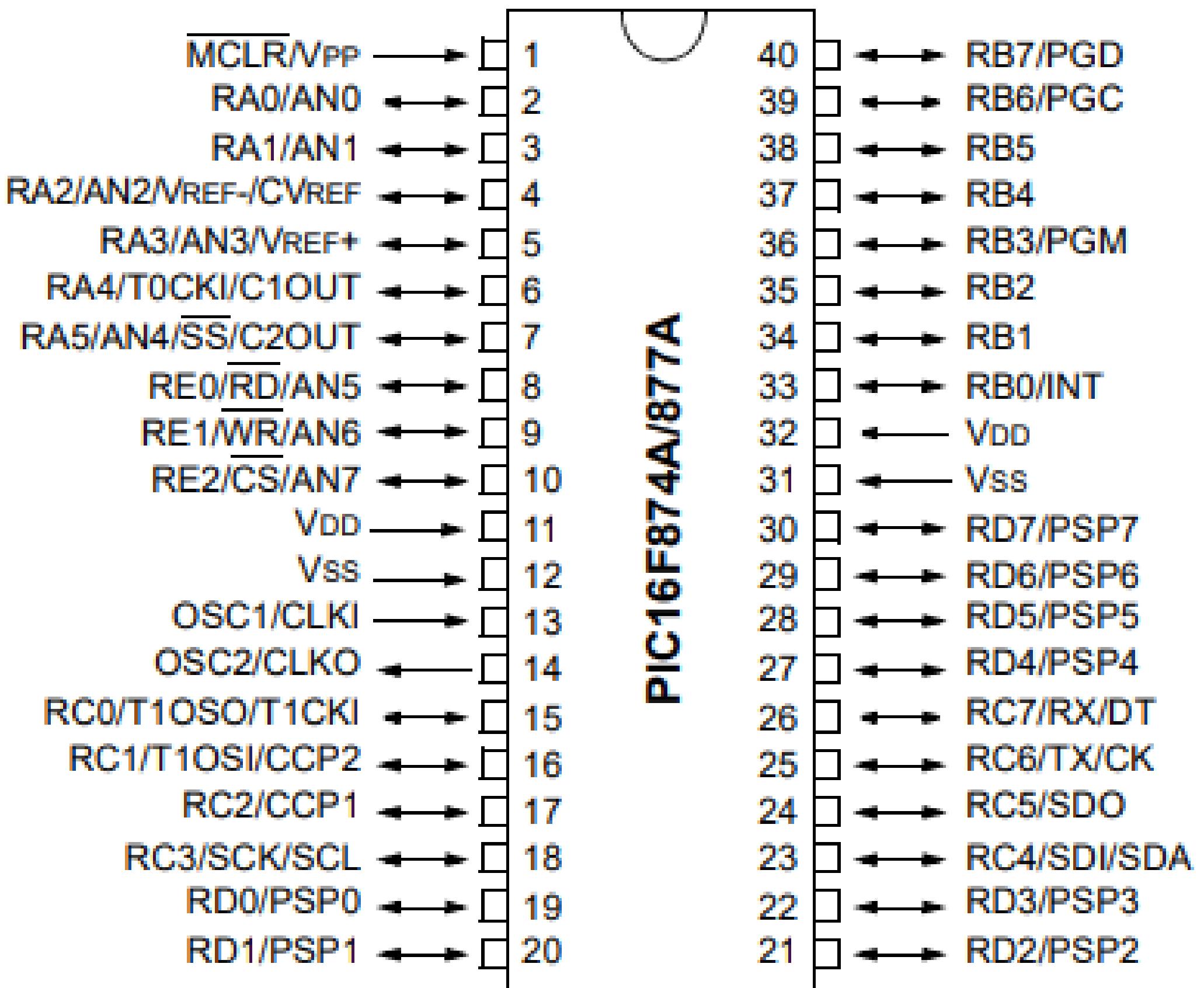


Figure 1 : PIC16F877A Pins Diagram



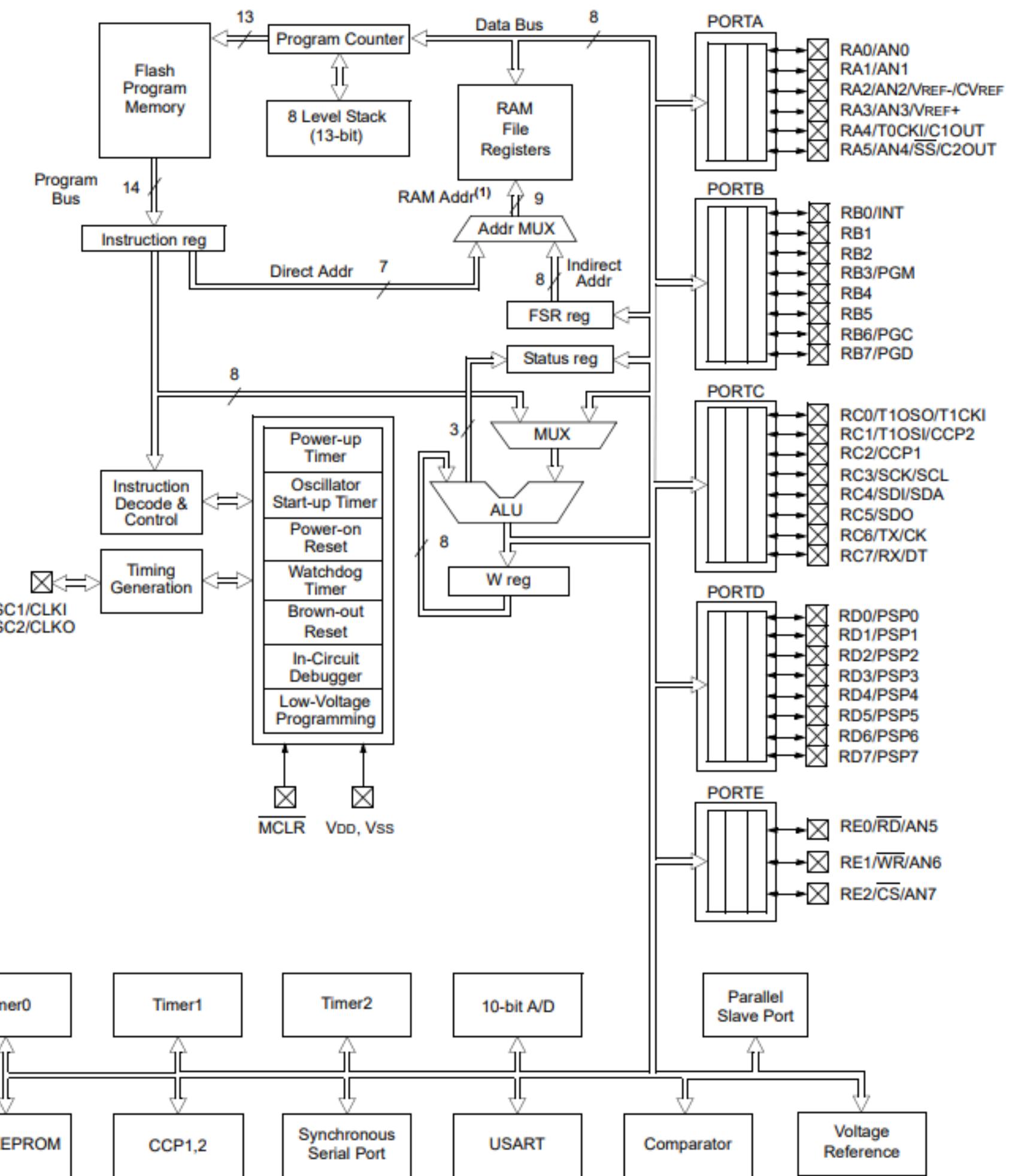
BLOCK DIAGRAM

Note :

- Higher order bits are from the Status register.

The characteristics of the PIC16F877A :

- Device : PIC16F877A
- Program Flash : 8K words
- Data Memory : 368 Bytes
- Data EEPROM : 256 Bytes





REGISTER MAP

Note :

- 1- These registers are not implemented on the PIC16F876A.
- 2- These registers are reserved; maintain these registers clear.

 Unimplemented data memory locations, read as '0'.

* Not a physical register.

File Address	File Address	File Address	File Address
Indirect addr. (*)	00h	Indirect addr. (*)	100h
	01h	OPTION_REG	101h
	02h	PCL	102h
	03h	STATUS	103h
	04h	FSR	104h
	05h	PORTA	105h
	06h	PORTB	106h
	07h	PORTC	107h
	08h	PORTD ⁽¹⁾	108h
	09h	PORTE ⁽¹⁾	109h
	0Ah	PCLATH	10Ah
	0Bh	INTCON	10Bh
	0Ch	PIR1	10Ch
	0Dh	PIR2	10Dh
	0Eh	TMR1L	10Eh
	0Fh	TMR1H	10Fh
	10h	T1CON	110h
	11h	TMR2	111h
	12h	T2CON	112h
	13h	SSPBUF	113h
	14h	SSPCON	114h
	15h	CCPR1L	115h
	16h	CCPR1H	116h
	17h	CCP1CON	117h
	18h	RCSTA	118h
	19h	TXREG	119h
	1Ah	RCREG	11Ah
	1Bh	CCPR2L	11Bh
	1Ch	CCPR2H	11Ch
	1Dh	CCP2CON	11Dh
	1Eh	ADRESH	11Eh
	1Fh	ADCON0	11Fh
	20h		120h
		General Purpose Register 16 Bytes	
		97h	
		TXSTA	
		98h	
		SPBRG	
		99h	
		9Ah	
		9Bh	
		9Ch	
		9Dh	
		9Eh	
		9Fh	
		A0h	
		General Purpose Register 80 Bytes	
		96 Bytes	
		EFh	
		F0h	
		FFh	
	7Fh	General Purpose Register 80 Bytes	
		accesses 70h-7Fh	
		16Fh	
		170h	
		17Fh	
		accesses 70h - 7Fh	
		17Fh	
		1FFh	
		Bank 0	
		Bank 1	
		Bank 2	
		Bank 3	



BANK 0

Note :

- 1- The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.
- 2- Bits PSPIE and PSPIF are reserved on PIC16F873A/876A devices; always maintain these bits clear.
- 3- These registers can be addressed from any bank.
- 4- PORTD, PORTE, TRISD and TRISE are not implemented on PIC16F873A/876A devices, read as '0'.
- 5- Bit 4 of EEADRH implemented only on the PIC16F876A/877A devices.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:							
Bank 0																		
00h ⁽³⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)									0000 0000 31, 150							
01h	TMR0	Timer0 Module Register									xxxx xxxx 55, 150							
02h ⁽³⁾	PCL	Program Counter (PC) Least Significant Byte									0000 0000 30, 150							
03h ⁽³⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxx 22, 150								
04h ⁽³⁾	FSR	Indirect Data Memory Address Pointer									xxxx xxxx 31, 150							
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read							--0x 0000 43, 150							
06h	PORTB	PORTB Data Latch when written: PORTB pins when read									xxxx xxxx 45, 150							
07h	PORTC	PORTC Data Latch when written: PORTC pins when read									xxxx xxxx 47, 150							
08h ⁽⁴⁾	PORTD	PORTD Data Latch when written: PORTD pins when read									xxxx xxxx 48, 150							
09h ⁽⁴⁾	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	49, 150							
0Ah ^(1,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter													
0Bh ⁽³⁾	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x 24, 150								
0Ch	PIR1	PSPIF ⁽³⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000 26, 150								
0Dh	PIR2	—	CMIF	—	EEIF	BCLIF	—	—	CCP2IF	-0-0 0--0 28, 150								
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register									xxxx xxxx 60, 150							
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register									xxxx xxxx 60, 150							
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000 57, 150								
11h	TMR2	Timer2 Module Register									0000 0000 62, 150							
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000 61, 150								
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register									xxxx xxxx 79, 150							
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000 82, 82, 150								
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)									xxxx xxxx 63, 150							
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)									xxxx xxxx 63, 150							
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000 64, 150								
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x 112, 150								
19h	TXREG	USART Transmit Data Register									0000 0000 118, 150							
1Ah	RCREG	USART Receive Data Register									0000 0000 118, 150							
1Bh	CCPR2L	Capture/Compare/PWM Register 2 (LSB)									xxxx xxxx 63, 150							
1Ch	CCPR2H	Capture/Compare/PWM Register 2 (MSB)									xxxx xxxx 63, 150							
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000 64, 150								
1Eh	ADRESH	A/D Result Register High Byte									xxxx xxxx 133, 150							
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	127, 150							

Figure 4 : TABLE (BANK0) - SPECIAL FUNCTION REGISTER SUMMARY



BANK 1

Note :

- 1- The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.
- 2- Bits PSPIE and PSPIF are reserved on PIC16F873A/876A devices; always maintain these bits clear.
- 3- These registers can be addressed from any bank.
- 4- PORTD, PORTE, TRISD and TRISE are not implemented on PIC16F873A/876A devices, read as '0'.
- 5- Bit 4 of EEADRH implemented only on the PIC16F876A/877A devices.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:	
Bank 1												
80h ⁽³⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	31, 150	
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	23, 150	
82h ⁽³⁾	PCL	Program Counter (PC) Least Significant Byte								0000 0000	30, 150	
83h ⁽³⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxx	22, 150	
84h ⁽³⁾	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	31, 150	
85h	TRISA	—	—	PORTA Data Direction Register								
86h	TRISB	PORTB Data Direction Register								1111 1111	45, 150	
87h	TRISC	PORTC Data Direction Register								1111 1111	47, 150	
88h ⁽⁴⁾	TRISD	PORTD Data Direction Register								1111 1111	48, 151	
89h ⁽⁴⁾	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction bits					
8Ah ^(1,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter							
8Bh ⁽³⁾	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 150	
8Ch	PIE1	PSPIE ⁽²⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	25, 151	
8Dh	PIE2	—	CMIE	—	EEIE	BCLIE	—	—	CCP2IE	-0-0 0--0	27, 151	
8Eh	PCON	—	—	—	—	—	—	—	POR	BOR	---- --qq	29, 151
8Fh	—	Unimplemented								—	—	
90h	—	Unimplemented								—	—	
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	83, 151	
92h	PR2	Timer2 Period Register								1111 1111	62, 151	
93h	SSPADD	Synchronous Serial Port (I ² C mode) Address Register								0000 0000	79, 151	
94h	SSPSTAT	SMP	CKE	D [—] A	P	S	R/W	UA	BF	0000 0000	79, 151	
95h	—	Unimplemented								—	—	
96h	—	Unimplemented								—	—	
97h	—	Unimplemented								—	—	
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	111, 151	
99h	SPBRG	Baud Rate Generator Register								0000 0000	113, 151	
9Ah	—	Unimplemented								—	—	
9Bh	—	Unimplemented								—	—	
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	135, 151	
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	141, 151	
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx	133, 151	
9Fh	ADCON1	ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0	00-- 0000	128, 151	

Figure 5 : TABLE (BANK1) - SPECIAL FUNCTION REGISTER SUMMARY



BANK 2 – BANK 3

Note :

- 1-** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.
- 2-** Bits PSPIE and PSPIF are reserved on PIC16F873A/876A devices; always maintain these bits clear.
- 3-** These registers can be addressed from any bank.
- 4-** PORTD, PORTE, TRISD and TRISE are not implemented on PIC16F873A/876A devices, read as ‘0’.
- 5-** Bit 4 of EEADRH implemented only on the PIC16F876A/877A devices.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:	
Bank 2												
100h ⁽³⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	31, 150	
101h	TMR0	Timer0 Module Register								xxxx xxxx	55, 150	
102h ⁽³⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	30, 150	
103h ⁽³⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxx	22, 150	
104h ⁽³⁾	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	31, 150	
105h	—	Unimplemented								—	—	
106h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	45, 150	
107h	—	Unimplemented								—	—	
108h	—	Unimplemented								—	—	
109h	—	Unimplemented								—	—	
10Ah ^(1,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	30, 150	
10Bh ⁽³⁾	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 150	
10Ch	EEDATA	EEPROM Data Register Low Byte								xxxx xxxx	39, 151	
10Dh	EEADR	EEPROM Address Register Low Byte								xxxx xxxx	39, 151	
10Eh	EEDATH	—	—	EEPROM Data Register High Byte						--xx xxxx	39, 151	
10Fh	EEADRH	—	—	—	— ⁽⁵⁾	EEPROM Address Register High Byte					---- xxxx	39, 151
Bank 3												
180h ⁽³⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	31, 150	
181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	23, 150	
182h ⁽³⁾	PCL	Program Counter (PC) Least Significant Byte								0000 0000	30, 150	
183h ⁽³⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxx	22, 150	
184h ⁽³⁾	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	31, 150	
185h	—	Unimplemented								—	—	
186h	TRISB	PORTB Data Direction Register								1111 1111	45, 150	
187h	—	Unimplemented								—	—	
188h	—	Unimplemented								—	—	
189h	—	Unimplemented								—	—	
18Ah ^(1,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	30, 150	
18Bh ⁽³⁾	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 150	
18Ch	EECON1	EEPGD	—	—	—	WRERR	WREN	WR	RD	x--- x000	34, 151	
18Dh	EECON2	EEPROM Control Register 2 (not a physical register)								-----	39, 151	
18Eh	—	Reserved; maintain clear								0000 0000	—	
18Fh	—	Reserved; maintain clear								0000 0000	—	

Figure 6 : TABLE (BANK2-3) - SPECIAL FUNCTION REGISTER SUMMARY



INSTRUCTIONS

Note :

1- When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0' .

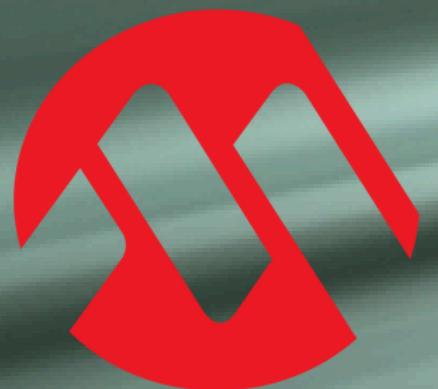
2- If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module .

3- If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

Additional information on the mid-range instruction set is available in the PICmicro® Mid-Range MCU Family Reference Manual (DS33023).

Mnemonic, Operands	Description	Cycles	14-Bit Opcode		Status Affected	Notes
			MSb	LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF f, d	Add W and f	1	00	0111 dfff ffff	C,DC,Z	1,2
ANDWF f, d	AND W with f	1	00	0101 dfff ffff	Z	1,2
CLRF f	Clear f	1	00	0001 1fff ffff	Z	2
CLRW -	Clear W	1	00	0001 0xxx xxxx	Z	
COMF f, d	Complement f	1	00	1001 dfff ffff	Z	1,2
DECFSZ f, d	Decrement f, Skip if 0	1(2)	00	0011 dfff ffff	Z	1,2
INCF f, d	Increment f	1	00	1010 dfff ffff	Z	1,2
INCFSZ f, d	Increment f, Skip if 0	1(2)	00	1111 dfff ffff	Z	1,2,3
IORWF f, d	Inclusive OR W with f	1	00	0100 dfff ffff	Z	1,2
MOVF f, d	Move f	1	00	1000 dfff ffff	Z	1,2
MOVWF f	Move W to f	1	00	0000 1fff ffff		
NOP -	No Operation	1	00	0000 0xx0 0000		
RLF f, d	Rotate Left f through Carry	1	00	1101 dfff ffff	C	1,2
RRF f, d	Rotate Right f through Carry	1	00	1100 dfff ffff	C	1,2
SUBWF f, d	Subtract W from f	1	00	0010 dfff ffff	C,DC,Z	1,2
SWAPP f, d	Swap nibbles in f	1	00	1110 dfff ffff	Z	1,2
XORWF f, d	Exclusive OR W with f	1	00	0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF f, b	Bit Clear f	1	01	00bb bfff ffff		1,2
BSF f, b	Bit Set f	1	01	01bb bfff ffff		1,2
BTFSZ f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb bfff ffff		3
BTFSZ f, b	Bit Test f, Skip if Set	1 (2)	01	11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW k	Add Literal and W	1	11	111x kkkk kkkk	C,DC,Z	
ANDLW k	AND Literal with W	1	11	1001 kkkk kkkk	Z	
CALL k	Call Subroutine	2	10	0kkk kkkk kkkk		
CLRWDT -	Clear Watchdog Timer	1	00	0000 0110 0100	TO,PD	
GOTO k	Go to Address	2	10	1kkk kkkk kkkk		
IORLW k	Inclusive OR Literal with W	1	11	1000 kkkk kkkk	Z	
MOVLW k	Move Literal to W	1	11	00xx kkkk kkkk		
RETFIE -	Return from Interrupt	2	00	0000 0000 1001		
RETLW k	Return with Literal in W	2	11	01xx kkkk kkkk		
RETURN -	Return from Subroutine	2	00	0000 0000 1000		
SLEEP -	Go into Standby mode	1	00	0000 0110 0011	TO,PD	
SUBLW k	Subtract W from Literal	1	11	110x kkkk kkkk	C,DC,Z	
XORLW k	Exclusive OR Literal with W	1	11	1010 kkkk kkkk	Z	

Figure 7 : TABLE - PIC16F87XA INSTRUCTION SET



MICROCHIP

PIC16F877A CONFIGURATION



OSCILLATOR CONFIGURATION

Note :

- 1- See the table for recommended values of C1 and C2.
- 2- A series resistor (Rs) may be required for AT strip cut crystals.
- 3- RF varies with the crystal chosen.

The PIC16F877A can be operated in four different oscillator modes.
The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes :

- LP Low-Power Crystal
- XT Crystal/Resonator
- HS High-Speed Crystal/Resonator
- RC Resistor/Capacitor

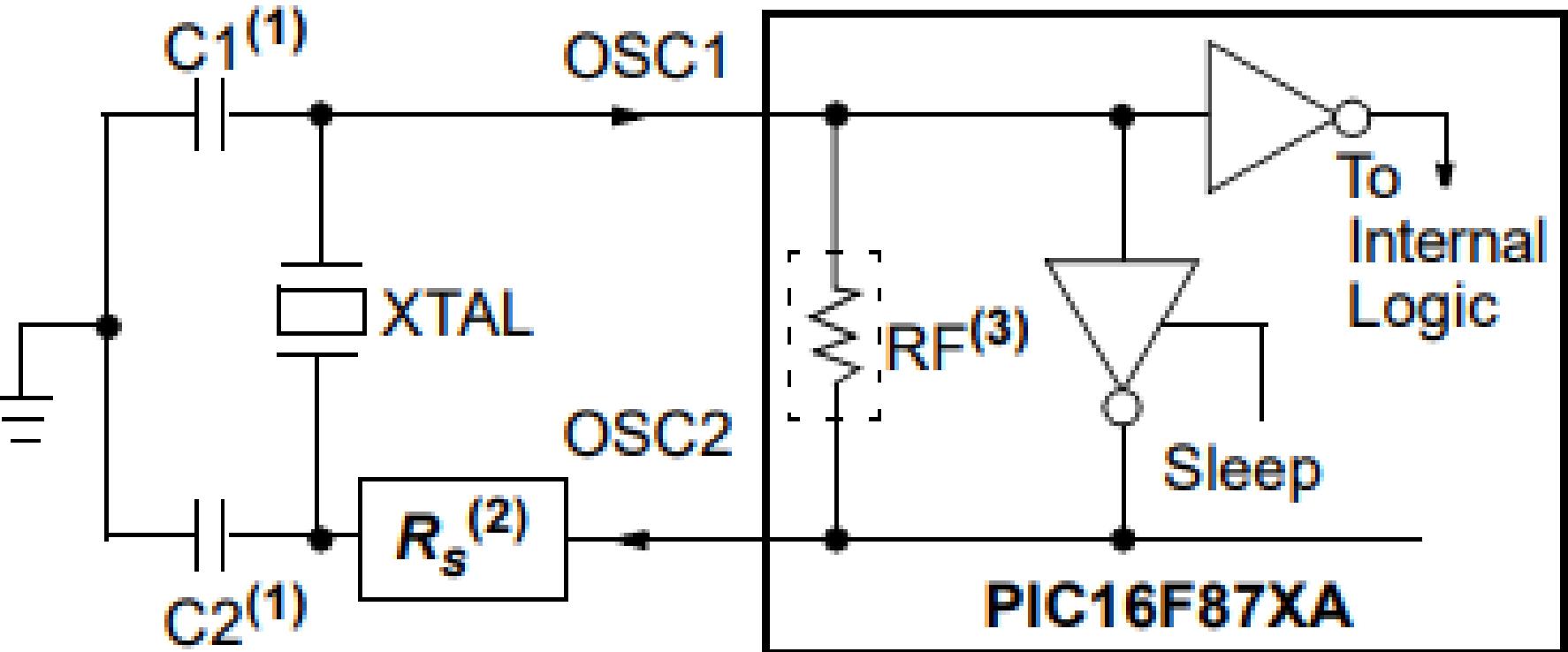


Figure 8 : CRYSTAL/CERAMIC RESONATOR OPERATION
(HS, XT OR LP OSC CONFIGURATION)

Osc Type	Crystal Freq.	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF

Figure 9 : CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

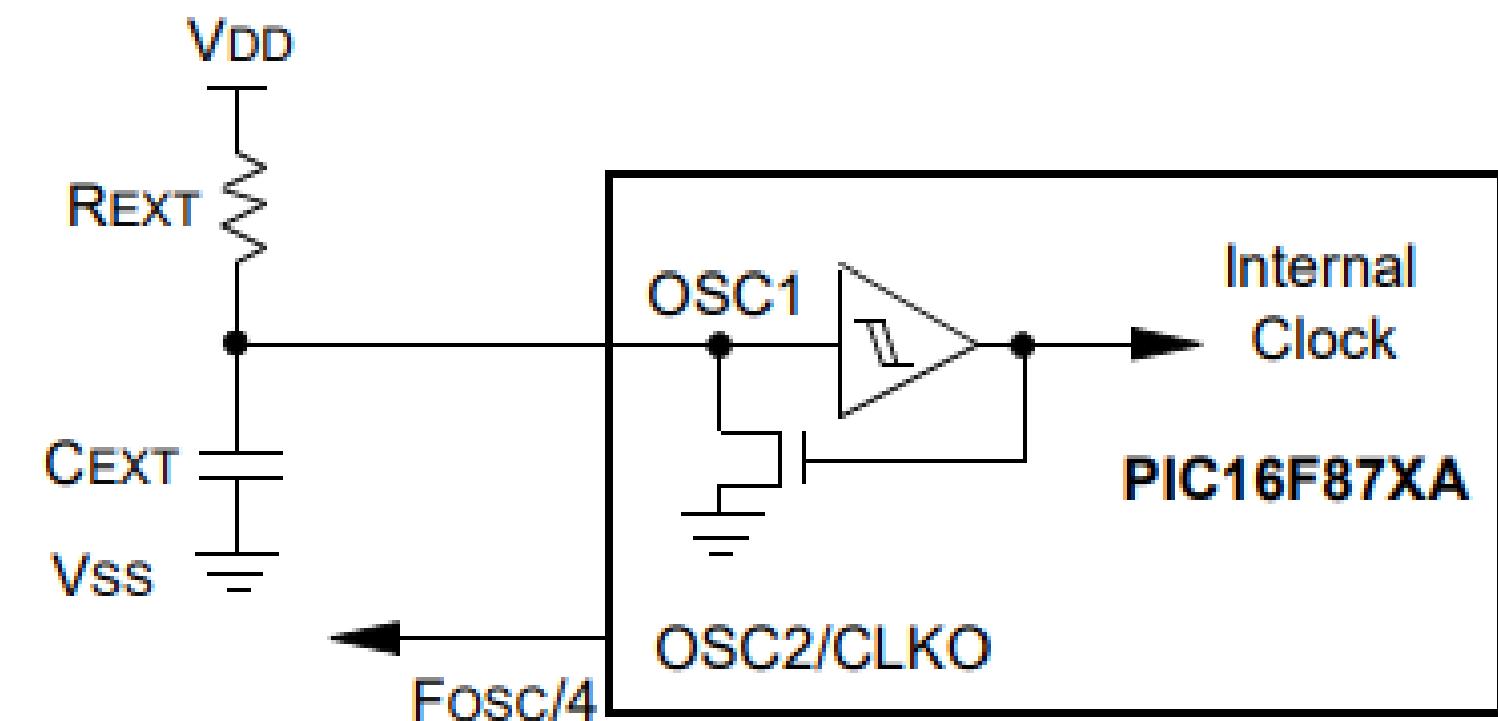


RC OSCILLATOR

Note :

- 1- Higher capacitance increases the stability of oscillator but also increases the start-up time.
- 2- Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
- 3- Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.
- 4- When migrating from other PICmicro® devices, oscillator performance should be verified.

For applications where precise timing isn't crucial, the RC device option offers a cost-effective solution. The RC oscillator's frequency depends on the supply voltage, the values of the external resistor (REXT) and capacitor (CEXT), and the operating temperature. Frequency variations can occur due to manufacturing differences, package types, and the tolerances of the external components. These factors make the RC oscillator ideal for less timing-sensitive applications, where small frequency changes are acceptable.



Recommended values:
 $3 \text{ k}\Omega \leq R_{EXT} \leq 100 \text{ k}\Omega$
 $C_{EXT} > 20 \text{ pF}$

Figure 10 : RC OSCILLATOR MODE

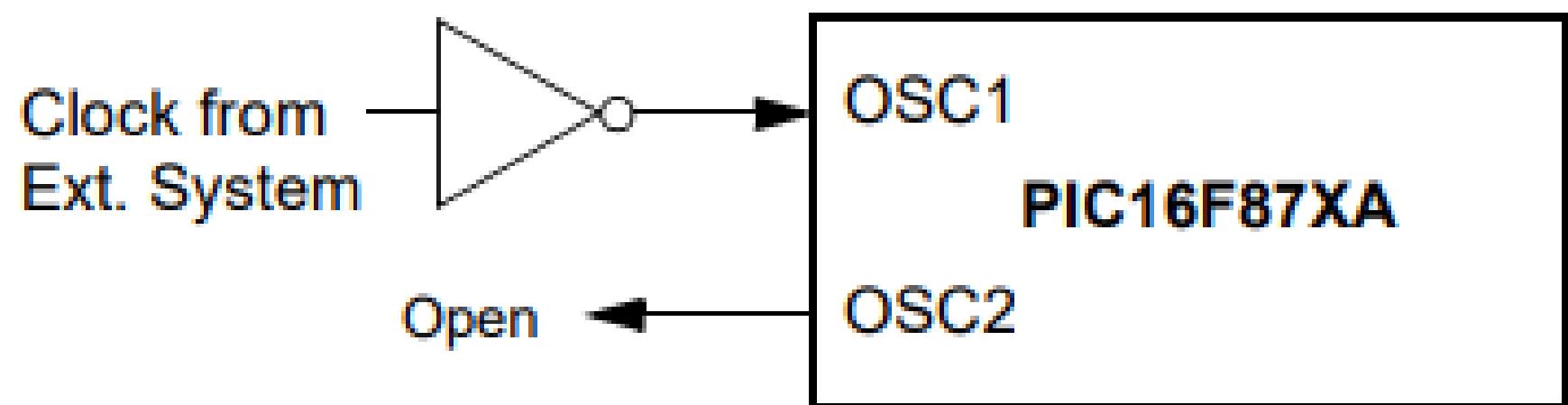


Figure 11 : EXTERNAL CLOCK INPUT OPERATION
(HS, XT OR LP OSC CONFIGURATION)



MCLR CONFIGURATION

Note :

1- $R1 < 40\text{ k}\Omega$ is recommended to make sure that the voltage drop across R does not violate the device's electrical specification.

2- $R2 > 1\text{K}$ will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR/VPP breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

The PIC16F877A microcontroller includes a noise filter in the MCLR Reset path, which ignores small pulses. A WDT (Watchdog Timer) Reset does not pull the MCLR pin low. Unlike previous models, the MCLR pin on this device has different ESD protection behavior. If voltages exceed specifications, it can cause unexpected Resets and increased current consumption. Therefore, Microchip recommends not tying the MCLR pin directly to VDD, but instead using an RCR network.

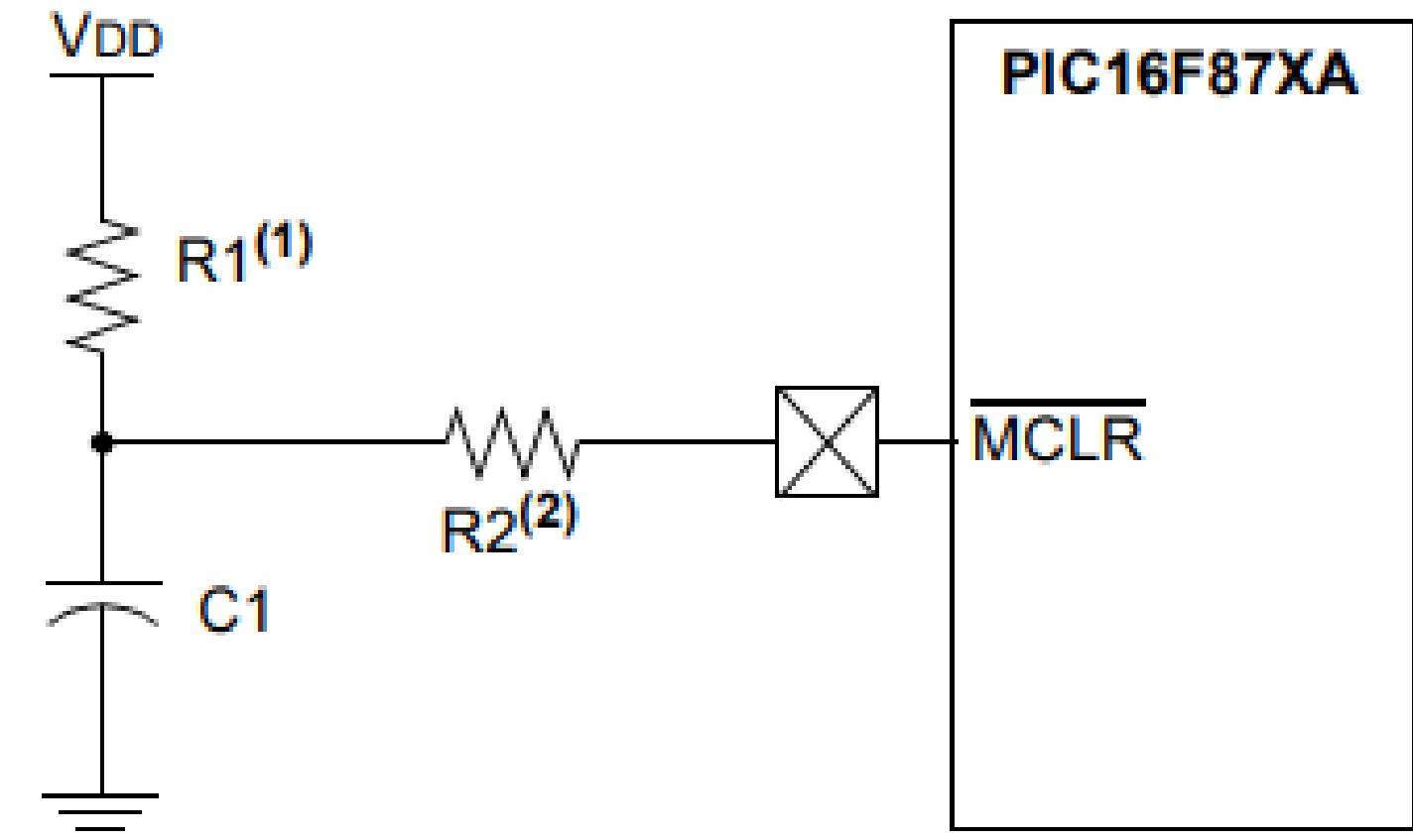


Figure 12 : RECOMMENDED MCLR CIRCUIT

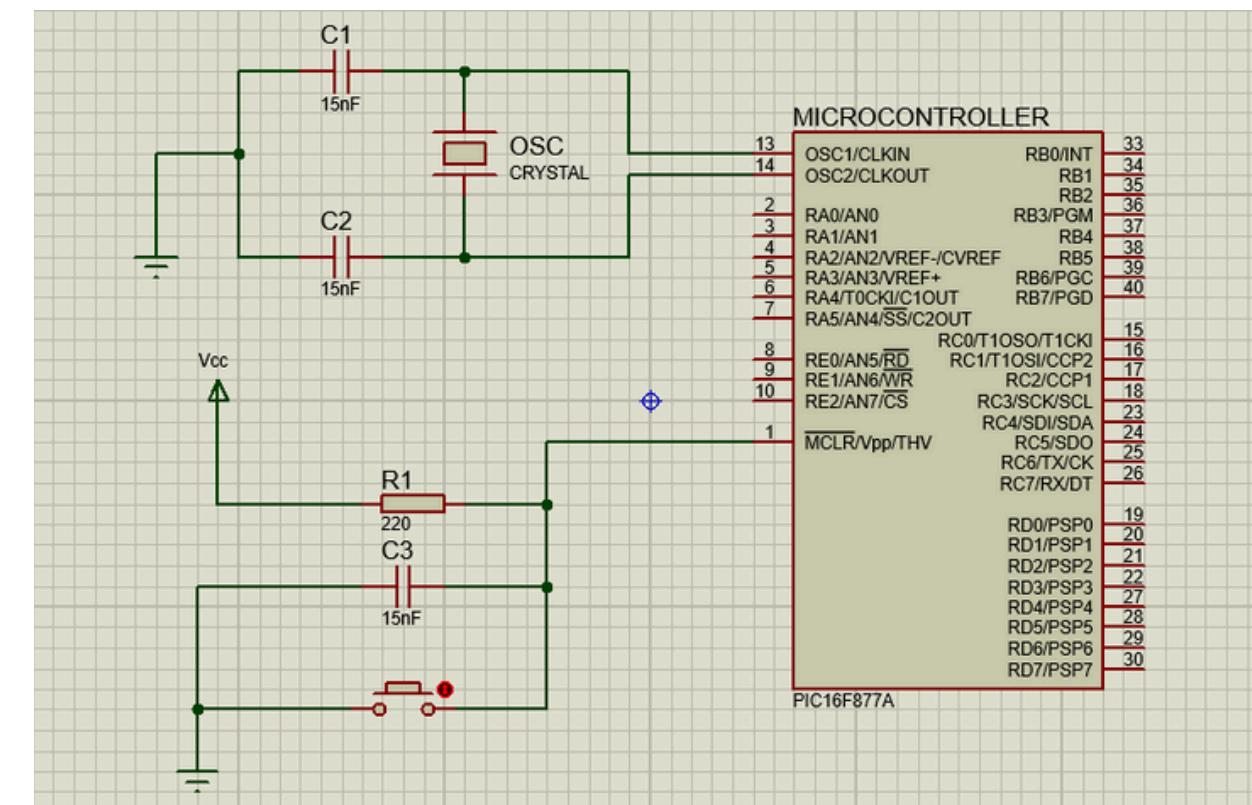


Figure 13 : EXAMPLE CONFIGURATION



PIC16F877A DATACHEET

- PIC16F877A Datasheet : Pinout diagram & RAM organization
 - Link : [RAM DATSHEET](#)
- PIC16F877A Datasheet : instruction Set
 - Link : [INSTRUCTIONS DATASHEET](#)
- ADC Datasheet for PIC16F877A
 - Link : [ADC DATASHEET](#)
- PWM Datasheet for PIC16F877A
 - Link : [PWM DATASHEET](#)
- USART Datasheet for PIC16F87XA
 - Link : [USART DATASHEET](#)