# MULTIPLIERS AND MAGNITUDE COMPARATORS

# Binary Multiplier

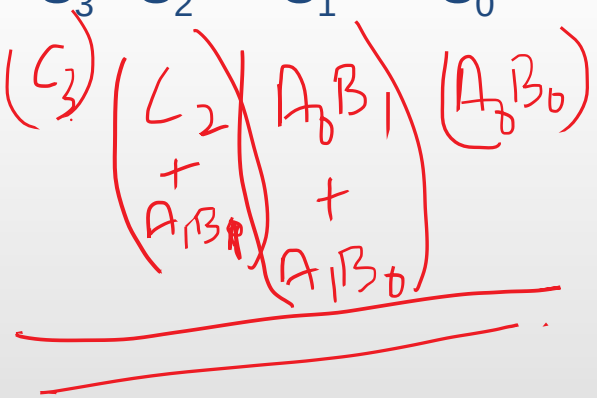
- 2 bit × 2 bit binary multiplier using adders and external gates.

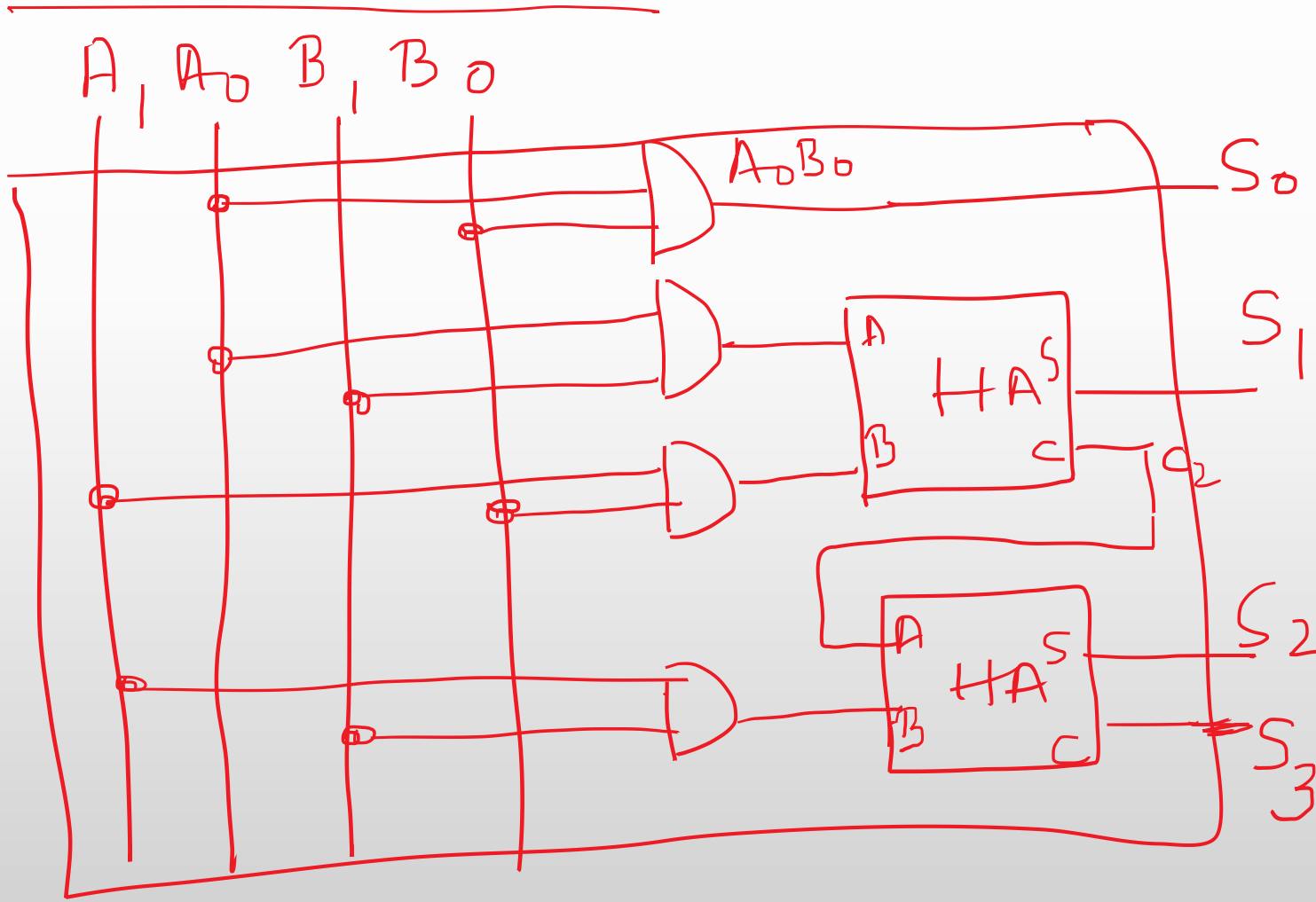
$B_1B_0 \times A_1A_0$

$C_3$ $C_2$ $A_0B_1$ $A_0B_0$

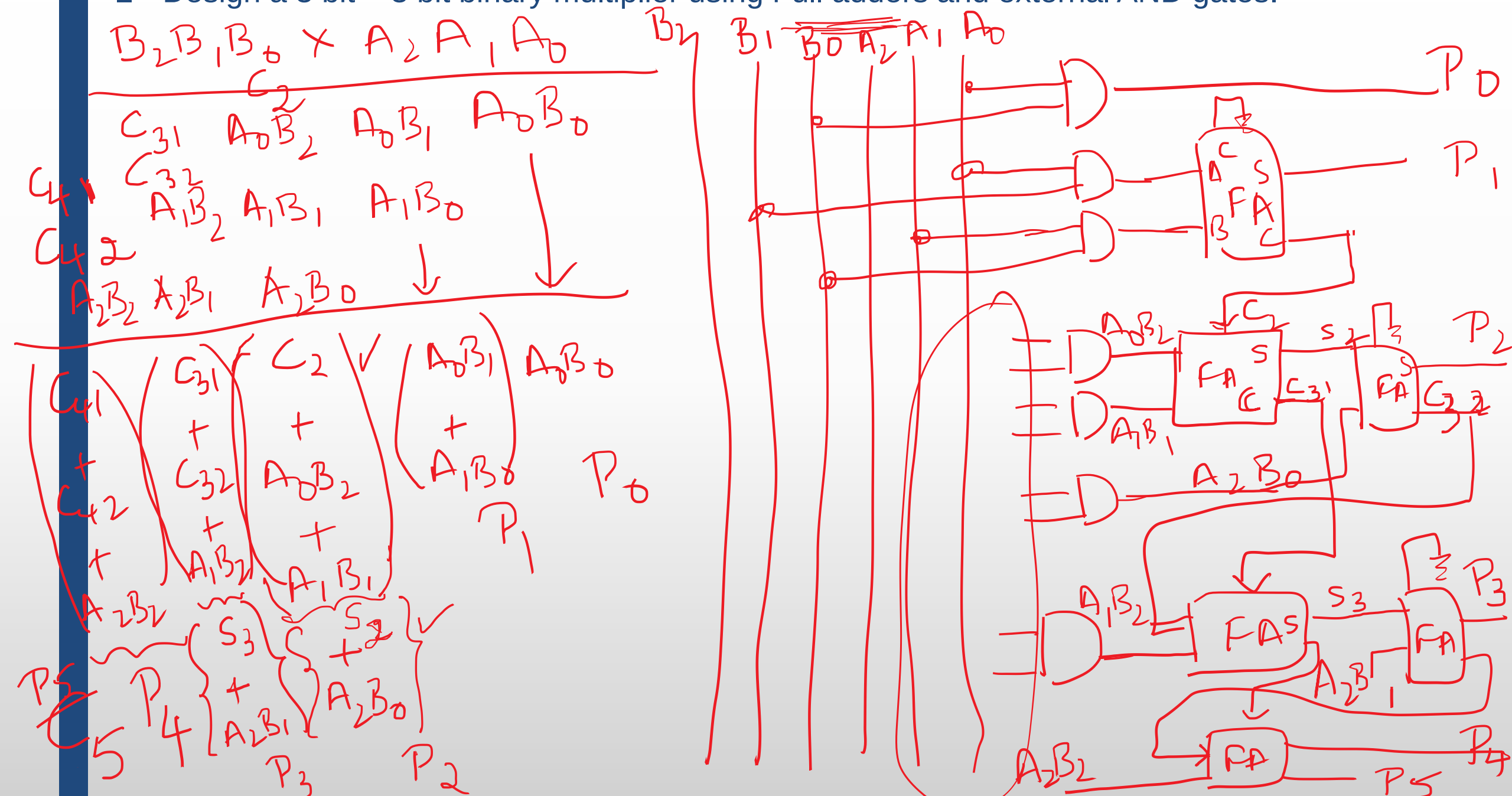
$A_1B_1$ $A_1B_0$

$S_3$ $S_2$ $S_1$ $S_0$

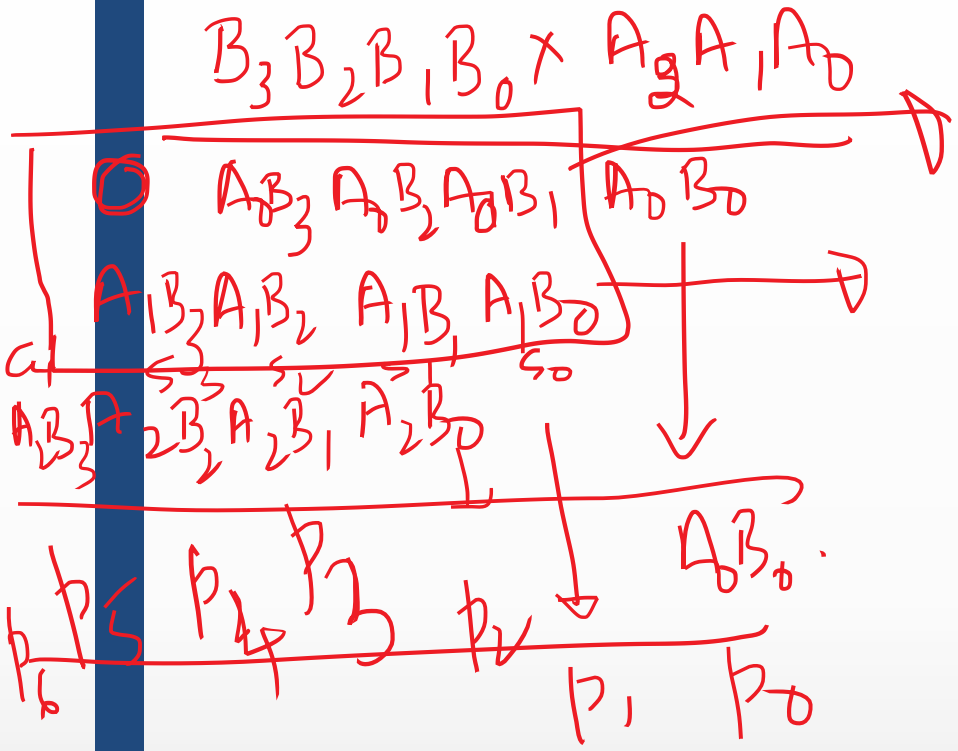


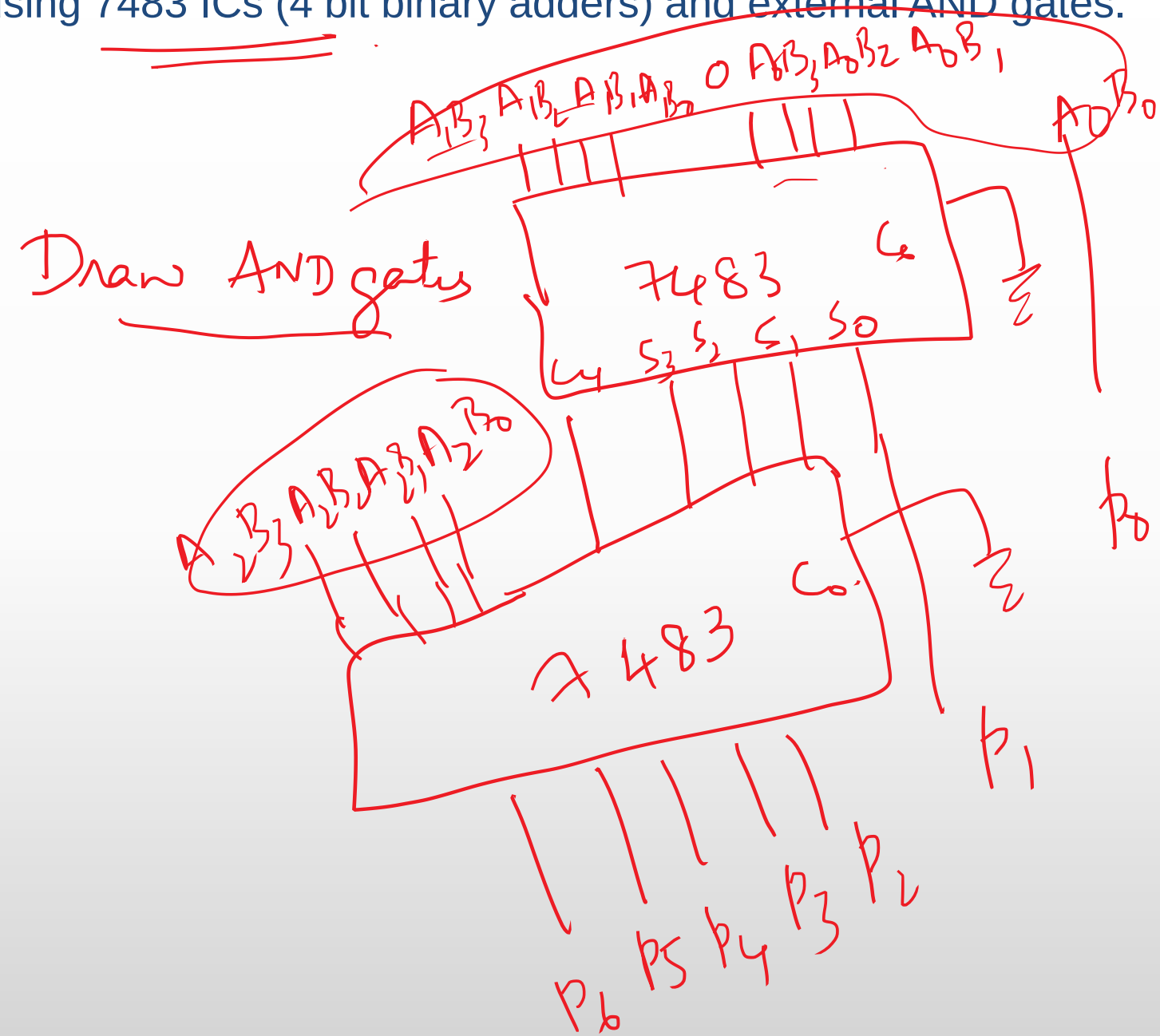



- Design a 3 bit × 3 bit binary multiplier using Full adders and external AND gates.



Design a 4 bit × 3 bit binary multiplier using 7483 ICs (4 bit binary adders) and external AND gates.

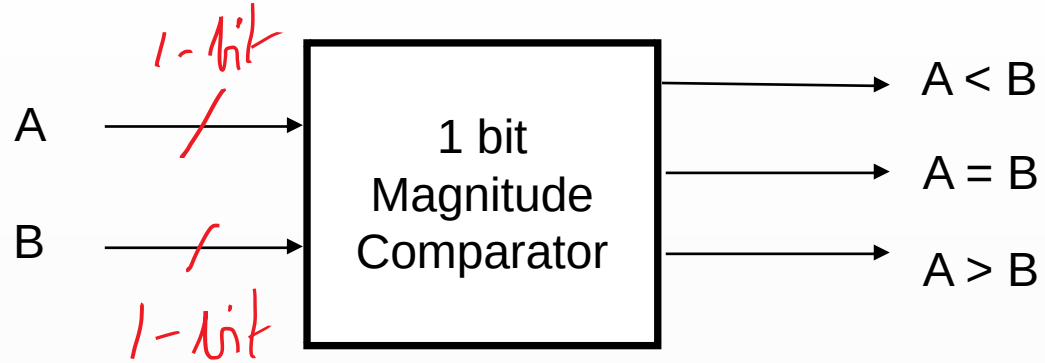


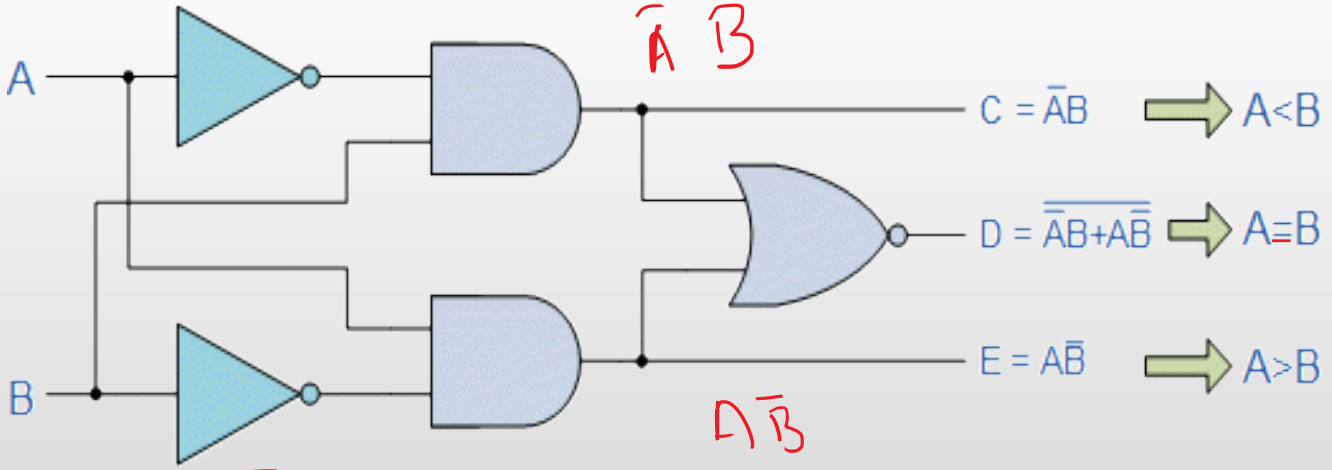



# Magnitude Comparator

- 1 bit Magnitude comparator

| Input | | Output | | |
|---|---|---|---|---|
| A | B | A>B | A=B | A<B |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |




$A > B, G = A\bar{B}$

$A = B, E = \bar{A}\bar{B} + AB$

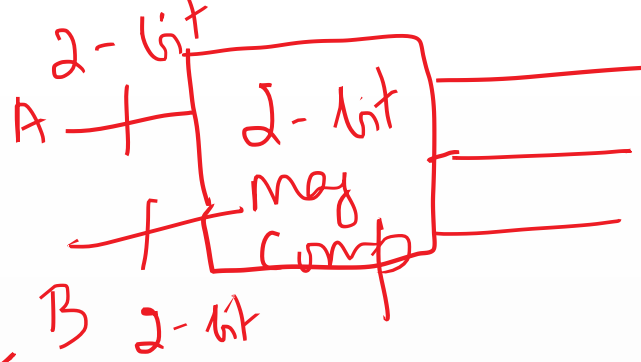
$= \overline{A \oplus B}$

$= A\bar{B} + \bar{A}B$

$A < B, L = \bar{A}B$

## 2 bit magnitude comparator

| Inputs | | | | Outputs | | |
|---|---|---|---|---|---|---|
| $A_1$ | $A_0$ | $B_1$ | $B_0$ | A>B | A=B | A<B |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |




$G_1 \Rightarrow A_1 > B_1$

$G_0 \Rightarrow A_0 > B_0$

$E_1 = A_1 = B_1$

$E_0 = A_0 = B_0$

$A > B, G = \bar{A}_1 A_0 \bar{B}_1 \bar{B}_0 + A_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + A_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + A_1 A_0 \bar{B}_1 \bar{B}_0 + A_1 A_0 \bar{B}_1 \bar{B}_0$

$= A_1 \bar{B}_1 [\bar{A}_0 \bar{B}_0 + \bar{A}_0 B_0 + A_0 \bar{B}_0 + A_0 B_0] + A_0 \bar{B}_0 [\bar{A}_1 \bar{B}_1 + A_1 B_1]$

$= A_1 \bar{B}_1 + A_0 \bar{B}_0 [A_1 \oplus B_1]$

$G = G_1 + G_0 E_1$

$G_1 = A_1 \bar{B}_1$

$G_0 = A_0 \bar{B}_0$

$E_1 = \overline{A_1 \bar{B}_1 + \bar{A}_1 B_1} = \overline{G_1 + L_1}$

$E_0 = \overline{G_0 + L_0}$

$L_1 = \bar{A}_1 B_1$

$L_0 = \bar{A}_0 B_0$ ✓

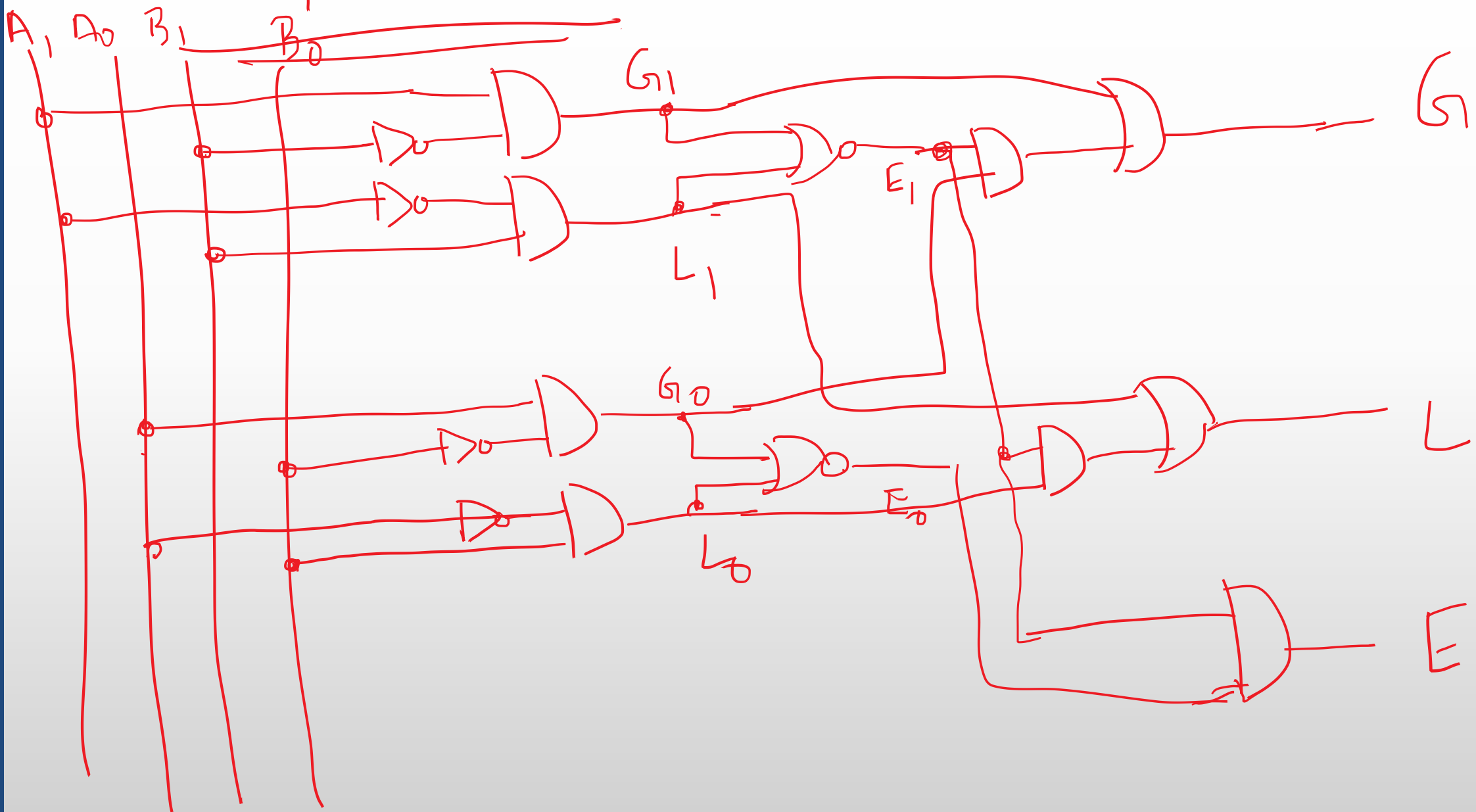
$$E = \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 A_0 \bar{B}_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0 + A_1 A_0 B_1 B_0$$

$$= \bar{A}_1 \bar{B}_1 \left[ \bar{A}_0 \bar{B}_0 + A_0 B_0 \right] + A_1 B_1 \left[ \bar{A}_0 \bar{B}_0 + A_0 B_0 \right]$$

$$= \left[ \bar{A}_1 \bar{B}_1 + A_1 B_1 \right] \left[ \bar{A}_0 \bar{B}_0 + A_0 B_0 \right]$$

$$= E_1 E_0$$

$$L = L_1 + \bar{E}_1 L_0$$



- 3 bit magnitude comparator

$A_2A_1A_0 \leftrightarrow B_2B_1B_0$

$$G = G_2 + E_2G_1 + E_2E_1G_0$$

$$E = E_2E_1E_0$$

$$L = L_2 + E_2L_1 + E_2E_1L_0$$

Draw the circuit

- 4 bit magnitude comparator

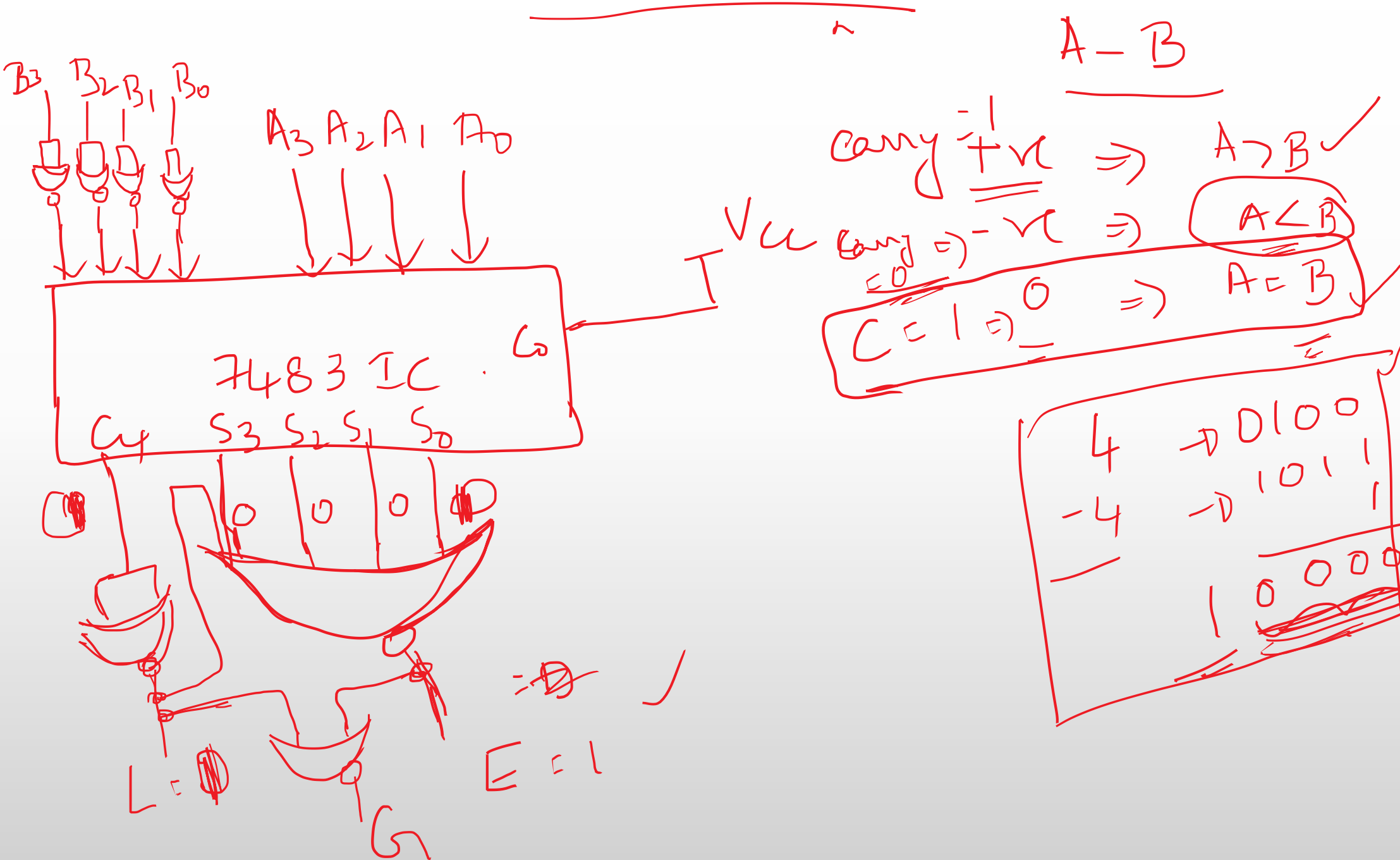
$$G = G_3 + E_3 G_2 + E_3 E_2 G_1 + E_3 E_2 E_1 G_0$$

$$E = \overline{E_3 E_2 E_1 E_0}$$

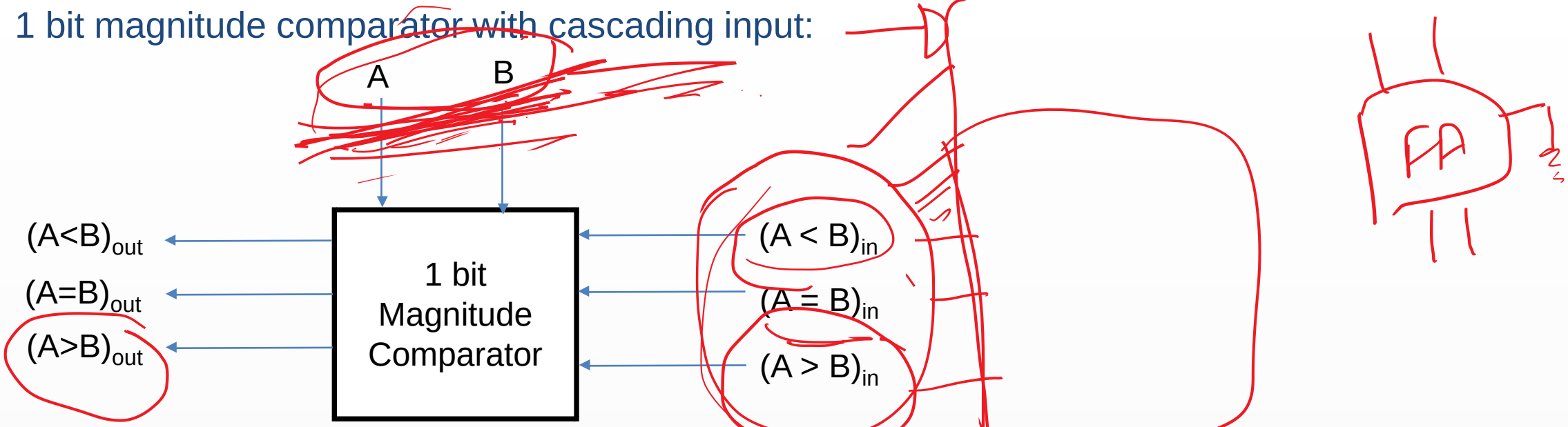
$$L = L_3 + E_3 L_2 + E_3 E_2 L_1 + E_3 E_2 E_1 L_0$$

Draw the circuit

Design 4 bit magnitude comparator using 7483 IC and external gates.



- 1 bit magnitude comparator with cascading input:




$(A>B)_{out} = (A>B) + (A=B)(A>B)_{in}$

$(A<B)_{out} = (A<B) + (A=B)\,(A<B)_{in}$

$(A=B)_{out} = (A=B)(A=B)_{in}$

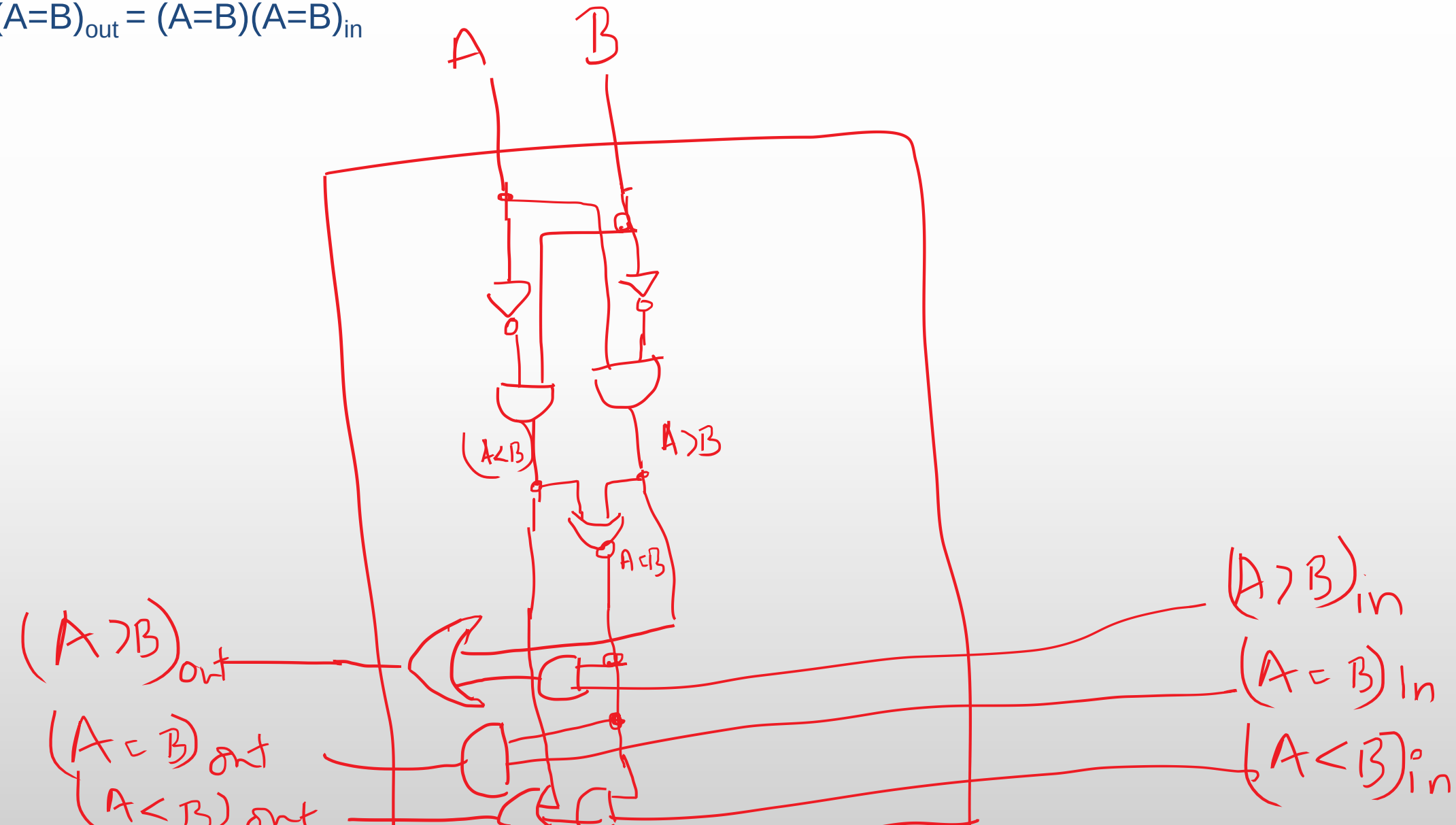
$G = G_1 + E_1 G_0$

$L = L_1 + E_1 L_0$

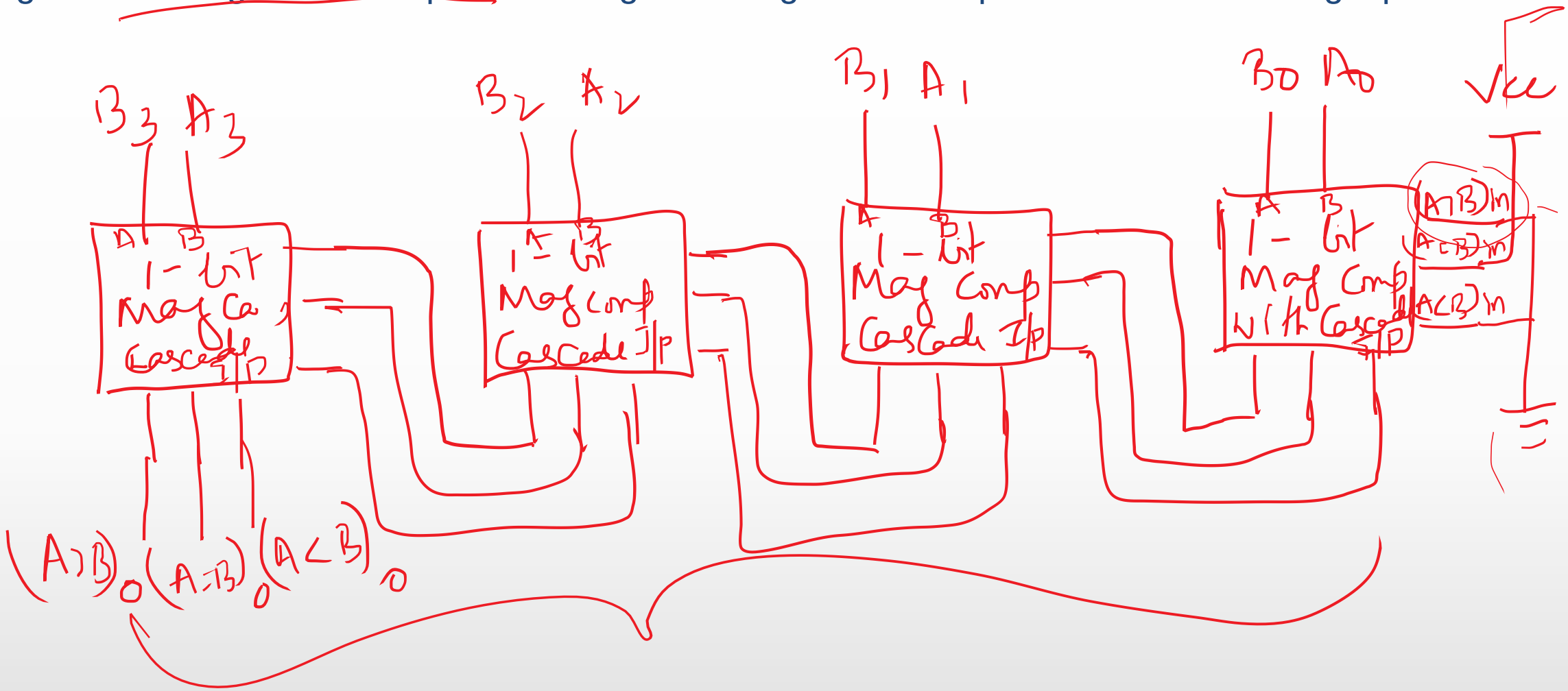
$(A>B)_{out} = (A>B) + (A=B)(A>B)_{in}$

$(A<B)_{out} = (A<B) + (A=B)(A<B)_{in}$

$(A=B)_{out} = (A=B)(A=B)_{in}$



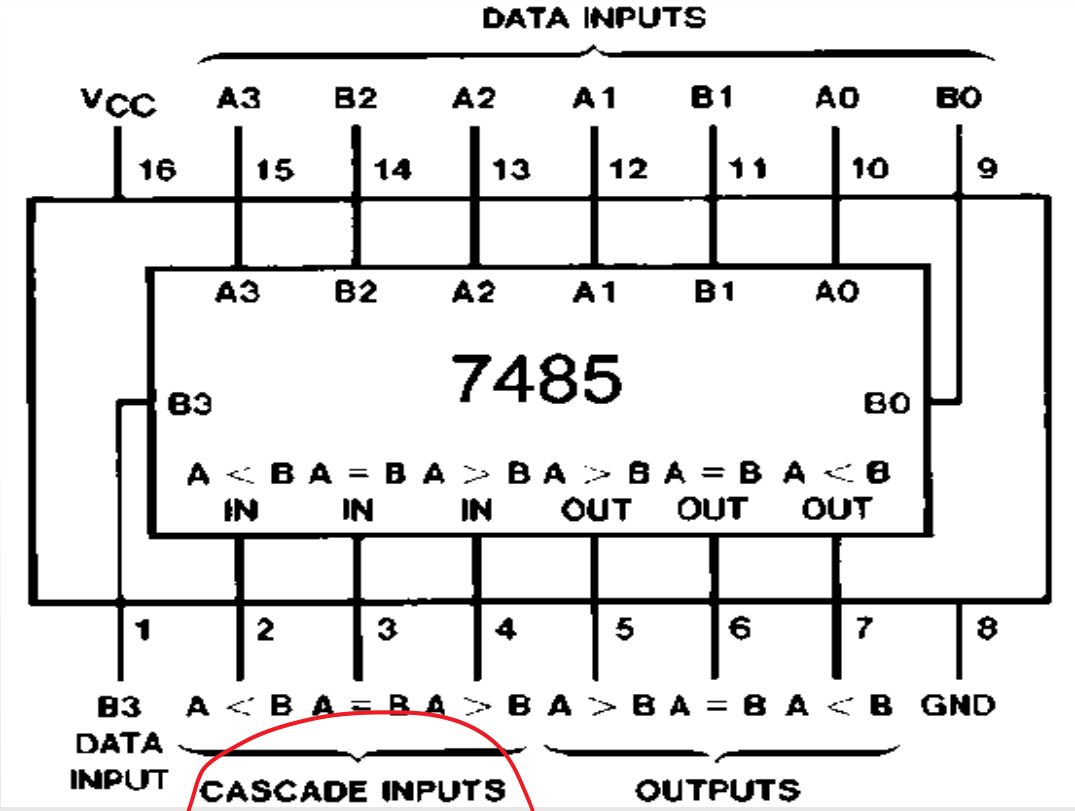
Design a 4 bit magnitude comparator using 1 bit magnitude comparator with cascading inputs.



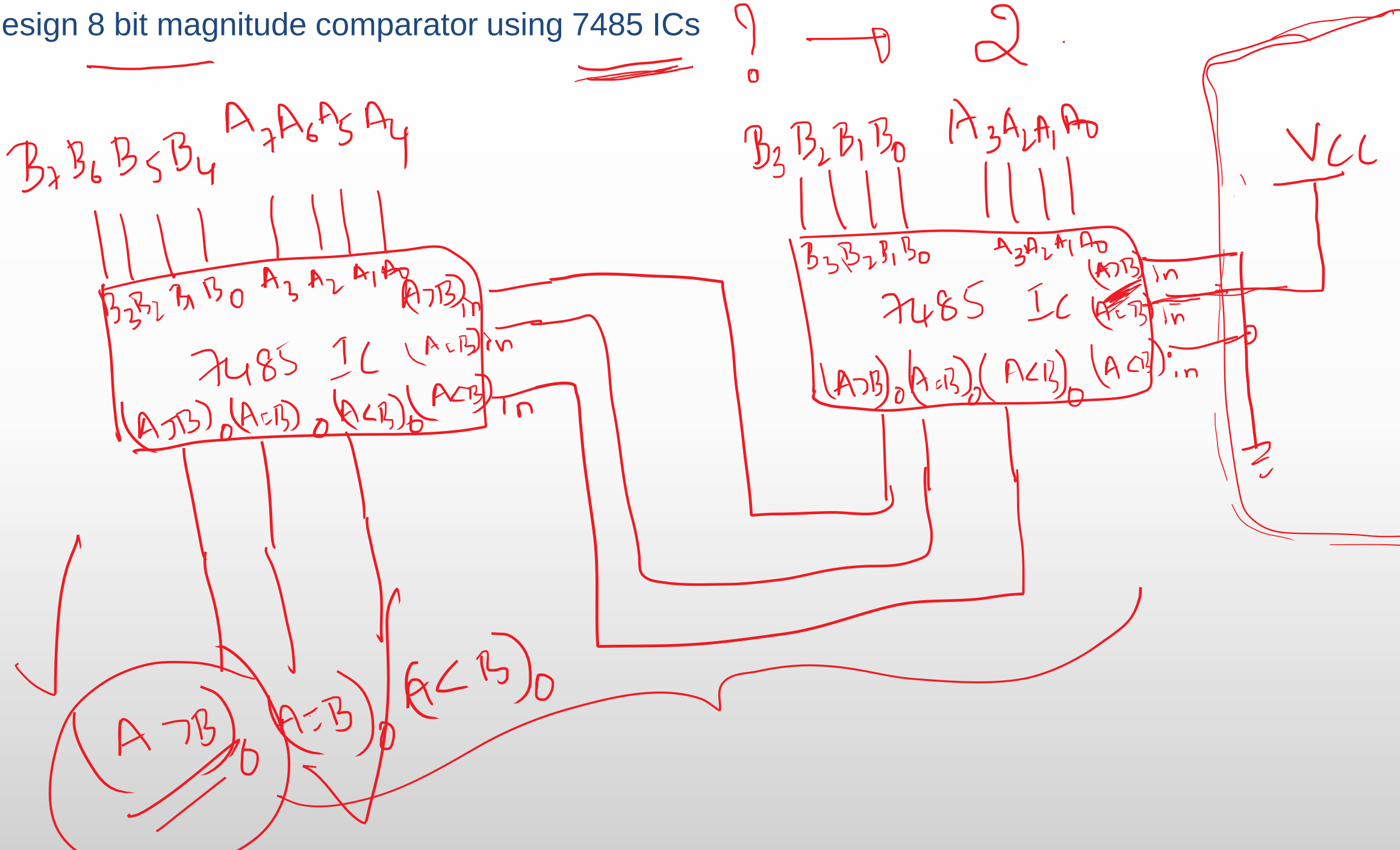

$A_3 A_2 A_1 A_0$

$B_3 B_2 B_1 B_0$

# 7485 IC ( 4 bit magnitude comparator with cascading inputs)



# Design 8 bit magnitude comparator using 7485 ICs



Design a combinational circuit using multipliers, 7483 IC and external gate to perform

F = 2X + Y when m=0,

F= X + 2Y when m=1

Where X, Y are two bit numbers and output F is a 4 bit number.