



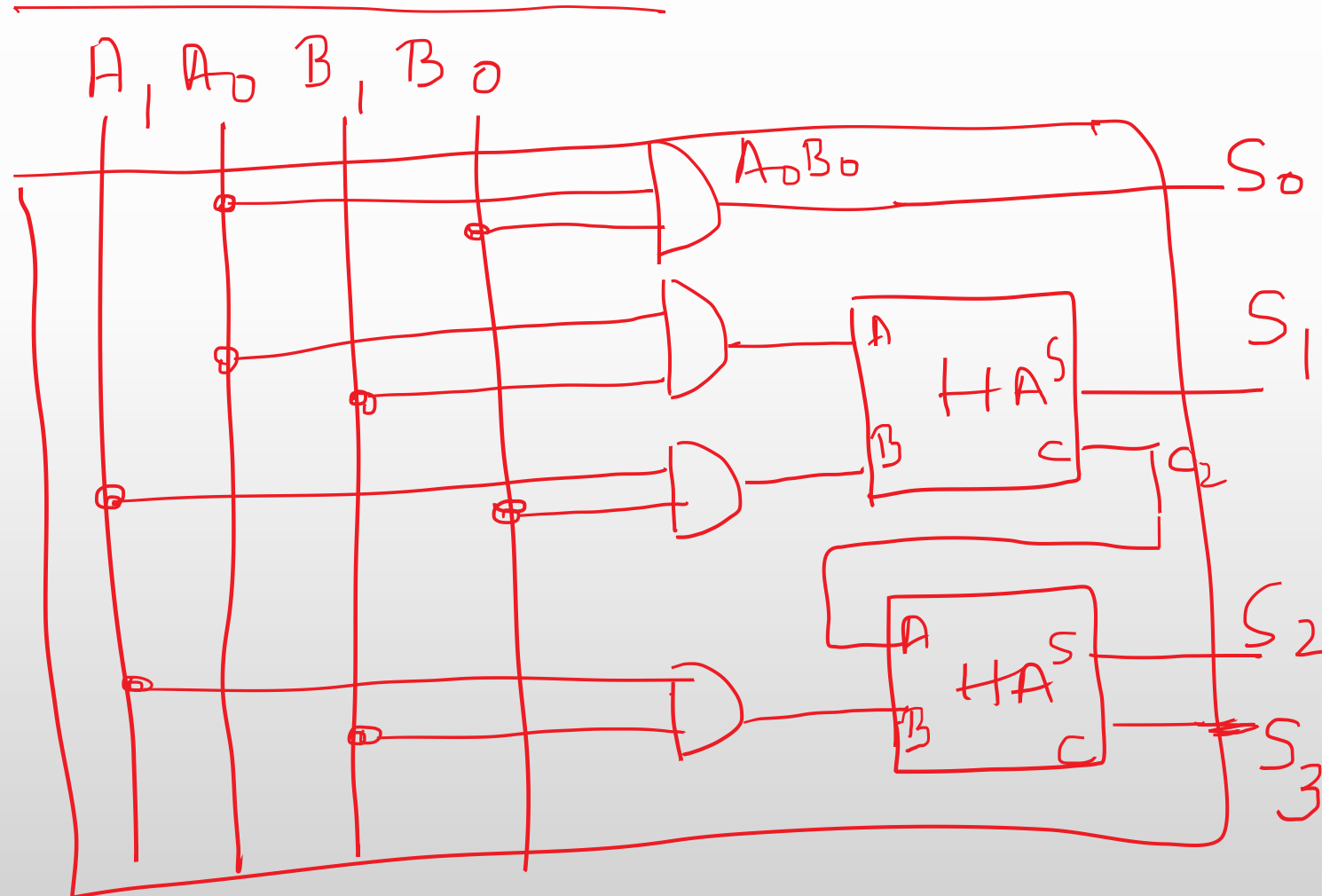
# MULTIPLIERS AND MAGNITUDE COMPARATORS

# Binary Multiplier

- 2 bit × 2 bit binary multiplier using adders and external gates.

$$\begin{array}{r}
 \text{B}_1\text{B}_0 \times \text{A}_1\text{A}_0 \\
 \hline
 \begin{array}{r}
 \text{C}_2 \quad \text{A}_0\text{B}_1 \quad \text{A}_0\text{B}_0 \\
 \text{A}_1\text{B}_1 \quad \text{A}_1\text{B}_0 \\
 \hline
 \text{S}_3 \quad \text{S}_2 \quad \text{S}_1 \quad \text{S}_0
 \end{array}
 \end{array}$$

(Handwritten notes in red:  $\text{C}_3$  above  $\text{S}_3$ ;  $\text{C}_2$  above  $\text{A}_0\text{B}_1$ ;  $\text{A}_0\text{B}_0$  and  $\text{A}_1\text{B}_0$  are grouped and added to produce  $\text{S}_0$ ;  $\text{A}_0\text{B}_1$  and  $\text{A}_1\text{B}_0$  are grouped and added to produce  $\text{S}_1$ ;  $\text{A}_1\text{B}_1$  is added to the carry from  $\text{S}_1$  to produce  $\text{S}_2$ ;  $\text{C}_2$  is added to the carry from  $\text{S}_2$  to produce  $\text{S}_3$ .)



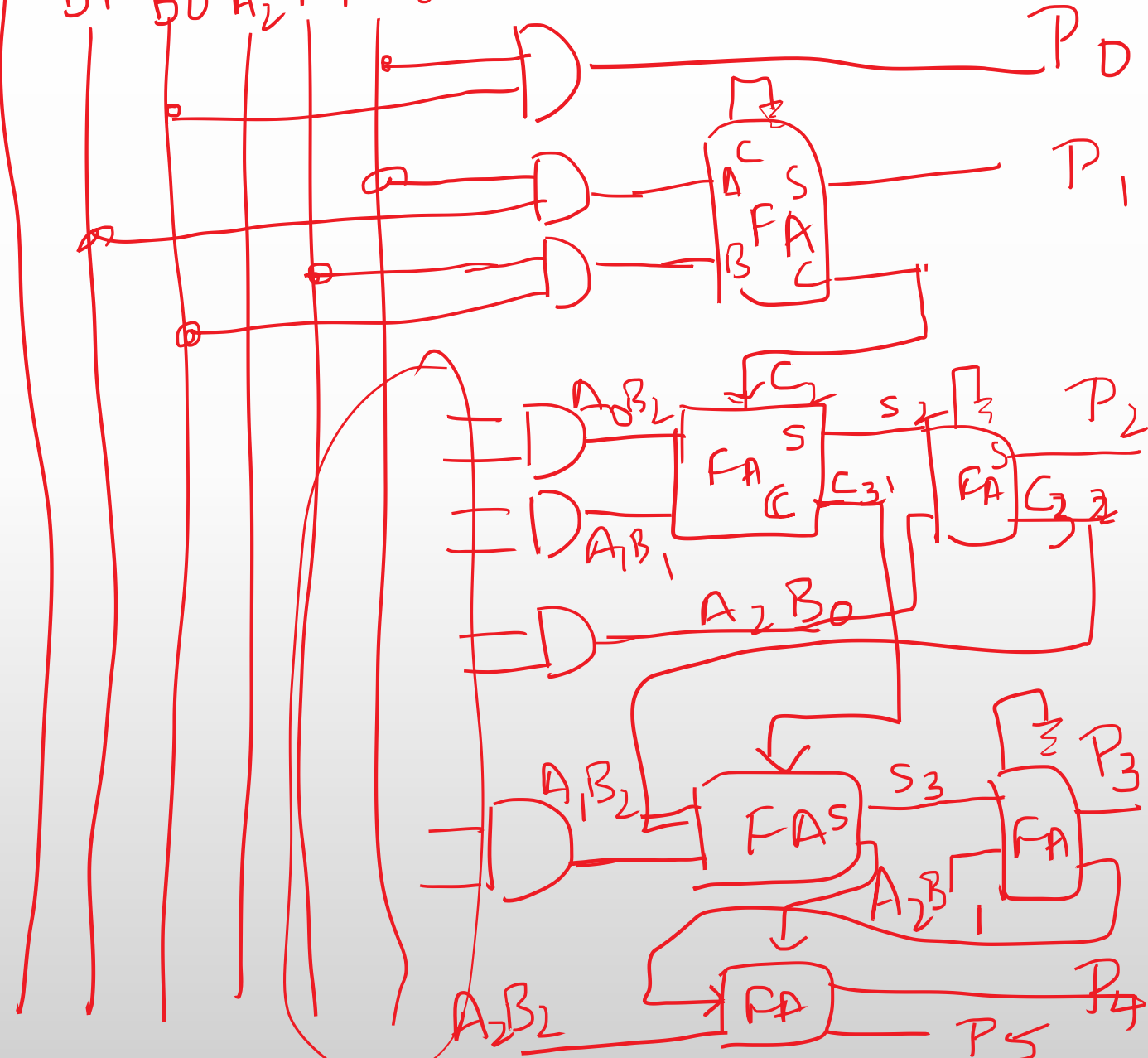
- Design a 3 bit x 3 bit binary multiplier using Full adders and external AND gates.

$$B_2 B_1 B_0 \times A_2 A_1 A_0$$

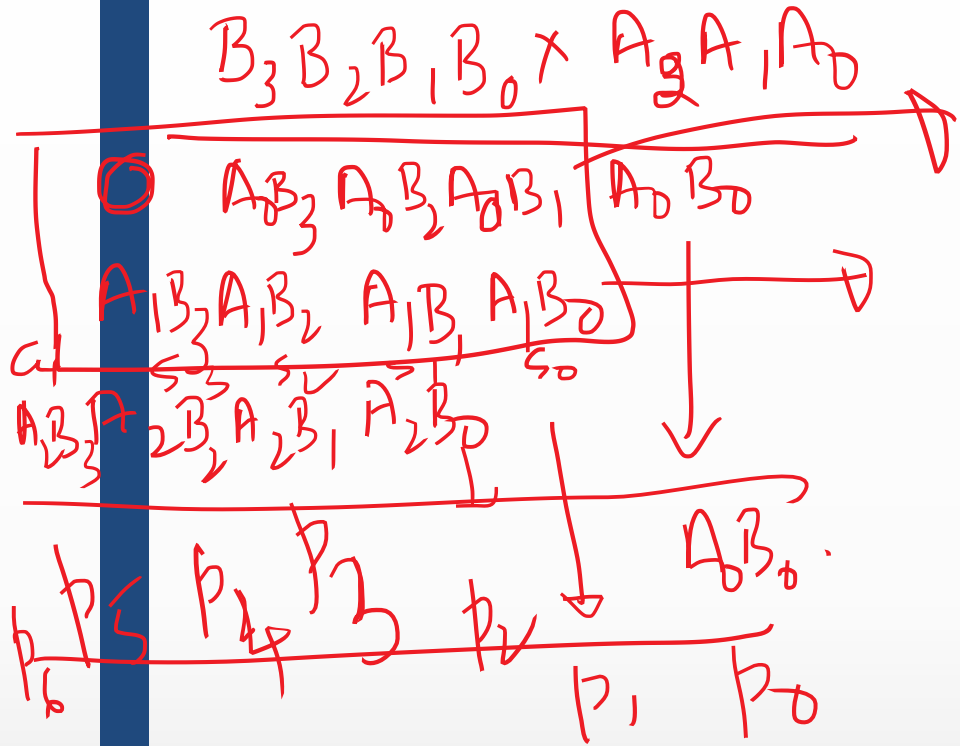
$$\begin{array}{r} C_2 \\ C_{31} \quad A_0 B_2 \quad A_0 B_1 \quad A_0 B_0 \\ C_{32} \\ C_{41} \quad A_1 B_2 \quad A_1 B_1 \quad A_1 B_0 \\ C_{42} \\ A_2 B_2 \quad A_2 B_1 \quad A_2 B_0 \end{array}$$

$$\begin{array}{r} C_{41} \quad C_{31} \quad C_2 \quad \checkmark \quad (A_0 B_1) \quad A_0 B_0 \\ + \quad + \quad + \quad + \quad + \quad + \\ C_{42} \quad C_{32} \quad A_0 B_2 \quad (A_1 B_0) \quad P_0 \\ + \quad + \quad + \quad + \quad + \quad + \\ A_2 B_2 \quad A_1 B_1 \quad A_1 B_1 \quad A_1 B_1 \quad A_1 B_1 \quad A_1 B_1 \\ \underbrace{A_2 B_2}_{P_5} \quad \underbrace{A_1 B_2}_{P_4} \quad \underbrace{A_0 B_2}_{P_3} \quad \underbrace{A_2 B_1}_{P_4} \quad \underbrace{A_1 B_1}_{P_3} \quad \underbrace{A_0 B_1}_{P_2} \end{array}$$

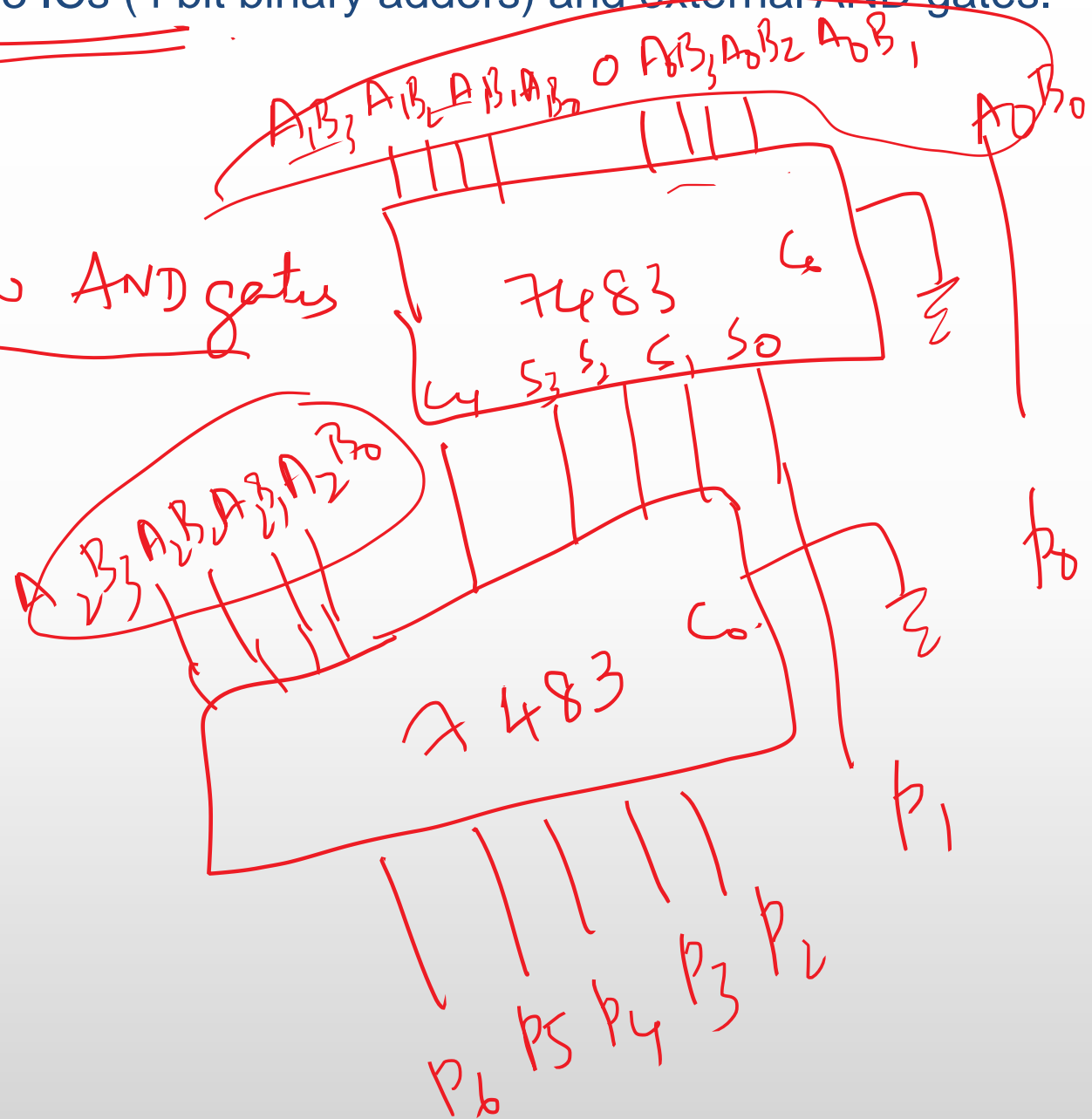
$$B_2 B_1 B_0 A_2 A_1 A_0$$



Design a 4 bit x 3 bit binary multiplier using 7483 ICs (4 bit binary adders) and external AND gates.



Draw AND gates



# Magnitude Comparator

## ■ 1 bit Magnitude comparator

Input		Output		
A	B	$G$ $A > B$	$E$ $A = B$	$L$ $A < B$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

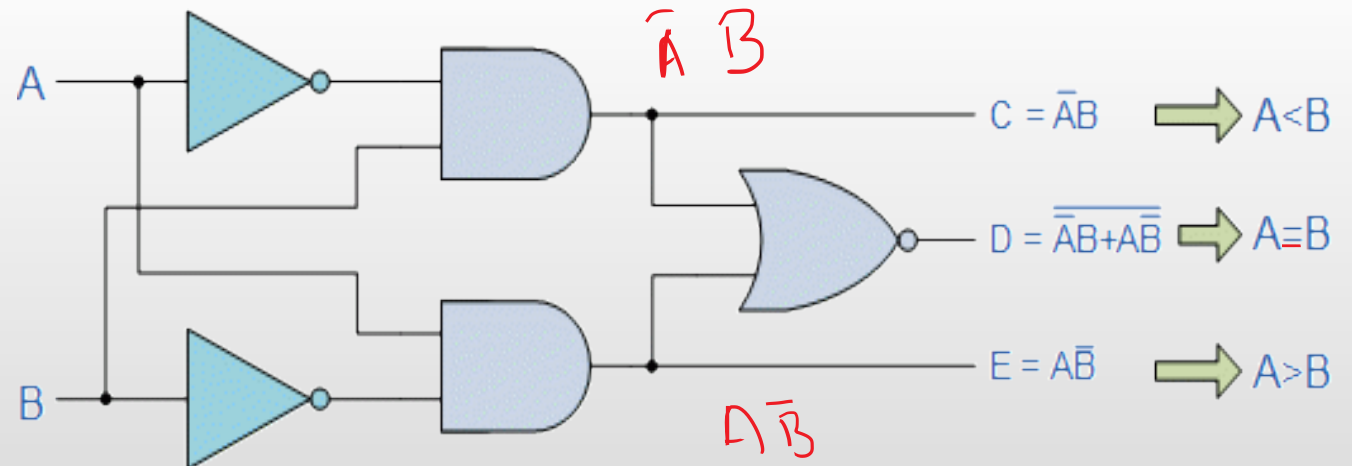
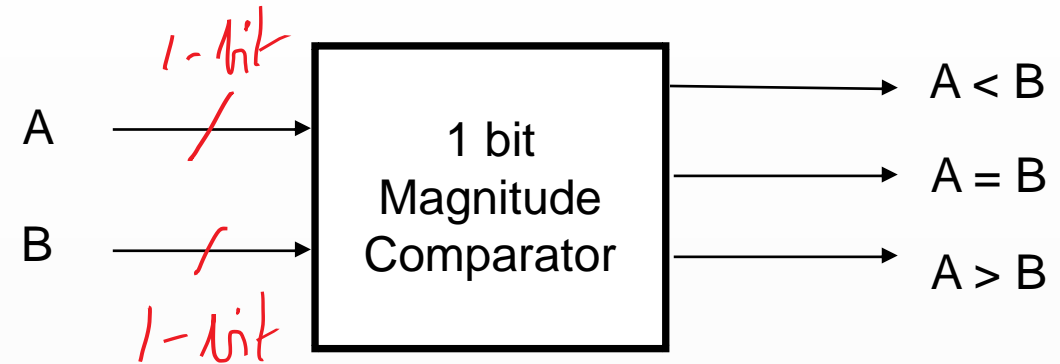
$$A > B, G = A \bar{B}$$

$$A = B, E = \bar{A} \bar{B} + A B$$

$$= \overline{A \oplus B}$$

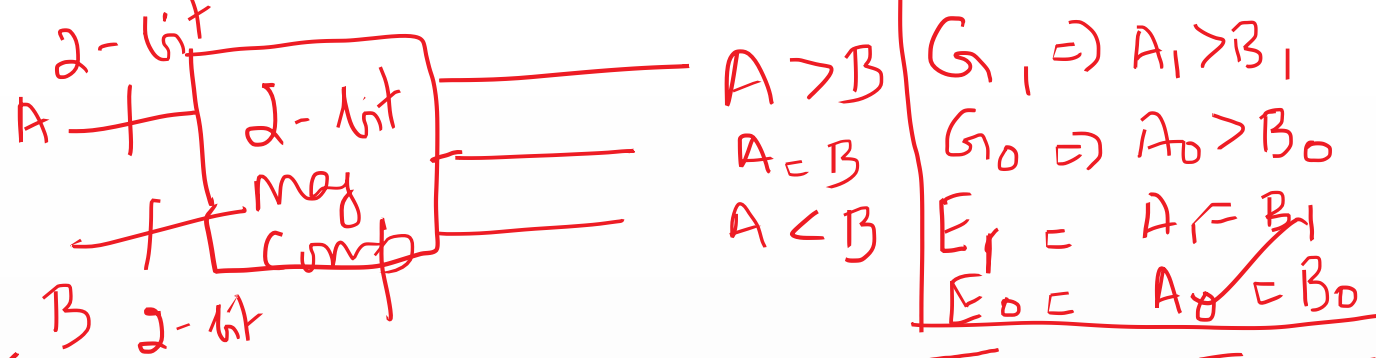
$$= \bar{A} B + A \bar{B} = G + L$$

$$A < B, L = \bar{A} B$$



## 2 bit magnitude comparator

Inputs				Outputs		
A <sub>1</sub>	A <sub>0</sub>	B <sub>1</sub>	B <sub>0</sub>	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0



$$A > B, G = \bar{A}_1 \bar{A}_0 \bar{B}_1 B_0 + \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 \bar{A}_0 B_1 B_0 + \bar{A}_1 \bar{A}_0 B_1 \bar{B}_0$$

$$+ \bar{A}_1 A_0 \bar{B}_1 B_0 + \bar{A}_1 A_0 \bar{B}_1 \bar{B}_0$$

$$A_1 \bar{B}_1 \left[ \bar{A}_0 \bar{B}_0 + \bar{A}_0 B_0 + \bar{A}_0 \bar{B}_0 + \bar{A}_0 B_0 \right]$$

$$+ A_0 \bar{B}_0 \left[ \bar{A}_1 \bar{B}_1 + \bar{A}_1 B_1 \right]$$

$$= A_1 \bar{B}_1 + A_0 \bar{B}_0 \left[ A_1 \oplus B_1 \right]$$

$$G = G_1 + G_0 E_1$$

$$G_1 \Rightarrow A_1 \bar{B}_1$$

$$G_0 \Rightarrow A_0 \bar{B}_0$$

$$E_1 = \overline{A_1 \bar{B}_1 + \bar{A}_1 B_1}$$

$$= G_1 + L_1$$

$$E_0 = \overline{G_0 + L_0}$$

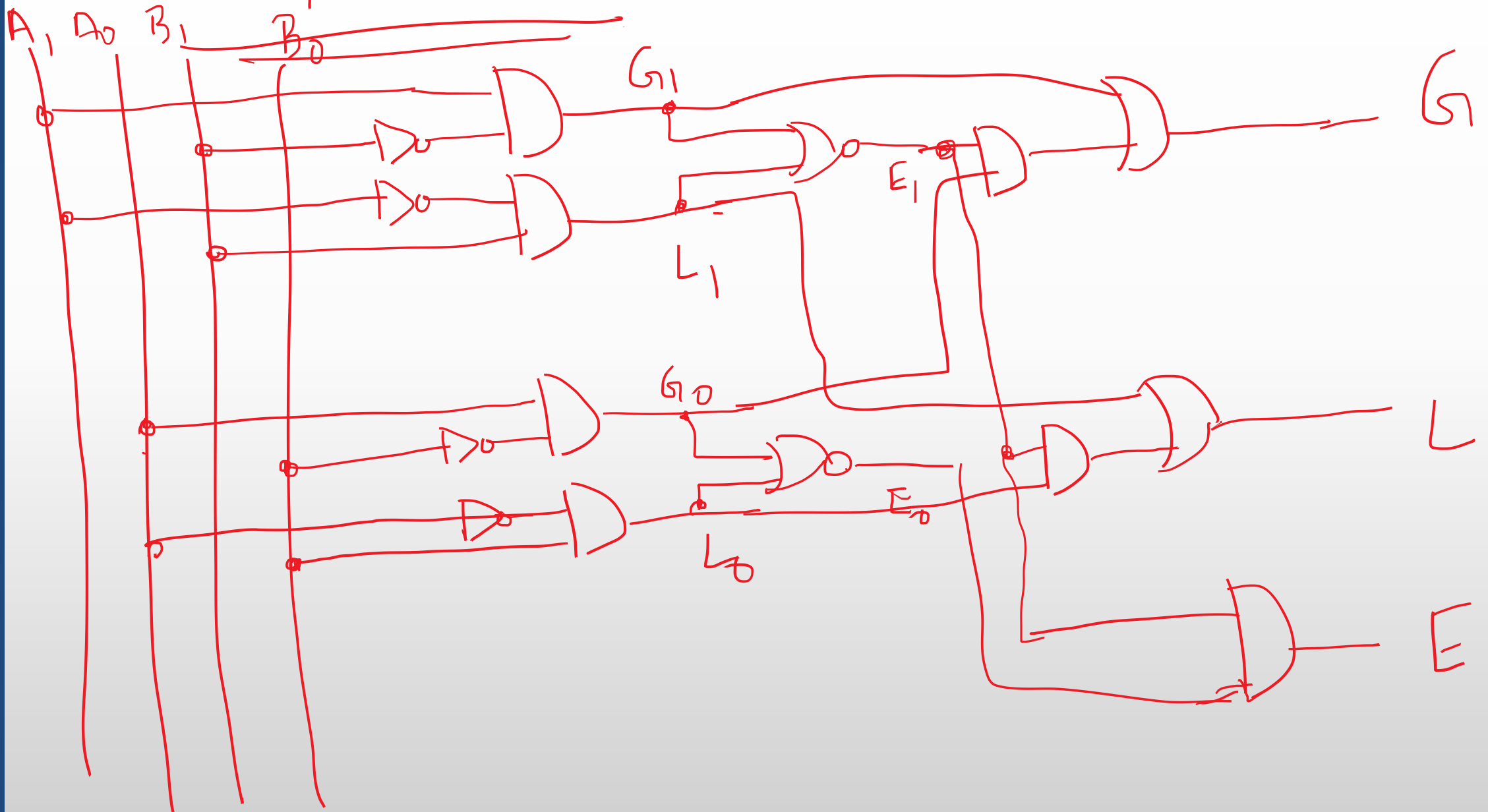
$$L_1 = \bar{A}_1 B_1$$

$$L_0 = \bar{A}_0 B_0$$

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$$\begin{aligned} E &= \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 A_0 \bar{B}_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0 + A_1 A_0 B_1 B_0 \\ &= \bar{A}_1 \bar{B}_1 [\bar{A}_0 \bar{B}_0 + A_0 B_0] + A_1 B_1 [\bar{A}_0 \bar{B}_0 + A_0 B_0] \\ &= [\bar{A}_1 \bar{B}_1 + A_1 B_1] [\bar{A}_0 \bar{B}_0 + A_0 B_0] \\ &= E_1 E_0 \end{aligned}$$

$$L = L_1 + \bar{E}_1 L_0$$





■ 3 bit magnitude comparator

$$A_2 A_1 A_0 \leftrightarrow B_2 B_1 B_0$$

$$G = \underline{G_2 + E_2 G_1 + E_2 E_1 G_0}$$

$$E = \underline{E_2 E_1 E_0}$$

$$L = \underline{L_2 + E_2 L_1 + E_2 E_1 L_0}$$

Draw the circuit

## ■ 4 bit magnitude comparator

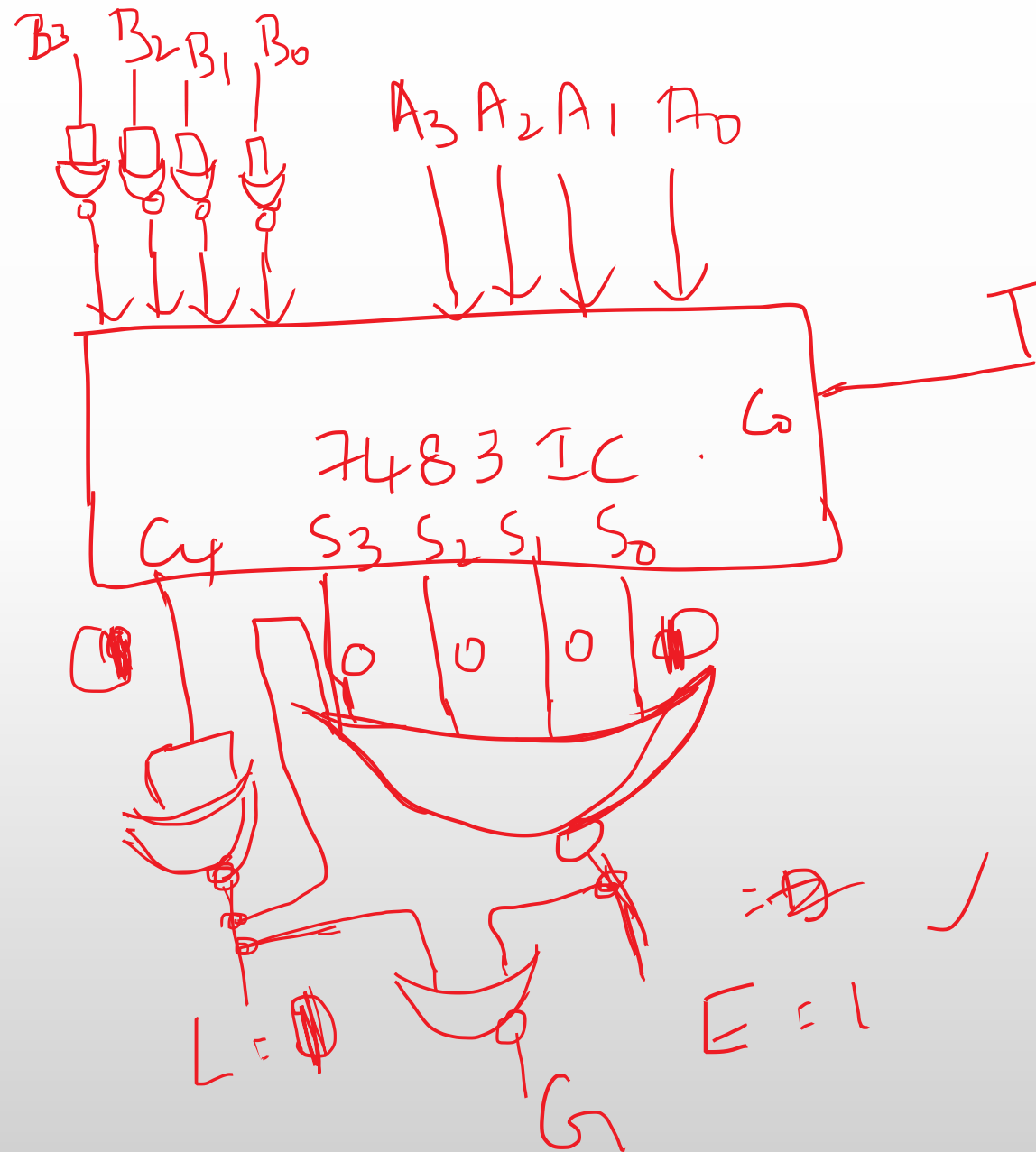
$$G = G_3 + E_3 G_2 + E_3 E_2 G_1 + E_3 E_2 E_1 G_0$$

$$E = E_3 E_2 E_1 E_0$$

$$L = L_3 + \bar{E}_3 L_2 + \bar{E}_3 \bar{E}_2 L_1 + \bar{E}_3 \bar{E}_2 \bar{E}_1 L_0$$

Draw the circuit

# Design 4 bit magnitude comparator using 7483 IC and external gates. <sup>NOR</sup>



A - B

Carry  $\neq 1 \Rightarrow A > B$  ✓

$V_{CC}$  Carry  $= 0 \Rightarrow A < B$  ✓

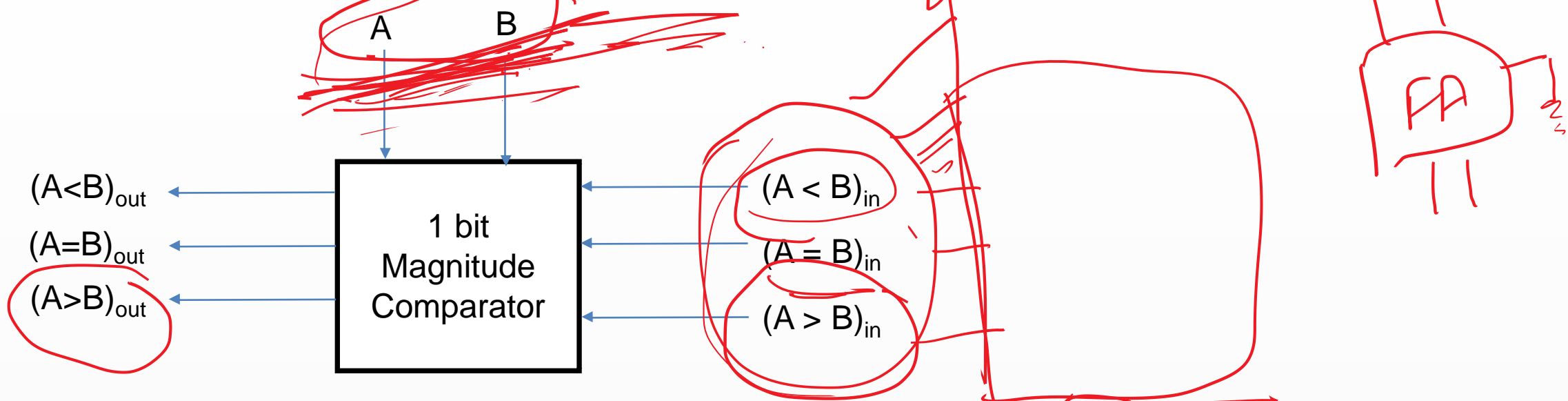
$C = 1 \Rightarrow A = B$  ✓

4  $\rightarrow 0100$

-4  $\rightarrow 1011$

10000

■ 1 bit magnitude comparator with cascading input:



$$(A > B)_{out} = (A > B) + (A = B)(A > B)_{in}$$

$$(A < B)_{out} = (A < B) + (A = B)(A < B)_{in}$$

$$(A = B)_{out} = (A = B)(A = B)_{in}$$

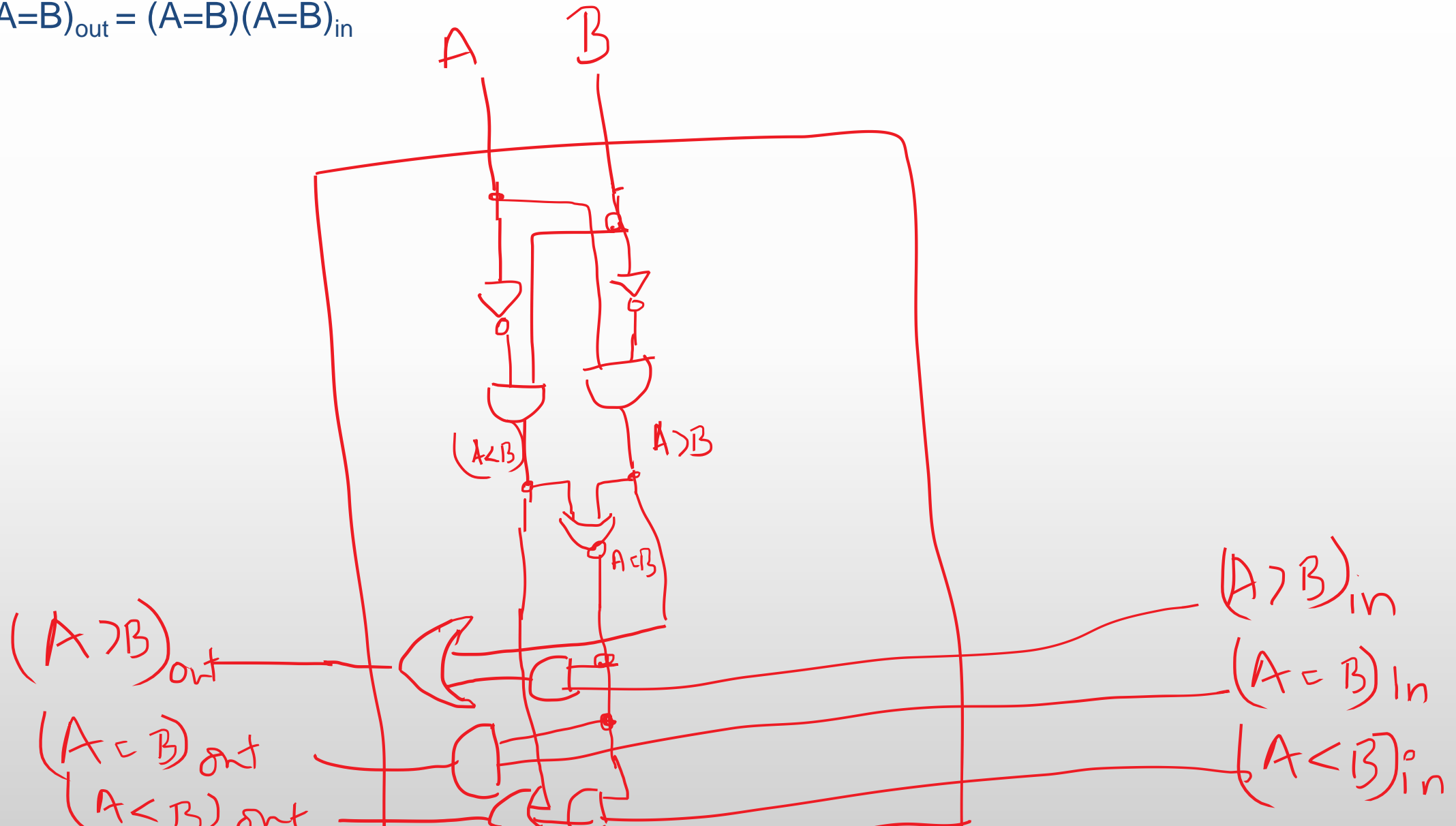
$$G = G_1 + E_1 G_0$$

$$L = L_1 + E_1 L_0$$

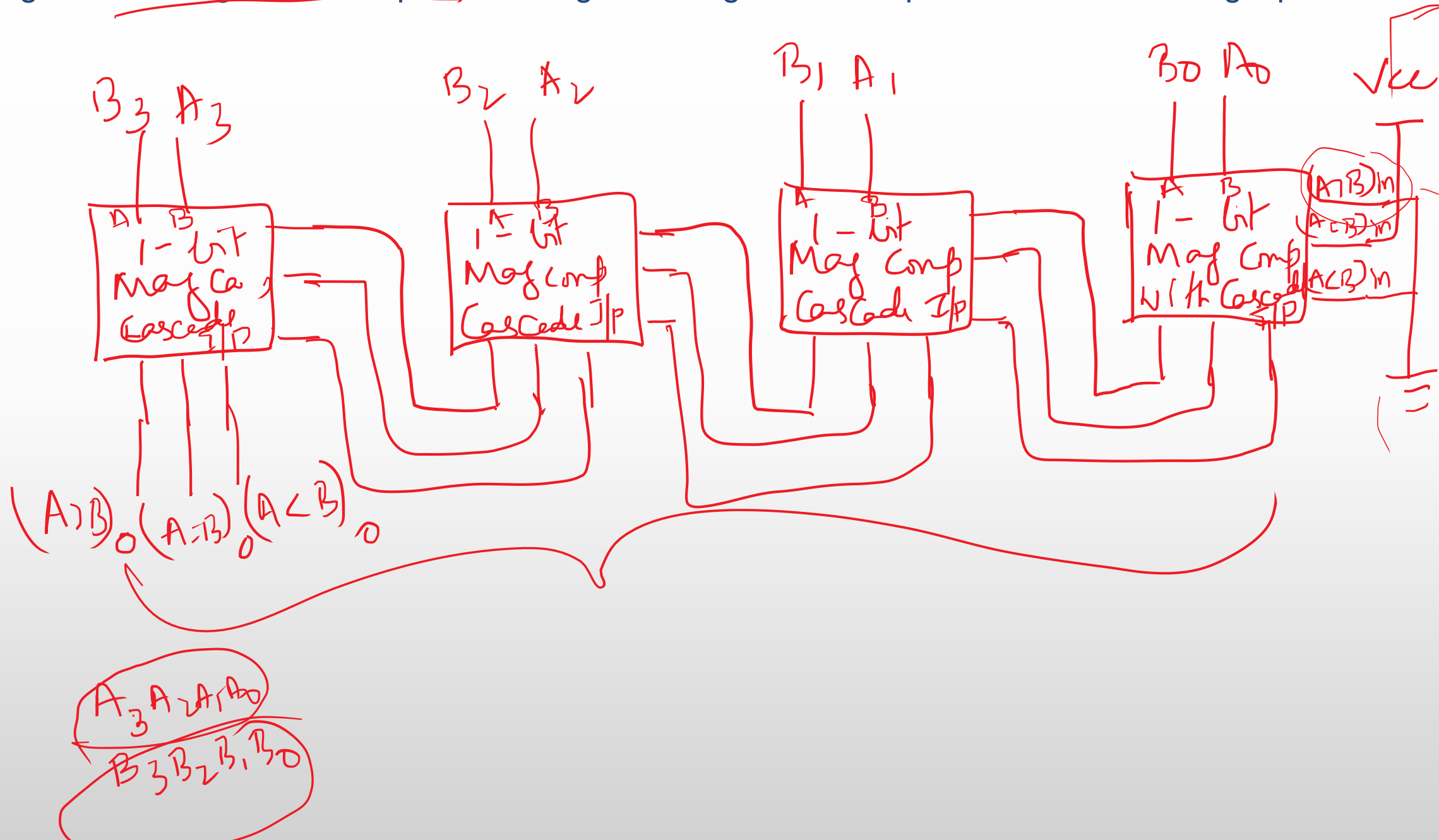
$$(A > B)_{\text{out}} = (A > B) + (A = B)(A > B)_{\text{in}}$$

$$(A < B)_{\text{out}} = (A < B) + (A = B)(A < B)_{\text{in}}$$

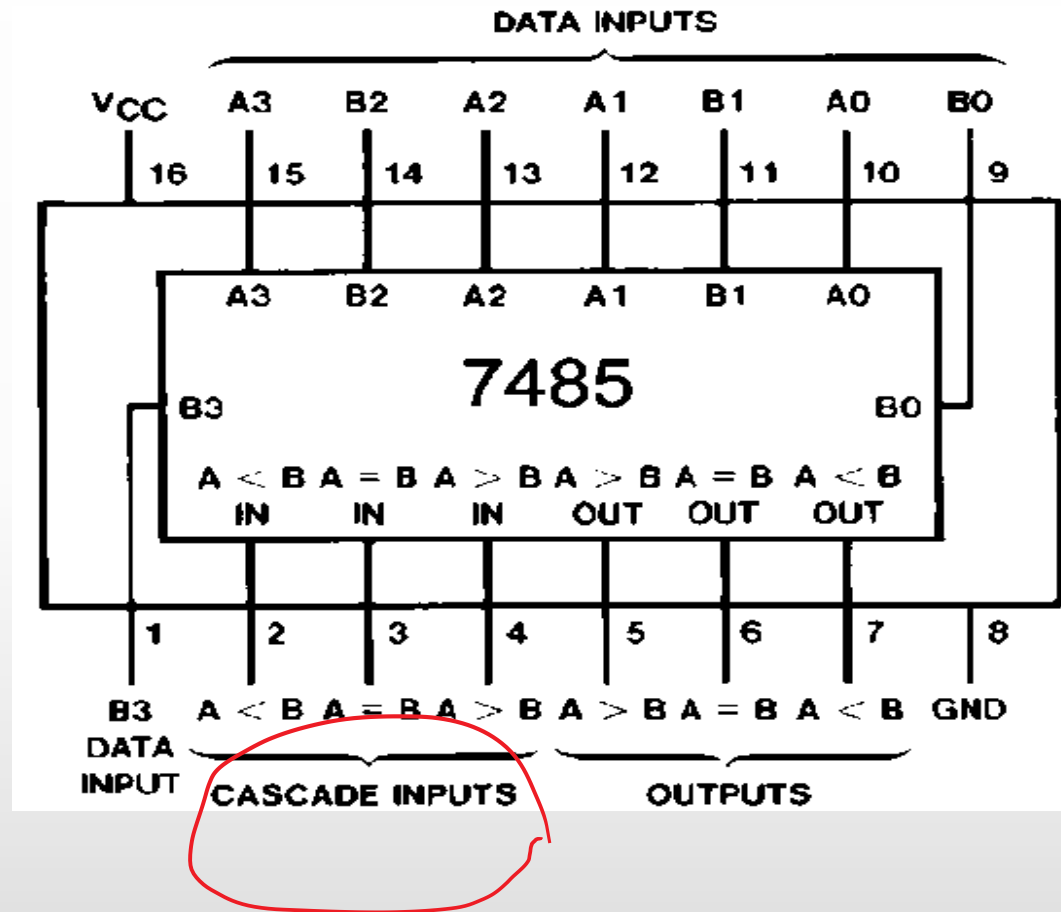
$$(A = B)_{\text{out}} = (A = B)(A = B)_{\text{in}}$$



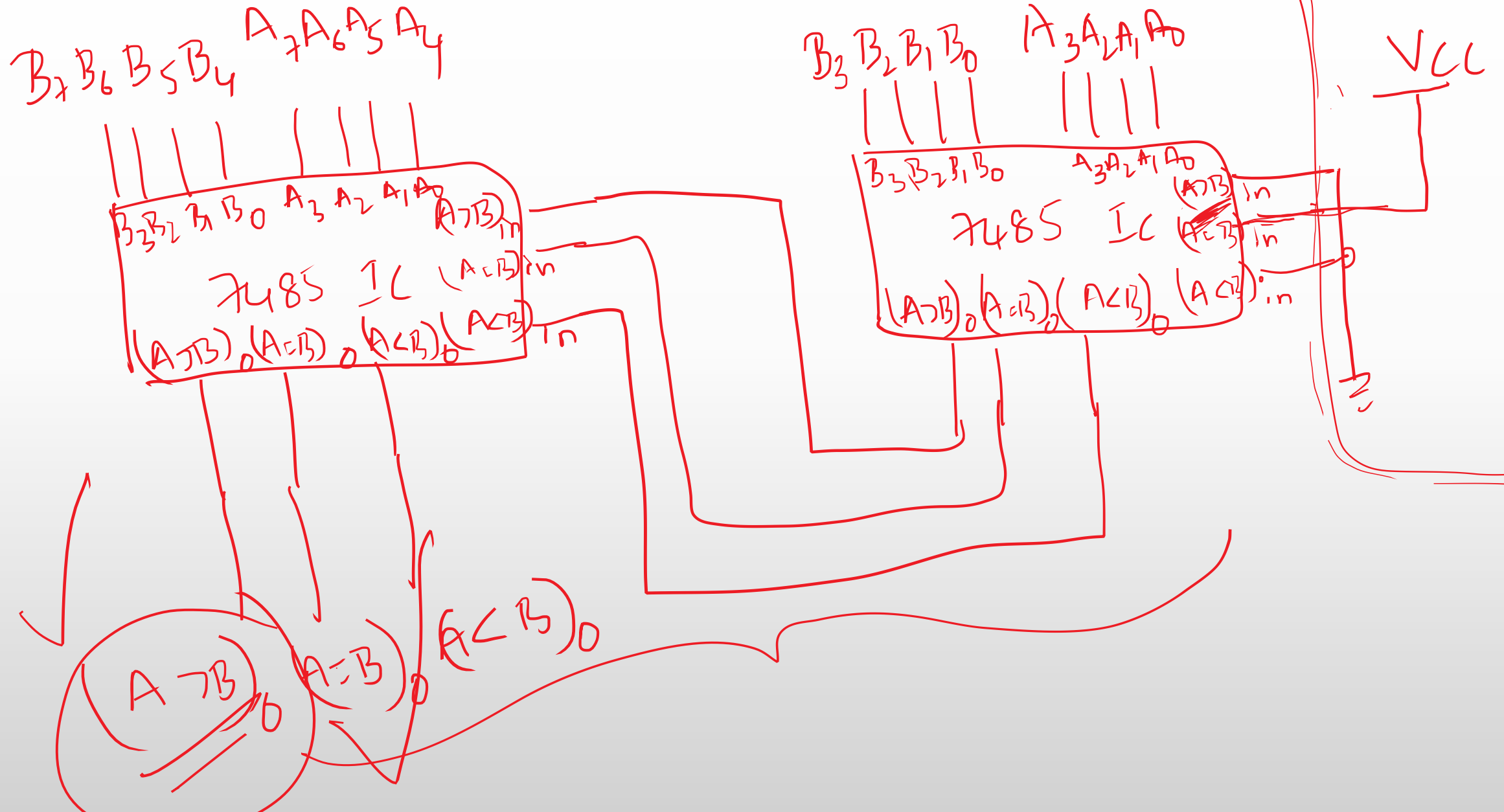
Design a 4 bit magnitude comparator using 1 bit magnitude comparator with cascading inputs.



## 7485 IC ( 4 bit magnitude comparator with cascading inputs)



1 → 2





Design a combinational circuit using multipliers, 7483 IC and external gate to perform

$$F = 2X + Y \text{ when } m=0,$$

$$F = X + 2Y \text{ when } m=1$$

Where  $X$ ,  $Y$  are two bit numbers and output  $F$  is a 4 bit number.

