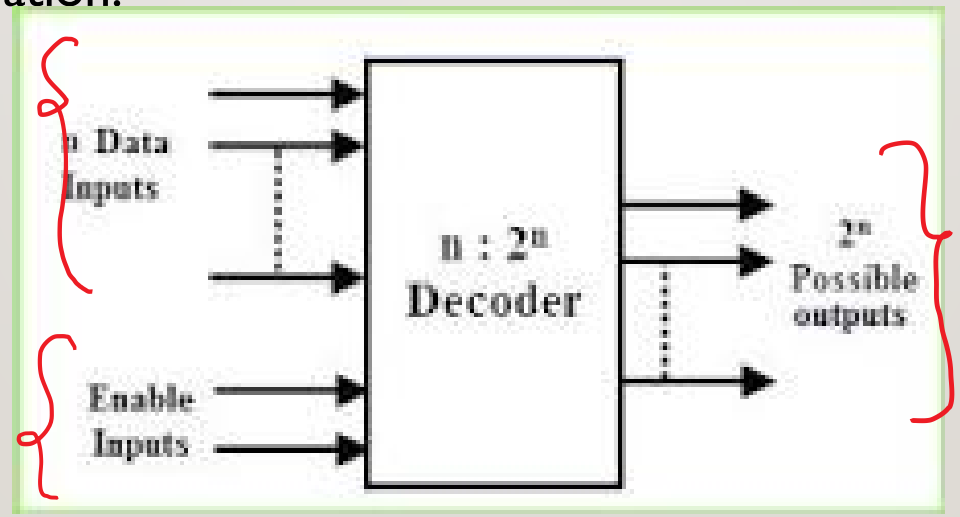
DECODERS AND ENCODERS

STUDENTS ARE ADVISED TO WRITE DOWN THE NOTES FOR EVERY LECTURE

DECODER:

- A combinational circuit
- Converts a binary information from n-input lines to a maximum of 2^n unique output lines (n-to- 2^n line decoder) and one or more enable inputs.Ex: 2-to-4 line, 3-to-8 line..etc
- In standard decoders, only one output line will be active at a time corresponding to the input binary combination.

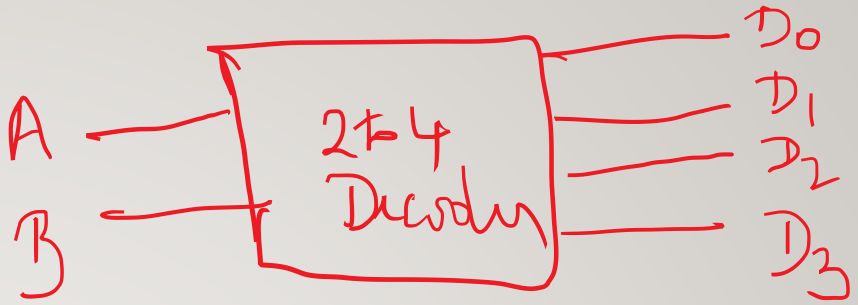


2 to 2^2 → 2 to 4

3 to 2^3 ⇒ 3 to 8

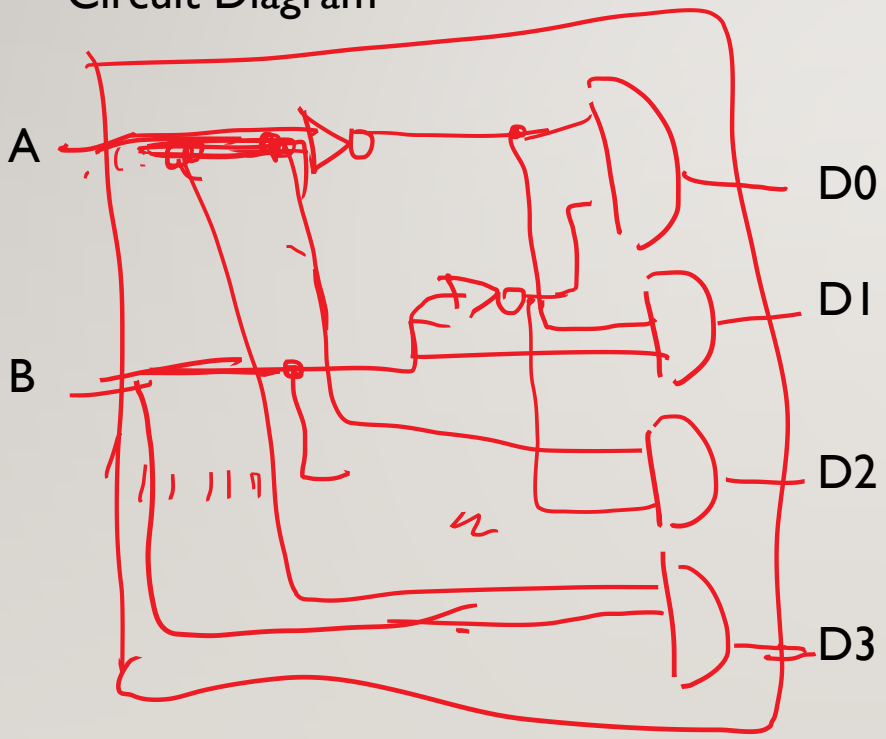
4 to 2^4 ⇒ 4 to 16

2-to-4 line decoder



Active high o/p Decoder

Circuit Diagram



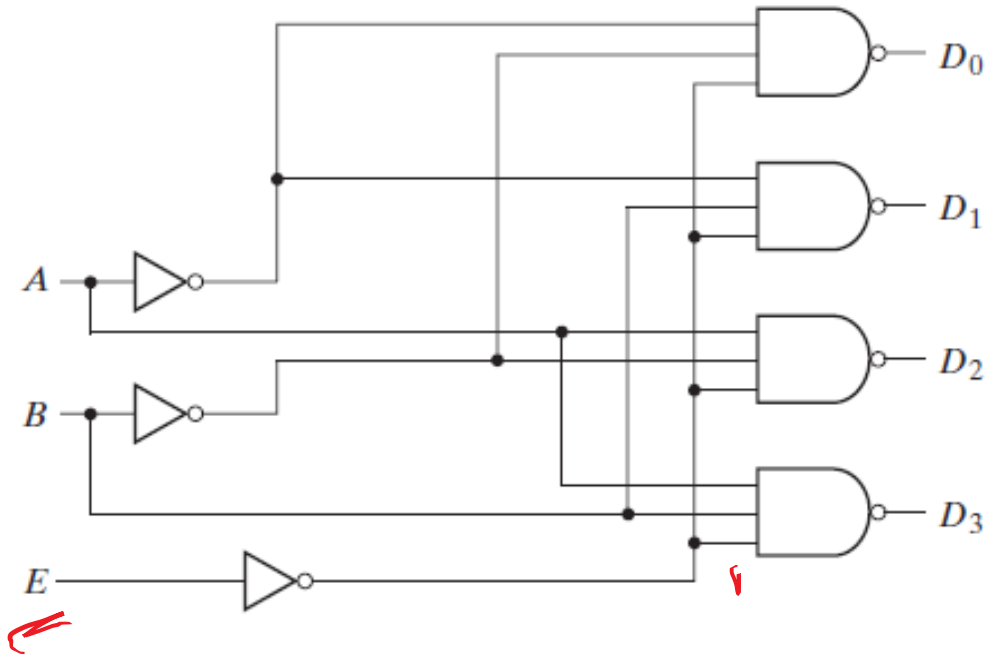
Truth table

A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$D_0 = \bar{A}\bar{B}$ $D_1 = \bar{A}B$

$D_2 = A\bar{B}$ $D_3 = AB$

2-to-4 line decoder with active low output & enable input



(a) Logic diagram

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table

→ Disabled

$D_0 = \overline{E+A+B} = \overline{E} \cdot \overline{A} \cdot \overline{B}$

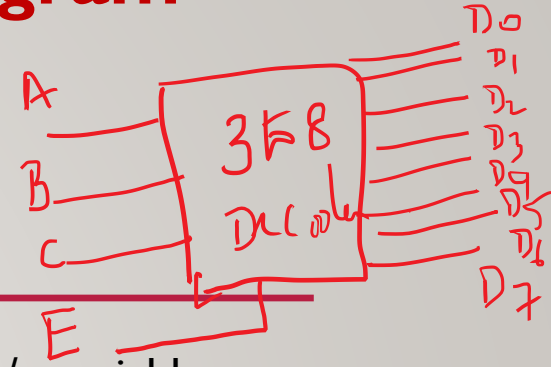
$D_1 = \overline{E+A+\overline{B}} = \overline{E} \cdot \overline{A} \cdot B$

$D_2 = \overline{E+\overline{A}+B} = \overline{E}\,A\,\overline{B}$

$D_3 = \overline{E+\overline{A}+\overline{B}} = \overline{E}\,AB$

Write the truth table ,logic diagram and block diagram of 3-to-8 line decoder

- Note: Unless specified, assume the output and enable input to be active high



Inputs				Outputs							
E	A	B	C	D0	D1	D2	D3	D4	D5	D6	D7
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

Expressions for o/p variables

$D_0 = E\bar{A}\bar{B}\bar{C}$

$D_1 = E\bar{A}\bar{B}C$

$D_2 = E\bar{A}B\bar{C}$

$D_3 = E\bar{A}BC$

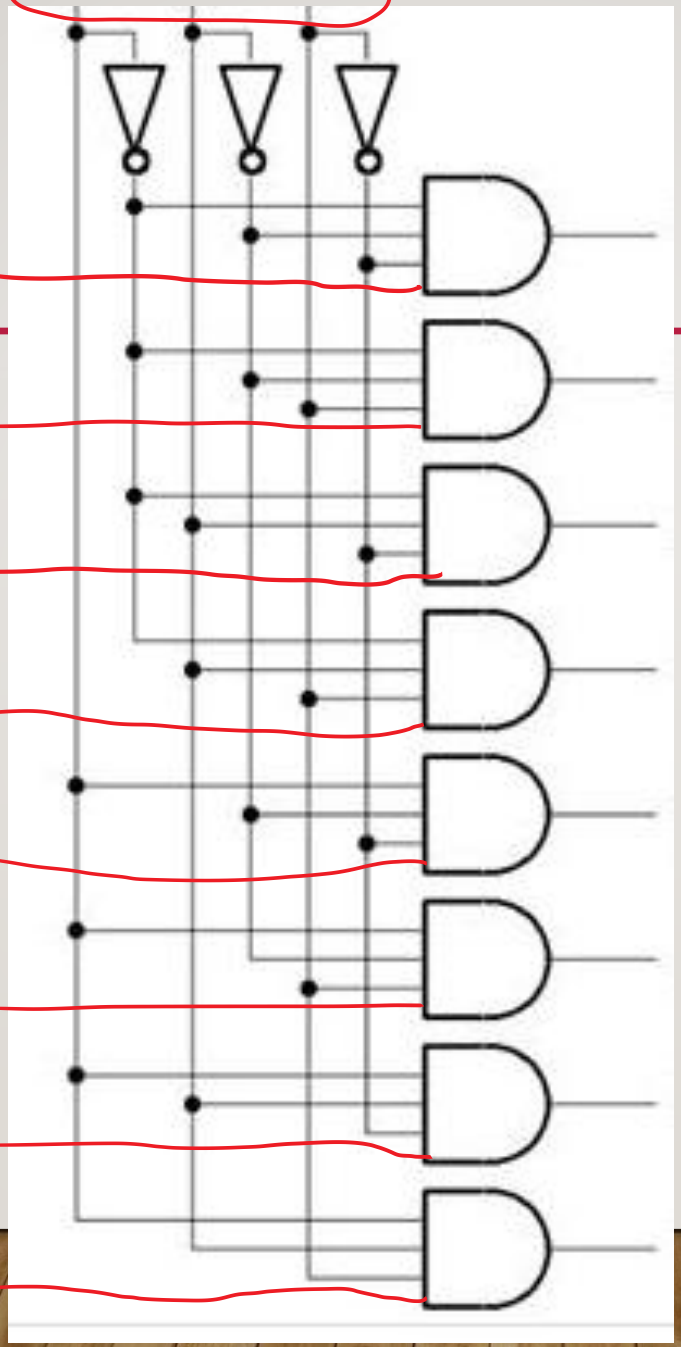
$D_4 = EA\bar{B}\bar{C}$

$D_5 = EA\bar{B}C$

$D_6 = EAB\bar{C}$

$D_7 = EABC$

How do you input enable E to the circuit?



3 to 8 line Decoder with Active low O/P :- Active low Enable.

E	A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
1	x	x	x	1	1	1	1	1	1	1	1
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0

$D_0 = \bar{E}\,\bar{A}\,\bar{B}\,\bar{C}$

$= \overline{E + A + B + C}$

$D_1 = \bar{E} \cdot \bar{A}\,\bar{B}\,C$

$D_2 =$

$D_3 =$

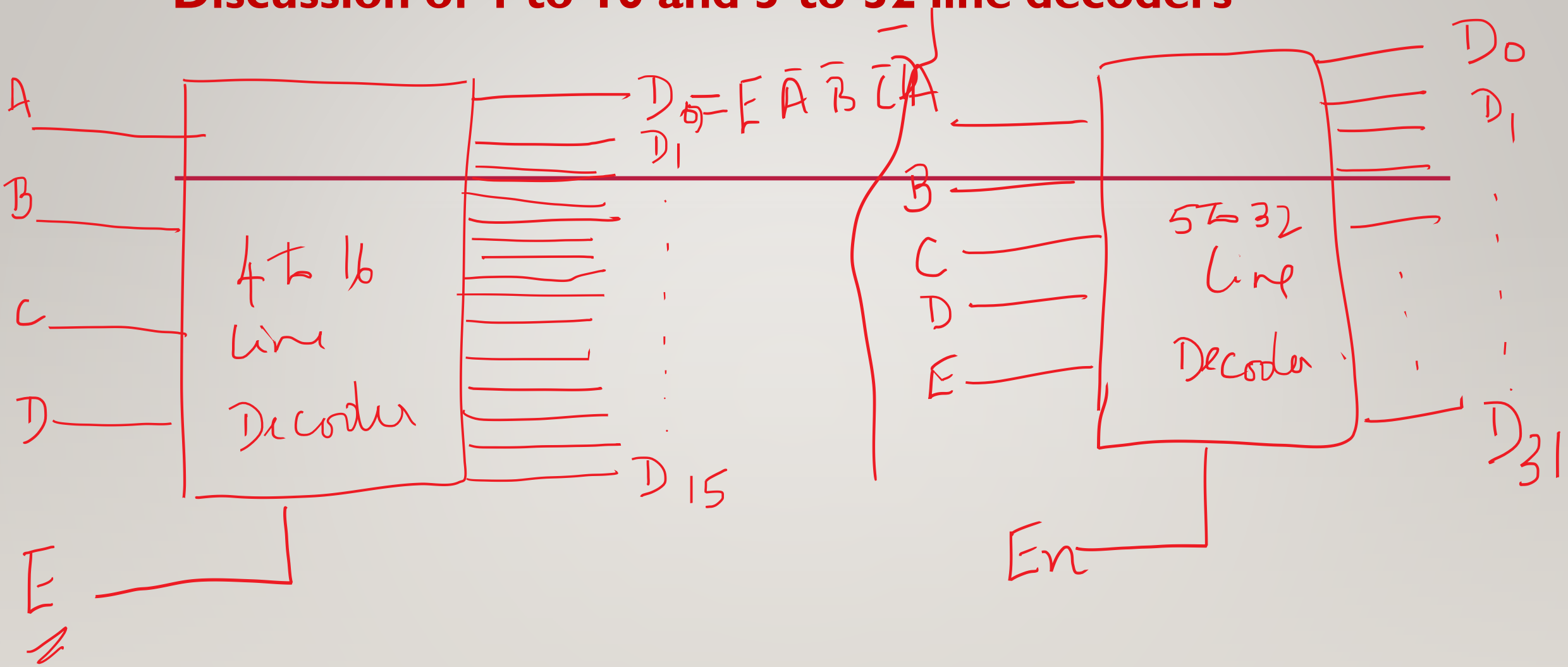
$D_4 =$

$D_5 =$

$D_6 =$

$D_7 =$

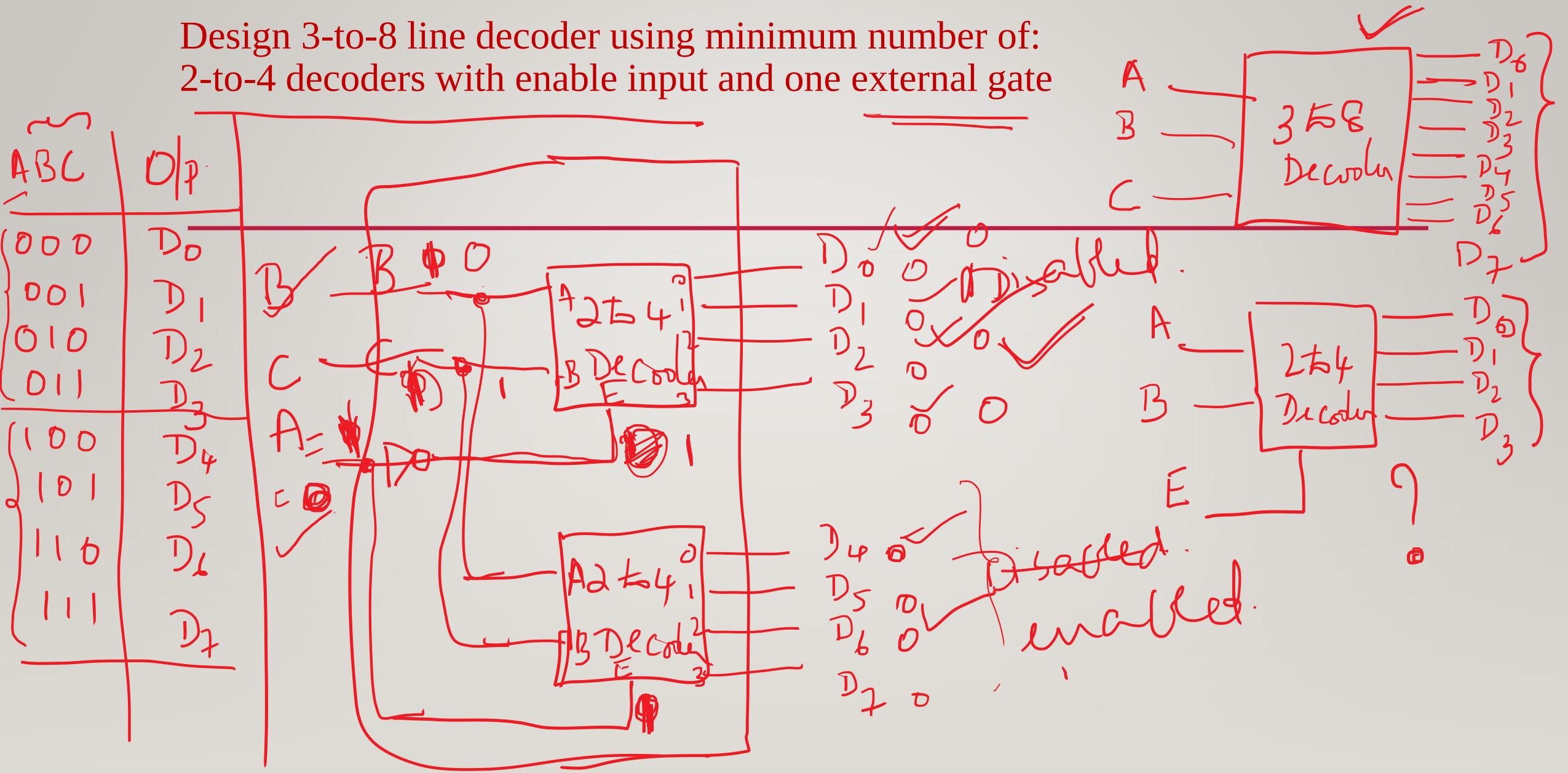
Discussion of 4-to-16 and 5-to-32 line decoders



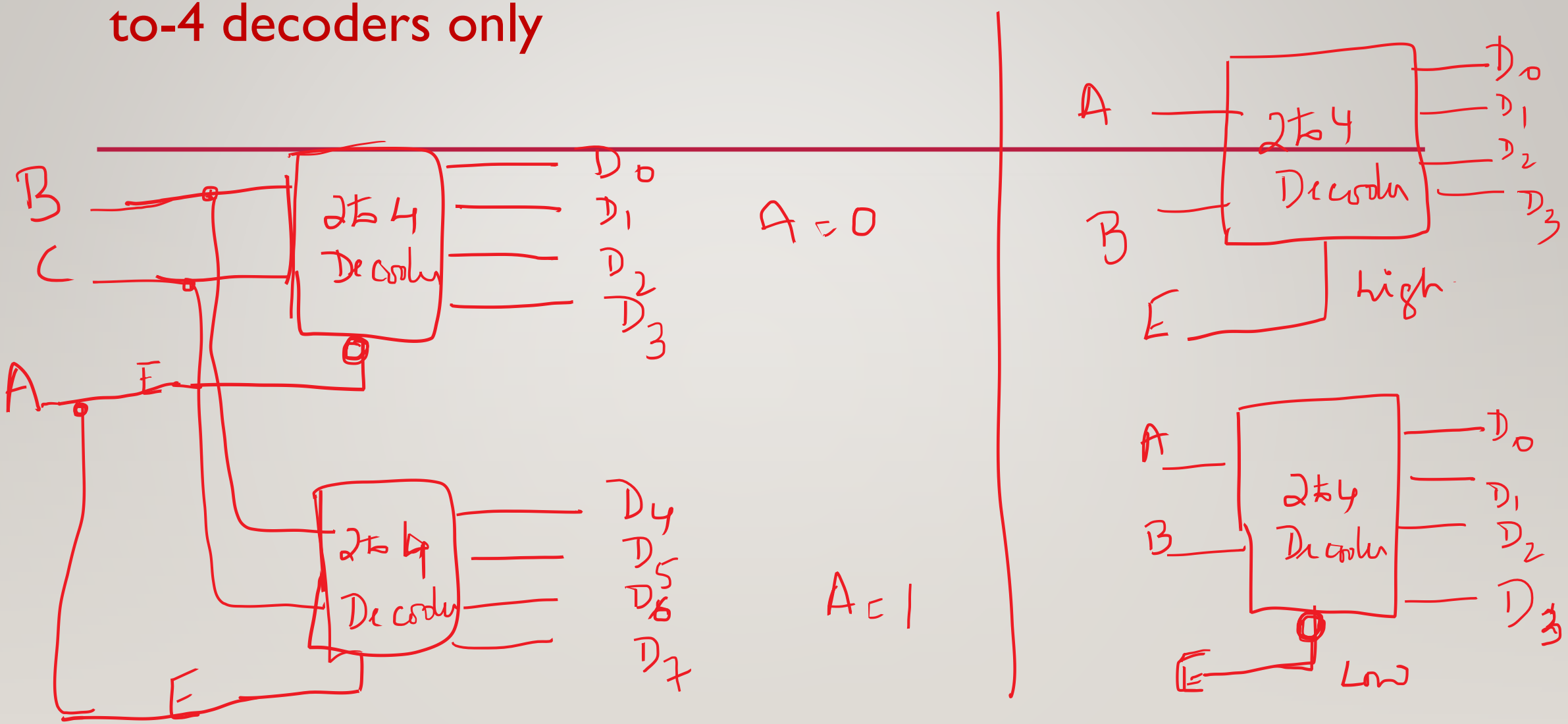
Design 3-to-8 line decoder using minimum number of:

1. 2-to-4 decoders with enable input and one external gate
2. 2-to-4 decoders with enable inputs only

Design 3-to-8 line decoder using minimum number of: 2-to-4 decoders with enable input and one external gate



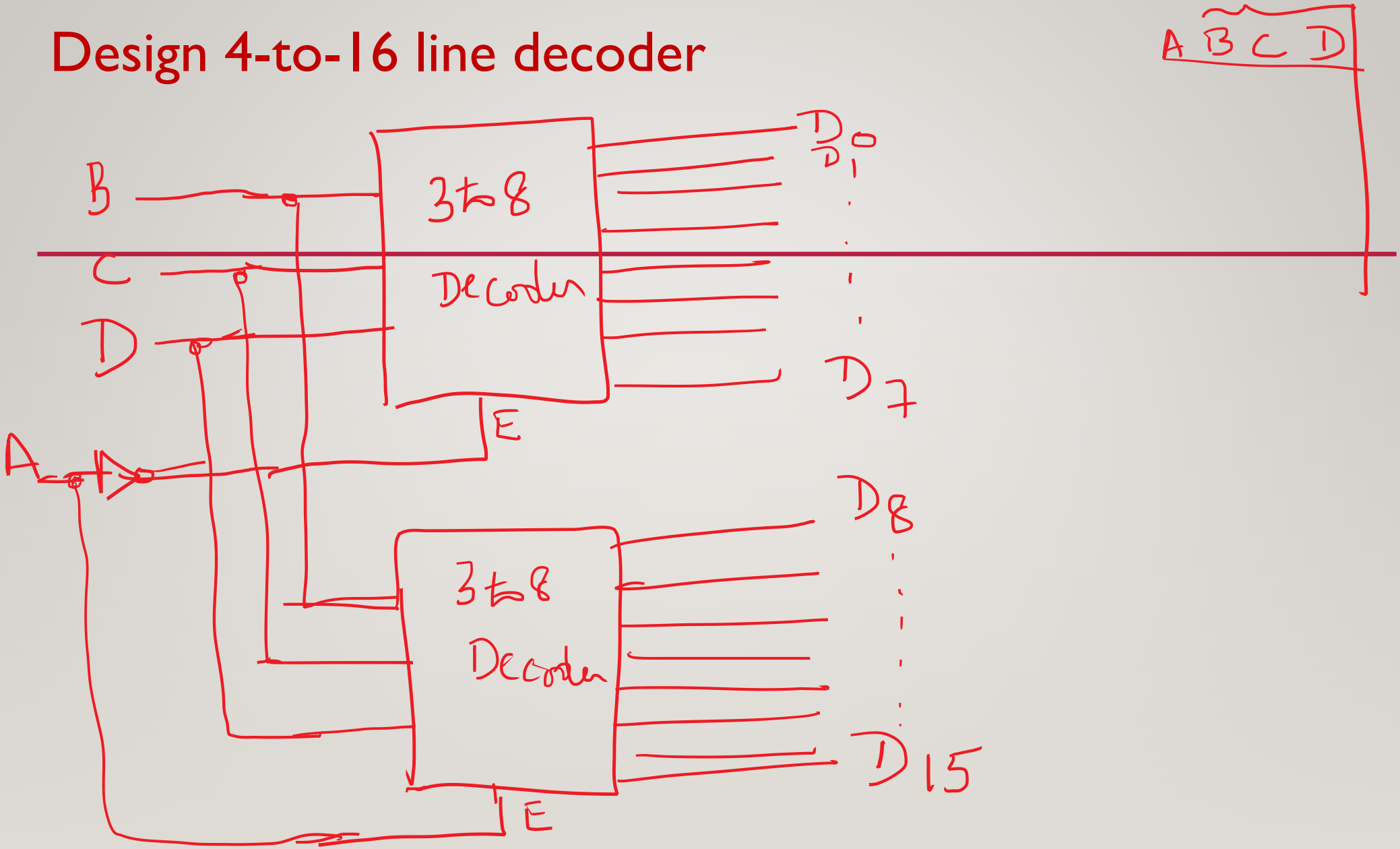
Design 3-to-8 line decoder using minimum number of 2-to-4 decoders only



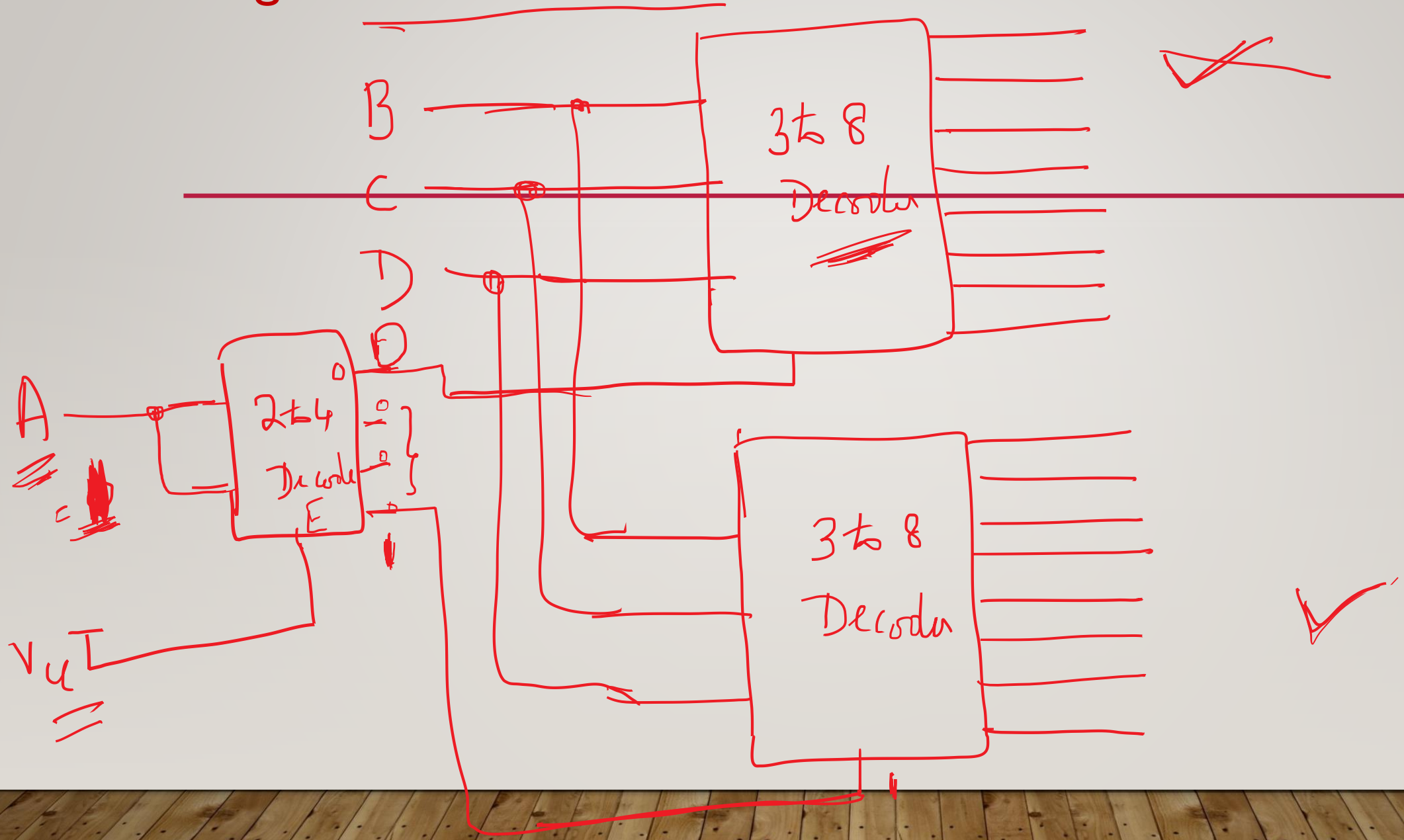
Design 4-to-16 line decoder using minimum number of

1. 3-to-8 decoders with enable input and one external gate
2. Only 3-to-8 and 2-to-4 line decoders with enable inputs
3. Only 2-to-4 line decoders with enable inputs

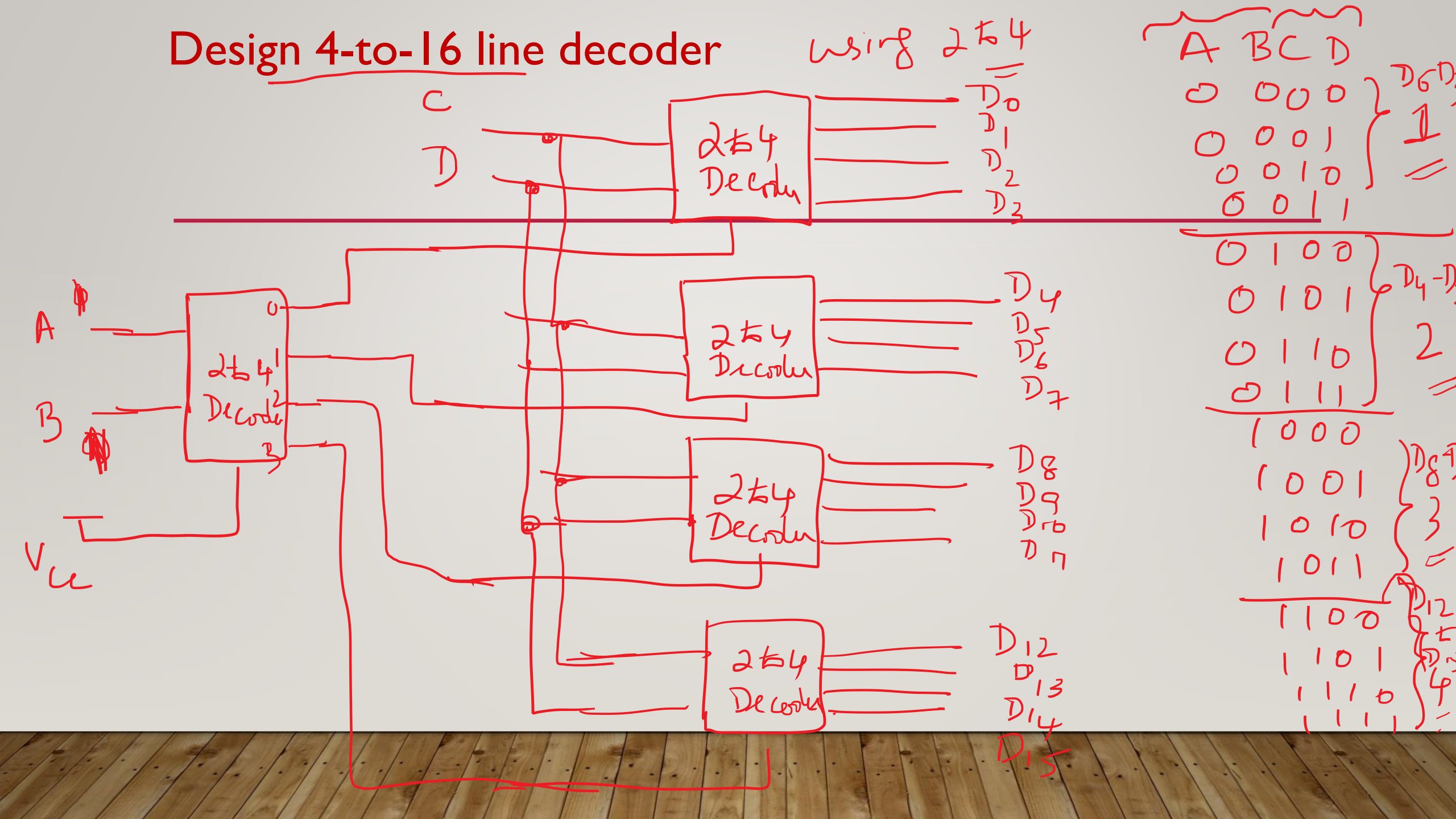
Design 4-to-16 line decoder



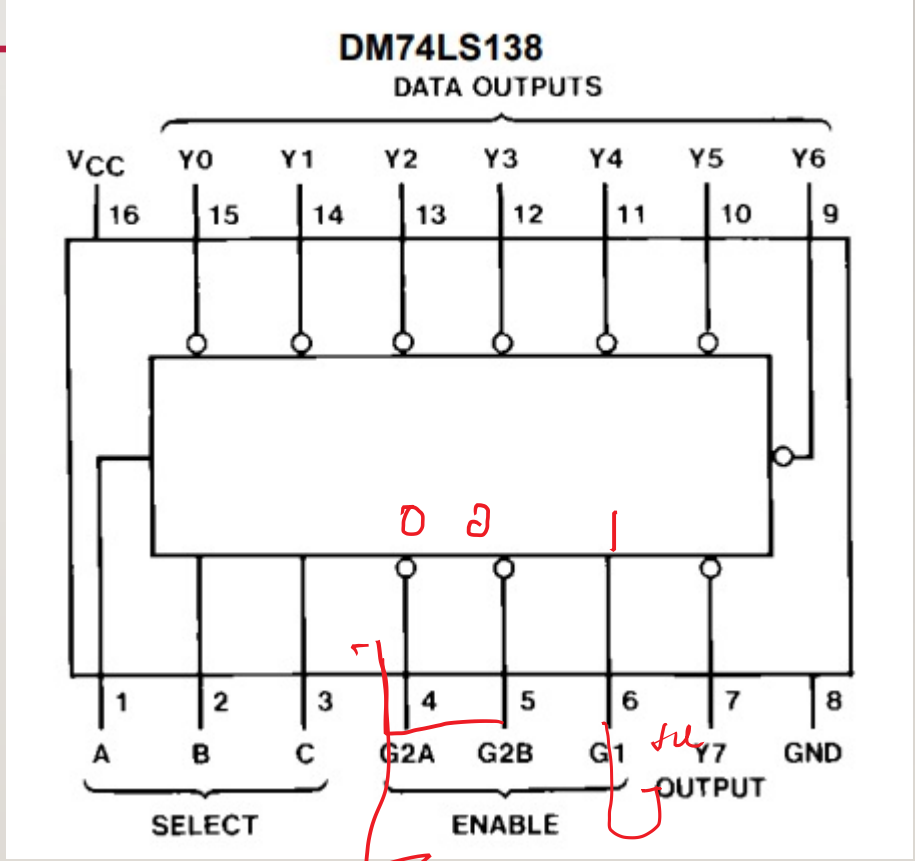
Design 4-to-16 line decoder



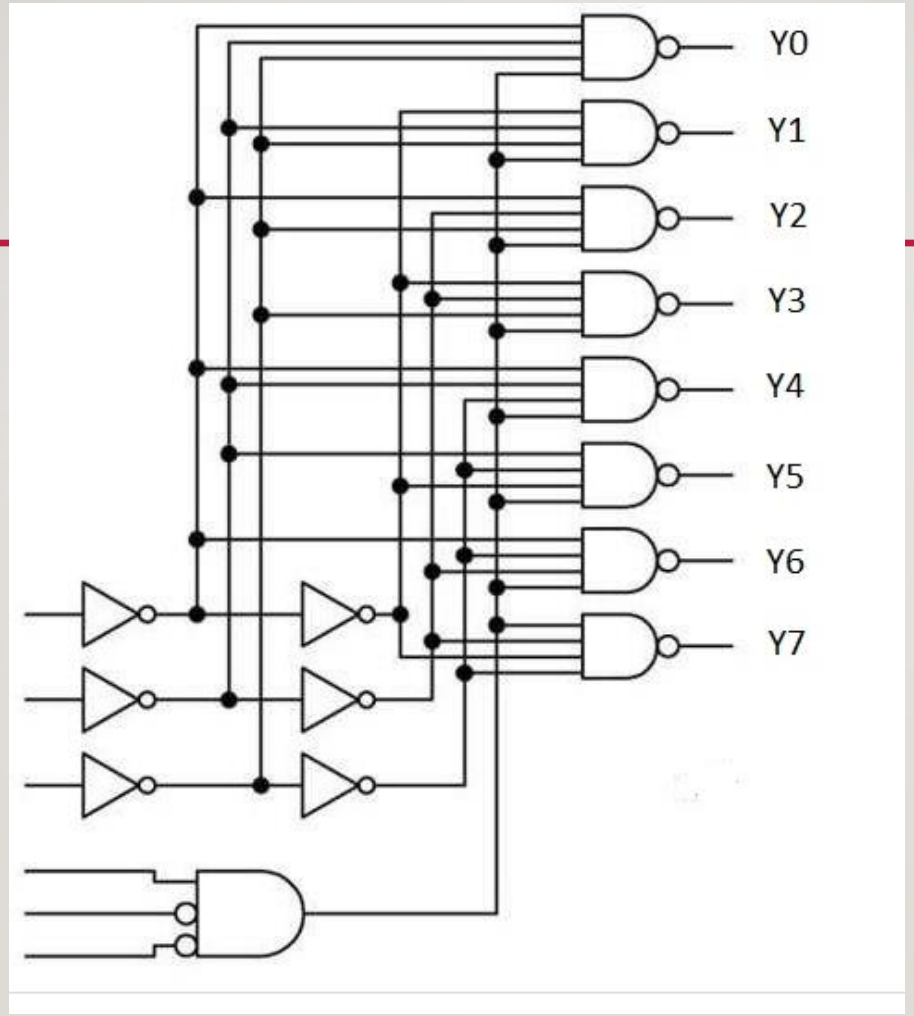
Design 4-to-16 line decoder



74138 IC: 3-to-8 line decoder with active low output



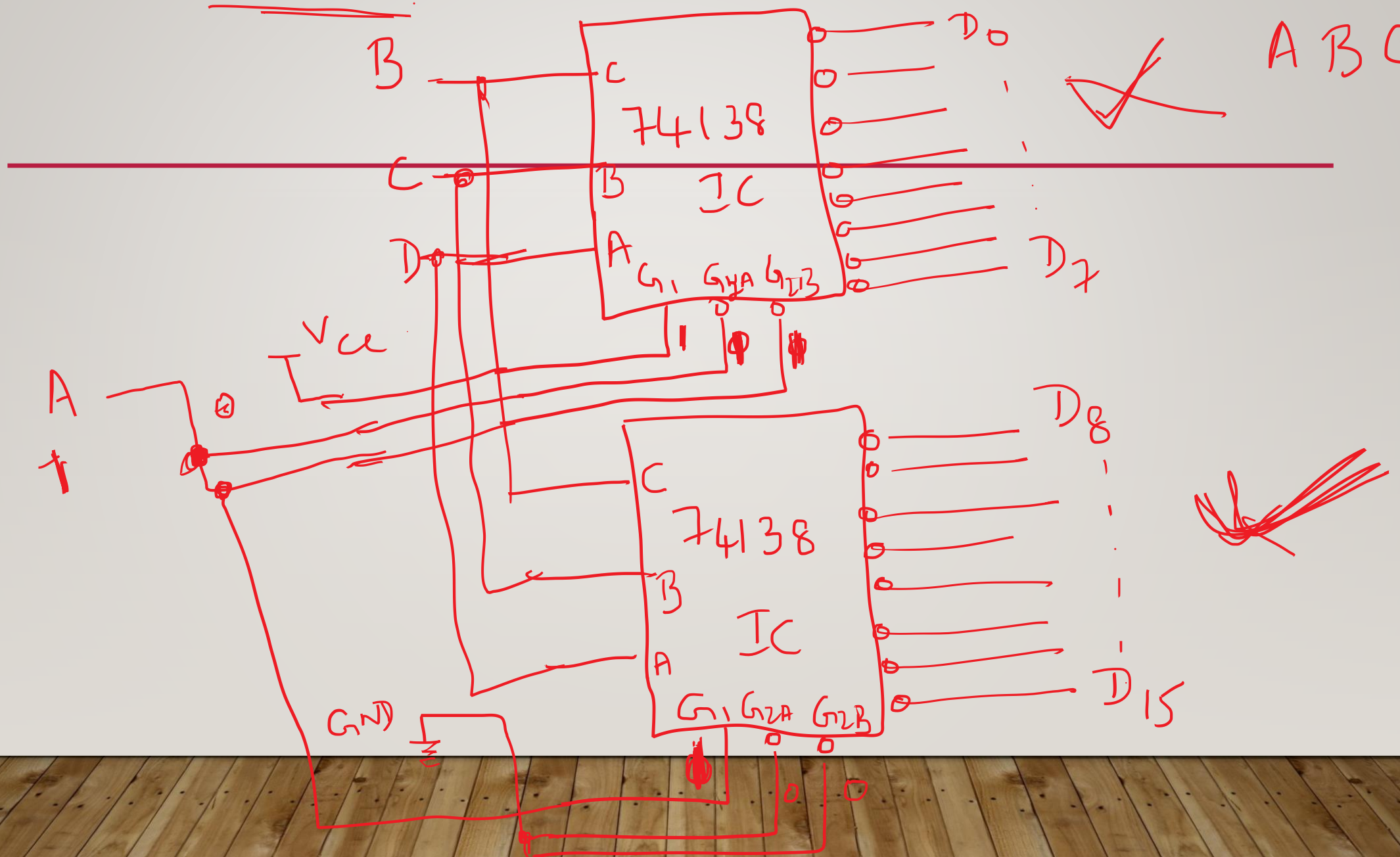
74138 IC internal diagram



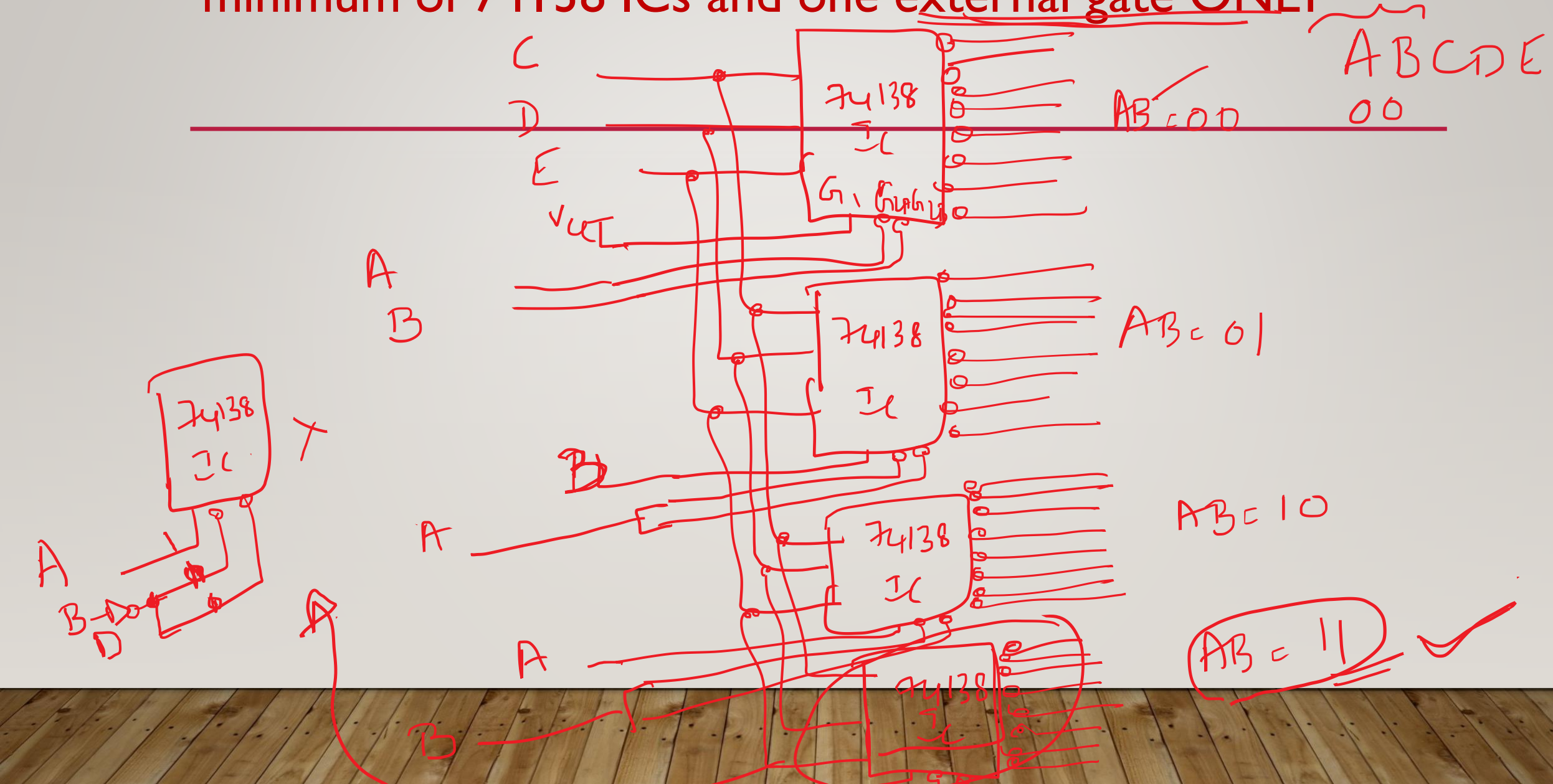
A B C

C B A

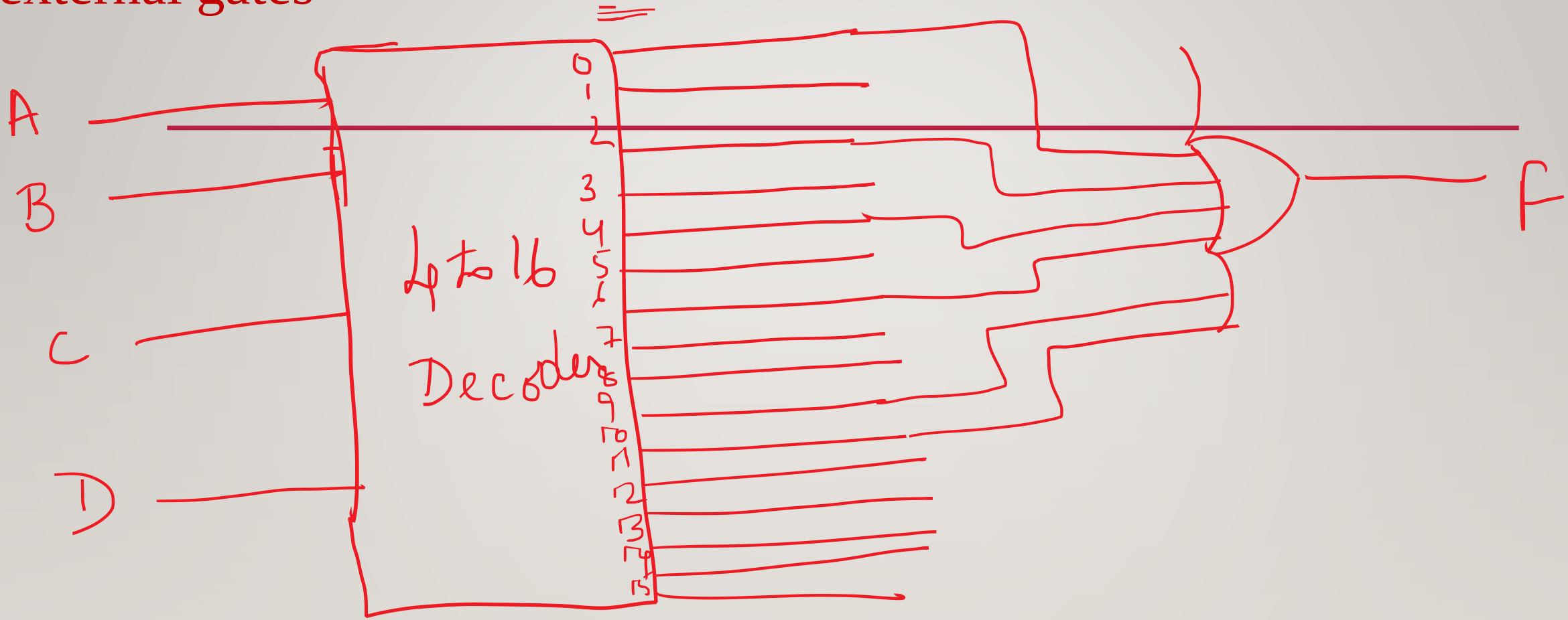
Design 4-to-16 decoder using minimum of 74138 ICs ONLY



Design 5-to-32 decoder with active low output using minimum of 74138 ICs and one external gate ONLY



Implement f(A,B,C,D) = Σm(0,2,4,6,9,10) using suitable decoder and external gates

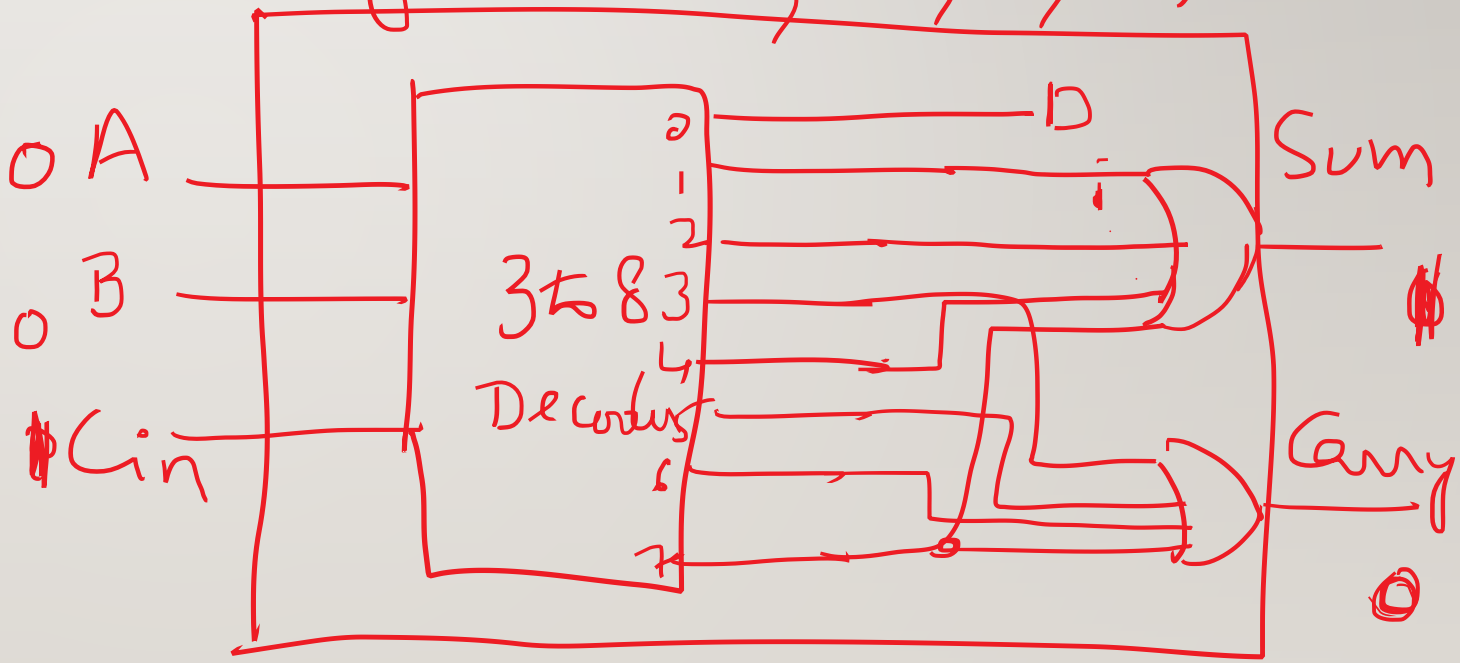


Design a full adder using 3-to-8 line decoder and external gates

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$Sum \equiv \Sigma(1,2,4,7)$$

$$Carry = \Sigma(3,5,6,7)$$

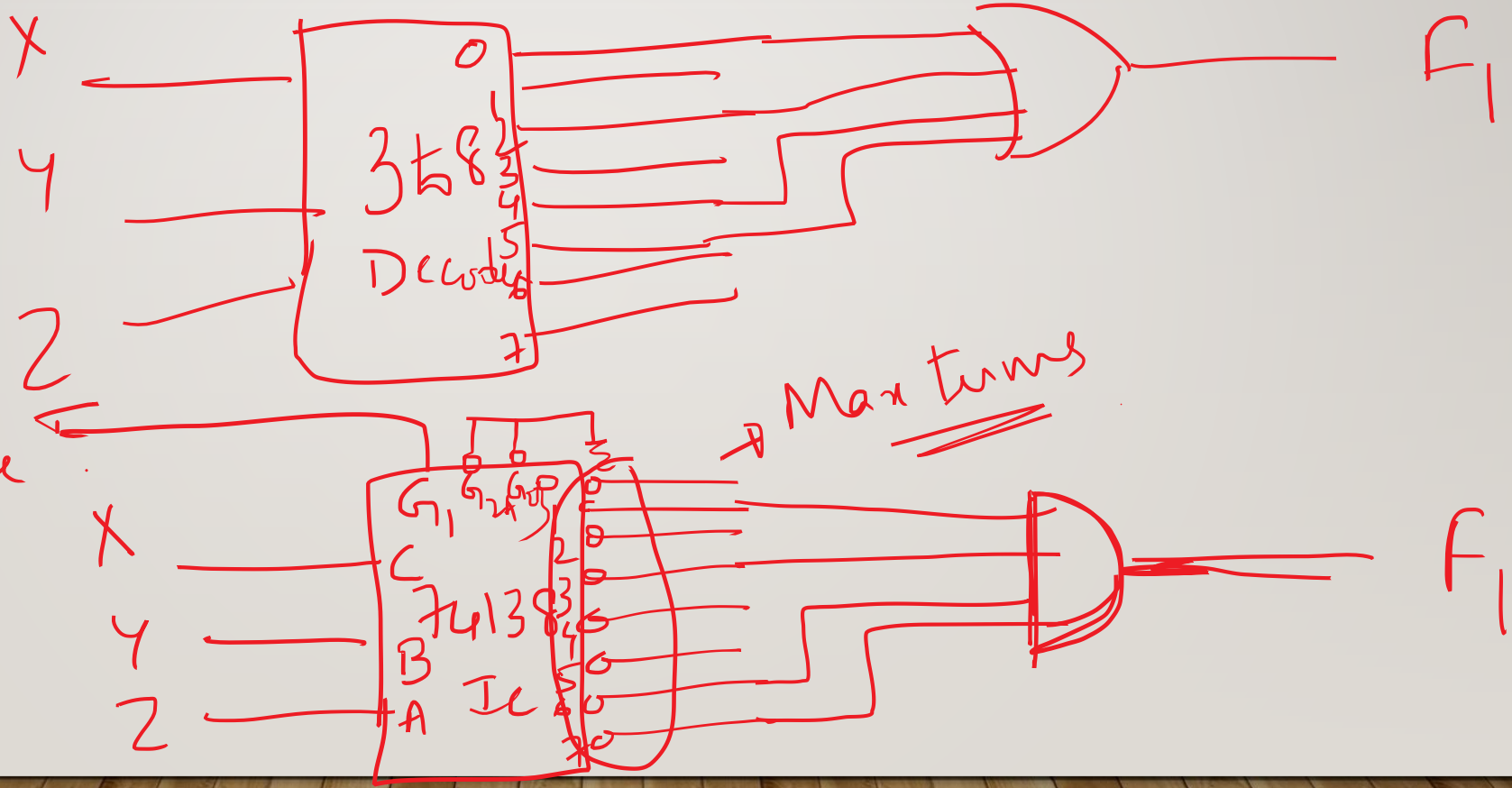


Realize f1(x,y,z) = ΠM(1,3,6,7) using

a. 3-to-8 line decoder with active high output and suitable gates

b. 74138 decoder and suitable gates

$F_1(x,y,z) \equiv \Sigma m(0,2,4,5)$



- Any questions?