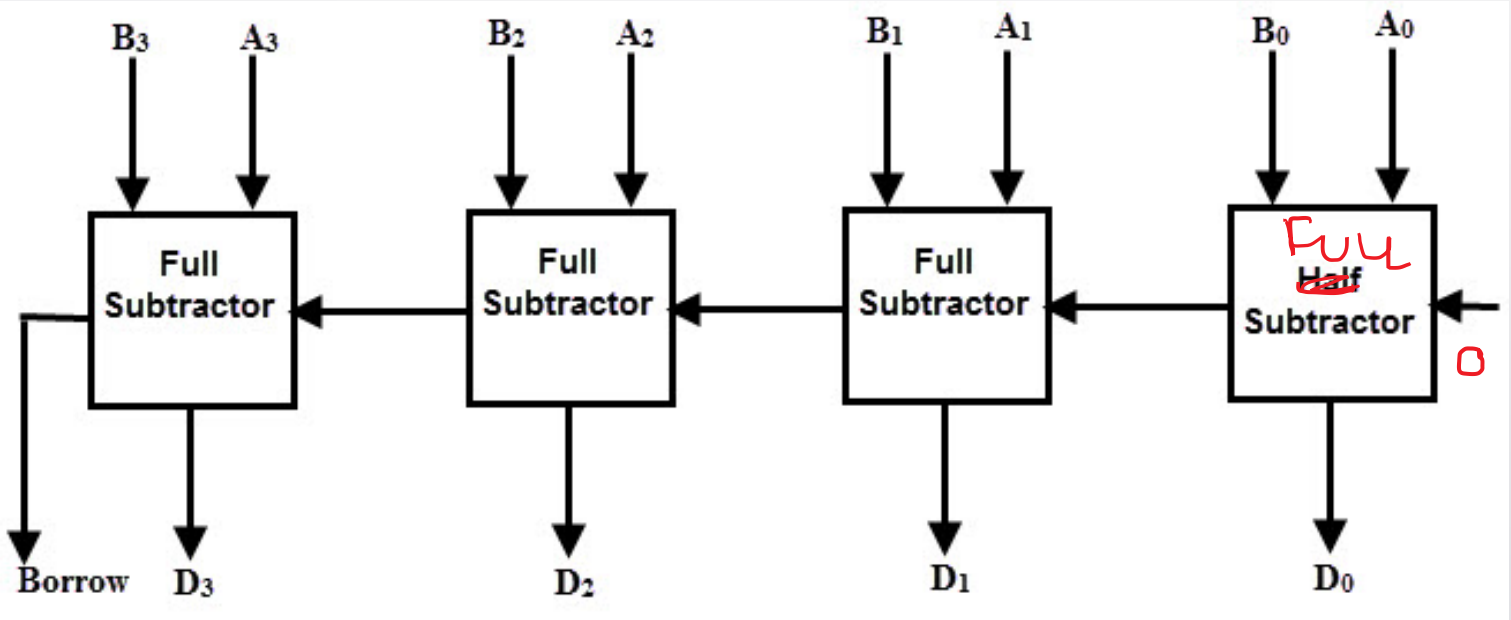
Binary adders and subtractors

- Half adder, full adder, parallel adder
- Half subtractor , full subtractor, parallel subtractor
- Subtraction using complements, parallel adder/subtractor
- Carry Look ahead adder, Decimal adder

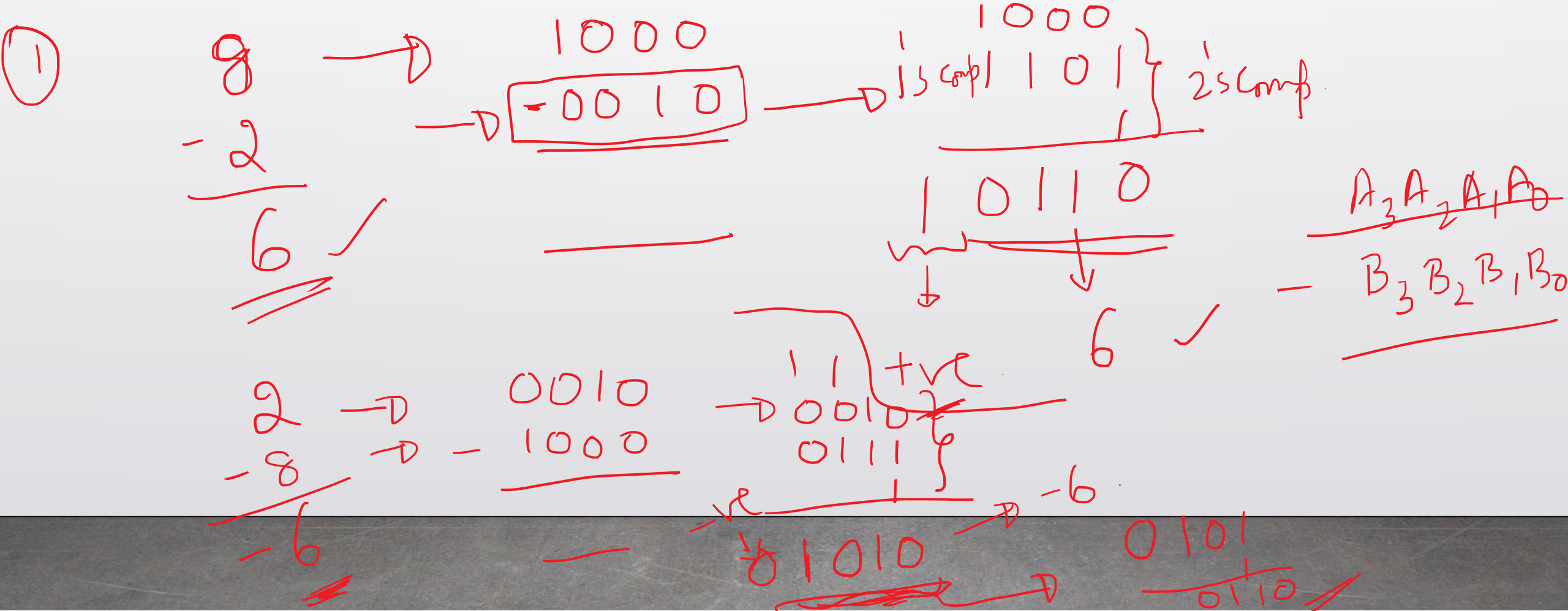
4-bit parallel subtractor using FS blocks

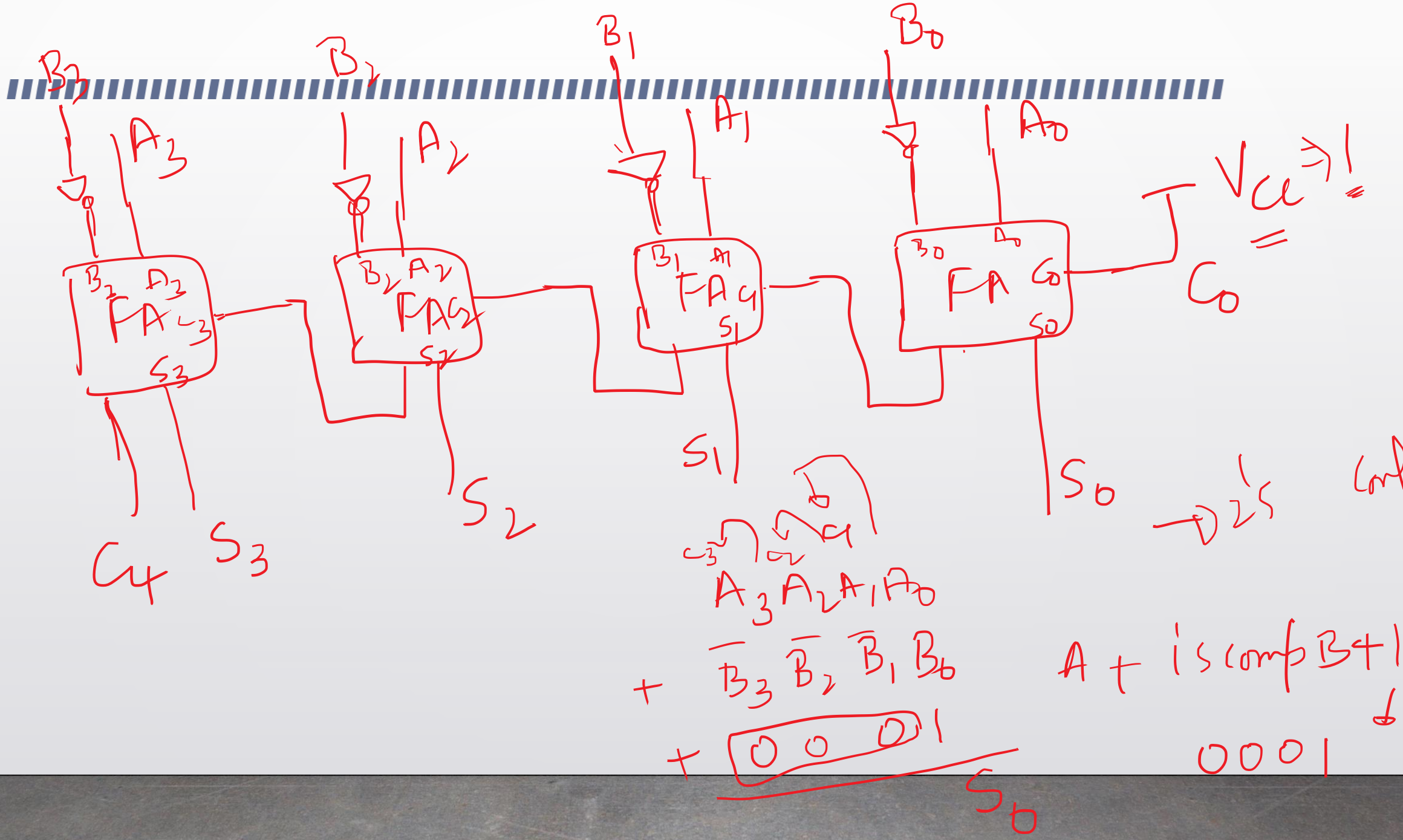
Consider subtraction of 2, 4-bit numbers: (A3 A2 A1 A0) and (B3 B2 B1 B0)



Subtraction using complements

- Using 2's complement method
- Using 1's complement method




B3
B2
B1
B0
A3
A2
A1
A0
FA3
FA2
FA1
FA0
C4
S3
S2
S1
S0
Vcc ⇒ 1
C0
A3A2A1A0
+ B̄3B̄2B̄1B̄0
+ 0 0 0 1
S0
A + iscomp B+1
0001

Decimal number :- 10's comp.

8 → 8

− 4 + 6

4 14

+ve

9's comp of 4 → 9 − 4 = 5

10's comp 5 + 1 = 6

4 → 4

− 8 + 2

−4 06

-ve

10's comp of 4 → 9 − 6 = 3 + 1 = 4

9's comp of 8 → 9 − 8 = 1

10's comp → 1 + 1 = 2

1's complement method :

8 → 1000

−2 → 0010

6 → 0110

1000 → A

+ 1101 → B

1 0101 → S = Sum

1

0110 → +ve

Draw the circuit

2 → 0010

−8 → −1000

−6

0010

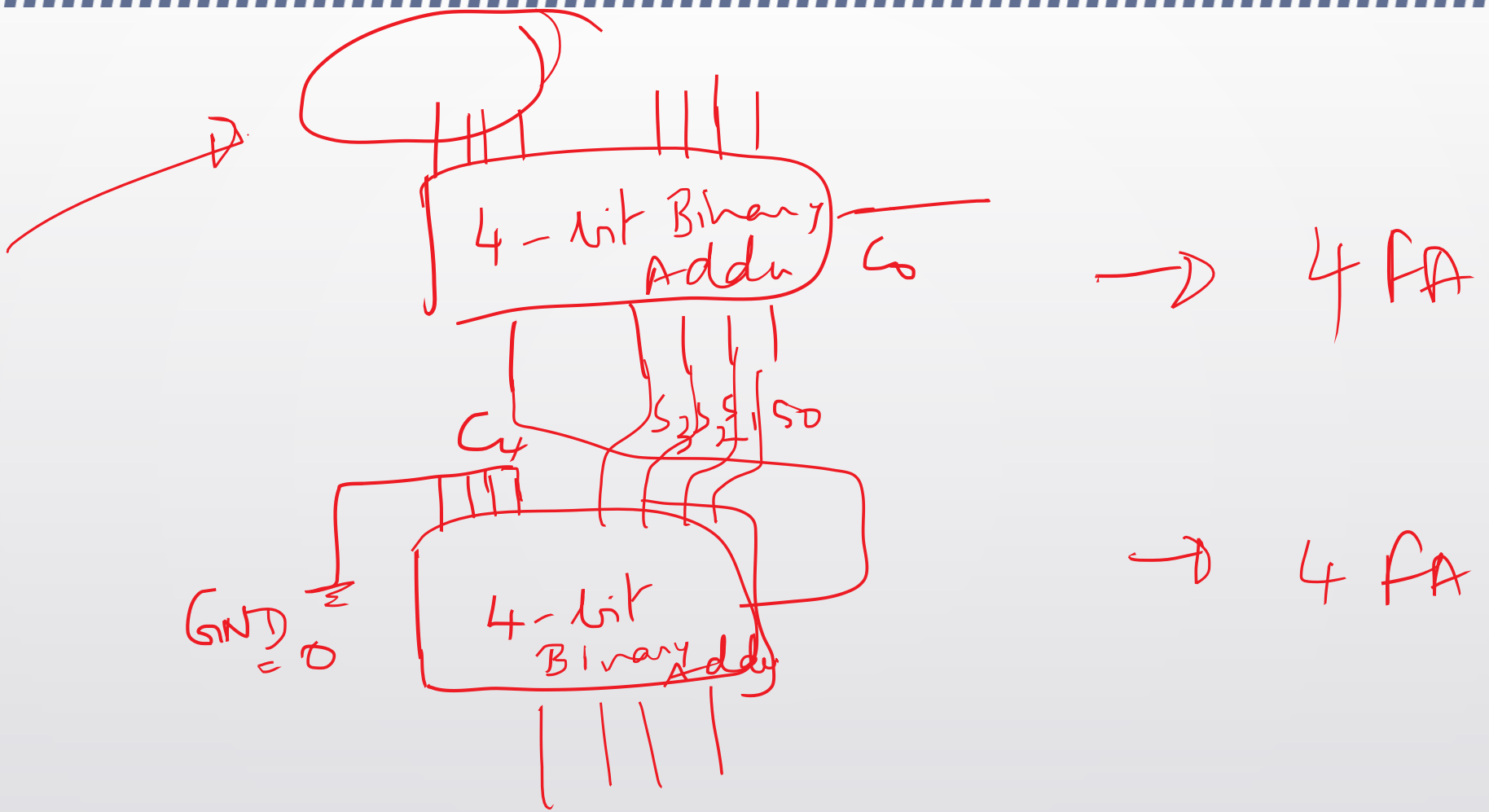
0111

0 1001 → −6

−ve

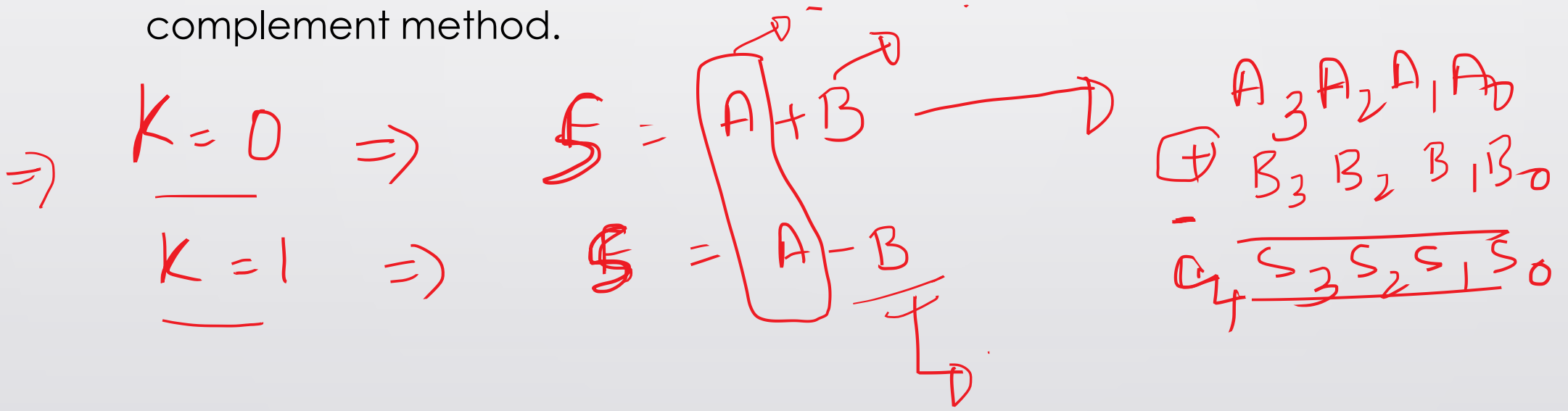
is comp.

0110 → 6

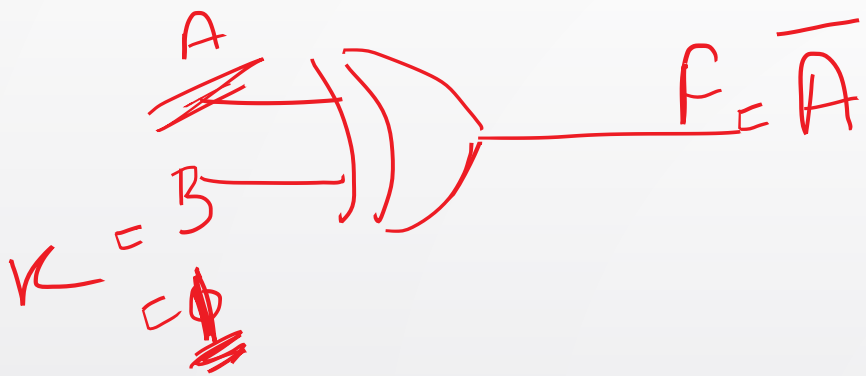

4-bit Binary Addr
C_0
S_3 S_2 S_1 S_0
C_4
GND = 0
4-bit Binary Addr
→ 4 FA
→ 4 FA

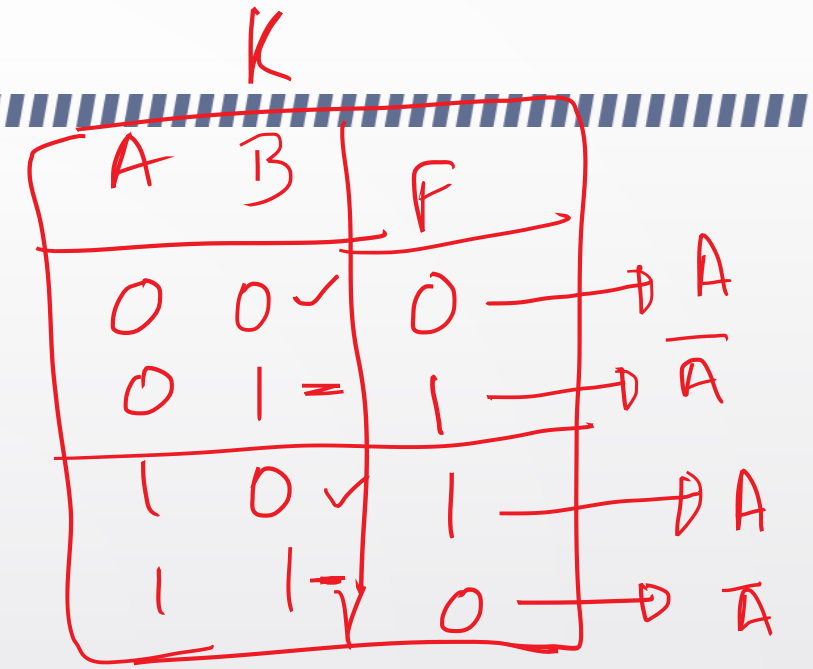
4-bit parallel adder/subtractor :

- Design a 4-bit adder/ subtractor using FA blocks or 7483 IC and minimum external gates, i.e. if the control input bit K=0, the circuit should add the input numbers or if K=1, the circuit should subtract the two numbers using 2's complement method.
- Note: Unless and otherwise mentioned assume subtraction to be using 2's complement method.

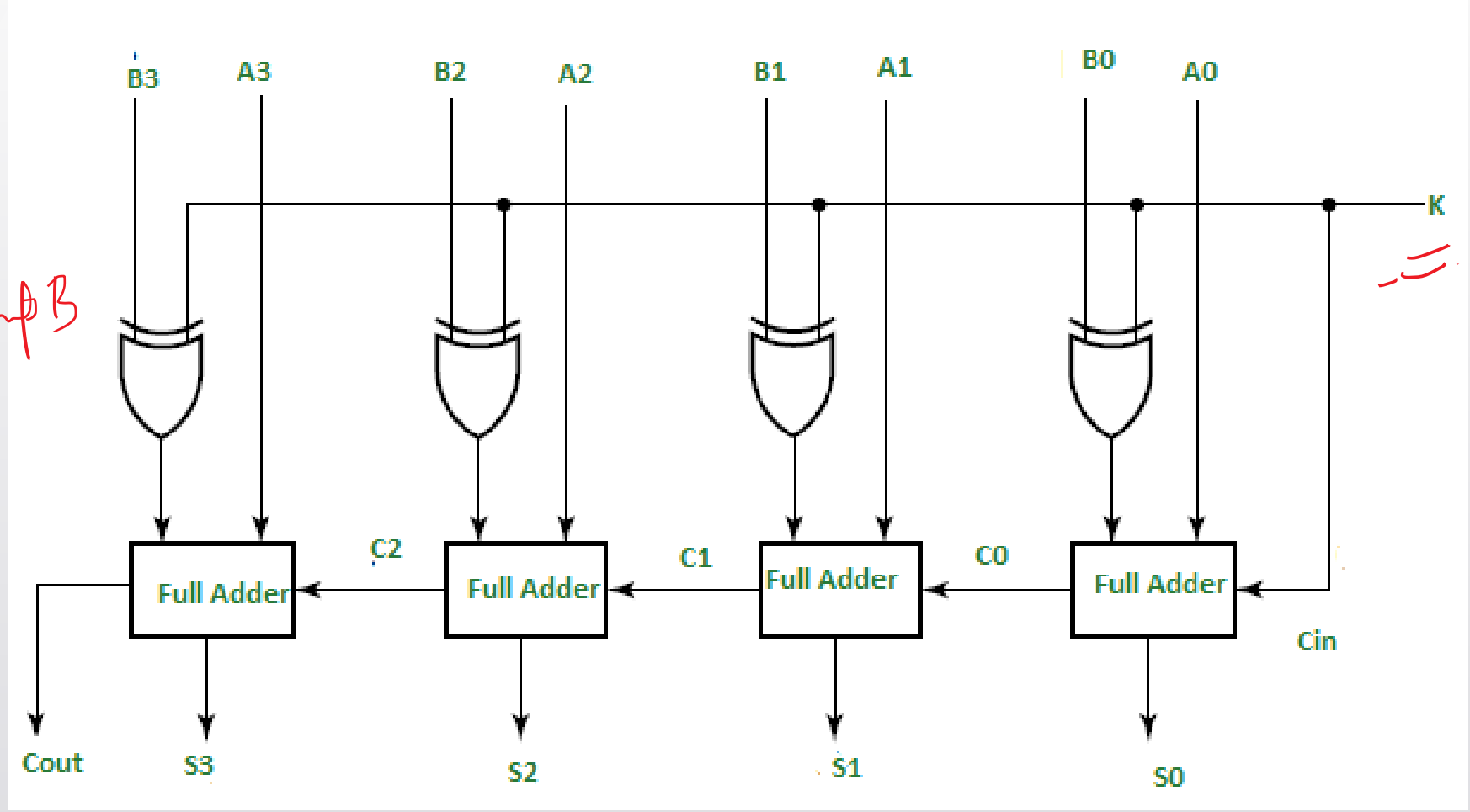


4-bit parallel adder/subtractor :



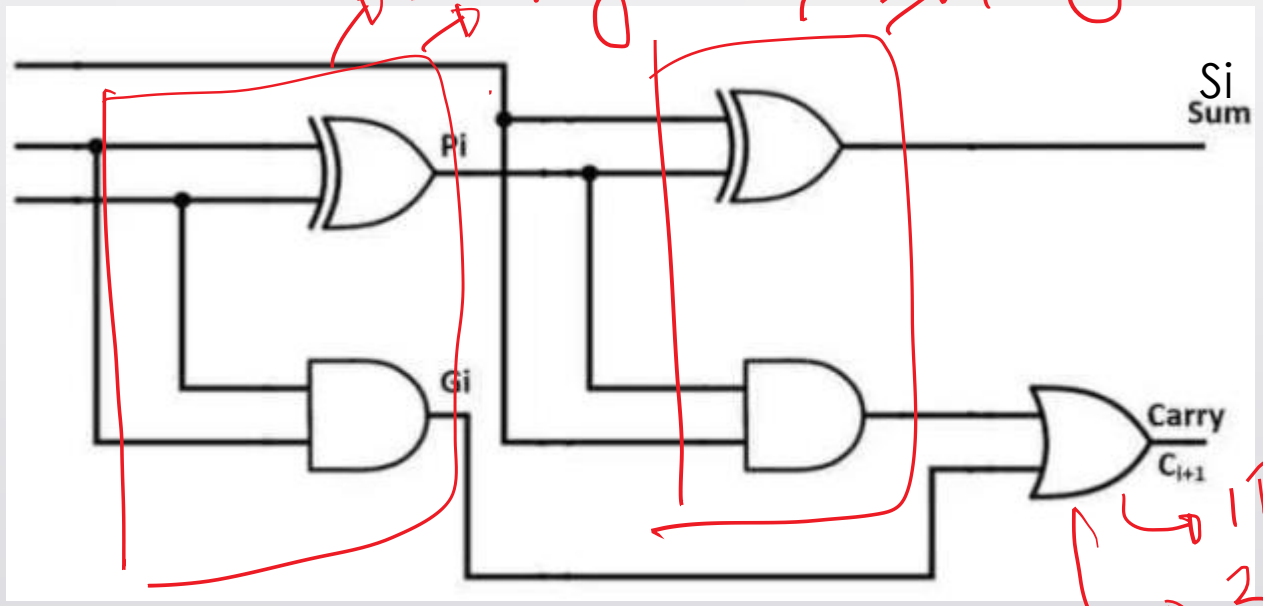


4-bit parallel adder/subtractor :



Carry Look Ahead (CLA) Adder [Parallel Adder]

- Propogation delay in Full Adder is $3T_g$ with respect to following circuit, where Tg is the propagation delay of a gate. All the gates are assumed to have a propagation delay of Tg.
- Pi is the carry propagate term and Gi is the carry generate term



$P_i = A_i \oplus B_i$ Carry Propagate

$G_i = A_i . B_i$ Carry Generate

$S_i = A_i \oplus B_i \oplus C_i$

$C_{i+1} = A_i B_i + (A_i \oplus B_i) C_i$

$= G_i + P_i C_i$

1st Tg, 2nd 1Tg, 1Tg

$= 3T_g$

CLA continued

$C_{i+1} = G_i + P_i C_i$

- Carry generation in CLA from A_i, B_i, and C_0
- Co= input carry

C1 = $G_0 + P_0 C_0 = A_0 B_0 + (A_0 \oplus B_0) C_0$

C2= $G_1 + P_1 C_1 = G_1 + P_1 [G_0 + P_0 C_0]$

$= G_1 + P_1 G_0 + P_1 P_0 C_0$

C3=

$G_2 + P_2 C_2 = G_2 + P_2 [G_1 + P_1 G_0 + P_1 P_0 C_0]$

$= G_2 + G_1 P_2 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$

CLA Continued

4- bit CLA

- Expressions for sum

S0 = $A_0 \oplus B_0 \oplus C_0$

S1= $A_1 \oplus B_1 \oplus C_1$

S2 = $A_2 \oplus B_2 \oplus C_2$

S3 = $A_3 \oplus B_3 \oplus C_3$

C4 = $G_3 + P_3 C_3$

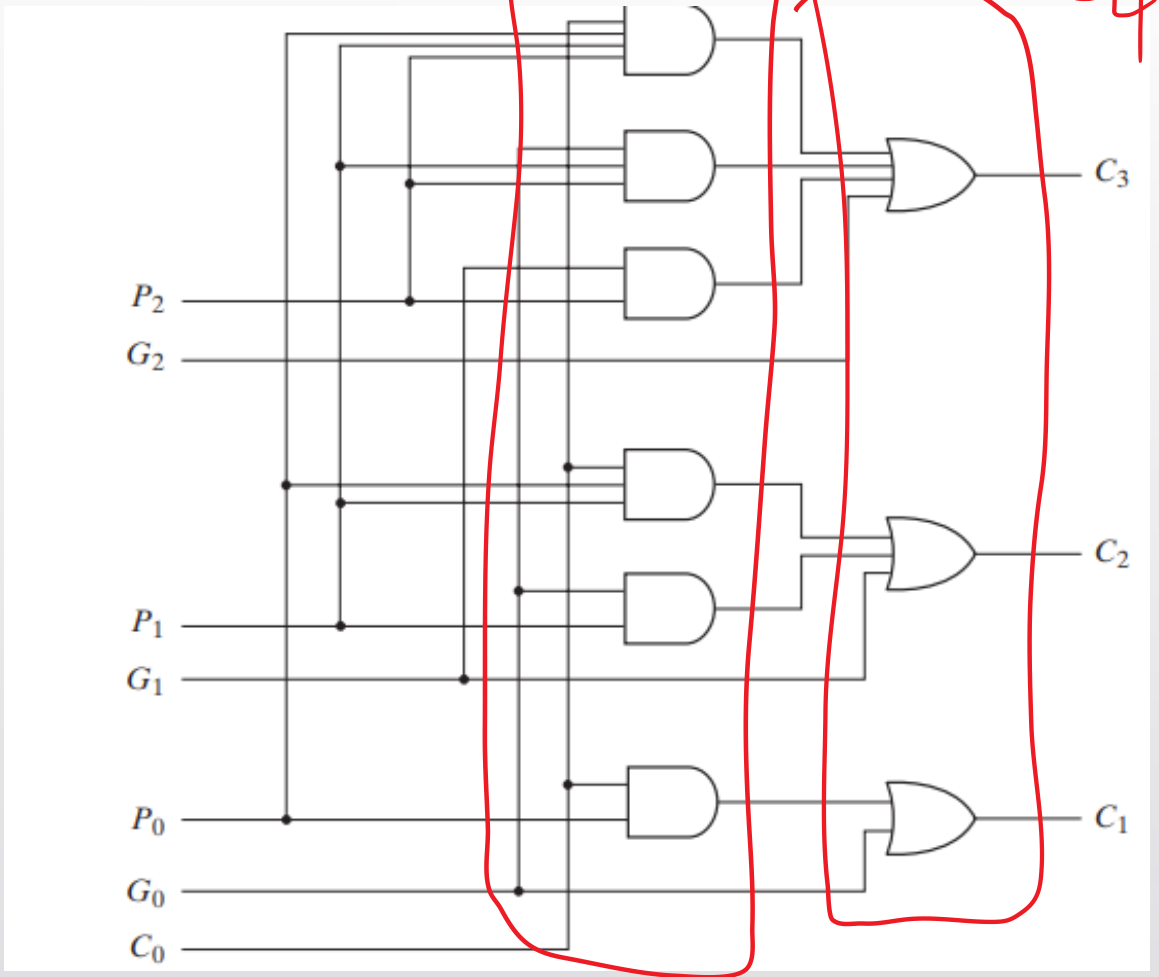
$= G_3 + P_3 [G_2 + G_1 P_2 + G_0 P_1 P_2 + C_0 P_0 P_1 P_2]$

$= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$

CLA: Carry look ahead generator circuit

- Draw the combinational circuit to generate C1, C2 and C3 from Pi , Gi and C0 terms.

CLA: Carry look ahead generator circuit

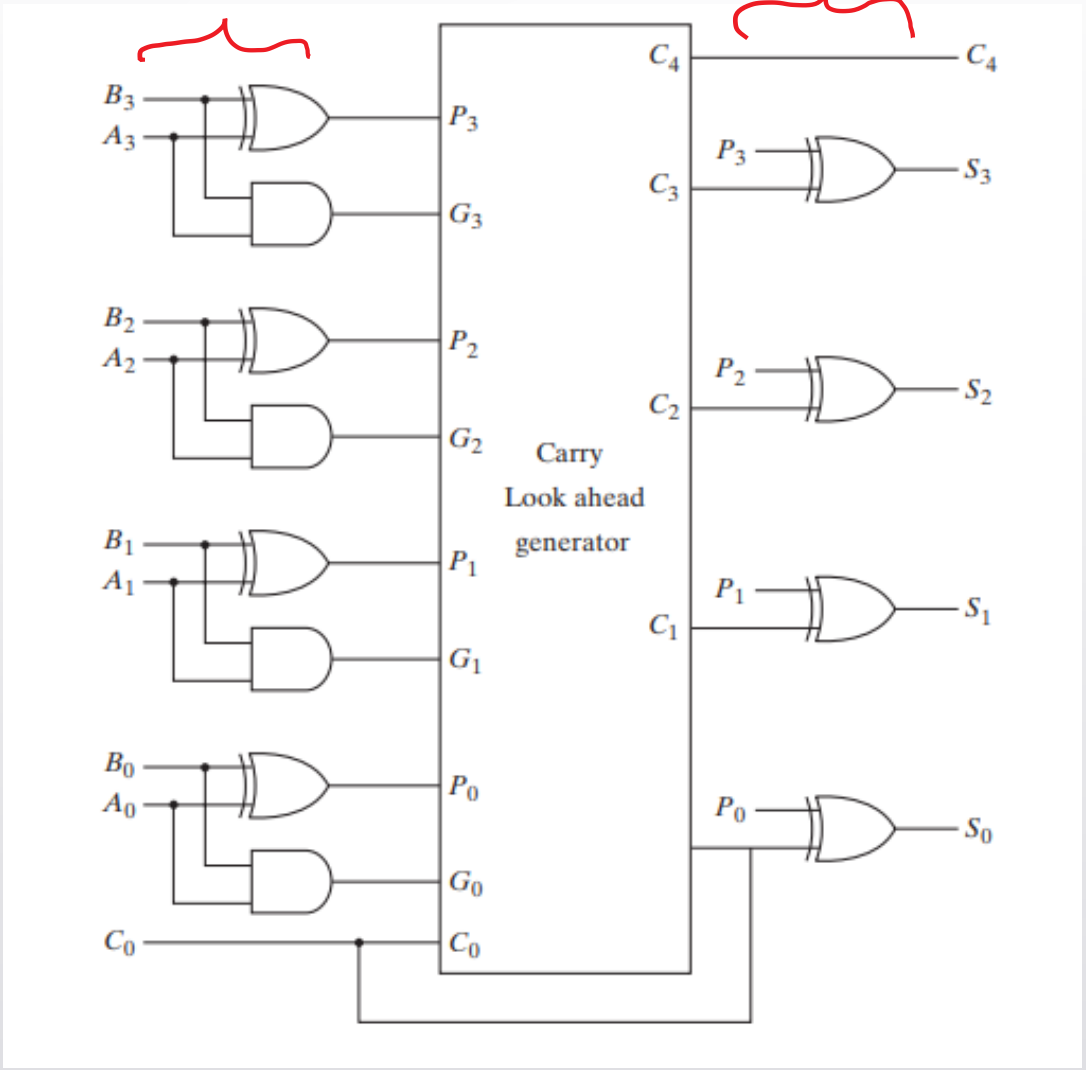


C_4 → Carry generator.

Time required to generate C1,C2,C3 in terms of Tg?

$= 2T_g$

4-bit CLA



Time required to generate S1,S2,S3,C4 in terms of Tg?

Comparison

- CLA or CPA…which is better?

4-bit Adder:

CLA ⇒ 4TG

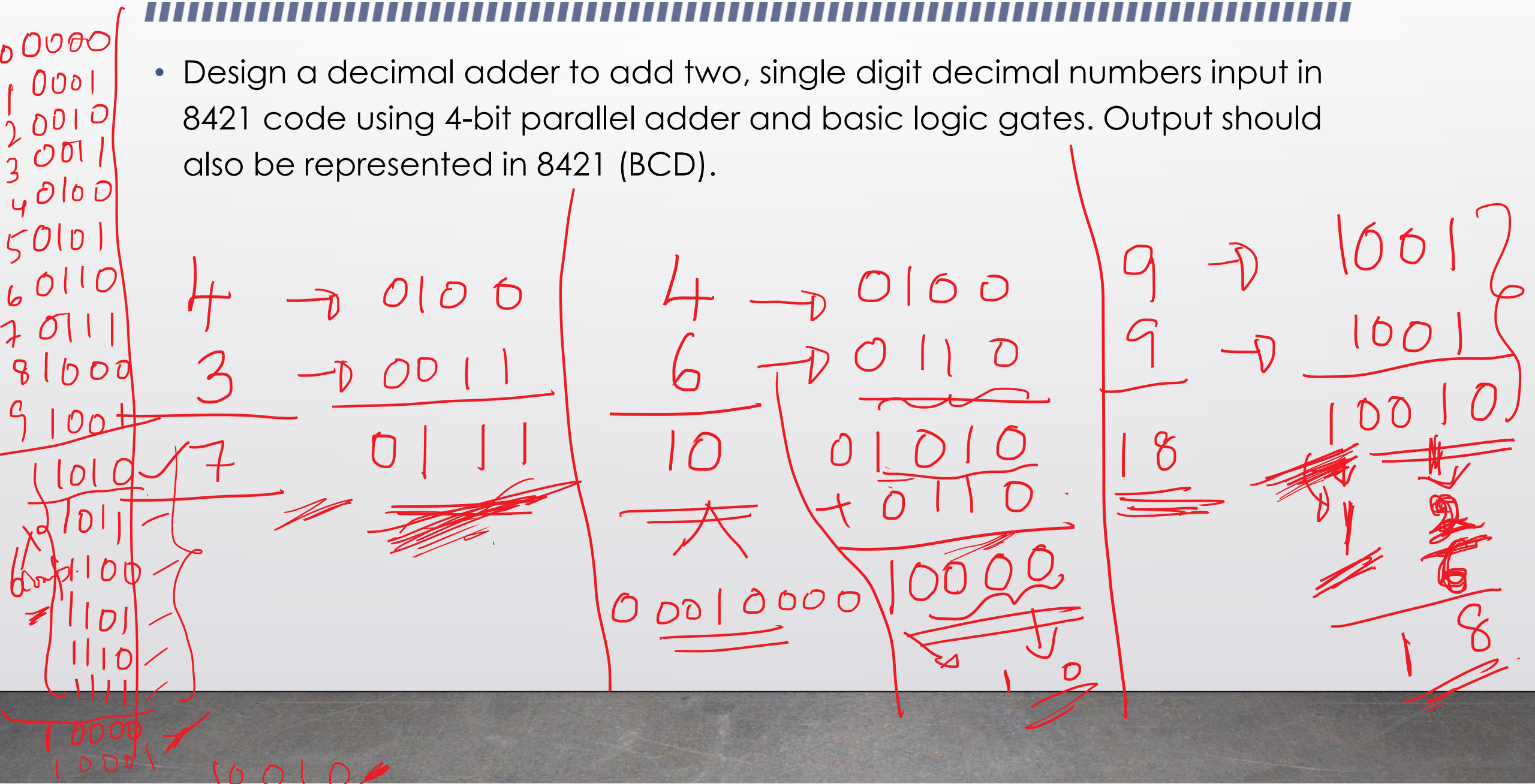
CPA ⇒ 12TG

4-bit CLA is 3 times faster than 4-bit CPA

Decimal adder: Used to add decimal numbers represented in binary coded form

Decimal adder:

- Design a decimal adder to add two, single digit decimal numbers input in 8421 code using 4-bit parallel adder and basic logic gates. Output should also be represented in 8421 (BCD).



Questions?