



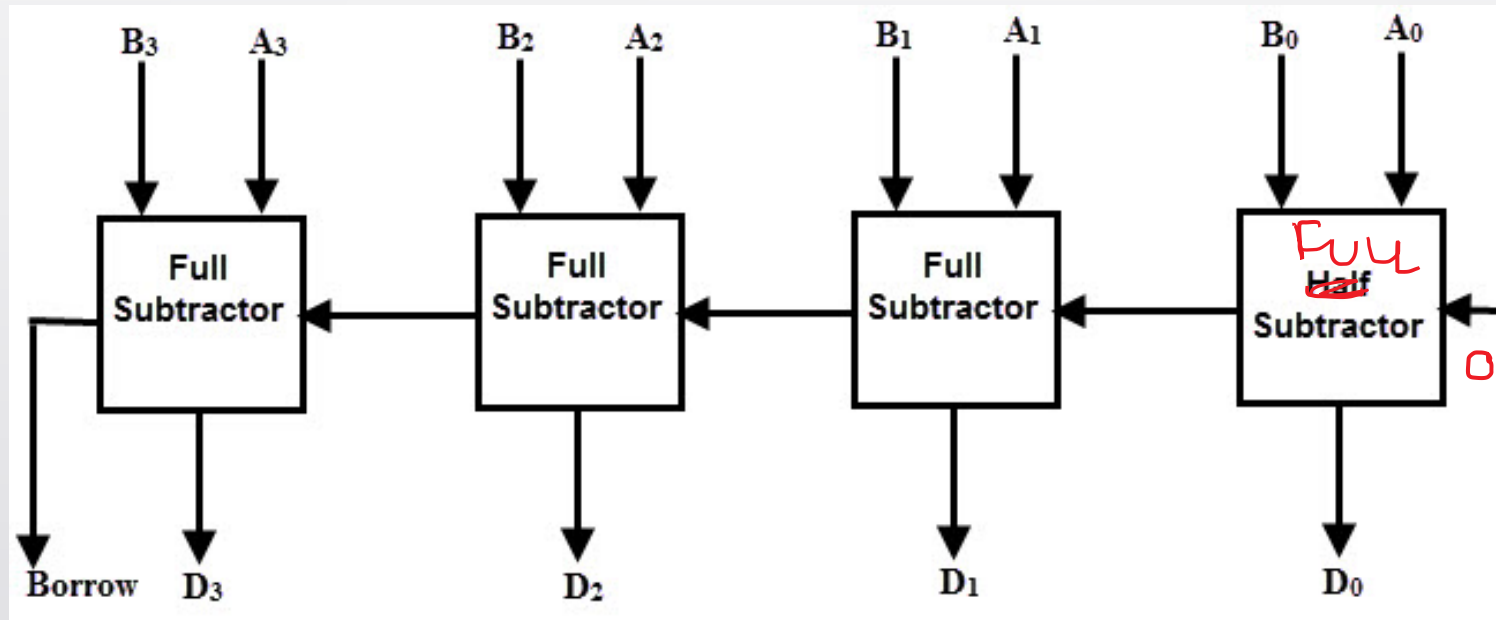
Binary adders and subtractors

- Half adder, full adder, parallel adder
- Half subtractor , full subtractor, parallel subtractor
- Subtraction using complements, parallel adder/subtractor
- Carry Look ahead adder, Decimal adder

4-bit parallel subtractor using FS blocks



Consider subtraction of 2, 4-bit numbers: $(A_3 A_2 A_1 A_0)$ and $(B_3 B_2 B_1 B_0)$



Subtraction using complements

☐ Using 2's complement method ✓

☐ Using 1's complement method

①

$$\begin{array}{r} 8 \\ - 2 \\ \hline 6 \end{array}$$

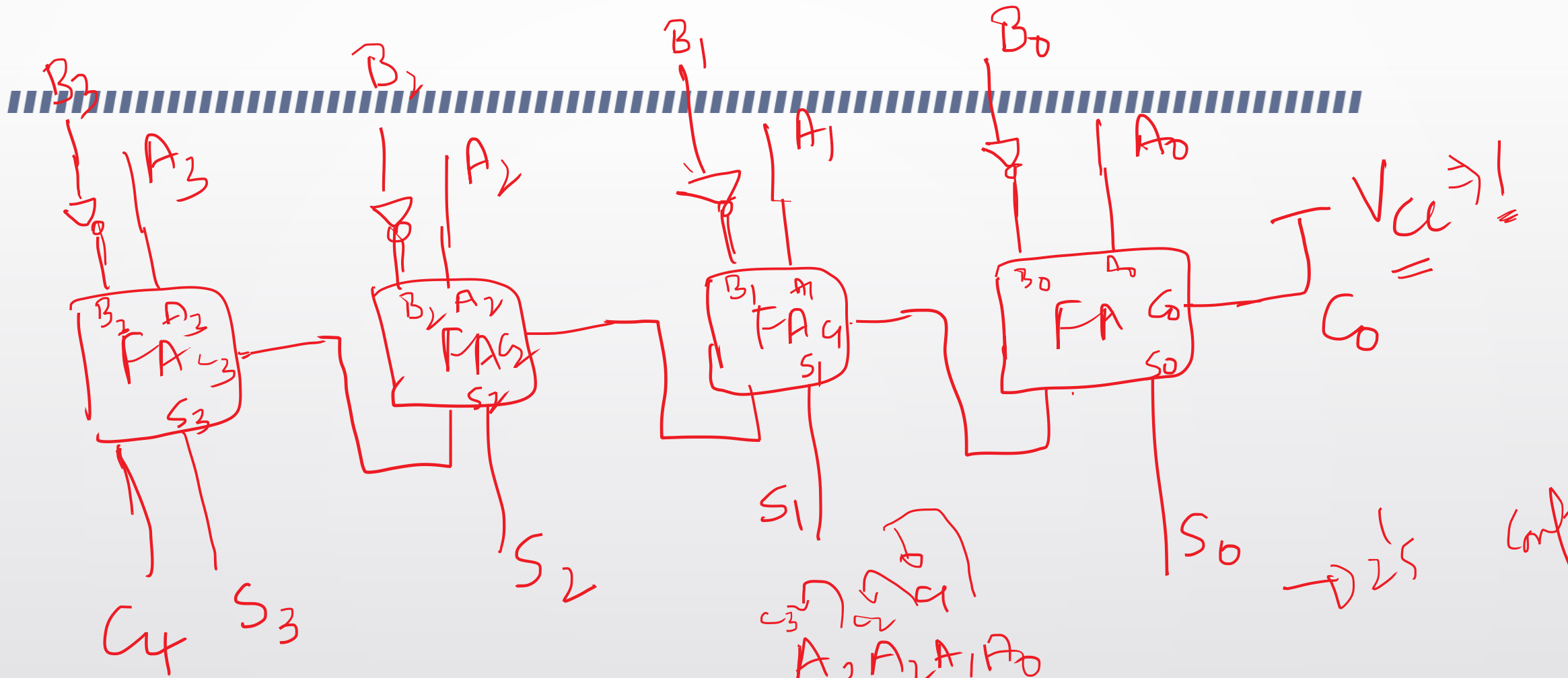
→ 1000
→ -0010 → 1's comp 1000
→ 1000 } 2's comp
→ 10110
→ 6 ✓

$$\begin{array}{r} A_3 A_2 A_1 A_0 \\ - B_3 B_2 B_1 B_0 \\ \hline \end{array}$$

$$\begin{array}{r} 2 \\ - 8 \\ \hline -6 \end{array}$$

→ 0010
→ 1000
→ 0010 } +ve
→ 0111 }
→ 01010 → -6

$$\begin{array}{r} 0101 \\ - 0110 \\ \hline \end{array}$$



$$\begin{aligned}
 & A_3 A_2 A_1 A_0 \\
 & + \bar{B}_3 \bar{B}_2 \bar{B}_1 B_0 \\
 & + \boxed{0001} \\
 & \hline
 & S_0
 \end{aligned}$$

$A + 1$ is comp $B + 1$
 0001

Decimal number - 10's comp.

$$\begin{array}{r} 8 \rightarrow \\ - 4 \\ \hline 4 \end{array}$$

$$\begin{array}{r} 8 \\ + 6 \\ \hline 14 \\ \hline \end{array}$$

+ve

9's comp of 4 \rightarrow

$$\begin{array}{r} 9 \\ - 4 \\ \hline 5 \end{array}$$

10's comp \rightarrow

$$\begin{array}{r} 5 \\ + 1 \\ \hline 6 \end{array}$$

$$\begin{array}{r} 4 \rightarrow \\ - 8 \\ \hline -4 \end{array}$$

$$\begin{array}{r} 4 \\ + 2 \\ \hline 06 \\ \hline \end{array}$$

-ve

10's comp of 4 \rightarrow

$$\begin{array}{r} 9 \\ - 6 \\ \hline 3 + 1 = 4 \end{array}$$

9's comp of 8 \rightarrow

$$\begin{array}{r} 9 \\ - 8 \\ \hline 1 \end{array}$$

10's comp \rightarrow

$$\begin{array}{r} 1 \\ + 1 \\ \hline 2 \end{array}$$

's complement method :-

$$\begin{array}{r}
 8 \rightarrow 1000 \\
 -2 \rightarrow 0010 \\
 \hline
 6 \rightarrow 0110
 \end{array}$$

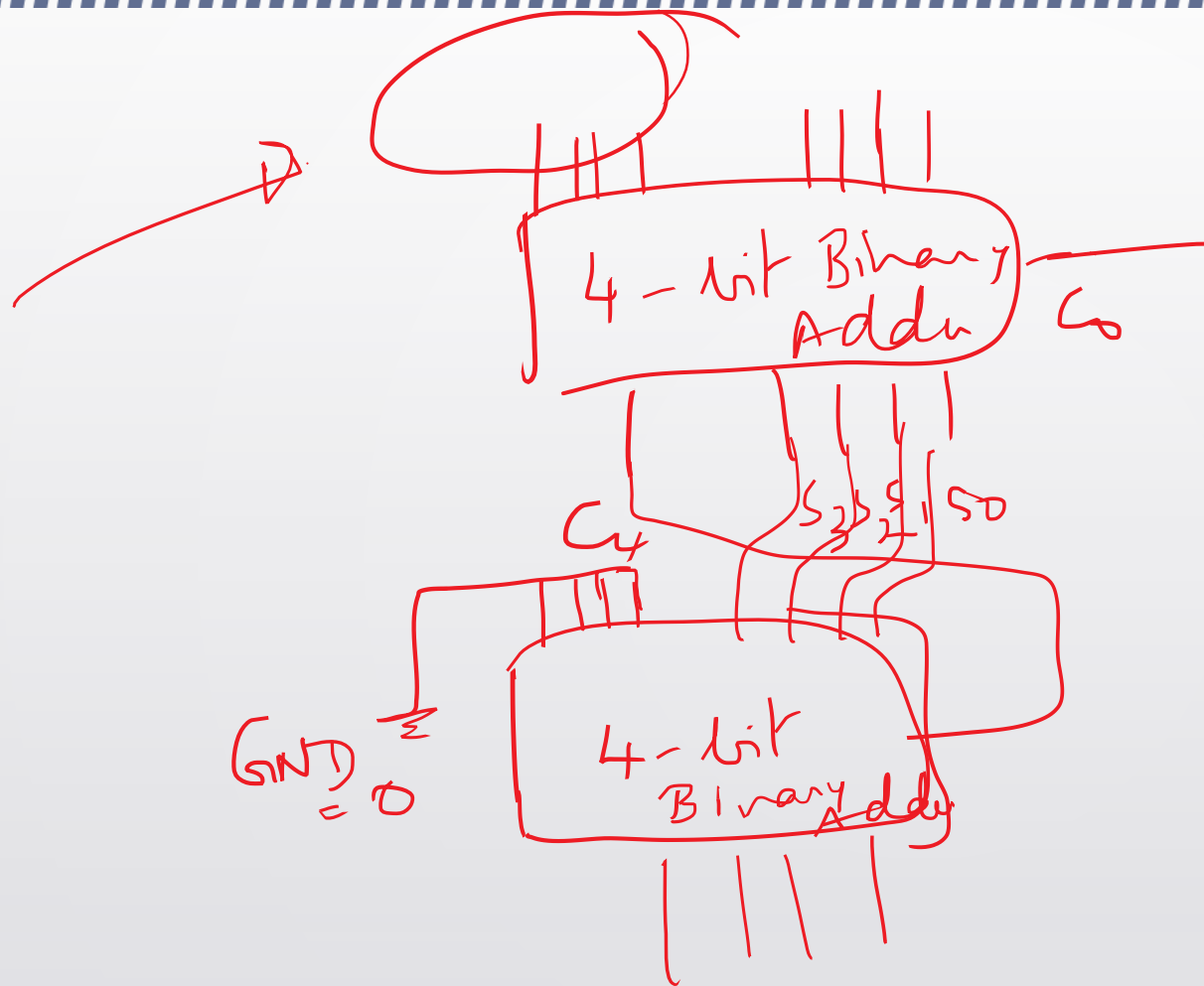
$$\begin{array}{r}
 1000 \rightarrow A \\
 + 1101 \rightarrow B \\
 \hline
 10101 \rightarrow S_0 S_1 S_2 S_3 \\
 \hline
 1 \rightarrow 1 \\
 \hline
 +ve \quad 0110 \rightarrow
 \end{array}$$

Draw the circuit

$$\begin{array}{r}
 2 \rightarrow 0010 \\
 -8 \rightarrow -1000 \\
 \hline
 -6
 \end{array}$$

$$\begin{array}{r}
 0010 \\
 0111 \\
 \hline
 01001 \rightarrow -6 \\
 \hline
 -ve \quad 0110 \rightarrow 6
 \end{array}$$

is comp.

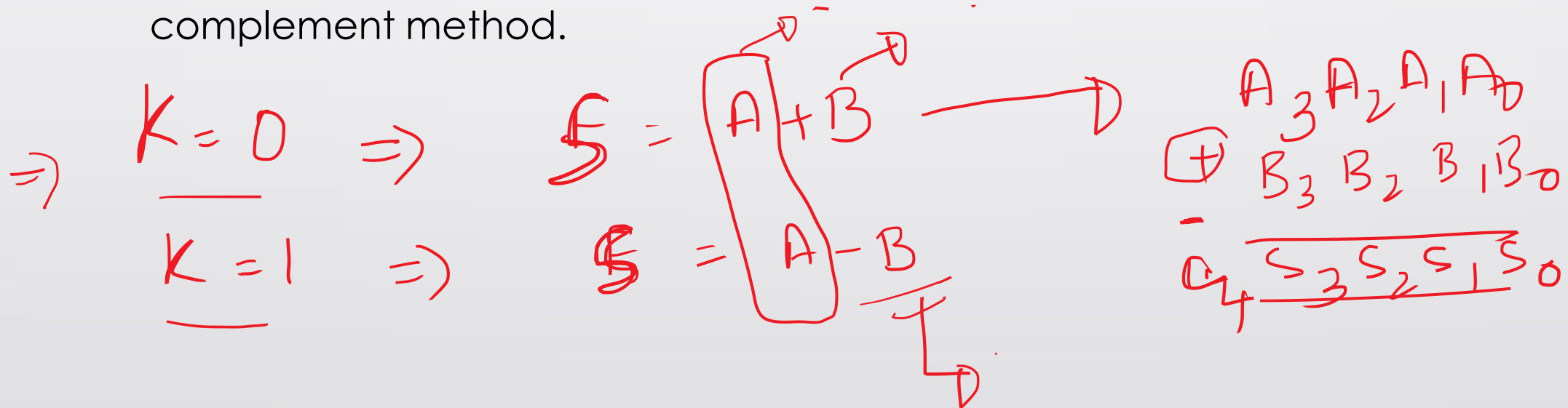


→ 4 FA

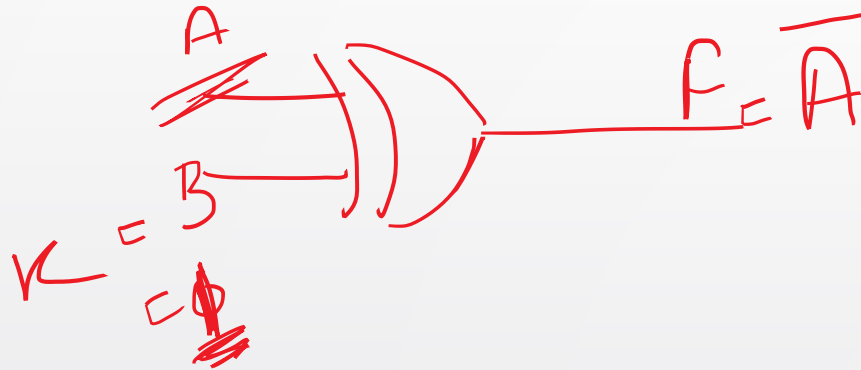
→ 4 FA

4-bit parallel adder/subtractor :

- Design a 4-bit adder/ subtractor using FA blocks or 7483 IC and minimum external gates, i.e. if the control input bit $K=0$, the circuit should add the input numbers or if $K=1$, the circuit should subtract the two numbers using 2's complement method.
- Note: Unless and otherwise mentioned assume subtraction to be using 2's complement method.



4-bit parallel adder/subtractor :

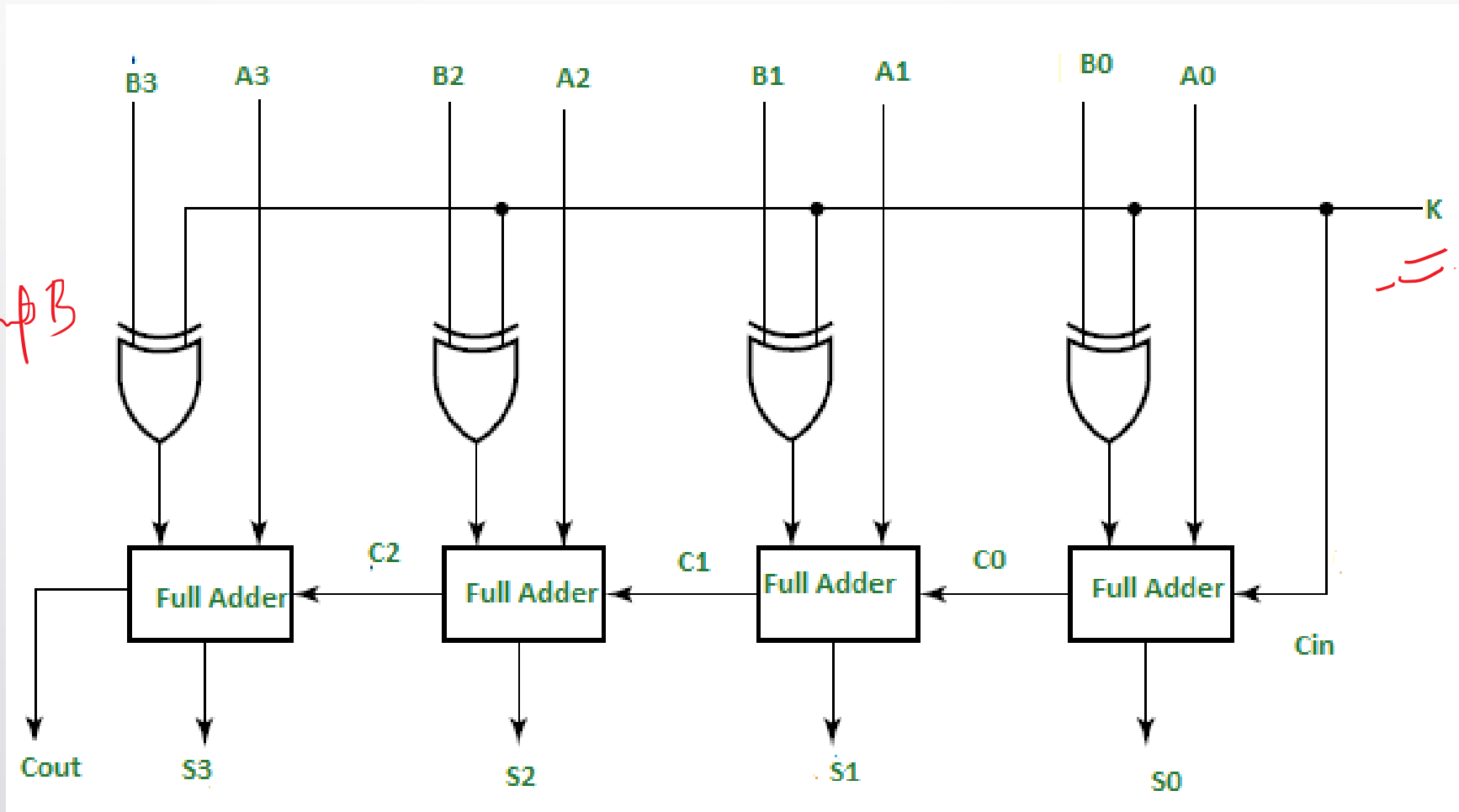


K			
A	B	F	
0	0 ✓	0	→ A
0	1 =	1	→ \overline{A}
1	0 ✓	1	→ A
1	1 ✓	0	→ \overline{A}

4-bit parallel adder/subtractor :



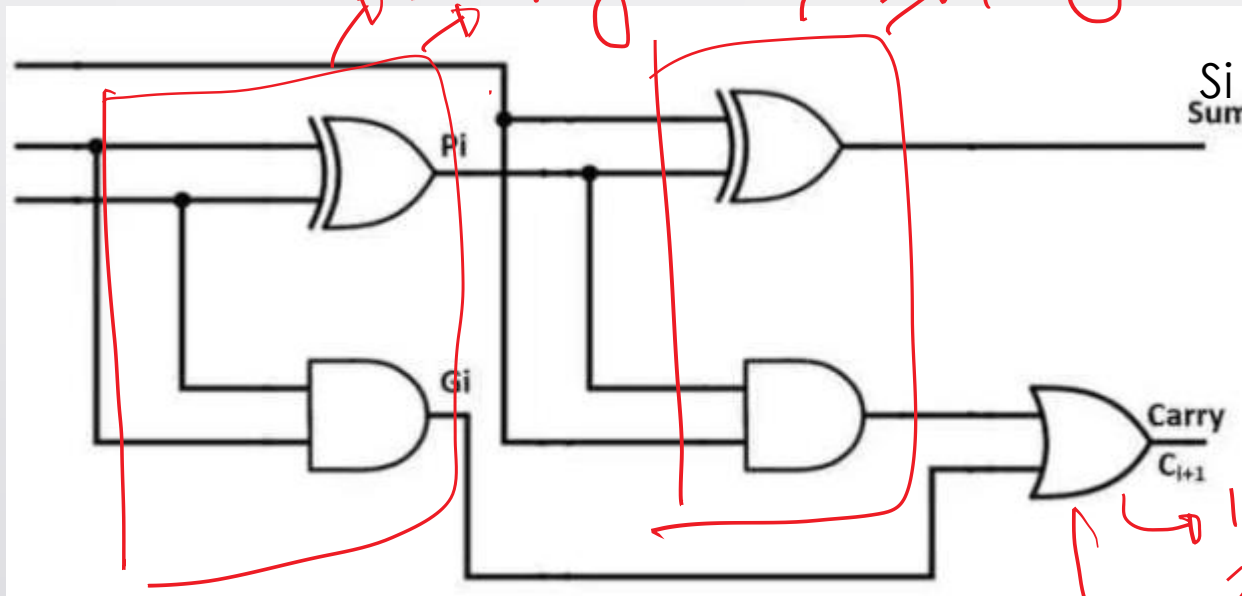
$K \Rightarrow A + B + 0$
 $K \Rightarrow A + \text{comp } B + 1$



Carry Look Ahead (CLA) Adder [Parallel Adder]

- Propagation delay in Full Adder is $3T_g$ with respect to following circuit, where T_g is the propagation delay of a gate. All the gates are assumed to have a propagation delay of T_g .
- P_i is the carry propagate term and G_i is the carry generate term

C_i
 A_i
 B_i



$$P_i = A_i \oplus B_i$$

Carry Propagate

$$G_i = A_i \cdot B_i$$

Carry Generate

$$S_i = A_i \oplus B_i \oplus C_i$$

$$C_{i+1} = A_i B_i + (A_i \oplus B_i) C_i$$

$$= G_i + P_i C_i$$

$$= 3T_g$$

CLA continued

$$C_{i+1} = G_i + P_i C_i$$

- Carry generation in CLA from A_i , B_i , and C_0
- C_0 = input carry

$$C_1 = G_0 + P_0 C_0 = A_0 B_0 + (A_0 \oplus B_0) C_0$$

$$\begin{aligned} C_2 &= G_1 + P_1 C_1 = G_1 + P_1 [G_0 + P_0 C_0] \\ &= G_1 + \underline{P_1 G_0} + \underline{P_1 P_0 C_0} \end{aligned}$$

$$\begin{aligned} C_3 &= G_2 + P_2 C_2 = G_2 + P_2 [G_1 + P_1 G_0 + P_1 P_0 C_0] \\ &= G_2 + \underline{G_1 P_2} + \underline{P_2 P_1 G_0} + \underline{P_2 P_1 P_0 C_0} \end{aligned}$$

CLA Continued

4-bit CLA

- Expressions for sum

$$S_0 = A_0 \oplus B_0 \oplus C_0$$

$$S_1 = A_1 \oplus B_1 \oplus C_1$$

$$S_2 = A_2 \oplus B_2 \oplus C_2$$

$$S_3 = A_3 \oplus B_3 \oplus C_3$$

$$C_4 = G_3 + P_3 C_3$$

$$= G_3 + P_3 [G_2 + G_1 P_2 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0]$$

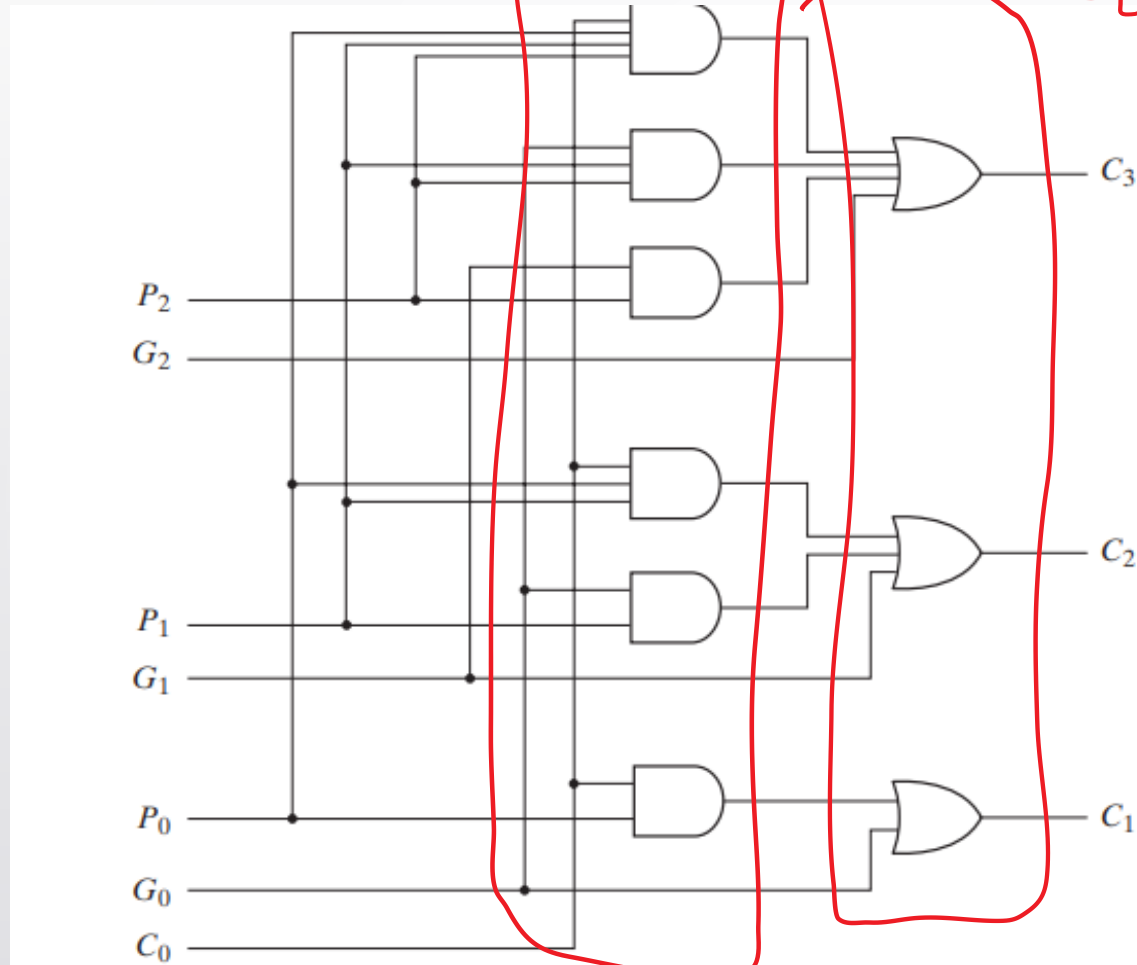
$$= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$$

CLA: Carry look ahead generator circuit



- Draw the combinational circuit to generate C_1 , C_2 and C_3 from P_i , G_i and C_0 terms.

CLA: Carry look ahead generator circuit



$C_4 \rightarrow$ Carry generator.

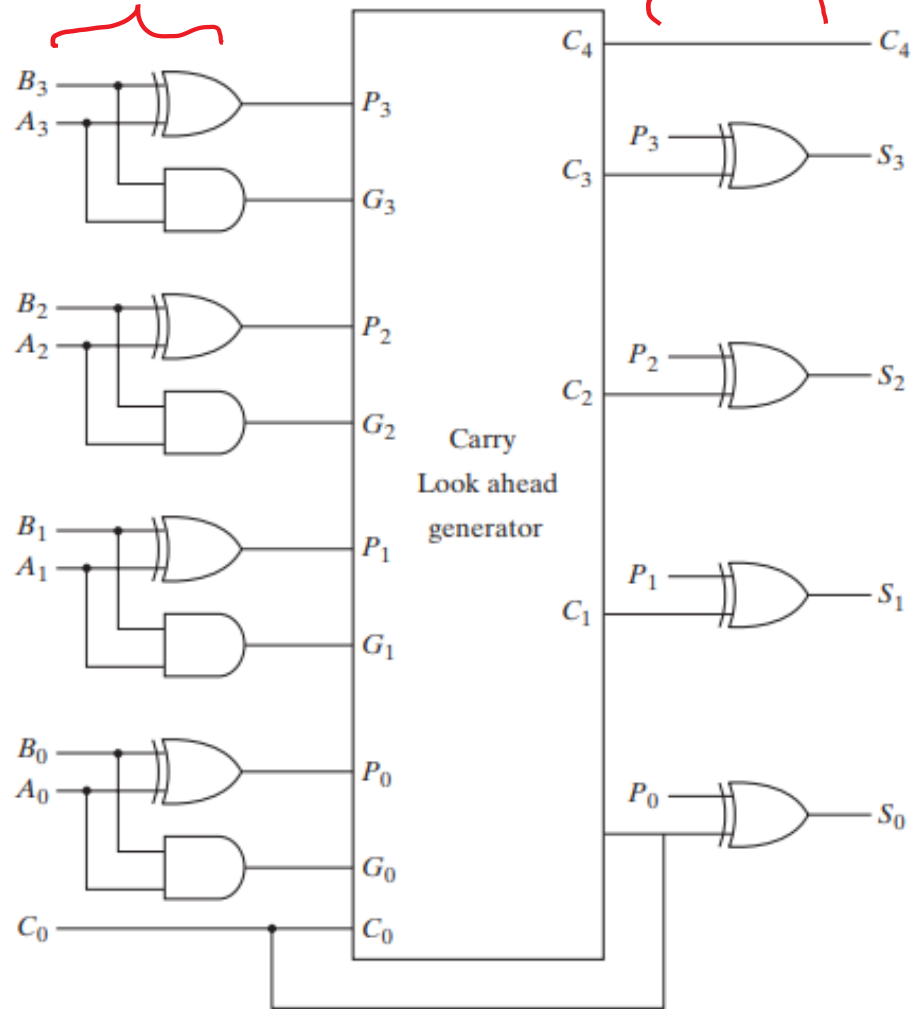
Time required to generate C_1, C_2, C_3
in terms of T_g ?

$\checkmark = \underline{\underline{2T_g}}$

4-bit CLA

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$



Time required to generate
S1,S2,S3,C4 in terms of Tg?

$$S_i = A_i \oplus B_i \oplus C_i$$

$$S_i = P_i \oplus C_i$$

Comparison

- CLA or CPA...which is better?

4-bit Adder :-

CLA \Rightarrow 4 Tg

CPA \Rightarrow 12 Tg

4-bit CLA is 3 times faster than ^{4-bit} CPA



**Decimal adder: Used to add decimal numbers
represented in binary coded form**

Decimal adder:

- Design a decimal adder to add two, single digit decimal numbers input in 8421 code using 4-bit parallel adder and basic logic gates. Output should also be represented in 8421 (BCD).

Handwritten notes and calculations for a decimal adder design:

8421 BCD Table:

Decimal	8421 BCD
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Handwritten Calculations:

Example 1:

$$\begin{array}{r} 4 \rightarrow 0100 \\ 3 \rightarrow 0011 \\ \hline 7 \rightarrow 0111 \end{array}$$

Example 2:

$$\begin{array}{r} 4 \rightarrow 0100 \\ 6 \rightarrow 0110 \\ \hline 10 \rightarrow 01010 \\ + 0110 \\ \hline 00010000 \end{array}$$

Example 3:

$$\begin{array}{r} 9 \rightarrow 1001 \\ 9 \rightarrow 1001 \\ \hline 18 \rightarrow 10010 \end{array}$$

Additional Notes:

- Handwritten numbers: 10000, 10001, 10010.
- Handwritten numbers: 10010, 10011, 10012.



Questions?