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Department of Electronics and Communication Engineering

Complementary Metal-Oxide Semiconductor (CMOS)

Project Title: 8T SRAM CELL Design Using CMOS Technology.

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What is an 8T SRAM CELL?

The 8T SRAM Cell (8-transistor Static Random-Access Memory cell) is an enhanced SRAM architecture developed to improve read stability and reduce power consumption compared to the traditional 6T SRAM cell. While the 6T cell is commonly used in many memory applications, the 8T SRAM cell provides distinct benefits for low-power and high-performance systems, particularly under reduced supply voltages often found in scaled CMOS technologies.

Key Components and Design of an 8T SRAM Cell

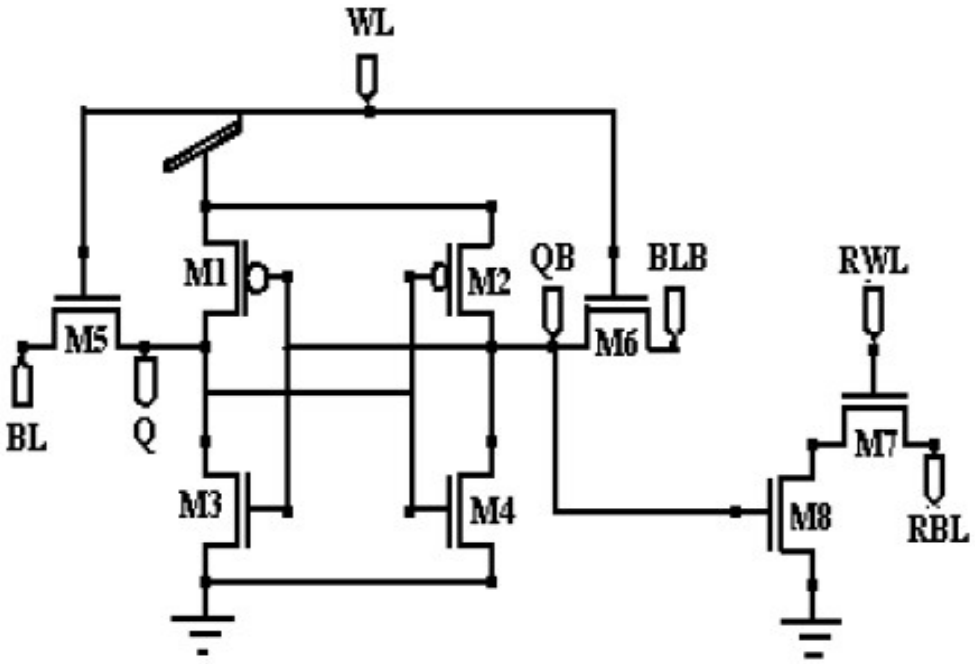
The 8T SRAM cell is based on the conventional cross-coupled inverter pair found in a 6T design, with added transistors to improve read reliability and minimize read disturbance. The main components of the 8T cell include:

1. **Cross-Coupled Inverters**: As in the 6T design, the 8T SRAM cell includes two CMOS inverters connected in a feedback loop to form a bistable latch that retains the logic value ("1" or "0").

2. **Write Access Transistors**: Two NMOS transistors connect the storage nodes (Q and QB) to the bit lines (BL and BLB). These transistors are controlled by the write word line (WWL), enabling data to be written into the cell when activated.
3. **Dedicated Read Path:** Unlike the 6T SRAM, which uses shared access transistors for both reading and writing, the 8T cell incorporates a separate read path consisting of two NMOS transistors. These transistors form a read stack controlled by a read word line (RWL), allowing data to be read without affecting the internal node voltages.

4. **Read Isolation**: The separation of read and write paths ensures that the storage nodes are not disturbed during a read operation. This read isolation significantly improves read stability, especially under low-voltage conditions, making the 8T SRAM cell suitable for energy-efficient designs.

Schematic diagram-



8T SRAM cell

WINSPICE Netlist

1.8 T SRAM CELL WRITE-

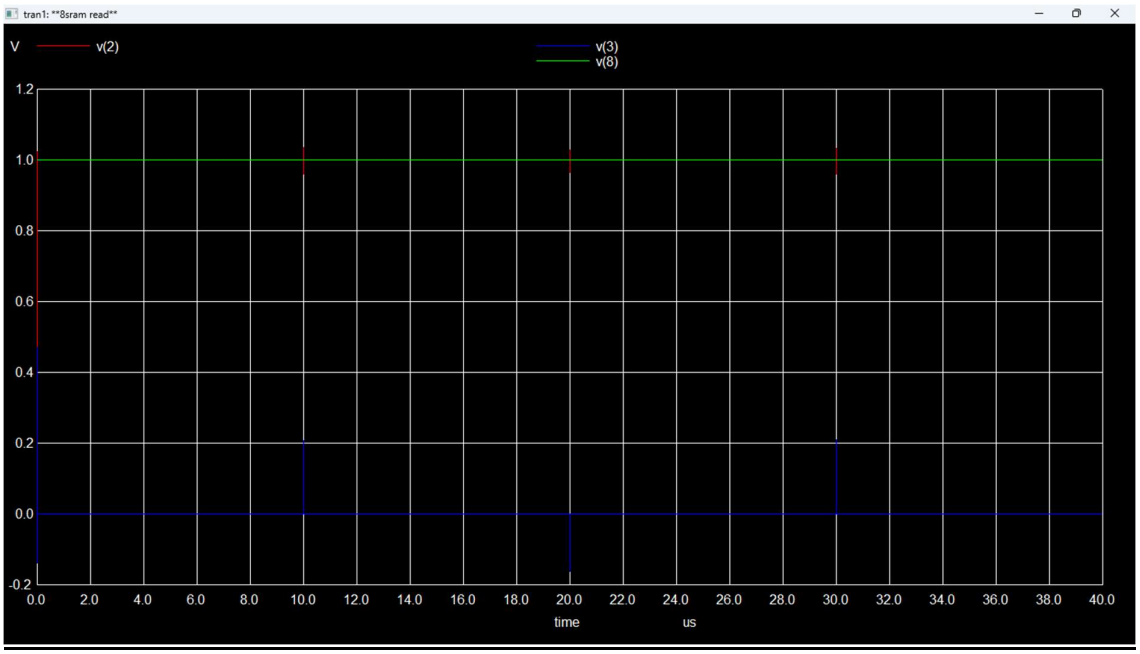
```
**8 SRAM Write**

Vdd 1 0 DC 1V
Vwl 6 0 PULSE(5 0 0 0 0 10n 20n)
Vbl 4 0 DC 0V
Vblb 5 1 DC 0V
Vrwl 7 0 DC 0V
Vrbl 8 0 DC 0V

.model pmod pmos level=54 version=4.7
.model nmod nmos level=54 version=4.7

M1 2 3 1 1 pmod W=20u L=1u
```

M2 3 2 1 1 pmod W=20u L=1u
M3 2 3 0 0 nmod W=10u L=1u
M4 3 2 0 0 nmod W=10u L=1u

M5 2 6 4 0 nmod W=10u L=1u
M6 3 6 5 0 nmod W=10u L=1u

M7 9 7 3 0 nmod W=10u L=1u
M8 8 9 0 0 nmod W=10u L=1u

.control
tran 1n 100n
plot V(2) V(3)
.endc
.end



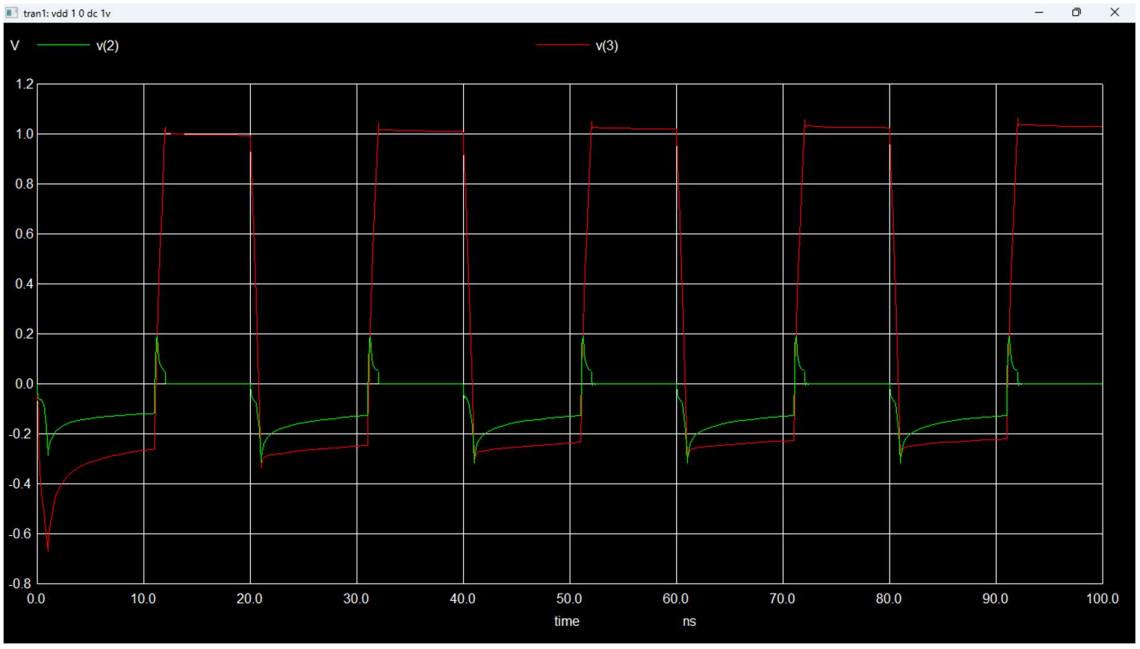
Simulation OF 8T SRAM CELL WRITE

1.8 T SRAM CELL READ-

8SRAM Read

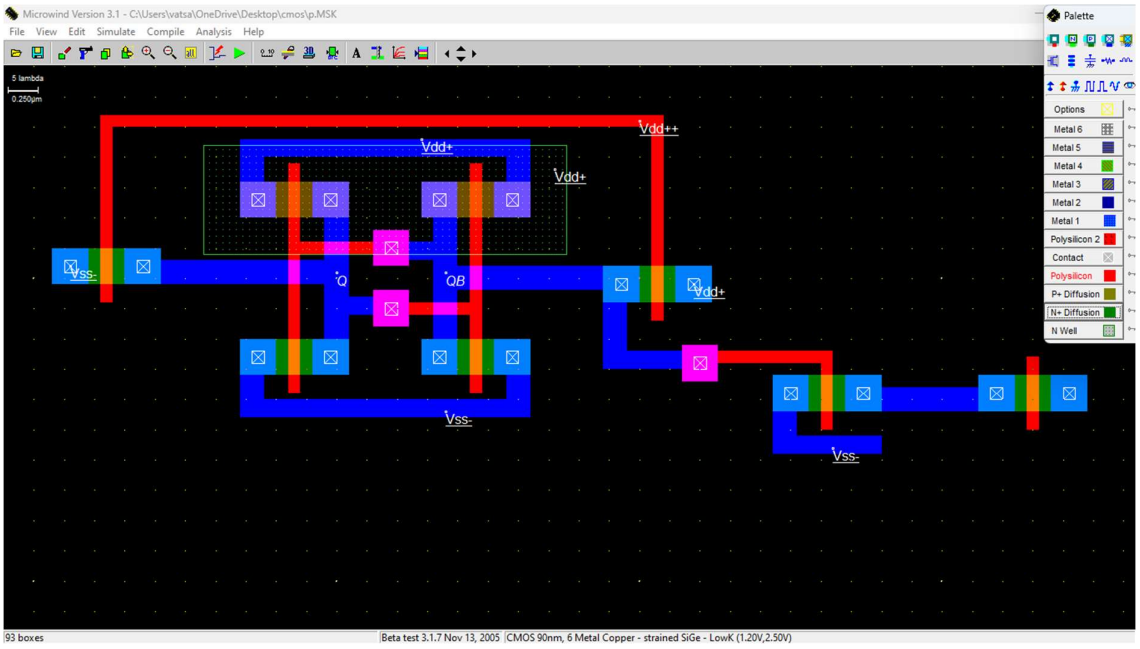
8SRAM Read
* Power Supply

```
Vdd 1 0 DC 1V
* Control Signals
Vwl 6 0 DC 0V
Vbl 4 0 DC 0V
Vblb 5 0 DC 0V
Vrwl 7 0 PULSE(5 0 0 0 0 10u 20u)
Vrbl 8 0 DC 1V

* Models
.model pmod pmos level=54 version=4.7
.model nmod nmos level=54 version=4.7

* Cross-coupled inverters (6T Core)
M1 2 3 1 1 pmod W=20u L=1u
M2 3 2 1 1 pmod W=20u L=1u
M3 2 3 0 0 nmod W=10u L=1u
M4 3 2 0 0 nmod W=10u L=1u

* Write Access Transistors (disabled)
M5 2 6 4 4 nmod W=10u L=1u
M6 3 6 5 5 nmod W=10u L=1u

* Read Access Transistors (enabled)
M7 9 7 3 3 nmod W=10u L=1u
M8 8 9 0 0 nmod W=10u L=1u

* Simulation Control
.control
tran 1n 40u
plot V(8) V(2) V(3)
.endc
.end
```

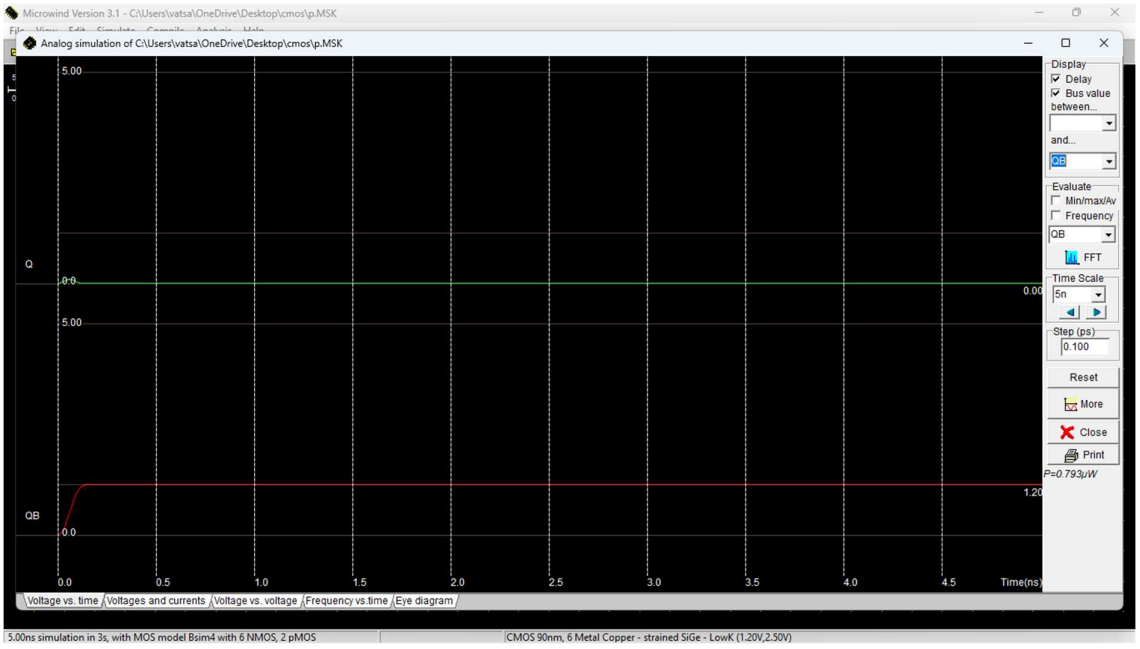


Simulation OF 8T SRAM CELL READ

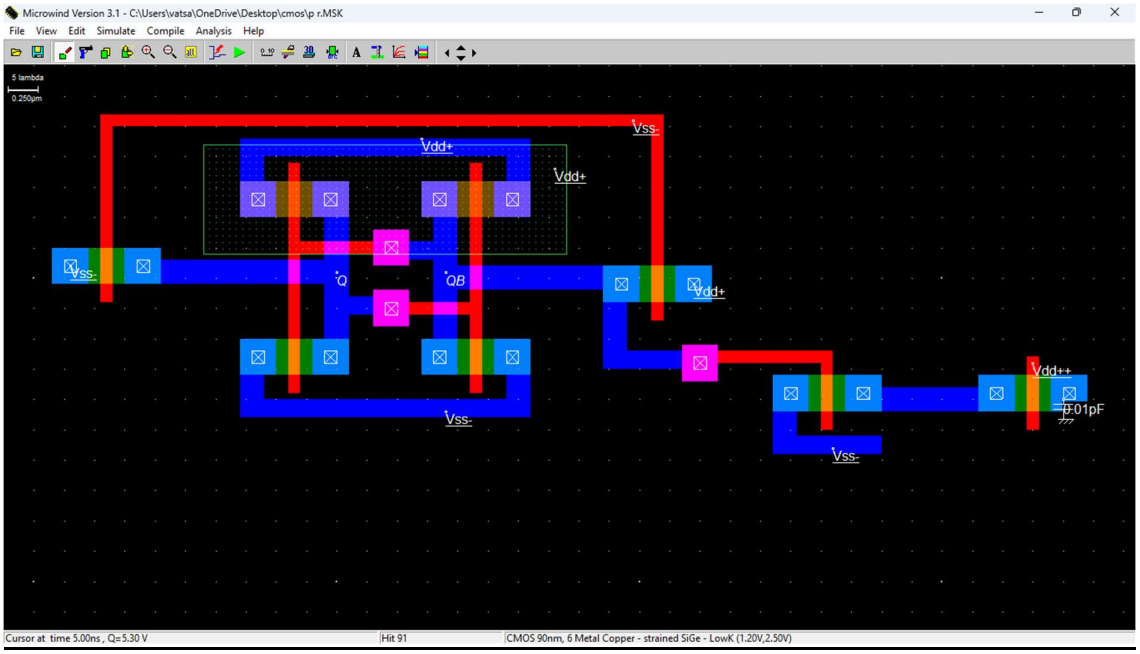
Microwind Layouts-



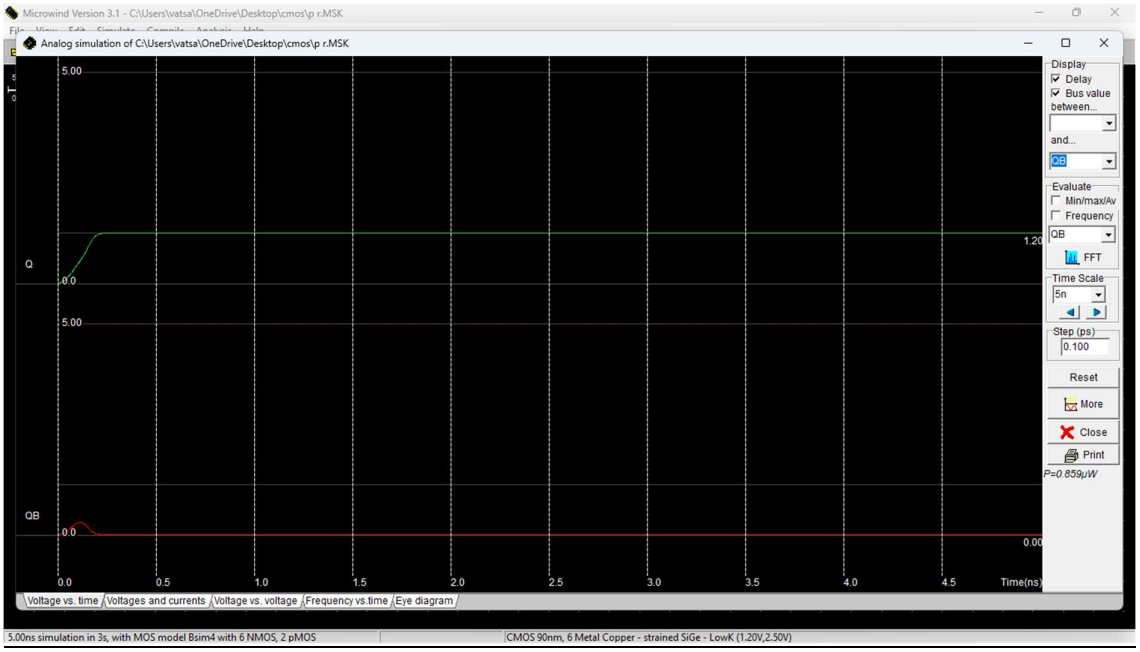
8T SRAM CELL WRITE



Simulation of 8T SRAM CELL WRITE



8T SRAM CELL READ



Simulation of 8T SRAM CELL READ

Advantages over 6T SRAM CELL-

1. Power Consumption

- 6T SRAM:
  - Read Power: Generally higher due to the need for full bitline precharge to VDDV_{DD}VDD before read operations.
  - Write Power: Moderate, but power spikes can occur as data flips and charges are shared.
  - Standby Power: Low, but leakage current in the standby mode can contribute significantly to power usage, especially in scaled-down nodes (sub-100 nm).
- 8T SRAM:
  - Read Power: Lower than 6T SRAM because the dedicated read path avoids bit line swinging on the main bit lines, and only a single-ended read bit line is used, reducing dynamic power consumption.
  - Write Power: Comparable to 6T or slightly higher, depending on the design of the write access path. The write operation uses standard access transistors, and since the read path is isolated, it does not interfere, but the added transistors slightly increase capacitance.

- Standby Power: Lower than 6T SRAM due to the separation of read and write circuits, which helps minimize leakage and disturbances during idle periods.

Comparison Summary: The 8T SRAM cell typically offers lower power consumption during reads and standby due to its isolated and efficient read path. Write power is similar or marginally higher compared to 6T SRAM, depending on the implementation. This makes the 8T SRAM an attractive option for low-power and high-reliability applications.

2. Leakage Current

- 6T SRAM:
  - Leakage can be significant, particularly in modern nodes, because all transistors are active during both read and write, and no isolation exists between read/write paths.
  - In a low-power or deep-sleep mode, leakage current can degrade data integrity.
- 10T SRAM:
  - Additional transistors in the 8T cell isolate the storage nodes during **read operations**, which helps reduce the risk of data disturbance and minimizes leakage through the read path.
  - Reduced soft- Improved compared to 6T SRAM, as the isolated read path reduces the exposure of sensitive storage nodes to external disturbances, though slightly less robust than 10T in extreme environments.

Comparison Summary: The 8T SRAM cell exhibits lower leakage current during read operations due to storage node isolation. While standby leakage is reduced compared to 6T, it's slightly higher than 10T due to fewer isolation transistors. However, 8T still offers a good trade-off between leakage control and area efficiency.

3. Stability (Read and Write Margins)

- 6T SRAM:
  - Lower stability during read operations because accessing the bitline directly impacts the storage nodes, which can lead to data flipping in scaled-down technologies.

    - Write margin can be adjusted by sizing transistors, but this can affect read stability negatively, creating a trade-off.
- 8T SRAM:
    - Improved read stability due to the separation of the read path, which prevents the read operation from disturbing the data held in the cell.
    - Write stability is also slightly better, with selective control of write access, reducing the risk of unintended data flipping.

Comparison Summary: 8T SRAM generally has better stability for both read and write operations, as well as a more favorable noise margin.

4. Performance and Speed

- 6T SRAM:
    - Typically faster due to its simpler structure and fewer transistors.
    - Some power-performance trade-offs arise if speed is prioritized at the expense of read stability.
- 8T SRAM:
    - Slightly slower due to additional transistors, which increase cell capacitance and delay.
    - More suited for applications where stability and power efficiency are prioritized over raw speed.

Comparison Summary: 6T SRAM tends to be faster, but 8T SRAM provides more reliability, especially in power-constrained environments.

Example Data (Based on Research Papers and Trends)

Here's an example of typical performance metrics, though actual numbers depend heavily on technology and specific design parameters.

Summary of Advantages of 8T Over 6T

- Power Efficiency: Lower power consumption during read and standby.
- Stability: Improved read and write stability, particularly valuable for low-voltage or noise-sensitive applications.
- Leakage Reduction: Lower leakage current, contributing to longer battery life in low-power applications.
- Noise Immunity: Higher noise margins make it more suitable for aggressive scaling or low-power designs.

Application-

The 8T SRAM cell is especially valuable in applications where high stability, low power, and robust read and write operations are essential. Here are some key applications in the electronics industry:

1. Low-Power Mobile and Wearable Devices

- Smartphones and tablets demand memory solutions that minimize power usage without sacrificing performance. The reduced leakage current and power efficiency of 8T SRAM cells make them ideal for these devices, which require long battery life.
- Wearable electronics like fitness trackers, smartwatches, and health monitoring devices also benefit from the 8T cell's low standby power and high reliability, as these devices operate at low voltages and need energy-efficient memory.

2. Battery-Powered Medical Devices

- Many medical devices, such as portable diagnostic tools, implantable devices, and continuous monitoring systems, require long operational life with limited power sources. The 8T SRAM's energy-efficient and reliable operation makes it suitable for these applications, where memory stability can be life-critical, and power sources like batteries are challenging to replace.

3. Artificial Intelligence (AI) and Machine Learning (ML) Accelerators

- AI and ML applications often involve large datasets and require high memory bandwidth and reliability. The 8T SRAM cell can improve memory access stability and efficiency, making it suitable for AI/ML accelerators, which rely on high-performance memory for data processing, caching, and storing weights and parameters.