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| |  | | --- | | 258057-15121013434242 | | 2022/10/17  實驗五  FSM練習  姓名：王嘉羽 學號：00957116  班級：資工3B  E-mail：vayne20011125@gmail.com | |  | |  | |  | | --- | | 注意繳交時一律轉PDF檔繳交期限為上完課後當週五晚上12點前一人繳交一份檔名：學號\_HW?.pdf檔名請按照作業檔名格式進行填寫未依照格式不予批改 | |  | |  | |

1. **Counter + register**

* **實驗說明：**

1. counter數到20做累加運算，counter加到10的時候將值傳到port\_A，加到20的時候傳到port\_B
2. 輸入：clk, reset
3. 輸出：port\_A[7:0]、port\_B[7:0]

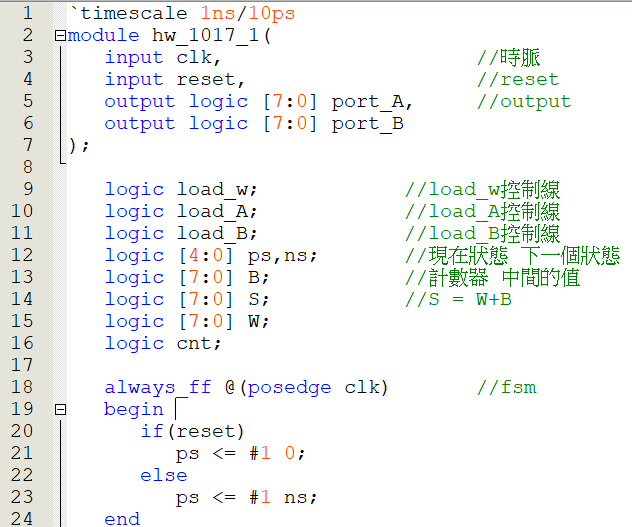
* **系統硬體架構方塊圖（接線圖）：**

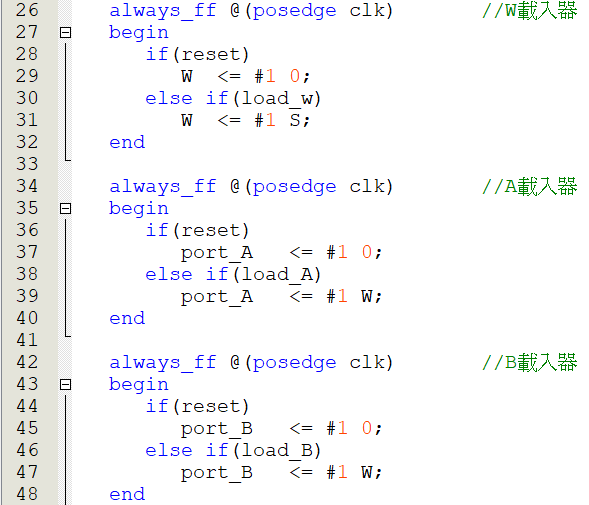


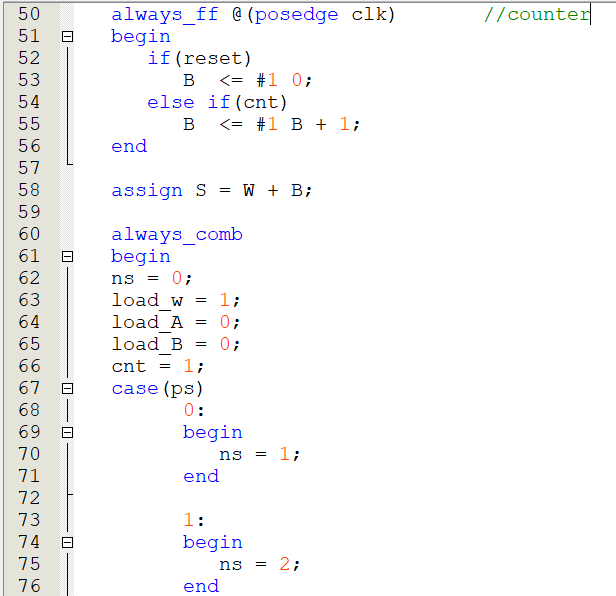
* **系統架構程式碼、測試資料程式碼與程式碼說明(.sv檔及.do檔都要截圖)**

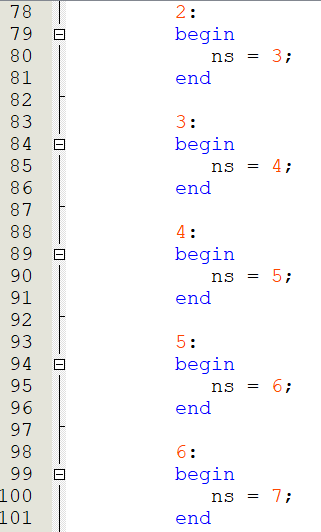
**截圖請善用win+shift+S**

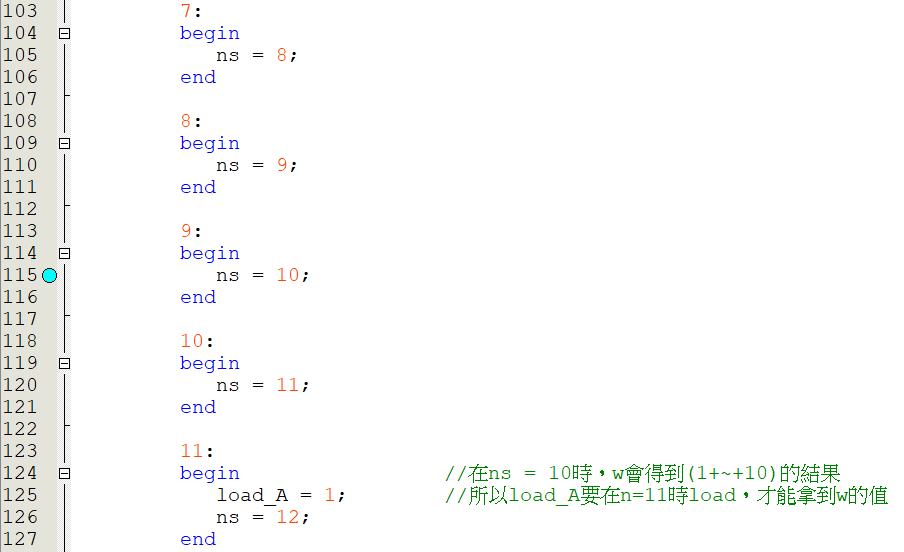
* Hw\_1017\_1.sv

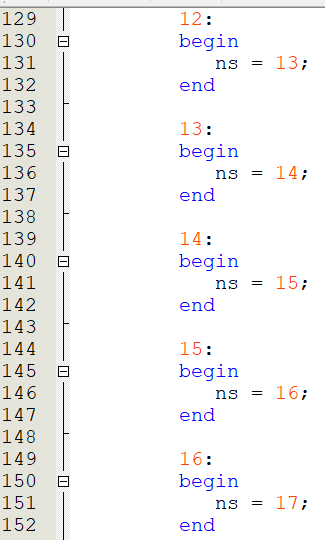


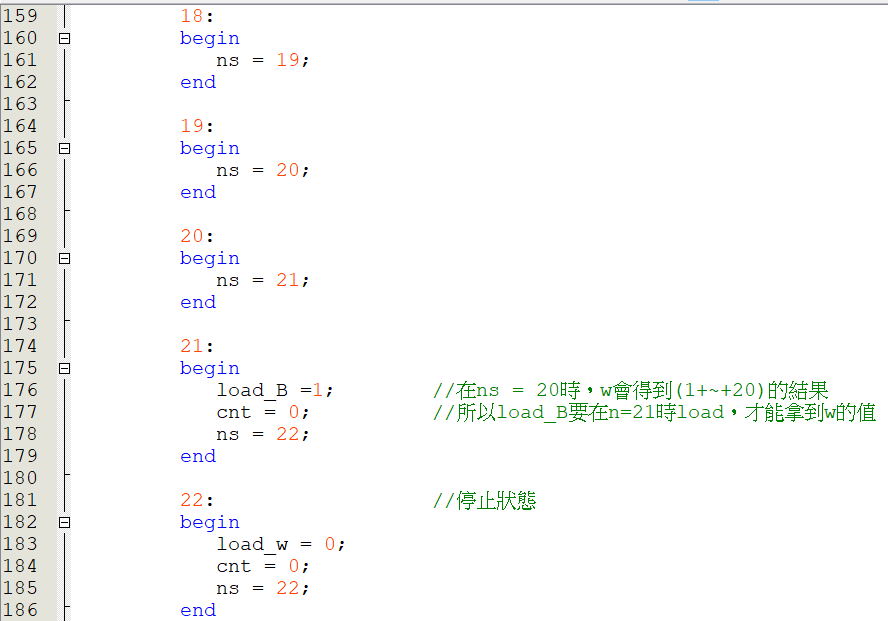


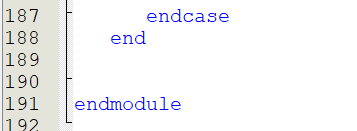




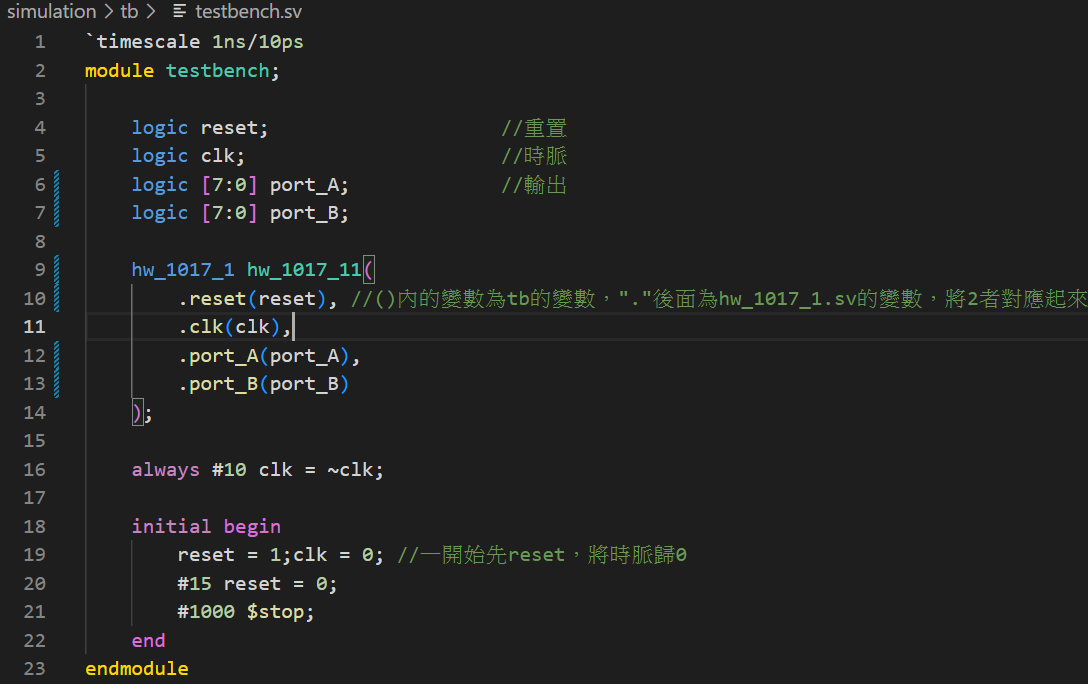




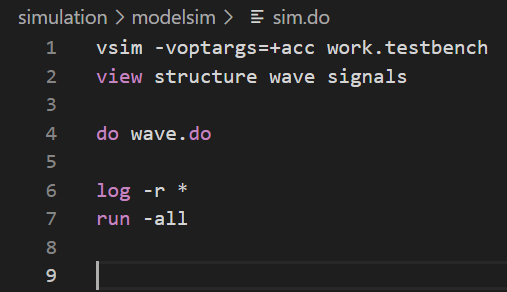




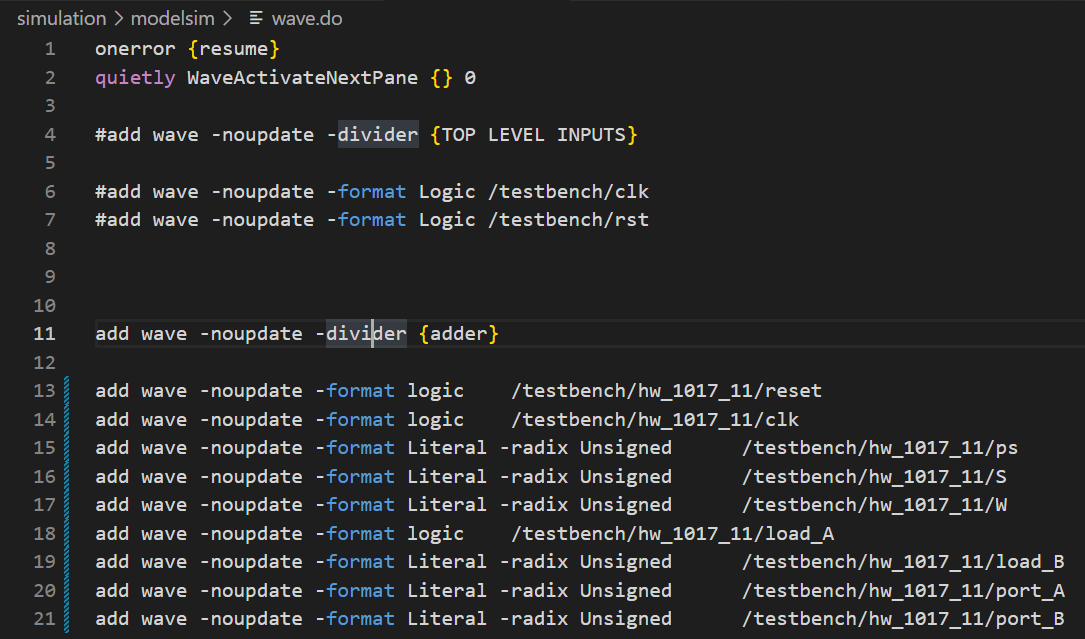
* Testbench.do



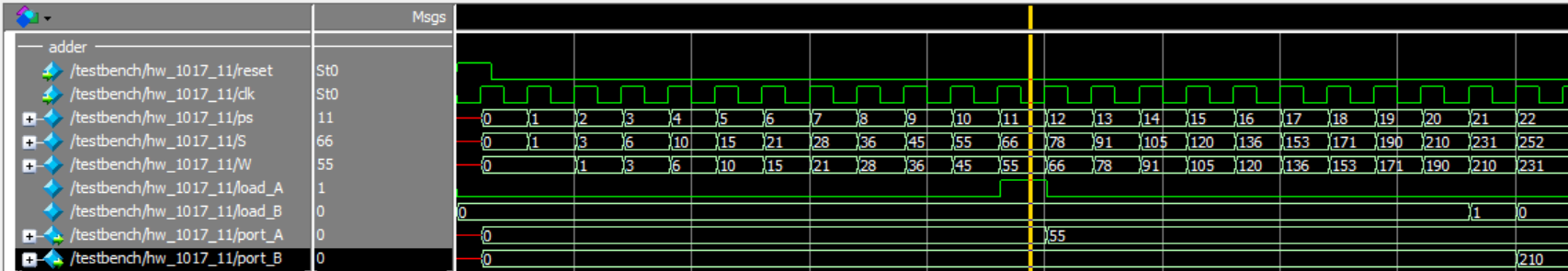
* Sim.do



* wave.do



* **模擬結果與結果說明：**



要在conuter加到10的時候把值load到port\_A，但load到port\_A之前，要先load到W，所以是ps = 10 -> s 加到 10 -> w 得到值; ps = 11時在讓port\_A去對W做load，所以會在n=12時取得w的值。同理port\_B;

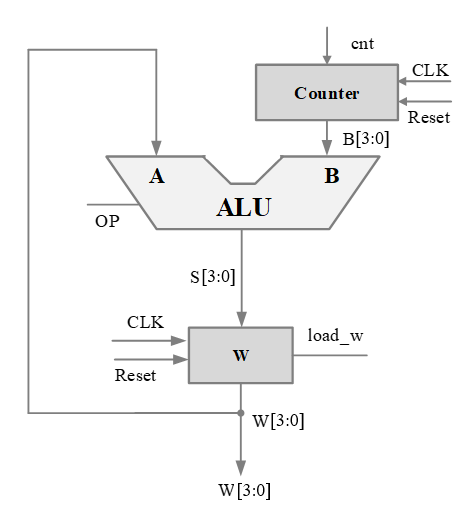
1. **Counter+ALU+register**

* **實驗說明：**

1. 設計一電路，此電路由counter、ALU、register組成，Counter 由0數到10  
   S = 0 + 1 | 2 \* 3 - 4 / 5 + 6 + 7 ^ 8 + 9 & 10，依序計算，並將計算結果S依序存入W暫存器
2. 輸入：clk, reset
3. 輸出：W[3:0]

|  |  |  |
| --- | --- | --- |
| op[2:0] | ALU運算 | 註解 |
| 3’b000 | S = A + B | 相加 |
| 3’b001 | S = A - B | 相減 |
| 3’b010 | S = A \* B | 相乘 |
| 3’b011 | S = A / B | 除法 |
| 3’b100 | S = A & B | AND |
| 3’b101 | S = A | B | OR |
| 3’b110 | S = A ^ B | XOR |

* **系統硬體架構方塊圖（接線圖）：**

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* **系統架構程式碼、測試資料程式碼與程式碼說明(.sv檔及.do檔都要截圖)**

**截圖請善用win+shift+S**

* **模擬結果與結果說明：**
* **結論與心得：**