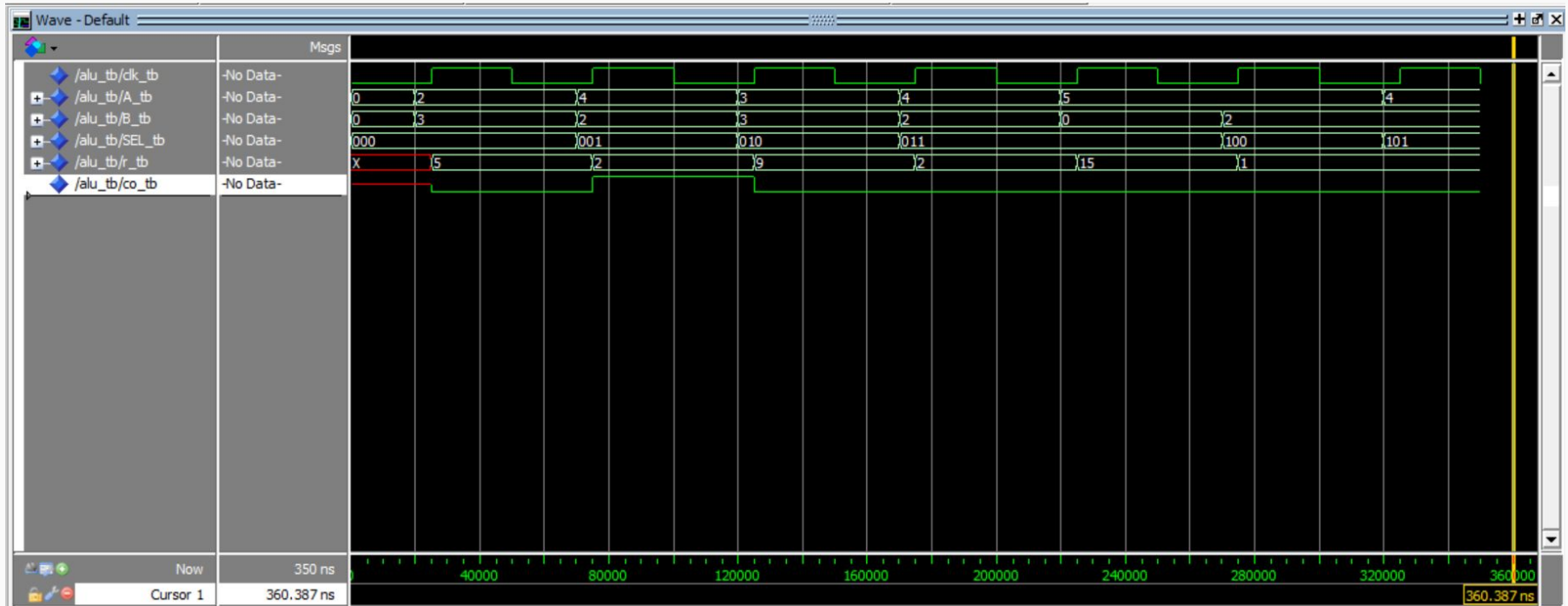


Arithmetic Logic Unit (ALU)

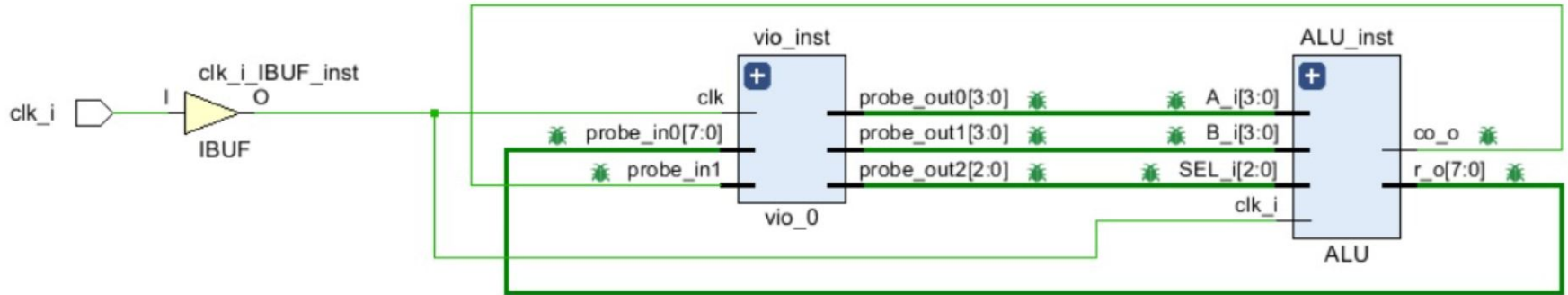
Proyecto Final de *Circuitos Lógicos Programables*

- **Profesor:** Nicolás Alvarez
- **Alumno:** Agustin Vazquez

ALU de 4 bits



Implementación de la ALU de 4 bits



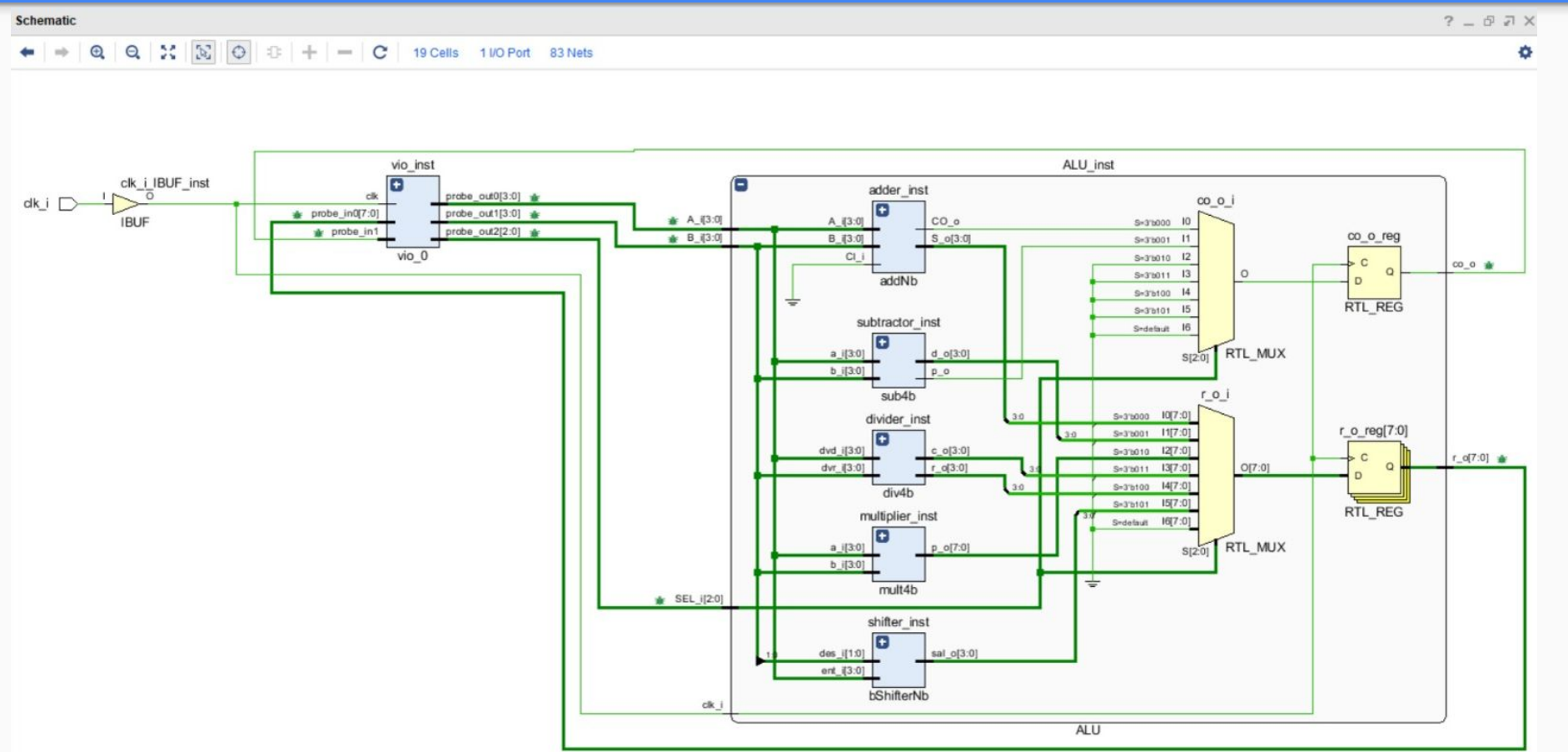
[illegible]

Tabla de operaciones de la ALU

ALU_Sel	Operación	Resultado
000	Suma	$A + B$
001	Resta	$A - B$
010	Multiplicación	$A * B$
011	División	A / B
100	Módulo	$A \% B$
101	Desplazamiento	$A \gg B$

Simulación Modelsim

Operación: suma

The screenshot displays the Modelsim simulation environment. At the top, the 'Wave - Default' window shows a list of variables on the left and a waveform on the right. The variables are: /addnb_tb/A_tb, /addnb_tb/B_tb, /addnb_tb/CI_tb, /addnb_tb/S_tb, and /addnb_tb/CO_tb. The waveform shows values for these variables over time, with specific values like 12, 15, and 0 visible.

Below the wave window, there are two 'hw_vios' windows, each showing a table of hardware variables and their values. The left 'hw_vios' window shows the following data:

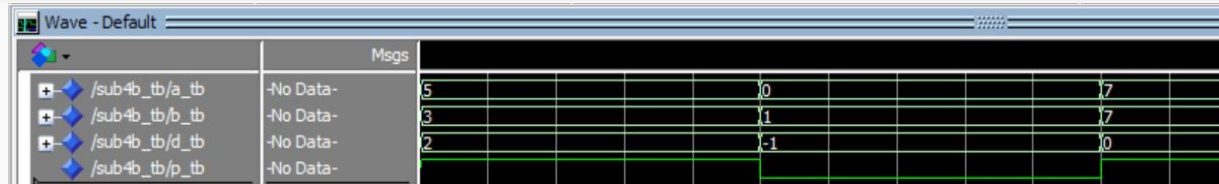
Name	Value	Activity	Direction	VIO
> A_[3:0]	[H] 5		Output	hw_vio_1
> B_[3:0]	[H] 2		Output	hw_vio_1
int_co	[B] 0		Input	hw_vio_1
> int_r[7:0]	[H] 07		Input	hw_vio_1
> SEL_[2:0]	[H] 0		Output	hw_vio_1

The right 'hw_vios' window shows the following data:

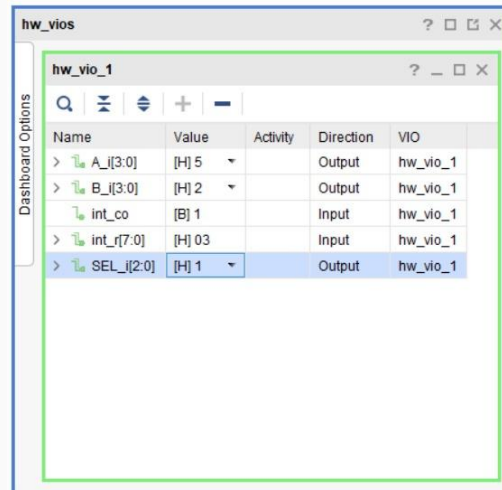
Name	Value	Activity	Direction	VIO
> A_[3:0]	[H] E		Output	hw_vio_1
> B_[3:0]	[H] 3		Output	hw_vio_1
int_co	[B] 1		Input	hw_vio_1
> int_r[7:0]	[H] 01		Input	hw_vio_1
> SEL_[2:0]	[H] 0		Output	hw_vio_1

Simulación Modelsim

Operación: resta



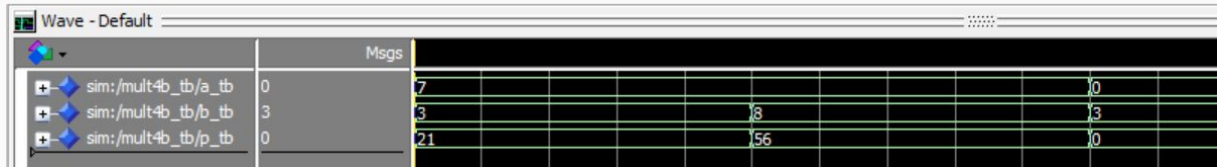
Msgs									
5					0				7
3					1				7
2					-1				0



Name	Value	Activity	Direction	VIO
> A_[3:0]	[H] 5		Output	hw_vio_1
> B_[3:0]	[H] 2		Output	hw_vio_1
int_co	[B] 1		Input	hw_vio_1
> int_[7:0]	[H] 03		Input	hw_vio_1
> SEL_[2:0]	[H] 1		Output	hw_vio_1

Simulación Modelsim

Operación: **multiplicación**



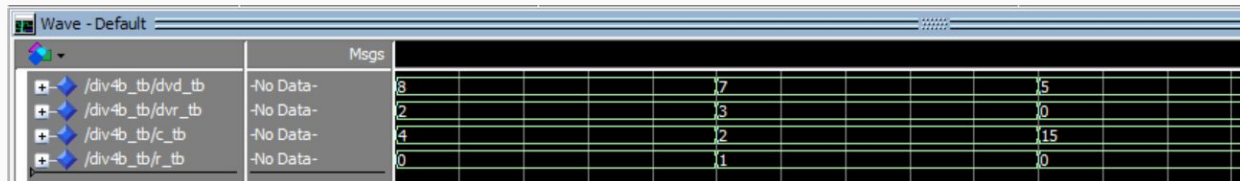
hw_vios

hw_vios_1

Name	Value	Activity	Direction	VIO
> A_([3:0])	[H] 5		Output	hw_vios_1
> B_([3:0])	[H] 2		Output	hw_vios_1
int_co	[B] 0		Input	hw_vios_1
> int_r[7:0]	[H] 0A		Input	hw_vios_1
> SEL_([2:0])	[H] 2		Output	hw_vios_1

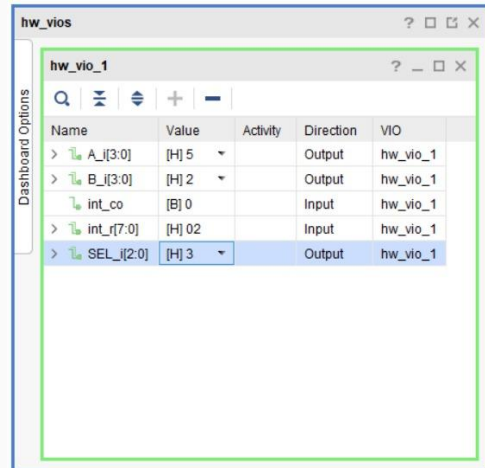
Simulación Modelsim

Operación: división y módulo



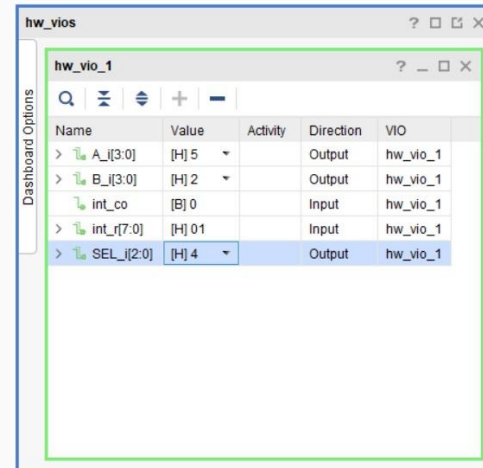
Wave - Default

	Msgs
/div4b_tb/dvd_tb	-No Data- 8 7 5
/div4b_tb/dvr_tb	-No Data- 2 3 0
/div4b_tb/c_tb	-No Data- 4 2 15
/div4b_tb/r_tb	-No Data- 0 1 0



hw_vios

Name	Value	Activity	Direction	VIO
> A_[3:0]	[H] 5		Output	hw_vio_1
> B_[3:0]	[H] 2		Output	hw_vio_1
int_co	[B] 0		Input	hw_vio_1
> int_r[7:0]	[H] 02		Input	hw_vio_1
> SEL_[2:0]	[H] 3		Output	hw_vio_1

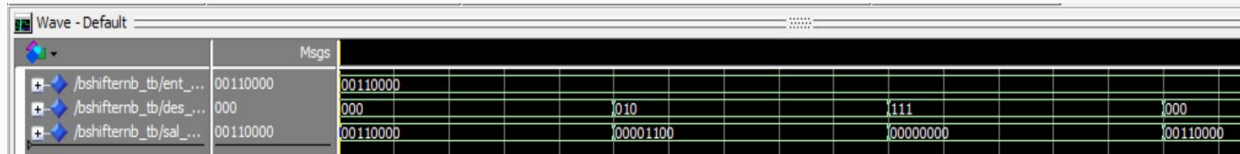


hw_vios

Name	Value	Activity	Direction	VIO
> A_[3:0]	[H] 5		Output	hw_vio_1
> B_[3:0]	[H] 2		Output	hw_vio_1
int_co	[B] 0		Input	hw_vio_1
> int_r[7:0]	[H] 01		Input	hw_vio_1
> SEL_[2:0]	[H] 4		Output	hw_vio_1

Simulación Modelsim

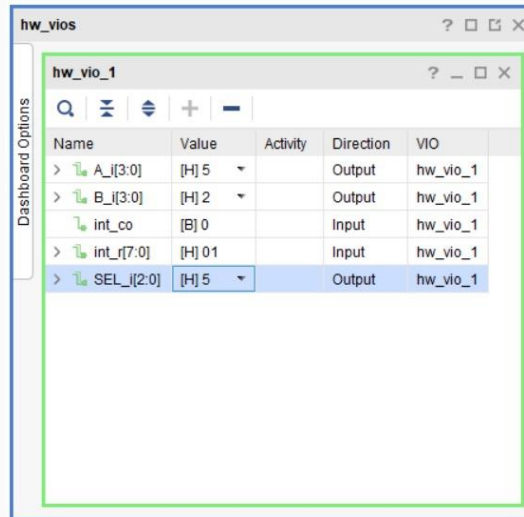
Operación: desplazamiento



Wave - Default

Signal	Value
/bshifternb_tb/ent_...	00110000
/bshifternb_tb/des_...	000
/bshifternb_tb/sal_...	00110000

Timing diagram showing waveforms for three signals. The signals are: /bshifternb_tb/ent_..., /bshifternb_tb/des_..., and /bshifternb_tb/sal_... The waveforms show binary values over time.



hw_vios

hw_vio_1

Name	Value	Activity	Direction	VIO
> A_[(3:0)]	[H] 5		Output	hw_vio_1
> B_[(3:0)]	[H] 2		Output	hw_vio_1
int_co	[B] 0		Input	hw_vio_1
> int_r[7:0]	[H] 01		Input	hw_vio_1
> SEL_[(2:0)]	[H] 5		Output	hw_vio_1

Dashboard Options

File Edit Flow Tools Reports Window Layout View Help Quick Access

write_bitstream Complete ✓

Default Layout

Flow Navigator

- Schematic
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Utilization
 - Report Power
 - Schematic
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager
 - Open Target
 - Program Device

HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/003017B7EDF5A

No hardware target is open. Open target

Hardware

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/003017B7EDF5A	Closed

Hardware Target Properties

localhost3121/xilinx_tcf/Digilent/003017B7EDF5A

Name: localhost/xilinx_tcf/Digilent/003017B7EDF5A

Type: xilinx_tcf

Status: Closed

General Properties

Tcl Console

```
commit_hw_vio [get_hw_probes A_i] -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z010_1] -filter {CELL_NAME=="vio_inst"}]]
set_property OUTPUT_VALUE 3 [get_hw_probes A_i -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z010_1] -filter {CELL_NAME=="vio_inst"}]]
commit_hw_vio [get_hw_probes A_i] -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z010_1] -filter {CELL_NAME=="vio_inst"}]]
close_hw_target [localhost:3121/xilinx_tcf/Digilent/003017B7EDF5A]
INFO: [Labtoolstcl 44-464] Closing hw_target localhost:3121/xilinx_tcf/Digilent/003017B7EDF5A
```

Type a Tcl command here

¡Muchas gracias por su
atención!