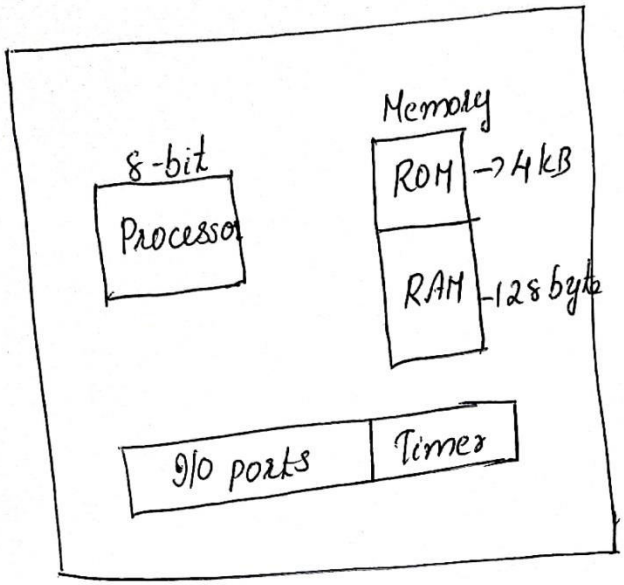
8051 MICROCONTROLLER

What is a microcontroller?

A microcontroller is a small, low-cost computer-on a-chip which usually includes:

- An 8 or 16 bit (CPU).
- A small amount of RAM.
- Programmable ROM and/or flash memory.
- Parallel and/or serial I/O.
- Timers and signal generators.
- Analog to Digital (A/D) and/or Digital to Analog (D/A) conversion.



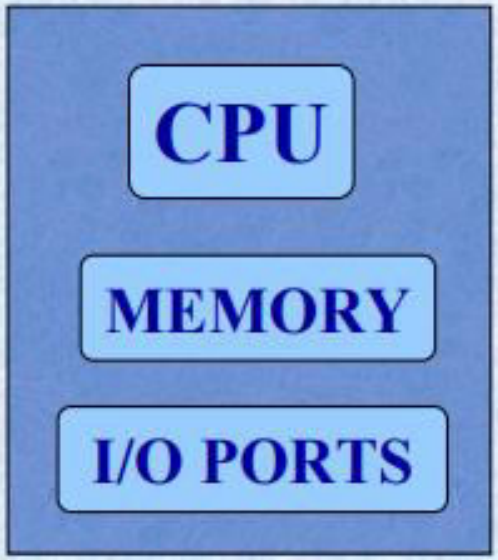
ROM - Program m/m

RAM - Data m/m

Difference

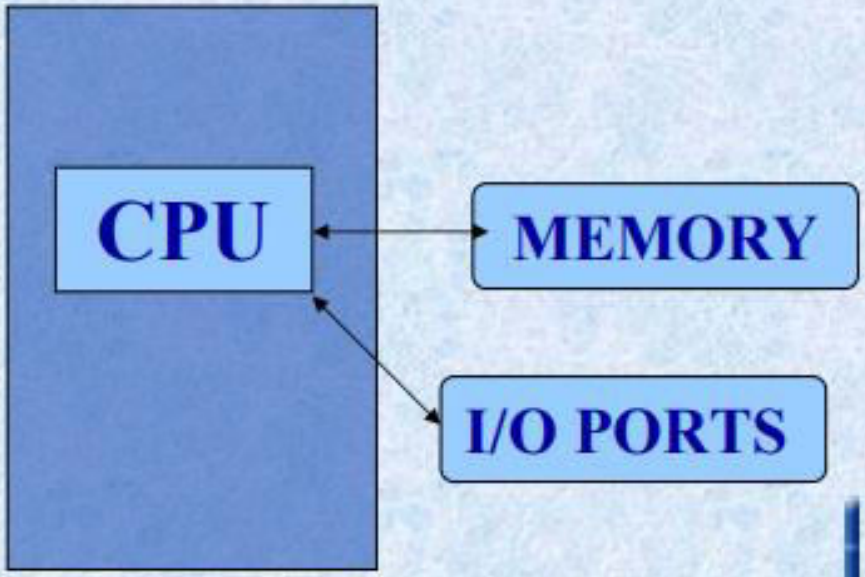
MICRO CONTROLLER

- It is a single chip
- Consists Memory,
- I/o ports

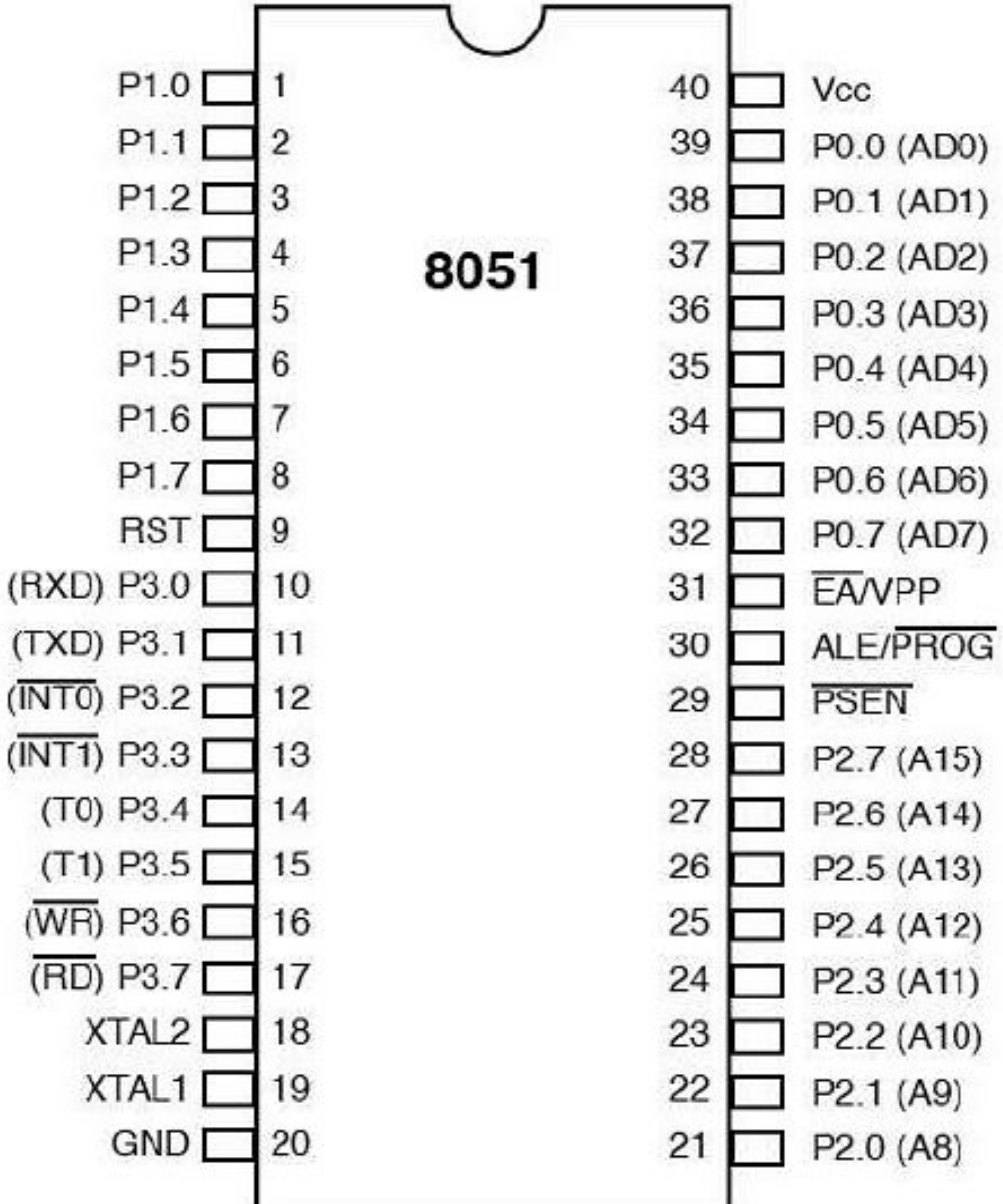


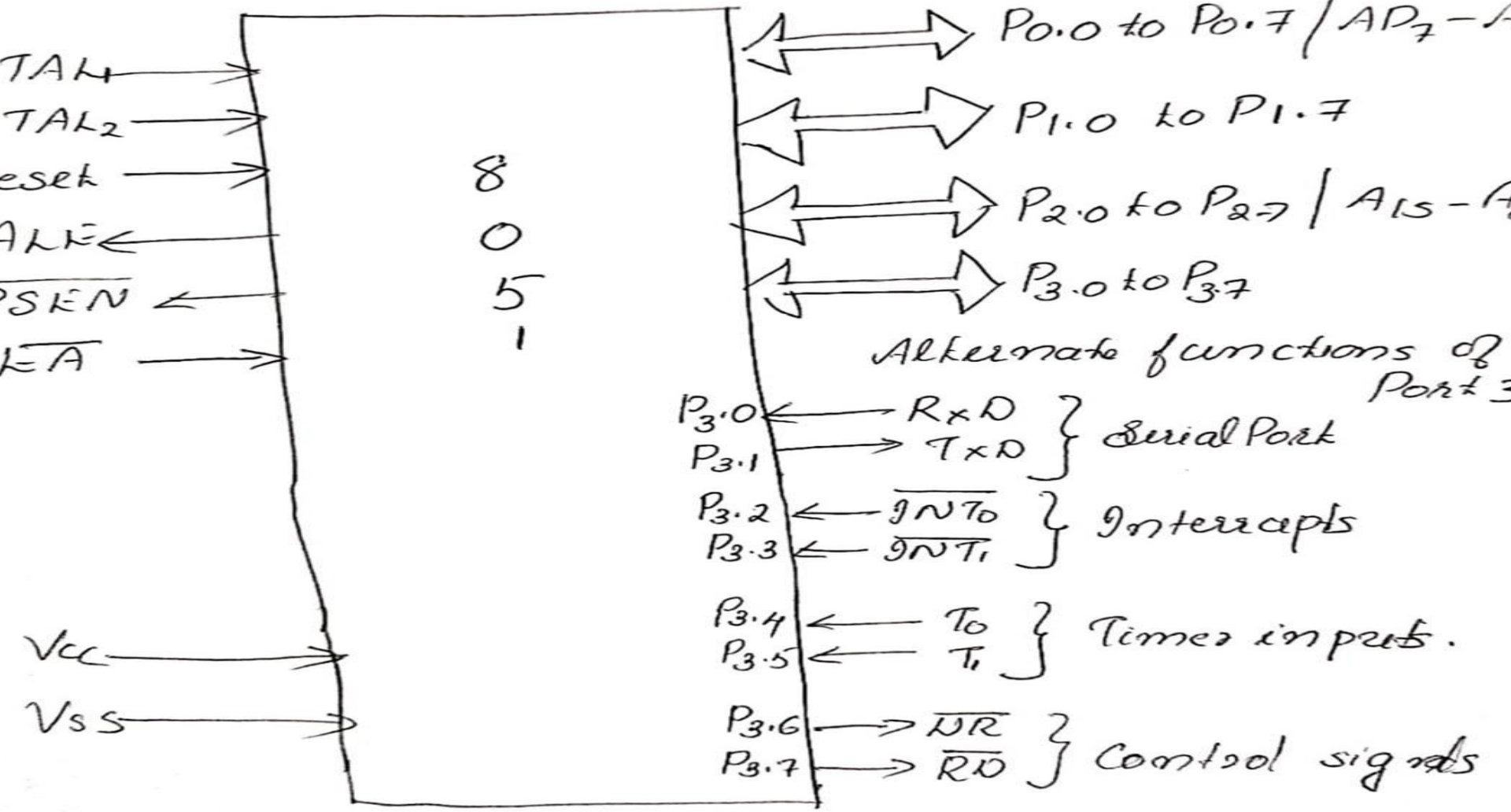
MICRO PROCESSER

- It is a cpu
- Memory, I/O Ports to be connected externally



Pin Diagram of 8051




TAL1
TAL2
eset
ALE
PSEN
EA
8
0
5
1
Vcc
Vss
P0.0 to P0.7 / AD7 - A
P1.0 to P1.7
P2.0 to P2.7 / A15 - A
P3.0 to P3.7
Alternate functions of Port 3
P3.0 RxD
P3.1 TxD
Serial Port
P3.2 INT0
P3.3 INT1
Interrupts
P3.4 T0
P3.5 T1
Timer inputs.
P3.6 WR
P3.7 RD
Control signals

Pins 1 to 8 − These pins are known as Port 1. This port doesn't serve any other functions. It is internally pulled up, bi-directional I/O port.

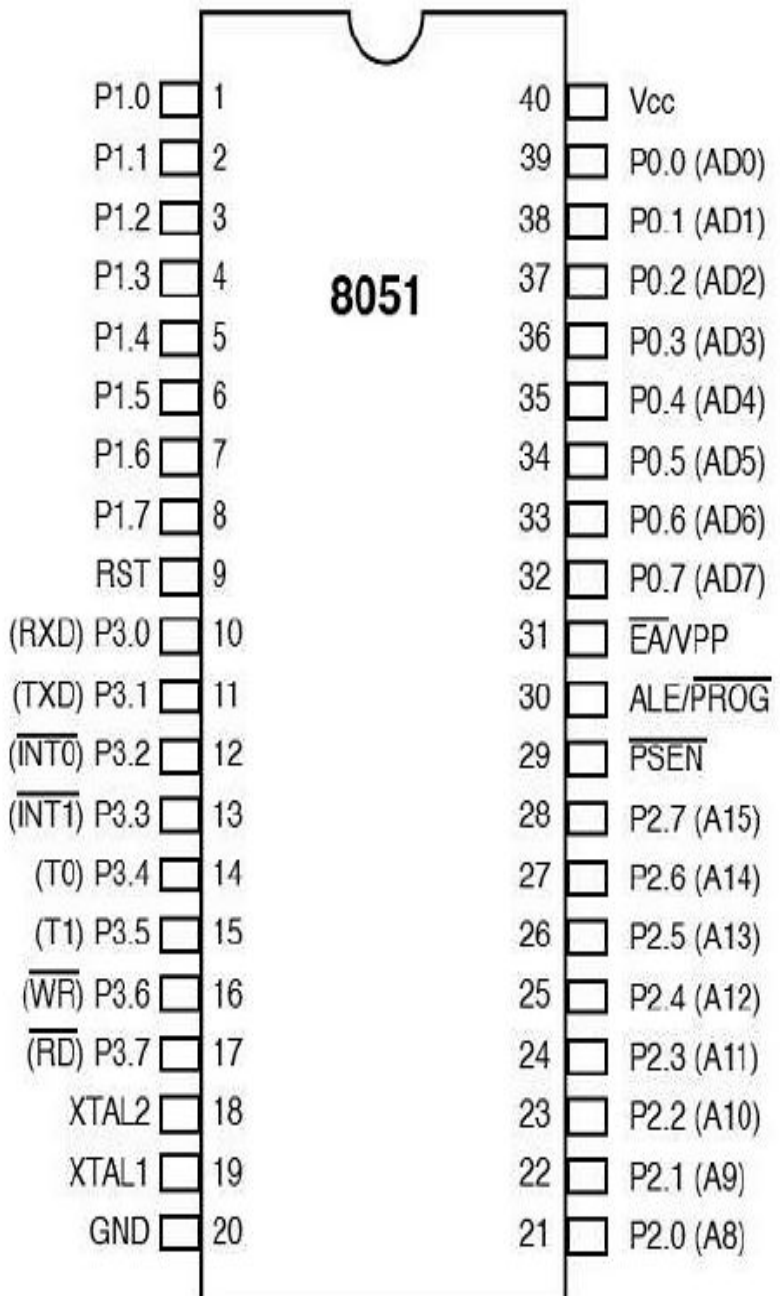
Pin 9 − It is a RESET pin, which is used to reset the microcontroller to its initial values.

Pins 10 to 17 − These pins are known as Port 3. This port serves some functions like interrupts, timer input, control signals, serial communication signals RxD and TxD, etc.

Pins 18 & 19 − These pins are used for interfacing an external crystal to get the system clock.

Pin 20 − This pin provides the ground supply to the circuit.

Pins 21 to 28 − These pins are known as Port 2. It serves as I/O port. Higher order address bus signals are also multiplexed using this port.



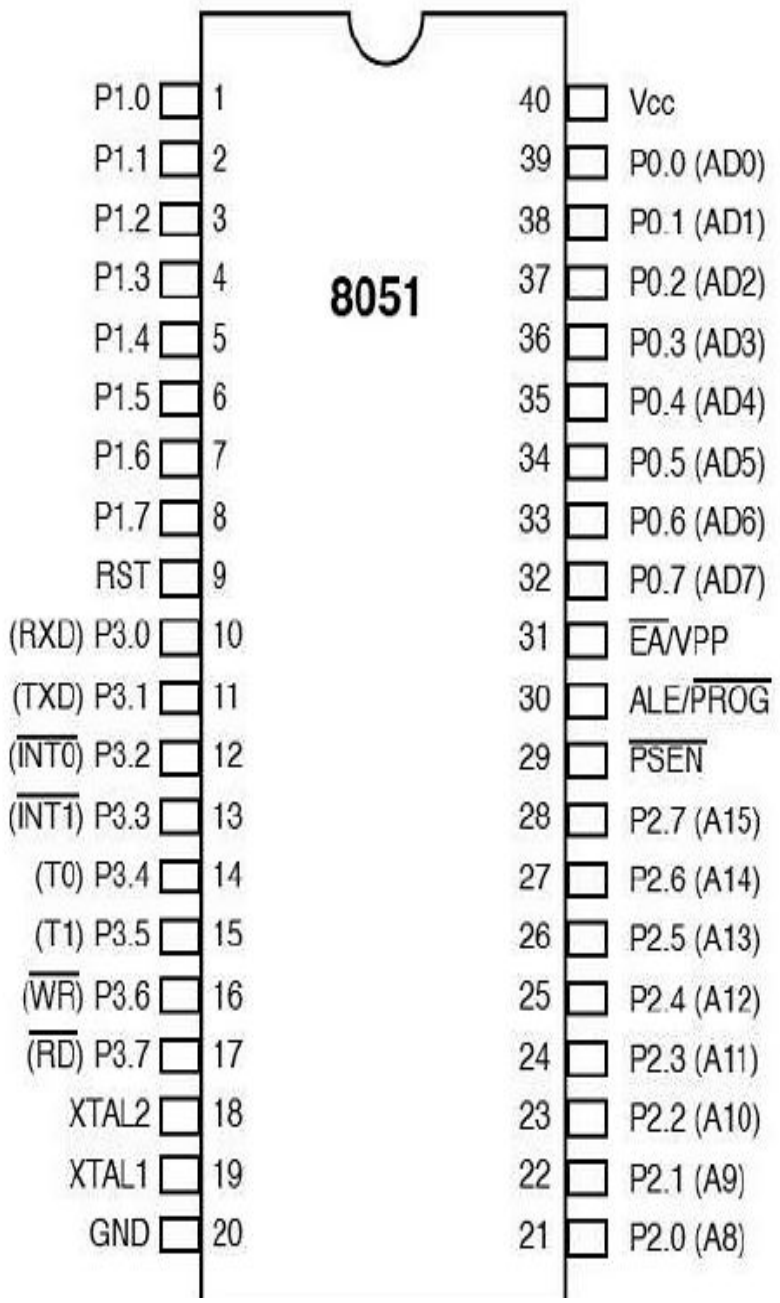
Pin 29 − This is PSEN pin which stands for Program Store Enable. It is used to read a signal from the external program memory.

Pin 31 − This is EA pin which stands for External Access input. It is used to enable/disable the external memory interfacing.

Pin 30 − This is ALE pin which stands for Address Latch Enable. It is used to demultiplex the address-data signal of port.

Pins 32 to 39 − These pins are known as Port 0. It serves as I/O port. Lower order address and data bus signals are multiplexed using this port.

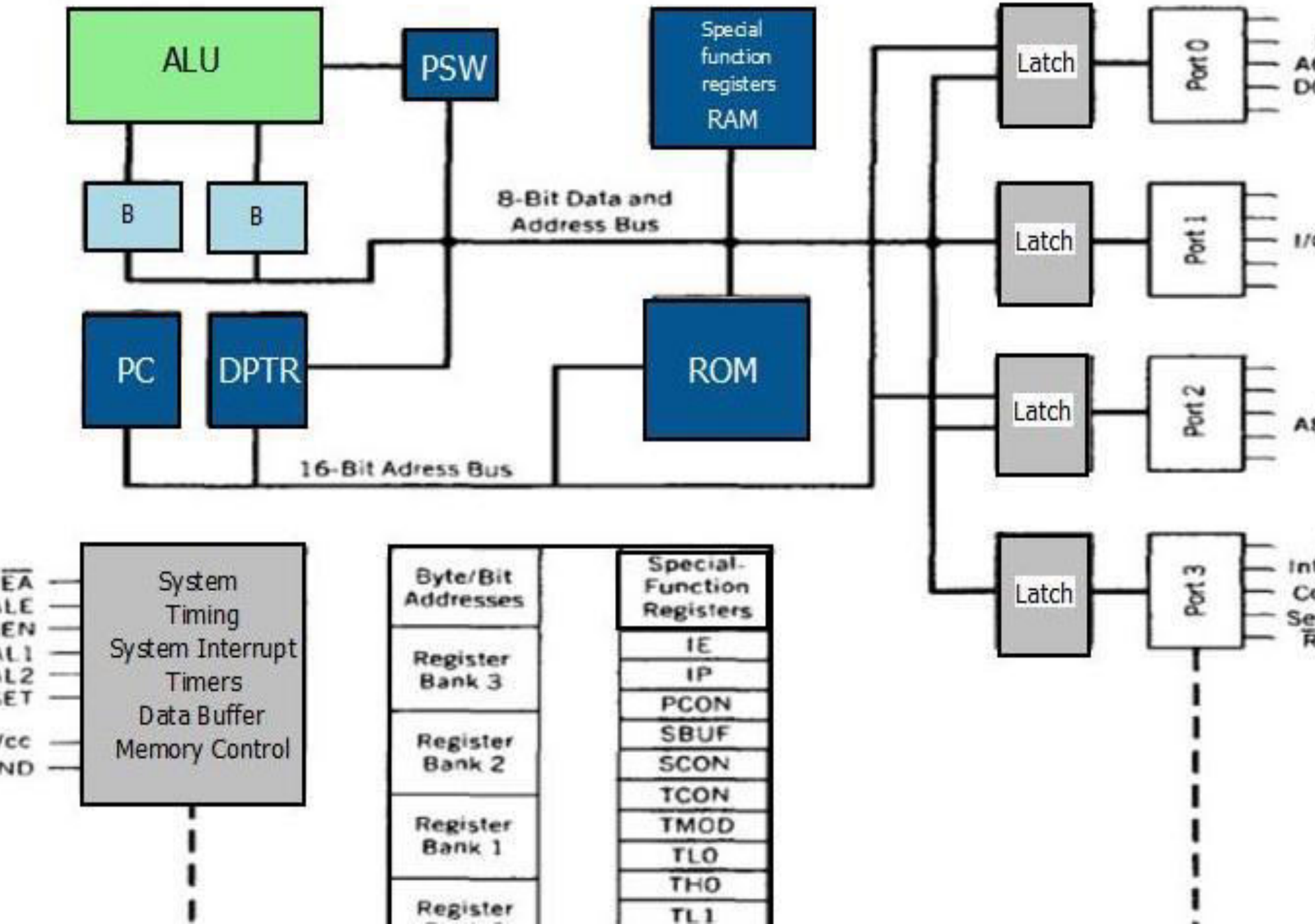
Pin 40 − This pin is used to provide power supply to the circuit.

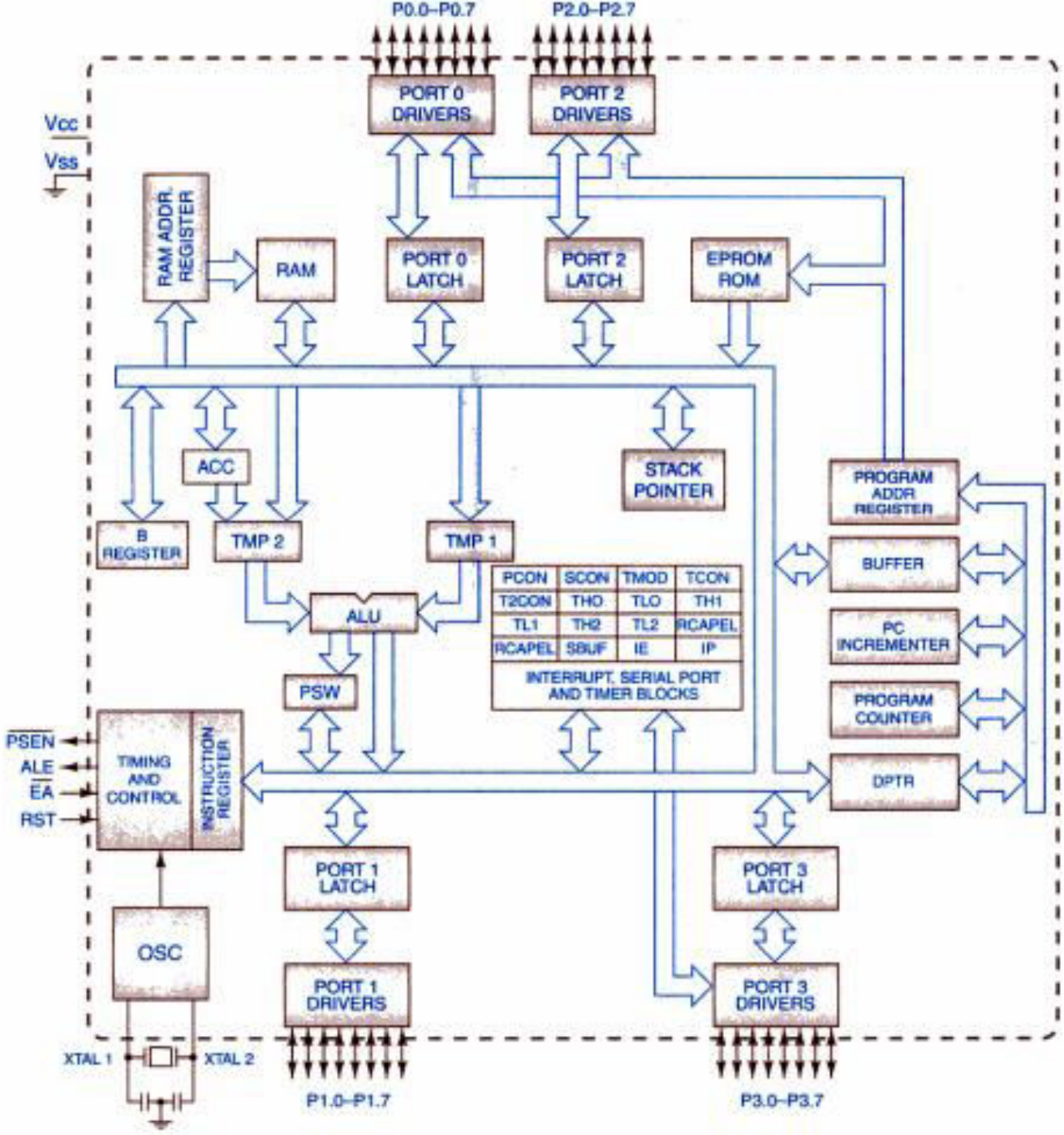


8051 Internal Architecture

The 8051 architecture include

- 8 bit CPU
- Memory
- Four 8 bit I/O
- Two 16 bit timers/counters
- Universal Asynchronous Receiver Transmitter(UART)


ALU
PSW
Special function registers
RAM
B
B
8-Bit Data and Address Bus
PC
DPTR
ROM
16-Bit Adress Bus
Latch
Latch
Latch
Latch
Port 0
Port 1
Port 2
Port 3
System
Timing
System Interrupt
Timers
Data Buffer
Memory Control
Byte/Bit Addresses
Special-Function Registers
Register Bank 3
Register Bank 2
Register Bank 1
IE
IP
PCON
SBUF
SCON
TCON
TMOD
TL0
TH0
TL1


P0.0–P0.7
P2.0–P2.7
PORT 0 DRIVERS
PORT 2 DRIVERS
Vcc
Vss
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
EPROM ROM
ACC
STACK POINTER
PROGRAM ADDR REGISTER
B REGISTER
TMP 2
TMP 1
BUFFER
PCON SCON TMOD TCON
T2CON TH0 TL0 TH1
TL1 TH2 TL2 RCAPEL
RCAPEH SBUF IE IP
INTERRUPT, SERIAL PORT AND TIMER BLOCKS
ALU
PC INCREMENTER
PSW
PROGRAM COUNTER
PSEN
ALE
EA
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
XTAL 1
XTAL 2
P1.0–P1.7
P3.0–P3.7

8051 Internal Architecture

PROCESSOR

The processor includes

- Arithmetic and Logic Unit
- Instruction Decoder and Timing Generation Unit
- Accumulator
- B register and status register

8051 Internal Architecture

ARITHMETIC AND LOGIC UNIT

- The accumulator is an 8 bit register
- In arithmetic and logic operations, one of the operands is in ‘A’ register

INSTRUCTION DECODER AND CONTROL

- Decodes the instructions and establish the sequence of events to flow

TIMING GENERATION UNIT

- Synchronizes all the microcontroller operations with the clock
- Generates control signals necessary for communication between the microcontroller and peripherals

8051 Internal Architecture

CPU REGISTERS

Accumulator (E0 H) register :-

- The accumulator is an 8 bit register
- In arithmetic and logic operations, one of the operands is in ‘A’ register
- After the arithmetic and logic operations, the result is stored in A register.

B (F0 H) register :-

- 8 bit register used during multiply and divide operations
- In multiplication operation,the higher byte of the result is in ‘B’ register
- In division operation 8 bit divisor is in ‘B’ register and then remainder is stored in ‘B’ register

CPU Registers

Program Status Word (D0 H) (Flag Register)

- 8 bits wide, but only 6 bits of it are used
- remaining two unused bits are user-definable flags
- From the 6 bits, the 4 of them are *conditional flags*-
  - CY [carry]
  - AC [auxiliary carry]
  - P [Parity]
  - OV [overflow].
- other 2 bits are designated as RS0 and RS1, and are used to change the bank registers

FORMAT OF PSW

Bits of the Program Status Word Register:

CY	AC	F0	RS1	RS0	OV	--	P

CY	PSW.7	Carry Flag
AC	PSW.6	Auxiliary Carry Flag
----	PSW.5	Available to the user for general purpose
RS1	PSW.4	Register Bank Selector bit 1
RS0	PSW.3	Register Bank Selector bit 0
OV	PSW.2	Overflow Flag
----	PSW.1	User Definable bit
P	PSW.0	Parity Flag. Set / Cleared by hardware each instruction cycle to indicate an Odd / Even number of 1 bits in the accumulator

RS1	RS0	Register Bank	Address
0	0	0	00H - 07H
0	1	1	08H - 0FH
1	0	2	10H - 17H
1	1	3	18H - 1FH

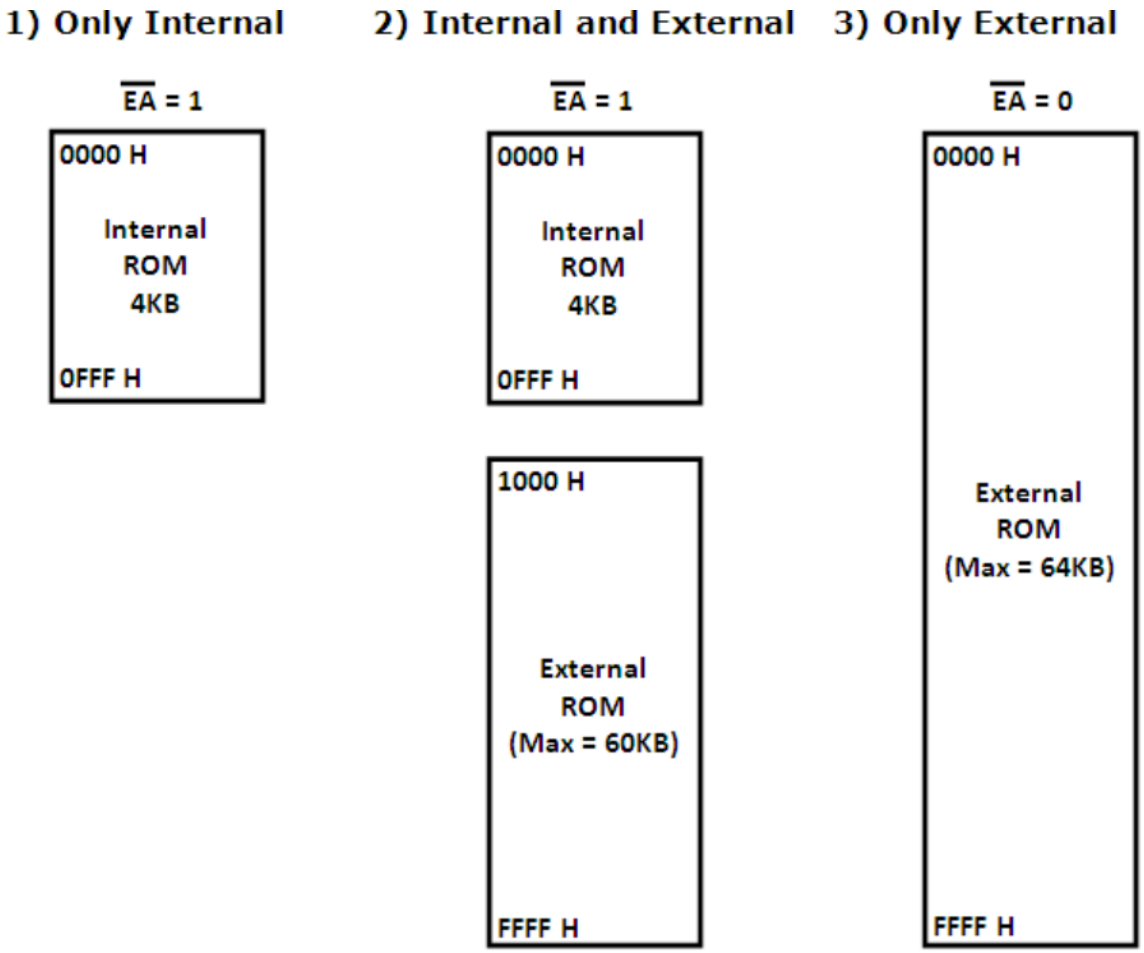
8051 MEMORY ORGANIZATION

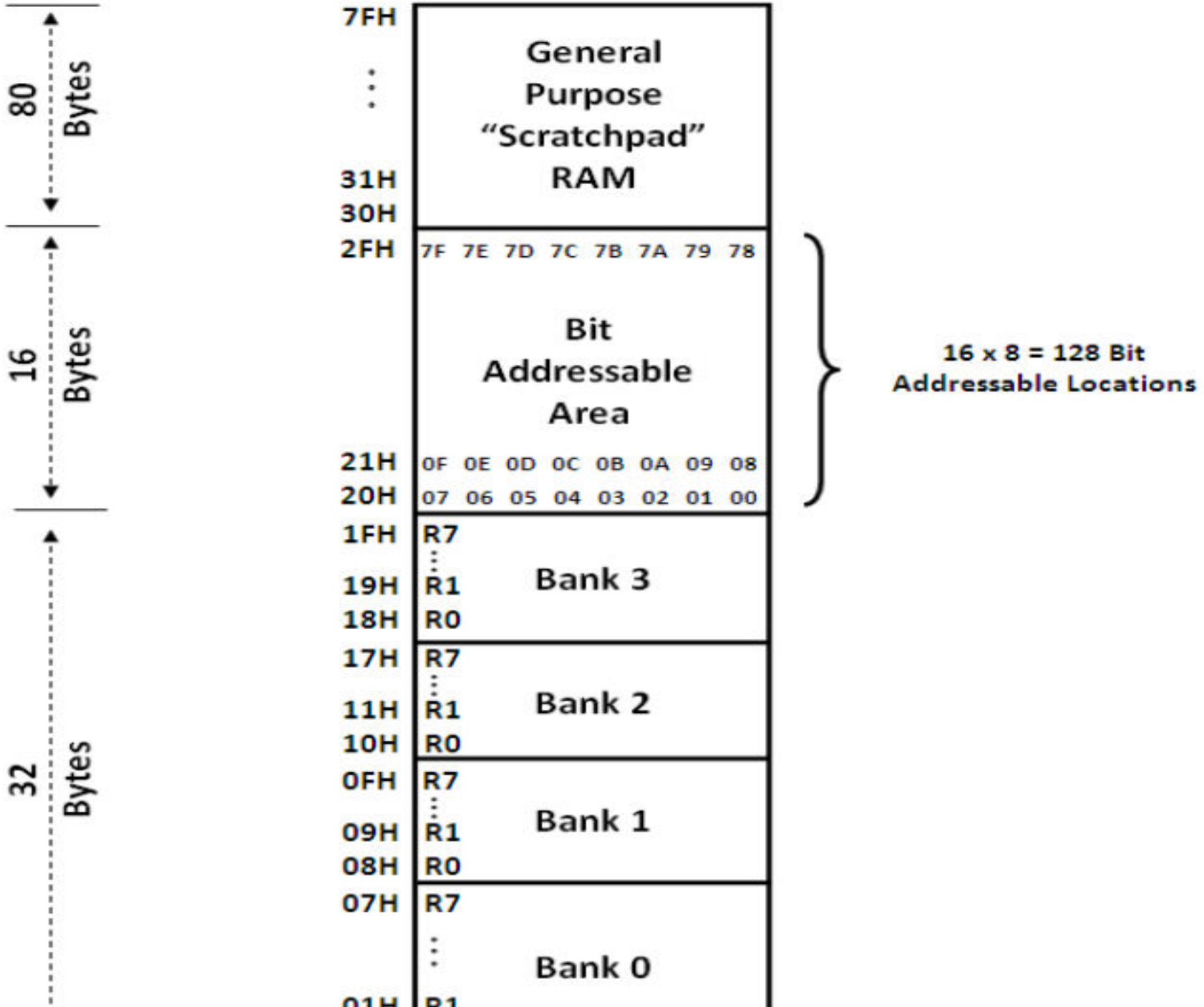
- divided into
  - Program Memory and
  - Data Memory
- Program Memory (ROM) is used for permanent saving program being executed
- Data Memory (RAM) is used for temporarily storing and keeping intermediate results and variables.

8051 PROGRAM MEMORY (ROM)

- Program Memory (ROM) is used for permanent saving program (CODE) being executed.
- 8051 memory organization allows external program memory to be added.
- **If EA=0** , the microcontroller completely ignores internal program memory and executes only the program stored in external memory.
- **If EA=1** In this case, the microcontroller executes first the program from built-in ROM, then the program stored in external memory.

8051 MEMORY ORGANIZATION




80 Bytes
16 Bytes
32 Bytes
7FH
General Purpose "Scratchpad" RAM
31H
30H
2FH
7F 7E 7D 7C 7B 7A 79 78
Bit Addressable Area
21H
0F 0E 0D 0C 0B 0A 09 08
20H
07 06 05 04 03 02 01 00
16 x 8 = 128 Bit Addressable Locations
1FH
R7
19H
R1
18H
R0
Bank 3
17H
R7
11H
R1
10H
R0
Bank 2
0FH
R7
09H
R1
08H
R0
Bank 1
07H
R7
Bank 0
01H
R1

Special Function Registers (SFRs of 8051)

	[illegible]	[illegible]	[illegible]	[illegible]
	TCON*	Timer/Counter Control	88H	8FH...88H
Used for Timer Control	TMOD	Timer/Counter Mode Control	89H	NA
	TL0	Timer 0 Low Byte	8AH	NA
	TL1	Timer 1 Low Byte	8BH	NA
	TH0	Timer 0 High Byte	8CH	NA
	TH1	Timer 1 High Byte	8DH	NA
Used for Interrupt Control	IE*	Interrupt Enable	0A8H	0AFH...0A8H
	IP*	Interrupt Priority	0B8H	0BFH...0B8H
Used for Power Control	PCON	Power Control	87H	NA

*Means the SFR is Bit Addressable

8051 STACK AND REGISTER BANKS

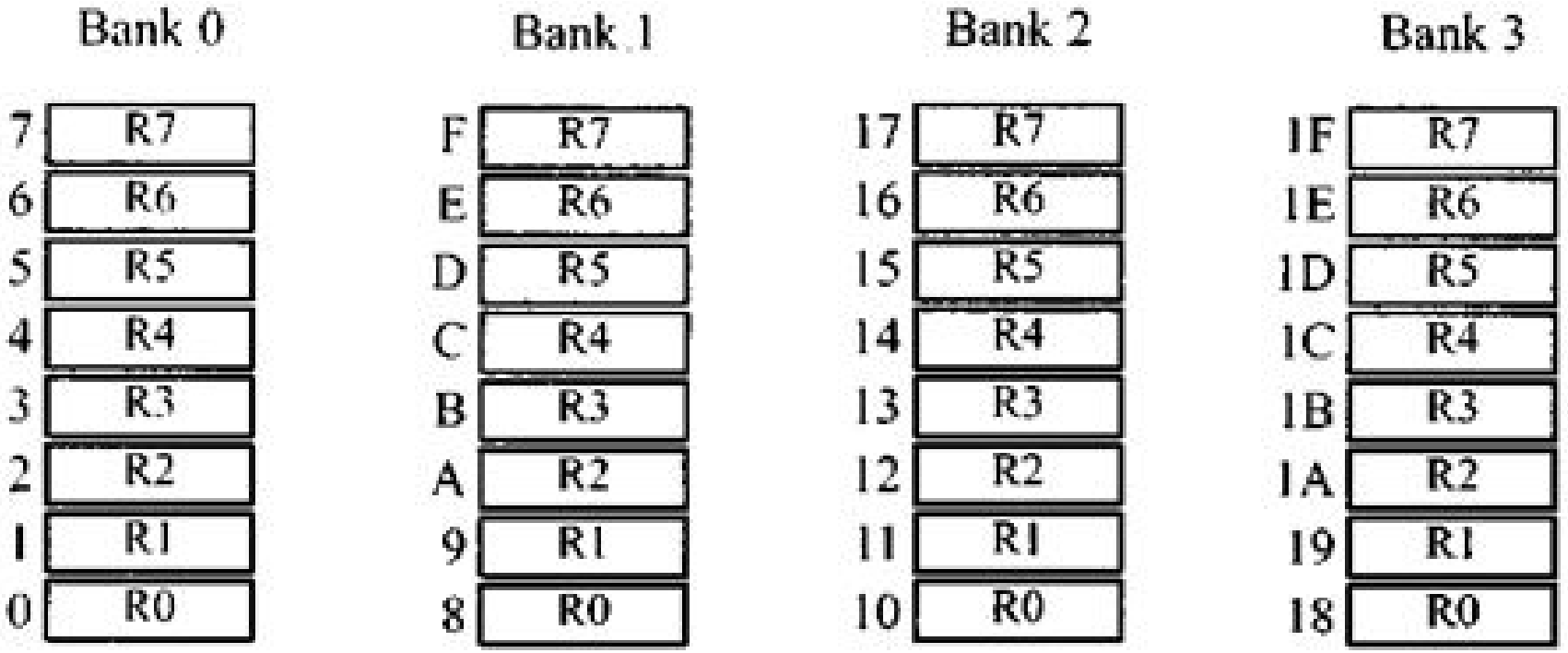
- 128 bytes of RAM in the 8051
- assigned addresses 00 to 7FH.
- The 128 bytes are divided into three different groups as follows.
  - **32 bytes from locations 00 to 1F** set aside for register banks and the stack.
  - **16 bytes from locations 20H to 2FH** set aside for bit addressable Read/Write memory.
  - **80 bytes from locations 30H to 7FH** are used for read and write storage. These 80 bytes locations of RAM are widely used for the purpose of storing data and parameters by 8051 programmers.

RAM ALLOCATION IN 8051

REGISTER BANKS IN THE 8051:

- 32 bytes of RAM are divided into 4 banks of registers in which each bank has 8 registers, R0 - R7.
- RAM locations from 0 to 7 are set aside for bank 0 of R0 - R7.
- Second bank of registers R0 - R7 starts at RAM location 08H and goes to location 0FH.
- Third bank of R0-R7 starts at memory location 10H and goes to location 17H.
- Fourth bank of R0-R7 starts at memory location 18H and goes to location 1FH.

REGISTER BANKS IN THE 8051:



STACK IN THE 8051

- stack is a section of RAM used by the CPU to store information temporarily.
- this information could be data or an address.
- the register used to access the stack is called the SP (stack pointer) register.
- the stack pointer in the 8051 is only 8 bits wide, which means that it can take values of 00 to FFH.
- When the 8051 is powered up, the SP register contains value 07.
- This means that RAM location 08 is the first location used for the stack by the 8051.

PUSHING ONTO THE STACK

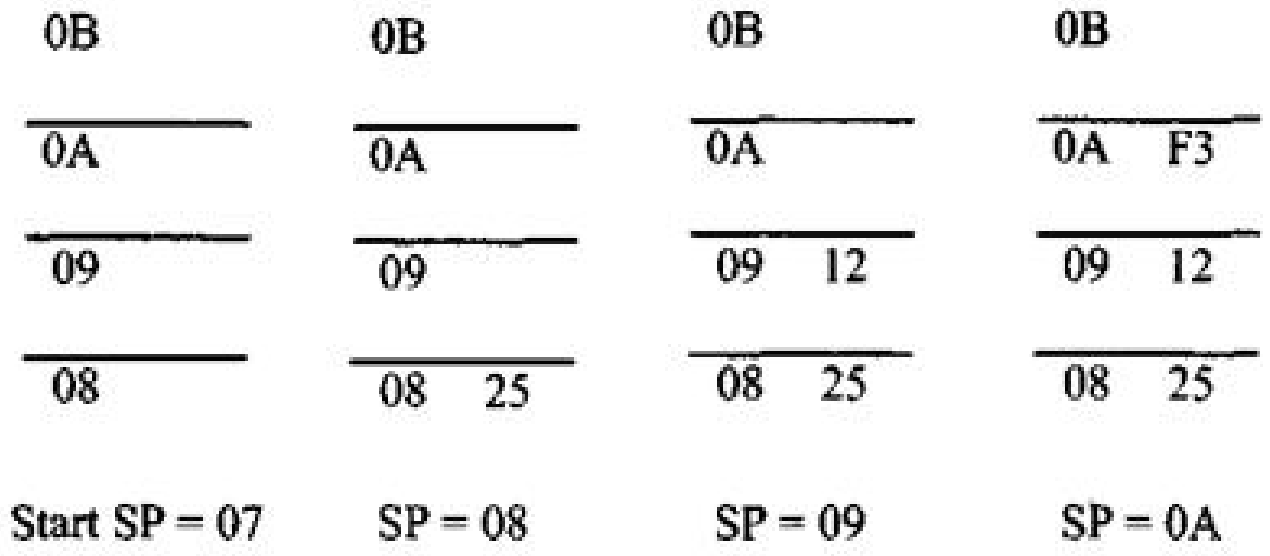
- the stack pointer (SP) points to the last used location of the stack.
- as data is pushed onto the stack, the stack pointer (SP) is incremented by one.
- as each PUSH is executed, the contents of the register are saved on the stack and SP is incremented by 1.
- to push the registers onto the stack their RAM addresses should be used.
- For example, the instruction “PUSH 1″ pushes register Rl onto the stack.

PUSHING ONTO THE STACK

Show the stack and stack pointer for the following. Assume the default stack area and register 0 is selected.

```
MOV   R6,#25H
MOV   R1,#12H
MOV   R4,#0F3H
PUSH  6
PUSH  1
PUSH  4
```

Solution:



POPPING FROM THE STACK

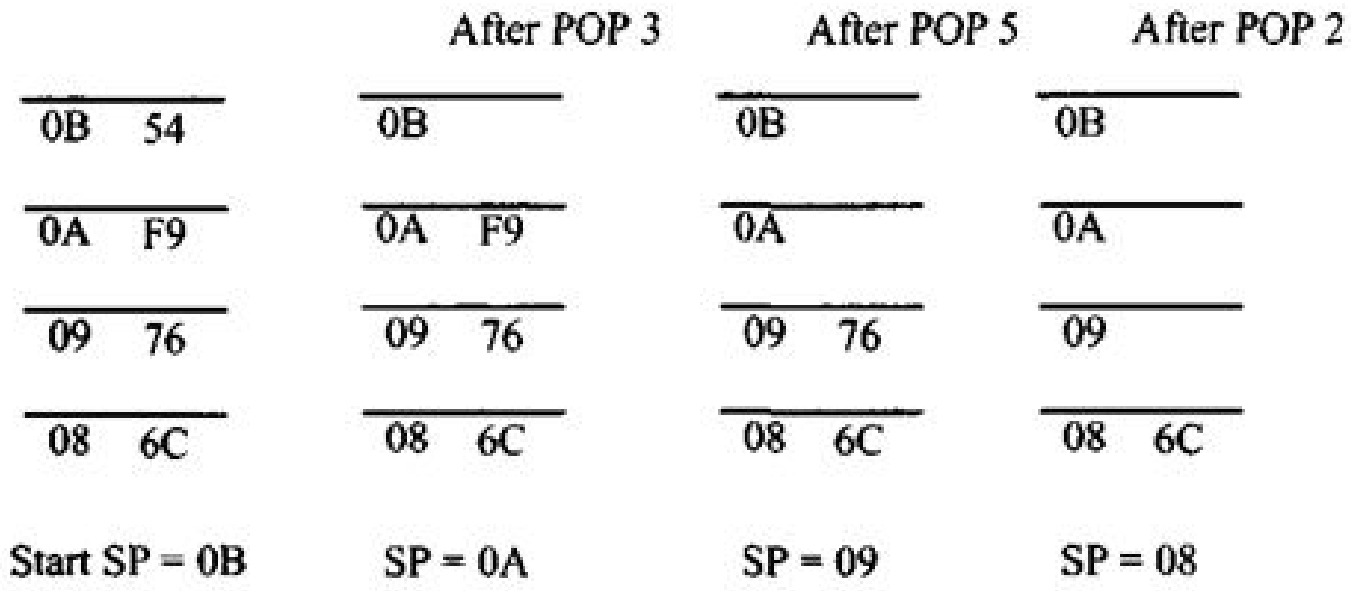
- Popping the contents of the stack back into a given register is the opposite process of pushing.
- With every pop, the top byte of the stack is copied to the register specified by the instruction and the stack pointer is decremented once

POPPING FROM THE STACK

Examining the stack, show the contents of the registers and SP after execution of the following instructions. All values are in hex.

```
POP   3     ;POP stack into R3
POP   5     ;POP stack into R5
POP   2     ;POP stack into R2
```

Solution:



8051 Interrupts

- **Interrupt Structure**: An interrupt is an external or internal event that disturbs the microcontroller to inform it that a device needs its service.
- The program which is associated with the interrupt is called the **interrupt service routine** (ISR) or **interrupt handler**.
- Upon receiving the interrupt signal the Microcontroller , finish current instruction and saves the PC on stack. Jumps to a fixed location in memory depending on type of interrupt Starts to execute the interrupt service routine until RETI (return from interrupt)
- Upon executing the RETI the microcontroller returns to the place where it was interrupted. Get pop PC from stack

8051 Interrupts

- The 8051 microcontroller has **FIVE interrupts in addition to Reset. They are**
  - Timer 0 overflow Interrupt (TF0)
  - Timer 1 overflow Interrupt (TF1)
  - External Interrupt 0 (INT0)
  - External Interrupt 1(INT1)
  - Serial Port events (buffer full, buffer empty, etc) Interrupt (R1=T1)

8051 Interrupts

- Each interrupt has a specific place in code memory where program execution (interrupt service routine) begins.
  - External Interrupt 0: 0003 H
  - Timer 0 overflow: 000B H
  - External Interrupt 1: 0013 H
  - Timer 1 overflow: 001B H
  - Serial Interrupt: 0023 H

  (Interrupt lists above in the decreasing order of priority)