Special Function Registers

S.No	Microprocessor	Microcontroller
1	Microprocessor acts as a heart of computer system.	Microcontroller acts as a heart of embedded system.
2	It is a processor in which memory and I/O output component is connected externally.	It is a controlling device in which memory and I/O output component is present internally.
3	Since memory and I/O output is to be connected externally. Therefore the circuit is more complex.	Since on chip memory and I/O output component is available. Therefore the circuit is less complex.
4	It cannot be used in compact system. Therefore microprocessor is inefficient.	It can be used in compact system. Therefore microcontroller is more efficient.
5	A microprocessor having a zero status flag.	A microcontroller has no zero flag.
6	It is mainly used in personal computers.	It is mainly used in washing machines, air conditioners etc.
7	It doesn't consist of RAM, ROM, I/O ports. It uses its pins to interface to peripheral devices.	It consists of CPU, RAM, ROM, I/O ports.
8	Its power consumption is high because it has to control the entire system.	It is built with CMOS technology, which requires less power to operate.
10	Microprocessors are used for big applications	Microcontrollers a10re used to execute a single task within an application.

Registers

- General purpose and special purpose registers
- General purpose register : Banks, bit addressable area, scratch pad memory
- Special purpose registers:

Special Function Registers (SFRs of 8051)

- 21 8-bit SFR's are there in 8051

	Name	Function	Byte Address	Bit Address
Used for holding data and status during Programming	A*	Accumulator	0E0H	0E7H...0E0H
	B*	Arithmetic	0F0H	0F7H...0F0H
	PSW*	Program Status Word	0D0H	0D7H...0D0H
Used in instructions to point to memory	SP	Stack Pointer	81H	NA
	DPL	Address External Memory	82H	NA
	DPH	Address External Memory	83H	NA
Used by the respective I/O Ports	P0*	I/O Port latch	80H	87H...80H
	P1*	I/O Port latch	90H	97H...90H
	P2*	I/O Port latch	0A0H	0A7H...0A0H
	P3*	I/O Port latch	0B0H	0B7H...0B0H
Used by the Serial Port	SCON*	Serial Port Control	98H	9FH...98H
	SBUF	Serial Port Data Buffer	99H	NA
Used for Timer Control	TCON*	Timer/Counter Control	88H	8FH...88H
	TMOD	Timer/Counter Mode Control	89H	NA
	TL0	Timer 0 Low Byte	8AH	NA
	TL1	Timer 1 Low Byte	8BH	NA
	TH0	Timer 0 High Byte	8CH	NA
	TH1	Timer 1 High Byte	8DH	NA
Used for Interrupt Control	IE*	Interrupt Enable	0A8H	0AFH...0A8H
	IP*	Interrupt Priority	0B8H	0BFH...0B8H
Used for Power Control	PCON	Power Control	87H	NA

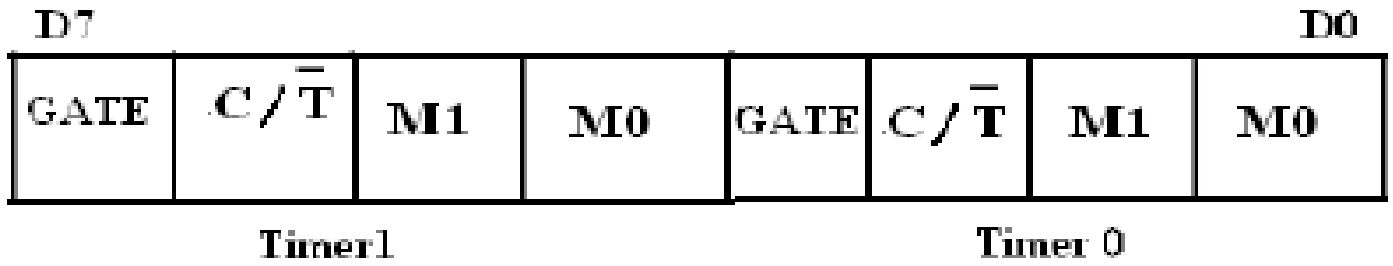
*Means the SFR is Bit Addressable

Timer Control Register(TCON)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0 (88H)
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

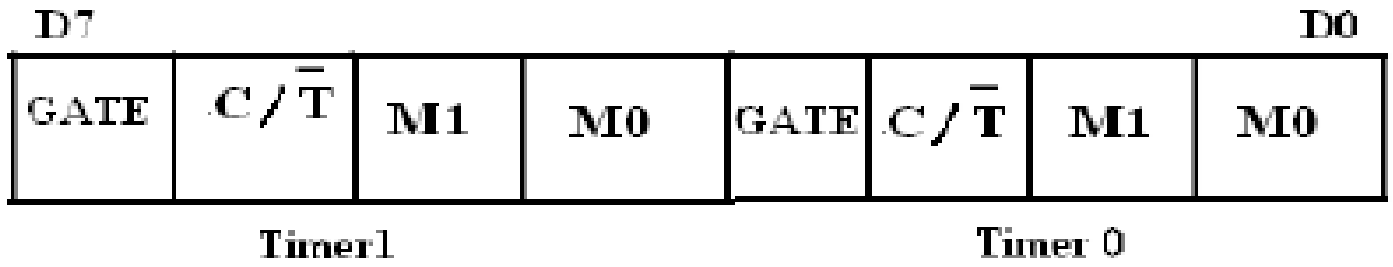
- **TF0/TF1:** Timer0/1 overflow flag is set when the timer/ counter overflows, reset by program
- **TR0/TR1:** Timer0/1 run control bit is set to start, reset to stop the timer0/1
- **IE0/IE1:** External Interrupt 0/1 edge detected flag: 1 is set when an external interrupt edge is detected.
- IT0/IT1 External **Interrupt Type (1: falling edge triggered, 0 low level triggered**)

Timer Mode Register(TMOD)



- GATE: This bit is used to start or stop the timers by hardware/software .When GATE= 1 ,the timers can be started / stopped by the external sources. When GATE= 0, the timers can be started or stopped by software instructions like SETB TR0 or SETB TR1
- C/T (counter/Timer) : C/T = 0 ,the Timer is used as delay generator and if C/T=1 the timer is used as an event counter.

Timer Mode Register(TMOD)



S.No	M0	M1	Mode	Operation
1	0	0	0	13-bit Timer mode 8-bit Timer/counter. THx with TLx as 5-bit prescalar
2	0	1	1	16-bit Timer mode.16-bit timer /counter without pre-scalar
3	1	0	2	8-bit auto reload. THx contains a value that is to be loaded into TLx each time it overflows
4	1	1	3	Split timer mode

PCON (Power Control Register)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SMOD	--	--	--	GF1	GF2	PD	IDL

- SMOD(serial mode) 1= high baud rate, 0 = low baud rate
- GF1, GF2 flags for free use
- PD: 1= power down mode for CMOS
- IDL: 1= idle mode.
- In **Power Down** mode, the oscillator clock provided to system is OFF i.e. CPU and peripherals clock remains inactive in this mode.
- In **Idle** Mode, only the clock provided to CPU gets deactivated ,whereas peripherals clock will remain active in this mode.
- Hence power saved in power down mode is more than in idle mode.

SCON (Serial Port Control Register)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

- **REN:** Receiver enable is set/reset by program
- **TB8:** This selects 9th bit that will be transmitted in mode2 and mode3
- **RB8:** In mode 2 ,3 this is the 9th data bit that was received.
- **TI:** Transmit Interrupt is set at the end of 8th bit (mode 0)
  or at the stop bit (other modes) indicating the completion
  of one byte transmission, reset by program
- **RI:** Receive Interrupt is set at the end of 8th bit (mode 0)
  or at the stop bit (other modes) indicating the completion
  of one byte receiving, reset by program
- RI and TI flag in SCON SFR are used to detect the interrupt events.

If **RI = 1** then a byte is received at the RxD pin. If **TI = 1** then a byte is

- transmitted from the TxD pin.
- **SM2-**This enables multiprocessor commn feature in mode2 and mode3.

SCON (Serial Port Control Register)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

SM0	SM1	Serial Mode	Baud Rate	Device
0	0	0 (Sync.) half duplex,	Oscillator/12 (fixed)	8-bit shift register
0	1	1(Async) full duplex	Set by Timer 1	8-bit UART
1	0	2(Sync) half duplex	Oscillator/64 (fixed)	9-bit UART
1	1	3(Async) full duplex	Set by Timer 1	9-bit UART

Interrupt Enable Register (IE)

EA	——	ET2	ES	ET1	EX1	ET0	EX0

- EA : Global enable/disable. To enable the interrupts this bit must be set High.
- Undefined-reserved for future use.
- ET2 : Enable /disable Timer 2 overflow interrupt.
- ES : Enable/disable Serial port interrupt.
- ET1 : Enable /disable Timer 1 overflow interrupt.
- EX1 : Enable/disable External interrupt1.
- ET0 : Enable /disable Timer 0 overflow interrupt.
- EX0 : Enable/disable External interrupt 2

Interrupt Priority Register (IP)

—	—	PT2	PS	PT1	PX1	PT0	PX0

- IP.7: reserved
- IP.6: reserved
- IP.5: Timer 2 interrupt priority bit (8052 only)
- IP.4: Serial port interrupt priority bit
- IP.3: Timer 1 interrupt priority bit
- IP.2: External interrupt 1 priority bit
- IP.1: Timer 0 interrupt priority bit
- IP.0: External interrupt 0 priority bit

TIMER 0 and TIMER 1