MEMORY INTERFACING

Interfacing Memory

Static Memory Interfacing

The semiconductor memories are organised as two dimensional arrays of memory locations.

• For example 4K * 8 or 4K byte memory contains 4096 locations, where each locations contains 8-bit data and only one of the 4096 locations can be selected at a time. Once a location is selected all the bits in it are accessible using a group of conductors called Data bus.

• For addressing the 4K bytes of memory, 12 address lines are required.

• In general to address a memory location out of N memory locations, will require at least n bits of address, i.e. n address lines where $n = \text{Log}_2 N$.

• Thus if the microprocessor has n address lines, then it is able to address at the most N locations of memory, where $2^n = N$.

- If out of N locations only P memory locations are to be interfaced, then the least significant p address lines out of the available n lines can be directly connected from the microprocessor to the memory chip while the remaining (n-p) higher order address lines may be used for address decoding as inputs to the chip selection logic.
- The memory address depends upon the hardware circuit used for decoding the chip select (CS). The output of the decoding circuit is connected with the CS pin of the memory chip.

The general procedure of static memory interfacing with 8086

1. Arrange the available memory chips so as to obtain 16-bit data bus width.

The upper 8-bit bank is called ‘odd address memory bank’ and the lower 8-bit bank is called ‘even address memory bank’.

2. Connect available memory address lines of memory chips with those of the microprocessor and also connect the memory RD and WR inputs to the corresponding processor control signals. Connect the 16-bit data bus of the memory bank with that of the microprocessor 8086.

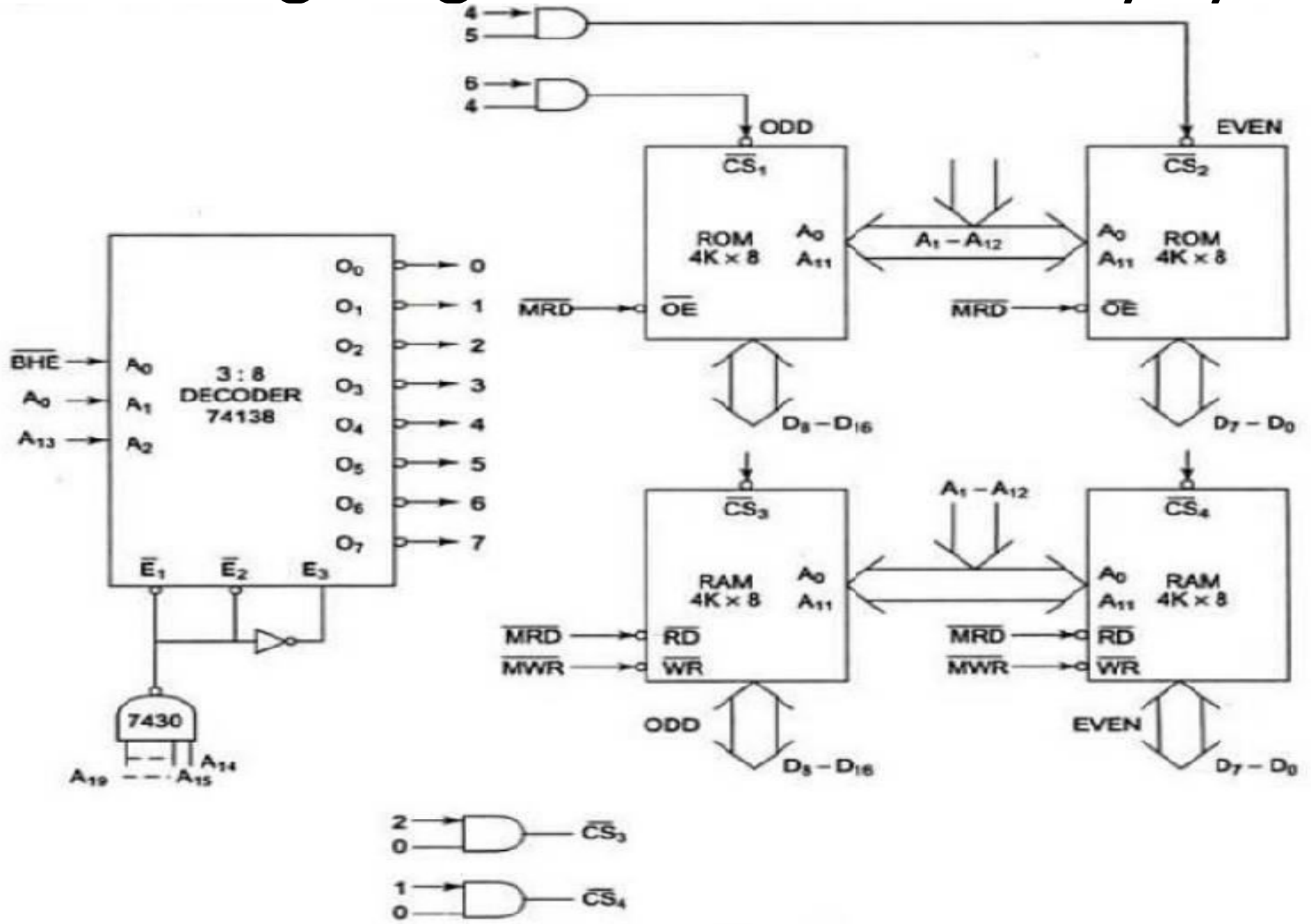
3. The remaining address lines of the microprocessor, BHE and Ao are used for decoding the required chip select signals for the odd and even memory banks. The CS of memory is derived from the output of the decoding circuit.

4. As a good and efficient interfacing practice, the address map of the system should be continuous as far as possible

Interface two 4Kx8 EPROMS and two 4Kx8 RAM chips with 8086. select suitable maps.

Address	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_{09}	A_{08}	A_{07}	A_{06}	A_{05}	A_{04}	A_{03}	A_{02}	A_{01}	A_{00}
FFFFFH	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
						EPROM							8K × 8							
FE000H	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
FDFFFH	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
						RAM						8K × 8								
FC000H	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Interfacing diagram for the memory system



- The memory system in this example contains in total four 4Kx8 memory chip.
- The two 4Kx8 chips of RAM and ROM are arranged in parallel to obtain 16-bit data bus width. Ao is 0, i.e. the address is even and is in RAM, then the lower RAM chip is selected indicating 8-bit transfer at an even address.
- If Ao is 1, i.e. the address is odd and is in RAM, the BHE goes low, the upper RAM chip is selected, further indicating that the 8-bit transfer is at an odd address.

The selection of chips takes place as shown in table.

Memory Chip Selection Table:

Decoder I/P --> Address/$\overline{BHE}$ -->	A2 A13	A1 A0	A0 $\overline{BHE}$	Selection/ Comment
Word transfer on D0 - D15	0	0	0	Even and odd address in RAM
Byte transfer on D7 - D0	0	0	1	Only even address in RAM
Byte transfer on D8 - D15	0	1	0	Only odd address in RAM
Word transfer on D0 - D15	1	0	0	Even and odd address in RAM
Byte transfer on D7 - D0	1	0	1	Only even address in RAM
Byte transfer on D8 - D15	1	1	0	Only odd address in ROM

2) Design an 8086 based system having 32K EPROM using 16 kb chips & 128K RAM using 32K chips

3)Design an interface between 8086 CPU and two chips of 16K×8 EPROM and two chips of 32K×8 RAM. Select the starting address of EPROM suitably. The RAM address must start at 00000 H.

2) Design an 8086 based system having 32K EPROM using 16 kb chips & 128K RAM using 32K chips. The RAM address must start at 00000H

Memory Calculations:

EPORM:

Required = 32 KB, Available = 16 KB

No. of chips = 2 chips.

Starting address of EPROM is calculated as:

FFFFFH – (Space required by total EPROM of 32 KB)

```
  F F F F F H
-   7 F F F H
  F 8 0 0 0 H
```

Size of a single EPROM chip = 16 KB

$= 16 \times 1KB = 2^4 \times 2^{10}$
$= 2^{14}$
= 14 address lines

= **(A 14 ... A1)**

RAM:

Required = 128 KB, Available = 32 KB

No. of chips = 4 chips.

Starting address of RAM is: 00000H

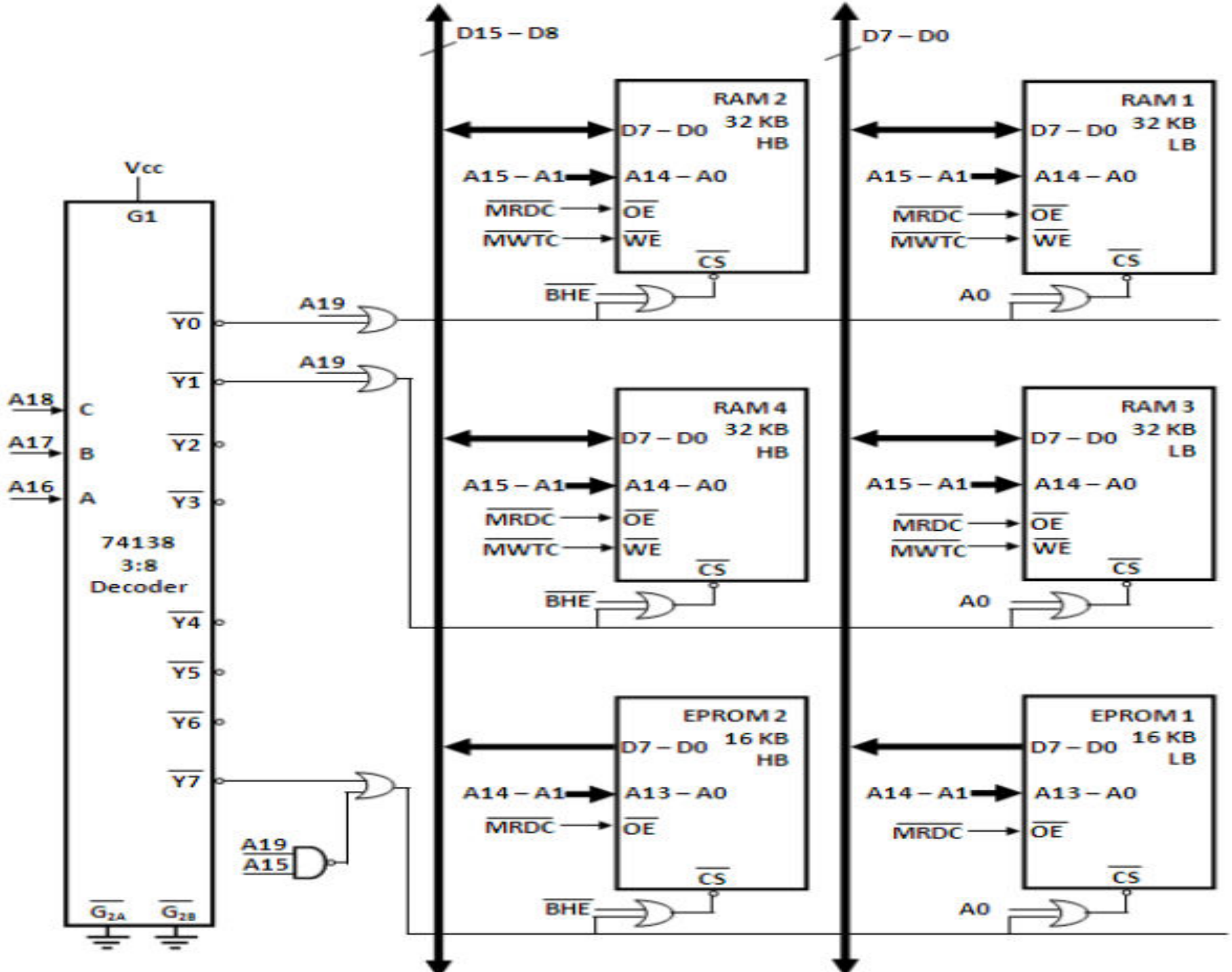
Size of a single RAM chip = 32 KB

$= 32 \times 1\ KB = 2^5 \times 2^{10}$
$= 2^{15}$
= 15 address lines

= **(A15 ... A1)**

MEMORY MAP

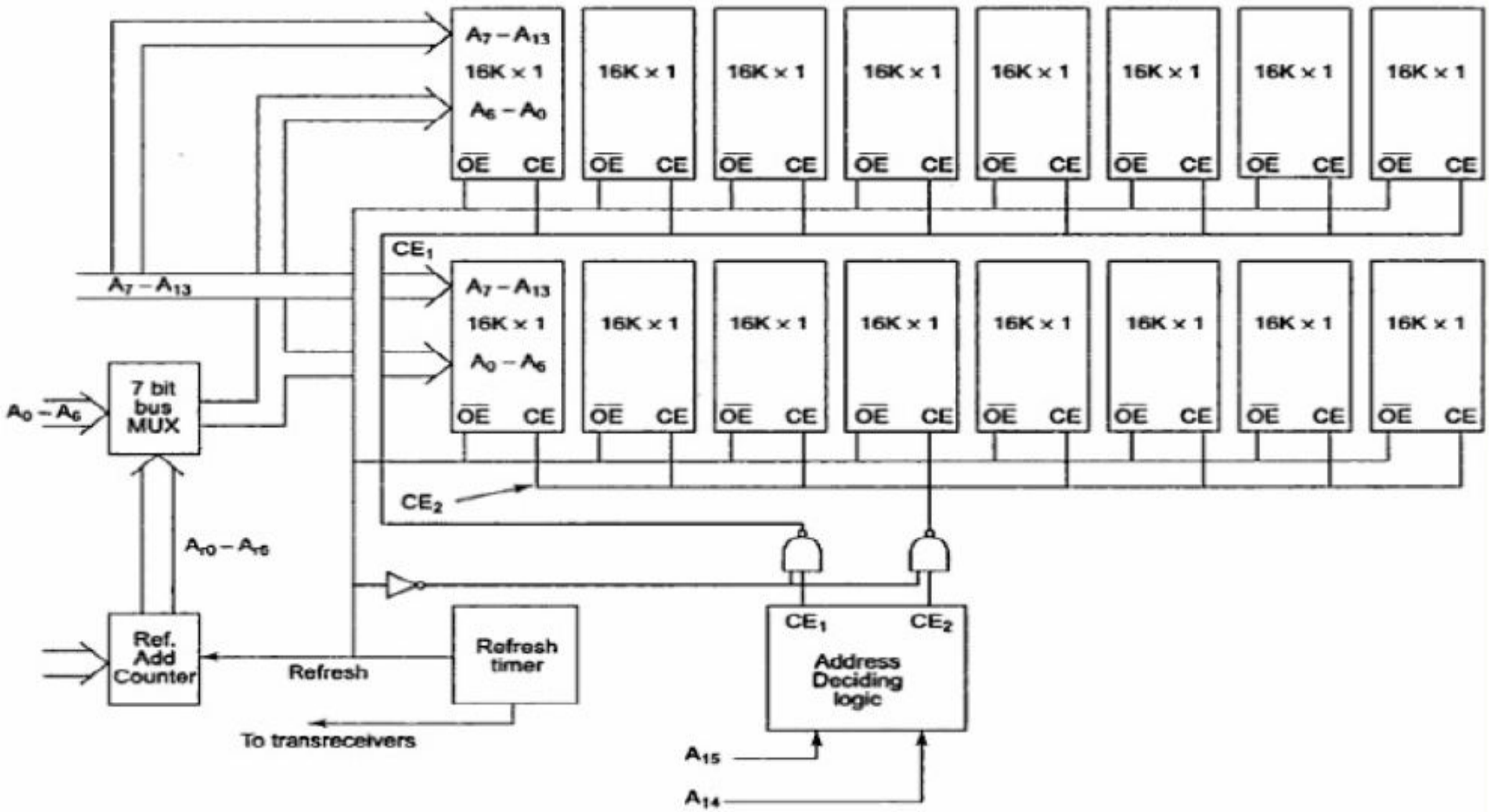
Memory Chip	Address Bus																				Memory Address
	A19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	A0	
RAM 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00000H
(LB)	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0FFFEH
RAM 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	00001H
(HB)	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0FFFFH
RAM 3	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10000H
(LB)	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1FFFEH
RAM 4	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	10001H
(HB)	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFFFH
EPORM 1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F8000H
(LB)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	FFFFEH
EPORM 2	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	F8001H
(HB)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFFFH


D15 – D8
D7 – D0
RAM 2
32 KB
HB
RAM 1
32 KB
LB
RAM 4
32 KB
HB
RAM 3
32 KB
LB
EPROM 2
16 KB
HB
EPROM 1
16 KB
LB
D7 – D0
A15 – A1
A14 – A0
A14 – A1
A13 – A0
MRDC
MWTC
OE
WE
CS
BHE
A0
Vcc
G1
A18
A17
A16
C
B
A
74138
3:8
Decoder
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
A19
A15
G2A
G2B

Dynamic RAM Interfacing

- The basic Dynamic RAM cell uses a capacitor to store the charge as a representation of data. This capacitor is manufactured as a diode that is reverse-biased so that the storage capacitance comes into the picture.
- This storage capacitance is utilized for storing the charge representation of data.
- The reverse-biased diode has a leakage current that tends to discharge the capacitor giving rise to the possibility of data loss.
- To avoid this possible data loss, the data stored in a dynamic RAM cell must be refreshed after a fixed time interval reguraly.
- The process of refreshing the data in the RAM is known as refresh cycle.
- During this refresh period all other operations (accesses) related to the memory subsystem are suspended.

- The advantages of dynamic RAM. Like low power consumption, higher packaging density and low cost, most of the advanced computer systems are designed using dynamic RAMs.
- Also the refresh mechanism and the additional hardware required makes the interfacing hardware, in case of dynamic RAM, more complicated


A7 – A13
16K × 1
A6 – A0
OE
CE
CE1
A0 – A6
7 bit bus MUX
A10 – A16
CE2
Ref. Add Counter
Refresh
Refresh timer
To transreceivers
Address Deciding logic
A15
A14

- Generally dynamic RAM is available in units of several Kilobits to even Megabits of memory.
- This memory is arranged internally in a two dimensional matrix array so that it will have n rows and m columns.
- The diagram shown in figure explains the refreshing logic and 8086 interfacing with dynamic RAM.
- Each of the used chips 16K * 1-bit Dynamic RAM cell array.
- The system contains two 16 Kbytes Dynamic RAM units.
- All the address and the data lines are assumed to be available from an 8086 microprocessor system.
- The OE pin controls output data buffers of the memory chip.
- The CE pins are active high chip select of memory chips.
- The refresh cycle starts, if the refresh output of the refresh timer goes high. OE and CE tends to be high
- The high CE enables the memory chip for refreshing .

I/O Interfacing Techniques

- Input/output devices can be interfaced with microprocessor systems in two ways :

  1. I/O mapped I/O
  2. Memory mapped I/O

- **1. I/O mapped I/O :**
- The devices are viewed as distinct I/O devices and are addressed accordingly
- All the available address lines are not used for interfacing
- The I/O mapped device requires IN and OUT instructions for accessing them
- Requires less hardware for decoding as less no: of address lines used
- Max of 64k input and 64K output devices or 32K input and 32K output devices can be interfaced
- In addition to data and address buses to address device, IORD and IOWR signals are used for I/O mapped interfacing

- **. Memory mapped I/O**
- The devices are viewed as memory locations and are addressed likewise
- In this type of I/O interfacing, the 8086 uses 20 address lines to identify an I/O device.
- Can have 1M memory-mapped input and output devices
- MRDC and MRTC signals are used for interfacing in memory-mapped I/O scheme
- All the applicable data transfer instructions can be can be used to communicate with memory-mapped I/O devices
- Complex decoding hardware is required