Module 3

PROGRAMMABLE INTERRUPT CONTROLLER (PIC) 8259A

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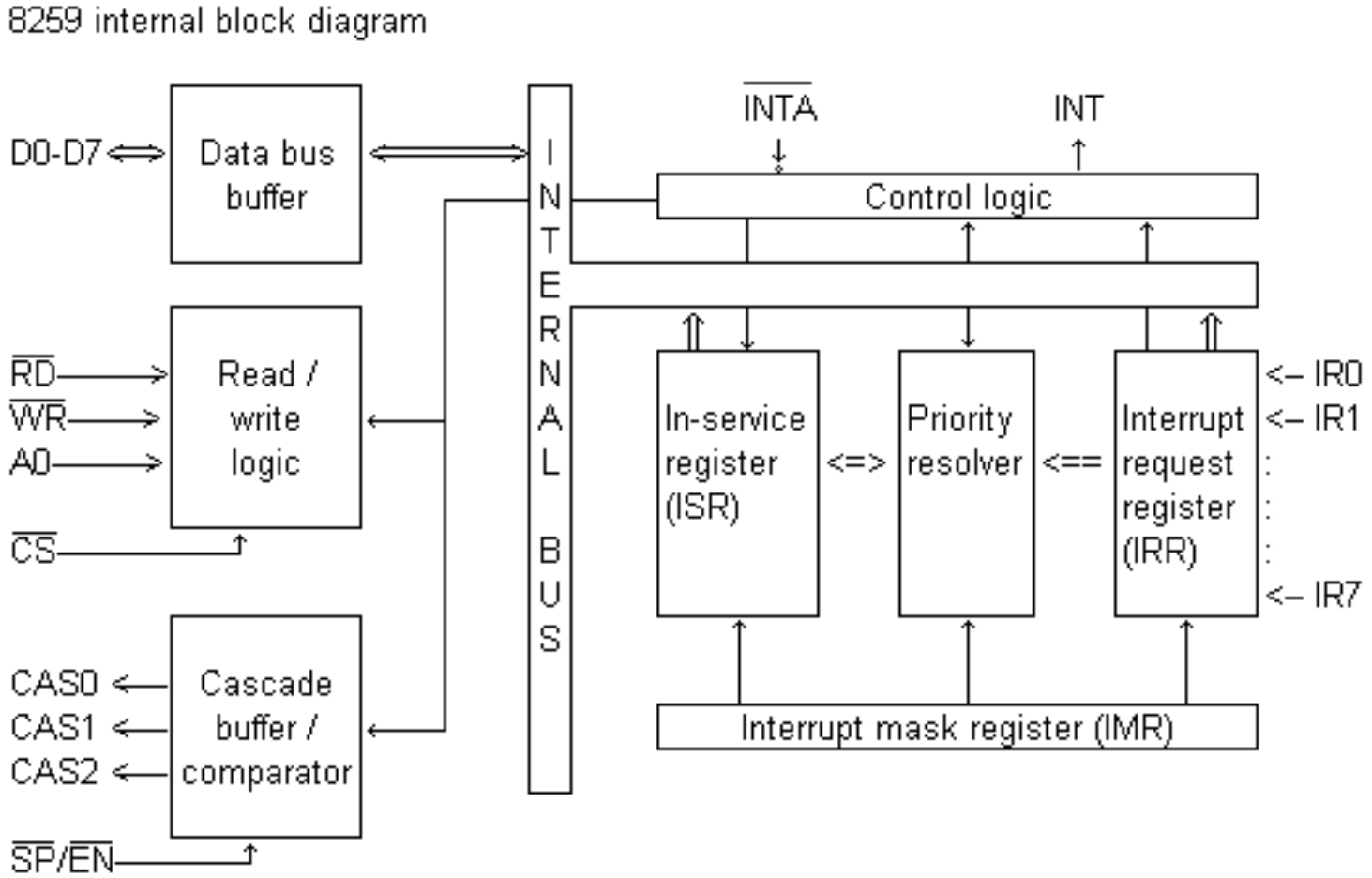


Interrupt Request Register (IRR): The interrupts at IRQ input lines are handled by Interrupt Request Register internally. IRR stores all the interrupt request in it in order to serve them one by one on the priority basis.

In-Service Register (ISR): This stores all the interrupt requests those are being served, i.e. ISR keeps trackof the requests being served

Priority Resolver : This unit determines the priorities of the interrupt requests appearing simultaneously. The highest priority is selected and stored into the corresponding bit of ISR during INTA pulse. The IR0 has the highest priority while the IR7 has the lowest one, normally in fixed priority mode. The priorities however may be altered by programming the 8259A in rotating priority mode.

Interrupt Mask Register (IMR) : This register stores the bits required to mask the interrupt inputs. IMR operates on IRR at the direction of the Priority Resolver.

- **Interrupt Control Logic** : This block manages the interrupt and interrupt acknowledge signals to be sent to the CPU for serving one of the eight interrupt requests. This also accepts the interrupt acknowledge (INTA) signal from CPU that causes the 8259A to release vector address on to the data bus.
- **Data Bus Buffer** : This tristate bidirectional buffer interfaces internal 8259A bus to the microprocessor system data bus. Control words, status and vector information pass through data buffer during read or write operations.

Read/Write Control Logic : This circuit accepts and decodes commands from the CPU. This block also allows the status of the 8259A to be transferred on to the data bus.

Cascade Buffer/Comparator : This block stores and compares the ID's of all the 8259A used in system. The three I/O pins CASO-CAS2 are outputs when the 8259A is used as a master. The same pins act as inputs when the 8259A is in slave mode. The 8259A in master mode sends the ID of the interrupting slave device on these lines. The slave thus selected, will send its preprogrammed vector address on the data bus during the next INTA pulse.

Interrupt Sequence in an 8086 system

One or more IR lines are raised high that set corresponding IRR bits

2. 8259A resolves priority and sends an INT signal to CPU
3. The CPU acknowledge with INTA pulse.
4. Upon receiving an INTA signal from the CPU, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive data during this period
5. The 8086 will initiate a second INTA pulse. During this period 8259A releases an 8-bit pointer on to a data bus from where it is read by the CPU
6. This completes the interrupt cycle. The ISR bit is reset at the end of the second INTA pulse if automatic end of interrupt (AEOI) mode is programmed. Otherwise ISR bit remains set until an appropriate EOI command is issued at the end of interrupt subroutine

Programming of 8259

- 8259A has two types of command words, initialization(ICWs) and operational control word(OCWs)

i. Initialization command word:

   a. ICW1 for chip (8259A) control

   b. ICW2 for type

   c. ICW3 for status control

   d. ICW4 for mode control

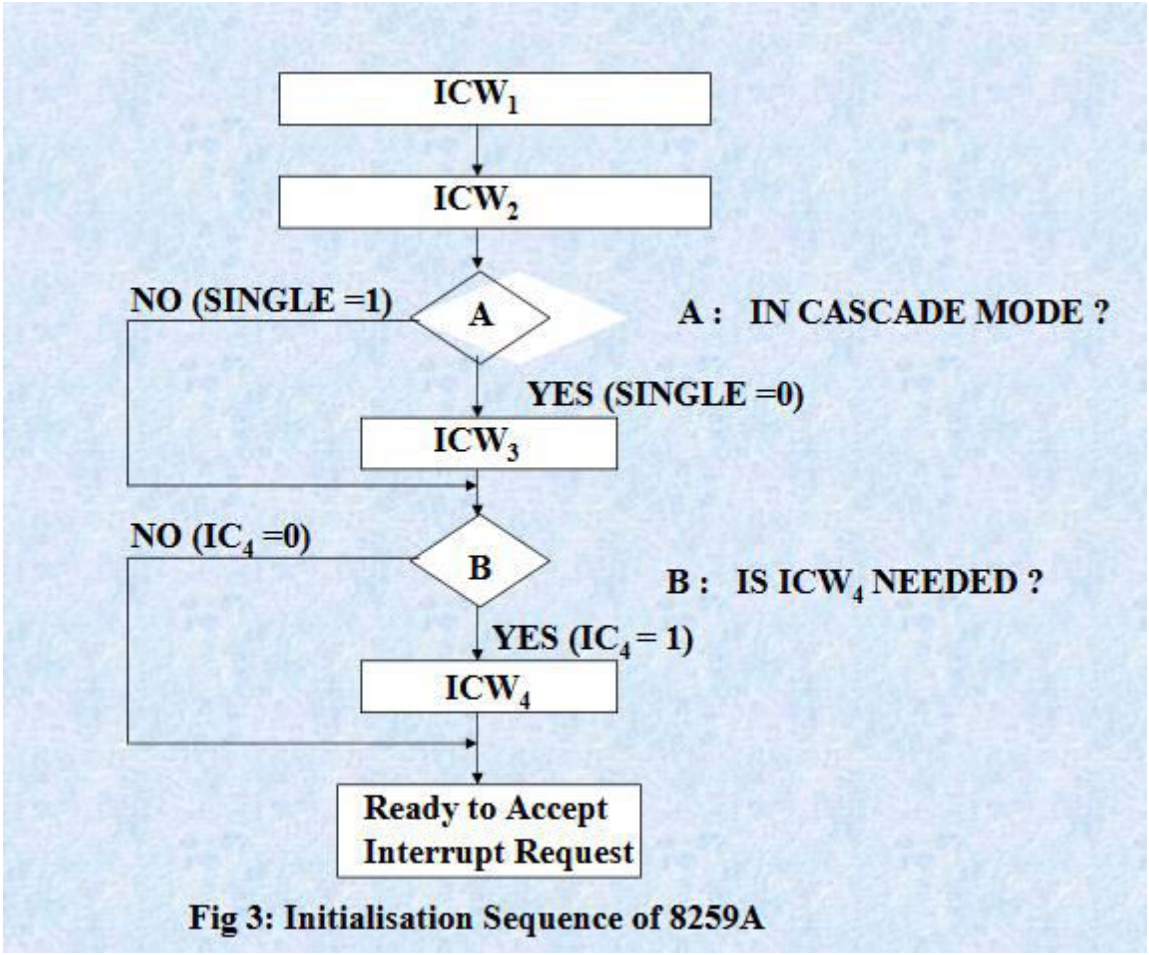


Fig 3: Initialisation Sequence of 8259A

Initialization command word

ICW1

- Control bits for edge/level triggered mode , single/cascade mode , call address interval and whether ICW4 is required or not needed

ICW2

- Stored details regarding interrupt vector addresses

Initialization command word

ICW3

- Used in cascaded mode

ICW4

- Used for mode control

ICW1

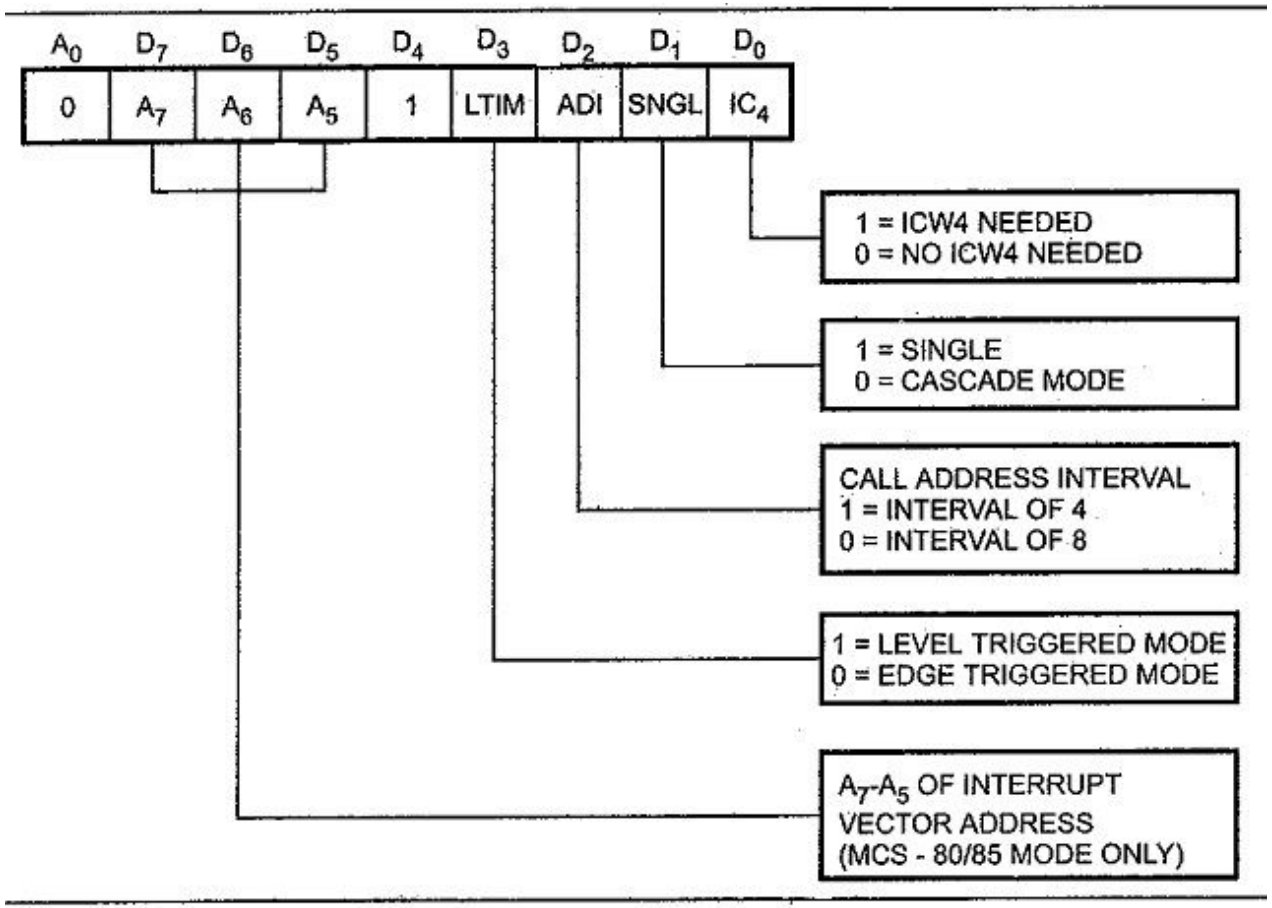


Fig. 14.76 Initialization command word 1 (ICW1)

ICW2, ICW3(master)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_{15}/T_2	A_{14}/T_6	A_{13}/T_5	A_{12}/T_4	A_{11}/T_3	A_{10}	A_9	A_8

a) The format of ICW3 to be issued to master 8259A is,

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

ICW3(Slave)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	0	ID_2	ID_1	ID_0	Slave Device
					0	0	0	0
					0	0	1	1
					0	1	0	2
					0	1	1	3
					1	0	0	4
					1	0	1	5
					1	1	0	6
					1	1	1	7

ICW4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	SFNM	BUF	MS	AEOI	μPM

Operation Command words

- Modes of operations can be selected by programming, i.e. writing three internal registers called as operation command Words
- In the three operation command words OCW 1, OCW2 and OCW3 every bit corresponds to some operational feature of the mode selected, except for a few bits those are either 1 or 0.

OCW1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0

OCW2

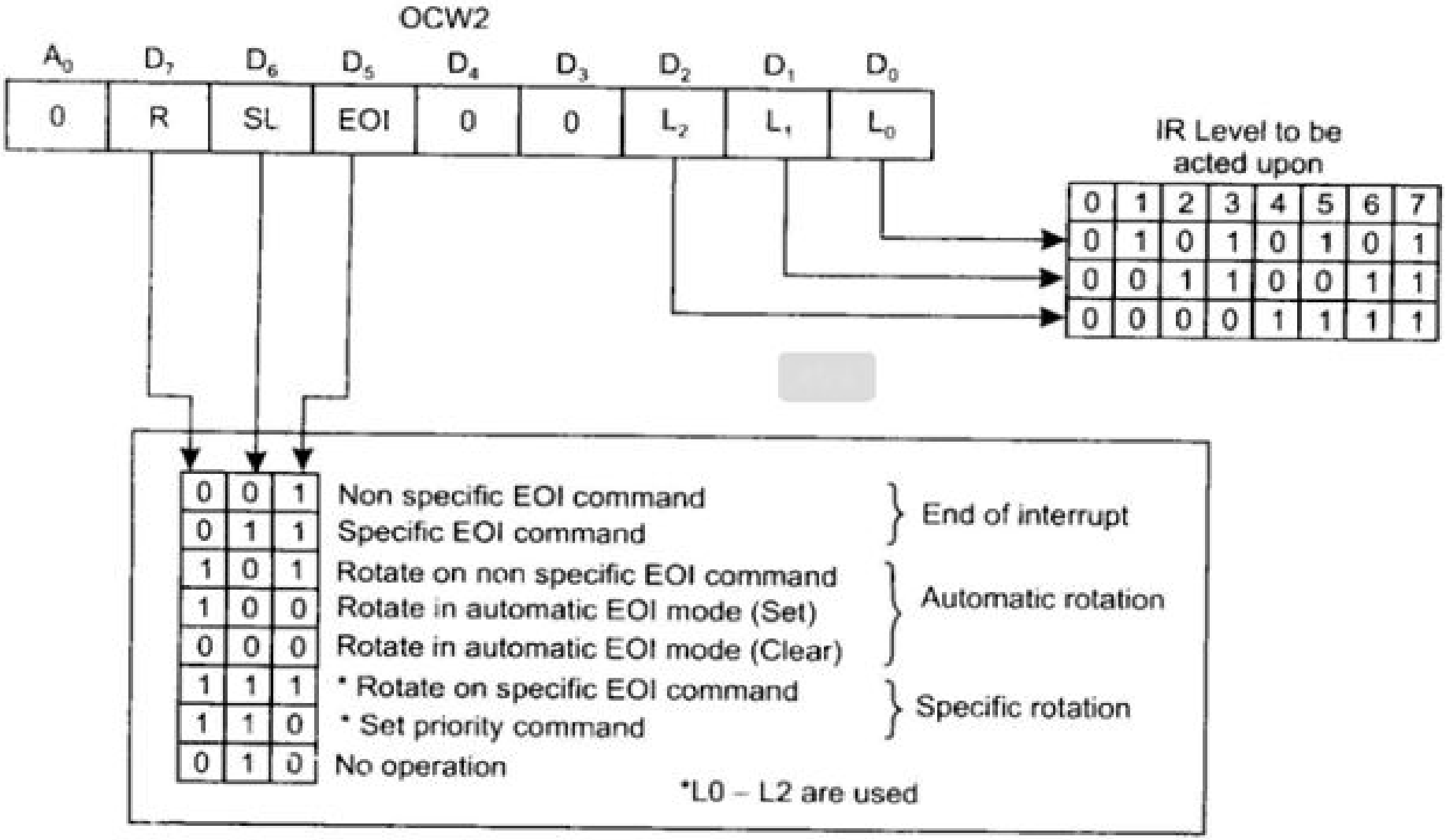


Fig. 9e.13: Format of operation command word 2
(*Source:* Intel Corporation)

OCW3

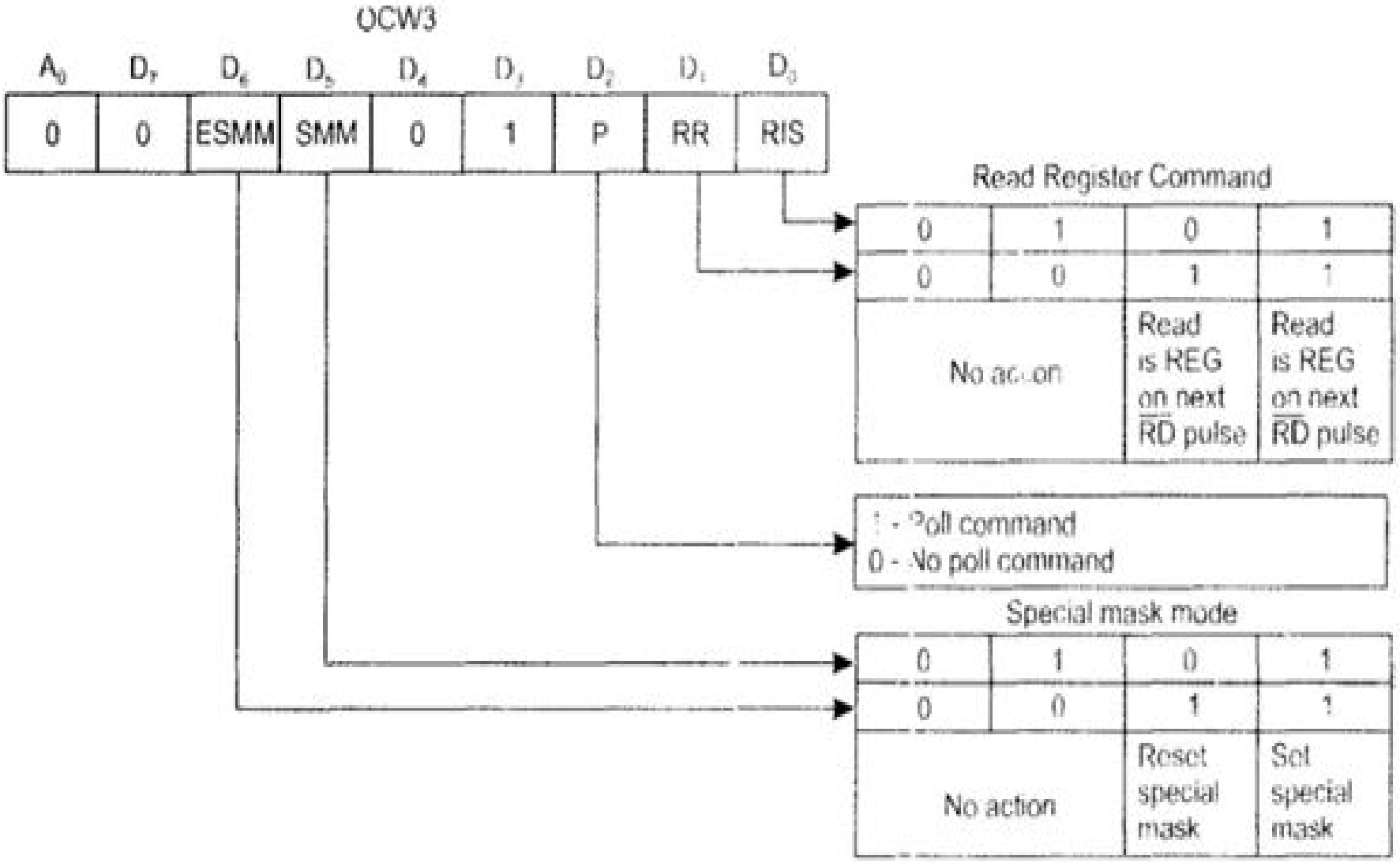
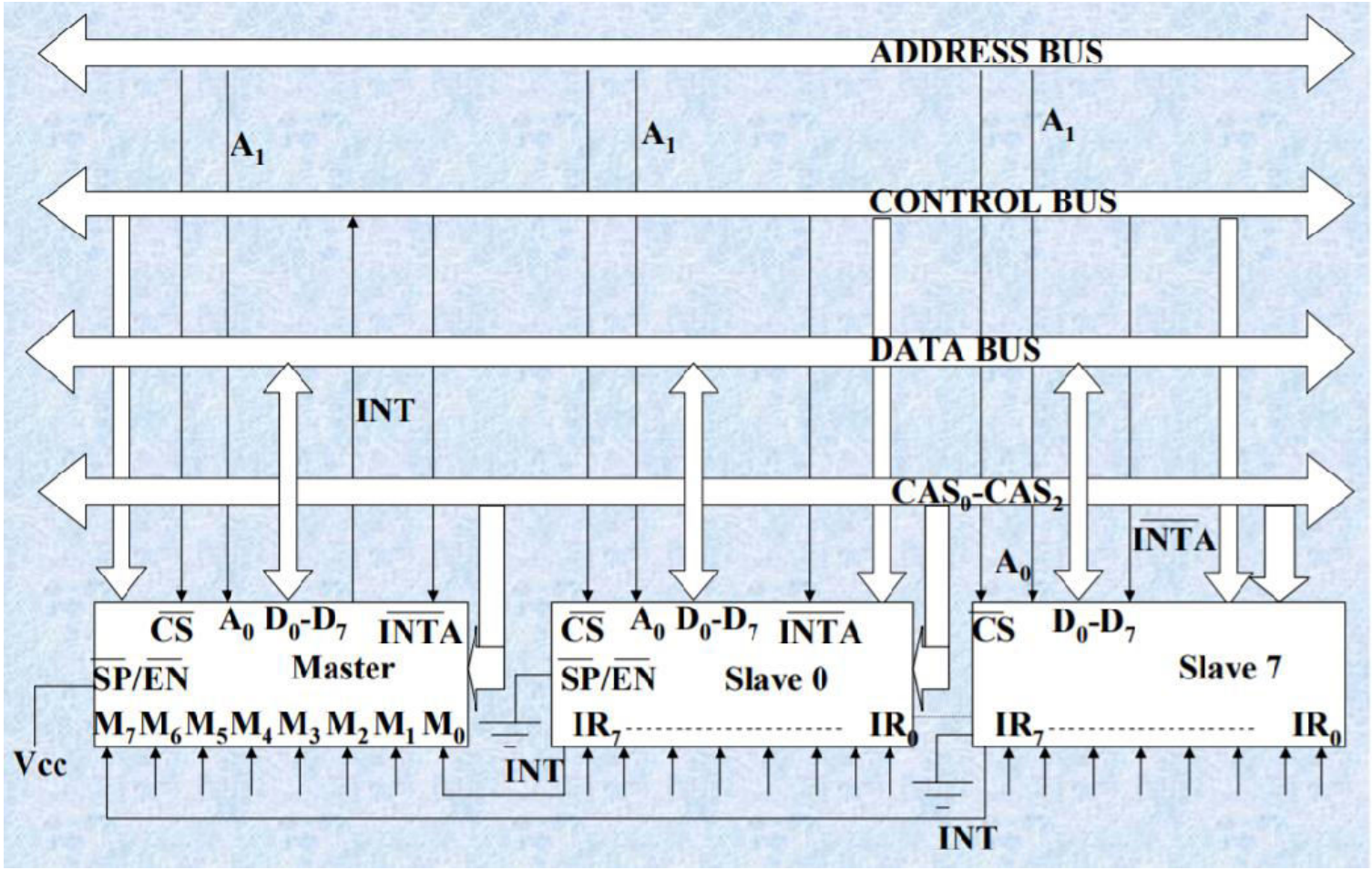
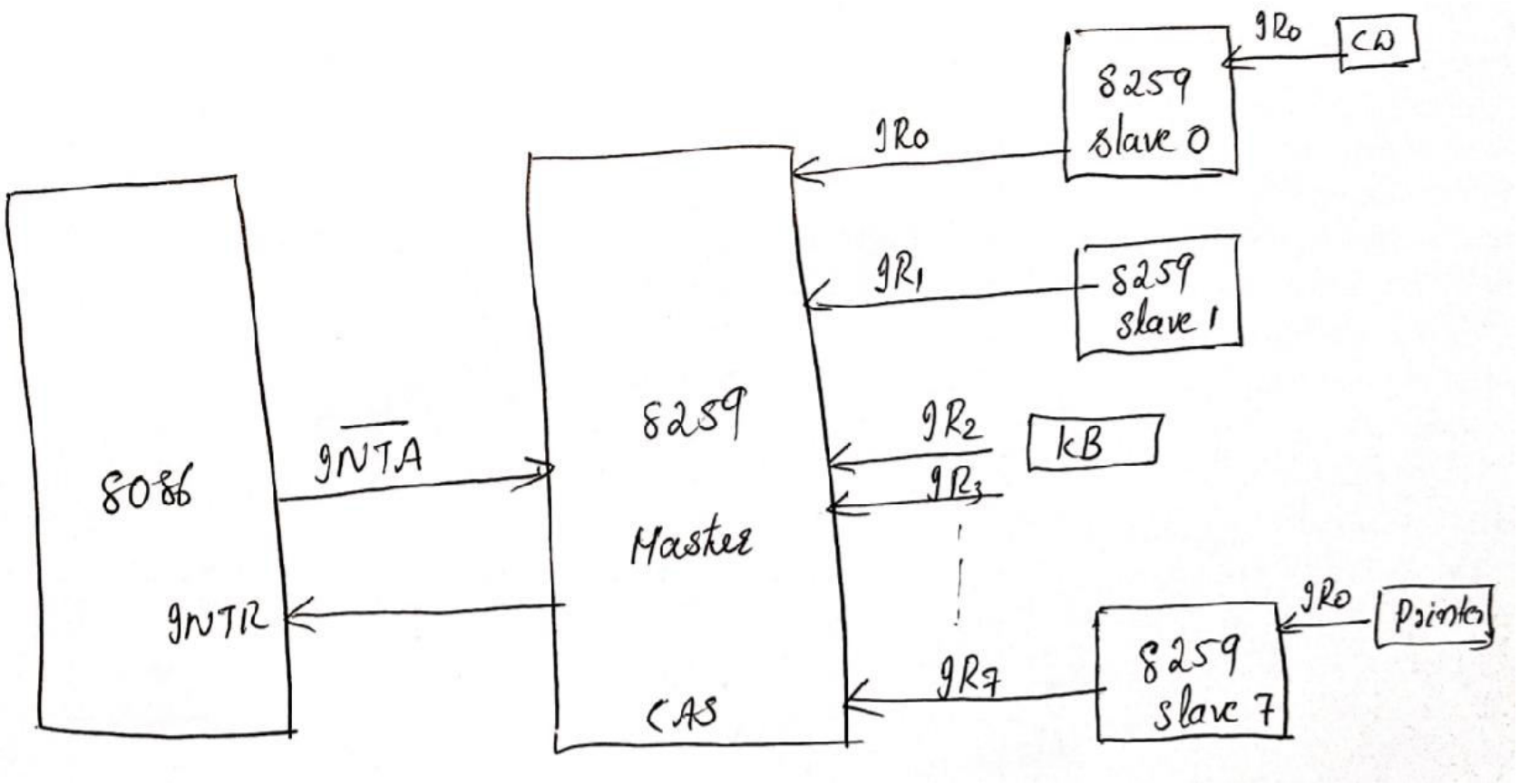


Fig. 9e.14: Format of operation command word 3
(*Source:* Intel Corporation)

8259 in cascaded mode




8086
INTA
INTR
8259
Master
CAS
IR0
IR1
IR2
IR3
IR7
8259
slave 0
8259
slave 1
8259
slave 7
IR0
CD
KB
IR0
Printer

Operating Modes of 8259

- **Fully nested mode :** default priority mode, IR0 – highest,IR7-lowest priority , fixed, single
- **Specially Fully nested mode** : default, IR0 – highest,IR7-lowest priority , fixed, cascaded
- **Rotating Priority Modes-2 types**
  - Automatic rotation mode : Applicable where all interrupting devices are of equal priority . After servicing a device , it gets lowest priority . All other priorities rotates subsequently
  - Specific rotation mode: Here user can assign lower priority to any IR line and thus fix all other priorities

Operating Modes of 8259 Contd…

- **Special Mask mode(SMM)**

It inhibits further interrupts at that level and enables interrupt from other levels

- **Poll mode:**

Here INT line of 8259 is not used.In return 8259 gives poll command.Poll command indicates highest priority interrupt which requires service

Poll Word

I	×	×	×	×	W_2	W_1	W_0

1= Valid Interrupt
0 = No valid interrupt

Level No of the highest priority interrupt to be serviced

W_2	W_1	W_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

- End of Interrupt modes (EOI):

  Normal EOI mode

  - Non Specific EOI mode:Prgmer does nt specify the bit to be cleared.8259 automatically clears the bit with highest priority from InSR
  - Specific EOI mode: Prgmer specify the bit to be cleared from InSR

  Auto EOI mode(AEOI): EOI is not needed .8259 itself clear he corresponding bit from InSR

```
ASSSUME CS : CODE, DS : DATA
DATA      SEGMENT
     FILENAME  DB "RESULT", "$"
     MESSAGE DB "FILE WASN'T CREATED SUCCESSFULLY",0AH,0DH,"$"
DATA    ENDS
```

```
CODE    SEGMENT
START:  MOV AX, CODE
        MOV DS, AX
        MOV DX, OFFSET ISROA
        MOV AX,250AH
        INT 21H
        MOV DX, OFFSET FILENAME
        MOV AX, DATA
        MOV DS, AX
        MOV CX, 00H
        MOV AH, 3CH
        INT 21H
        JNC FURTHER
        MOV DX,OFFSET MESSAGE
        MOV AH,09H
        INT 21H
        JMP STOP
FURTHER :   INT 0AH
STOP :      MOV AH,4CH
            INT 21H


ISROA PROC NEAR
      MOV BX, AX
      MOV CX, 500H
      MOV DX, 1000H
      MOV AX, 1000H
      MOV DS, AX
```

```
        MOV AH, 40 H
        INT 21 H
        IRET
ISROA     ENDP
CODE      ENDS
          END START
```