Vivek Govindasamy

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Born in Tracy, California, 3/3/1998 | U.S. Citizen | Residential Address: 1401, Palo Verde Road, Irvine, California

RESEARCH DOMAIN

System-Level Modeling, Computer Architecture, Embedded Systems, Firmware

TECHNICAL SKILLS

Programming Languages: C, C++, SystemC, Python, MATLAB, Verilog, GNU Bash
Application Softwares: Docker, Git, Linux, Excel

EDUCATION

University of California, Irvine — Irvine, California
PhD in Computer Engineering | Advisor: Prof. Doemer (doemer@uci.edu) — In Progress
MS in Computer Engineering | GPA: 3.82/4.0 — February, 2022
MS Thesis: Mapping of an APNG Encoder to the Grid of Processing Cells Architecture | Advisor: Prof. Doemer
Relevant Courses: Computer Architecture, Operating Systems, Embedded Systems

Vellore Institute of Technology — Vellore, India
B. Tech in Electronics & Computer Engineering | GPA: 9.10/10 — June, 2020
Relevant Courses: Advanced Microcontrollers (ARM), Digital Logic Design, Digital Signal Processing

PROFESSIONAL EXPERIENCE

University of California, Irvine — Irvine, California
Graduate Student Researcher, Center for Embedded and Cyber-Physical Systems — September, 2020 – Present
- Created a virtual prototype of a novel cache-less computer architecture called as the Grid of Processing Cells (GPC) in SystemC TLM-2.0 with a team of graduate students.
- Created an instruction accurate simulation of the GPC using RISC-V virtual prototypes.
- Designed a shared memory processor with coherent caches to compare the performance of the models.
- Created bare metal streaming applications (Canny, JPEG, PNG) to evaluate the GPC.
- A conference paper is currently under review.

University of California, Irvine — Irvine, California
Teaching Assistant, Center for Embedded and Cyber-Physical Systems
- Undergraduate course- EECS 22L: Software Engineering in C — April, 2022 – June, 2022
- Graduate course- ECPS 203: Embedded System Modeling — September, 2022 – December, 2022
- Graduate course- ECPS 204: Embedded System Software — January, 2021 – March, 2021
- Graduate course- ECPS 211: Machine Learning and Data Mining — January, 2022 – March, 2022

Indian Institute of Science — Bangalore, India
Intern, Electrical Engineering Department — May, 2019 – June, 2019
- Performed JPEG image compression using an FPGA. The Verilog design was able to compress an image using the Discrete Cosine Transform as well as encode it using Huffman Coding.

PUBLICATIONS

Minimizing Memory Contention in an APNG Encoder using a Grid of Processing Cells — Paderborn, Germany, November, 2022
- Conference Paper - International Embedded Systems Symposium

Mapping of an APNG Encoder to the Grid of Processing Cells Architecture — Irvine, California
- CECS Technical Report, September, 2022

A SystemC Model of a PNG Encoder — Irvine, California
- CECS Technical Report, December, 2020

Coverless Image Steganography using Haar Integer Wavelet Transform — Tamilnadu, India
- Conference Paper - International Conference on Computing Methodologies and Communication — March, 2020

RELEVANT PROJECTS

Coverless Image Steganography using the Haar Wavelet Transform *Capstone Project* — January, 2020 – May, 2020
- Developed a technique for sending secret information using images without modifying the image using Haar wavelets.
- Prototyped the model in MATLAB and implemented it using a Zynq Zedboard. The final model was able to achieve very high information per image at the cost of increased encoding and decoding complexity. Funded by DRDO.