INDIAN INSTITUTE OF TECHNOLGY ROPAR

EE-301 Analog Circuits

Course Project

Designing Cascode amplifier and Current mirror schematic and layout for 180nm and 22nm technology

Submitted by:

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Objective:

Design of cascode amplifier and cascode current mirror in schematic and layout using LTspice and Magic in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node.

Design specifications:

- V_{DD} = 1.8 V (180nm) and 0.8V (22nm)
- A_V = 20 V/V
- Power dissipation (P_D) < 5 mW
- Load Capacitance (C_L) = 1 pF
- Unity Gain Bandwidth (UGB) > 500 KHz.

Theory:

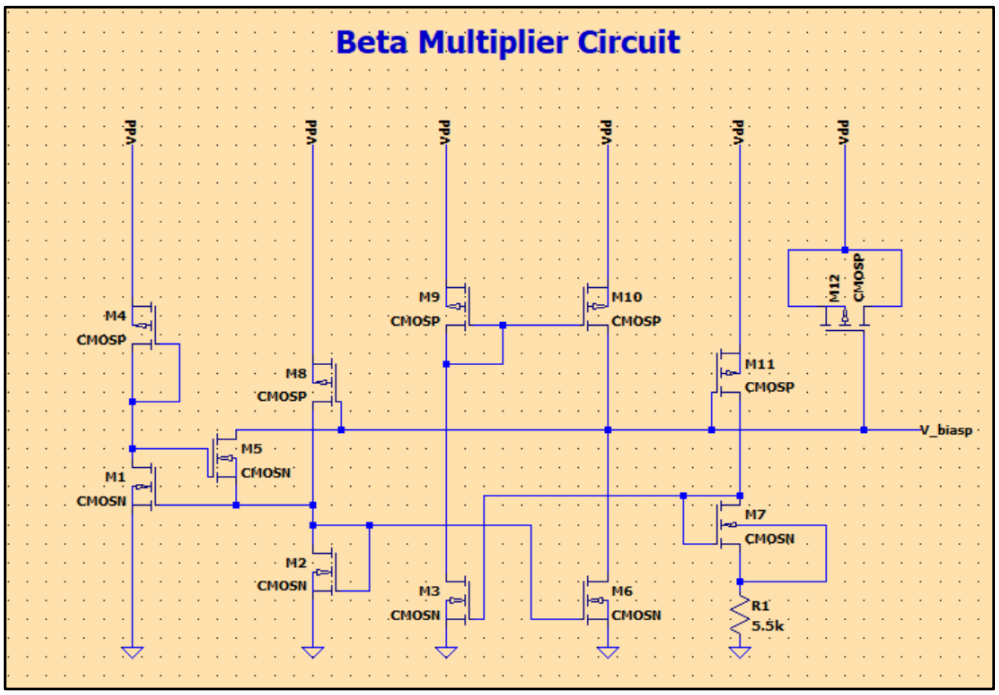
Beta multiplier circuit: The beta multiplier circuit is an example of positive feedback. The resistor is added to stabilize the close loop gain of the circuit by requiring higher V_{GS}. The beta multiplier current reference circuit is an alternative method for (potentially) getting a PTAT-like current without utilizing bipolar transistors.

Cascode current mirror: The output (V_{biasp}) of the beta multiplier circuit is fed to the input of the current mirror. The outputs of the circuit are Vbias1, Vbias2, and Vbias3, which are used in the cascode amplifier stage for biasing of the circuit.

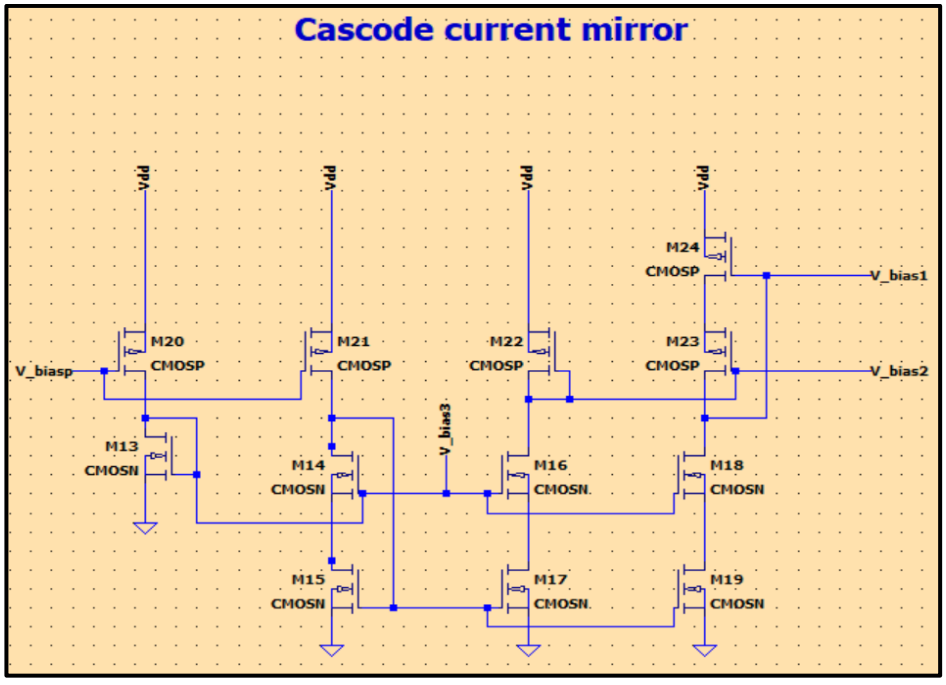
Cascode amplifier: It consists of a common source stage (CS) with a common gate stage (CG). Compared to a single amplifier stage, this combination may have one or more characteristics: higher input-output isolation, higher input impedance, high output impedance, and higher bandwidth. The bottom transistor's source and drain terminals have virtually constant voltage levels, and there is nothing to provide gate feedback. Whereas the higher transistor likewise keeps the source and gate terminal voltages constant. There are only output and input nodes with the appropriate voltage values.

180nm Technology

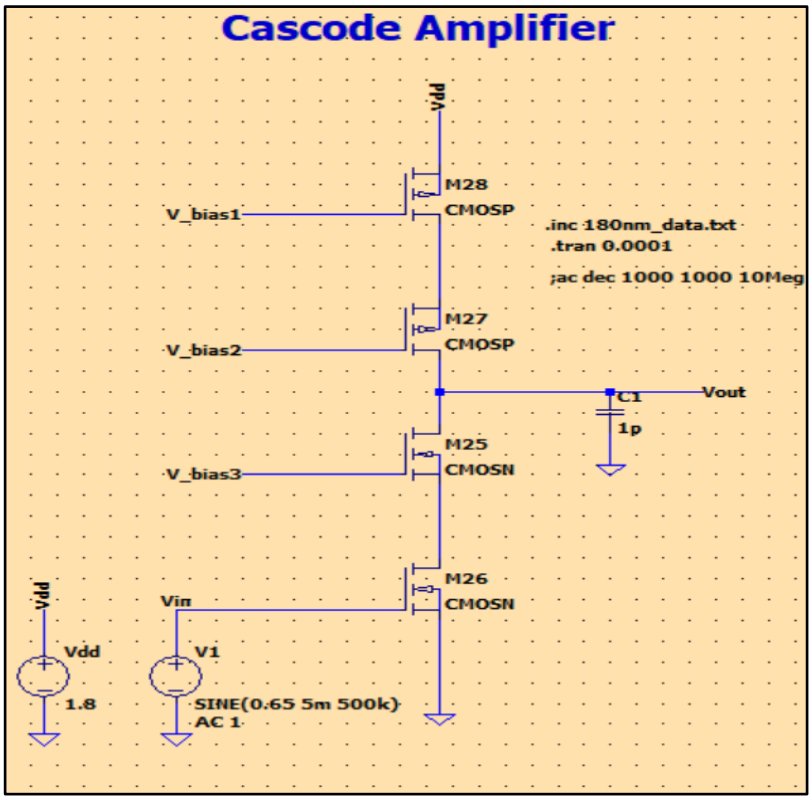
Beta Multiplier Circuit:



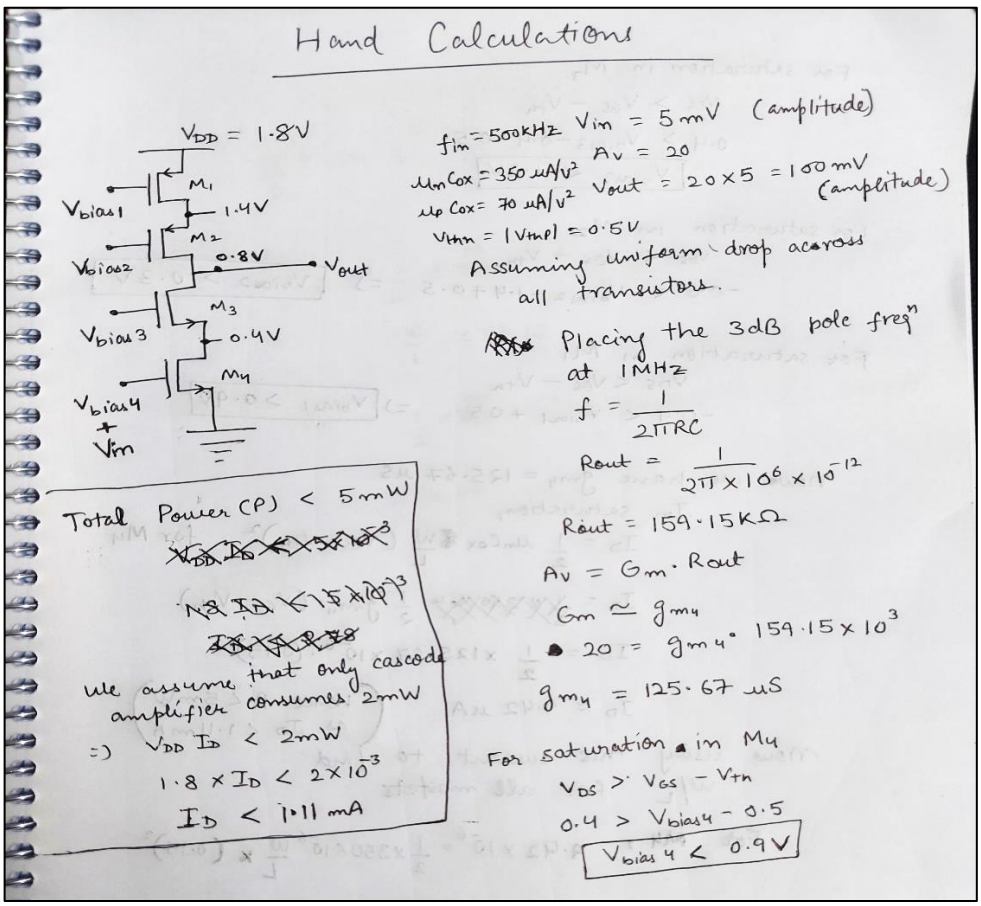
Current Mirror:



Cascode Amplifier:



Calculations:



For saturation in M_3

$V_{DS} > V_{GS} - V_{th}$

$0.4 > V_{bias3} - 0.4 - 0.5$

$\boxed{V_{bias3} < 1.3V}$

For saturation in M_2

$V_{DS} < V_{GS} - V_{th}$

$-0.6 < V_{bias2} - 1.4 + 0.5 \Rightarrow \boxed{V_{bias2} > 0.3V}$

For saturation in M_1

$V_{DS} < V_{GS} - V_{th}$

$-0.4 < V_{bias1} + 0.5 \Rightarrow \boxed{V_{bias1} > 0.9V}$

Now we have $g_{m4} = 125.67\ \mu S$

In saturation,

$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$ for M_4

$I_D = \frac{1}{2} g_{m4} \cdot (V_{GS} - V_{th})$

$I_D = \frac{1}{2} \times 125.67 \times 10^{-6} \cdot (0.15)$

$I_D \approx 9.42\ \mu A$ (Hence $P < 5mW$ as $I_D < 1.11mA$)

Now using this current to find W/L for all mosfets

For M_4, $9.42 \times 10^{-6} = \frac{1}{2} \times 350 \times 10^{-6} \frac{W}{L} \times (0.15)^2$

$\frac{W}{L} = \frac{9.42 \times 2}{350 \times (0.15)^2} \approx 3$

For M_3 $I_D = \frac{1}{2} \times 350 \times 10^{-6} \times \frac{W}{L} \times (0.6 - 0.5)^2 = 9.42 \times 10^{-6}$

$\frac{W}{L} \simeq 6$

For M_2 $I_D = \frac{1}{2} \times 70 \times 10^{-6} \times \frac{W}{L} (0.5 + 0.5)^2 = 9.42 \times 10^{-6}$

$\frac{W}{L} \simeq 12$

For M_1 $I_D = \frac{1}{2} \times 70 \times 10^{-6} \times \frac{W}{L} \times (-0.6 + 0.5)^2 = 9.42 \times 10^{-6}$

$\frac{W}{L} \simeq 27$

The actual values of Voltages and W/L ratio in the LTspice simulation may differ from the above obtained values so as to obtain the target specification. This difference occurs due to non-idealities in the models used.

Results:

W/L ratios for current mirror:

MOSFET	W/L Ratio
M13	360/360
M14	360/180
M15	425/180
M16	9000/180
M17	1800/360
M18	2800/180
M19	2800/180
M20	13650/180
M21	6000/180
M22	555/360
M23	3600/180
M24	1100/180

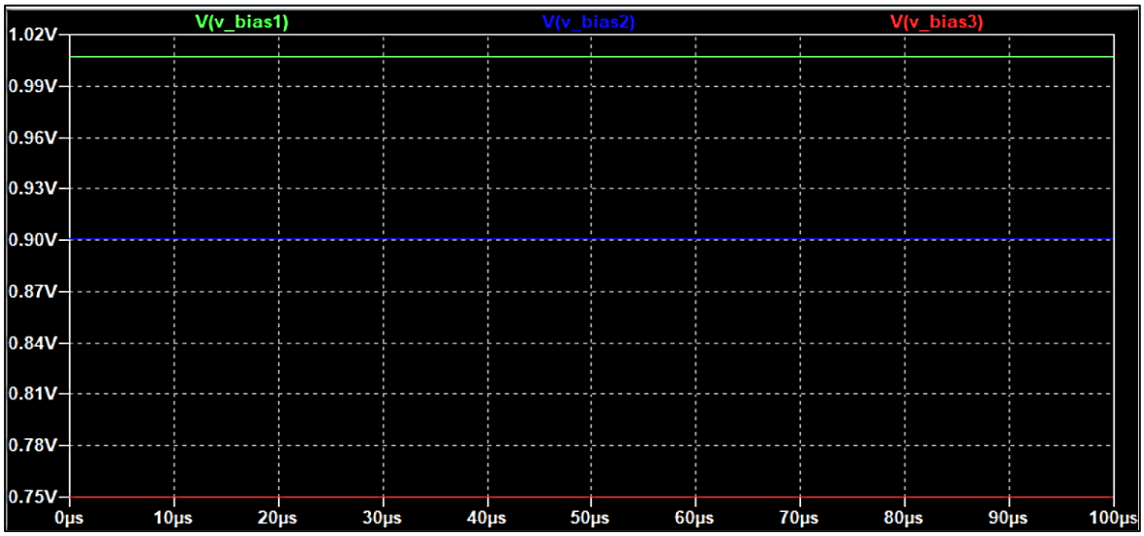
W/L for cascode amplifier:

MOSFET	W/L Ratio
M25	1060/180
M26	1110/180
M27	1490/180
M28	1595/180

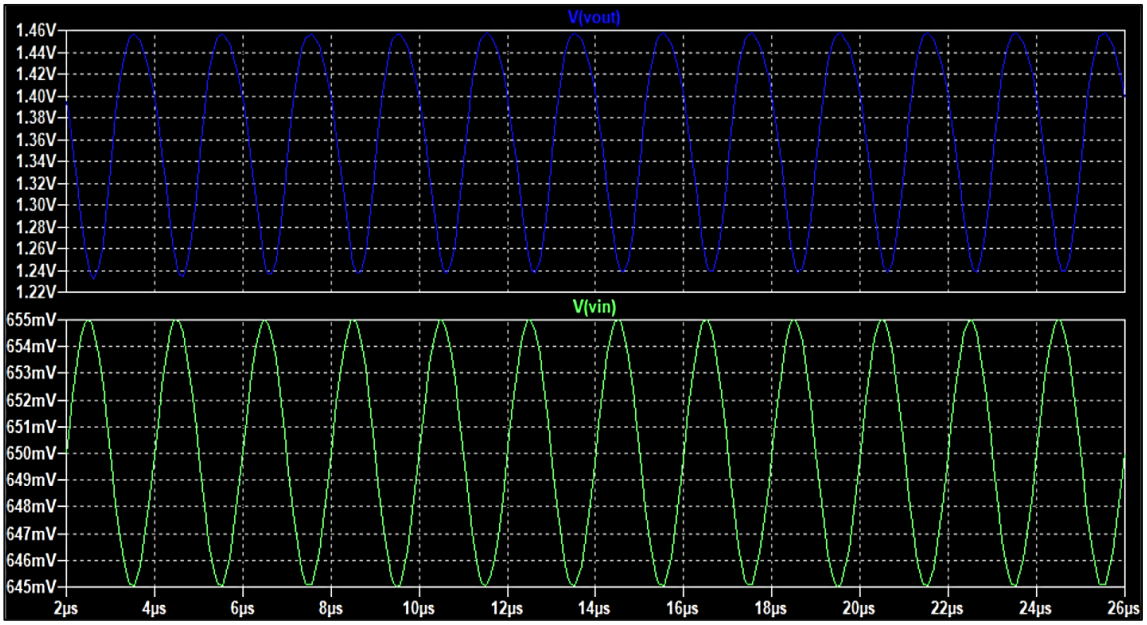
Bias voltages:

V_bias1 = 1V V_bias2 = 0.9V V_bias3 = 0.75V

V_bias4 (DC offset in source) = 0.65V V_biasp = 1.29V



Output and Input waveform:

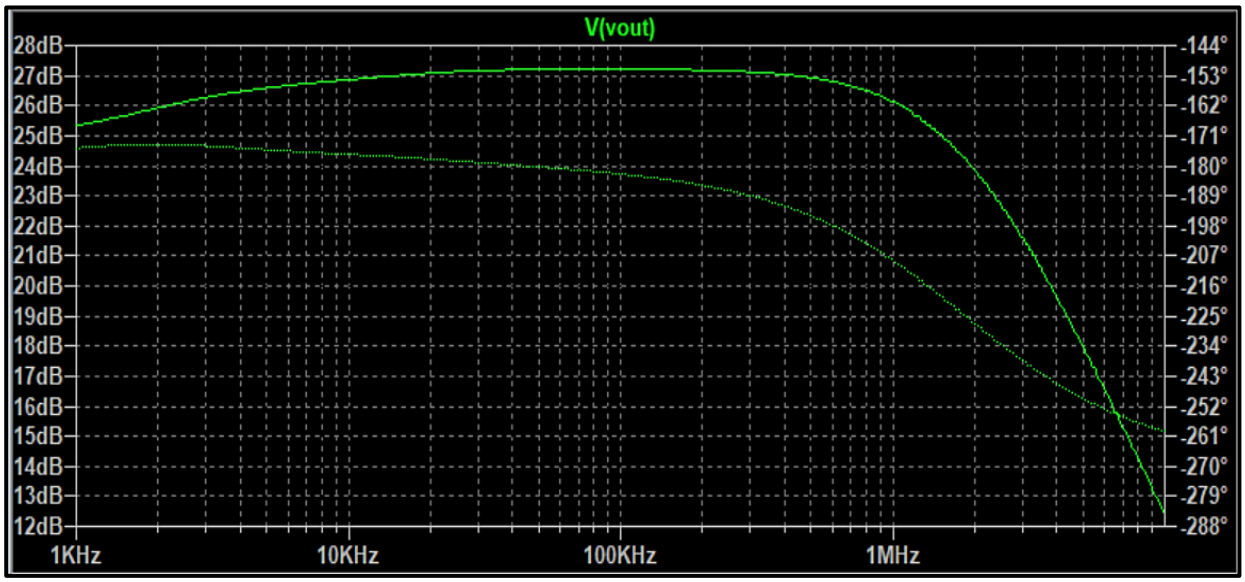


Input voltage amplitude (small signal) = 5mV

Output voltage amplitude = 110mV

Gain = Vout/ Vin = 110/5 = 22 V/V = 26.84 dB (at input frequency of 500kHz)

AC response:

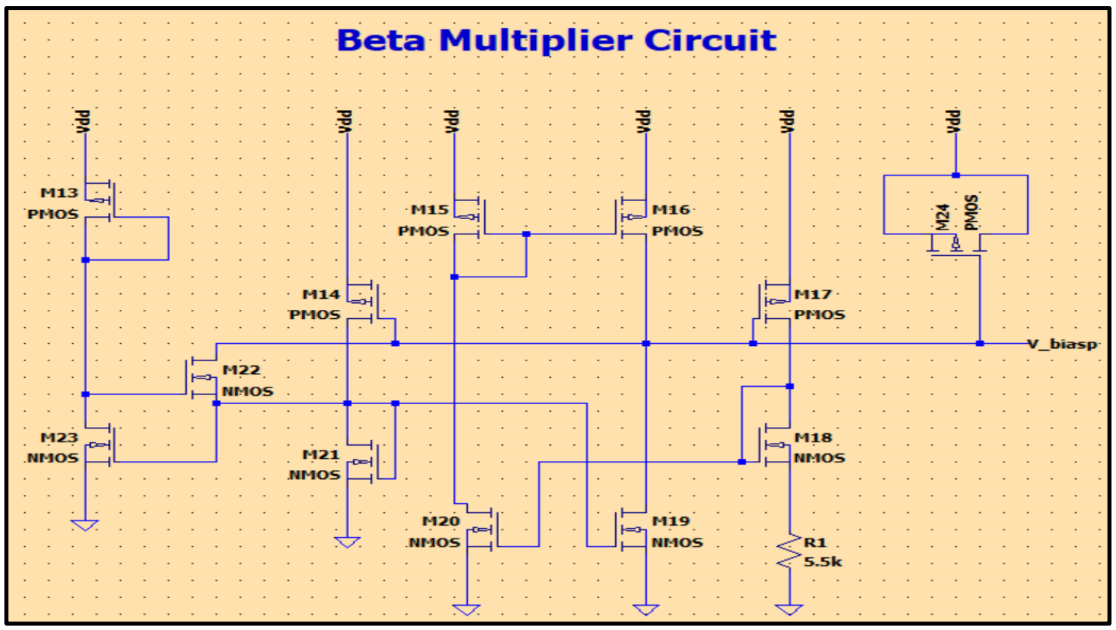


Hence, we have achieved:

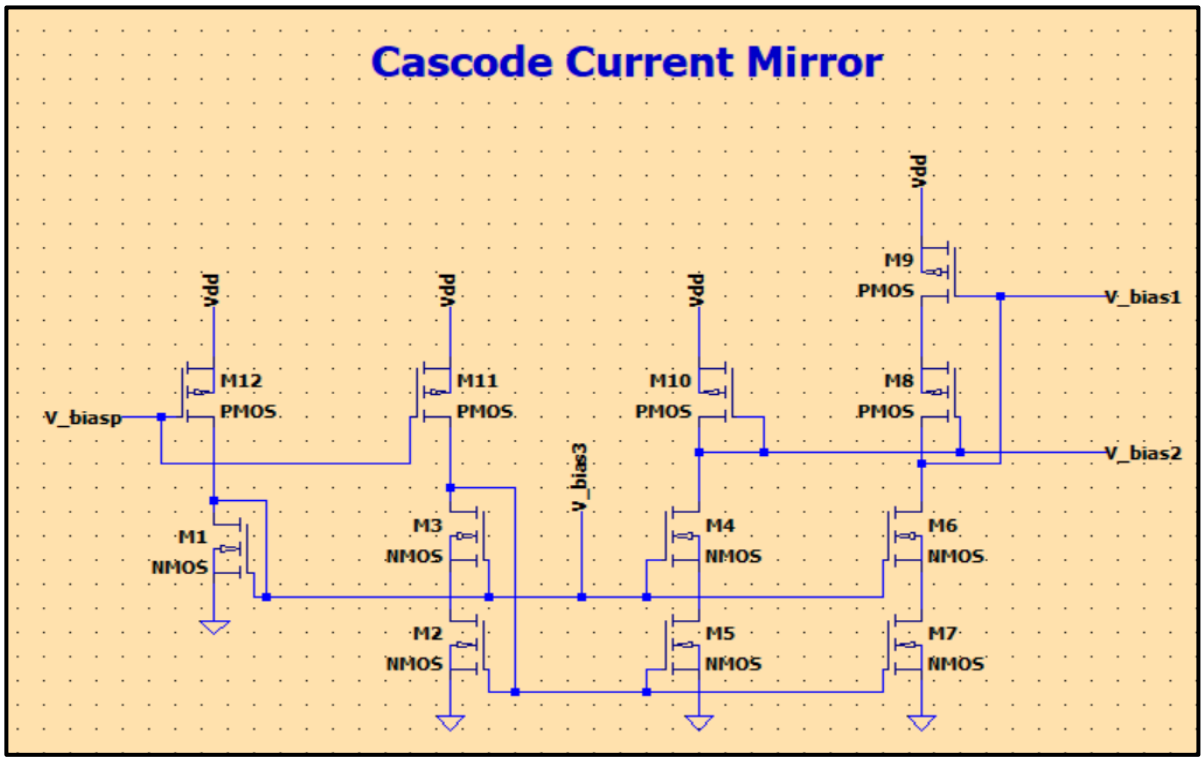
- Power dissipation less than 5mW
- UGB greater than 500kHz (more than 1MHz for our amplifier)
- Gain 26.84 dB for 500kHz input frequency

22nm technology

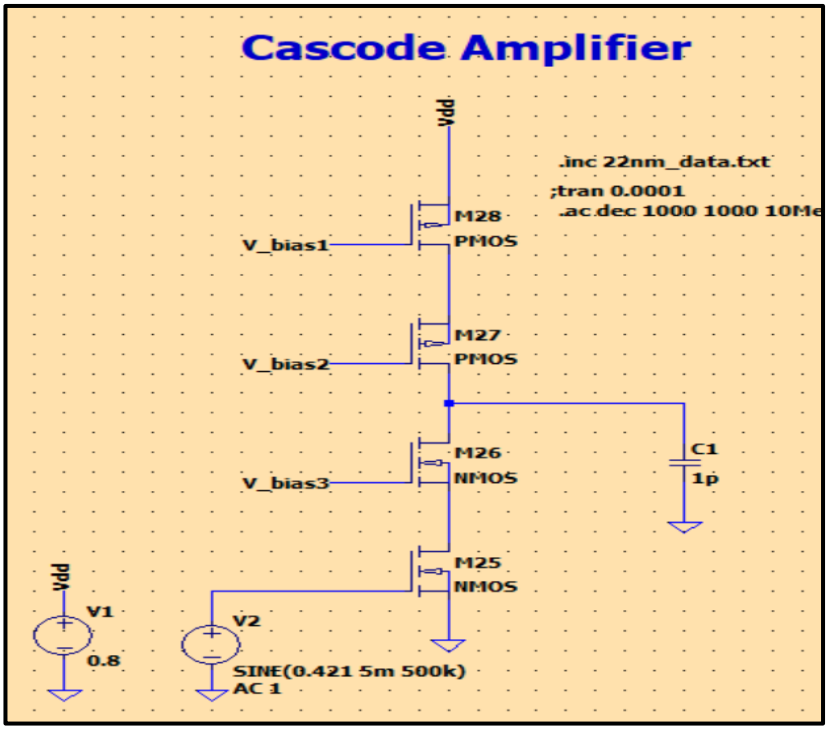
Beta multiplier circuit:



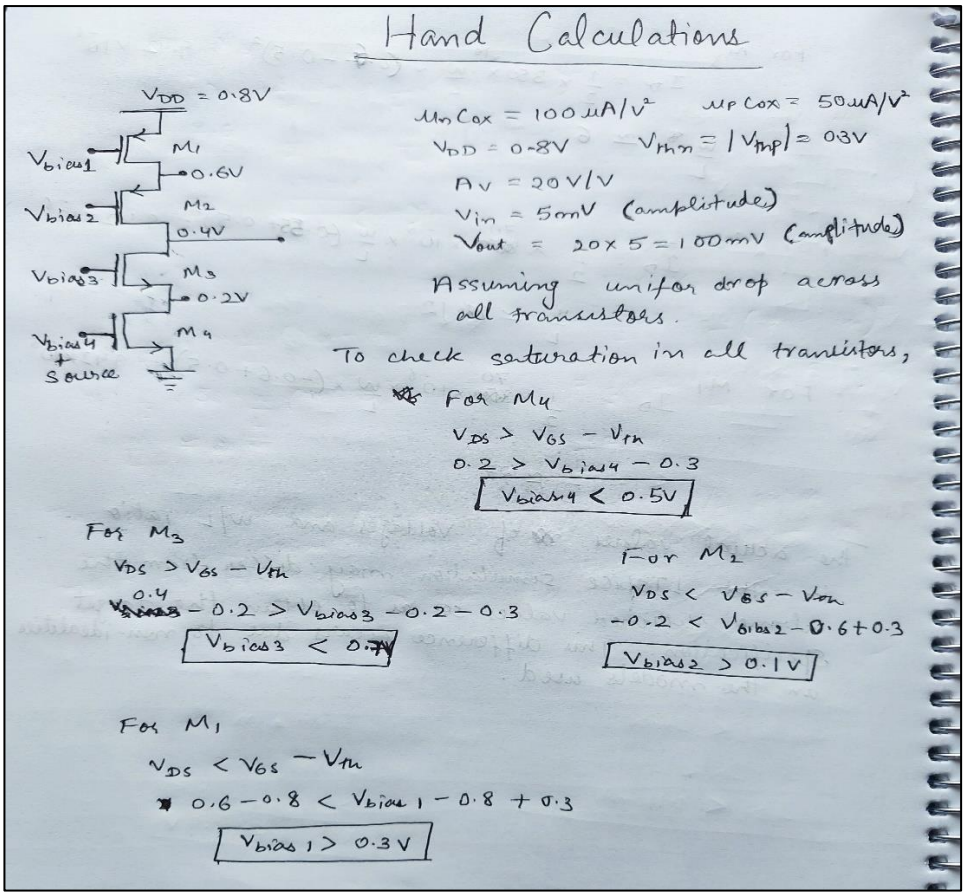
Current mirror:



Cascode amplifier:



Calculations:



Now to place pole frequency (3-dB) at 1 MHz

$$f = \frac{1}{2\pi R_{out} C}$$

$$R_{out} = \frac{1}{2\pi \times 10^6 \times 10^{-12}} = 159.15\ K\Omega$$

$A_v = 20 = G_m R_{out}$

For cascode amplifier,

$G_m \simeq g_{m4}$

$20 = g_{m4} \cdot 159.15 \times 10^3$

$g_{m4} = 125.67\ \mu S$

In saturation for M_4

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$$

$$I_D = \frac{1}{2} \cdot g_{m4} \cdot (V_{GS} - V_{th})$$

$$I_D = \frac{1}{2} \times 125.67 \times 10^{-6} (0.121)$$

$= 7.6\ \mu A$

$\Rightarrow I_D = 7.6\ \mu A < 2.5\ mA$

$\therefore I_D = 7.6\ \mu A$

$P_{total} = 5\ mW$
Assuming cascode amplifier consumes 2mW alone.

$V_{DD} \cdot I_D < 2mW$

$I_D < \frac{2 \times 10^{-3}}{0.8}$

$I_D < 2.5\ mA$

To find W/L for M_4

$$g_{m4} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})$$

$$125.67 = 100 \times \frac{W}{L} (0.121)$$

$$\frac{W}{L} \simeq 11$$

For M_3,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \times (V_{GS} - V_{th})^2$$

$$7.6 = \frac{1}{2} \times 100 \times \frac{W}{L} \times (0.95 - 0.3)^2$$

$$\frac{W}{L} = \frac{2 \times 7.6}{100 \times (0.15)^2} \Rightarrow \frac{W}{L} \simeq 7$$

For M_2

$$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$$

$$I_D = \frac{1}{2} \times 50 \times \frac{W}{L} \left(\frac{0.105}{}\right)^2 = 7.6$$

$$\frac{W}{L} \simeq 121$$

For M_1

$$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$$

$$= \frac{1}{2} \times 50 \times \frac{W}{L} (0.095)^2 = 7.6$$

$$\frac{W}{L} \simeq 34$$

The actual values of bias voltages and W/L ratios may differ from the values used in LTspice to meet the target specifications of the amplifier. These differences occur due to non-idealities in the model.

Results:

W/L ratios for cascode current mirror:

MOSFET	W/L ratio
M1	45/44
M2	109/22
M3	111/22
M4	290/22
M5	179/22
M6	44/22
M7	162/22
M8	2200/22
M9	264/22
M10	34/22
M11	264/22
M12	4400/22

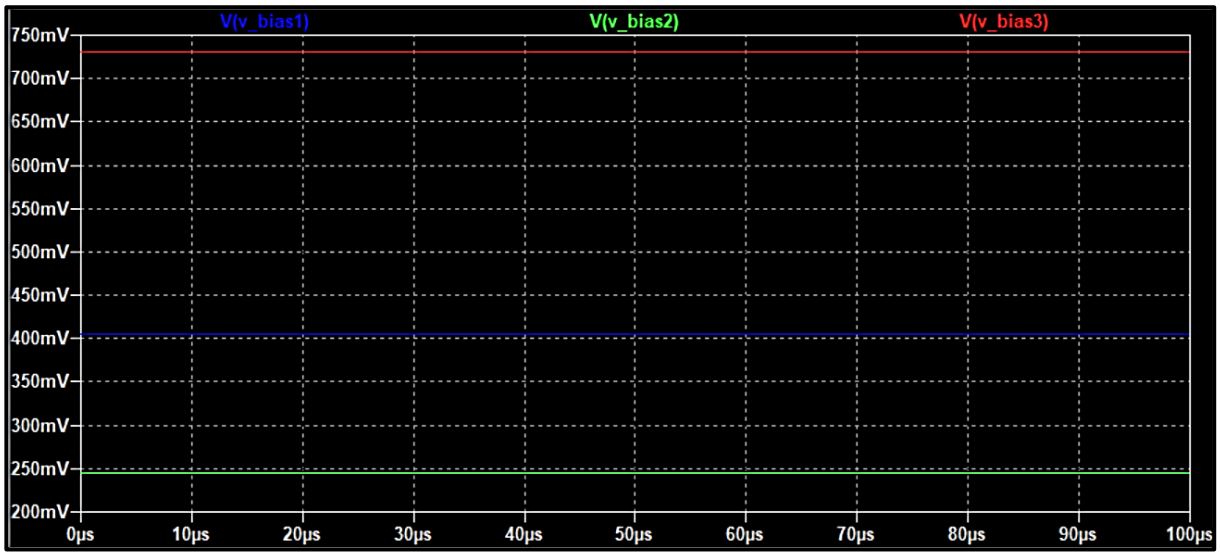
W/L Ratio for cascode amplifier:

MOSFET	W/L ratio
M25	425/22
M26	1660/132
M27	11000/44
M28	17000/44

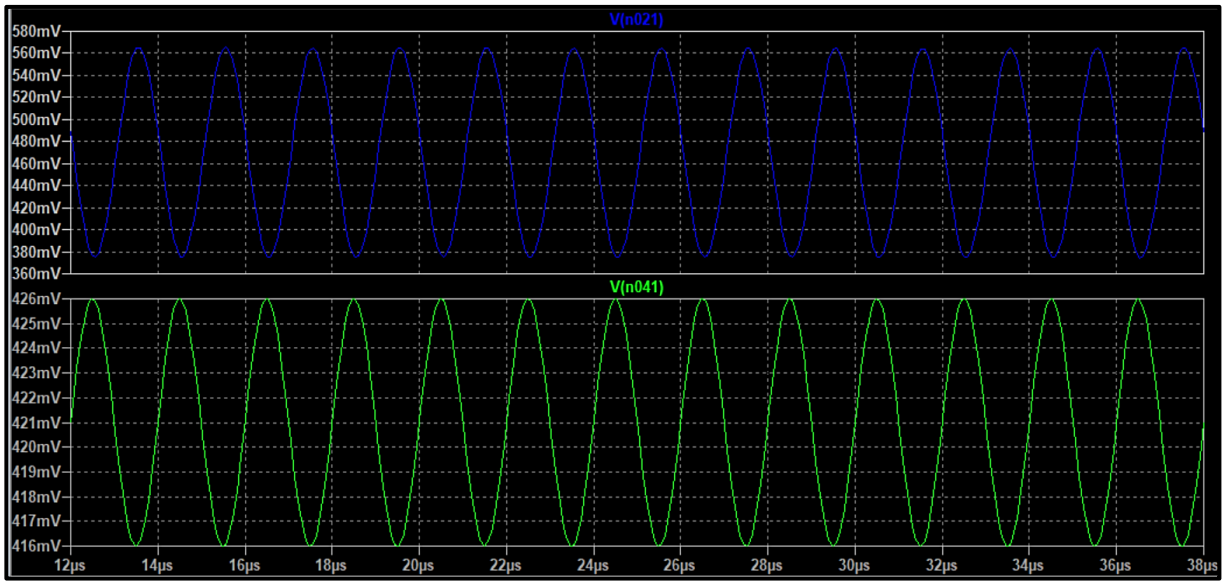
Bias voltage:

V_bias1 = 0.405V V_bias2 = 0.245V V_bias3 = 0.73V

V_bias4 (DC offset in source) = 0.421V V_biasp = 0.455V



Output and input waveform:

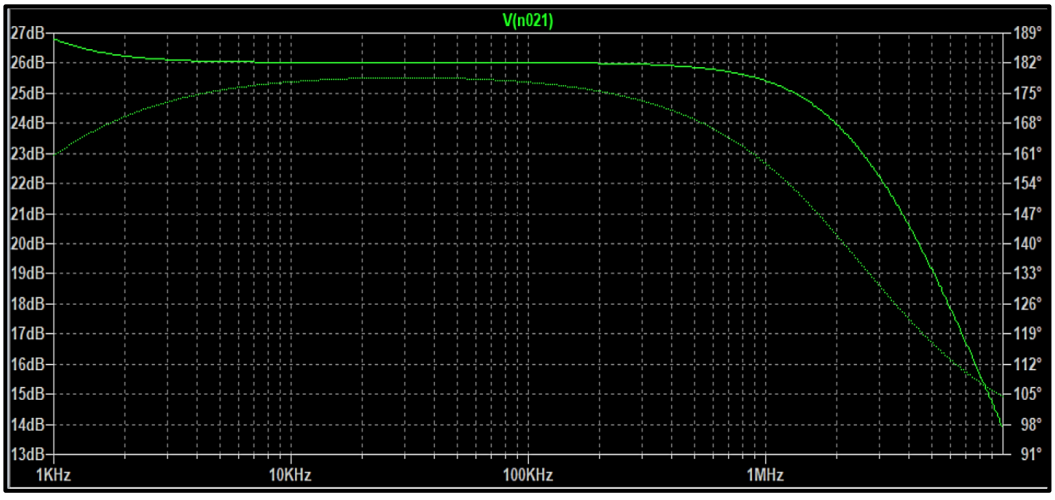


Input voltage amplitude (small signal) = 5mV

Output voltage amplitude = 95mV

Gain = Vout/ Vin = 95/5 = 19 V/V = 25.57 dB (at input frequency of 500kHz)

AC response:



Hence, we have achieved:

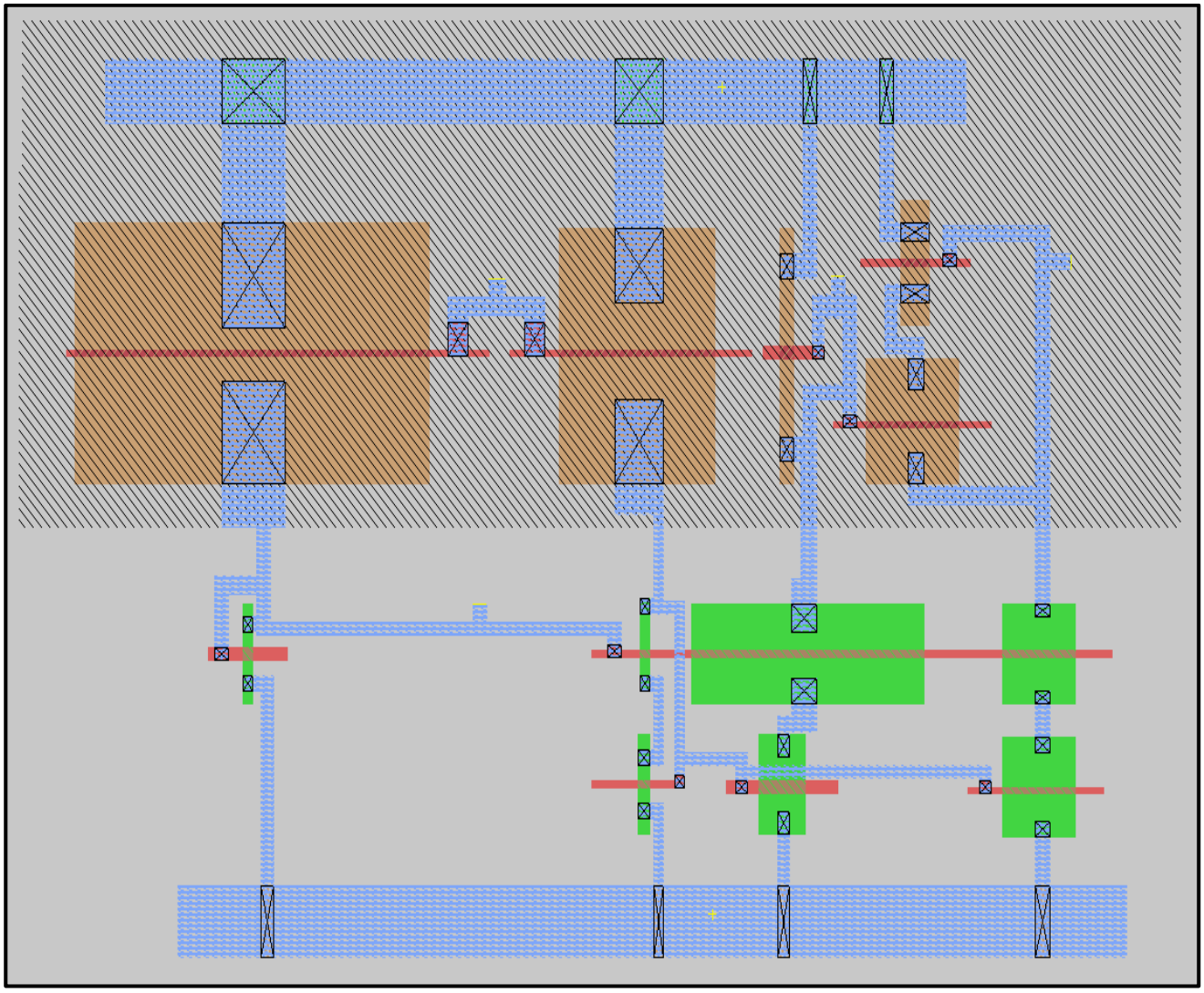
- Power dissipation less than 5mW
- UGB greater than 500kHz (more than 1MHz for our amplifier)
- Gain 25.57 dB for 500kHz input frequency

Magic Layout for 180nm technology

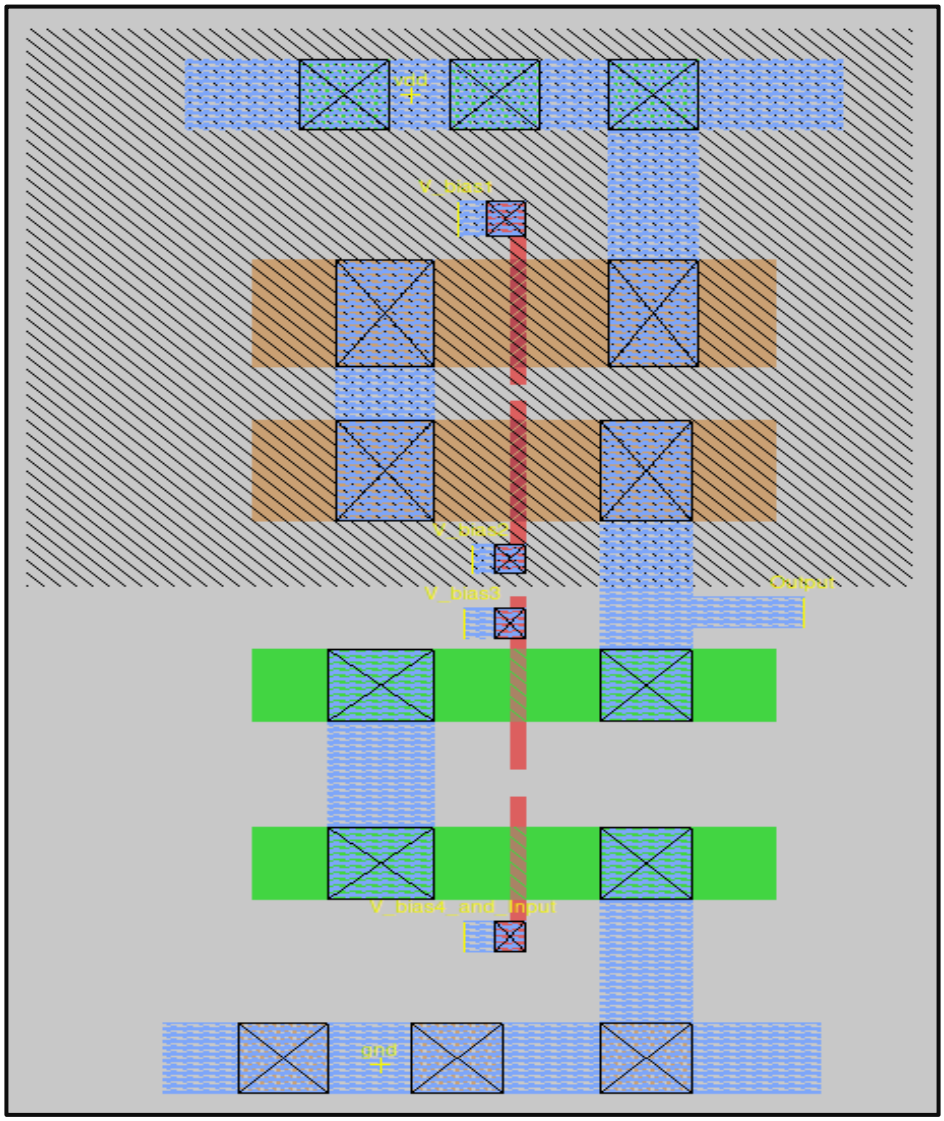
Procedure:

- P-diffusion (along with n-well) and N-diffusion were used for PMOS and NMOS respectively.
- The contacts on drain/source were made using nd-contact and pd-contact.
- The connections were laid using metal-1.
- The connection to Vdd and ground were made using n-substrate contact and p-substrate contact.
- The gate was laid using polysilicon and gate contact using polycontact.

Cascode Current Mirror Layout:



Cascode Amplifier Layout:



Conclusion:

The project results indicate that the target performance was successfully achieved for both the 180nm and 22nm technology files, while adhering to the specified constraints, in the case of a cascaded amplifier biased through a current mirror. Furthermore, the layout for the cascode amplifier was meticulously crafted in accordance with the prescribed design guidelines using the Magic tool.