

Vishal Canumalla

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Research Interests

- Programming Languages
- Program Synthesis
- Compilers
- High-performance Computing

Education

2020–2024 **Bachelor's of Computer Science**, *University of Washington*, Seattle.

Employment

- 2021–present **Undergraduate Researcher**, *University of Washington*, Seattle, WA.
Advisor: Zachary Tatlock
- Summer 2022 **Software Engineering Intern**, *Toyota Connected North America*, Plano, TX.
- Spring 2022 **Research Intern**, *Certora*, Seattle, WA.
Advisor: Chandrakana Nandi

Presentations and Posters

- Sept. 2023 **Application of Sketch Guided Synthesis to Runtime Reconfigurable FPGA Primitives**,
ICFP Student Research Competition.
- May 2023 **FPGA Synthesis via Program Synthesis**,
Allen School Undergraduate Research Showcase.
- Nov. 2023 **Specialized Accelerators: Addressing the Mapping Gap**,
Allen School Annual Affiliate Research Showcase.

Publications

- Pre-print **FPGA Technology Mapping Using Sketch-Guided Program Synthesis**
Gus Henry Smith, Ben Kushigian, [Vishal Canumalla](#), Andrew Cheung, Steven Lyubomirsky,
Sorawee Porncharoenwase, René Just, Zachary Tatlock.
Conditionally Accepted
- Arxiv 2023 **Application-Level Validation of Accelerator Designs Using a Formal Software/Hardware Interface**
Bo-Yuan Huang, Steven Lyubomirsky, Yi Li, Mike He, Thierry Tambe, Gus Henry Smith,
Akash Gaonkar, [Vishal Canumalla](#), Andrew Cheung, Gu-Yeon Wei, Arti Gupta, Zachary
Tatlock, Sharad Malik.
Under Minor Revision to TODAES 2023
- ICFP SRC 2023 **Application of Sketch Guided Synthesis to Runtime Reconfigurable FPGA Primitives**
[Vishal Canumalla](#)
3rd Place in Undergraduate Division
- PLARCH 2023 **Generate Compilers from Hardware Models!**
Gus Henry Smith, Ben Kushigian, [Vishal Canumalla](#), Andrew Cheung, Zachary Tatlock.

Research Projects

- Lakeroad Applying program synthesis to the problem of FPGA technology-mapping. Synthesized more optimal usage of digital signal processor primitives compared to commercial compilers.
- 3LA Developing a formal hardware/software interface for end-to-end testing of accelerator designs. Wrote compiler passes to generate accelerator invocations from deep learning applications.
- Gambit Applying mutation testing to formal verification of smart contracts. Developed prototype mutations on Solidity AST nodes, finding common bugs across developer smart contracts.
- Glenside Contributor to Glenside, an open-source pure tensor program representation. Wrote program rewrites from TVM Relay to specialized accelerator invocations.

Awards

- 2023 3rd Place in Undergraduate Division, ICFP Student Research Competition
- 2022 ACM PacNW Div. 2 State Champions
- 2019 U.S. National Chemistry Olympiad Semifinalist

Coursework

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| ◦ Graduate Programming Languages | ◦ Computer Aided Reasoning |
| ◦ Algorithms | ◦ Programming Languages |
| ◦ Distributed Systems | ◦ Systems Programming |