DEVELOPING LOW TEMPERATURE CONTACTS FOR MONOLAYER TMD HETEROSTRUCTURES

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I. ABSTRACT

Studies of two-dimensional (2D) Van der Waals (VdW) heterostructure devices have contributed significantly to novel optoelectronics advancements and correlated quantum states at the atomic scale. WSe_2, a semiconducting transition metal dichalcogenide (TMD), has a direct bandgap when reduced to a monolayer, and can be used for both optical and electrical measurements. However, a lack of reliable, low resistance electrical contacts to semiconducting 2D materials has hindered careful electron transport studies and further development of optoelectronic devices. Here, we aim to develop reliable, Ohmic contacts by using pre-patterned platinum contacts for p-type WSe_2 monolayers. Bulk graphite, hexagonal boron nitride (h-BN), and WSe_2 are mechanically exfoliated and stacked by dry transfer. We fabricate h-BN encapsulated monolayer WSe_2 with dual graphite gates, allowing independent doping of the contact areas and the WSe_2 channel. After designing and evaporating platinum Hall bar contacts using electron beam lithography and evaporation, we first demonstrate reliable doping of WSe_2 through photoluminescence measurements to observe exciton and trion formation, then take transport measurements at low temperatures (1.7 K) to extract the contact resistance and linearity of the contact response. The development of low temperature contacts will open up the possibility to measure Quantum Hall states with observable Shubnikov-de Haas (SdH) oscillations and other quantum structures such as electrically controlled quantum dots and correlated states in TMD twisted heterostructures. Going forward, we will try to develop contacts for other TMD materials to expand the available 2D materials for electronic studies and the development of efficient, silicon-based devices among modern electronics.

II. INTRODUCTION

Research in silicon-based semiconductors largely contributes to the development of modern optoelectronics. By studying TMDs in silicon-based devices, optoelectronics can be made more efficient when we consider their integration. TMDs have a direct band gap at the monolayer limit. In an indirect band gap, the excitation of an electron from the valence to conduction band by the Coulomb force requires the aid of a phonon, whereas the excitation with a direct band gap does not. An exciton is a combination of the electron and the positively charged hole. In direct band gaps, the formation of this pair as an exciton can be made easier without the phonon mediation, therefore making the process faster. The recombination process of the electron-hole pair where light is generated is therefore more efficient. By building a device consisting of monolayer WSe_2, encapsulated with h-BN and dual-gated with graphite, along with a patterned Hall Bar on WSe_2, we aim to perform quantum transport measurements. The device can be tuned by an electric field and under a perpendicular magnetic field, should result in observation of SdH oscllations from which we can extract the carrier mobility and other transport qualities of WSe_2. Platinum contacts are ideal for transport measurements because their high work function matches the valence band of WSe_2. Here, gold contacts were used for initial test devices. A single-gated, encapsulated monolayer WSe_2 device with gold prepatterned contacts was fabricated to help conclude the quality of WSe_2. We performed optical measurements to measure the exciton emission energy through photoluminescence across multiple gate voltages to demonstrate efficient gating and the quality of the WSe2 monolayer. The gate-dependent photoluminescence data was acquired at both room temperature (293 K) and low temperature (1.7K).

III. MATERIALS AND METHODS

Mechanical Exfoliation

Fabrication of the heterostructure devices begins with mechanical exfoliation of the materials to be stacked in the heterostructure—graphite, hexagonal boron nitride, and WSe_2. During this procedure, a 90 nm silicon dioxide (SiO2) wafer is first cut into chips, approximately 0.5cm by 0.7cm each, with each cut following the 1-0-0 lattice structure, which resulted in straight edges on all sides to serve as the substrate. In this process, a piece of bulk material is placed onto a strip of Scotch tape. Sticking the tape together and peeling back multiple times creates an array of the material on the strip, with each replication thinning out the bulk piece through cleaving at the VdW interface. After multiple arrays are formed, chips are laid face-down onto the tape, which is then flipped over and pressed firmly against the surface of the table. The tape is slowly peeled back, ideally at a constant rate, to reveal the transfer of crystals on the tape to the substrate **(Fig. 1)**.

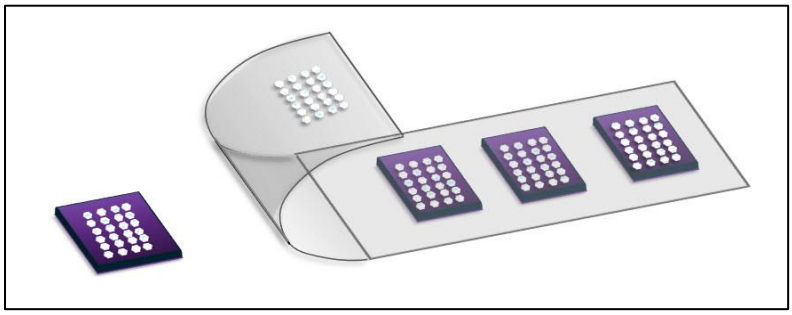

Figure 1. Mechanical exfoliation revealing h-BN crystals on substrate

For certain materials, the use of oxygen plasma cleaning or heating is added to achieve higher yields or samples of a desired thickness. When exfoliating WSe_2, both steps were done to maximize the probability of getting large monolayer WSe_2. Oxygen plasma cleaning removes

organic debris, and SiO2 wafer chips were placed into the cleaner after being cut at medium radio frequency (RF) level with an oxygen flow rate of 10.6 mL/min for five minutes. Electrons and gas particles couple to generate plasma, which is of a purple color from energy states, based on the RF power level. Because this cleaning process removes organics, it could be applied to clean the substrate and materials such as graphite.

Heating of the tape is done right after laying the chips onto the arrays. Through heat, the tape and crystals are easily conformed to the SiO2 substrate, therefore, increasing its adhesiveness onto the chip. For WSe_2 and select h-BN samples, this was done at 90°C for two to three minutes, then cooled down before the tape is peeled back.

After exfoliation is done for all materials, each substrate chip is scanned under a microscope to locate monolayer WSe_2, approximately 20 to 40 nm thick h-BN, and graphite all with the proper shape. The h-BN samples must be large enough in area to prevent the different layers from being electrically connected. For the Hall bar device, the WSe_2 sample has a minimum of 10 μm by 3 μm to fit the complete Hall bar patterning with enough room for error, where the actual piece was 14.9 μm by 3.1 μm. Each sample used in the device was uniform in thickness, with uniform color and contrast against the substrate. To determine the thickness of each flake, the contrast values were measured and compared to data from atomic force microscopy (AFM). The AFM tip can be used to accurately measure vertical displacement by tapping or contact mode.

Device Design

We determine the test device design by the specific shapes of flakes considered for the monolayer WSe_2, graphite contact and gate, and top and bottom h-BN. The shapes of each flake were traced on PowerPoint, then superimposed, where the composition of the device was: Top

graphite gate, top h-BN, monolayer WSe_2, graphite contact, bottom-BN from top to bottom. This design was then superimposed on the design of pre-patterned gold contacts, where the graphite gate and contact would touch two separate leads **(Fig. 2)**.

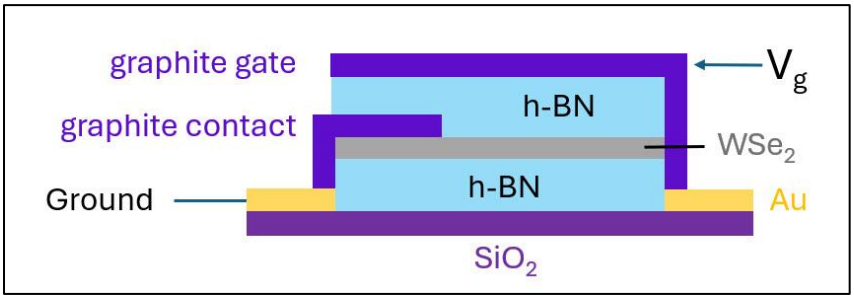

Figure 2. Composition of test device

Patterning

The design of contacts and alignment marks was first made on CAD software (KLayout). For this project, patterning has been done for alignment marks and pre-patterned contacts and will be done for the Hall Bar on the final device.

Substrate chips, relatively smaller than ones used for exfoliation to fit in a sample holder, are first spin-coated with 940 PMMA A4, a polymer, then baked at 180°C for five minutes. Electron-beam lithography (EBL) etches each KLayout pattern out of the polymer, and each chip was developed with methyl isobutyl ketone (MIBK), then stopped with isopropanol (IPA). Electron-beam evaporation (EBE) is used to evaporate materials onto the chips in uniform quality. For alignment marks and prepatterned contacts, 0.05 nm of titanium is first evaporated, then 0.5 nm of gold to improve intactness. The chips are placed in an acetone bath at 60°C overnight, then washed off with additional acetone and IPA. This process reveals the patterns in gold on the substrate chips **(Fig. 3).**

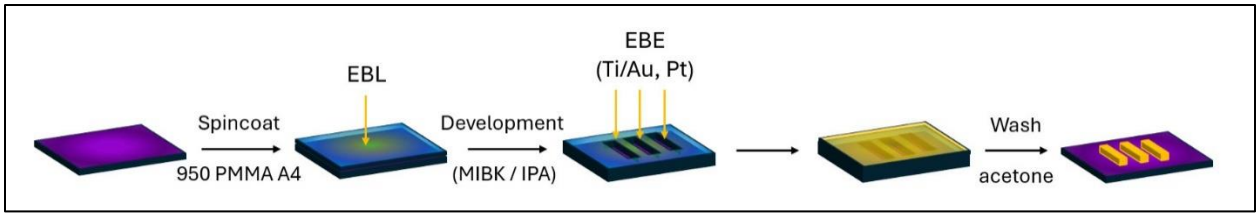

Figure 3. Patterning process using EBL and EBE onto SiO_2

Dry Transfer

The samples are stacked by the dry transfer method to create the heterostructure. For the test device, the PowerPoint design was used as reference, tracing the shapes onto a plastic sheet to determine proper positioning. We placed a 0.5 cm by 0.5 cm piece of Polydimethylsiloxane (PDMS) onto a clean microscope slide, then a 0.3 cm by 0.3 cm piece of Poly(Bisphenol A Carbonate) (PC) on top to create a transfer slide, adjusting to avoid bubbles or debris in the stack **(Fig. 4)**.

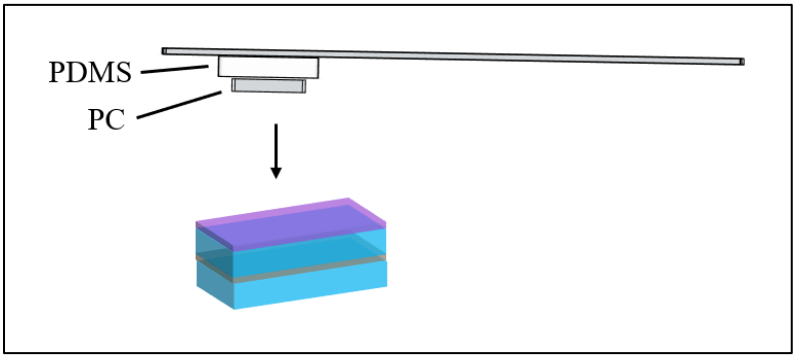

Figure 4. PDMS / PC transfer slide for stacking heterostructure

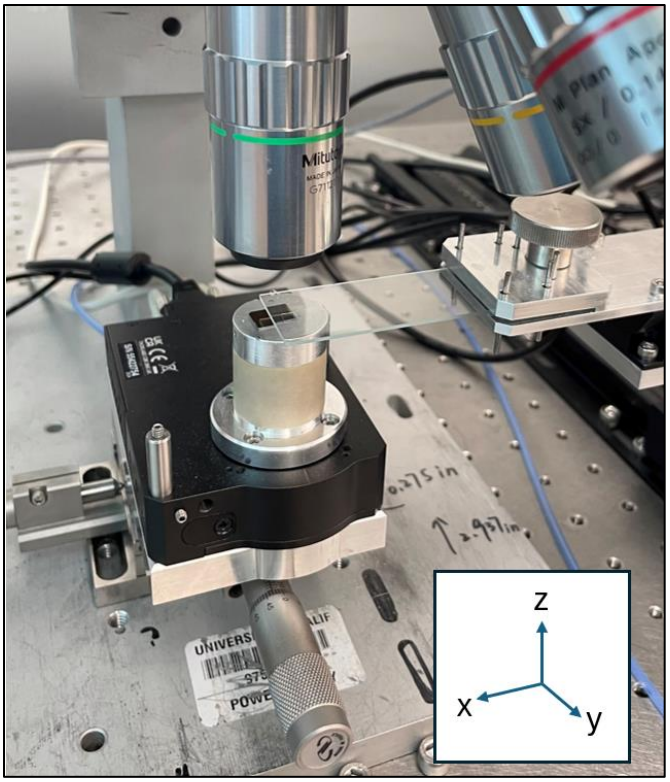

Figure 5. Transfer stage setup allows for adjustment of chip and stamp position

The transfer stage has two components: the sample stage and transfer slide adjustment **(Fig. 5)**. To pick up, both components are adjusted by the x and y axes, and the slide component can be lifted and dropped by the z axis adjustment. This helps to align the chip and stamp position to ensure accurate and successful transfer of the samples. Because PC increases in adhesiveness and melts with higher temperature, the transfer slide is heated depending on the pickup material, then lowered slowly to the chip. The sample and stamp are cooled, then lifted back up to reveal the picked-up sample on the PC. We performed this procedure for each layer of the heterostructure, stacking each component of the device from top to bottom. In the final step to drop off the stack, we place the stamp down to the substrate with gold prepatterned contacts, then melt the PC off onto the substrate, peeling the PDMS back. With the PC and stack on the chip, we place the sample

into a beaker of chloroform after a waiting period of 16 hours. The sample is then washed with IPA to fully remove debris and reveal a clean device.

For the Hall Bar device, we have transferred the bottom graphite gate and h-BN, in anticipation of Hall bar patterning, followed by a final transfer session of top graphite gate, top h-BN, and the WSe_2 monolayer.

Measurements

We use a home-built confocal microscope to perform photoluminescence at room (293 K) and cryogenic temperatures (1.7 K). We use a 630nm HeNe laser as the excitation, which we position onto the TMD layer, and capture the emitted light into a spectrometer. The collected light is dispersed onto a CCD camera which gives intensity as a function of the wavelength of light. We apply voltage onto the wire-bonded sample by using a Keithley 2400 which is connected to our cryostat's probe wiring (Attodry 2100).

IV. RESULTS

When illuminating the sample in our test device with laser excitation of 630 nm at room temperature (293 K), we identified exciton activity in a broad peak between the application range of approximately -2 V to 0.5 V, within 750 – 760 nm **(Fig. 6)**. Above 0.5 V, the signal does not appear, indicating doping of the sample. The mild peak between the application of -4 V to -2.5 V is expected to be a trion peak.

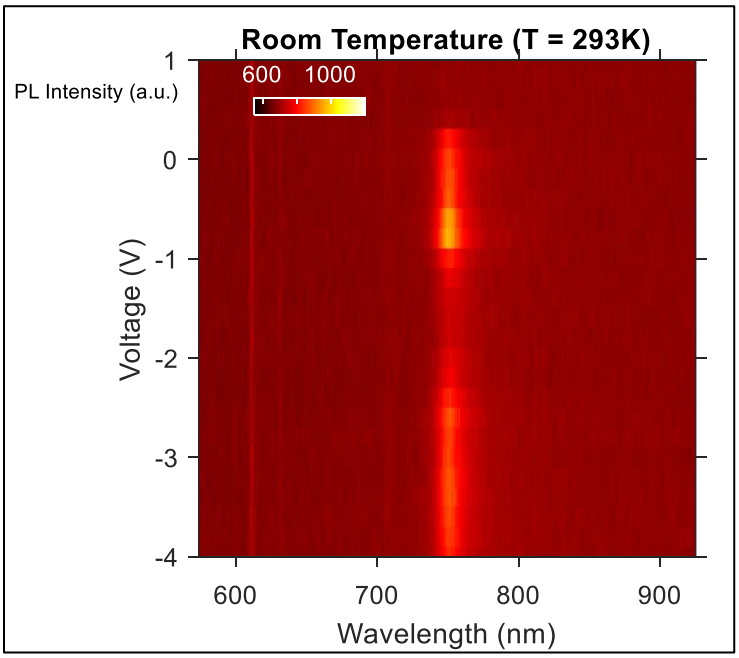

Figure 6. PL for input voltages -4 V to 1 V using a step size of 0.2 V

When illuminating at a low temperature of 1.7 K, we identify the neutral exciton peak X_0 at ~ 715 nm, charged exciton peak X_T at ~ 720 nm, and dark exciton peak X_D at 725 nm **(Fig. 7)**. Peaks X_0 and X_T demonstrate excitons with an in-plane dipole with spin-allowed radiative recombination. X_D is an out-of-plane dipole with spin-forbidden radiative recombination, where its emission is not entirely captured due to it being out-of-plane. When the electron-hole pair recombines, a photon is produced for radiative recombination. We also observe a peak towards the

bottom, moving from 720 nm to 725 nm as the applied voltage increases from -1.2 V to -4 V, indicating there is a red shift of a trion peak when a negative voltage is applied.

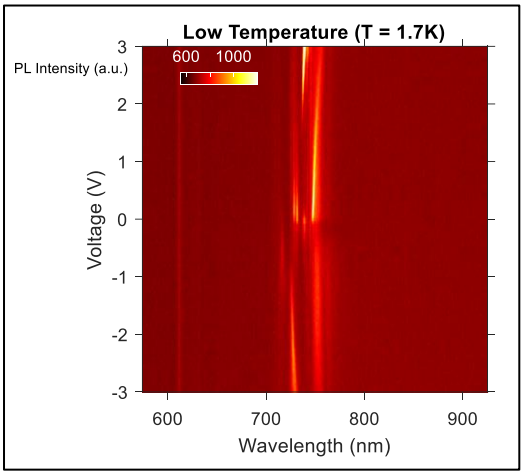

Figure 7. PL for input voltages -3 V to +3 V using step size of 0.05 V; Neutral exciton emission, charged exciton emission, and dark exciton emitting out-of-plane are identifiable

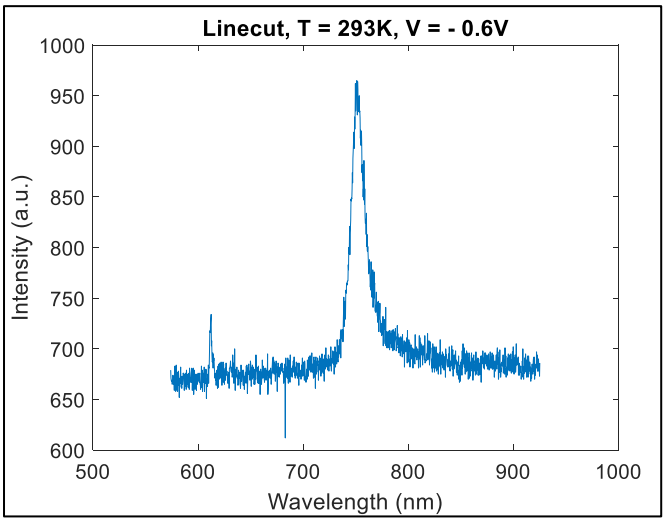

Figure 8. Horizontal linecut of PL plot at -0.6 V, illustrating a broad peak of exciton activity at approximately 750 nm

We take a linecut of Fig. 6 at ~0.6 V, where the peak is relatively intense **(Fig. 8)**. The broad single peak in the linecut does not allow for identification of different exciton types.

At low temperature, each peak occurs at different ranges of applied voltages and at a slightly different wavelength. Therefore, when taking linecuts at several voltages, we expect to see individual identifiable peaks for neutral, charged, and dark excitons as opposed to a single broad one as taken in room temperature. For instance, when taking a linecut at -0.55 V **(Fig. 9)**, we observe the neutral exciton peak X_0 at 715 nm. Likewise, taking linecuts at the respective voltages where X_T (720 nm) and X_D (725 nm) appear give a plot of a distinct peak for each.

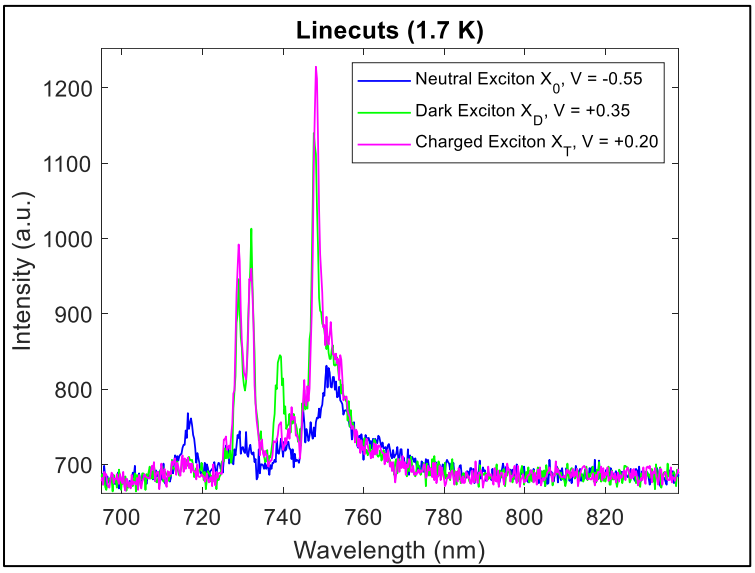

Figure 9. Horizontal linecuts of PL plot at low temperature 1.7K, with distinct, identifiable peaks

Focusing on the identifiable neutral exciton peak at low temperature **(Fig. 10)** and the broader peak at room temperature **(Fig. 11)**, we fit the peak to a Lorentzian function, commonly used to visualize the spectral shape as opposed to the Gaussian function.

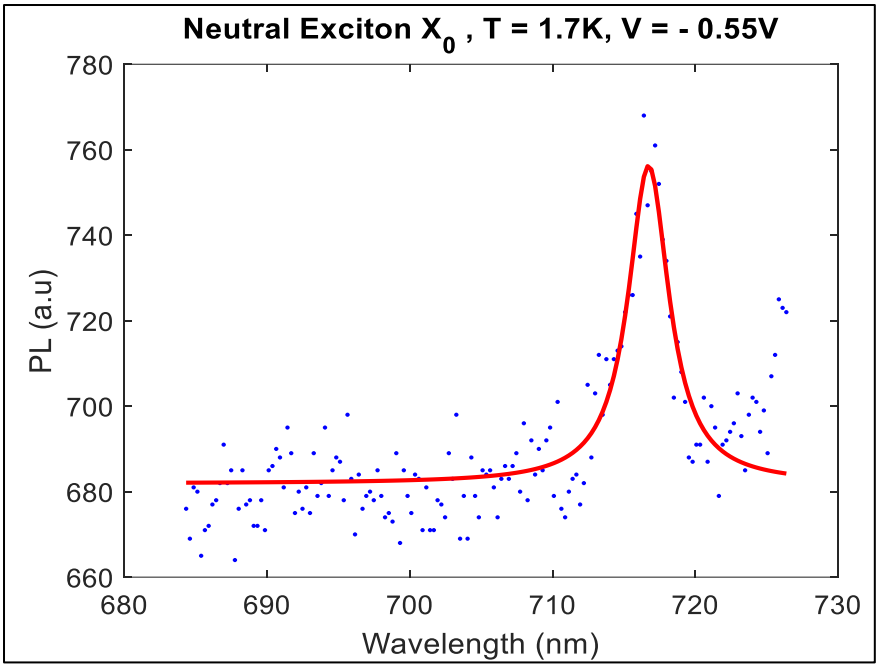

Figure 10. Neutral exciton emission peak of Fig. 4 fitted to the Lorentzian function

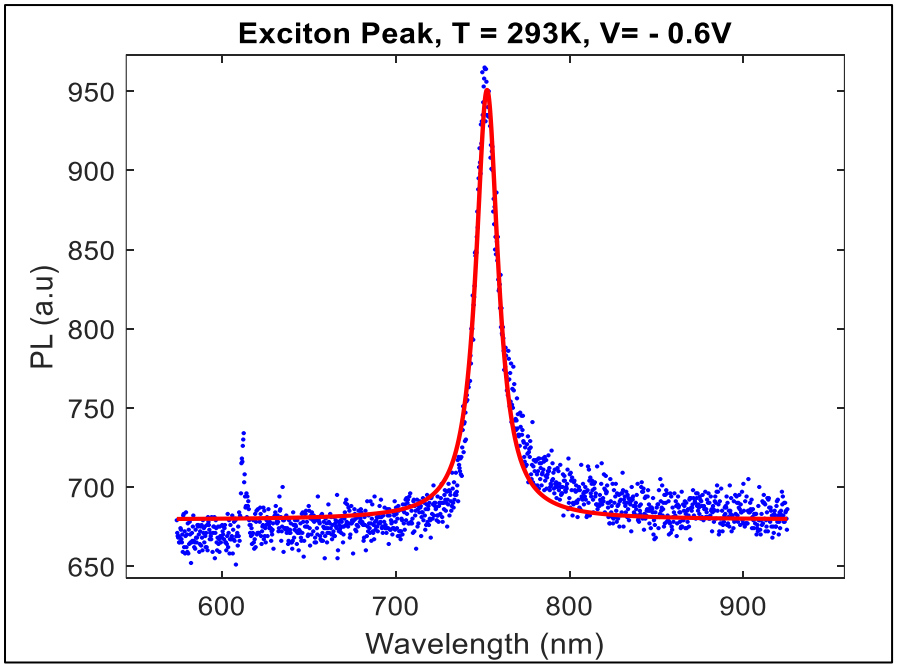

Figure 11. Exciton peak of Fig. 1 at 750 nm fitted to the Lorentzian function

V. DISCUSSION

With the PL data at 1.7 L, we identified the exciton peaks X_T, X_0, and X_D, indicating neutral exciton emission, charged exciton emission, and dark exciton emission out-of-plane, respectively. The peaks and their wavelengths are consistent with ones reported from Zhou, et al. (2017) for far-field PL. We identified and concluded gate-dependable exciton behavior in monolayer WSe_2, contrasting from broad single peak at 273 K.

From the linecuts illustrating the exciton peak at room temperature and neutral exciton emission peak at 1.7 K, we fit the linewidth (width at half maximum of aforementioned fitted peaks) with a Lorentzian function to be 34.5 meV and 8.4 meV, respectively. Linewidth tells the range of wavelengths as a width in a spectral line, which takes into account the uncertainty of the data point. It is more ideal to have a narrower linewidth, as a wide linewidth has a larger range of wavelengths and therefore a higher uncertainty. We compared our neutral exciton peak linewidth value to 2 – 4 meV as stated in Zhou, et al. (2017), concluding the WSe_2 monolayer is of relatively good quality, as a narrower linewidth indicates less defects from cleanliness or temperature, with more consistent exciton behavior.

As our data is comparable to accepted values and observations, we will proceed to continue with the fabrication of the Hall bar device. Electron doping, causing defects, causes energy dependent scattering. We will take PL measurements under the same temperatures—293 K and 1.7 K—to determine energy, as well as transport data from SdH oscillations and Hall mobility. When plotting the value of the applied perpendicular magnetic field against Hall resistance R_{xy}, we can estimate the hole carrier density. We expect to see a non-monotonic relation between doping and mobility. Following, we aim to study this further with other TMDs.

Alternatively, we can fabricate a monolayer WSe_2 device with contacts varying in distances across the length of the WSe_2, with an increase of one micron for each subsequent contact. Using the transmission length method (TLM), we will test the contact resistance of the monolayer WSe_2 by plotting the distances between this array of contacts against resistivity. We expect to see a positive, linear progression, where the y-intercept has the value of two times the value of contact resistivity R_c and has a slope of R_s / W, where R_s is sheet resistivity of the substrate and W is the contact width. With this, we are able to measure contact resistance, as a lower resistance value indicates better charge carrier injection, contributing to a more efficient and improved device.

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