



# CS 380 - GPU and GPGPU Programming

## Lecture 23: CUDA Memory, Pt. 4

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# Reading Assignment #13 (until Nov 30)

## Read (required):

- Programming Massively Parallel Processors book, 3<sup>rd</sup> edition  
Chapter 9 (Parallel patterns – parallel histogram computation)
- Programming Massively Parallel Processors book, 3<sup>rd</sup> edition  
Chapter 13 (CUDA dynamic parallelism)

## Read (optional):

- Prefix Sums and Their Applications, Guy Blelloch  
<https://www.cs.cmu.edu/~guyb/papers/Ble93.pdf>



# Memory and Cache Types

## Global memory

- [Device] L2 cache
- [SM] L1 cache (shared mem carved out; *or* L1 shared with tex cache)
- [SM/TPC] Texture cache (separate, or shared with L1 cache)
- [SM] Read-only data cache (storage might be same as tex cache)

## Shared memory

- [SM] Shareable only between threads in same thread block

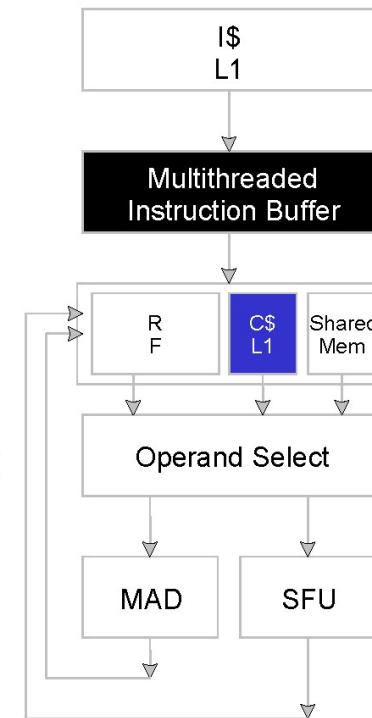
Constant memory: Constant (uniform) cache

Unified memory programming: Device/host memory sharing

# Constants

- Immediate address constants
- Indexed address constants
- Constants stored in DRAM, and cached on chip
  - L1 per SM
- A constant value can be broadcast to all threads in a Warp
  - Extremely efficient way of accessing a value that is common for all threads in a block!

```
// specify as global variable
__device__ __constant__ float gpuGamma[2];
...
// copy gamma value to constant device memory
cudaMemcpyToSymbol(gpuGamma, &gamma, sizeof(float));
// access as global variable in kernel
res = gpuGamma[0] * threadIdx.x;
```



# Texture Memory

---

- **Cached**, potentially exhibiting higher bandwidth if there is locality in the texture fetches;
- They are not subject to the constraints on memory access patterns that global or constant memory reads must respect to get good performance
- The latency of addressing calculations is hidden better, possibly improving performance for applications that perform random accesses to the data
- No penalty when accessing float4
- Optional
  - 8-bit and 16-bit integer input data may be optionally converted to 32-bit floatingpoint
  - Packed data may be broadcast to separate variables in a single operation;
  - values in the range [0.0, 1.0] or [-1.0, 1.0]
  - texture filtering
  - address modes, e.g. wrapping / texture borders

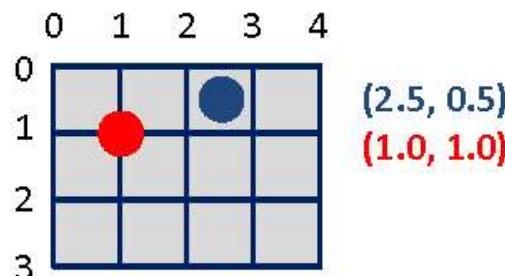


# Additional Texture Functionality

- **All of these are “free”**
  - Dedicated hardware
  - Must use CUDA texture objects
    - See CUDA Programming Guide for more details
    - Texture objects can interoperate graphics (OpenGL, DirectX)
- **Out-of-bounds index handling: clamp or wrap-around**
- **Optional interpolation**
  - Think: using fp indices for arrays
  - Linear, bilinear, trilinear
    - Interpolation weights are 9-bit
- **Optional format conversion**
  - {char, short, int, fp16} -> float



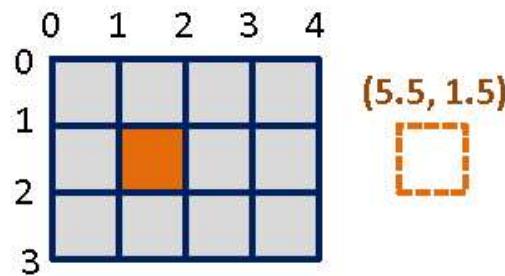
# Examples of Texture Object Indexing



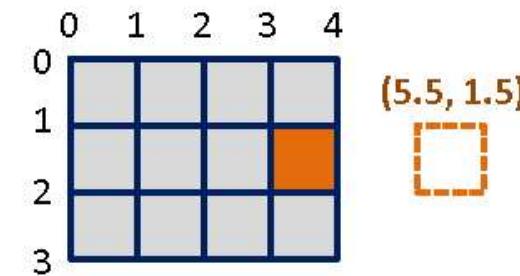
**Integer indices fall between elements**  
**Optional interpolation:**

Weights are determined by coordinate distance

## Index Wrap:



## Index Clamp:

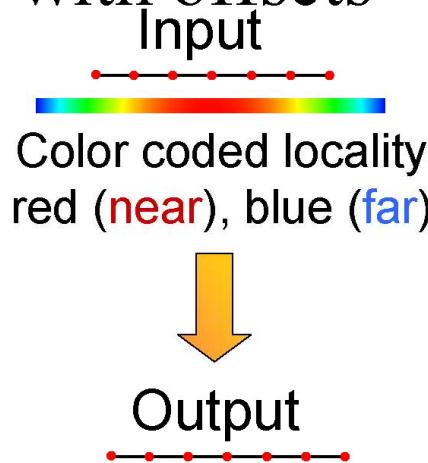


# Native Memory Layout – Data Locality

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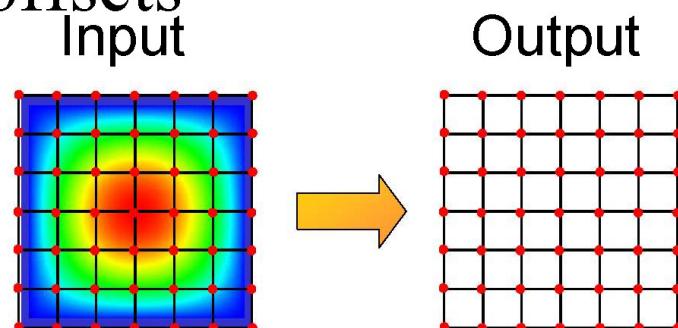
## CPU

- 1D input
- 1D output
- Other dimensions with offsets



## GPU

- 2D input
- 2D output
- Other dimensions with offsets

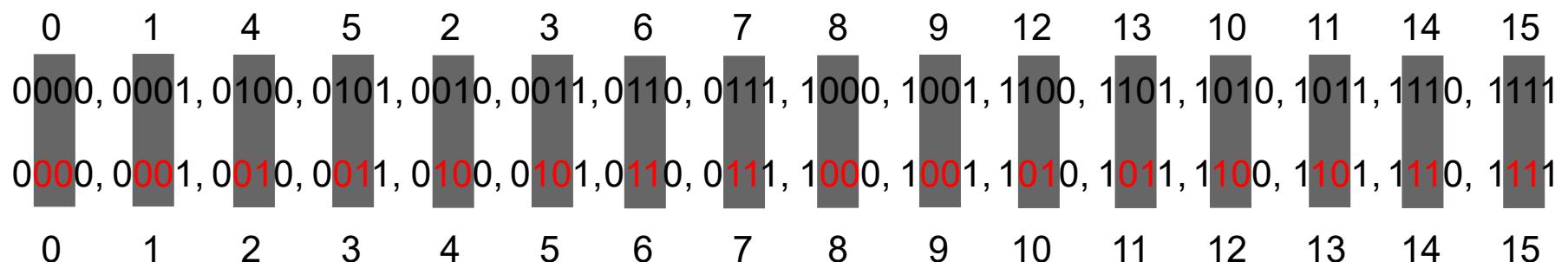
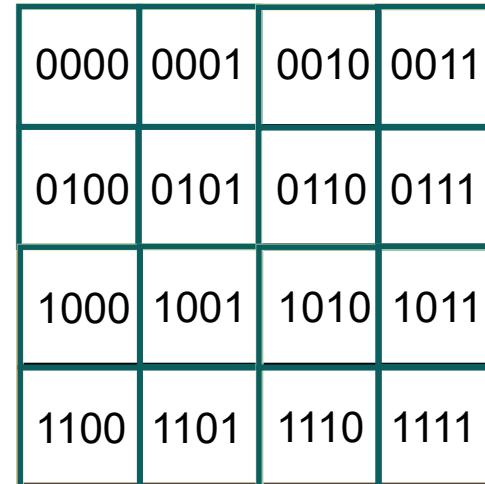
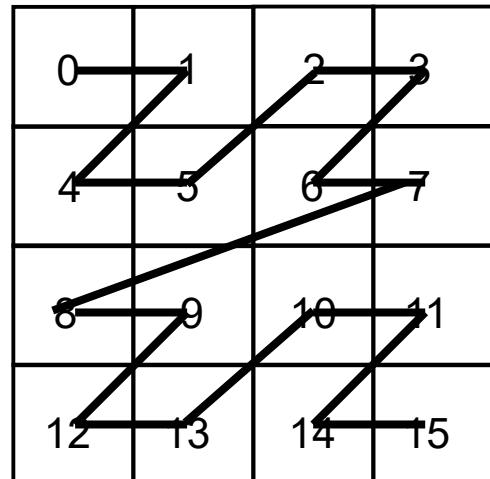


# Space-Filling Curves: Morton Order (Z Order)



# Map higher-dimensional space to 1D

- Z-order: Equivalent to quadtree (octree in 3D) depth-first traversal order



# 1D Access

---

- **Access to linear Cuda memory**

```
float4* pos; cudaMalloc( (void**)&pos, x*sizeof(float4) );
```

- **Texture reference**

- type
  - access/filtering mode

```
// global texture reference  
texture< float4, 1, cudaMemcpyElementType> texPos;
```

- **Bind to linear array**

```
cudaBindTexture(0, texPos, pos, x*sizeof(float4));  
cudaUnbindTexture(texPos);
```

- **Within kernel**

```
float4 pa1 = tex1Dfetch( texPos, threadIdx.x);
```

- **Writing to a texture that is currently read by some threads is undefined!!!**

# 2D Access

---

- Optimized for 2D / 3D locality

```
texture< float4, 2, cudaMemcpyElementType> texImg;
```

- Requires binding to **special Array memory – special memory layout**

```
cudaChannelFormatDesc floatTex =  
cudaCreateChannelDesc<float4>();  
  
float4* src;  
  
cudaArray* img;  
  
cudaMallocArray( &img, &floatTex, w, h);  
cudaMemcpyToArray(img, 0, 0, src, w*h*sizeof(float4),  
cudaMemcpyHostToDevice);  
cudaBindTextureToArray( texImg, img, floatTex) );  
cudaUnbindTexture(texImg);
```

# 2D Access

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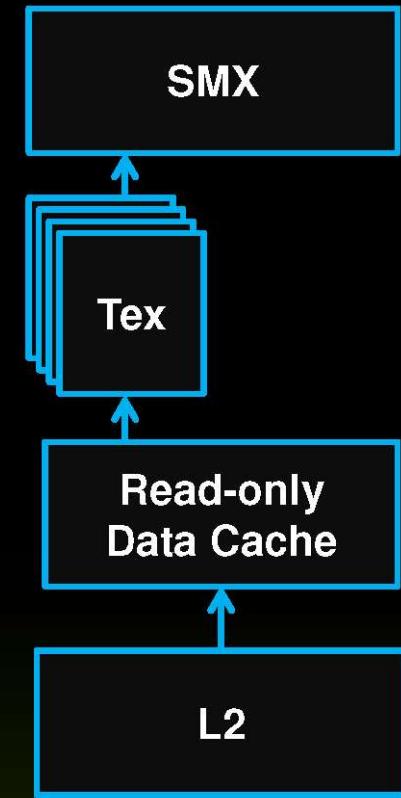
- **Within kernel**

```
float4 r = tex2D( texImg, x +xoff, y+yoff);
```

- **Pros**
  - optimized for 2D locality (optimized memory layout / spacefilling curve)
- **Cons**
  - If the result of some kernel should be used as 2D texture  
`cudaMemcpyToArray` is required
  - You cannot write to a texture which is currently read from
- **CUDA “surfaces” are writeable textures!**

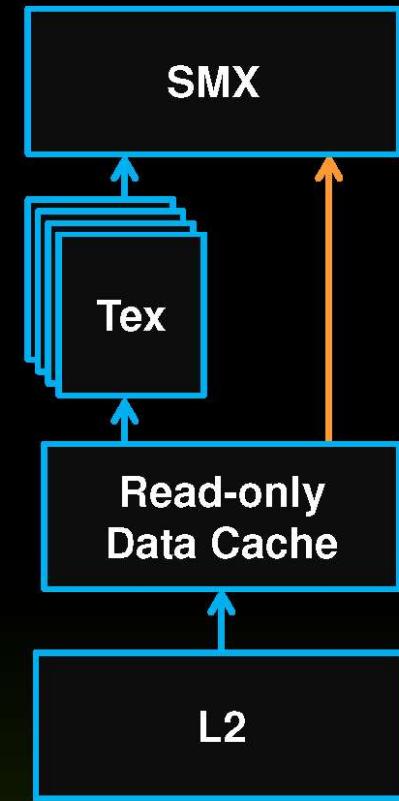
# Texture performance

- **Texture :**
  - Provides hardware accelerated filtered sampling of data (1D, 2D, 3D)
  - Read-only data cache holds fetched samples
  - Backed up by the L2 cache
- **SMX vs Fermi SM :**
  - 4x filter ops per clock
  - 4x cache capacity



# Texture Cache Unlocked

- Added a new path for compute
  - Avoids the texture unit
  - Allows a global address to be fetched and cached
  - Eliminates texture setup
- Why use it?
  - Separate pipeline from shared/L1
  - Highest miss bandwidth
  - Flexible, e.g. unaligned accesses
- Managed automatically by compiler
  - “`const __restrict`” indicates eligibility





## Global Memory Accesses

- Memory coalescing
- Cached memory access

# Memory Layout of a Matrix in C

M <sub>0,0</sub>	M <sub>1,0</sub>	M <sub>2,0</sub>	M <sub>3,0</sub>
M <sub>0,1</sub>	M <sub>1,1</sub>	M <sub>2,1</sub>	M <sub>3,1</sub>
M <sub>0,2</sub>	M <sub>1,2</sub>	M <sub>2,2</sub>	M <sub>3,2</sub>
M <sub>0,3</sub>	M <sub>1,3</sub>	M <sub>2,3</sub>	M <sub>3,3</sub>

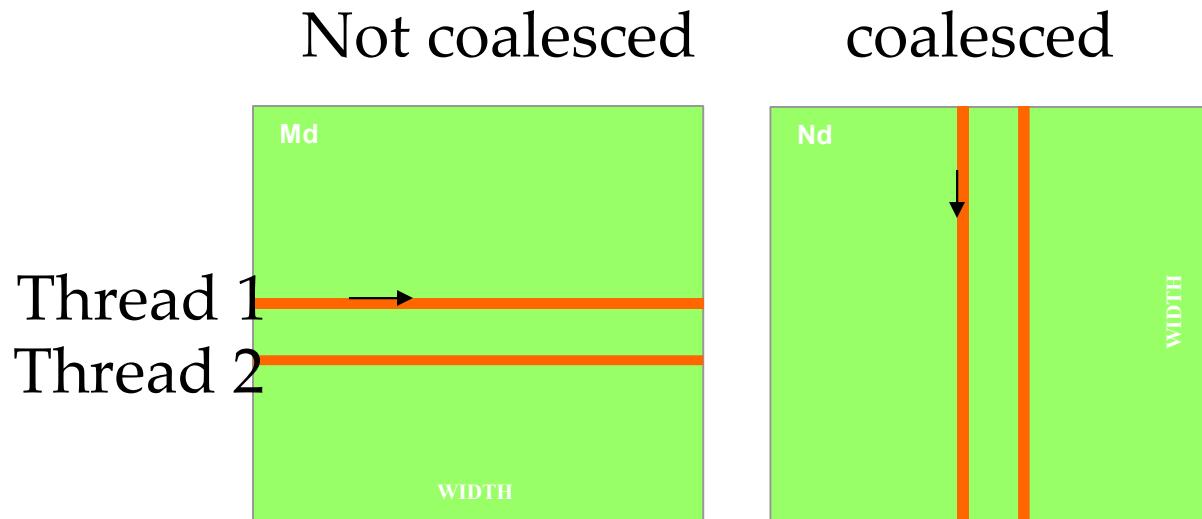
M



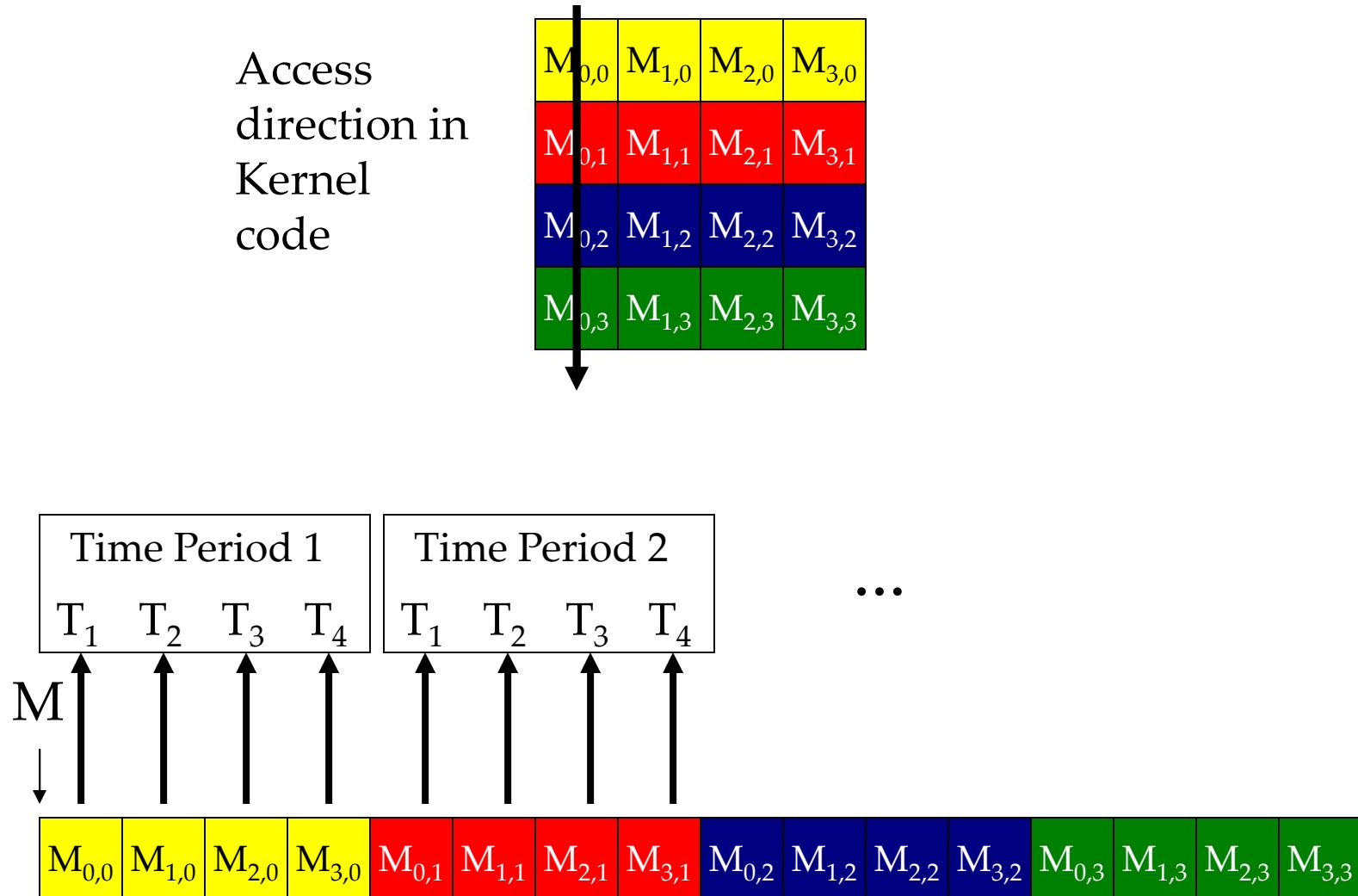
M <sub>0,0</sub>	M <sub>1,0</sub>	M <sub>2,0</sub>	M <sub>3,0</sub>	M <sub>0,1</sub>	M <sub>1,1</sub>	M <sub>2,1</sub>	M <sub>3,1</sub>	M <sub>0,2</sub>	M <sub>1,2</sub>	M <sub>2,2</sub>	M <sub>3,2</sub>	M <sub>0,3</sub>	M <sub>1,3</sub>	M <sub>2,3</sub>	M <sub>3,3</sub>
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# Memory Coalescing

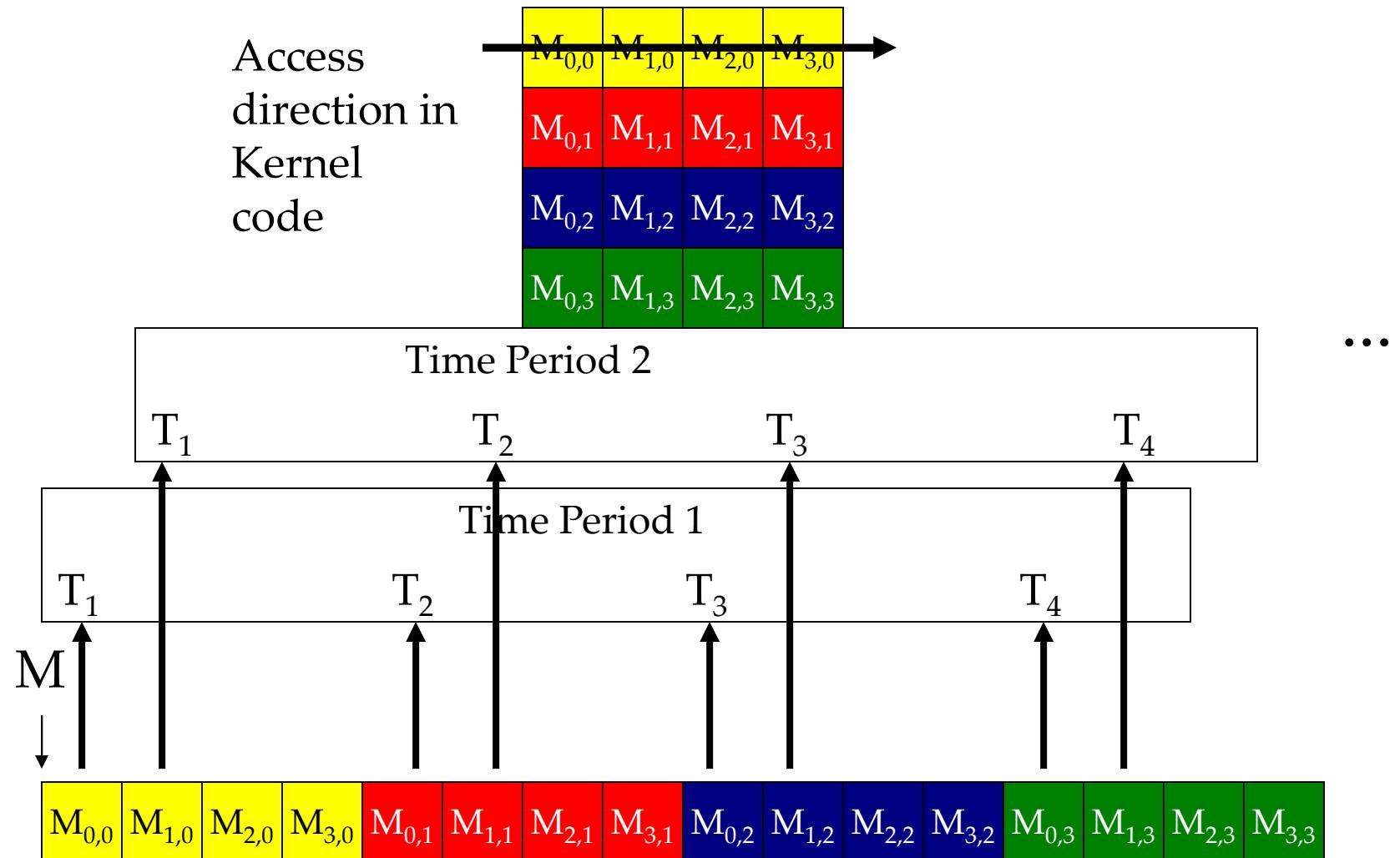
- When accessing global memory, peak performance utilization occurs when all threads in a half warp (**full warp on Fermi**) access continuous memory locations.
- Requirements relaxed on  $\geq 1.2$  devices; L1 cache on Fermi!



# Memory Layout of a Matrix in C



# Memory Layout of a Matrix in C



# Global Memory Acc.

CUDA 6.5 (cc. 1.0 – 3.x)

Cached on Fermi (cc. 2.x)  
and higher

L1 cache per SM

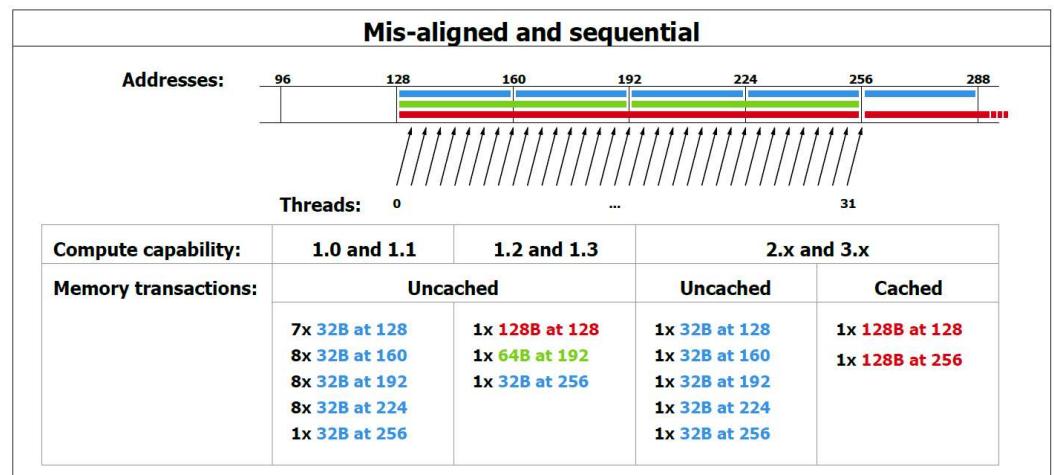
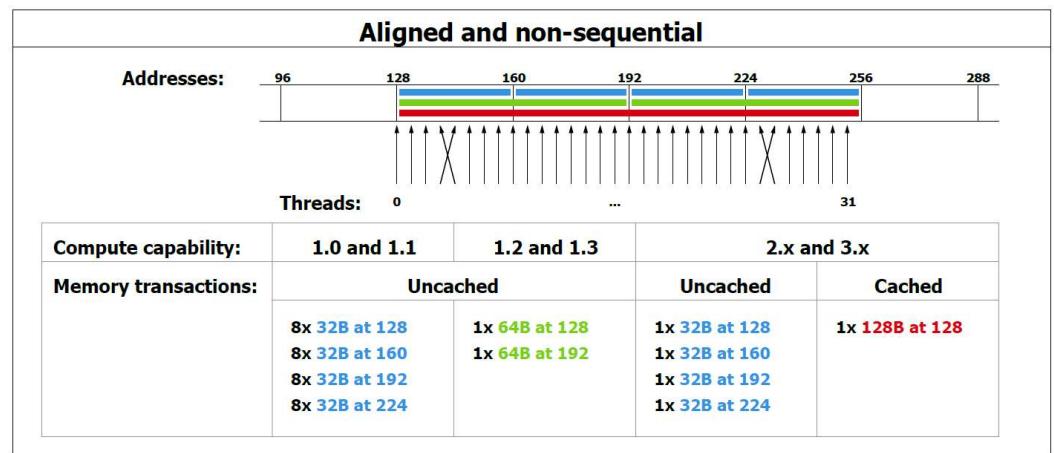
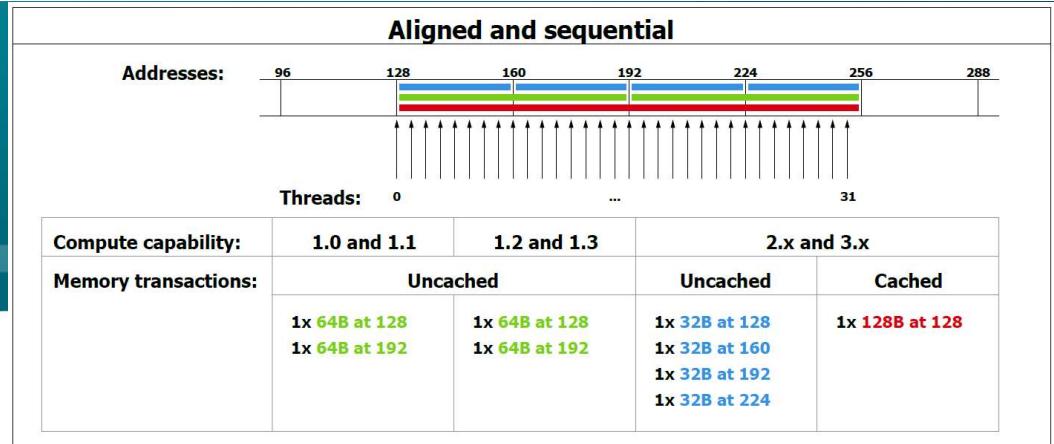
Global L2 cache

Compile time flag can choose:

- Caching in both L1 and L2
- Caching only in L2

Cache line size (L1, L2):

- 128 bytes



# Global Memory Access Arch. Differences (1)



Aligned and sequential							
Addresses:	96	128	160	192	224	256	288
Threads:	0	...				31	
Compute capability:	1.0 and 1.1		1.2 and 1.3		2.x and 3.0		
Memory transactions:	Uncached			Cached			
	1 x 64B at 128		1 x 64B at 128		1 x 128B at 128		
	1 x 64B at 192		1 x 64B at 192				

# Global Memory Access Arch. Differences (2)



Aligned and non-sequential							
Addresses:	96	128	160	192	224	256	288
Threads:	0			...		31	
Compute capability:	1.0 and 1.1		1.2 and 1.3		2.x and 3.0		
Memory transactions:	Uncached			Cached			
	8 x 32B at 128		1 x 64B at 128		1 x 128B at 128		
	8 x 32B at 160		1 x 64B at 192				
	8 x 32B at 192						
	8 x 32B at 224						

# Global Memory Access Arch. Differences (3)



Misaligned and sequential									
Addresses:	96	128	160	192	224	256	288		
Threads:	0	...				31			
Compute capability:	1.0 and 1.1			1.2 and 1.3		2.x and 3.0			
Memory transactions:	Uncached			Cached					
	7 x 32B at 128		1 x 128B at 128	1 x 128B at 128		1 x 128B at 128			
	8 x 32B at 160		1 x 64B at 192	1 x 128B at 256					
	8 x 32B at 192		1 x 32B at 256						
	8 x 32B at 224								
	1 x 32B at 256								



# Compute Capab. 3.x (Kepler, Part 3)

Global memory accesses for devices of compute capability 3.x are cached in L2 and for devices of compute capability 3.5 or 3.7, may also be cached in the read-only data cache described in the previous section; they are normally not cached in L1. Some devices of compute capability 3.5 and devices of compute capability 3.7 allow opt-in to caching of global memory accesses in L1 via the **-Xptxas -dlcm=ca** option to **nvcc**.

A cache line is 128 bytes and maps to a 128 byte aligned segment in device memory. Memory accesses that are cached in both L1 and L2 are serviced with 128-byte memory transactions whereas memory accesses that are cached in L2 only are serviced with 32-byte memory transactions. Caching in L2 only can therefore reduce over-fetch, for example, in the case of scattered memory accesses.



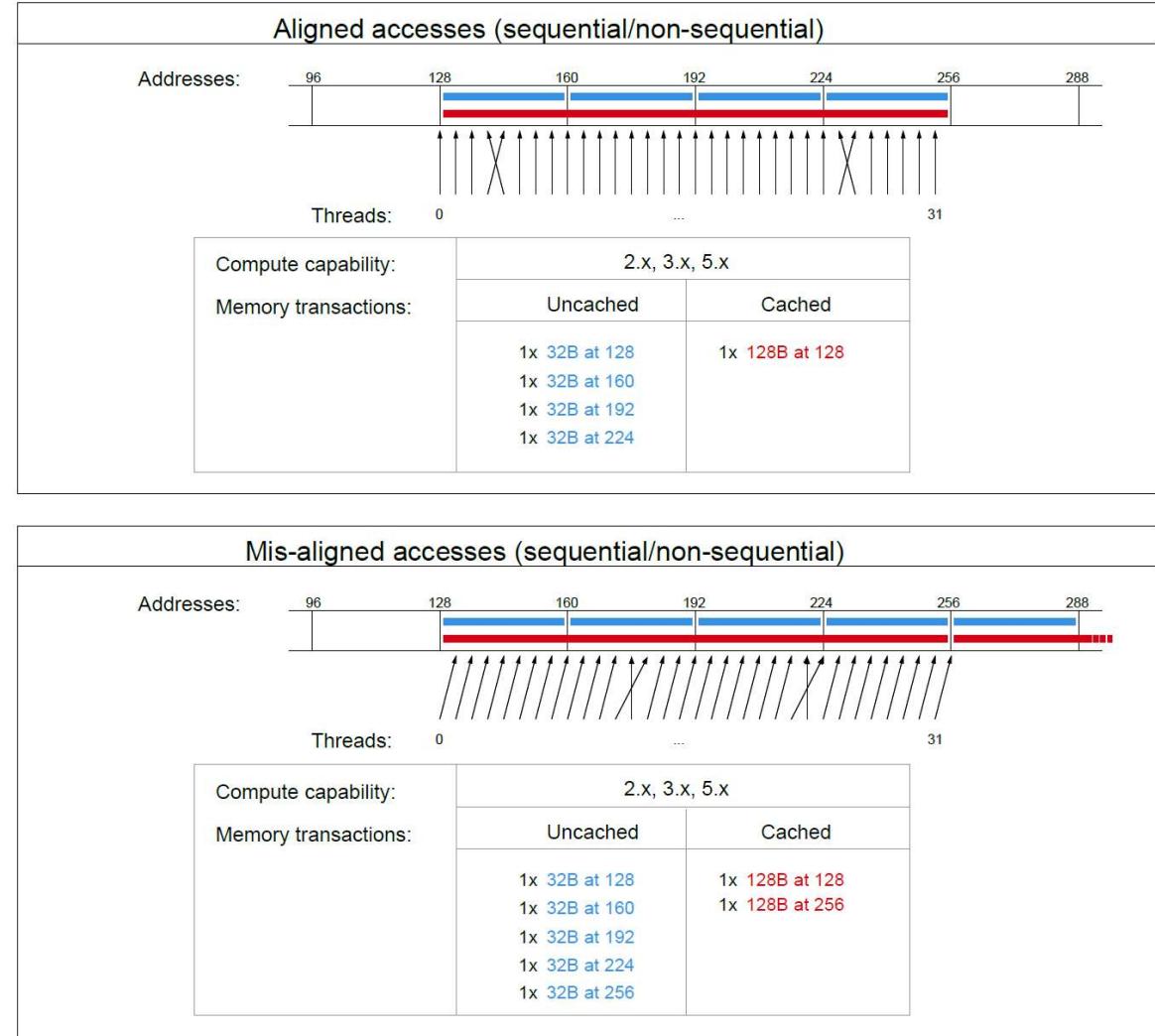
# Global Memory Access

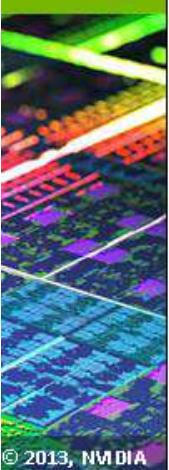
all recent  
compute capabilities  
(- 8.x)

Beware:

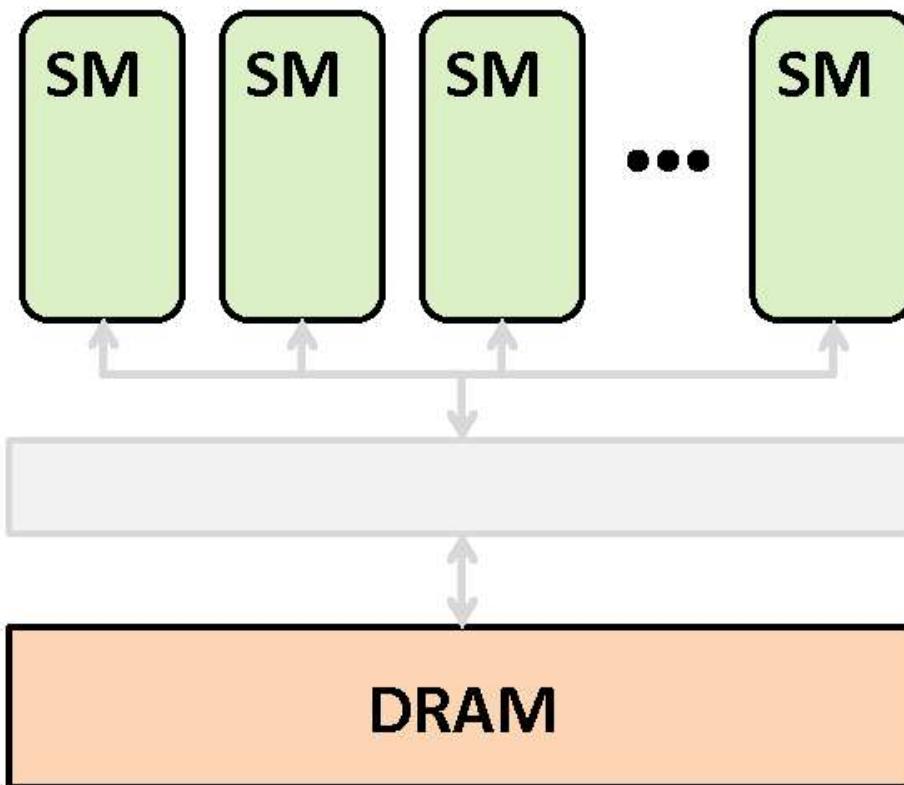
*Uncached here means  
not cached in L1*

*the L2 cache is  
always used!*

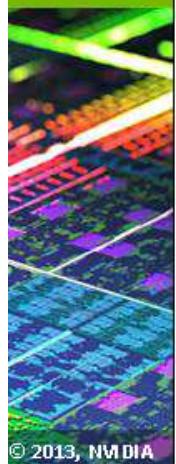




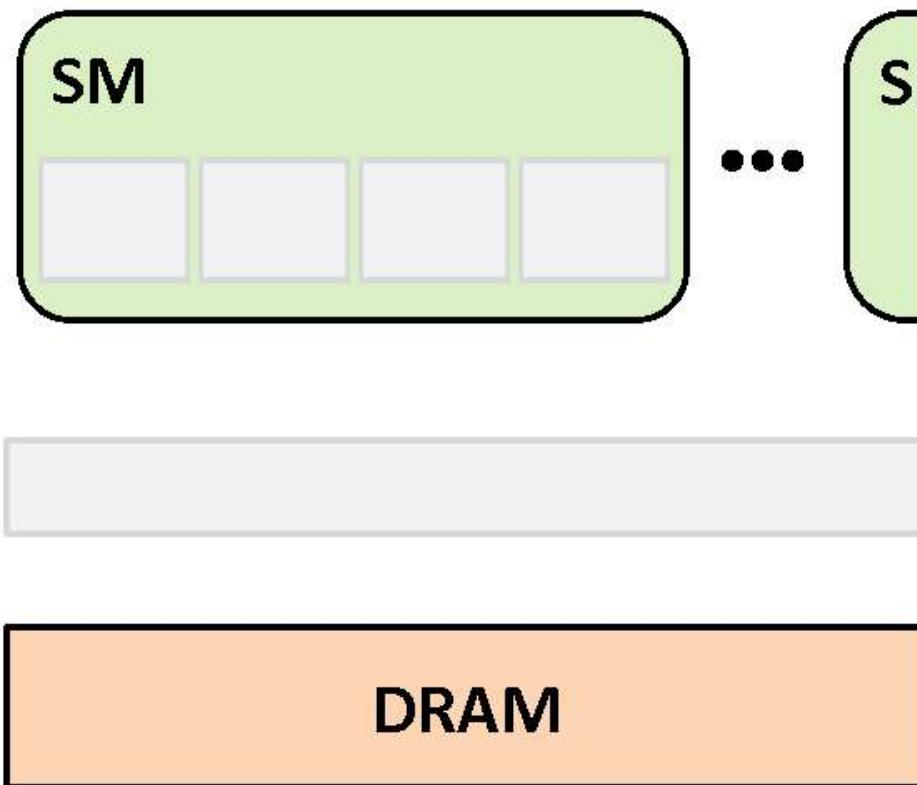
# Maximize Byte Use



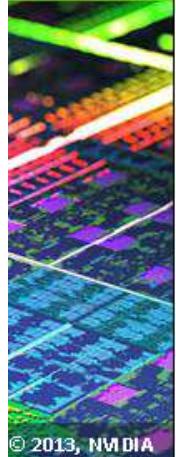
- **Two things to keep in mind:**
  - Memory accesses are per warp
  - Memory is accessed in discrete chunks
    - lines/segments
    - want to make sure that bytes that travel from DRAM to SMs get used
  - For that we should understand how memory system works
- **Note: not that different from CPUs**
  - x86 needs SSE/AVX memory instructions to maximize performance



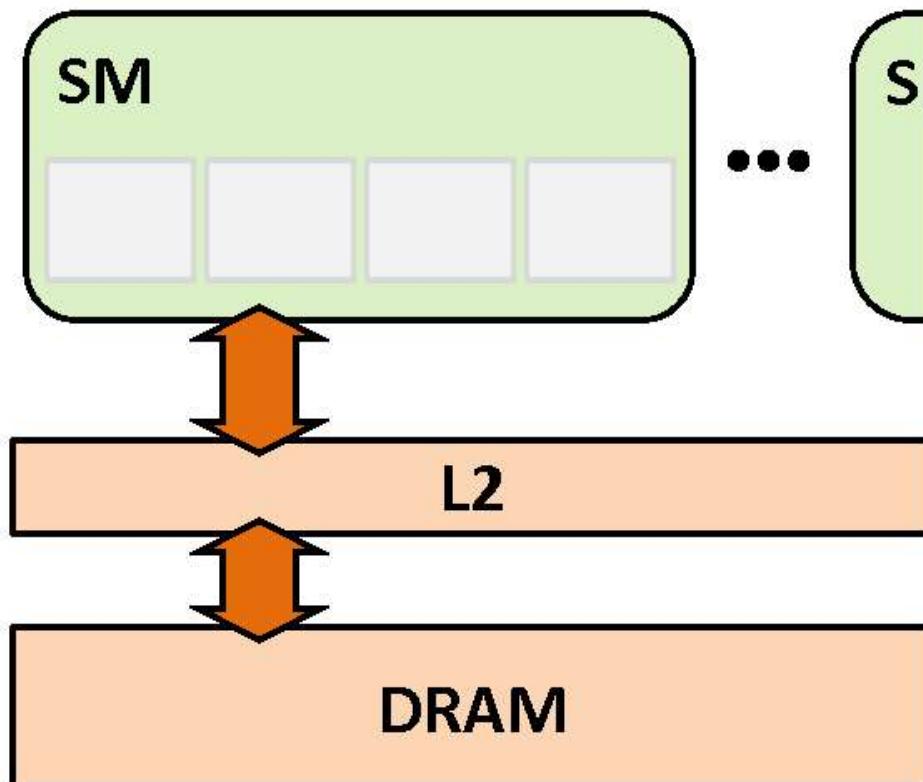
# GPU Memory System



- All data lives in DRAM
  - Global memory
  - Local memory
  - Textures
  - Constants

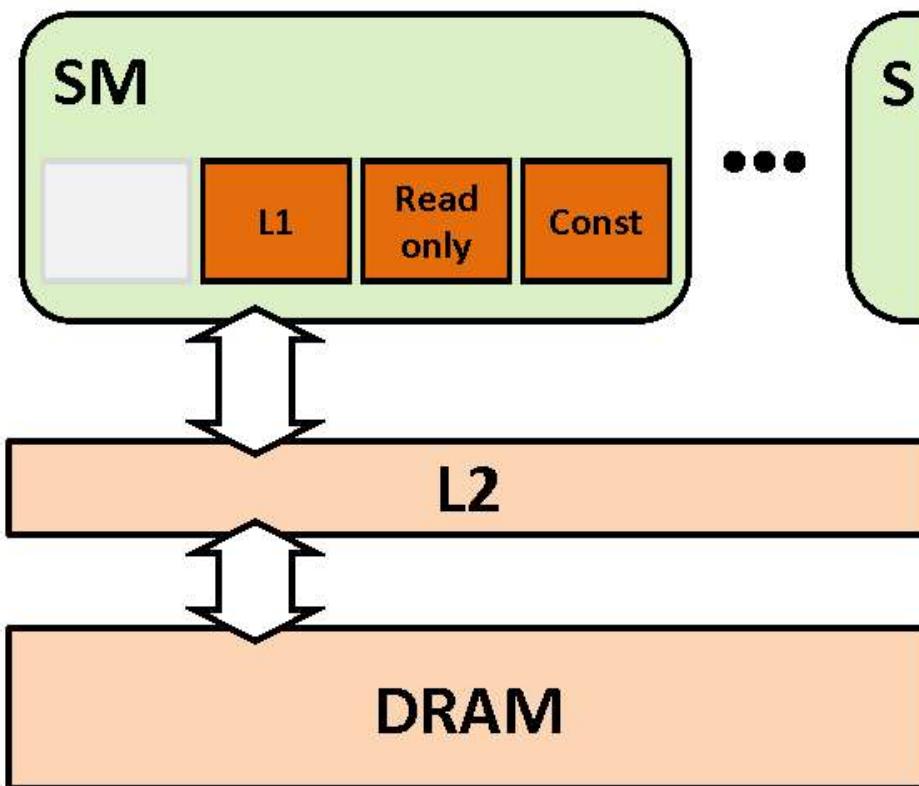


# GPU Memory System



- All DRAM accesses go through L2
- Including copies:
  - P2P
  - CPU-GPU

## GPU Memory System

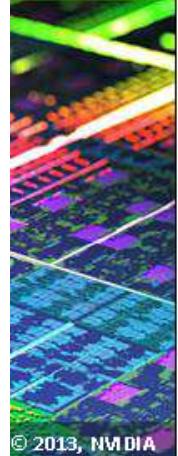


- Once in an SM, data goes into one of 3 caches/buffers
- Programmer's choice
  - L1 is the “default”
  - Read-only, Const require explicit code



# Access Path

- **L1 path**
  - Global memory
    - Memory allocated with `cudaMalloc()`
    - Mapped CPU memory, peer GPU memory
    - Globally-scoped arrays qualified with `__global__`
  - Local memory
    - allocation/access managed by compiler so we'll ignore
- **Read-only/TEX path**
  - Data in texture objects, CUDA arrays
  - CC 3.5 and higher:
    - Global memory accessed via intrinsics (or specially qualified kernel arguments)
- **Constant path**
  - Globally-scoped arrays qualified with `__constant__`



## Access Via L1

- **Natively supported word sizes per thread:**
  - 1B, 2B, 4B, 8B, 16B
    - Addresses must be aligned on word-size boundary
  - Accessing types of other sizes will require multiple instructions
- **Accesses are processed per warp**
  - Threads in a warp provide 32 addresses
    - Fewer if some threads are inactive
  - HW converts addresses into memory transactions
    - Address pattern may require multiple transactions for an instruction
    - If  $N$  transactions are needed, there will be ( $N-1$ ) replays of the instruction

# Compute Capab. 3.x (Kepler, Part 4)



If the size of the words accessed by each thread is more than 4 bytes, a memory request by a warp is first split into separate 128-byte memory requests that are issued independently:

- ▶ Two memory requests, one for each half-warp, if the size is 8 bytes,
- ▶ Four memory requests, one for each quarter-warp, if the size is 16 bytes.

Each memory request is then broken down into cache line requests that are issued independently. A cache line request is serviced at the throughput of L1 or L2 cache in case of a cache hit, or at the throughput of device memory, otherwise.

Note that threads can access any words in any order, including the same words.

Data that is read-only for the entire lifetime of the kernel can also be cached in the read-only data cache described in the previous section by reading it using the `_ldg()` function (see [Read-Only Data Cache Load Function](#)). When the compiler detects that the read-only condition is satisfied for some data, it will use `_ldg()` to read it. The compiler might not always be able to detect that the read-only condition is satisfied for some data. Marking pointers used for loading such data with both the `const` and `_restrict_` qualifiers increases the likelihood that the compiler will detect the read-only condition.



# Vectorized Memory Access

See <https://devblogs.nvidia.com/cuda-pro-tip-increase-performance-with-vectorized-memory-access/>

```
__global__ void device_copy_vector2_kernel(int* d_in, int* d_out, int N) {
    int idx = blockIdx.x * blockDim.x + threadIdx.x;
    for (int i = idx; i < N/2; i += blockDim.x * gridDim.x) {
        reinterpret_cast<int2*>(d_out)[i] = reinterpret_cast<int2*>(d_in)[i];
    }

    // in only one thread, process final element (if there is one)
    if (idx==N/2 && N%2==1)
        d_out[N-1] = d_in[N-1];
}

void device_copy_vector2(int* d_in, int* d_out, int n) {
    threads = 128;
    blocks = min((N/2 + threads-1) / threads, MAX_BLOCKS);

    device_copy_vector2_kernel<<<blocks, threads>>>(d_in, d_out, N);
}
```

```
/*0088*/           IMAD R10.CC, R3, R5, c[0x0][0x140]
/*0090*/           IMAD.HI.X R11, R3, R5, c[0x0][0x144]
/*0098*/           IMAD R8.CC, R3, R5, c[0x0][0x148]
/*00a0*/           LD.E.64 R6, [R10]
/*00a8*/           IMAD.HI.X R9, R3, R5, c[0x0][0x14c]
/*00c8*/           ST.E.64 [R8], R6
```

## SASS

LD.E.64, LD.E.128,  
ST.E.64, ST.E.128



# Vectorized Memory Access

See <https://devblogs.nvidia.com/cuda-pro-tip-increase-performance-with-vectorized-memory-access/>

```
__global__ void device_copy_vector4_kernel(int* d_in, int* d_out, int N) {
    int idx = blockIdx.x * blockDim.x + threadIdx.x;
    for(int i = idx; i < N/4; i += blockDim.x * gridDim.x) {
        reinterpret_cast<int4*>(d_out)[i] = reinterpret_cast<int4*>(d_in)[i];
    }

    // in only one thread, process final elements (if there are any)
    int remainder = N%4;
    if (idx==N/4 && remainder!=0) {
        while(remainder) {
            int idx = N - remainder--;
            d_out[idx] = d_in[idx];
        }
    }
}

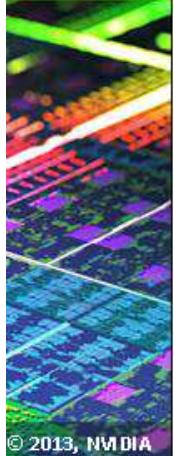
void device_copy_vector4(int* d_in, int* d_out, int N) {
    int threads = 128;
    int blocks = min((N/4 + threads-1) / threads, MAX_BLOCKS);

    device_copy_vector4_kernel<<<blocks, threads>>>(d_in, d_out, N);
}
```

```
/*0090*/          IMAD R10.CC, R3, R13, c[0x0][0x140]
/*0098*/          IMAD.HI.X R11, R3, R13, c[0x0][0x144]
/*00a0*/          IMAD R8.CC, R3, R13, c[0x0][0x148]
/*00a8*/          LD.E.128 R4, [R10]
/*00b0*/          IMAD.HI.X R9, R3, R13, c[0x0][0x14c]
/*00d0*/          ST.E.128 [R8], R4
```

SASS

LD.E.64, LD.E.128,  
ST.E.64, ST.E.128



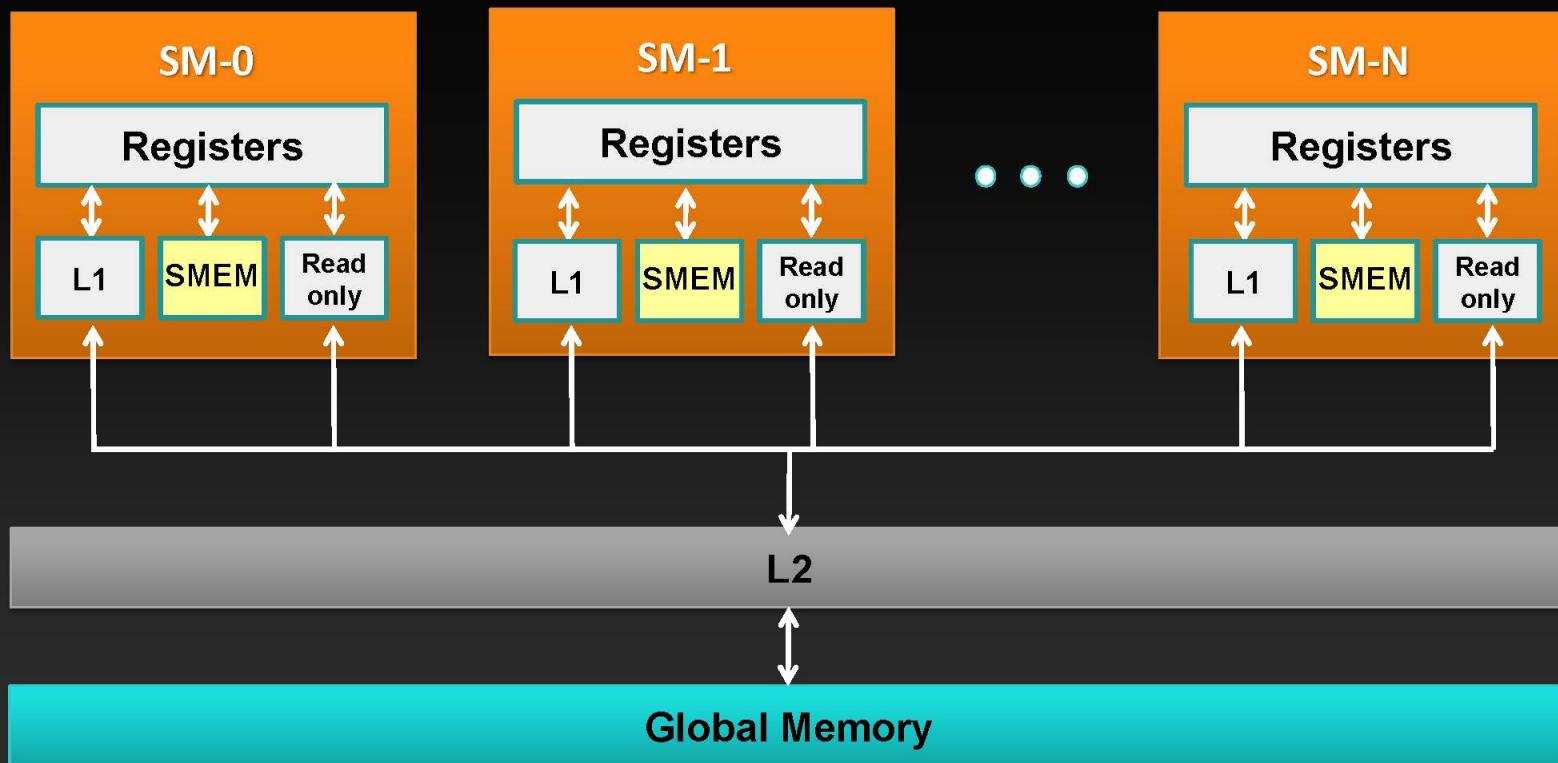
## GMEM Writes

- **Not cached in the SM**
  - Invalidate the line in L1, go to L2
- **Access is at 32 B segment granularity**
- **Transaction to memory: 1, 2, or 4 segments**
  - Only the required segments will be sent
- **If multiple threads in a warp write to the same address**
  - One of the threads will “win”
  - Which one is not defined

# OPTIMIZE

Kernel Optimizations: *Global Memory Throughput*

# Kepler Memory Hierarchy



# Load Operation

- Memory operations are issued **per warp** (32 threads)
  - Just like all other instructions
- Operation:
  - Threads in a warp provide memory addresses
  - Determine which lines/segments are needed
  - Request the needed lines/segments

# Memory Throughput Analysis

- Two perspectives on the throughput:
  - Application's point of view:
    - count only bytes requested by application
  - HW point of view:
    - count all bytes moved by hardware
- The two views can be different:
  - Memory is accessed at 32 byte granularity
    - Scattered/offset pattern: application doesn't use all the hw transaction bytes
  - Broadcast: the same small transaction serves many threads in a warp
- Two aspects to inspect for performance impact:
  - Address pattern
  - Number of concurrent accesses in flight

# Global Memory Operation

- **Memory operations are executed per warp**
  - 32 threads in a warp provide memory addresses
  - Hardware determines into which lines those addresses fall
    - Memory transaction granularity is 32 bytes
    - There are benefits to a warp accessing a contiguous aligned region of 128 or 256 bytes
- **Access word size**
  - **Natively supported sizes (per thread): 1, 2, 4, 8, 16 bytes**
    - Assumes that each thread's address is aligned on the word size boundary
  - If you are accessing a data type that's of non-native size, compiler will generate several load or store instructions with native sizes

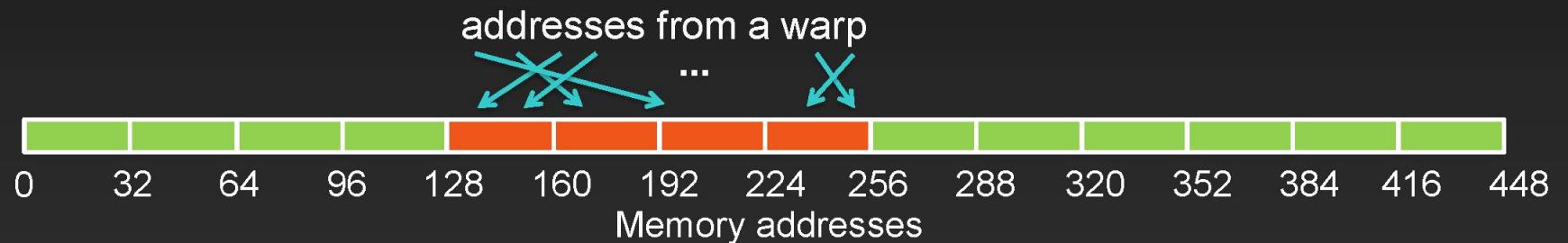
# Access Patterns vs. Memory Throughput

- Scenario:
    - Warp requests 32 aligned, consecutive 4-byte words
  - Addresses fall within 4 segments
    - Warp needs 128 bytes
    - 128 bytes move across the bus
    - Bus utilization: 100%



# Access Patterns vs. Memory Throughput

- Scenario:
    - Warp requests 32 aligned, permuted 4-byte words
  - Addresses fall within 4 segments
    - Warp needs 128 bytes
    - 128 bytes move across the bus
    - Bus utilization: 100%



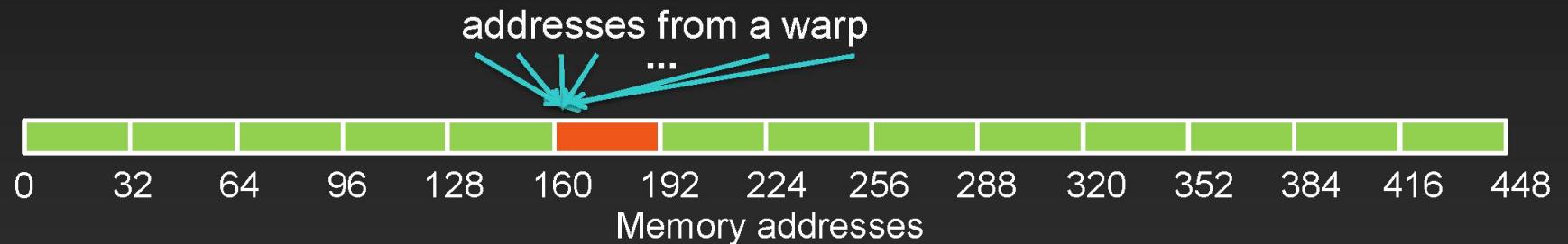
## Access Patterns vs. Memory Throughput

- Scenario:
  - Warp requests 32 misaligned, consecutive 4-byte words
- Addresses fall within at most 5 segments
  - Warp needs 128 bytes
  - At most 160 bytes move across the bus
  - Bus utilization: at least 80%
    - Some misaligned patterns will fall within 4 segments, so 100% utilization



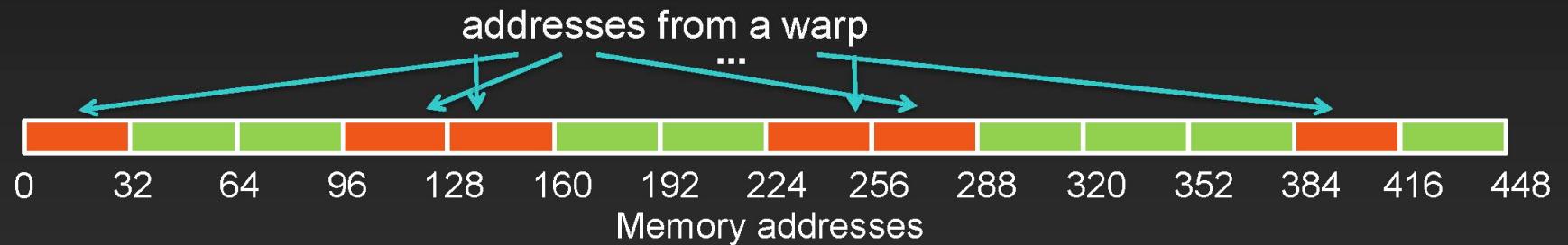
# Access Patterns vs. Memory Throughput

- Scenario:
  - All threads in a warp request the same 4-byte word
- Addresses fall within a single segment
  - Warp needs 4 bytes
  - 32 bytes move across the bus
  - Bus utilization: 12.5%



## Access Patterns vs. Memory Throughput

- Scenario:
  - Warp requests 32 scattered 4-byte words
- Addresses fall within  $N$  segments
  - Warp needs 128 bytes
  - $N \times 32$  bytes move across the bus
  - Bus utilization:  $128 / (N \times 32)$



## Structures of Non-Native Size

- Say we are reading a 12-byte structure per thread

```
struct Position
{
    float x, y, z;
};

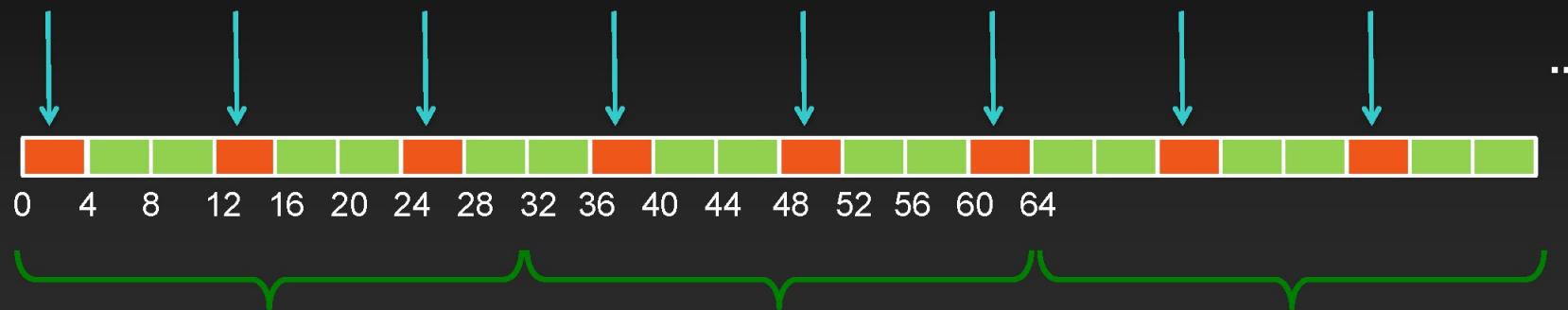
__global__ void kernel( Position *data, ... )
{
    int idx = blockIdx.x * blockDim.x + threadIdx.x;
    Position temp = data[idx];
    ...
}
```

## Structure of Non-Native Size

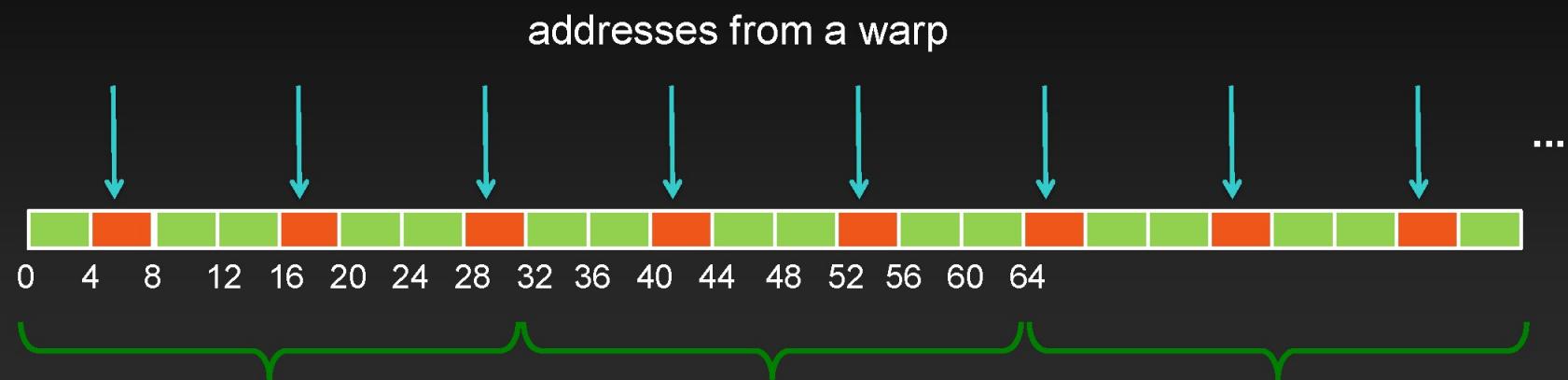
- Compiler converts `temp = data[idx]` into 3 loads:
  - Each loads 4 bytes
  - Can't do an 8 and a 4 byte load: 12 bytes per element means that every other element wouldn't align the 8-byte load on 8-byte boundary
- Addresses per warp for each of the loads:
  - Successive threads read 4 bytes at 12-byte stride

# First Load Instruction

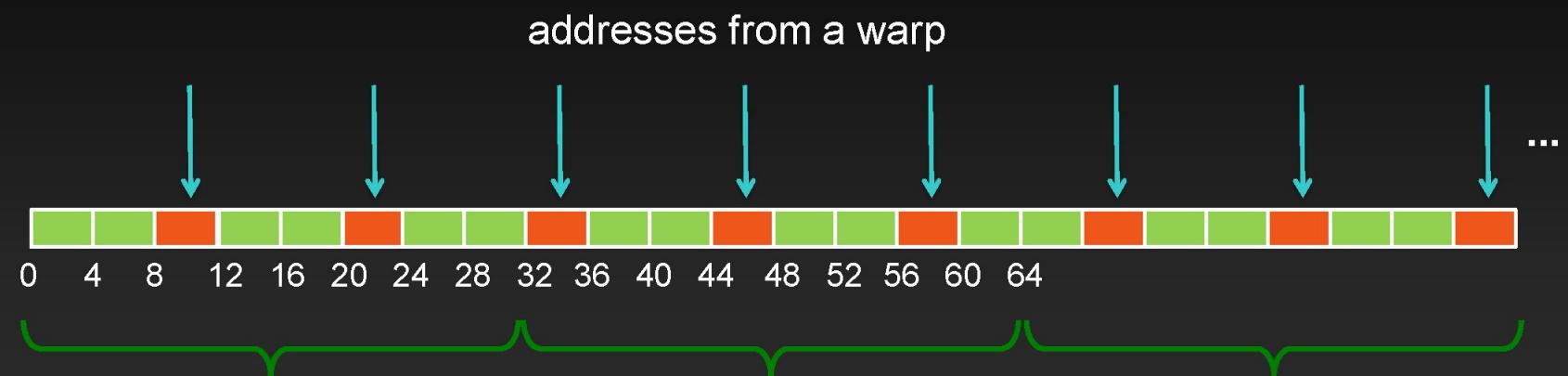
addresses from a warp



## Second Load Instruction



## Third Load Instruction



## Performance and Solutions

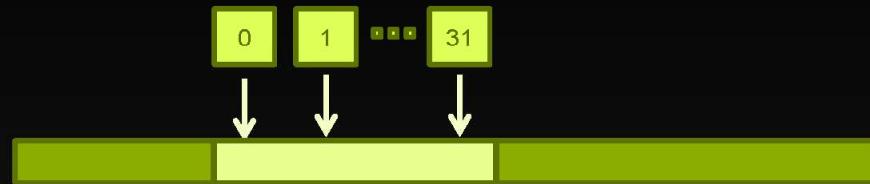
- Because of the address pattern, we end up moving 3x more bytes than application requests
  - We waste a lot of bandwidth, leaving performance on the table
- Potential solutions:
  - Change data layout from array of structures to structure of arrays
    - In this case: 3 separate arrays of floats
    - The most reliable approach (also ideal for both CPUs and GPUs)
  - Use loads via read-only cache
    - As long as lines survive in the cache, performance will be nearly optimal
  - Stage loads via shared memory

# Global Memory Access Patterns

- SoA vs AoS:

Good:  $\text{point.x}[i]$

Not so good:  $\text{point}[i].x$



- Strided array access:

~OK:  $x[i] = a[i+1] - a[i]$

Slower:  $x[i] = a[64*i] - a[i]$



- Random array access:

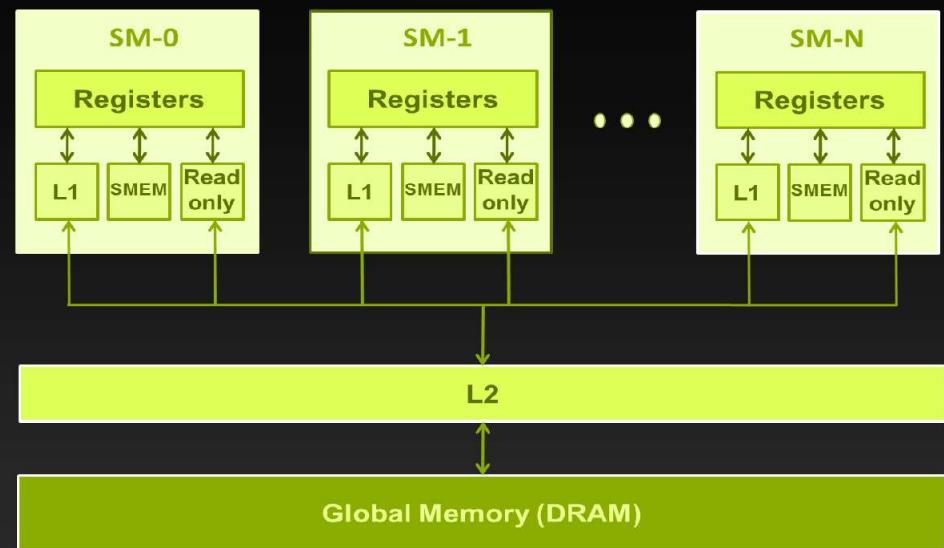
Slower:  $a[\text{rand}(i)]$

## **Summary: GMEM Optimization**

- **Strive for perfect address coalescing per warp**
  - Align starting address (may require padding)
  - A warp will ideally access within a contiguous region
  - Avoid scattered address patterns or patterns with large strides between threads
- **Analyze and optimize address patterns:**
  - Use profiling tools (included with CUDA toolkit download)
  - Compare the transactions per request to the ideal ratio
  - Choose appropriate data layout (prefer SoA)
  - If needed, try read-only loads, staging accesses via SMEM

## A note about caches

- L1 and L2 caches
  - Ignore in software design
  - Thousands of concurrent threads – cache blocking difficult at best
- Read-only Data Cache
  - Shared with texture pipeline
  - Useful for uncoalesced reads
  - Handled by compiler when `const __restrict__` is used, or use `_ldg()` primitive



## Read-only Data Cache

- Go through the read-only cache
  - Not coherent with writes
  - Thus, addresses must not be written by the same kernel
- Two ways to enable:
  - Decorating pointer arguments as hints to compiler:
    - Pointer of interest: `const __restrict__`
    - All other pointer arguments: `__restrict__`
      - Conveys to compiler that no aliasing will occur
  - Using `__ldg()` intrinsic
    - Requires no pointer decoration

# Read-only Data Cache

- Go through the read-only cache
  - Not coherent with writes
  - Thus, addresses must not be written by the same kernel
- Two ways to enable:
  - Decorating pointer arguments
    - Pointer of interest: `const`
    - All other pointer arguments
      - Conveys to compiler that they are not modified
  - Using `__ldg()` intrinsic
    - Requires no pointer decoration

```
__global__ void kernel(
    int* __restrict__ output,
    const int* __restrict__ input )
{
    ...
    output[idx] = input[idx];
}
```

# Read-only Data Cache

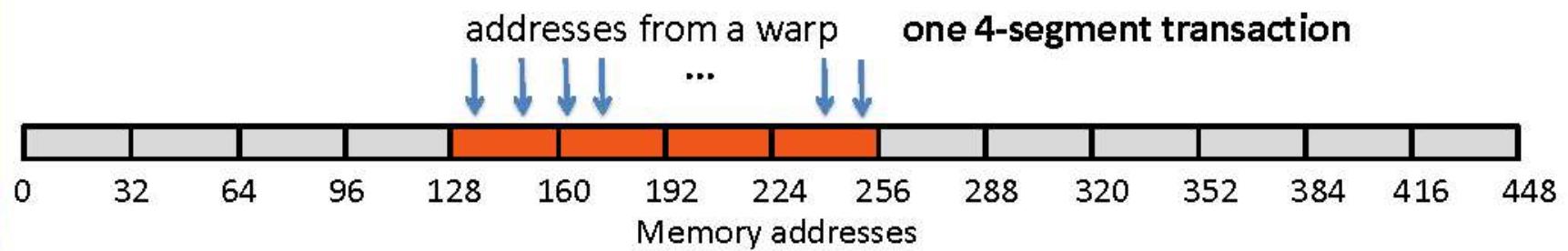
- Go through the read-only cache
  - Not coherent with writes
  - Thus, addresses must not be written by the same kernel
- Two ways to enable:
  - Decorating pointer arguments
    - Pointer of interest: `const`
    - All other pointer arguments
      - Conveys to compiler that they are not modified
  - Using `__ldg()` intrinsic
    - Requires no pointer decoration

```
__global__ void kernel( int *output,
                      int *input )
{
    ...
    output[idx] = __ldg( &input[idx] );
}
```

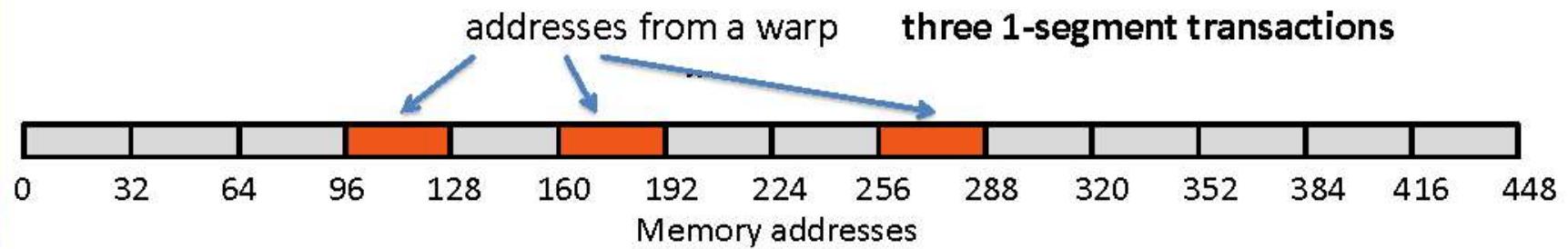
## Blocking for L1, Read-only, L2 Caches

- Short answer: DON'T
- GPU caches are not intended for the same use as CPU caches
  - Smaller size (especially per thread), so not aimed at temporal reuse
  - Intended to smooth out some access patterns, help with spilled registers, etc.
- Usually not worth trying to cache-block like you would on CPU
  - 100s to 1,000s of run-time scheduled threads competing for the cache
  - If it is possible to block for L1 then it's possible block for SMEM
    - Same size
    - Same or higher bandwidth
    - Guaranteed locality: hw will not evict behind your back

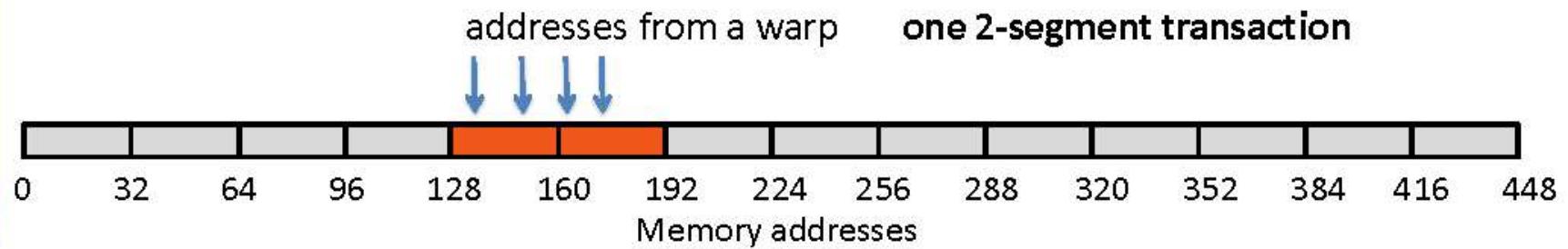
## Some Store Pattern Examples



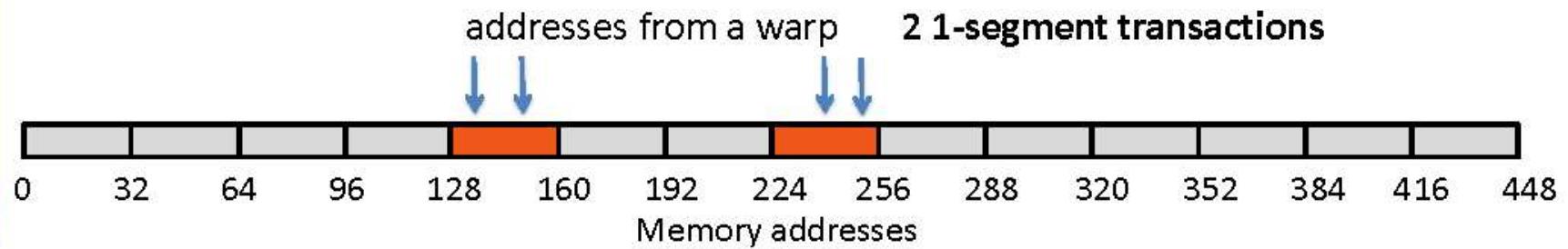
## Some Store Pattern Examples



## Some Store Pattern Examples



## Some Store Pattern Examples

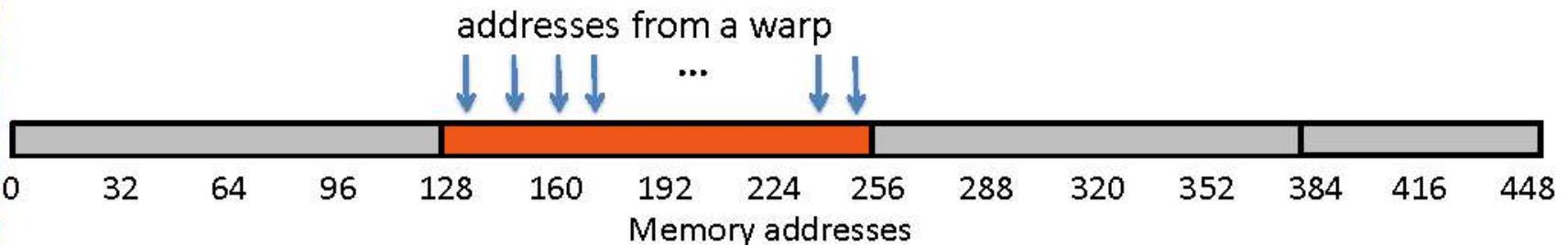


# GMEM Reads

- Attempt to hit in L1 depends on programmer choice and compute capability
- HW ability to hit in L1:
  - CC 1.x: no L1
  - CC 2.x: can hit in L1
  - CC 3.0, 3.5: cannot hit in L1
    - L1 is used to cache LMEM (register spills, etc.), buffer reads
- Read instruction types
  - Caching:
    - Compiler option: `-Xptxas -dlcm=ca`
    - On L1 miss go to L2, on L2 miss go to DRAM
    - Transaction: `128 B line`
  - Non-caching:
    - Compiler option: `-Xptxas -dlcm=cg`
    - Go directly to L2 (invalidate line in L1), on L2 miss go to DRAM
    - Transaction: `1, 2, 4 segments, segment = 32 B` (same as for writes)

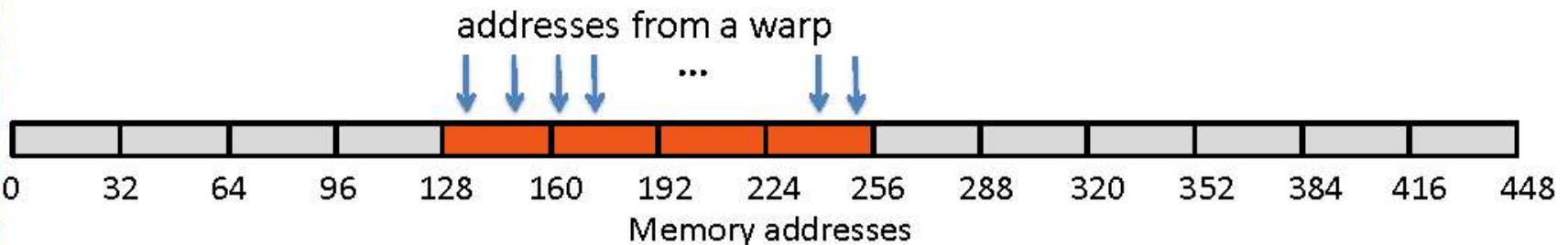
# Caching Load

- **Scenario:**
  - Warp requests 32 aligned, consecutive 4-byte words
- **Addresses fall within 1 cache-line**
  - No replays
  - Bus utilization: 100%
    - Warp needs 128 bytes
    - 128 bytes move across the bus on a miss



# Non-caching Load

- **Scenario:**
  - Warp requests 32 aligned, consecutive 4-byte words
- **Addresses fall within 4 segments**
  - No replays
  - Bus utilization: 100%
    - Warp needs 128 bytes
    - 128 bytes move across the bus on a miss



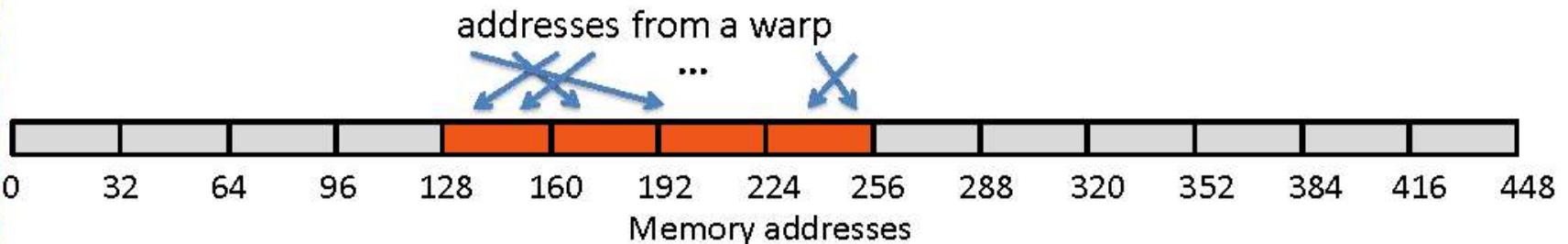
# Caching Load

- **Scenario:**
  - Warp requests 32 aligned, permuted 4-byte words
- **Addresses fall within 1 cache-line**
  - No replays
  - Bus utilization: 100%
    - Warp needs 128 bytes
    - 128 bytes move across the bus on a miss



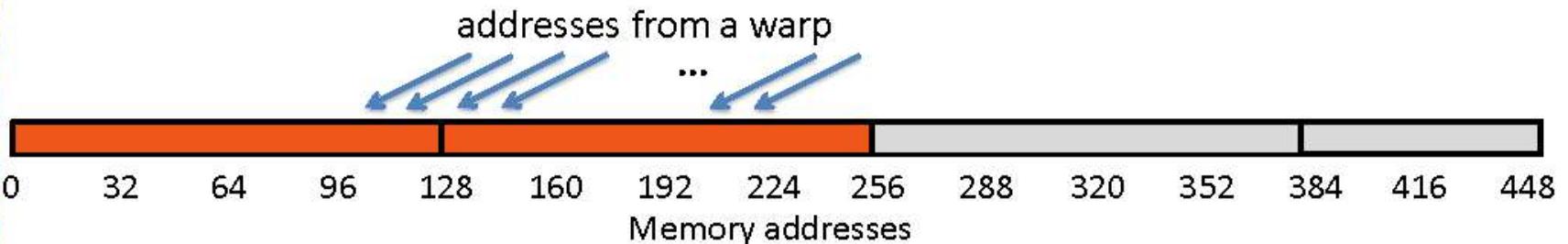
# Non-caching Load

- **Scenario:**
  - Warp requests 32 aligned, permuted 4-byte words
- **Addresses fall within 4 segments**
  - No replays
  - Bus utilization: 100%
    - Warp needs 128 bytes
    - 128 bytes move across the bus on a miss



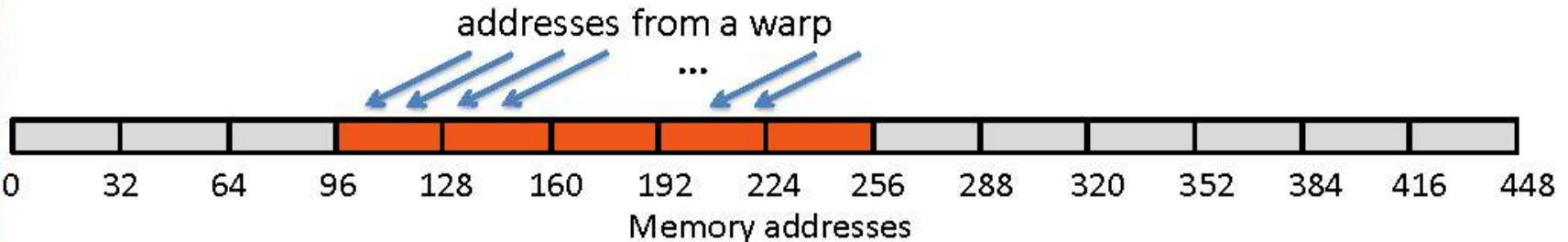
# Caching Load

- **Scenario:**
  - Warp requests 32 consecutive 4-byte words, offset from perfect alignment
- **Addresses fall within 2 cache-lines**
  - 1 replay (2 transactions)
  - Bus utilization: 50%
    - Warp needs 128 bytes
    - 256 bytes move across the bus on misses



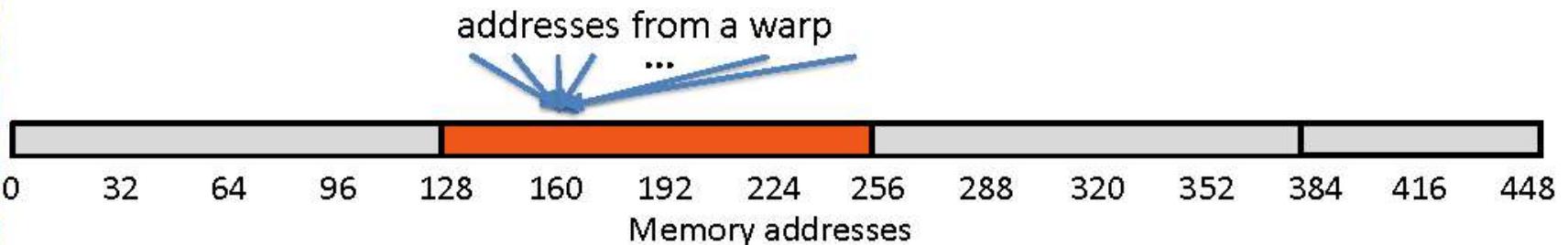
# Non-caching Load

- **Scenario:**
  - Warp requests 32 consecutive 4-byte words, offset from perfect alignment
- **Addresses fall within at most 5 segments**
  - 1 replay (2 transactions)
  - Bus utilization: at least 80%
    - Warp needs 128 bytes
    - At most 160 bytes move across the bus
    - Some misaligned patterns will fall within 4 segments, so 100% utilization



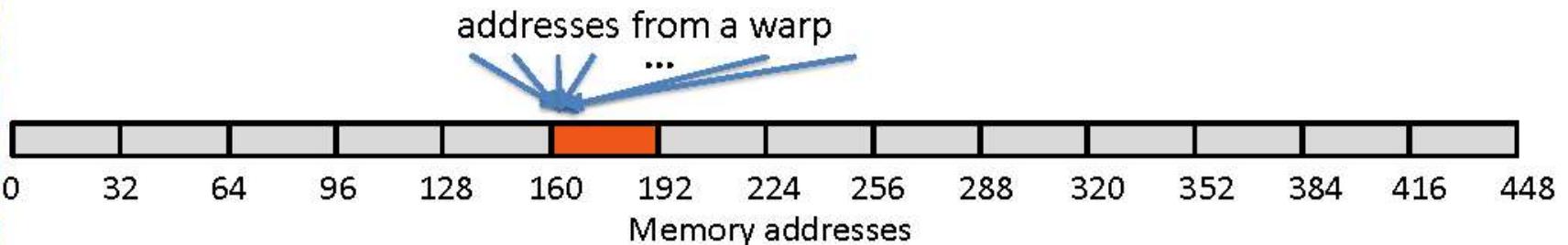
# Caching Load

- **Scenario:**
  - All threads in a warp request the same 4-byte word
- **Addresses fall within a single cache-line**
  - No replays
  - Bus utilization: 3.125%
    - Warp needs 4 bytes
    - 128 bytes move across the bus on a miss



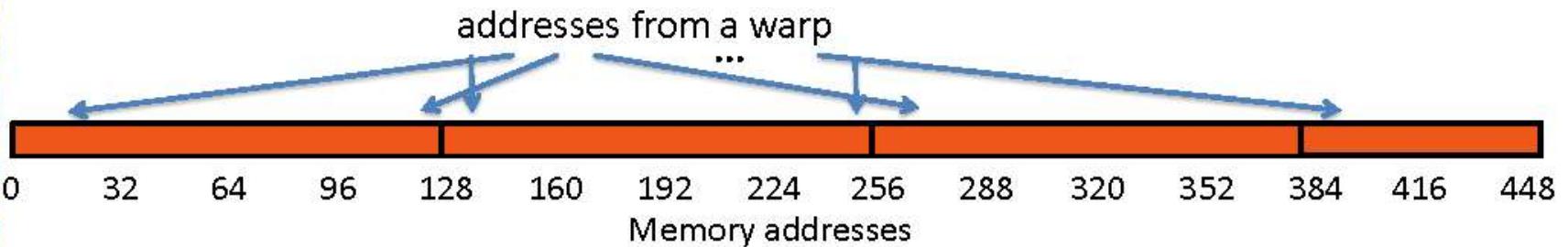
# Non-caching Load

- **Scenario:**
  - All threads in a warp request the same 4-byte word
- **Addresses fall within a single segment**
  - No replays
  - Bus utilization: 12.5%
    - Warp needs 4 bytes
    - 32 bytes move across the bus on a miss



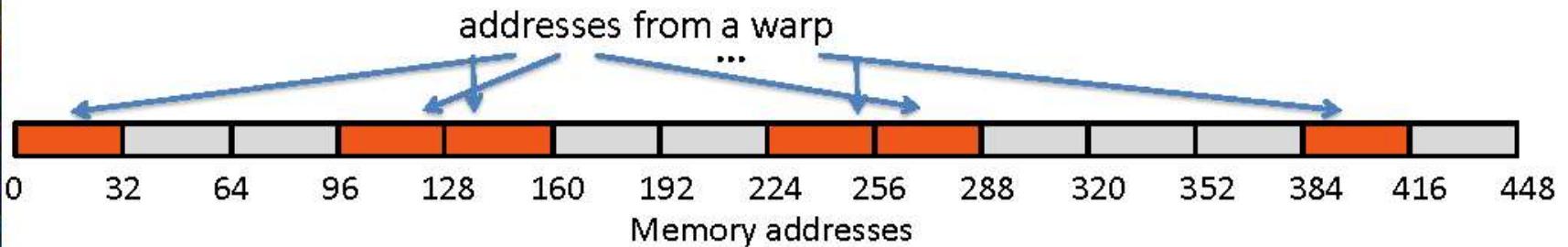
# Caching Load

- **Scenario:**
  - Warp requests 32 scattered 4-byte words
- **Addresses fall within  $N$  cache-lines**
  - $(N-1)$  replays ( $N$  transactions)
  - Bus utilization:  $32*4B / (N*128B)$ 
    - Warp needs 128 bytes
    - $N*128$  bytes move across the bus on a miss



# Non-caching Load

- **Scenario:**
  - Warp requests 32 scattered 4-byte words
- **Addresses fall within  $N$  segments**
  - $(N-1)$  replays ( $N$  transactions)
    - Could be lower some segments can be arranged into a single transaction
  - Bus utilization:  $128 / (N \cdot 32)$  (4x higher than caching loads)
    - Warp needs 128 bytes
    - $N \cdot 32$  bytes move across the bus on a miss





# Caching vs Non-caching Loads

- **Compute capabilities that can hit in L1 (CC 2.x)**
  - Caching loads are better if you count on hits
  - Non-caching loads are better if:
    - Warp address pattern is scattered
    - When kernel uses lots of LMEM (register spilling)
- **Compute capabilities that cannot hit in L1 (CC 1.x, 3.0, 3.5)**
  - Does not matter, all loads behave like non-caching
- **In general, don't rely on GPU caches like you would on CPUs:**
  - 100s of threads sharing the same L1
  - 1000s of threads sharing the same L2

# L1 Sizing

- Fermi and Kepler GPUs split 64 KB RAM between L1 and SMEM
  - Fermi GPUs (CC 2.x): 16:48, 48:16
  - Kepler GPUs (CC 3.x): 16:48, 48:16, 32:32
- Programmer can choose the split:
  - Default: 16 KB L1, 48 KB SMEM
  - Run-time API functions:
    - `cudaDeviceSetCacheConfig()`, `cudaFuncSetCacheConfig()`
  - Kernels that require different L1:SMEM sizing cannot run concurrently
- Making the choice:
  - Large L1 can help when using lots of LMEM (spilling registers)
  - Large SMEM can help if occupancy is limited by shared memory



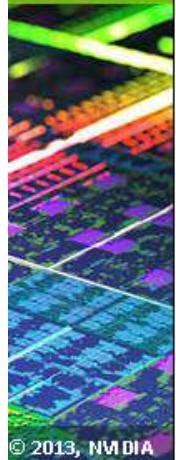
# Read-Only Cache

- **An alternative to L1 when accessing DRAM**
  - Also known as *texture* cache: all texture accesses use this cache
  - CC 3.5 and higher also enable global memory accesses
    - Should not be used if a kernel reads and writes to the same addresses
- **Comparing to L1:**
  - Generally better for scattered reads than L1
    - Caching is at 32 B granularity (L1, when caching operates at 128 B granularity)
    - Does not require replay for multiple transactions (L1 does)
  - Higher latency than L1 reads, also tends to increase register use
- **Aggregate 48 KB per SM: 4 12-KB caches**
  - One 12-KB cache per scheduler
    - Warps assigned to a scheduler refer to only that cache
  - Caches are not coherent – data replication is possible

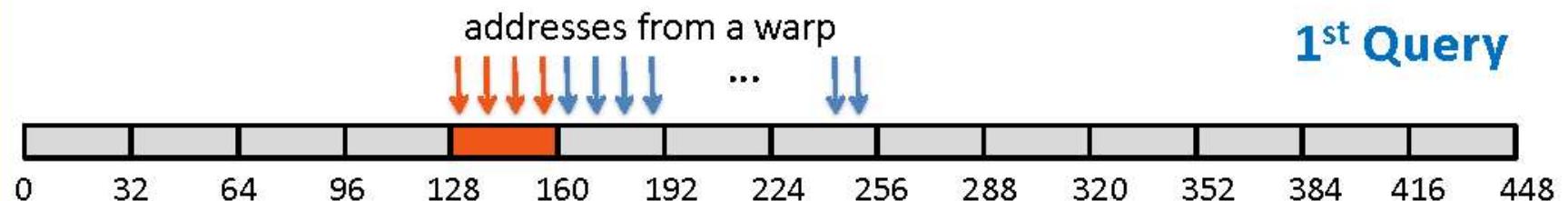


## Read-Only Cache Operation

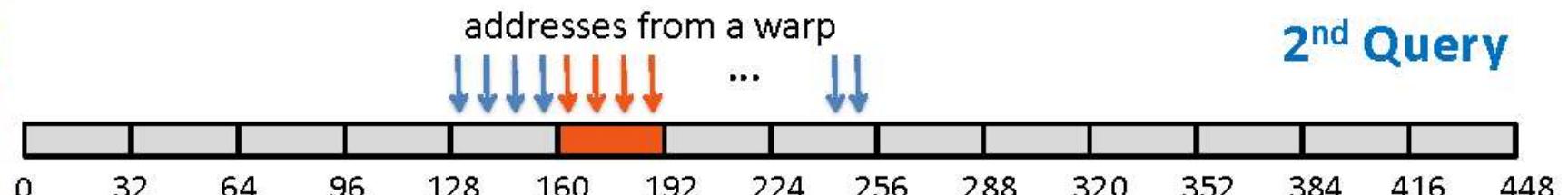
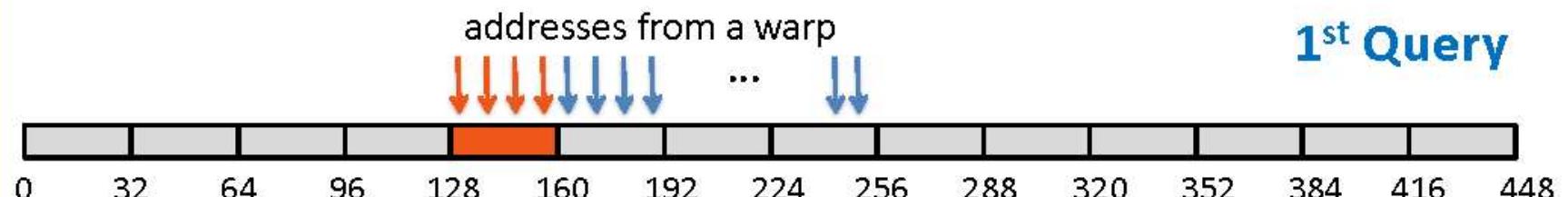
- Always attempts to hit
- Transaction size: 32 B queries
- Warp addresses are converted to queries 4 threads at a time
  - Thus a minimum of 8 queries per warp
  - If data within a 32-B segment is needed by multiple threads in a warp, segment misses at most once
- Additional functionality for texture objects
  - Interpolation, clamping, type conversion

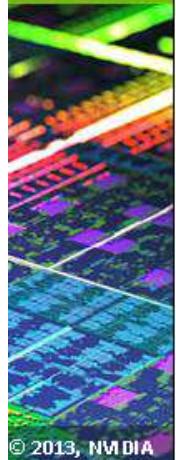


# Read-Only Cache Operation

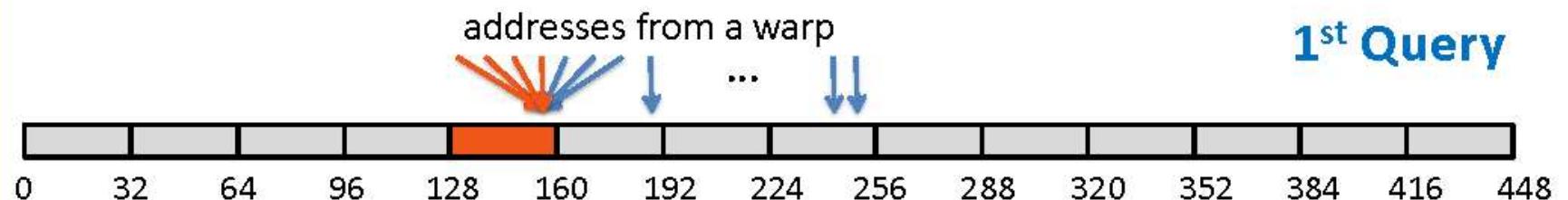


# Read-Only Cache Operation

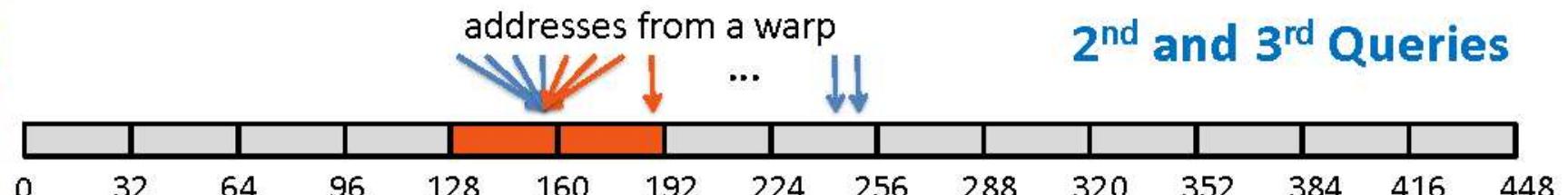
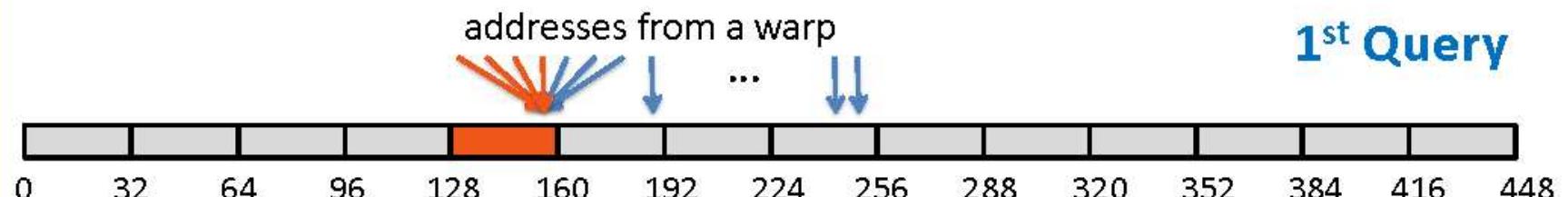




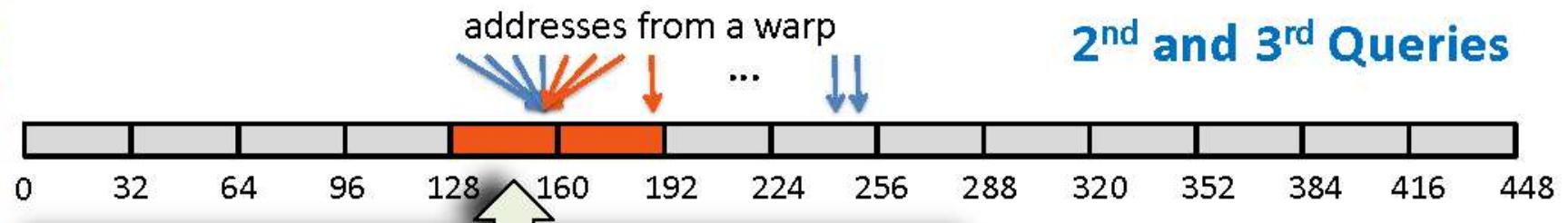
# Read-Only Cache Operation



# Read-Only Cache Operation



# Read-Only Cache Operation



Note this segment was already requested in the 1<sup>st</sup> query:  
cache hit, no redundant requests to L2



# PTX State Spaces (1)

Memory type/access etc. organized using notion of *state spaces*

Table 6 State Spaces

Name	Description
.reg	Registers, fast.
.sreg	Special registers. Read-only; pre-defined; platform-specific.
.const	Shared, read-only memory.
.global	Global memory, shared by all threads.
.local	Local memory, private to each thread.
.param	Kernel parameters, defined per-grid; or Function or local parameters, defined per-thread.
.shared	Addressable memory shared between threads in 1 CTA.
.tex	Global texture memory (deprecated).



# PTX State Spaces (2)

Table 7 Properties of State Spaces

Name	Addressable	Initializable	Access	Sharing
.reg	No	No	R/W	per-thread
.sreg	No	No	RO	per-CTA
.const	Yes	Yes <sup>1</sup>	RO	per-grid
.global	Yes	Yes <sup>1</sup>	R/W	Context
.local	Yes	No	R/W	per-thread
.param (as input to kernel)	Yes <sup>2</sup>	No	RO	per-grid
.param (used in functions)	Restricted <sup>3</sup>	No	R/W	per-thread
.shared	Yes	No	R/W	per-CTA
.tex	No <sup>4</sup>	Yes, via driver	RO	Context

**Notes:**

<sup>1</sup> Variables in .const and .global state spaces are initialized to zero by default.

<sup>2</sup> Accessible only via the `ld.param` instruction. Address may be taken via `mov` instruction.

<sup>3</sup> Accessible via `ld.param` and `st.param` instructions. Device function input and return parameters may have their address taken via `mov`; the parameter is then located on the stack frame and its address is in the .local state space.

<sup>4</sup> Accessible only via the `tex` instruction.



# PTX Cache Operators

Table 27 Cache Operators for Memory Load Instructions

Operator	Meaning
.ca	Cache at all levels, likely to be accessed again. The default load instruction cache operation is <code>ld.ca</code> , which allocates cache lines in all levels (L1 and L2) with normal eviction policy. Global data is coherent at the L2 level, but multiple L1 caches are not coherent for global data. If one thread stores to global memory via one L1 cache, and a second thread loads that address via a second L1 cache with <code>ld.ca</code> , the second thread may get stale L1 cache data, rather than the data stored by the first thread. The driver must invalidate global L1 cache lines between dependent grids of parallel threads. Stores by the first grid program are then correctly fetched by the second grid program issuing default <code>ld.ca</code> loads cached in L1.
.cg	Cache at global level (cache in L2 and below, not L1). Use <code>ld.cg</code> to cache loads only globally, bypassing the L1 cache, and cache only in the L2 cache.
.cs	Cache streaming, likely to be accessed once. The <code>ld.cs</code> load cached streaming operation allocates global lines with evict-first policy in L1 and L2 to limit cache pollution by temporary streaming data that may be accessed once or twice. When <code>ld.cs</code> is applied to a Local window address, it performs the <code>ld.lu</code> operation.
.lu	Last use. The compiler/programmer may use <code>ld.lu</code> when restoring spilled registers and popping function stack frames to avoid needless write-backs of lines that will not be used again. The <code>ld.lu</code> instruction performs a load cached streaming operation ( <code>ld.cs</code> ) on global addresses.
.cv	Don't cache and fetch again (consider cached system memory lines stale, fetch again). The <code>ld.cv</code> load operation applied to a global System Memory address invalidates (discards) a matching L2 line and re-fetches the line on each new load.



# SASS LD/ST Instructions

Architecture-dep.

Kepler:

Compute Load/Store Instructions	
LDC	Load from Constant
LD	Load from Memory
LDG	Non-coherent Global Memory Load
LDL	Load from Local Memory
LDS	Load from Shared Memory
LDSLK	Load from Shared Memory and Lock
ST	Store to Memory
STL	Store to Local Memory
STS	Store to Shared Memory
STSCUL	Store to Shared Memory Conditionally and Unlock
ATOM	Atomic Memory Operation
RED	Atomic Memory Reduction Operation
CCTL	Cache Control
CCTLL	Cache Control (Local)
MEMBAR	Memory Barrier

(see also LDG.CI etc.)

Thank you.

- NVIDIA