# Zedoled Controller

## Summary

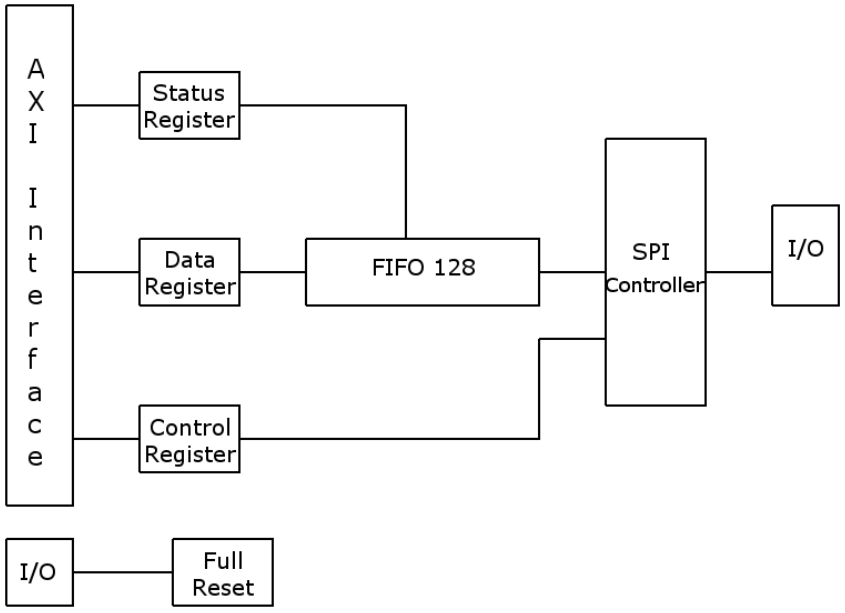


## Introduction

The Zedoled Controller enables to control the OLED display on Zedboard.

## Functional description

The Zedoled Controller includes a 128-byte FIFO for data and commands. Data is written into FIFO through the Data Register. FIFO status can be read through the Status Register. The Control Register enables to control VBAT and VDD voltage during initialization. It enables also to reset the FIFO, SPI Controller and OLED display with bit [1]. D/C line is selected using the Control Register.



# Programming guide

## Initialization

Oled display can be initialized as follow:
Initial state: Vdd and Vbat off (bits high), Res off (bit high), D/C* low

1. Set Vdd on
2. Send "Display Off" command 0xAE
3. Set Res high (reset the controller and display)
4. Set Res low
5. Charge Pump. Send following commands: 0x8D, 0x14, 0xD9, 0xF1
6. Set Vbat on and wait 10ms
7. Send contrast commands: 0x81, 0x0F
8. Send display config commands: 0xD3, 0x20; 0xDA, 0x22; 0x20, 0x00; 0x21, 0x00, 0x7F; 0x22, 0x00, 0x07
9. Send display on command: 0xAF

Then change D/C* line to Data (set bit high) and fill the Fifo to display pixels on the screen.

*Note: Fifo should be empty when changing D/C* bit in the Controller Register.*

*Note: Using the initialization sequence above, the display is in Horizontal Addressing Mode. Refer to SSD1306 reference manual for more details.*

# I/O Interfaces

The input can be connected to a push button to reset the entire Controller and the display. This reset-input is active high.
Constraint file should connect input/outputs as follow:

```
Net "…_ZEDOLED_SDIN_pin" LOC = AA12 | IOSTANDARD = LVCMOS33;
Net "…_ZEDOLED_SCLK_pin" LOC = AB12 | IOSTANDARD = LVCMOS33;
Net "…_ZEDOLED_DC_pin"   LOC = U10  | IOSTANDARD = LVCMOS33;
Net "…_ZEDOLED_RES_pin"  LOC = U9   | IOSTANDARD = LVCMOS33;
Net "…_ZEDOLED_VBAT_pin" LOC = U11  | IOSTANDARD = LVCMOS33;
Net "…_ZEDOLED_VDD_pin"  LOC = U12  | IOSTANDARD = LVCMOS33;
Net "…_ZEDOLED_RST_pin"  LOC = P16  | IOSTANDARD = LVCMOS33;
```

# Registers

Module name: Zedoled Controller
Base Address: refer to implementation info

| Register name | Address | Description |
|---|---|---|
| CONTROL | 0x00 | This register defines basic controls |
| DATA | 0x04 | Write data into FIFO |
| STATUS | 0x08 | FIFO Status |

## CONTROL Register

| Field name | Bits | Description |
|---|---|---|
| reserved | 31:4 | reserved |
| VDD | 3 | VDD, active low |

| | | |
|---|---|---|
| VBAT | 2 | VBAT, active low |
| RES | 1 | Reset, active low |
| D/C* | 0 | Select Data or Command:<br>1: Data<br>0: Command |

## DATA Register

| Field name | Bits | Description |
|---|---|---|
| reserved | 31:8 | reserved |
| DATA | 7:0 | Data to be written to FIFO.<br>Can be Data or Command. |

## STATUS Register

| Field name | Bits | Description |
|---|---|---|
| reserved | 31:2 | reserved |
| FULL | 1 | Fifo Full flag.<br>1: Fifo full<br>0: Fifo not full |
| Empty | 0 | Fifo empty flag.<br>1: Fifo empty<br>0: Fifo not empty |