C-DAC Four Days Technology Workshop

ON

Hybrid Computing – Coprocessors/Accelerators
Power-Aware Computing – Performance of Applications Kernels

hyPACK-2013
(Mode-1:Multi-Core

Lecture Topic:

Multi-Core Processors : Tuning & Performance –

Cluster of Multi-Core Processors

Venue : CMSD, UoHYD ; Date : October 15-18, 2013

An Overview of Multi-Core Processors

Lecture Outline

Following Topics will be discussed

- Tuning & Performance – Cluster of Multi-Core Processors
- Compiler Issues; Inter-connection Issues
- Cost of Message Passing
- Use of Performance Tools

Gains from tuning categories

Tuning Category	Typical Range of Gain
Source range	25-100%
Compiler Flags	5-20%
Use of libraries	25-200%
Assembly coding / tweaking	5-20%
Manual prefetching	5-30%
TLB thrashing/cache	20-100%
Using vis.inlines/micro-vectorization	100-200%

Source : Reference [4],[6], [7], [8], [32], 34]

Loop Optimization Techniques

- Dependence Analysis
- Transformation Techniques
- Loop distribution
- Loop Alignment
- Node Splitting
- Strip Mining
- Loop Collapsing
- Loop Fission Loop Fusion
- Wave front method
- Loop Optimizations

More about Loop Optimizations

- Basic Loop Unrolling & Qualifying Candidates for Loop Unrolling
- Negatives of Loop Unrolling
- Outer and Inner Loop Unrolling
- Associative Transformations
- Loop Interchange

Source : Reference [4],[6], [7], [8], [32], 34]

Compiler Options for Performance

- Improve usage of data cache, TLB
- Use VIS instructions (templates) directly, via –xvis option
- Optimize data alignment Prevent Register Window overflow
- Creating inline assembly templates for performance critical routines
- Loop Optimizations that compilers may miss:
  - Restructuring for pipelining and prefetching
  - Loop splitting/fission
  - Loop Peeling
  - Loop interchange
  - Loop unrolling and tiling
  - Pragma directed

Source : Reference [4],[6], [7], [8], [32], 34]

Compiler Options for Performance

Compiler optimization options:

- -xO1 thru -xO5 (default is “none”, -O implies -xO3)
- -fast:easy to use, best performance on most code,but it assumes compile platform = run platform and makes Floating point arithmetic simplifications.
- Understand program behavior and assert to optimizer:
  - -xrestrict, if only restricted pointers are passed to functions
  - -xalias_level, if pointers behave in certain ways
  - -fsimple if FP arithmetic can be simplified
- Target machine-related:
  - -xprefetch, -xprefetch_level
  - -xtarget=, -xarch=, -xcache=, -xchip=
  - -xvector to convert DO loops into vector

Compiler Options for Performance

Compiler Optimization Switches

- Fortran and C compilers have different levels of optimization that can do a fairly good job at improving a program's performance. The level is specified at compilation time with –O switch.
  - A same level of optimization on different machines will not always produce the same improvements (don't be surprised!)
  - –O is either default level of optimization. Safe level of optimization.
  - – O2 (same as –O on some machines) simple inline optimizations
  - – O3 (and –O4 on some machines) more complex optimizations designed to pipeline code, but may alter semantics of program
  - – fast Selects the optimum combination of compilation options for speed.
  - – parallel Parallelizes loops.
- Quite often, just a few simple changes to one's code improves performance by a factor of 2,3, or better!

Algorithm Overheads

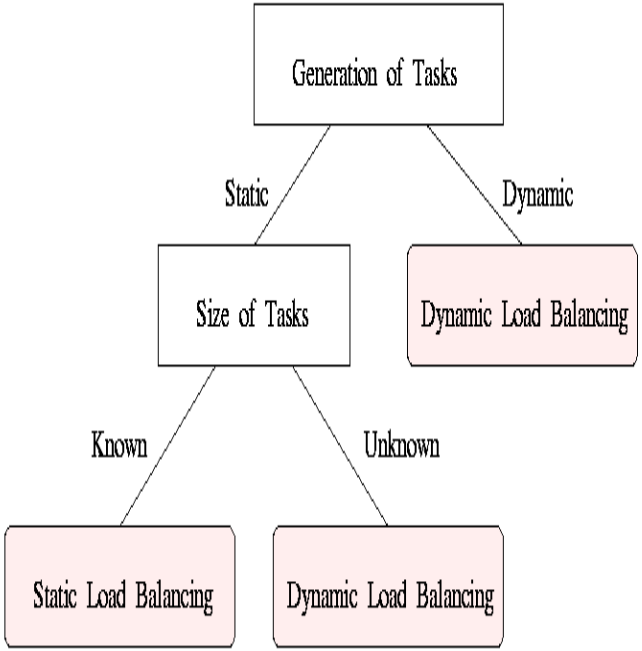
- Data parallelism;
- Task parallelism;
- Combination of Data and Task parallelism
- Static and Load Balancing
  - Mapping for load balancing
  - Minimizing Interaction
  - Overheads in parallel algorithms design
- Data Sharing Overheads

Decomposition techniques

- Recursive decomposition
- Data decomposition
- Exploratory decomposition
- Hybrid decomposition

Source : Reference :[1], [4]

Load Balancing Techniques



- **Static load-balancing**
  - Distribute the work among processors prior to the execution of the algorithm
  - Matrix-Matrix Computation
  - Easy to design and implement
- **Dynamic load-balancing**
  - Distribute the work among processors during the execution of the algorithm
  - Algorithms that require dynamic load-balancing are somewhat more complicated (Parallel Graph Partitioning)

System Configuration

- System configuration (OS, Compilers, Profilers)
- Interconnection Net-work – Point-point, One-all & All-to-All communications (Buffer Mechanism)
- Disk I/O Computations (Tuning II/O Controller)
  - Hardware; Processor Choice; Interconnect Choice
  - Network Card Choice (in some cases); IO Subsystem
  - Software; Compiler Choice; Compiler Options
  - MPI Choice; MPI Tuning; NIC Driver Tuning
  - Switch Tuning; OS Choice
- Sequential code Optimization (Compiler – Code Restructuring, Loop Optimization, Memory Allocators)

Tuning & Performance on Multi-Core Processors

Simple Approach

- Use Compiler Switches & explore performance – Localize the Data – Cache Utilization
- Use Profiler to understand behavior of programme
- Use Linux tool “top” to know about the CPU 7& Memory Utilization as well as Scalability with respect to varying size
- Threading APIs used; Locks & Heap contention
- Thread affinity – Explore the performance
- Sequential code Optimization – Use tuned libraries
- Check for Swapping (is the code Swapping ?) – Use “top” tools

Comparing compiler at various levels of Optimization

- Compiler vendors, sometimes include aggressive optimization at a lower level (For example -O2 may include some optimizations that other compiler vendors put in at -O3)
- Difficult to compare the same optimization levels among Compilers

CPU /Compiler	-O2	-O3	Aggressive	Tuning
AMD/PGI				
AMD PathScale				
Intel /PGI				
Intel Software				

- AbSoft
- Gcc

- Increasing the level of optimization doesn't improve the performance of the code.

Multi-Core Sub-system – Details

- CPU Utilization;
- Memory Usage;
- Network traffic,
- Disk Usage,
- Process Information

Multi-Core Sub-system – Details

Intel Compiler Optimization Switches

- Intel High-Level Optimizations (HLO)
- Intel Multiphase Optimizations
  - (IPO – Interprocedural Optmizations)
  - PGO –(Profile Guided Optimization) Switches
- Intel Math Kernel Library (MKL)
- Intel Integrated Performance Primitives

General Optimizations

Linux	Windows	-
-O0	/Od	Disables optimization
-g	/Z1	Creates symbols
-O1	/O1	Optimize binary Code for Server Size
-O2	/O2	Optimize for Speed (default)
-O3	/O3	Optimize for Data Cache : Loop floating point code
-axP	QaxP	Optimize for Intel Processors with SSE 3 Capabilities.
-parallel	-Qparallel	Auto-paalleization

Multi-Core Computing Systems

- Intel
- Cray
- IBM - Cell
- AMD
- SGI
- SUN
- HP

Multi-Core Sub-system – Details

- CPU Utilization; Memory Usage; Network traffic, Disk Usage, Process Information
- Intel Compiler Optimization Switches
- Intel High-Level Optimizations (HLO)
- Intel Multiphase Optimizations (IPC, PGO)
- Intel Multiphase Optimizations (PGO – Profile Guided Optimization Switches)
- Intel Math Kernel Library (MKL)
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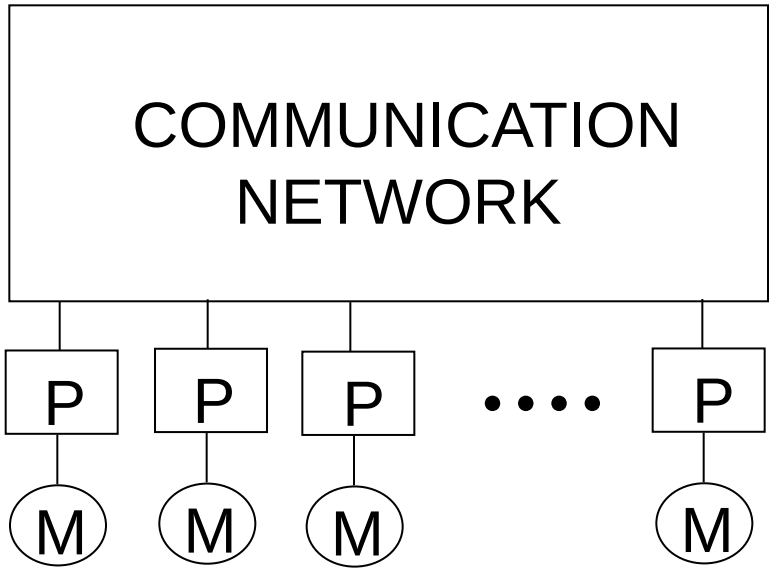
Message Passing Architecture Model

Message-Passing Programming Paradigm : Processors are connected using a message passing interconnection network.



- On most Parallel Systems, the processes involved in the execution of a parallel program are identified by a sequence of non-negative integers. If there are *p* processes executing a program, they will have ranks 0, 1,2, ……., *p-1.*

Interconnection Networks – Latency Bandwidth

- **TCP**
  - GiGE,
  - GigE with Jumbo Frames,
  - GAMMA, Level 5 GigE
  - 10 Gigabit Ethernet
  - 100 gigabit Ethernet
- **Myrinet**
- **Infiniband**
- **PathScale (Infinipath)**
- **Quadrics**
- **Dolphin**

- I/O time for Codes (CFD /Seismic Codes)

MPI Libraries (Open Source)

- Open-source
- **MPICH1 (Standard)**
- **MPICH2 (Standard)**
- LAM
- Open-MPI **(*)**
- GAMMA-MPI
- FT-MPI
- LA-MPI
- LA-MPI
- PACX-MPI
- MVAPICH
- OOMPI
- MPICH-GM
- MVICH
- MP_Lite

(*) OpenMPI combines the best features of LAM, FT-MPI, LA-MPI, and PACX-MPI. It supports TCP, Myrinet, Infiniband networks. http://icl.cs.utk.edu/open-mpi/

- OpenMPI has addition of the fault tolerance capability of FT-MPI.
- This will allow an MPI code to lose a node and then add a new node to finish the computations without lose of data.

Tuning & Performance on Multi-Core Processor Clusters

Test the following MPI Libraries (Open Source)

- Open-source
- **MPICH1 (Standard)**
- **MPICH2 (Standard)**
- LAM
- MPICH-GM (forMyrinet)
- MVAPICH (for Infiniband)
- Atleast one commercial MPI

- Choice of Compilers -Computing systems – Price / Performance
- Choice of MPI libraries Computing Systems – Price / Performance

Interconnection Networks – Latency Bandwidth

- **TCP**
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Tuning & Performance on Multi-Core Processor Clusters

- **MPI Library calls & MPI algorithms implementation**
  - MPI Point-to-Point communication Calls;
  - MPI collective Communications,
  - MPI Communication & Computation Library Calls
  - MPI-2 library Calls
  - MPI I/O library Calls
- **Communication overheads for all MPI library calls**
- MPI 3.0 Thread enabled MPI

MPI Point-to-Point Communication: Communication Modes

MPI Primitive	Blocking	Nonblocking
Standard Send	MPI_Send	MPI_Isend
Synchronous Send	MPI_Ssend	MPI_Issend
Buffered Send	MPI_Bsend	MPI_Ibsend
Ready Send	MPI_Rsend	MPI_Irsend
Receive	MPI_Recv	MPI_Irecv
Completion Check	MPI_Wait	MPI_Test

Different Send/Receive operations in MPI

MPI Collective Communications

Type	Routine	Functionality
Data Movement	MPI_Bcast	One-to-all, Identical Message
	MPI_Gather	All-to-One, Personalized messages
	MPI_Gatherv	A generalization of MPI_Gather
	MPI_Allgather	A generalization of MPI_Gather
	MPI_Allgatherv	A generalization of MPI_Allgather
	MPI_Scatter	One-to-all Personalized messages
	MPI_Scatterv	A generalization of MPI_Scatter
	MPI_Alltoall	All-to-All, personalized message
	MPI_Scatterv	A generalization of MPI_Alltoall

Tuning & Performance on Multi-Core Processor Clusters

- Commercial Code tuning
  - File System
  - Network (TCP Buffers NIC, Switches)
  - L1 Cache /L2 Cache on Multi-Core Processors
  - Compiler Switches
  - MPI Libraries
  - OS & Memory Usage (80 %)

- Scalability of computing Systems & Performance Issues are Challenging

Thread Safety & MPI – Issues to be addressed

- Performance tradefoffs between multi-threaded and single-threaded code.
  - I/O operations
  - Against Inconsistent updates to the same memory location from different threads
  - Software locks and System locks are quite expensive
- Vendors sometimes provide single threaded /Multi-threaded libraries
  - Have I been linked with the right library ?
  - DO I suffer with occasional and mysterious errors

Source : Reference : [4], [6], [11],[12],[24],[25], [26]

Using PAPI : Events

- Events are occurrences of specific signals related to a processor's function.

  Ex: cache misses, number of floating point operations

- Preset events are mappings from symbolic names to machine specific definitions for a particular hardware resource.
  - Ex: **PAPI_TOT_CYC** (I.e Total Cycles), **PAPI_FLOPS**

- Native events comprise the set of all events that are countable by the CPU.

Using PAPI : PAPI library Interface

- PAPI provides two APIs to access the underlying counter hardware:
  - The low level interface manages hardware events in user defined groups called EventSets. (PAPI low level)
  - The high level interface simply provides the ability to start, stop and read the counters for a specified list of events. (PAPI high level)

An Overview of Multi-Core Processors

Conclusions

- An Overview of Tuning & Performance of Software threading on Multi-Core Software is discussed.

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Thank You

Any questions ?