



全志科技
Allwinner Technology

V3s

Hardware Design Guide

ALLWINNER TECH
CONFIDENTIAL

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CPU

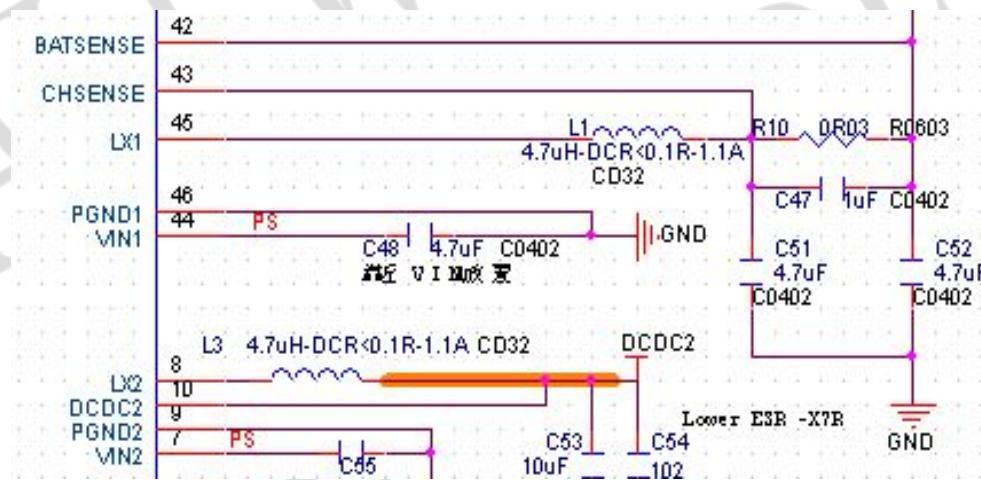
- 1. UART2: please keep the test points.
- 2. GPIO distribution: please follow the standard chart, do not arbitrarily adjust. If necessary, please contact the FAE.

DRAM

- › 1. V3s support 32M * 16bit DDR2, the supply voltage is **1.8V**.
- › 2. Master ZQ PIN is a 240R-1% accuracy pull-down resistor tied to the ground, placed close to the ground.

POWER

- › 1. For 4.7uH inductor, pay attention to saturation current to meet the maximum current demand, DC resistance must be < 100 milliohms.
- › 2. Select the LDO3IN input voltage according to the LDO3 output voltage.
- › 3. R10 resistance need to be adjusted according to the actual charge current size specifications, such as if R10 is modified from 30mR to 100mR, charging current is 3/10.



CAMERA

- 1. Camera AVDD/DVDD/IOVDD: the 3 supply voltages must conform to the sensor specification range.
- 2. The three channels of VCC-PE, MIPI-IOVCC, and VCC-LCD must share the same power supply.
- 3. A 33R resistor must be added to the MCLK and the NC capacitor to ground is used to increase the camera compatibility and reduce EMI emissions from the clock signal.
- 4. Check the pin definition of the camera module to see if it matches the socket. Special attention should be paid to the selection of the upper or lower contact of the general 24 pin socket. Check the direction of the contact surface of the gold finger on the module.
- 5. Camera's I2C control needs to use the CSI's own TWI, do not use the system's TWI

LCD

- 1. The serial 8-bit RGB screen wires and interface cannot be changed.
- 2. The RGB666 screen R/G/B interface can be interchanged in the entire group.
- 3. The CS signal is pulled down or up according to the screen data and is not connected to the master.

SPI NAND/NOR

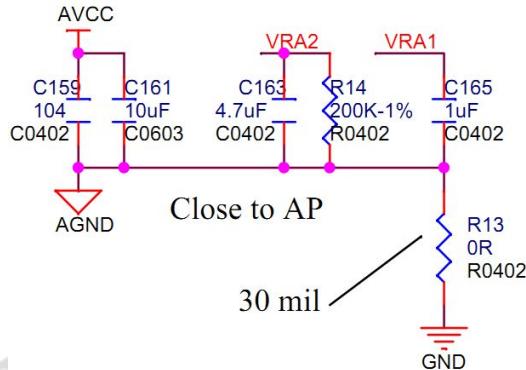
- V3 supports SPI NAND/NOR FLASH

CARD

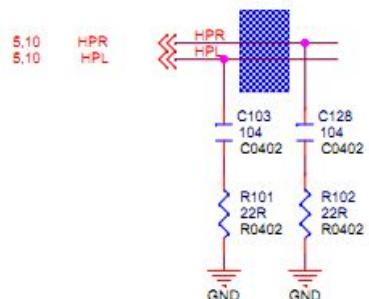
- › 1. Do not use a pull up resistor on the CLOCK pin. If a shunt capacitor is used, its capacitance must not exceed 15pF.
- › 2. A 33 ohm resistor is required on the CLOCK signal line and placed close to the CPU.

AUDIO

- 1. The ground points of VRP, VRA, and AGND are connected to a single point and connected to ground through a 0R resistor. The resistance and capacitance values cannot be modified.
- 2. The HPR/HPL features an RC-to-ground circuit between the amplifier and the preamp input.



- 3. The amplification ratio of Class AB amplifiers and Class D amplifiers is inconsistent, and the maximum volume can be adjusted by software. The value of pa_single_vol is modified in systemconfig.



USB

- 1. The ID pin on the USB connector is used for external device detection. It is connected to PG4 and pulled up to the VCC-3V3 voltage through a resistor. If the ID detection is low, it is USB Device mode; if the ID detection is high, it is USB Host mode.
- 2. USBVBUS input voltage is PS, POWER SWITCH switch plus pull-down resistor, which is turned off by default. It will only be turned on when it is powered by external device as HOST.
- 3. If reversing detection function is needed, the camera can be pulled back to increase the reversing judgment: after pulling the ISP, the reversing signal is received, and after the processor reads, the value of the ISP register is pulled to determine reversing.

KEY

- 1. Key number selection, according to need, directly remove the back button.
- 2. Buttons uses the remote control keys. The sampling range of the LRADC0/LRADC1 network is 0-2V. When a key is pressed, make sure that the LRADC0 network voltage range is 0-1.6V, and the LRADC0 voltage difference must be $\geq 0.15V$ when any two buttons are pressed.

ESD

- 1. For key devices such as CPU / Crystal ESD sensitive devices, it is recommended to use a metal shield.
- 2. The reset signal must be close to the AP, and a filter capacitor to GND must be mounted. The fixed value is 10nF.
- 3. Circuits that are directly connected to the outside or exposed, such as USB connectors, MICs, CARD holder, etc. must be equipped with ESD devices.

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Stack Up

- 1. Four-layer board, laminated structure and impedance control are recommended as follows (If you need to adjust the board thickness, please adjust the thickness of the medium between the layers 2 and 3, keep the other medium thickness unchanged)

| --- | | Stackup Structure | | Impedance Requirements | | | | | | | |
|------------------|-------------|-------------------|---------------|------------------------|-----------------------|-----------------|-------------------|--------------|--|--|--|
| Layer | Type | Thickness (mil) | | Dk(with Sim Z0) | Impedance spec (Ohms) | Reference layer | Width/space (mil) | Sim Z0(Ohms) | | | |
| 1 | solder mask | 0.5 | SM | 4.25 | 50±10% | 2 | 4 | 52.18 | | | |
| | TOP | 1.6 | 0.3oz+plating | | 90±10% | 2 | 4.5/7.5 | 90.03 | | | |
| | | | | | 100±10% | 2 | 3.8/8.7 | 98.5 | | | |
| 2 | prepreg | 2.9 | | 4 | | | | | | | |
| | GND | 1.2 | 1.0oz | | | | | | | | |
| | core | 27.0 | | 4.5 | | | | | | | |
| 3 | VCC | 1.2 | 1.0oz | | | | | | | | |
| | prepreg | 2.9 | | 4 | | | | | | | |
| | BOTTOM | 1.6 | 0.3oz+plating | | 50±10% | 3 | 4 | 52.18 | | | |
| 4 | | | | | 90±10% | 3 | 4.5/7.5 | 90.03 | | | |
| | | | | | 100±10% | 3 | 3.8/8.7 | 98.5 | | | |
| solder mask | | 0.5 | SM | 4.25 | | | | | | | |
| Board thickness: | | 39.4 | | | | | | | | | |

Stack Up

- 2. Two-layer board,
- 1) Follow the differential pair routing rules. Parallel traces, length \pm 10mil.
- 2) The differential pair are isolated. Add through holes on both sides of the differential pair, as shown in Figure 1.
- 3) The differential pair can be set with a line width of 6 mils/line spacing of 6 mils. The stacking parameters are shown in Figure 2 below.

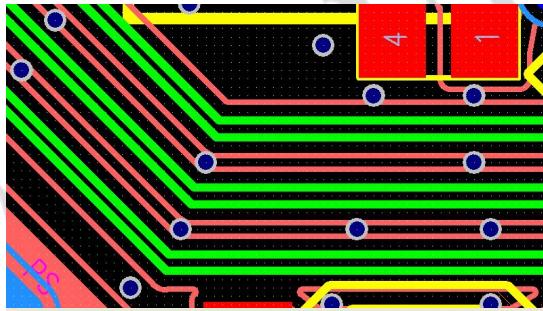
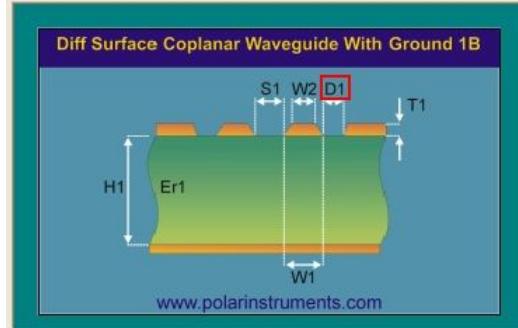


Figure 1

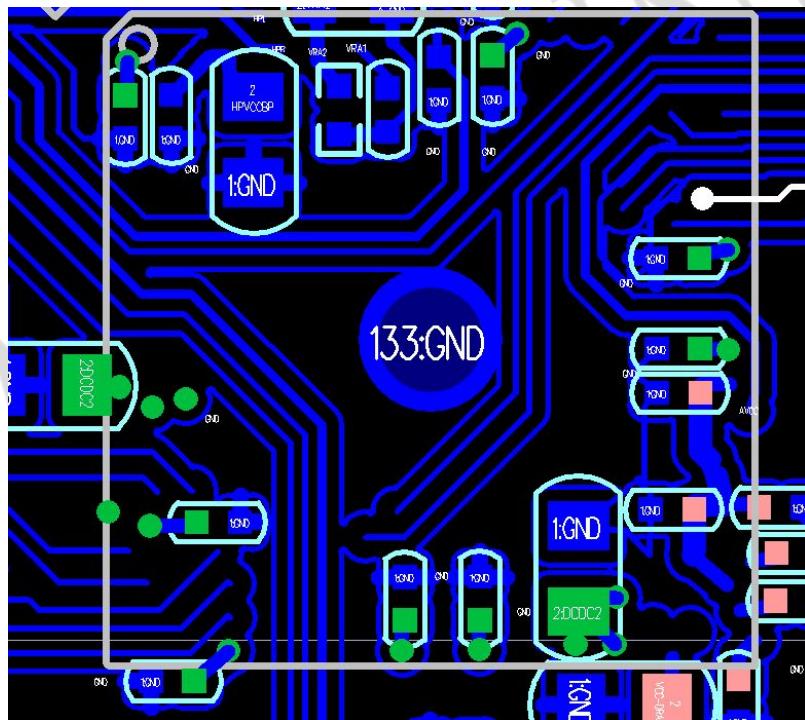


| Substrate 1 Height | H1 | 25.4000 | +/- | 0.0000 | Tolerance | Minimum | Maximum | Calculate |
|-------------------------|-----|---------|-----|--------|-----------|---------|---------|-----------|
| Substrate 1 Dielectric | Er1 | 4.2000 | +/- | 0.0000 | | 4.2000 | 4.2000 | Calculate |
| Lower Trace Width | W1 | 6.0000 | +/- | 0.0000 | | 6.0000 | 6.0000 | Calculate |
| Upper Trace Width | W2 | 6.0000 | +/- | 0.0000 | | 6.0000 | 6.0000 | Calculate |
| Trace Separation | S1 | 6.0000 | +/- | 0.0000 | | 6.0000 | 6.0000 | Calculate |
| Ground Strip Separation | D1 | 5.0000 | +/- | 0.0000 | | 5.0000 | 5.0000 | Calculate |
| Trace Thickness | T1 | 1.4000 | +/- | 0.0000 | | 1.4000 | 1.4000 | Calculate |
| Differential Impedance | | | | | | | | |
| Zdiff | | | | 114.77 | | 114.77 | 114.77 | Calculate |

Figure 2

CPU POWER

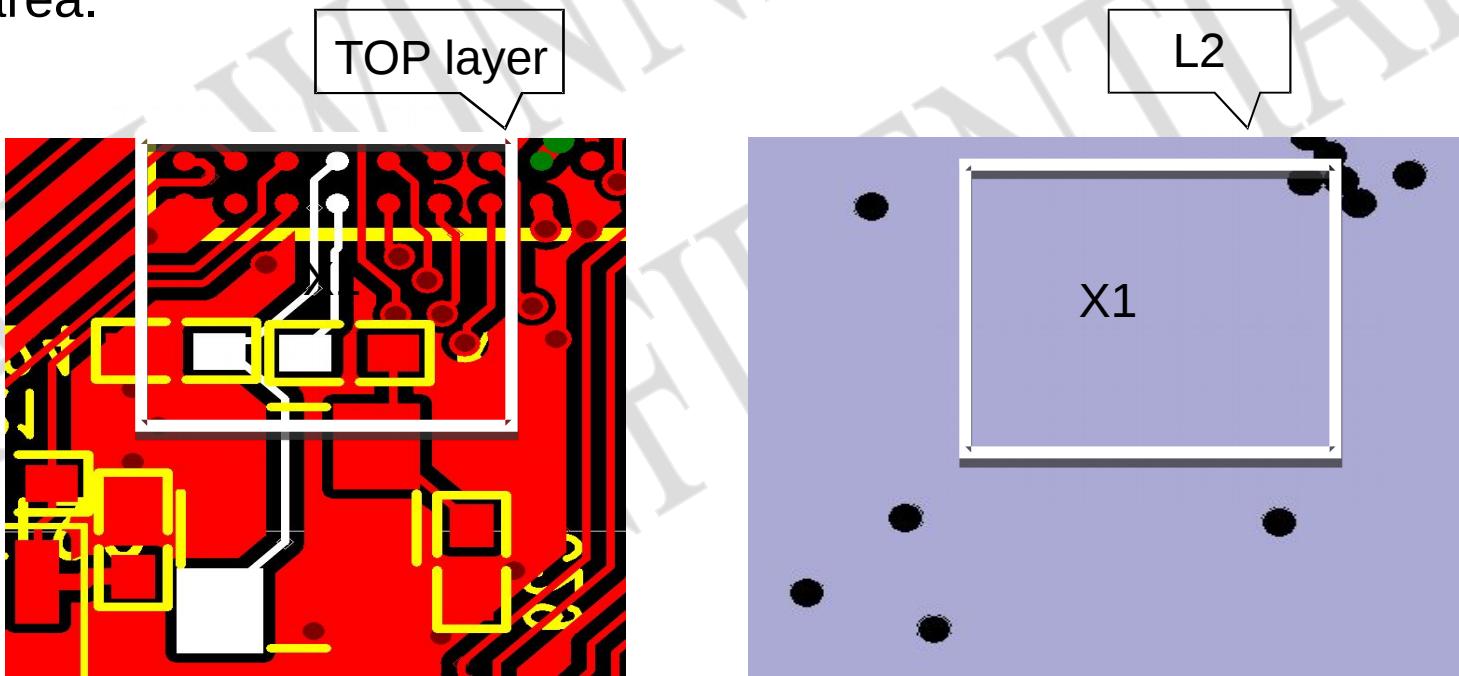
- 3. Bypass Capacitor - Double Sided Layout
 - 1) The CPU/SYS bypass capacitors are placed on the back of the V3s PCB and evenly distributed across the power supply pins.
 - 2) Make sure that the capacitors do not have more than one via hole per VCC pin or GND pin.



Note: The CPU/SYS bypass capacitor are in green; the DRAM bypass capacitor are in pink.

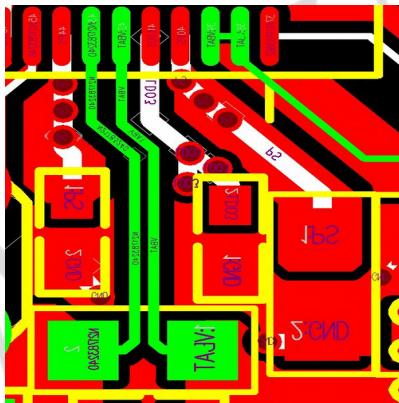
Crystal

- › 1. Place the crystal as close to the IC as possible to avoid long crystal traces.
- › 2. The matching capacitor of the crystal must be placed close to the crystal
- › 3. Peripheral and adjacent layers of the crystal and its trace areas must be shielded with GND.
- › 4. Avoid other traces in layers adjacent to the crystal and its routing area.



AXP209 POWER

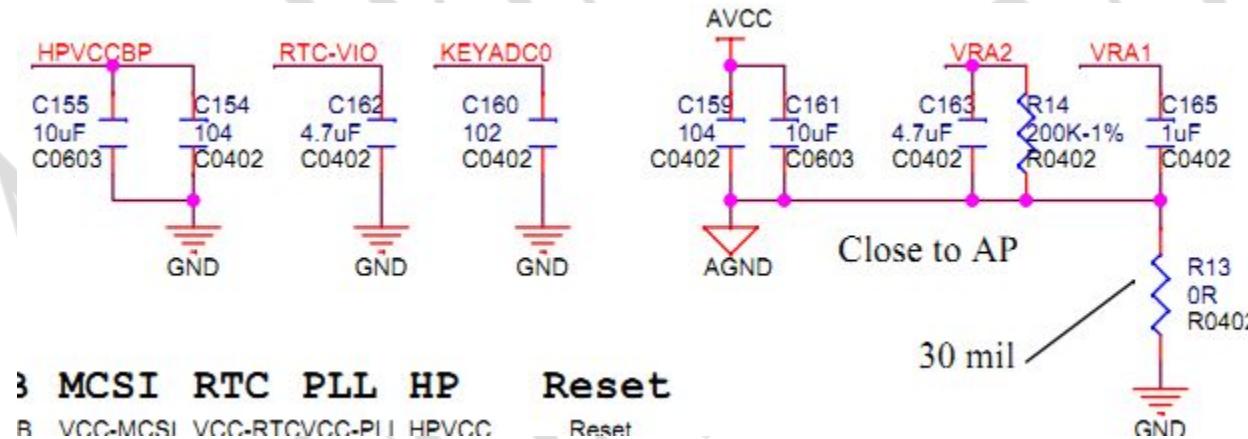
- › 1. For the AXP209, make the ground plane as complete as possible, it is the most effective solution for heat disipation. At the same time, the bottom PAD needs to be copper-plated in a fully connected manner with the ground plane.
- › 2. The charging loop must be short and wide. Do not run the charging trace parallel to other traces. The sampled feedback signals BATSENSE and CHSENSE are pulled out in parallel from both ends of the pad of the sampling resistor as shown in the figure below.



- › 3. Do not route the ground under the inductor to avoid switching noise from interfering with the ground plane.
- › 4. Sensitive signals such as clock must not be routed directly between the inductor traces.

AUDIO

1. AGND is single-grounded through the 0R resistor; the line width from the resistor to AGND is 1mm (80 mils).
2. VRA1/VRA2 is referenced to AGND, and the capacitance cannot be modified.
3. Audio's peripheral device layout and power signal area must not overlap.
4. LINEOUTR/LINEOUTL/MICIN/MICIN must be well shielded with ground to protect each pair of signals separately. Keep traces and vias away from DRAM, LCD high-speed signals.



3 MCSI RTC PLL HP Reset
B VCC-MCSI VCC-RTCVCC-PLL HPVCC Reset

CAMERA

- 1. The capacitor on MCLK must be close to the slave and the resistor must be close to the master.
- 2. Make sure the camera is in the correct direction.
- 3. The length of the main circuit and camera socket traces is 2000mil, which prevents the camera module FPC from being too long.
- 4. The AVDD, IOVDD, and DVDD filter capacitors need to be placed close to the camera daughter board connector.
- 5. The MCLK must be protected by a ground within 2 vias and the CLK signal must be routed as an inner trace on a 4-layer board. If it is a parallel port sensor, CSI-PCLK also needs to be protected, and have a minimum number of layer changes.
- 6. MIPI sensor clock and signals must be differentially routed with a high priority, a differential impedance of 100 ohms, with a minimum number of layers, and avoid cutting the reference plane.

USB

- 1. The differential impedance is 90 ohms, avoid cutting the reference plane.
- 2. USB D+/D- differential signal pair routing.
- 3. The length of the USB cable is controlled within 4000 mils and must not contain more than two trace vias.

CARD

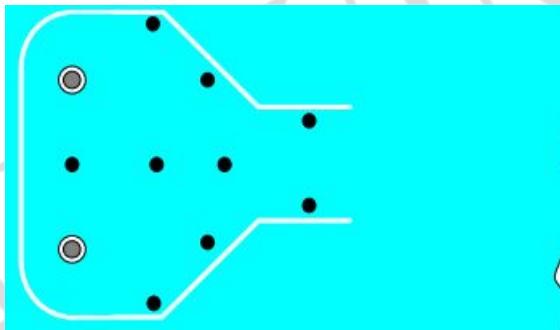
- 1. The card holder VCC capacitor and card holder must be on the same side of the PCB board and placed near the card holder.
- 2. The traces are separated from the high-frequency signals as much as possible. The data lines are grouped and there must be 2 or less vias.
- 3. CLK must be surrounded with ground.

- 1. The capacitor on CLK must be close to the slave and the resistor must be close to the master.
- 2. CLK must be surrounded with ground, traces must have 2 vias at most, CLK should be routed as inner traces on 4-layer board.
- 3. Backlight output capacitor rated voltage must be 50V.

ESD

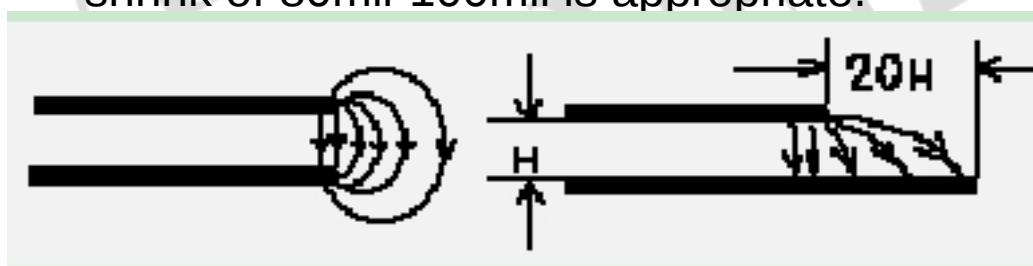
- 1. Remove the unnecessary power trace area of the third layer, VCC-3.3V can be connected using 30mil traces and fill with GND as much as possible.
- 2. The CPU/VDD-SYS/DRAM capacitor must be placed near the CPU. The GND of these capacitors should be reinforced with more vias.
- 3. CPU/VDD-SYS/DRAM should not be placed in sensitive areas such as the edge of the board, and their protection should be strengthened.
- 4. Try not to route traces below the camera/TF Card nest (vertical projection area of the nest, including 1 to 4 layers).
- 5. The fixed pad is connected to the main ground to prevent floating ground.

- 6. The Reset signal should not go on the edge of the board or in the sensitive area, and its protection should be strengthened. The filter capacitor should be placed close to the CPU.
- 7. For crystal traces close to an IO, a 20 mil trench should be cut on one side of the ground plane near the IO to reduce the effect of static electricity on it.



EMC

- 1. The CSI traces must use a complete reference plane as much as possible; signal traces must be connected in series with 33 ohm resistors; if the number of PCB layers exceeds 4 layers, inner traces are recommended.
- 2. LCD CLK, SDIO CLK, SDC CLK, CSI MCLK, CSI PCLK: Try to protect traces with ground or route on the inner layer as much as possible. Surround with ground and stitch with vias. The distance between the vias is $\leq 10\text{mm}$ (400 mils); the traces should not cut the reference plane; increase the series resistance. The series resistor must be placed near the master.
- 3. 24MHz crystal relative to the board edge distance $\geq 25\text{mm}$ (1000mils).
- 4. The VCC plane shrinks by 30 mils along the edge of the board relative to the GND plane. To prevent power radiation, it is best to shrink the power plane and follow this rule as much as possible. With an H (dielectric thickness between the power supply and the ground) as a unit, if the inner contraction is 20H, 70% of the electric field can be confined within the grounding edge; the inner contraction of 100H can limit the 8% electric field. General four-layer power supply layer shrink of 80mil-100mil is appropriate.



Structure

- 1. When the enclosure is metallic, use screw holes to get a good contact between the motherboard and the enclosure, thus greatly improving the ESD performance.
- 2. Do not connect the cables (camera, LCD, etc.) to the housing and fold them inward when installing. This prevents ESD from causing interference through cables.
- 3. When the screen is in close contact with the motherboard, pay attention to adding a heat sink to the CPU to prevent the LCD screen from displaying bad pixels (black blocks appear at high temperature) due to the high temperature of the CPU.

Revision History

| PART1 | Date | Changes compared to previous issue |
|-------|------------|------------------------------------|
| V1.0 | 2015-05-18 | Release Version |
| | | |

| PART2 | Date | Changes compared to previous issue |
|-------|------------|------------------------------------|
| V1.0 | 2015-05-18 | Release Version |
| | | |



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