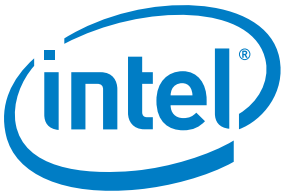

Intel® Quark™ SoC X1000 Platform: DDR3 Dual Rank Memory Down Schematic Guide

White Paper

December 2014

Document Number: 331167-003

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Revision History

Date	Revision	Description
December 2014	003	Minor updates.
October 2014	002	Minor updates.
September 2014	001	Initial release.

1 DDR3 Memory Introduction

This document covers the guidelines required to design a Intel® Quark™ SoC X1000 platform with DDR3 Memory Down on a Type 3 PCB at up to 800 MT/s.

1.1 Reference Documents

Table 1. Reference Documents

Document	Doc #
Intel® Quark™ SoC X1000™ SoC X1000 Platform Design Guide	330258
Intel® Quark™ SoC X1000™ Platform- DDR3 Dual Rank Memory Down Broad Layout Guide Technical White Paper	331204
Intel® Quark™ SoC X1000 SoC X1000 DDR3 Dual Rank Tree Topology Trace Length Calculator	551278
Intel® Quark™ SoC X1000 Platform – MRC Swapping Code Example White Paper	331623

1.2 Supported Memory Configurations

Table 2. Supported Configurations

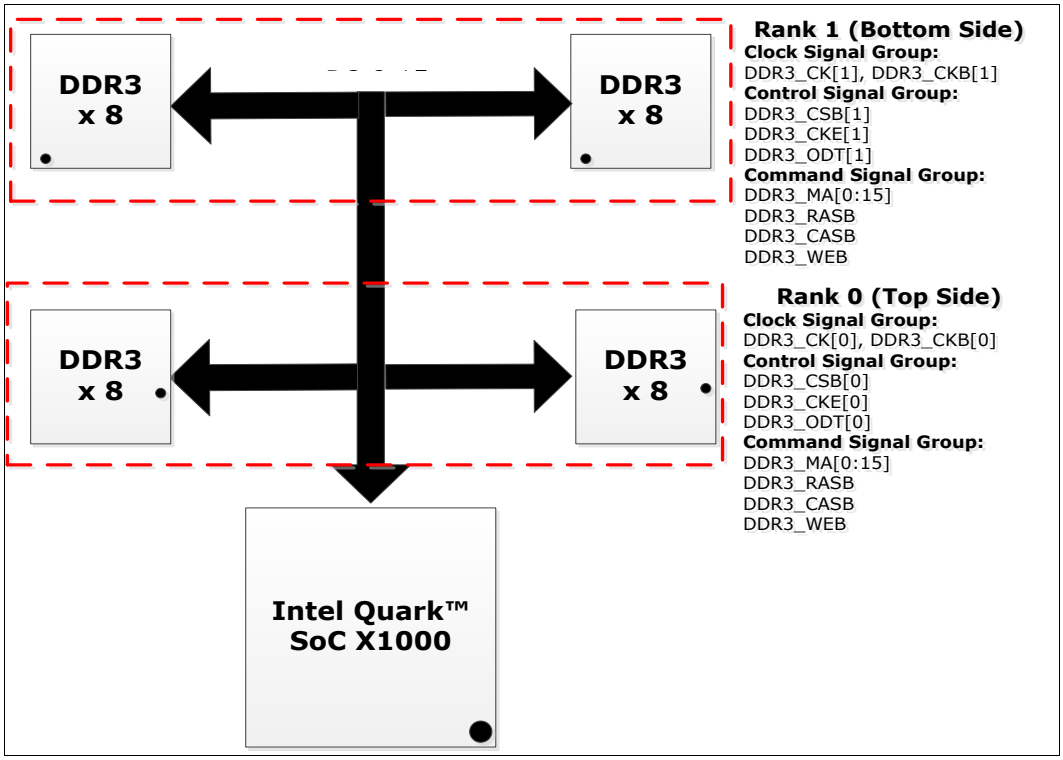
Parameter	DDR3
Topology	Memory Down Double-T Topology
Memory Capacity	512MB-2GB
Speed Supported	800 MT/s
Number of Channels Supported	1-Channel
Number of Ranks Supported	2
DRAM Device Densities Supported	1 Gb x 8 2 Gb x 8 4 Gb x 8
PCB Type	Type 3
PCB Layers	6 Layers

2 DDR3 Dual Rank Memory Down Design

2.1 Dual Rank Memory Down Block Diagram

Figure 1 shows the block diagram design for Dual Rank Memory Down.

Figure 1. Dual Rank Memory Down Block Diagram



This chapter provides the design guidelines based on this diagram.

In this topology, the 2 SDRAM devices of the 2nd rank are placed on the bottom layer , under the 2 SDRAM devices of the 1st rank, which are placed on the top layer.

The data (DQ) and address signals (MA) are able to take advantage of the mirrored parts so that both top and bottom BGA balls can be directly connected through a via.

The rest of signals, however, are not completely mirrored between top and bottom devices.

Swapping the pins of either the top or bottom device allows the two BGA balls that share the same data and address signal to stay physically closer to each other, within same type of signals.

This enables short and balanced stubs, which ease routing and improve signal integrity.

Refer to Section 2.2 for the bit swapping recommendation and Section 2.3 for the pin comparison to single rank configuration

Bit swapping is not necessary, but is recommended, to ease layout design. Please update the MRC as well if bit swapping is made.

Note: The guidelines on MRC code location in BIOS need to be changed. Refer to the *Intel® Quark™ SoC X1000 Platform – MRC Swapping Code Example White Paper* (doc#:331623) for more information.

2.2 Pin-to-Pin Connection for Dual Rank Memory Down

Table 3. Dual Rank Memory Pin Connection for Rank 0, Top Side

DDR3 SDRAM		Signal from SOC – RANK 0			
		Top Left (DQ 8 -15)		Top Right (DQ 0 - 7)	
Pin	Pinout Description	Pin	Netname	Pin	Netname
A1	GND	A1	GND	A1	GND
A2	VDD	A2	V1P5_S3	A2	V1P5_S3
A3	NC	A3		A3	
A7	NF	A7		A7	
A8	GND	A8	GND	A8	GND
A9	VDD	A9	V1P5_S3	A9	V1P5_S3
B1	GND	B1	GND	B1	GND
B2	GND	B2	GND	B2	GND
B3	DQ<0>	B3	M_DQ<10>	B3	M_DQ<0>
B7	DM/TDQS	B7	DDR3_DM1	B7	DDR3_DM0
B8	GND	B8	GND	B8	GND
B9	VDD	B9	V1P5_S3	B9	V1P5_S3
C1	VDD	C1	V1P5_S3	C1	V1P5_S3
C2	DQ<2>	C2	M_DQ<15>	C2	M_DQ<5>
C3	DQS<0>	C3	M_DQS<1>	C3	M_DQS<0>
C7	DQ<1>	C7	M_DQ<12>	C7	M_DQ<7>

DDR3 SDRAM		Signal from SOC – RANK 0			
		Top Left (DQ 8 -15)		Top Right (DQ 0 - 7)	
Pin	Pinout Description	Pin	Netname	Pin	Netname
C8	DQ<3>	C8	M_DQ<9>	C8	M_DQ<2>
C9	GND	C9	GND	C9	GND
D1	GND	D1	GND	D1	GND
D2	DQ<6>	D2	M_DQ<11>	D2	M_DQ<4>
D3	DQS_N<0>	D3	M_DQS_N<1>	D3	M_DQS_N<0>
D7	VDD	D7	V1P5_S3	D7	V1P5_S3
D8	GND	D8	GND	D8	GND
D9	GND	D9	GND	D9	GND
E1	VREFDQ	E1	VREF_22	E1	VREF_21
E2	VDD	E2	V1P5_S3	E2	V1P5_S3
E3	DQ<4>	E3	M_DQ<14>	E3	M_DQ<6>
E7	DQ<7>	E7	M_DQ<13>	E7	M_DQ<1>
E8	DQ<5>	E8	M_DQ<8>	E8	M_DQ<3>
E9	VDD	E9	V1P5_S3	E9	V1P5_S3
F1	NC	F1		F1	
F2	GND	F2	GND	F2	GND
F3	RAS_N	F3	M_RAS_N	F3	M_RAS_N
F7	CK<0>	F7	M_CK<0>	F7	M_CK<0>
F8	GND	F8	GND	F8	GND
F9	NC	F9		F9	
G1	ODT<0>	G1	M_ODT<0>	G1	M_ODT<0>
G2	VDD	G2	V1P5_S3	G2	V1P5_S3
G3	CAS_N	G3	M_CAS_N	G3	M_CAS_N
G7	CK_N<0>	G7	M_CK_N<0>	G7	M_CK_N<0>
G8	VDD	G8	V1P5_S3	G8	V1P5_S3
G9	CKE<0>	G9	M_CKE<0>	G9	M_CKE<0>
H1	NC	H1		H1	
H2	CS_N<0>	H2	M_CS_N<0>	H2	M_CS_N<0>
H3	WE_N	H3	M_WE_N	H3	M_WE_N
H7	A<10>	H7	M_MA<10>	H7	M_MA<10>
H8	ZQ	H8	Pull to GND with	H8	Pull to GND with

DDR3 SDRAM		Signal from SOC – RANK 0			
		Top Left (DQ 8 -15)		Top Right (DQ 0 - 7)	
Pin	Pinout Description	Pin	Netname	Pin	Netname
			240ohm,1%		240ohm,1%
H9	NC	H9		H9	
J1	GND	J1	GND	J1	GND
J2	BS<0>	J2	M_BS<0>	J2	M_BS<0>
J3	BS<2>	J3	M_BS<2>	J3	M_BS<2>
J7	A<15>	J7	M_MA<15>	J7	M_MA<15>
J8	VREFCA	J8	VREF_12	J8	VREF_11
J9	GND	J9	GND	J9	GND
K1	VDD	K1	V1P5_S3	K1	V1P5_S3
K2	A<3>	K2	M_MA<3>	K2	M_MA<3>
K3	A<0>	K3	M_MA<0>	K3	M_MA<0>
K7	A<12>	K7	M_MA<12>	K7	M_MA<12>
K8	BS<1>	K8	M_BS<1>	K8	M_BS<1>
K9	VDD	K9	V1P5_S3	K9	V1P5_S3
L1	GND	L1	GND	L1	GND
L2	A<5>	L2	M_MA<5>	L2	M_MA<5>
L3	A<2>	L3	M_MA<2>	L3	M_MA<2>
L7	A<1>	L7	M_MA<1>	L7	M_MA<1>
L8	A<4>	L8	M_MA<4>	L8	M_MA<4>
L9	GND	L9	GND	L9	GND
M1	V1P5_S3	M1	V1P5_S3	M1	V1P5_S3
M2	A<7>	M2	M_MA<7>	M2	M_MA<7>
M3	A<9>	M3	M_MA<9>	M3	M_MA<9>
M7	A<11>	M7	M_MA<11>	M7	M_MA<11>
M8	A<6>	M8	M_MA<6>	M8	M_MA<6>
M9	VDD	M9	V1P5_S3	M9	V1P5_S3
N1	GND	N1	GND	N1	GND
N2	RST_N	N2	M_DRAMRST_N	N2	M_DRAMRST_N
N3	A<13>	N3	M_MA<13>	N3	M_MA<13>
N7	A<14>	N7	M_MA<14>	N7	M_MA<14>
N8	A<8>	N8	M_MA<8>	N8	M_MA<8>
N9	GND	N9	GND	N9	GND

Table 4. Dual Rank Memory Pin Connection for Rank 1, Bottom Side

DDR3 SDRAM		Signal from SOC – RANK 1			
		Bottom Left (DQ 8 -15)		Bottom Right (DQ 0 - 7)	
Pin	Pinout Signal	Pin	Netname	Pin	Netname
A1	GND	A1	GND	A1	GND
A2	VDD	A2	V1P5_S3	A2	V1P5_S3
A3	NC	A3		A3	
A7	NF	A7		A7	
A8	GND	A8	GND	A8	GND
A9	VDD	A9	V1P5_S3	A9	V1P5_S3
B1	GND	B1	GND	B1	GND
B2	GND	B2	GND	B2	GND
B3	DQ<0>	B3	M_DQ<12>	B3	M_DQ<7>
B7	DM/TDQS	B7	DDR3_DM1	B7	DDR3_DM0
B8	GND	B8	GND	B8	GND
B9	VDD	B9	V1P5_S3	B9	V1P5_S3
C1	VDD	C1	V1P5_S3	C1	V1P5_S3
C2	DQ<2>	C2	M_DQ<9>	C2	M_DQ<2>
C3	DQS<0>	C3	M_DQS<1>	C3	M_DQS<0>
C7	DQ<1>	C7	M_DQ<10>	C7	M_DQ<0>
C8	DQ<3>	C8	M_DQ<15>	C8	M_DQ<5>
C9	GND	C9	GND	C9	GND
D1	GND	D1	GND	D1	GND
D2	DQ<6>	D2	M_DQ<8>	D2	M_DQ<3>
D3	DQS_N<0>	D3	M_DQS_N<1>	D3	M_DQS_N<0>
D7	VDD	D7	V1P5_S3	D7	V1P5_S3
D8	GND	D8	GND	D8	GND
D9	GND	D9	GND	D9	GND
E1	VREFDQ	E1	VREF_12	E1	VREF_11
E2	VDD	E2	V1P5_S3	E2	V1P5_S3
E3	DQ<4>	E3	M_DQ<13>	E3	M_DQ<1>
E7	DQ<7>	E7	M_DQ<14>	E7	M_DQ<6>
E8	DQ<5>	E8	M_DQ<11>	E8	M_DQ<4>
E9	VDD	E9	V1P5_S3	E9	V1P5_S3

DDR3 SDRAM		Signal from SOC – RANK 1			
		Bottom Left (DQ 8 -15)		Bottom Right (DQ 0 - 7)	
Pin	Pinout Signal	Pin	Netname	Pin	Netname
F1		F1		F1	
F2	GND	F2	GND	F2	GND
F3	RAS_N	F3	M_RAS_N	F3	M_RAS_N
F7	CK<0>	F7	M_CK<1>	F7	M_CK<1>
F8	GND	F8	GND	F8	GND
F9		F9		F9	
G1	ODT<0>	G1	M_ODT<1>	G1	M_ODT<1>
G2	VDD	G2	V1P5_S3	G2	V1P5_S3
G3	CAS_N	G3	M_CAS_N	G3	M_CAS_N
G7	CK_N<0>	G7	M_CK_N<1>	G7	M_CK_N<1>
G8	VDD	G8	V1P5_S3	G8	V1P5_S3
G9	CKE<0>	G9	M_CKE<1>	G9	M_CKE<1>
H1		H1		H1	
H2	CS_N<0>	H2	M_CS_N<1>	H2	M_CS_N<1>
H3	WE_N	H3	M_WE_N	H3	M_WE_N
H7	A<10>	H7	M_MA<10>	H7	M_MA<10>
H8	ZQ	H8	Pull to GND with 240ohm,1%	H8	Pull to GND with 240ohm,1%
H9		H9		H9	
J1	GND	J1	GND	J1	GND
J2	BS<0>	J2	M_BS<1>	J2	M_BS<1>
J3	BS<2>	J3	M_BS<2>	J3	M_BS<2>
J7	A<15>	J7	M_MA<15>	J7	M_MA<15>
J8	VREFCA	J8	VREF_22	J8	VREF_21
J9	GND	J9	GND	J9	GND
K1	VDD	K1	V1P5_S3	K1	V1P5_S3
K2	A<3>	K2	M_MA<4>	K2	M_MA<4>
K3	A<0>	K3	M_MA<0>	K3	M_MA<0>
K7	A<12>	K7	M_MA<12>	K7	M_MA<12>
K8	BS<1>	K8	M_BS<0>	K8	M_BS<0>
K9	VDD	K9	V1P5_S3	K9	V1P5_S3
L1	GND	L1	GND	L1	GND

DDR3 SDRAM		Signal from SOC – RANK 1			
		Bottom Left (DQ 8 -15)		Bottom Right (DQ 0 - 7)	
Pin	Pinout Signal	Pin	Netname	Pin	Netname
L2	A<5>	L2	M_MA<6>	L2	M_MA<6>
L3	A<2>	L3	M_MA<2>	L3	M_MA<2>
L7	A<1>	L7	M_MA<1>	L7	M_MA<1>
L8	A<4>	L8	M_MA<3>	L8	M_MA<3>
L9	GND	L9	GND	L9	GND
M1	V1P5_S3	M1	V1P5_S3	M1	V1P5_S3
M2	A<7>	M2	M_MA<8>	M2	M_MA<8>
M3	A<9>	M3	M_MA<9>	M3	M_MA<9>
M7	A<11>	M7	M_MA<11>	M7	M_MA<11>
M8	A<6>	M8	M_MA<5>	M8	M_MA<5>
M9	VDD	M9	V1P5_S3	M9	V1P5_S3
N1	GND	N1	GND	N1	GND
N2	RST_N	N2	M_DRAMRST_N	N2	M_DRAMRST_N
N3	A<13>	N3	M_MA<13>	N3	M_MA<13>
N7	A<14>	N7	M_MA<14>	N7	M_MA<14>
N8	A<8>	N8	M_MA<7>	N8	M_MA<7>
N9	GND	N9	GND	N9	GND

2.3 Pin Swap Comparison between Single Rank and Dual Rank

Table 5. Pin Swap from Single Rank to Dual Rank for DQ (0 – 7)

Single Rank		Dual Rank			
U1B5 (Top Right)		U1B5 (Top Right) - Rank 0		U2 (Bottom Right) - Rank 1	
Pin	Signals	Pin	Signals	Pin	Signals
A1	GND	A1	GND	A1	GND
A2	V1P5_S3	A2	V1P5_S3	A2	V1P5_S3
A3		A3		A3	
A7		A7		A7	
A8	GND	A8	GND	A8	GND
A9	V1P5_S3	A9	V1P5_S3	A9	V1P5_S3
B1	GND	B1	GND	B1	GND
B2	GND	B2	GND	B2	GND
B3	M_DQ<0>	B3	M_DQ<0>	B3	M_DQ<7>
B7	DDR3_DM0	B7	DDR3_DM0	B7	DDR3_DM0
B8	GND	B8	GND	B8	GND
B9	V1P5_S3	B9	V1P5_S3	B9	V1P5_S3
C1	V1P5_S3	C1	V1P5_S3	C1	V1P5_S3
C2	M_DQ<2>	C2	M_DQ<5>	C2	M_DQ<2>
C3	M_DQS<0>	C3	M_DQS<0>	C3	M_DQS<0>
C7	M_DQ<1>	C7	M_DQ<7>	C7	M_DQ<0>
C8	M_DQ<3>	C8	M_DQ<2>	C8	M_DQ<5>
C9	GND	C9	GND	C9	GND
D1	GND	D1	GND	D1	GND
D2	M_DQ<6>	D2	M_DQ<4>	D2	M_DQ<3>
D3	M_DQS_N<0>	D3	M_DQS_N<0>	D3	M_DQS_N<0>
D7	V1P5_S3	D7	V1P5_S3	D7	V1P5_S3
D8	GND	D8	GND	D8	GND
D9	GND	D9	GND	D9	GND
E1	VREF	E1*	VREF_21	E1**	VREF_11
E2	V1P5_S3	E2	V1P5_S3	E2	V1P5_S3
E3	M_DQ<4>	E3	M_DQ<6>	E3	M_DQ<1>

Single Rank		Dual Rank			
U1B5 (Top Right)		U1B5 (Top Right) - Rank 0		U2 (Bottom Right) - Rank 1	
Pin	Signals	Pin	Signals	Pin	Signals
E7	M_DQ<7>	E7	M_DQ<1>	E7	M_DQ<6>
E8	M_DQ<5>	E8	M_DQ<3>	E8	M_DQ<4>
E9	V1P5_S3	E9	V1P5_S3	E9	V1P5_S3
F1		F1		F1	
F2	GND	F2	GND	F2	GND
F3	M_RAS_N	F3	M_RAS_N	F3	M_RAS_N
F7	M_CK<0>	F7	M_CK<0>	F7	M_CK<1>
F8	GND	F8	GND	F8	GND
F9		F9		F9	
G1	M_ODT<0>	G1	M_ODT<0>	G1	M_ODT<1>
G2	V1P5_S3	G2	V1P5_S3	G2	V1P5_S3
G3	M_CAS_N	G3	M_CAS_N	G3	M_CAS_N
G7	M_CK_N<0>	G7	M_CK_N<0>	G7	M_CK_N<1>
G8	V1P5_S3	G8	V1P5_S3	G8	V1P5_S3
G9	M_CKE<0>	G9	M_CKE<0>	G9	M_CKE<1>
H1		H1		H1	
H2	M_CS_N<0>	H2	M_CS_N<0>	H2	M_CS_N<1>
H3	M_WE_N	H3	M_WE_N	H3	M_WE_N
H7	M_MA<10>	H7	M_MA<10>	H7	M_MA<10>
H8	Pull down to GND with 240ohm,1% resistor	H8	Pull down to GND with 240ohm,1% resistor	H8	Pull down to GND with 240ohm,1% resistor
H9		H9		H9	
J1	GND	J1	GND	J1	GND
J2	M_BS<0>	J2	M_BS<0>	J2	M_BS<1>
J3	M_BS<2>	J3	M_BS<2>	J3	M_BS<2>
J7	M_MA<15>	J7	M_MA<15>	J7	M_MA<15>
J8	VREF_11	J8**	VREF_11	J8*	VREF_21
J9	GND	J9	GND	J9	GND
K1	V1P5_S3	K1	V1P5_S3	K1	V1P5_S3
K2	M_MA<3>	K2	M_MA<3>	K2	M_MA<4>

Single Rank		Dual Rank			
U1B5 (Top Right)		U1B5 (Top Right) - Rank 0		U2 (Bottom Right) - Rank 1	
Pin	Signals	Pin	Signals	Pin	Signals
K3	M_MA<0>	K3	M_MA<0>	K3	M_MA<0>
K7	M_MA<12>	K7	M_MA<12>	K7	M_MA<12>
K8	M_BS<1>	K8	M_BS<1>	K8	M_BS<0>
K9	V1P5_S3	K9	V1P5_S3	K9	V1P5_S3
L1	GND	L1	GND	L1	GND
L2	M_MA<5>	L2	M_MA<5>	L2	M_MA<6>
L3	M_MA<2>	L3	M_MA<2>	L3	M_MA<2>
L7	M_MA<1>	L7	M_MA<1>	L7	M_MA<1>
L8	M_MA<4>	L8	M_MA<4>	L8	M_MA<3>
L9	GND	L9	GND	L9	GND
M1	V1P5_S3	M1	V1P5_S3	M1	V1P5_S3
M2	M_MA<7>	M2	M_MA<7>	M2	M_MA<8>
M3	M_MA<9>	M3	M_MA<9>	M3	M_MA<9>
M7	M_MA<11>	M7	M_MA<11>	M7	M_MA<11>
M8	M_MA<6>	M8	M_MA<6>	M8	M_MA<5>
M9	V1P5_S3	M9	V1P5_S3	M9	V1P5_S3
N1	GND	N1	GND	N1	GND
N2	M_DRAMRST_N	N2	M_DRAMRST_N	N2	M_DRAMRST_N
N3	M_MA<13>	N3	M_MA<13>	N3	M_MA<13>
N7	M_MA<14>	N7	M_MA<14>	N7	M_MA<14>
N8	M_MA<8>	N8	M_MA<8>	N8	M_MA<7>
N9	GND	N9	GND	N9	GND

Notes:

1. * Connect Rank 0 SDRAM pin E1 and Rank 1 SDRAM pin J8 at same net, VREF_21 to meet the design guide rules for the dual rank implementation.
2. ** Connect Rank 0 SDRAM pin J8 and Rank 1 SDRAM pin E1 at same net, VREF_11 to meet the design guide rules for the dual rank implementation.
3. Highlighted signal indicate the pin swapping occur. Swapping the signal allows the some of the address lines to be mirror image between SDRAMs on the top & bottom.

Table 6. Pin Swap from Single Rank to Dual Rank for DQ (8 – 15)

Single Rank		Dual Rank			
U1A1 (Top Left)		U1A1 (Top Left) - Rank 0		U1 (Bottom Left) - Rank 1	
Pin	Signals	Pin	Signals	Pin	Signals
A1	GND	A1	GND	A1	GND
A2	V1P5_S3	A2	V1P5_S3	A2	V1P5_S3
A3		A3		A3	
A7		A7		A7	
A8	GND	A8	GND	A8	GND
A9	V1P5_S3	A9	V1P5_S3	A9	V1P5_S3
B1	GND	B1	GND	B1	GND
B2	GND	B2	GND	B2	GND
B3	M_DQ<8>	B3	M_DQ<10>	B3	M_DQ<12>
B7	DDR3_DM1	B7	DDR3_DM1	B7	DDR3_DM1
B8	GND	B8	GND	B8	GND
B9	V1P5_S3	B9	V1P5_S3	B9	V1P5_S3
C1	V1P5_S3	C1	V1P5_S3	C1	V1P5_S3
C2	M_DQ<10>	C2	M_DQ<15>	C2	M_DQ<9>
C3	M_DQS<1>	C3	M_DQS<1>	C3	M_DQS<1>
C7	M_DQ<9>	C7	M_DQ<12>	C7	M_DQ<10>
C8	M_DQ<11>	C8	M_DQ<9>	C8	M_DQ<15>
C9	GND	C9	GND	C9	GND
D1	GND	D1	GND	D1	GND
D2	M_DQ<14>	D2	M_DQ<11>	D2	M_DQ<8>
D3	M_DQS_N<1>	D3	M_DQS_N<1>	D3	M_DQS_N<1>
D7	V1P5_S3	D7	V1P5_S3	D7	V1P5_S3
D8	GND	D8	GND	D8	GND
D9	GND	D9	GND	D9	GND
E1	VREF	E1*	VREF_22	E1**	VREF_12
E2	V1P5_S3	E2	V1P5_S3	E2	V1P5_S3
E3	M_DQ<12>	E3	M_DQ<14>	E3	M_DQ<13>
E7	M_DQ<15>	E7	M_DQ<13>	E7	M_DQ<14>
E8	M_DQ<13>	E8	M_DQ<8>	E8	M_DQ<11>

Single Rank		Dual Rank			
U1A1 (Top Left)		U1A1 (Top Left) - Rank 0		U1 (Bottom Left) - Rank 1	
Pin	Signals	Pin	Signals	Pin	Signals
E9	V1P5_S3	E9	V1P5_S3	E9	V1P5_S3
F1		F1		F1	
F2	GND	F2	GND	F2	GND
F3	M_RAS_N	F3	M_RAS_N	F3	M_RAS_N
F7	M_CK<0>	F7	M_CK<0>	F7	M_CK<1>
F8	GND	F8	GND	F8	GND
F9		F9		F9	
G1	M_ODT<0>	G1	M_ODT<0>	G1	M_ODT<1>
G2	V1P5_S3	G2	V1P5_S3	G2	V1P5_S3
G3	M_CAS_N	G3	M_CAS_N	G3	M_CAS_N
G7	M_CK_N<0>	G7	M_CK_N<0>	G7	M_CK_N<1>
G8	V1P5_S3	G8	V1P5_S3	G8	V1P5_S3
G9	M_CKE<0>	G9	M_CKE<0>	G9	M_CKE<1>
H1		H1		H1	
H2	M_CS_N<0>	H2	M_CS_N<0>	H2	M_CS_N<1>
H3	M_WE_N	H3	M_WE_N	H3	M_WE_N
H7	M_MA<10>	H7	M_MA<10>	H7	M_MA<10>
H8	Pull down to GND with 240ohm,1% resistor	H8	Pull down to GND with 240ohm,1% resistor	H8	Pull down to GND with 240ohm,1% resistor
H9		H9		H9	
J1	GND	J1	GND	J1	GND
J2	M_BS<0>	J2	M_BS<0>	J2	M_BS<1>
J3	M_BS<2>	J3	M_BS<2>	J3	M_BS<2>
J7	M_MA<15>	J7	M_MA<15>	J7	M_MA<15>
J8	VREF	J8**	VREF_12	J8*	VREF_22
J9	GND	J9	GND	J9	GND
K1	V1P5_S3	K1	V1P5_S3	K1	V1P5_S3
K2	M_MA<3>	K2	M_MA<3>	K2	M_MA<4>
K3	M_MA<0>	K3	M_MA<0>	K3	M_MA<0>
K7	M_MA<12>	K7	M_MA<12>	K7	M_MA<12>

Single Rank		Dual Rank			
U1A1 (Top Left)		U1A1 (Top Left) - Rank 0		U1 (Bottom Left) - Rank 1	
Pin	Signals	Pin	Signals	Pin	Signals
K8	M_BS<1>	K8	M_BS<1>	K8	M_BS<0>
K9	V1P5_S3	K9	V1P5_S3	K9	V1P5_S3
L1	GND	L1	GND	L1	GND
L2	M_MA<5>	L2	M_MA<5>	L2	M_MA<6>
L3	M_MA<2>	L3	M_MA<2>	L3	M_MA<2>
L7	M_MA<1>	L7	M_MA<1>	L7	M_MA<1>
L8	M_MA<4>	L8	M_MA<4>	L8	M_MA<3>
L9	GND	L9	GND	L9	GND
M1	V1P5_S3	M1	V1P5_S3	M1	V1P5_S3
M2	M_MA<7>	M2	M_MA<7>	M2	M_MA<8>
M3	M_MA<9>	M3	M_MA<9>	M3	M_MA<9>
M7	M_MA<11>	M7	M_MA<11>	M7	M_MA<11>
M8	M_MA<6>	M8	M_MA<6>	M8	M_MA<5>
M9	V1P5_S3	M9	V1P5_S3	M9	V1P5_S3
N1	GND	N1	GND	N1	GND
N2	M_DRAMRST_N	N2	M_DRAMRST_N	N2	M_DRAMRST_N
N3	M_MA<13>	N3	M_MA<13>	N3	M_MA<13>
N7	M_MA<14>	N7	M_MA<14>	N7	M_MA<14>
N8	M_MA<8>	N8	M_MA<8>	N8	M_MA<7>
N9	GND	N9	GND	N9	GND

Notes:

1. *Connect Rank 0 SDRAM pin E1 and Rank 1 SDRAM pin J8 at same net, VREF_22 to meet the design guide rules for the dual rank implementation.
2. ** Connect Rank 0 SDRAM pin J8 and Rank 1 SDRAM pin E1 at same net, VREF_12 to meet the design guide rules for the dual rank implementation.
3. Highlighted signal indicate the pin swapping occur. Swapping the signal allows the some of the address lines to be mirror image between SDRAMs on the top & bottom.

2.4 Dual Rank Memory Down Schematic Design

This section provides an example of a schematic drawing that is based on bit swapping, as described in Section 2.3.

Note: This schematic design is not based on an actual working board design. It is a reference schematic only.

Figure 2. Intel® Quark™ SoC X1000 – Rank 0, M_DQ [0-7] Memory Down Schematic Design

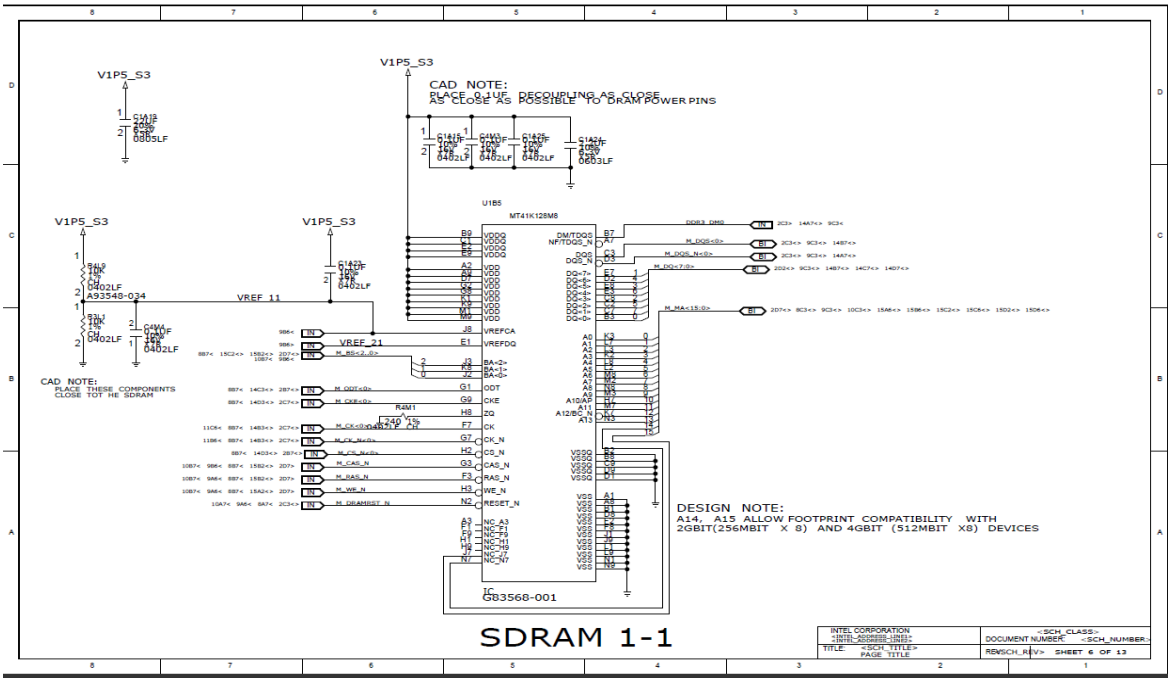


Figure 3. Intel® Quark™ SoC X1000 – Rank 0, M_DQ [8-15] Memory Down Schematic Design

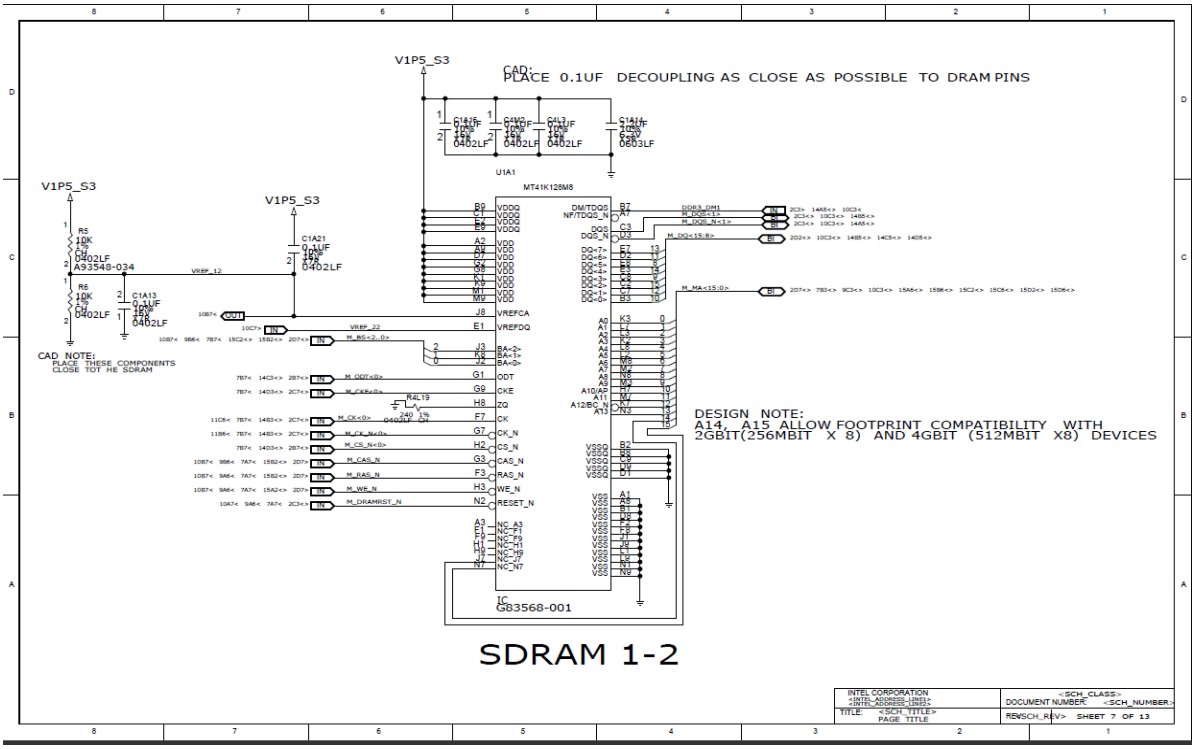


Figure 4. Intel® Quark™ SoC X1000 – Rank1, M_DQ [0-7] Memory Down Schematic Design

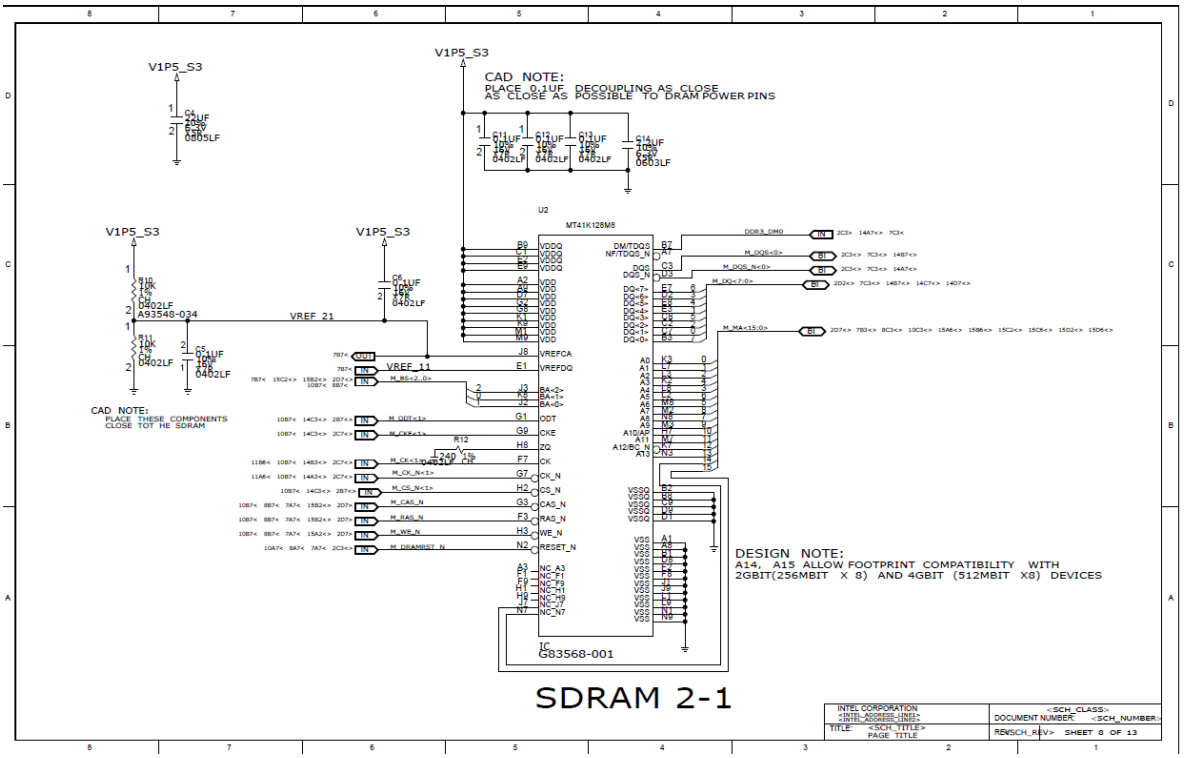


Figure 5. Intel® Quark™ SoC X1000 – Rank1, M_DQ [8-15] Memory Down Schematic Design

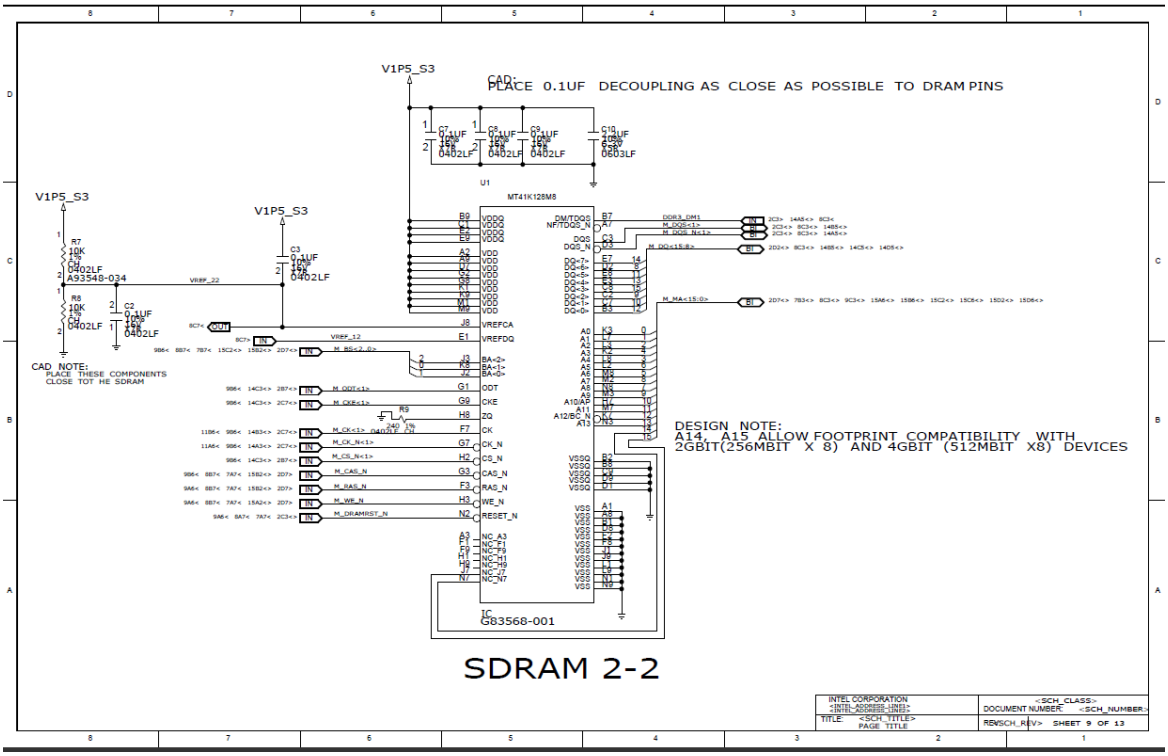
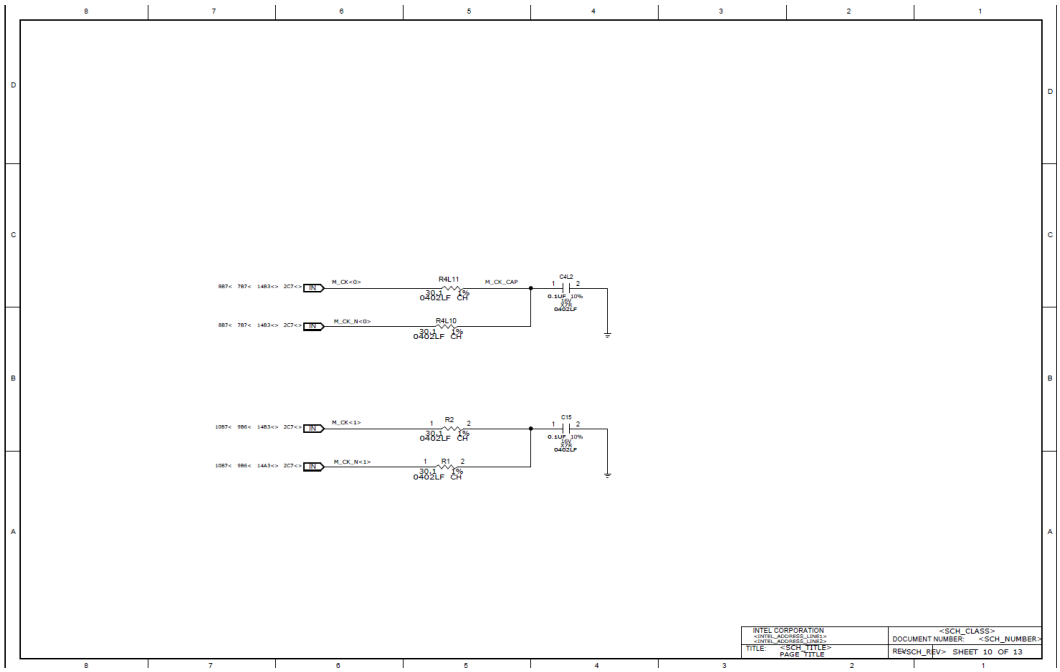


Figure 6. Intel® Quark™ SoC X1000 – Parallel Termination Resistors (30.1ohm)



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