



Intel[®] Quark[™] SoC X1000

Thermal and Mechanical Design Guide

June 2014



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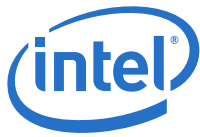
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Revision History

Date	Revision	Description
June 2014	002	Updates are indicated with change bars and include: <ul style="list-style-type: none">• Updated TDP• Updated Land Pattern
April 2014	001	Initial public release



1.0 Introduction

The Intel® Quark™ SoC X1000 is designed to be used in low-power embedded headless applications. Although the SoC is low power, it could be deployed in harsh industrial environments where the ambient temperature is high. Therefore, to ensure quality, reliability, and performance goals over the product's life cycle, the heat generated by the component must be properly dissipated. Typical methods to improve heat dissipation include the selective use of airflow ducting and chassis design, and the use of heatsinks.

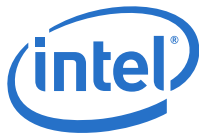
The goals of this document are to:

- Describe the thermal and mechanical specifications for the Intel® Quark™ SoC X1000
- Describe the reference solutions that meet the Intel® Quark™ SoC X1000 thermal and mechanical specifications

A properly designed thermal solution adequately cools the device die temperature at, or below, the thermal specification. This is accomplished by providing a suitable local ambient temperature, ensuring adequate local airflow, and minimizing the die to local ambient thermal resistance. Operation outside the functional limits can degrade system performance and may cause permanent changes in the operating characteristics of the component.

This document addresses thermal and mechanical design specifications for the Intel® Quark™ SoC X1000 only.

Note: Unless otherwise specified, the term SoC refers to the Intel® Quark™ SoC X1000.



1.1 Terminology

Definitions of terms used in this document are listed in Table 1.

Table 1. Terminology

Term	Definition
FCBGA	Flip Chip Ball Grid Array. A package type defined by a plastic substrate where a die is mounted using an under-fill C4 (Controlled Collapse Chip Connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. Note: The device arrives at the customer with solder balls attached.
T_{CASE}	The temperature of the component. This temperature is measured at the geometric center of the top of the package die. Also referred to as T_C .
$T_{CASE-MAX}$	Maximum allowed component temperature. This temperature is measured at the geometric center of the top of the package die. Also referred to as T_{C-MAX} .
TDP	Thermal Design Power. Target power dissipation level for thermal solution design. TDP is based on worst-case real world applications and benchmarks at maximum component temperature. TDP is not theoretical maximum power.
TIM	Thermal Interface Material. Thermally conductive material installed between two surfaces to improve heat transfer and reduce interface contact resistance.
T_J	The junction temperature of the component. Also referred to as $T_{JUNCTION}$.
T_{J-MAX}	Maximum allowed component junction temperature.
T_{LA}	Local ambient temperature. This is the temperature measured inside the chassis, approximately 1" upstream of a component heatsink. Also referred to as T_A .
T_{SINK}	Temperature measured at geometric center of the bottom surface of the heatsink base. Also referred to as T_S .
Ψ_{CA}	Case-to-ambient thermal characterization parameter. A measure of the thermal solution thermal performance using the total package power. Defined as $(T_{CASE} - T_{LA})/\text{Total Package Power}$. Note: Heat source must be specified for Ψ measurements.
Ψ_{CS}	Case-to-sink thermal characterization parameter. A measure of the thermal interface material performance using the total package power. Defined as $(T_{CASE} - T_S)/\text{Total Package Power}$. Also referred to as Ψ_{TIM} . Note: Heat source must be specified for Ψ measurements.
Ψ_{JA}	Junction-to-local ambient thermal characterization parameter ($^{\circ}\text{C}/\text{W}$)
Ψ_{SA}	Sink-to-ambient thermal characterization parameter. A measure of the heatsink thermal performance using the total package power. Defined as $(T_S - T_{LA})/\text{Total Package Power}$. Note: Heat source must be specified for Ψ measurements.
WTMD	Wide Trace Metal Defined

1.2 Reference Documents

Table 2 lists the reference documents.

Table 2. Reference Documents

Document	Document #
Intel® Quark™ SoC X1000 – Ball Out and Mechanical Package	514263
Intel® Quark™ SoC X1000 Datasheet	329676
Intel® Quark™ SoC X1000 Thermal Model User Guide (FloTherm*/Icepak*)	538053
Intel® Quark™ SoC X1000 Thermal Models	543243



1.3 Package Thermal Models

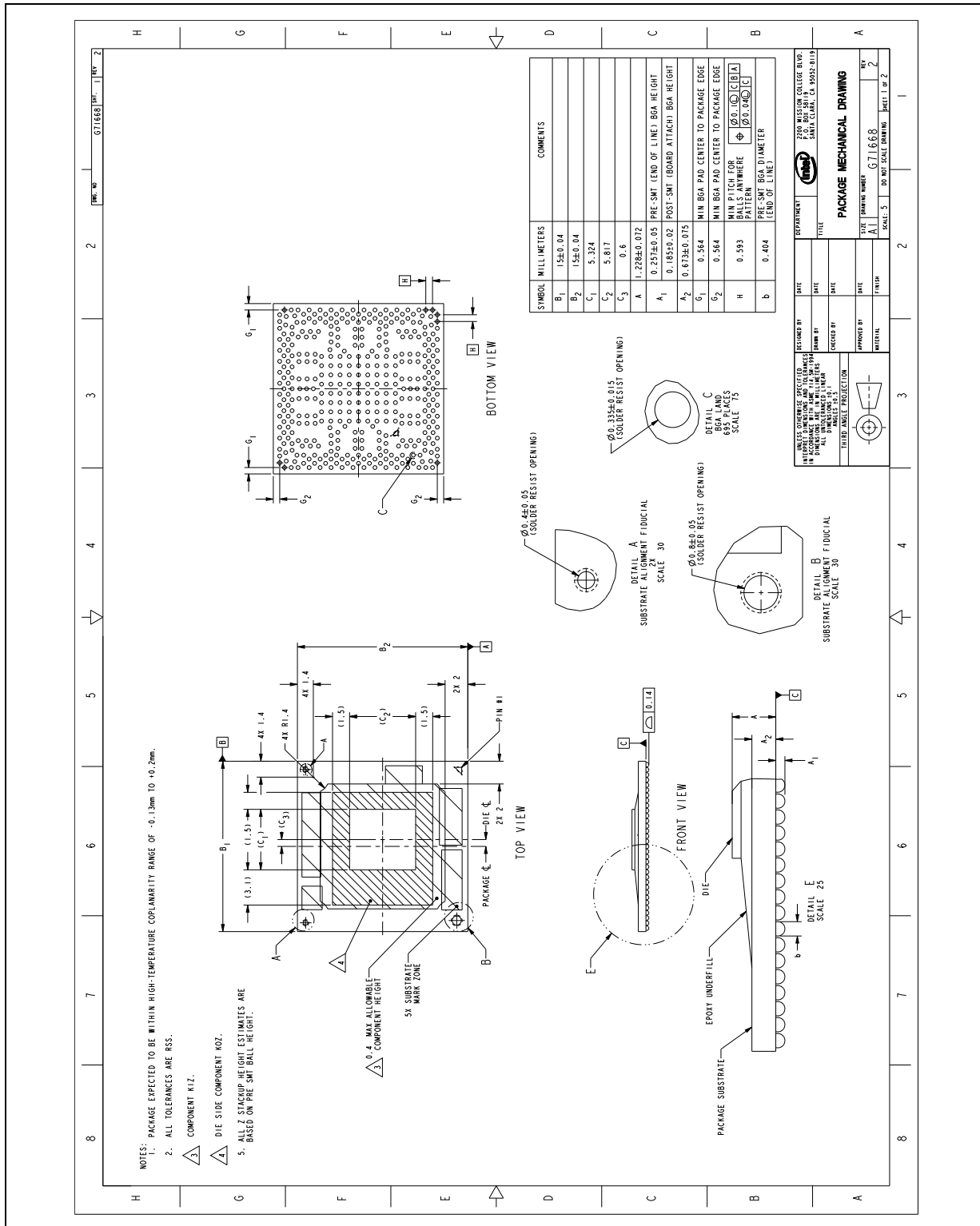
Intel provides thermal simulation models of the device and a thermal model user's guide to aid system designers in simulating, analyzing, and optimizing a thermal solution in an integrated system-level environment. The models are for use with commercially available Computation Fluid Dynamics (CFD) based thermal analysis tools FloTHERM* by Mentor Graphics and Icepak* by ANSYS.

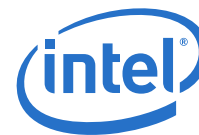
1.4 Package Information

The SoC utilizes a 15 x 15 mm Flip-Chip Ball Grid Array (FCBGA) package as shown in [Figure 1](#). The FCBGA package is a bare die package and is in direct contact with the thermal solution. Note that there are capacitors near the die. Although the die-side capacitors are slightly shorter than the silicon die, be careful to avoid contacting the capacitors with electrically conductive materials or a heatsink base. Consider using an insulating material between the capacitors and heatsink to prevent capacitor shorting.

The data provided in this section is for reference purposes only. Refer to *Intel® Quark™ SoC X1000 Datasheet* for up-to-date information. In the event of conflict, the device's datasheet supersedes data shown in these figures.

Figure 1. Mechanical Drawing





2.0 Thermal Specification

2.1 Thermal Design Power

The maximum allowed component temperature lists the Thermal Design Power (TDP) specifications. TDP is the recommended design point for the thermal solution power dissipation. TDP is based on running the worst-case, real-world applications and benchmarks at the maximum component temperature. TDP is not the absolute worst case power. It could, for example, be exceeded under a synthetic worst-case condition or under short power spikes. The thermal solution design must keep the component's maximum temperature within the specification while dissipating TDP.

Heat transfer through the FCBGA package and into the baseboard is limited. Since the cooling capacity without a thermal solution is also limited when the local ambient temperature is high, Intel recommends the use of a heatsink beyond a particular ambient temperature. This point changes based on the open PCB or enclosed environments.

2.2 Maximum Allowed Component Temperature

The SoC must maintain a maximum temperature at or below the value specified in [Table 3](#). See [Section 6.0, "Thermal Metrology" on page 18](#) for recommendations on temperature measurements using thermocouples to ensure the temperature is below the specification.

Table 3. SKU Definitions

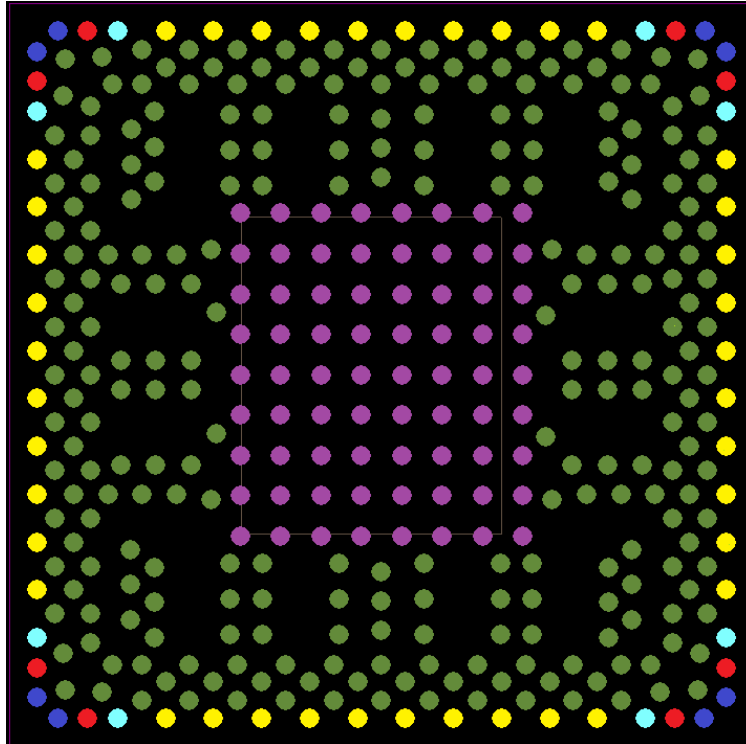
	SKU1 (Commercial)	SKU2 (Extended)
TDP (W)	2.2	1.9
T _{J-MAX} (°C)	110	
T _{CASE-MIN} (°C)	0	-40
T _{AMBIENT} (°C)	70	85

Note: Specifications presented in this table are preliminary and subject to change without notice.

3.0 Package Mechanical Specification

Due to Intel® Quark™ SoC X1000 design specifics, mechanical loading concerns must be assessed on a case-by-case basis. Please contact your local FAE for information regarding the maximum allowable static loading and package strain capability.

3.1 Land Pattern Guidance for Optimum Reliability Performance



Pad Color	Pad Description	Quantity
Blue	Pkg corner 14mil/SMD/CTF on 18mil metal pad (or flood Cu). Pins to be Redundant Pwr or Gnd.	8
Red	12mil/MD/CTF	8
Cyan	11mil/MD/CTF	8
Yellow	10x13mil/MD/CTF	40
Green	12mil/1WTMD/MD/CTF, wide trace = 10mil (SMD allowed as needed)	257
Purple	DS CTF 14mil/(1WTMD preferred)/SMD allowed as needed, (preferred wide trace = 10mil)	72
	Total	393

Note: I/O Trace = 4mil

Note: WTMD = Wide Trace Metal Defined = 10mil



Note: No 2WTMD or SMD pads allowed in Die Shadow.

4.0 Thermal Solution Requirements

4.1 Heatsink Design Considerations

To dissipate the heat generated by the SoC, three basic parameters should be considered.

1. **The area of the surface on which the heat transfer takes place.** Without any enhancements, this is the surface of the die. One method to improve thermal performance is to attach a heatsink to the die. A heatsink increases the effective heat transfer surface area by conducting heat out of the die and into the surrounding air through fins attached to the heatsink base.
2. **The conduction path from the heat source to the heatsink fins.** Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impact the thermal performance of the heatsink. In particular, the quality of the contact between the package die and the heatsink base has a higher impact on the overall thermal solution performance as the SoC cooling requirements become stricter. Thermal Interface Material (TIM) is used to fill the gap between the die and the bottom surface of the heatsink, and thereby improve the overall performance of the stack-up (die-TIM-heatsink). With extremely poor heatsink interface flatness or roughness, TIM may not adequately fill the gap. The TIM thermal performance depends on its thermal conductivity as well as the pressure applied to it.
3. **The heat transfer conditions on the surface on which heat transfer takes place.** Convective heat transfer occurs between the airflow and the surface exposed to the flow. It is characterized by the local ambient temperature of the air, TLA, and the local air velocity over the surface. The higher the air velocity over the surface and the cooler the air, the more efficient is the resulting cooling. The nature of the airflow can also enhance heat transfer via convection. Turbulent flow can provide improvement over laminar flow. In the case of a heatsink, the surface exposed to the flow includes in particular the fin faces and the heatsink base.

Active heatsinks typically incorporate a fan that helps manage the airflow through the heatsink. Passive heatsink solutions require in-depth knowledge of the airflow in the chassis. Typically, passive heatsinks see lower air speed. These heatsinks are therefore usually larger (and heavier) than active heatsinks due to the increase in the fin surface required to meet the required performance. As the heatsink fin density (the number of fins in a given cross-section) increases, the resistance to the airflow increases; it is more likely that the air travels around the heatsink instead of through it, unless air bypass is carefully managed. Using air-ducting techniques to manage the bypass area can be an effective method for controlling airflow through the heatsink.

4.2 Heatsink Size

The size of the heatsink is dictated by the height restrictions for installation in a system and by the space available on the motherboard and other considerations for component height and placement in the area potentially impacted by the heatsink. The height of the heatsink must comply with the requirements and recommendations published for the motherboard form factor of interest.



4.3 System-Level Thermal Solution Considerations

The heat generated by components within the chassis must be removed to provide an adequate operating environment for the processor and other components. Moving air through the chassis brings in air from the external ambient environment and removes the heat generated by the SoC and other components. The number, size, and relative position of the vents determine the chassis thermal performance, and the resulting ambient temperature around the processor.

The size and type (passive for the SoC) of the thermal solution and the amount of system airflow can be traded off against each other to meet specific system design constraints. Additional constraints are board layout, spacing, component placement, acoustic requirements, and structural considerations that limit the thermal solution size. For more information, see the appropriate form factor's thermal design suggestions.

To develop a reliable, cost-effective thermal solution, thermal characterization and simulation should be carried out at the system level, accounting for the thermal requirements of each component.

4.4 Characterizing the Thermal Solution Requirement

The idea of a thermal characterization parameter, Ψ (Greek letter Psi), is a convenient way to characterize the performance needed for the thermal solution and to compare thermal solutions in identical situations (i.e., heating source, local ambient conditions, etc.). The thermal characterization parameter is calculated using the total package power, whereas actual thermal resistance, Θ (theta), is calculated using the actual power dissipated between two points. Measuring the actual power dissipated into the heatsink is difficult, since some of the power is dissipated via heat transfer into the package and the board.

The junction-to-local ambient thermal characterization parameter (Ψ_{JA}) is used as a measure of the thermal performance of the overall thermal solution. The Ψ_{JA} is measured in units of °C/W and defined by the following equation:

Equation 1. $\Psi_{JA} = (T_J - T_{LA})/TDP$

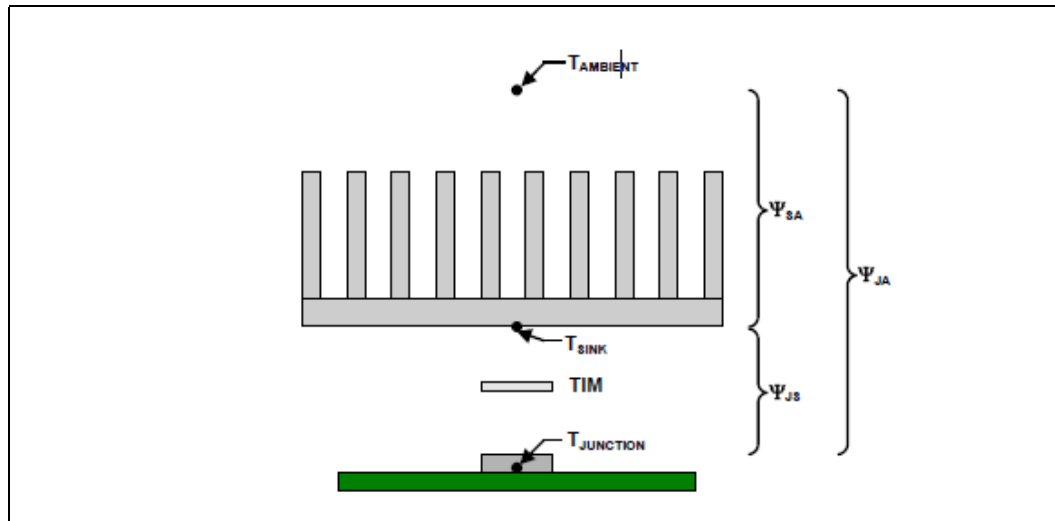
The junction-to-local ambient thermal characterization parameter, Ψ_{JA} , is comprised of Ψ_{JS} , the thermal interface material thermal characterization parameter, and of Ψ_{SA} , the sink-to-local ambient thermal characterization parameter. The Ψ_{JA} is defined by the following equation:

Equation 2. $\Psi_{JA} = \Psi_{JS} + \Psi_{SA}$

The Ψ_{JS} is strongly dependent on the thermal conductivity and thickness of the TIM between the heatsink and device package.

The Ψ_{SA} is a measure of the thermal characterization parameter from the bottom of the heatsink to the local ambient air. The Ψ_{SA} is dependent on the heatsink material, thermal conductivity, and geometry. The Ψ_{SA} is also strongly dependent on the air velocity through the fins of the heatsink. [Figure 2](#) illustrates the combination of the different thermal characterization parameters.

Figure 2. Model Temperatures



4.5 Thermal Performance Requirements

The following example demonstrates the required heatsink performance for a given set of boundary conditions. For this calculation assume:

- TDP = 2.7W
- Processor Local Ambient Temperature (T_{LA}) = 70 °C
- T_{J-MAX} = 110 °C

Using Equation 1, the junction-to-local ambient resistance can be calculated.

Equation 3. Maximum Allowable Resistance Calculation

$$\psi_{JA} = \frac{T_{J-MAX} - T_{LA}}{TDP} = \frac{110 - 70}{2.7} = 14.81^{\circ}\text{C/W}$$

If the assumption is a TIM impedance of 0.3 C/W (ψ_{JS}), the required heatsink performance (ψ_{SA}) can be calculated. The TIM impedance is provided by the manufacturer as pressure vs. impedance curves and can be used to select a proper TIM for a given application.

Equation 4. Required Heatsink Performance

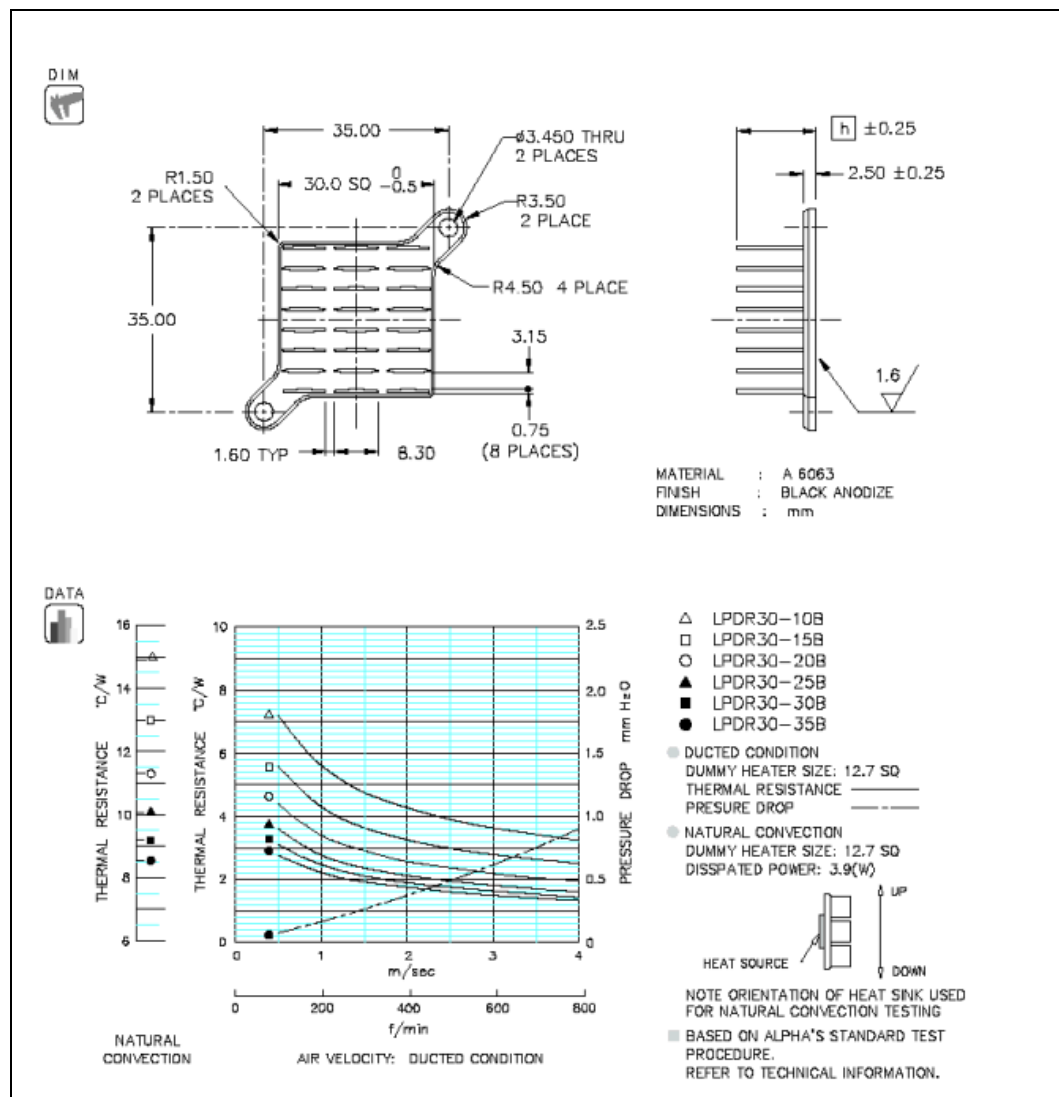
$$\psi_{SA} = \psi_{JA} - \psi_{JS} = 14.81 - 0.3 = 14.51^{\circ}\text{C/W}$$

It is evident from the above calculations that a reduction in the local ambient temperature can have a significant effect on the junction-to-ambient thermal resistance requirement. This effect can contribute to a more reasonable thermal solution including reduced cost, heatsink size, heatsink weight, or a lower system airflow rate.

5.0 Reference Heatsink

Figure 3 shows the reference heatsink form factor.

Figure 3. Reference Heatsink Form Factor

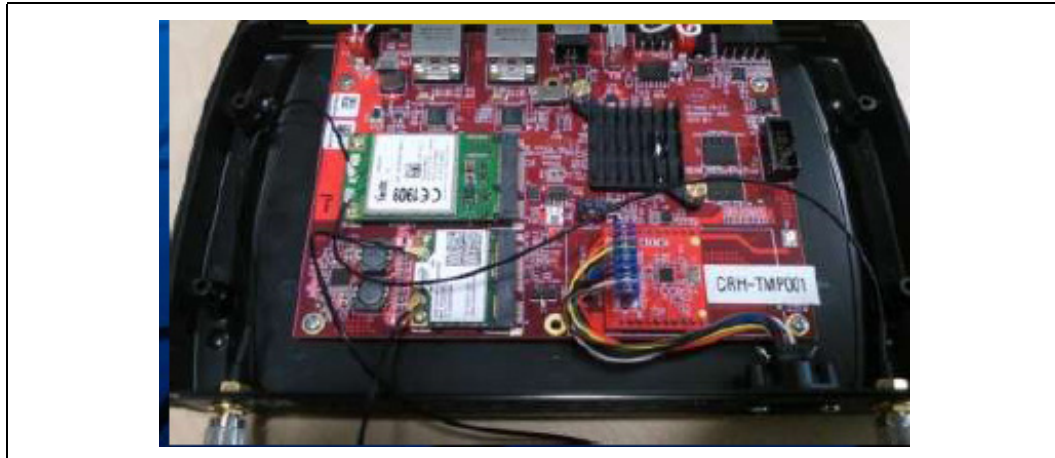


Note: The drawing is a property of Alpha Novatech*. Contact the vendor for more details.

5.1 Maximum Ambient Approximations

The T_{CASE} measurements were taken with the Intel® Quark™ SoC X1000 Industrial Reference Platform running a generic application stressing CPU, memory, I/O, WiFi, and Ethernet.

Figure 4. Intel® Quark™ SoC X1000 Industrial Reference Platform Design



The Reference Platform was run in four different configurations: horizontal and vertical, with and without a case. In all four test instances the heat sink was not used.

Table 4. Maximum Ambient Approximation

Orientation	Horizontal w/ Chassis	Vertical w/ Chassis	Horizontal w/o Chassis	Vertical w/o Chassis
T_{CASE} (°C)	85.2	78.1	70.0	62.8
$T_{AMBIENT}$ (°C)	22	22	22	22
Maximum Ambient (°C)	41.8	48.9	57.0	64.2

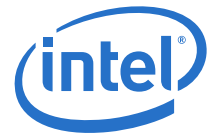
The test results can be used to approximate at which ambient temperature the Reference Platform can operate without a heat sink. As an example, the results of horizontal configuration with a chassis, the SoC T_{CASE} while running at 22 °C ambient is 85.2 °C. Using the T_{CASE} specification of 105 °C, the max ambient the board can run at in this particular configuration is 41.8 °C. Increasing the heat transfer from the SoC to the environment can increase the maximum ambient temperature at which the board can operate safely under the T_{J-MAX} specification (i.e., adding a Heat Sink). Similar approximations for all test conditions are listed in [Table 4](#).

Note: The maximum ambient calculations are made based on measurements taken on a single sample, at room temperature and does not take into account part-to-part variation. Results may vary with different boundary conditions (e.g., chassis venting, board layout, application workload, elevated ambient, etc.).

Note: As of the time of this publication, T_{CASE} estimates with a heatsink are not available.

5.2 Heatsink Orientation

The heatsink orientation for a vertically oriented board should be placed such that the fins are parallel to the direction of flow. For passive applications this means orienting the heatsink fins parallel with gravity.



The effect of heatsink orientation on a horizontally oriented board does not have significant impact on the efficacy of the thermal solution. Slight performance benefits may be seen if the fins are orientated perpendicular to the chassis vents. System modeling and testing need to be performed to ensure the T_{CASE} is maintained below the maximum allowable temperature specification defined in Table 4.

5.3 Thermal Interface Material (TIM) Thickness

The reference heatsink comes assembled with the TIM attached. The TIM performance can be requested from the supplier if choosing a third-party manufacturer.

5.4 Heatsink Installation

The reference solution shown in Figure 3 on page 15 comes fully assembled with TIM, push pins, springs, and heatsink from Alpha Novatech, Inc. The drawing can be used for board level KOZ's and mounting hole locations during board layout. To install the heatsink to the SoC package, simply push the pins into the through holes on the PCB surrounding the SoC package. The pins are flanged such that a clicking sound is heard once the pin is fully engaged.

5.5 Reference Heatsink Supplier

Alpha Novatech

<http://alphanovatech.com>

6.0 Thermal Metrology

6.1 T_{CASE} Temperature Measurements

6.1.1 Bare Die

For bare die applications, the T_{CASE} measurements can be taken by using epoxy to attach a thermocouple onto the center of the die. Smaller thermocouples will lead to more accurate temperature measurements.

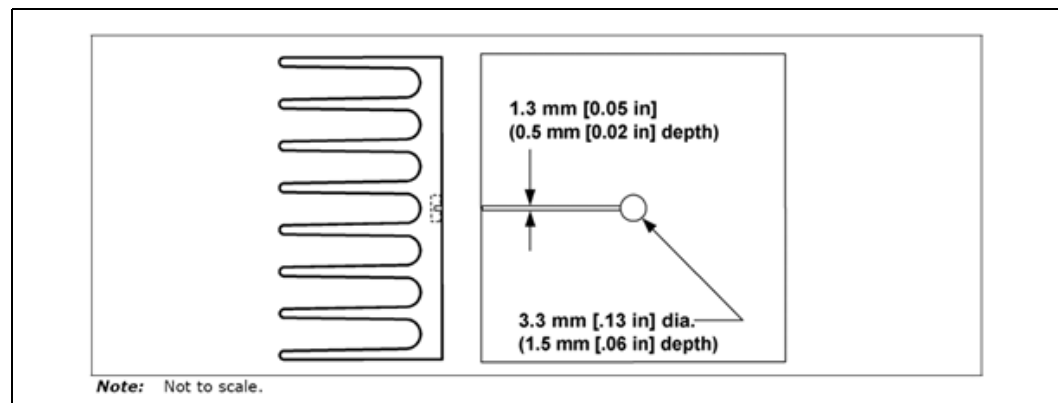
6.1.2 Passive Heatsink

For passive heatsink applications, Intel recommends attaching a thermocouple to the center of a grooved heatsink for temperature measurement (T_{SINK}). For more information on thermocouple attach methodologies contact your Intel FAE. Figure 5 is an example of a grooved heatsink for attaching a thermocouple for T_{SINK} measurements. The T_{SINK} along with the case-to-sink resistance (or TIM resistance), the ψ_{CS} allows for estimation of the T_{CASE} for a particular application.

Note: Intel advises against using a thermocouple to measure T_{CASE} with an ungrooved heatsink. The thermocouple bead/epoxy causes stress concentrations in the center of the die which could lead to die cracking.

Note: Information regarding the TIM resistance vs. pressure can be requested from the TIM manufacturer.

Figure 5. Reference Heatsink Groove for a Thermocouple





Sample calculation, assume:

- TDP = 2.7W
- $\psi_{CS} = 2 \text{ }^{\circ}\text{C/W}$
- $T_{SINK} = 95 \text{ }^{\circ}\text{C}$ (measured)

With the above parameters, the T_{CASE} of the SoC can be estimated:

Equation 5. Case-to-Sink (TIM) Resistance

$$\psi_{CS} = \frac{T_{CASE} - T_{SINK}}{TDP}$$

Using Equation 5:

$$T_{CASE} = \psi_{CS} \times TDP + T_{SINK} = 2.0 \times 2.7 + 95 = 100.4^{\circ}\text{C}$$

The calculation shows the impact of TIM performance on overall thermal solution efficacy.

