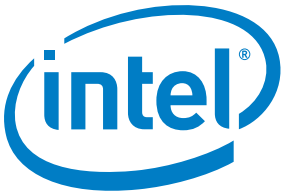


Intel® Quark SoC X1000 Platform: DDR3 Dual Rank Memory Down Board Layout Guide

White Paper

September 2014

Document Number: 331204-001

Contents

Figures

Tables

Revision History

Date	Revision	Description
September 2014	001	Initial release.

1 DDR3 Memory Overview

1.1 Introduction

This document covers the simulated guidelines required to design an Intel® Quark SoC X1000 platform with DDR3 Memory Down at 800 MT/s, on a 6 layers Type 3 PCB.

1.2 Supported Memory Configurations

Table 1. This Guideline Supports the Following Configurations

Parameter	DDR3
Topology	Memory Down Double-T Topology
Memory Capacity	512MB-2GB
Speed Supported	800 MT/s
Number of Channels Supported	1-Channel
Number of Ranks Supported	2
DRAM Device Densities Supported	1 Gb x 8 2 Gb x 8 4 Gb x 8
PCB Type	Type 3
PCB Layers	6 Layers

1.3 Reference Documents

Table 2. Reference Documents

Document	Doc # /Location
Intel® Quark SoC X1000™ SoC X1000 Platform Design Guide	520083/330258
Intel® Quark SoC X1000™ Platform- DDR3 Dual Rank Memory Down Schematic Guide Technical White Paper	331167-001 / EDC
Intel® Quark SoC X1000 SoC X1000 DDR3 Dual Rank Tree Topology Trace Length Calculator	551278

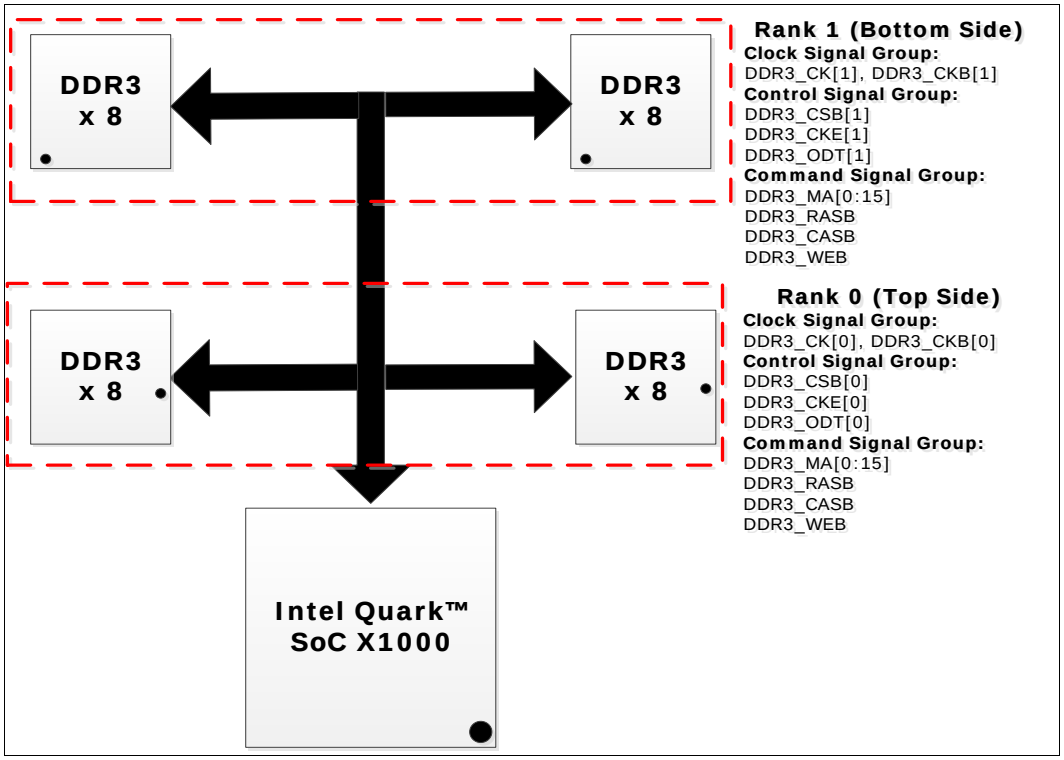
2 DDR3 Dual Rank Memory Down Design Overview and Stackup Consideration

This chapter provides detailed information on the Dual Rank Memory Down Design and Stackup Consideration.

2.1 Dual Rank Memory Down Block Diagram

Figure 1 shows the block diagram design for Dual Rank Memory Down.

Figure 1. Dual Rank Memory Down Block Diagram



The design guidelines provided in this chapter are based on this block diagram.

In this topology, the 2 SDRAM devices of the 2nd rank are placed on the bottom layer, under the 2 SDRAM devices of the 1st rank, which are placed on the top layer.

The data (DQ) and address signals (MA) are able to take advantage of the mirrored parts so that both top and bottom BGA balls can be directly connected through a via.

The rest of signals, however, are not completely mirrored between top and bottom devices.

Swapping the pins of either the top or bottom device allows the two BGA balls that share the same data and address signal to stay physically closer to each other, within same type of signals.

This enables short and balanced stubs, which ease routing and improve signal integrity.

Bit swapping is not necessary, but is recommended, to ease layout design.

Refer to the *Intel® Quark SoC X1000™ 2R Memory Down Schematic Guide Technical White Paper* (Intel EDC Document Number 331167-001, and Intel CDI Document Number 549743) for more detailed information on the bit swapping recommendation.

2.2 Memory Stackup Guidelines

The guidelines provided below define the 6-layers board. Individual byte lanes must be routed as a group on the same layer to minimize data to strobe skew.

Figure 2. Layer Stackup

			OPCM Stack-up Information								
Layer		Cu Weight	Proposed Thickness (mils)	Structure	Dk @ 2 GHz	Df @ 2 GHz	Ref.	Single End 50ohm +/- 10%		Diffential 85ohm +/- 10%	
								Target LW	Finished LW	Target LW/SP	Finished LW/SP
	Soldermask		0.50								
L1	Top	Hoz+Plating	1.80				L2	4.2	4.5	4.2/5.0	4.5/4.7
	Prepreg		2.70	1080	3.86	0.024					
L2	GND	1oz	1.20								
	Core		3	3mil core	4.08	0.024					
L3	Signal	1oz	1.20				L2,5	~4.0	4.0		4.0/5.2
	Prepreg		41.00	1080+2313 +28mil dummy core 1080+2313	3.86	0.024					
L4	Signal	1oz	1.20				L2,5	~4.0	4.0		4.0/5.2
	Core		3	3mil core	4.08	0.024					
L5	GND	1oz	1.20								
	Prepreg		2.70	1080	3.86	0.024					
L6	Bottom	Hoz+Plating	1.80				L5	4.2	4.5	4.2/5.0	4.5/4.7
	Soldermask		0.50								
Finished Thickness (mils)			61.8								

Notes:

- Material required: Isola* 370HR.
- Impedance tolerance required: +/-10%
- Board thickness is around 62 mils +/- 10%

3 Topology and Routing Guidelines

The DDR3 Memory Down Dual Rank topology was simulated using a 6-Layer Type 3 PCB, at 800MT/s speed. The topology diagrams and guidelines for each signal group are shown in the following sections. The below table shows a summary of memory channel signal groups routing recommendations.

Table 3. Memory Channel Signal Groups Routing

Board Routing Topology	Clock	Control	Command	Data	Data Strobe
Double-T	Differential Pair Double-T Topology	Differential Pair Double-T Topology	Differential Pair Double-T Topology	Point-to-Point Topology	Differential Pair Point-to-Point Topology
Reference Plane	GND referenced	GND referenced	GND referenced	GND referenced	GND referenced

Notes:

- Intel recommends all of the signals to have solid GND referencing planes on one side.
- Minimize the size of void if there are voids on reference planes.

3.1 Data (DQ/DQS) Signal Topology

Figure 3. Data Signal Routing Topology

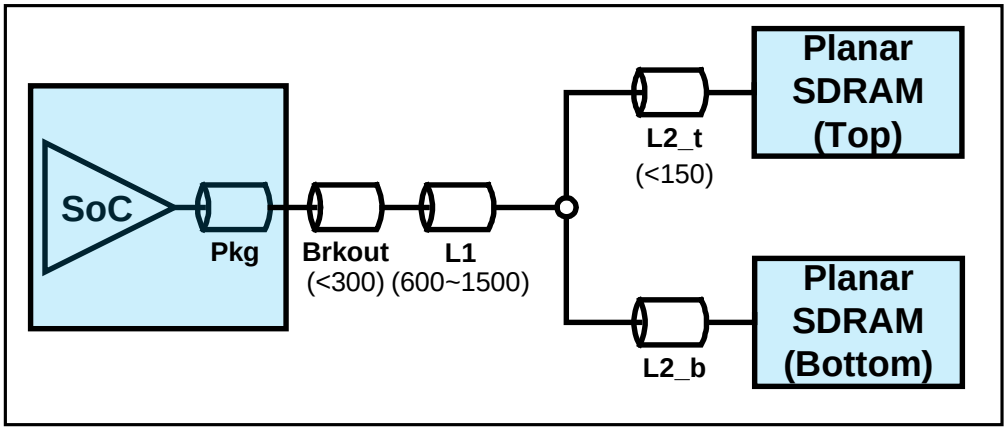


Table 4. Data Signal Layout Routing Constraints

Parameter	Definition
Signal Group	DDR3_DQ[0:15], DDR3_DQS/DQSB[0:1]
Topology	Point to Point
Reference Plane	GND Referenced
Layer Assignment	Microstrip (MS) or Stripline (SL)
Target Impedance (Z0:DQ; Zdiff: DQS)	DQ: 50 Ohm ± 10%, DQS: 85 Ohm ± 10%
DQS Routing Trace Width and Spacing within pair	MS: 4.5 mils trace width / 4.7 mils spacing SL: 4.0 mils trace width / 5.2 mils spacing
DQ Routing Trace Width and Spacing within same Byte Group	MS: 4.5 mils trace width / 12 mils spacing SL: 4.0 mils trace width / 10 mils spacing
DQS to DQ Spacing within same Byte Group	≥15 mils
Byte Group to Byte Group Spacing, Data to Other Signals Spacing	≥20 mils
Pkg	Refer to package length report
Brkout	< 300 mils
L1	600 - 1500 mils
L2_t, L2_b	< 150 mils, length match the L2_t and L2_b within 10 mils
L_brd (Brkout+L1+L2)	< 1950 mils (not including Pkg length)
DQS Length Matching within Pair	Including Pkg length, DQS and DQSB should be length matched within 5 mils
DQ to DQS Length Matching	Within the same byte group, the total length (Pkg+L_brd) of DQ from SoC die pad to SDRAM pin should be length matched to the total length (Pkg+L_brd) of DQS from SoC die pad to SDRAM pin within 10 mils.

3.2 Clock (CLK) Signal Topology

Figure 4. Clock Signal Routing Topology

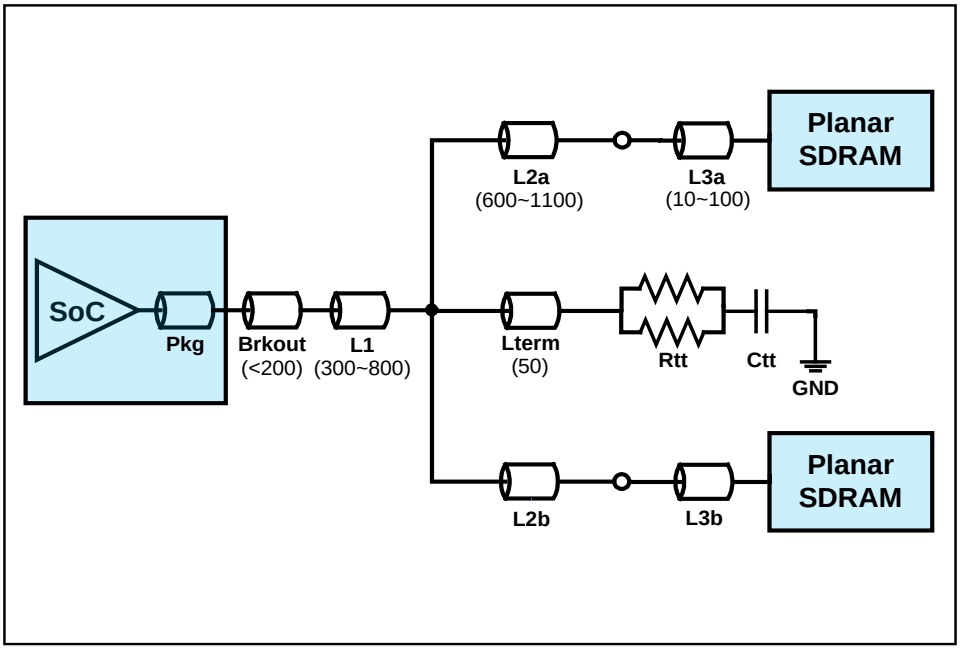


Table 5. Clock Signal Layout Routing Constraints

Parameter	Definition
Signal Group	DDR3_CK/CKB[0], DDR3_CK/CKB[1]
Topology	Double-T
Reference Plane	GND Referenced
Layer Assignment	Microstrip (MS) or Stripline (SL)
Target Impedance (Diff Z0)	85 Ohm ± 10%
CLK Routing Trace Width and Spacing within pair	MS: 4.5 mils trace width / 4.7 mils spacing SL: 4.0 mils trace width / 5.2 mils spacing
CLK Routing Spacing to other Signals	≥15 mils
Pkg	Refer to package length report
Brkout	< 200 mils
L1	300 - 800 mils
L2a, L2b	600 - 1100 mils
L3a, L3b	10 - 100 mils, length match L3a and L3b within 10 mils

Parameter	Definition
(L2a+L3a) to (L2b+L3b) Length Matching	Length match the two branches within 50 mils
L_brd (Brkout+L1+L2+L3)	< 2200 mils (not including Pkg length)
Lterm	50 mils (maximum)
CLK Length Matching within Pair	Including Pkg length, CK and CKB should be length matched within 5 mils
Rtt	30 Ohm
Ctt	0.1uF

3.3 Control (CTL) Signal Topology

Figure 5. Control Signal Routing Topology

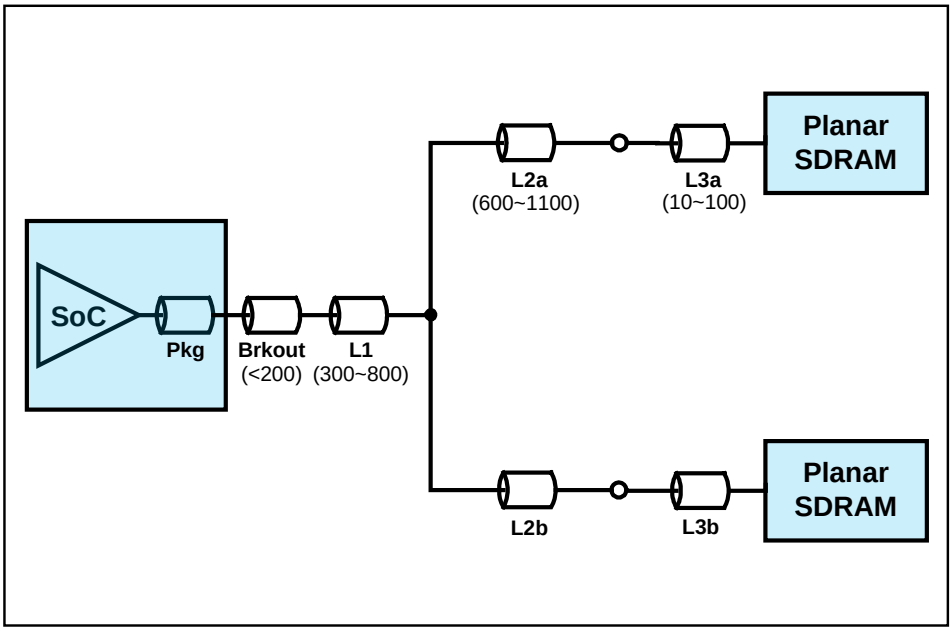


Table 6. Control Signal Layout Routing Constraints

Parameter	Definition
Signal Group	DDR3_CSB[0:1], DDR3_CKE[0:1], DDR3_ODT[0:1]
Topology	Double-T
Reference Plane	GND Referenced
Layer Assignment	Microstrip (MS) or Stripline (SL)
Target Impedance (Z0)	50 Ohm ± 10%
CTL Routing Trace Width and Spacing	MS: 4.5 mils trace width / 6 mils spacing SL: 4.0 mils trace width / 6 mils spacing
Pkg	Refer to package length report
Breakout	< 200 mils
L1	300 - 800 mils
L2a, L2b	600 - 1100 mils
L3a, L3b	10 - 100 mils, length match L3a and L3b within 50 mils
(L2a+L3a) to (L2b+L3b) Length Matching	Length match the two branches within 100 mils
L_brd (Brkout+L1+L2+L3)	< 2200 mils (not including Pkg length)
CTL to CLK Length Matching	The total length (Pkg+L_brd) of CTL from SoC die pad to SDRAM pin should be length matched to the total length (Pkg+L_brd) of CLK from SoC die pad to SDRAM pin within 200 mils

3.4 Command (CMD) Signal Topology

Figure 6. Command Signal Routing Topology

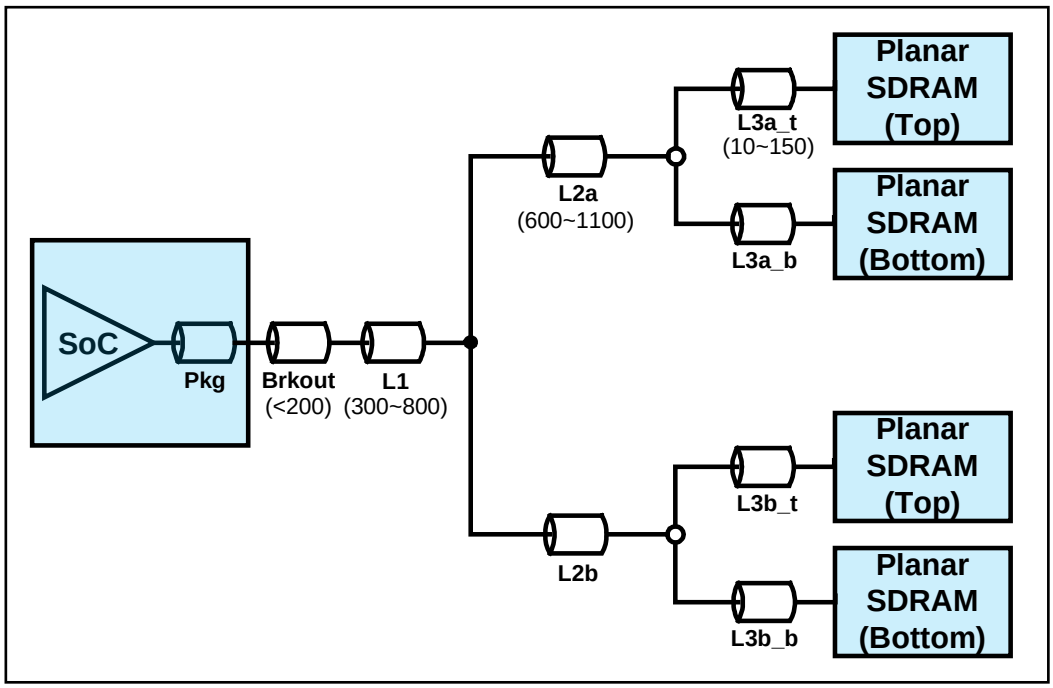


Table 7. Command Signal Layout Routing Constraints

Parameter	Definition
Signal Group	DDR3_MA[0:15], DDR3_CASB, DDR3_RASB, DDR3_WEB
Topology	Double-T
Reference Plane	GND Referenced
Layer Assignment	Microstrip (MS) or Stripline (SL)
Target Impedance (Z0)	50 Ohm ± 10%
CA Routing Trace Width and Spacing	MS: 4.5 mils trace width / 6 mils spacing SL: 4.0 mils trace width / 6 mils spacing
Pkg	Refer to package length report
Breakout	< 200 mils
L1	300 - 800 mils
L2a, L2b	600 - 1100 mils
L3a_t, L3a_b, L3b_t, L3b_b	10 - 150 mils
L3a_t to L3a_b and L3b_t to L3b_b Length Matching	Length match L3a_t to L3a_b within 50 mils, L3b_t to L3b_b within 50 mils
(L2a+L3a_t) to (L2b+L3b_t) and (L2a+L3a_b) to (L2b+L3b_b) Length Matching	Length match (L2a+L3a_t) to (L2b+L3b_t) within 100 mils, (L2a+L3a_b) to (L2b+L3b_b) within 100 mils
L_brd (Brkout+L1+L2+L3)	< 2250 mils (not including Pkg length)
CMD to CLK Length Matching	The total length (Pkg+L_brd) of CMD from SoC die pad to SDRAM pin should be length matched to the total length (Pkg+L_brd) of CLK from SoC die pad to SDRAM pin within 200 mils