[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR ESTABLISHING SYNCHRONIZATION WITH A SYNCHRONIZATION SIG-
NAL
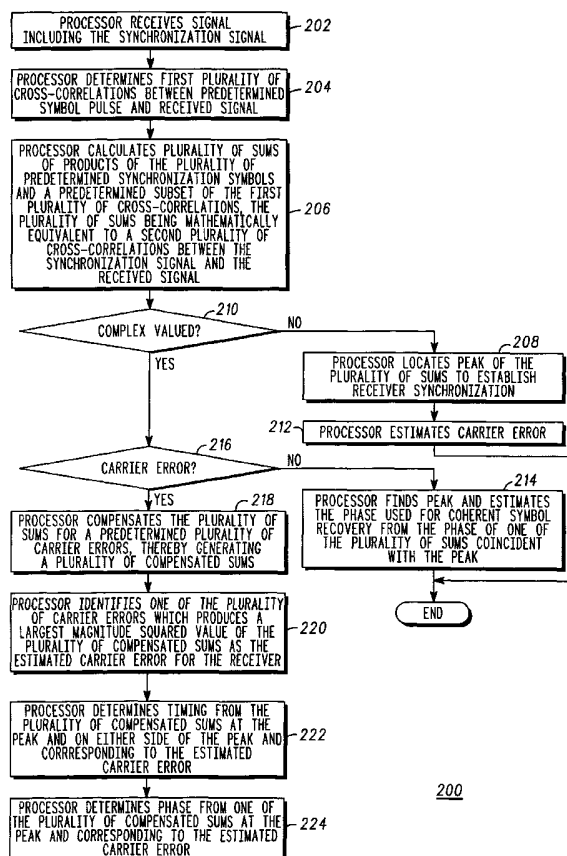
(57) Abstract: A synchronization signal includes a plurality of
predetermined synchronization symbols shaped by a predeter-
mined symbol pulse. A receiver (100) receives (202) a signal
including the synchronization signal, and a processor (106) de-
termines (204) a first plurality of cross-correlations between the
predetermined symbol pulse and the received signal. The proces-
sor calculates (206) a plurality of sums of products of the plurality
of predetermined synchronization symbols and a predetermined
subset of the first plurality of cross-correlations. The plurality
of sums are mathematically equivalent to a second plurality of
cross-correlations between the synchronization signal and the re-
ceived signal. The processor locates (208) a peak of the plurality
of sums to establish receiver synchronization.

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METHOD AND APPARATUS FOR ESTABLISHING SYNCHRONIZATION WITH A SYNCHRONIZATION SIGNAL

Related Application

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Application Docket No. PF02052NA, filed concurrently herewith by Chen et al., entitled " METHOD AND APPARATUS IN A WIRELESS COMMUNICATION SYSTEM FOR FACILITATING DETECTION OF, AND SYNCHRONIZATION WITH, A PREDETERMINED SYNCHRONIZATION SIGNAL" is a related application. Said

10   application is hereby incorporated herein by reference.

Field of the Invention

This invention relates in general to wireless communication systems, and more

15   specifically to a method and apparatus for establishing synchronization with a synchronization signal

Background of the Invention

20   A digital communication receiver must establish synchronization with a received signal before decoding the information in the received signal. One synchronization technique has been to perform a plurality of cross-correlations between a known synchronization pattern and the received signal, each cross-correlation calculated for a different portion of the received signal, until a point of highest correlation is detected.

25   Some systems, such as Bluetooth, utilize rather lengthy synchronization signals, causing a straightforward calculation of the cross-correlation values to require large amounts of memory and processing. Such a requirement is undesirable, especially in portable, battery-powered devices.

Thus, what is needed is an efficient method and apparatus for establishing

30   synchronization with a received signal. Preferably, the method and apparatus will not require large amounts of memory and processing.

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Brief Description of the Drawings

FIG. 1 is an electrical block diagram of an exemplary communication receiver in accordance with the present invention.

FIG. 2 is a first flow diagram depicting a synchronization technique used in the communication receiver in accordance with the present invention.

FIG. 3 is a second flow diagram depicting an efficient implementation for calculating the cross-correlation for a frequency shift keyed channel in accordance with the present invention.

FIG. 4 is a third flow diagram depicting an efficient implementation for calculating the cross-correlation for a phase shift keyed channel in accordance with the present invention.

FIG. 5 is a fourth flow diagram depicting an efficient implementation for calculating the cross-correlation for a phase shift keyed channel with carrier error in accordance with the present invention.

Detailed Description of the Drawings

Referring to FIG. 1, an electrical block diagram depicts an exemplary communication receiver 100 in accordance with the present invention comprising a conventional receiver front end 102 for receiving and demodulating a received signal. The receiver 100 further comprises a processor 106 coupled to the receiver front end 102 for processing the received signal to establish synchronization with a synchronization signal present in the received signal. The synchronization signal preferably comprises a plurality of predetermined synchronization symbols, each shaped by a predetermined symbol pulse. The receiver 100 also includes a memory 108 coupled to the processor 106 for storing operating variables and software for programming the processor. It will be appreciated that, alternatively, the processor 106 can be arranged such that the memory 108 is included as an integral component of the processor, and that the functions of the processor 106 and the memory 108 can also be manufactured as an application-specific integrated circuit (ASIC).

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The memory 108 comprises a communication control program 110 for programming the processor 106 to control the communications of the receiver 100 through well-known techniques. The memory 108 also includes a location 112 for storing the predetermined symbols and information describing the predetermined symbol pulse. In addition the

5   memory 108 has a location for storing received signal samples 114 being used for various computations. The memory 108 further comprises a symbol pulse-received signal cross-correlation program 116 for programming the processor 106 to determine a first plurality of cross-correlations between the predetermined symbol pulse and the received signal.

The memory 108 also includes a sums of products calculation program 118 for

10   programming the processor 106 to calculate a plurality of sums of products of the plurality of predetermined synchronization symbols and a predetermined subset of the first plurality of cross-correlations. The programs 116, 118 operate such that the plurality of sums are mathematically equivalent to a second plurality of cross-correlations between the synchronization signal and the received signal, but are advantageously much less

15   computationally intense and more memory efficient. In addition, the memory 108 includes a peak location program 120 for programming the processor 106 to locate a peak of the plurality of sums to establish receiver synchronization. The memory further comprises a phase estimation program 122 for programming the processor 106 to estimate the phase of a complex signal. The memory 108 also includes a carrier error compensation program

20   124 for programming the processor 106 to compensate the plurality of sums for a predetermined plurality of trial carrier errors, thereby generating a plurality of compensated sums. In addition, the memory 108 includes a carrier error estimation program 126 for programming the processor 106 to identify one of the plurality of trial carrier errors which produces a largest magnitude squared value of the plurality of

25   compensated sums as the estimated carrier error for the receiver 100. Operation of the receiver 100 in accordance with the present invention will be described further below.

FIG. 2 is a first flow diagram 200 depicting a general synchronization technique used in the communication receiver 100 in accordance with the present invention. The diagram 200 begins with the processor 106 receiving 202 a signal including the synchronization

30   signal. As the samples of the received signal arrive, the processor 106 determines 204 a first plurality of cross-correlations between the predetermined symbol pulse and the received signal. The processor 106 also calculates 206 a plurality of sums of products of

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the plurality of predetermined synchronization symbols and a predetermined subset of the first plurality of cross-correlations, the plurality of sums being mathematically equivalent to a second plurality of cross-correlations between the synchronization signal and the received signal. When at step 210 the particular embodiment of the present invention is for

5   a received signal and synchronization symbols which are not complex valued, the processor 106 locates 208 the peak of the plurality of sums to establish the receiver synchronization. The processor 106 then estimates the carrier error through well-known techniques, and the process ends.

       If, on the other hand, the embodiment is for a received signal and synchronization

10   symbols which are complex valued, at step 210 the flow moves to step 216, where the processor 106 checks 216 whether the particular embodiment also performs carrier error correction. If not, the processor 106 finds 214 the peak, preferably by locating the one of the plurality of sums having the largest magnitude squared value. The processor 106 then estimates the phase that will be used for coherent symbol recovery from the phase of one

15   of the plurality of sums coincident with the peak.

       If, on the other hand, at step 216 carrier error detection is to be performed, then the processor 106 compensates 218 the plurality of sums for a predetermined plurality of carrier errors, thereby generating a plurality of compensated sums. The processor 106 then identifies 220 one of the plurality of carrier errors which produces a largest magnitude

20   squared value of the plurality of compensated sums as the estimated carrier error for the receiver. The processor 106 determines 222 the timing of the received signal from the plurality of compensated sums at the peak and on either side of the peak and corresponding to the estimated carrier error, preferably by applying a well-known second-order polynomial fitting technique. The processor 106 then determines 224 the phase of the

25   received signal from one of the plurality of compensated sums at the peak and corresponding to the estimated carrier error, preferably as the arctangent of the quadrature portion of the one of the compensated sums divided by the real portion.

       The following describes the synchronization process in greater detail, emphasizing efficient techniques for performing the calculations. We will begin with the efficient

30   calculation of the cross-correlation of the received signal $x(n)$ and the predetermined synchronization signal $s(m)$.

5

$$R_{SX}(n) = \sum_{m=1}^{N} x(m+n)s(m)$$

In one embodiment, the symbol rate is 1 million symbols per second. The synchronization signal includes 64 FSK symbols, which are real valued

$$\alpha_k = \pm 1$$

and there are 4 samples per symbol. In the cross-correlation equation above, N is then 256. A straightforward calculation of the cross-correlation would thus require 256x2=512 memory locations, and further would require 256 multiplications and 256 additions *per 0.25 microsecond*. This is equivalent to about 1024 million instructions per second (MIPS).

As received, each symbol pulse stretches over about 12 samples. The synchronization signal can be represented as

$$s(m) = \sum_{k=1}^{64} \alpha_k g_s(m-4k)$$

where g_s represents the symbol pulse. Substituting the right side of the above equation into the cross-correlation equation and simplifying the equation with the intent of reducing the memory and processing requirements produces the following transformation.

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$$R_{SX}(n) = \sum_m x(m+n)s(m)$$

$$= \sum_m x(m+n) \sum_{k=1}^{64} \alpha_k g_s(m-4k) = \sum_{k=1}^{64} \alpha_k R_{GX}(n+4k)$$

where

$$R_{GX}(n) = \sum_{m=-6}^{6} g_s(m)x(n+m) = \sum_{m=1}^{6} g_s(m)[x(n+m) + x(n-m)]$$

This transformation advantageously reduces the memory requirements to 253+12=265 locations, and substantially reduces the calculations to 6 multiplications and 6+5+64=75 additions—about a 95% saving in calculations. In addition, the complexity of the 6 multiplications is equivalent to the complexity of 3 of the multiplications of the straightforward approach, because the $g_s(m)$ values are known and can be built into the multipliers. Also, the generation of $s(m)$, $m = 1, 2, ..., 256$ from α_k, $k = 1, 2, ..., 64$ is avoided. The significant reduction in calculations advantageously translates directly into power reduction, which can be especially important in a portable wireless transceiver, for example.

FIG. 3 is a second flow diagram 300 depicting an efficient implementation for calculating the cross-correlation for a frequency shift keyed channel in accordance with the present invention. A first shift register 302 receives each sample of the received signal $x(n)$. The twelve positions of the first shift register 102 are tapped and the values therein combined with the six values of $g_s(n)$ in six multipliers and 11 adders to generate $R_{GX}(n)$. A second shift register 304 receives each sample of $R_{GX}(n)$ and is tapped at every fourth position to generate $R_{SX}(n)$. Note that, because the α_k values are ± 1, the 64 multipliers associated therewith are realized quite simply, as they only change the sign of the value received from the shift register 604.

When the received signal and the synchronization signal are complex valued, as in PSK modulation, the synchronization can be accomplished as follows. The synchronization signal can be expressed as

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$$s(m) = \sum_{k=1}^{64} \alpha_k g_s(m-4k)$$

where the synchronization symbols are

$$\alpha_k = e^{j\varphi_k}$$

5   and $g_s(m)$ is the real-valued symbol pulse. The received signal is

$$x(n) = e^{j\phi} s(m) + N(n)$$

where ϕ is a random phase offset between the transmitter and the receiver, uniformly

distributed over $[-\pi, \pi]$, and $N(n)$ is noise (which averages out of the cross-correlation and

10   can be ignored). As in the real-valued case described above, the cross-correlation of the

received signal and the predetermined synchronization signal is used

$$R_{SX}(n) = \sum_{m=1}^{N} x(m+n)\bar{s}(m)$$

where $\bar{s}$ is the complex conjugate of the sync signal. The peak of the magnitude squared

value of the cross-correlation $|R_{SX}(n)|^2$ will provide the timing of the channel. The phase

15   ϕ of $R_{SX}(n)$ at the peak will provide the phase estimation, which can be used for coherent

symbol recovery.

        The efficient calculation of the cross-correlation is similar to that of the real-valued

case.

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$$R_{SX}(n) = \sum_{m=1}^{M} x(m+n)\bar{s}(m)$$

$$= \sum_{m=1}^{M} x(m+n) \sum_{k=1}^{K} \bar{\alpha}_k g_s(m-4k) = \sum_{k=1}^{K} \bar{\alpha}_k R_{GX}(n+4k)$$

where $\bar{\alpha}_k$ is the complex conjugate of the sync symbol, and where

$$R_{GX}(n) = \sum_{m=-l_g}^{l_g} g_s(m)x(n+m) = \sum_{m=1}^{l_g} g_s(m)[x(n+m)+x(n-m)]$$

5   However, the real and quadrature portions of $R_{GX}(n)$ are calculated separately.

$$R_{GX}(n) =$$

$$\sum_{m=1}^{l_g} g_s(m)[x_I(n+m)+x_I(n-m)] + j\sum_{m=1}^{l_s} g_s(m)[x_Q(n+m)+x_Q(n-m)]$$

Thus

$$R_{SX}(n) = \sum_{k=1}^{K} \bar{\alpha}_k[R_{GXI}(n+4k)+jR_{GXQ}(n+4k)]$$

10

where

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$$R_{GXI}(n) = \sum_{m=1}^{l_g} g_s(m)[x_I(n+m) + x_I(n-m)]$$

and

$$R_{GXQ}(n) = \sum_{m=1}^{l_g} g_s(m)[x_Q(n+m) + x_Q(n-m)]$$

FIG. 4 is a third flow diagram 400 depicting an efficient implementation for calculating the cross-correlation for a complex-valued phase shift keyed channel in accordance with the present invention. The diagram 400 is similar to the diagram 300, the

5   essential differences being the elements 402, 404, and 406. Element 402 calculates the magnitude squared value of the cross-correlation. Element 404 finds the peak through well-known techniques, and determines the timing therefrom. Element 406 estimates the phase.

When carrier error is present in the complex-valued case, the above calculations

10   must compensate for the carrier error. As before, the cross-correlation of the received signal with the predetermined synchronization signal is derived from a plurality of cross-correlations of the received signal with the predetermined symbol pulse. Thus, for each sample index *n* the cross-correlation of the received signal with the predetermined symbol pulse is needed.

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$$R_{GX}(n) = \sum_{m=-l_g}^{l_g} x(m+n)g_s(m)$$

This is calculated efficiently exactly as before for the complex-valued case.

In deriving the cross-correlation of the received signal with the predetermined synchronization signal, however, the effect of the carrier error must be taken into

20   consideration.

10

$$R_{SX}(\omega_l, n) \approx \sum_{k=1}^{K} \bar{\alpha}_k e^{-j\omega_l T_s(k-1)} R_{GX}(n + kT_S)$$

The above equation is modified because

$$R_{GX}(\omega_l, n + kT_S) = e^{-j\omega_l T_s(k-1)} R_{GX}(n + kT_S)$$

is to remove the carrier error effects in the symbol correlation

$$R_{GX}(n + kT_S)$$

Since we do not know in advance what the carrier error is, we will use a plurality of trial values ω_l, where ω_l is in the search window $\omega_l = -\omega_{max}, ..., \omega_{max}$ with N_ω trials. This requires recursive calculation for

$$e^{-j\omega_l T_s k} = \{e^{-j\omega_l T_s(k-1)}\} e^{-j\omega_l T_s} \quad ,$$

$$k = 1, 2, ... N/T_S, \text{ and } \omega_l = -\omega_{max}, ..., \omega_{max}$$

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Also required are N_ω correlations

$$R_{SX}(\omega_l, n) = \sum_{k=1}^{K} \bar{\alpha}_k R_{GX}(\omega_l, n + kT_S),$$

each requiring K complex multiplications. Peak metrics and carrier-error estimates are determined for each sample received

$$P = max_{\omega_n}|R_{SX}(\omega_l, n)|^2, \text{ and } \omega_{max}(n) = \arg max_{\omega_n}|R_{SX}(\omega_l, n)|^2$$

The three most recently calculated peak metrics and carrier-error estimates, as well as the three most recently calculated cross-correlations at the corresponding carrier-error estimates are saved in three shift registers.

$$P \to P(1) \to P(2) \to P(3) \text{ and } \omega_{max} \to \omega(1) \to \omega(2) \to \omega(3)$$
$$R_{SX}(\omega_{max}, n) \to R(1) \to R(2) \to R(3)$$

A peak is detected if $P(2) \geq P(3)$ **and** $P(2) > P(1)$

The timing estimate is preferably calculated from a second-order interpolation from

$$\{P(3), P(2), P(1)\}$$

The carrier error estimate is equal to $\omega(2)$. The phase is calculated from the real and quadrature parts of the cross-correlation.

$$\hat{\phi} = atan\frac{R_Q(2)}{R_I(2)}$$

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FIG. 5 is a fourth flow diagram 500 depicting an efficient implementation for calculating the cross-correlation for a phase shift keyed channel with carrier error in accordance with the present invention. The diagram 500 is similar to the diagram 300, the essential differences being the elements 502 through 510. The complex multipliers 502

5   compensate for the carrier error. The peak metric calculator 504 calculates the magnitude squared value of the cross correlation for each sample interval and each carrier error trial value. The carrier-error estimator 506 determines the carrier estimate at the correlation peak, while the timing estimator 508 determines the timing at that carrier error estimate. The phase estimator 510 estimates the phase at that timing and carrier error estimate.

10   It should be clear from the preceding disclosure that the present invention provides a method and apparatus for establishing synchronization with a received signal. Advantageously, the method and apparatus does not require large amounts of memory and processing and it performs efficiently with both real-valued and complex signals.

Many modifications and variations of the present invention are possible in light of

15   the above teachings. For example, although specific synchronization signal sizes, symbol rates, samples per symbol, and samples per symbol pulse were given in the example embodiments presented herein above, one of ordinary skill in the art will readily be able to envision modifications to these and other parameters without departing from the scope of the present invention. Thus, it is to be understood that, within the scope of the appended

20   claims, the invention can be practiced other than as specifically described herein above.

What is claimed is:

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CLAIMS

1. A method in a communication receiver for establishing synchronization with a
synchronization signal comprising a plurality of predetermined synchronization symbols,
5   each shaped by a predetermined symbol pulse, the method comprising the steps of:

receiving a signal including the synchronization signal;

determining a first plurality of cross-correlations between the predetermined
symbol pulse and the received signal;

calculating a plurality of sums of products of the plurality of predetermined
10   synchronization symbols and a predetermined subset of the first plurality of cross-
correlations, said plurality of sums being mathematically equivalent to a second plurality
of cross-correlations between the synchronization signal and the received signal; and

locating a peak of said plurality of sums to establish receiver
synchronization.

15

2. The method of claim 1,

wherein the received signal and the predetermined synchronization symbols
are complex valued, and

wherein the determining step comprises the step of determining the first
20   plurality of cross-correlations separately for real and quadrature portions of the received
signal.

3. The method of claim 1,

wherein the received signal and the predetermined synchronization symbols
25   are complex valued, and

wherein the calculating step comprises the step of calculating said plurality
of sums from products of complex conjugates of the plurality of predetermined
synchronization symbols and a predetermined subset of the first plurality of cross-
correlations.

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4.   The method of claim 1,

        wherein the received signal and the predetermined synchronization symbols
are complex valued, and

        wherein the locating step comprises the step of locating the peak from a

5   magnitude squared value of said plurality of sums.

5.   The method of claim 1,

        wherein the received signal and the predetermined synchronization symbols
are complex valued, and

10   wherein the method further comprises the step of estimating a phase used
for coherent symbol recovery from the phase of one of said plurality of sums coincident
with the peak.

6.   The method of claim 1,

15   wherein the received signal and the predetermined synchronization symbols
are complex valued, and a carrier error exists between the received signal and the
communication receiver,

        wherein the calculating step comprises the step of compensating said
plurality of sums for a predetermined plurality of carrier errors, thereby generating a

20   plurality of compensated sums, and

        identifying one of the predetermined plurality of carrier errors which
produces a largest magnitude squared value of said plurality of compensated sums as an
estimated carrier error for the receiver.

25   7.   The method of claim 6, further comprising the step of

        determining timing from said plurality of compensated sums at the peak and
on either side of the peak and corresponding to the estimated carrier error.

8.   The method of claim 6, further comprising the step of

30   determining phase from one of said plurality of compensated sums at the
peak and corresponding to the estimated carrier error.

15

9.   A communication receiver for establishing synchronization with a synchronization signal comprising a plurality of predetermined synchronization symbols, each shaped by a predetermined symbol pulse, the communication receiver comprising:

a receiver front end for receiving a signal including the synchronization

5   signal; and

a processor coupled to the receiver front end for processing the received signal, wherein the processor is programmed to:

determine a first plurality of cross-correlations between the predetermined symbol pulse and the received signal;

10   calculate a plurality of sums of products of the plurality of predetermined synchronization symbols and a predetermined subset of the first plurality of cross-correlations, said plurality of sums being mathematically equivalent to a second plurality of cross-correlations between the synchronization signal and the received signal; and

locate a peak of said plurality of sums to establish receiver synchronization.

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10.   The communication receiver of claim 9,

wherein the received signal and the predetermined synchronization symbols are complex valued, and

wherein the processor is further programmed to determine the first plurality

20   of cross-correlations separately for real and quadrature portions of the received signal.

11.   The communication receiver of claim 9,

wherein the received signal and the predetermined synchronization symbols are complex valued, and

25   wherein the processor is further programmed to calculate said plurality of sums from products of complex conjugates of the plurality of predetermined synchronization symbols and a predetermined subset of the first plurality of cross-correlations.

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12. The communication receiver of claim 9,

wherein the received signal and the predetermined synchronization symbols are complex valued, and

wherein the processor is further programmed to locate the peak from a

5   magnitude squared value of said plurality of sums.

13. The communication receiver of claim 9,

wherein the received signal and the predetermined synchronization symbols are complex valued, and

10   wherein the processor is further programmed to estimate a phase used for coherent symbol recovery from the phase of one of said plurality of sums coincident with the peak.

14. The communication receiver of claim 9,

15   wherein the received signal and the predetermined synchronization symbols are complex valued, and a carrier error exists between the received signal and the communication receiver,

wherein the processor is further programmed to:

compensate said plurality of sums for a predetermined plurality of

20   carrier errors, thereby generating a plurality of compensated sums, and

identify one of the predetermined plurality of carrier errors which produces a largest magnitude squared value of said plurality of compensated sums as an estimated carrier error for the receiver.

25   15. The communication receiver of claim 14, wherein the processor is further programmed to

determine timing from said plurality of compensated sums at the peak and on either side of the peak and corresponding to the estimated carrier error.

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16. The communication receiver of claim 14, wherein the processor is further programmed to

determine phase from one of said plurality of compensated sums at the peak and corresponding to the estimated carrier error.

5

17. An apparatus for use with a receiver front end that receives a signal including a predetermined synchronization signal comprising a plurality of predetermined synchronization symbols, each shaped by a predetermined symbol pulse, the apparatus for establishing synchronization with the received signal, the apparatus comprising:

10   a processor for processing the received signal, wherein the processor is programmed to:

determine a first plurality of cross-correlations between the predetermined symbol pulse and the received signal;

calculate a plurality of sums of products of the plurality of

15 predetermined synchronization symbols and a predetermined subset of the first plurality of cross-correlations, said plurality of sums being mathematically equivalent to a second plurality of cross-correlations between the synchronization signal and the received signal; and

locate a peak of said plurality of sums to establish receiver

20 synchronization.

18. The apparatus of claim 17,

wherein the received signal and the predetermined synchronization symbols are complex valued, and

25   wherein the processor is further programmed to determine the first plurality of cross-correlations separately for real and quadrature portions of the received signal.
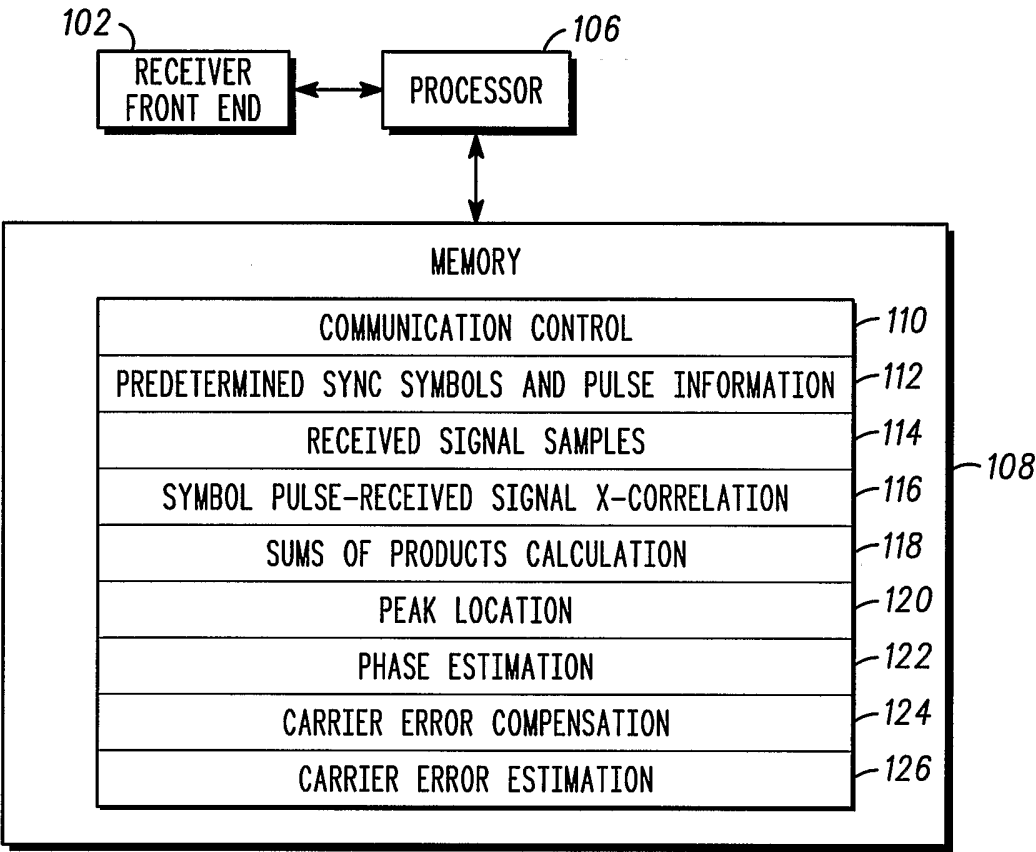
18

19. The apparatus of claim 17,

      wherein the received signal and the predetermined synchronization symbols are complex valued, and

      wherein the processor is further programmed to calculate said plurality of sums from products of complex conjugates of the plurality of predetermined synchronization symbols and a predetermined subset of the first plurality of cross-correlations.

20. The apparatus of claim 17,

      wherein the received signal and the predetermined synchronization symbols are complex valued, and

      wherein the processor is further programmed to locate the peak from a magnitude squared value of said plurality of sums.

21. The apparatus of claim 17,

      wherein the received signal and the predetermined synchronization symbols are complex valued, and

      wherein the processor is further programmed to estimate a phase used for coherent symbol recovery from the phase of one of said plurality of sums coincident with the peak.

22. The apparatus of claim 17,

      wherein the received signal and the predetermined synchronization symbols are complex valued, and a carrier error exists between the received signal and the receiver front end,

      wherein the processor is further programmed to:

            compensate said plurality of sums for a predetermined plurality of carrier errors, thereby generating a plurality of compensated sums, and

            identify one of the predetermined plurality of carrier errors which produces a largest magnitude squared value of said plurality of compensated sums as an estimated carrier error for the receiver.

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23. The apparatus of claim 22, wherein the processor is further programmed to
determine timing from said plurality of compensated sums at the peak and
on either side of the peak and corresponding to the estimated carrier error.

5   24. The apparatus of claim 22, wherein the processor is further programmed to
determine phase from one of said plurality of compensated sums at the peak
and corresponding to the estimated carrier error.

102 — RECEIVER FRONT END

106 — PROCESSOR

MEMORY

COMMUNICATION CONTROL	110
PREDETERMINED SYNC SYMBOLS AND PULSE INFORMATION	112
RECEIVED SIGNAL SAMPLES	114
SYMBOL PULSE-RECEIVED SIGNAL X-CORRELATION	116
SUMS OF PRODUCTS CALCULATION	118
PEAK LOCATION	120
PHASE ESTIMATION	122
CARRIER ERROR COMPENSATION	124
CARRIER ERROR ESTIMATION	126

108

100

FIG. 1

PROCESSOR RECEIVES SIGNAL
INCLUDING THE SYNCHRONIZATION SIGNAL — 202

PROCESSOR DETERMINES FIRST PLURALITY OF
CROSS-CORRELATIONS BETWEEN PREDETERMINED — 204
SYMBOL PULSE AND RECEIVED SIGNAL

PROCESSOR CALCULATES PLURALITY OF SUMS
OF PRODUCTS OF THE PLURALITY OF
PREDETERMINED SYNCHRONIZATION SYMBOLS
AND A PREDETERMINED SUBSET OF THE FIRST
PLURALITY OF CROSS-CORRELATIONS, THE — 206
PLURALITY OF SUMS BEING MATHEMATICALLY
EQUIVALENT TO A SECOND PLURALITY OF
CROSS-CORRELATIONS BETWEEN THE
SYNCHRONIZATION SIGNAL AND THE
RECEIVED SIGNAL

COMPLEX VALUED? — 210
                                   NO

YES

PROCESSOR LOCATES PEAK OF THE
PLURALITY OF SUMS TO ESTABLISH — 208
RECEIVER SYNCHRONIZATION

212 — PROCESSOR ESTIMATES CARRIER ERROR

CARRIER ERROR? — 216
                                   NO

YES — 218

PROCESSOR COMPENSATES THE PLURALITY OF
SUMS FOR A PREDETERMINED PLURALITY OF
CARRIER ERRORS, THEREBY GENERATING
A PLURALITY OF COMPENSATED SUMS

PROCESSOR FINDS PEAK AND ESTIMATES
THE PHASE USED FOR COHERENT SYMBOL — 214
RECOVERY FROM THE PHASE OF ONE OF
THE PLURALITY OF SUMS COINCIDENT
WITH THE PEAK

PROCESSOR IDENTIFIES ONE OF THE PLURALITY
OF CARRIER ERRORS WHICH PRODUCES A
LARGEST MAGNITUDE SQUARED VALUE OF THE — 220
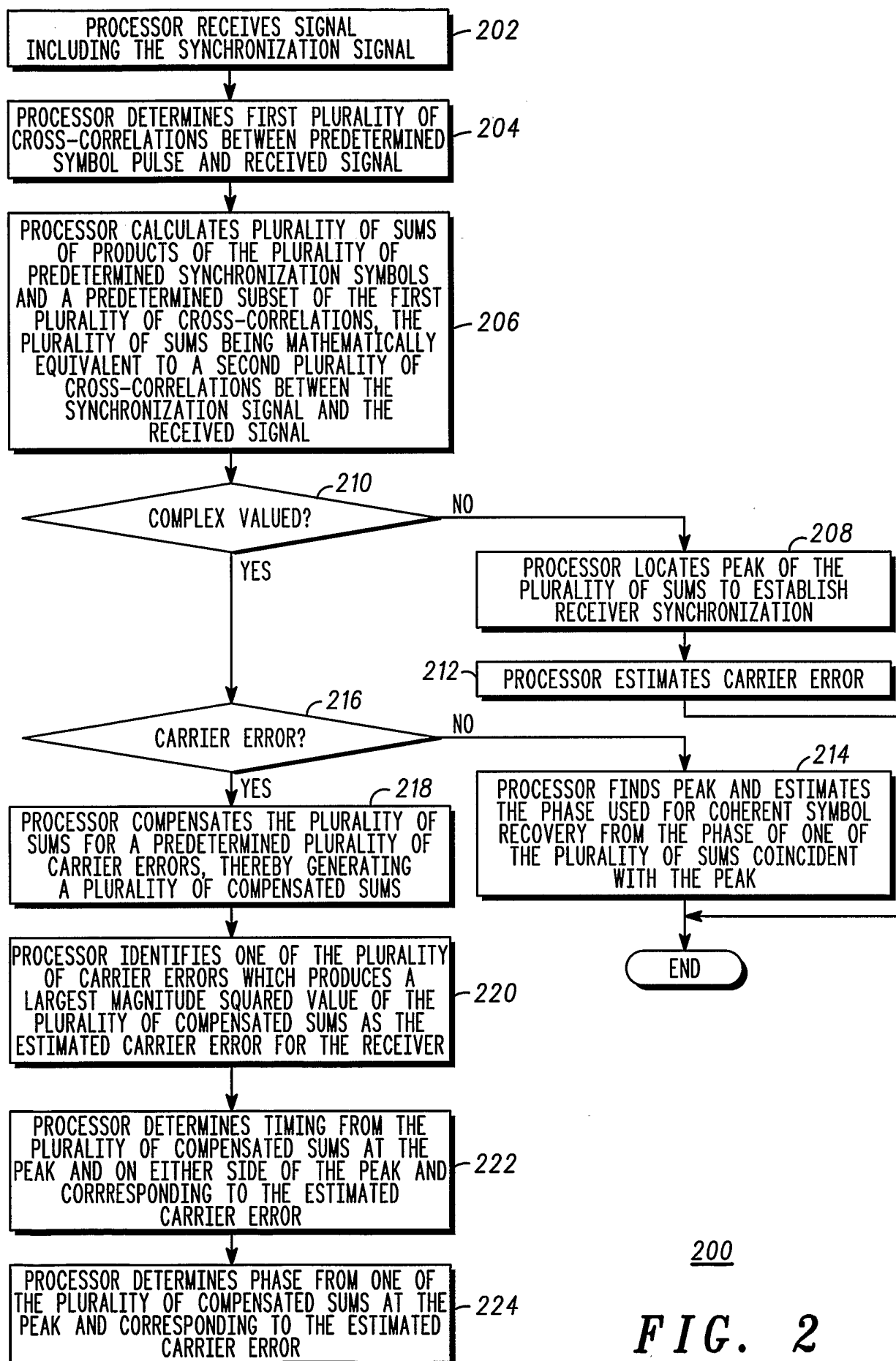PLURALITY OF COMPENSATED SUMS AS THE
ESTIMATED CARRIER ERROR FOR THE RECEIVER

END

PROCESSOR DETERMINES TIMING FROM THE
PLURALITY OF COMPENSATED SUMS AT THE
PEAK AND ON EITHER SIDE OF THE PEAK AND — 222
CORRRESPONDING TO THE ESTIMATED
CARRIER ERROR

200

PROCESSOR DETERMINES PHASE FROM ONE OF
THE PLURALITY OF COMPENSATED SUMS AT THE — 224
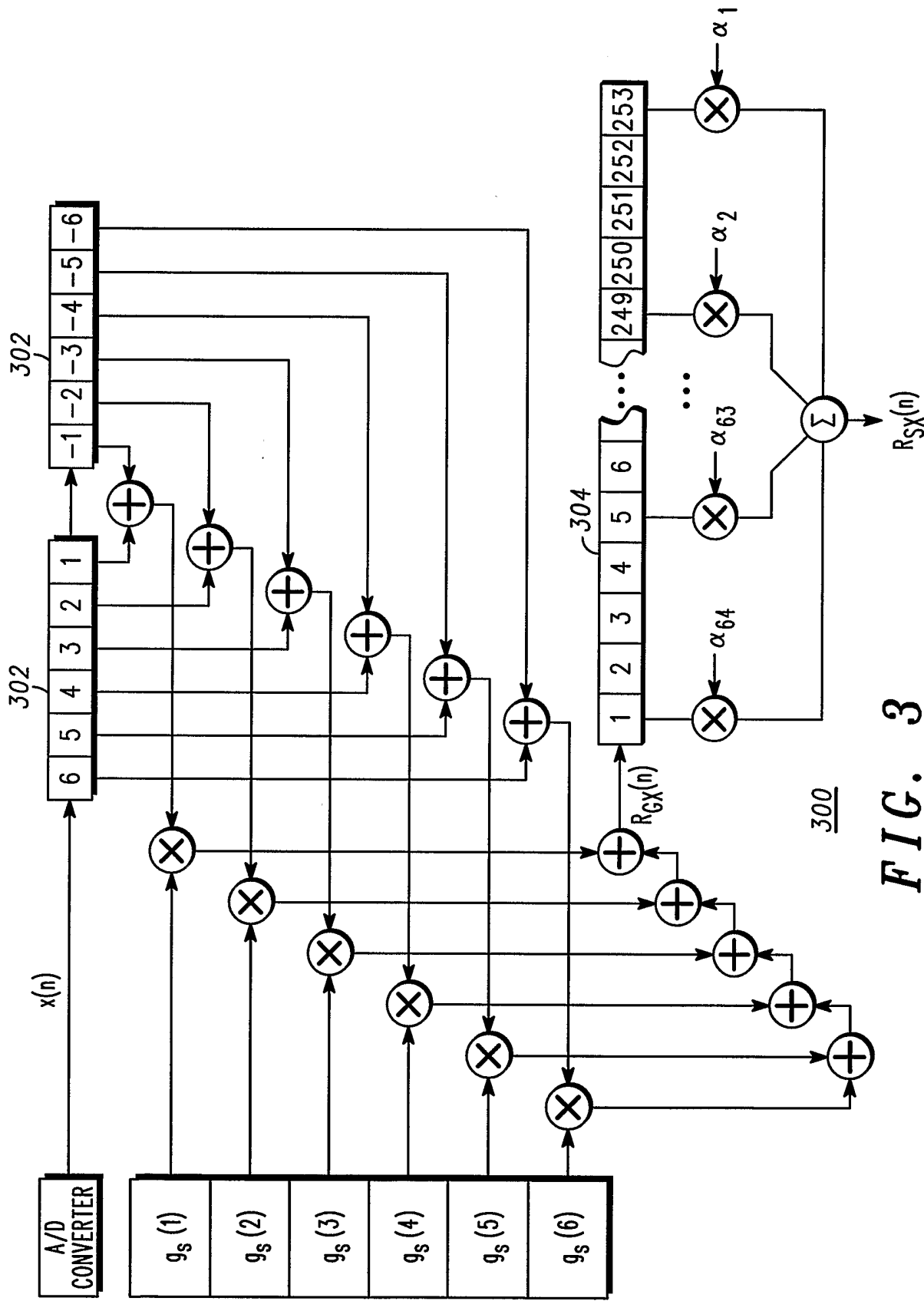PEAK AND CORRESPONDING TO THE ESTIMATED
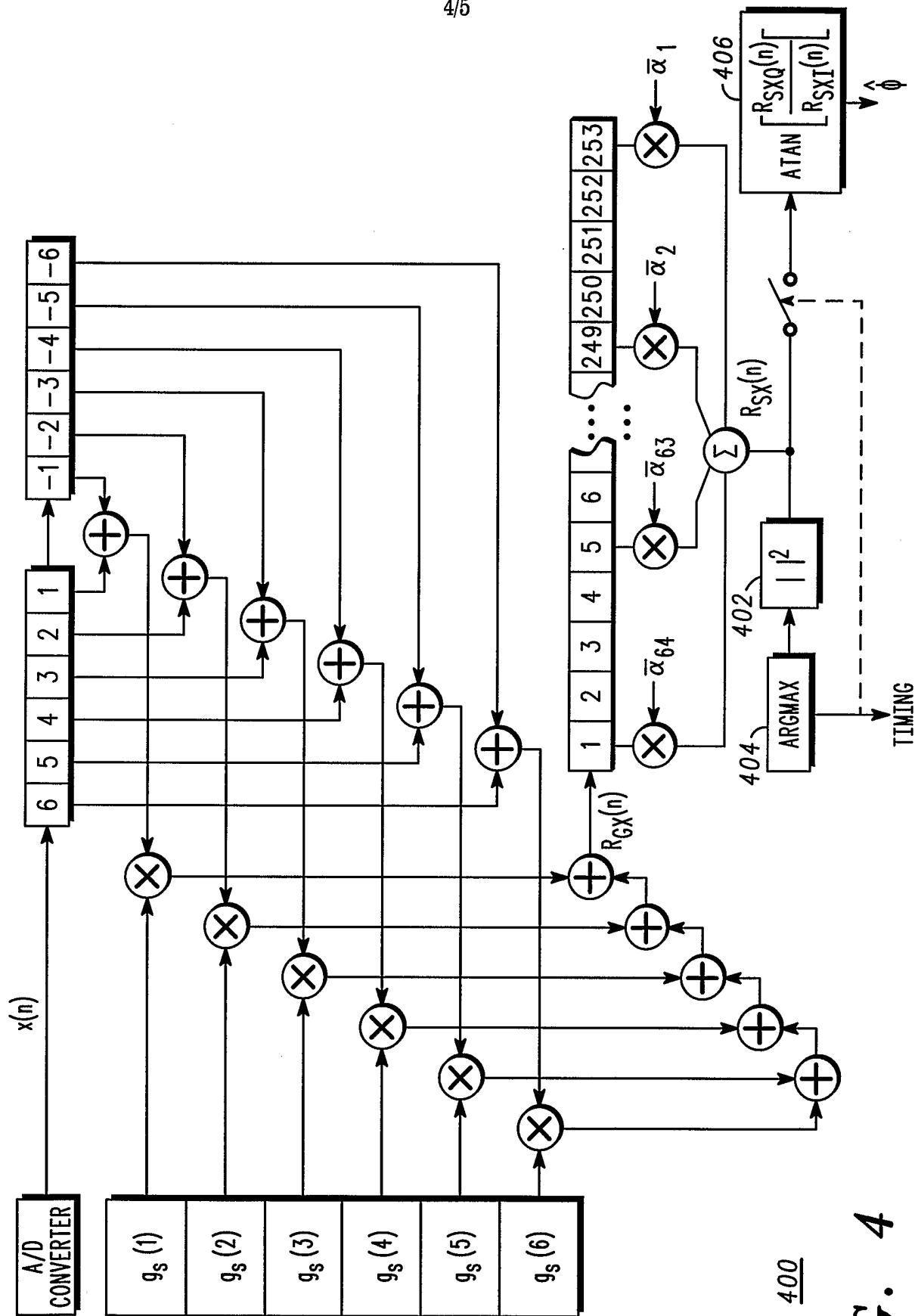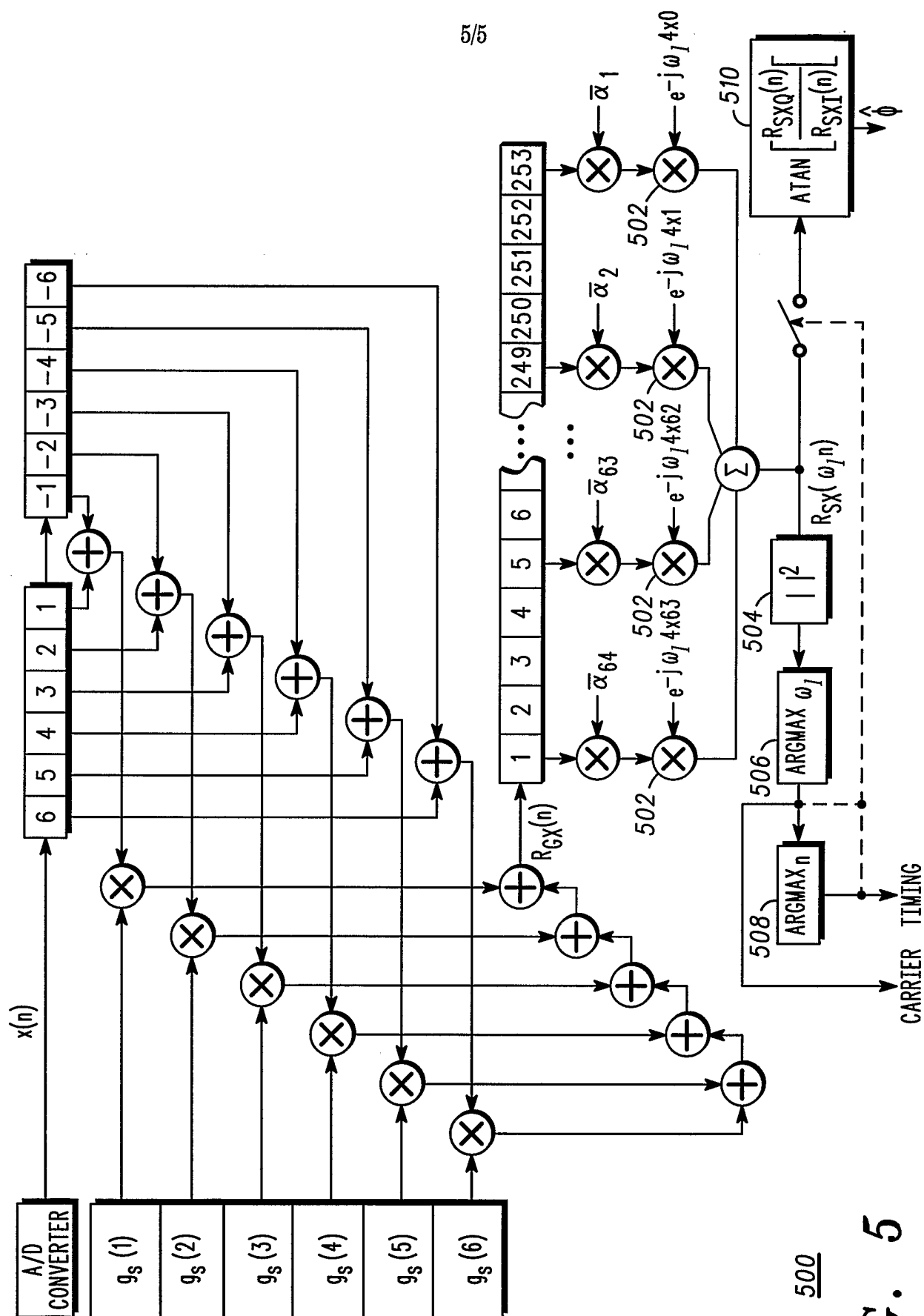CARRIER ERROR

FIG. 2

FIG. 3

300

4/5

F I G. 4

FIG. 5

INTERNATIONAL SEARCH REPORT

A.	CLASSIFICATION OF SUBJECT MATTER

IPC(7)　　:　H04L 7/00
US CL　　:　375/354

According to International Patent Classification (IPC) or to both national classification and IPC

B.	FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
　　U.S. : 375/142, 149, 150, 354, 355, 365, 368; 370/208, 342

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C.	DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,949,817 A (MARSHALL) 07 September 1999, all	1-24
A	US 5,732,114 A (THEBAULT et al.) 24 March 1998, all	1-24

☐ Further documents are listed in the continuation of Box C.　　☐　See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier application or patent published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 October 2002 (25.10.2002)	
Name and mailing address of the ISA/US 　　Commissioner of Patents and Trademarks 　　Box PCT 　　Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Shuwang Liu Telephone No. 703 308-9556

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INTERNATIONAL SEARCH REPORT

Continuation of B. FIELDS SEARCHED Item 3:
East
search terms: synchronization signal, cross-correlation, peak