## Main Features:

- Power Line Communication (PLC) modem chip
- Incorporates Yitran's high performance DLL (Data Link Layer) and extremely robust PHY (Physical) layer
- Simple serial Host interface (logical command language over UART)
- Ideal for "No New Wires" applications over the existing electrical wiring and grids, such as automation, command and control, security and AMR (Automatic Meter Reading)

## Layer 2 (DLL) Main Features:

- PLC optimized Data Link Layer (DLL)
- Up to 1023 logical networks and 2047 nodes/network
- Acknowledged (ACK) and Unacknowledged (UnAck) data transmission services
- Re-transmission mechanism
- Support for all Layer 1 (PHY) transport modes with automatic rate control
- CSMA/CA (Carrier Sense Multiple Access with Collision Avoidance) channel access scheme
- Patent pending Adaptive back-off algorithm based on IEEE802.11 and optimized for the power line medium

## Layer 1 (PHY) Main Features:

- PLC optimized Physical Layer (PHY)
- DCSK (Differential Code Shift Keying) patented modulation technique provides extremely high communication reliability (US patent No. 6,064,695)
- High immunity to signal fading, various noise characteristics, impedance modulation and phase/frequency distortion
- High in-phase and cross-phase reliability
- Forward short-block soft decoding error correction mechanism and CRC-16
- Complies with worldwide regulation requirements (FCC, ARIB, EN50065-1-CENELEC)
- Multiple transport modes:
  - FCC and ARIB bands maximum raw bit rate:
    - 7.5Kbps Standard Mode (SM)
    - 5.0Kbps Robust Mode (RM)
    - 1.25Kbps Extremely Robust Mode (ERM)
  - CENELEC bands maximum raw bit rate:
    - 2.5 Kbps Robust Mode (RM)
    - 0.625Kbps Extremely Robust Mode (ERM)

  Note: CENELEC-A2 will be times ¾ of the above rates.
- Requires low-cost external AFE (Analog Front End)

## General Description:

The IT800D is a highly integrated SoC (System on a Chip) power line communication modem. With Yitran's high performance DLL (Data Link Layer) and extremely reliable PHY (Physical) layer, the IT800D provides an ideal solution for a variety of applications and supports the implementation of various protocols. The utilization of an advanced patented DCSK (Differential Code Shift Keying) spread spectrum modulation technique in the IT800 modem core, enables extremely robust communication over the existing electrical wiring with data rates up to 7.5Kbps. In addition to the inherent interference immunity provided by the DCSK modulation, the device utilizes several mechanisms for enhanced communication robustness, such as forward short block soft decoding error correction algorithm (patent pending) and special synchronization algorithms. UART interface and simple command language enable simple seamless connection to an external Host. The IT800D complies with worldwide regulations (FCC part 15, ARIB and CENELEC bands) and is an ideal solution for a variety of "No New Wires" narrowband applications.

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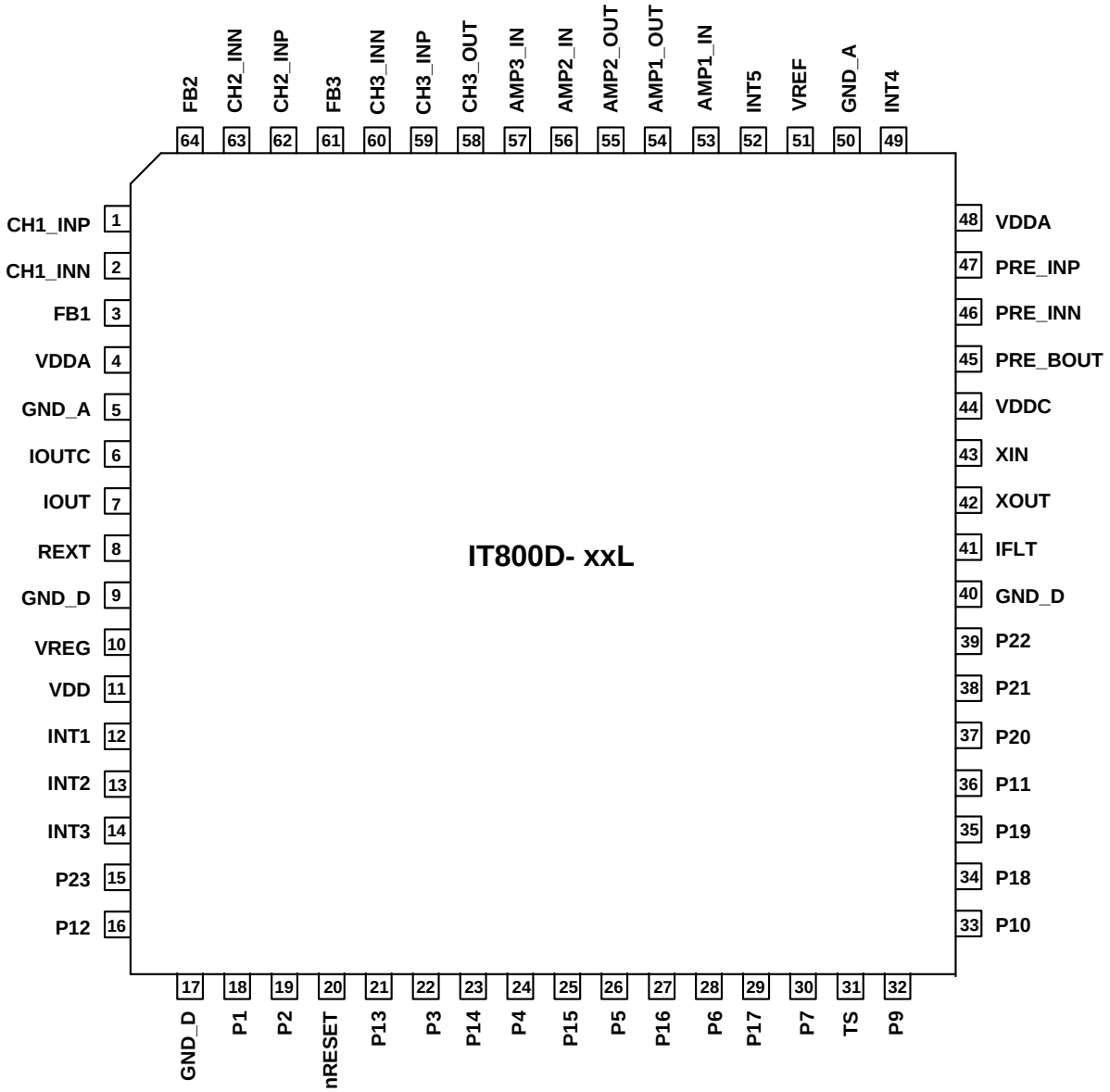
# 1. Pin Description

The following figure illustrates the pinout of the IT800D LQFP64 package (IT800D-xxL):

**Figure 1: LQFP64 ("L" Suffix) Package Pinout**




For mechanical details of the package refer to Figure 24.

## 1.1 Pin Description

The functionality of the IT800D pins is described in Table 2. The pin type format used is **xx/yy** and the options for the **xx** and **yy** fields are shown in the following table:

**Table 1: Pin Type Syntax**

| xx | Description |
|---|---|
| I | Input |
| O | Output |
| IO | Input or Output |

| yy | Description |
|---|---|
| PD | Internal Pull-Down |
| PU | Internal Pull-UP |
| A | Analog |

For further details about xx/PU and xx/PD types refer to section 3.1.

**Table 2: IT800D Pin Description**

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 1 | **CH1_INP** | I/A | Channel 1 ADC differential input |
| 2 | **CH1_INN** | I/A | Channel 1 ADC differential input |
| 3 | **FB1** | A | Channel 1 ADC external capacitor connection |
| 4 | **VDDA** | Power | +3.3V power supply voltage (analog) |
| 5 | **GND_A** | Power | Ground (analog) |
| 6 | **IOUTC** | O/A | DAC differential current output |
| 7 | **IOUT** | O/A | DAC differential current output |
| 8 | **REXT** | A | DAC external reference resistor connection |
| 9 | **GND_D** | Power | Ground (digital) |
| 10 | **VREG** | O/A | +1.8V core voltage output (must be connected to VDDC pin, #44) |
| 11 | **VDD** | Power | +3.3V power supply |
| 12 | **INT1** | IO/PU | Not used |
| 13 | **INT2** | IO/PU | Not used |
| 14 | **INT3** | IO/PU | Not used |
| 15 | **P23** | IO/PU | Not used |
| 16 | **P12** | IO/PD | RX LED – Reception indication. This signal remains high for the duration of the packet reception. |
| 17 | **GND_D** | Power | Ground (digital) |
| 18 | **P1** | O/PD | **SCL** (Serial Clock Line) - EEPROM 2-wire interface clock |
| 19 | **P2** | IO/PU | **SDA** - (Serial Data) - EEPROM 2-wire interface data |
| 20 | **nRESET** | I/PU | RESET (active low) |
| 21 | **P13** | IO/PU | Not used |
| 22 | **P3** | IO/PD | Not used |
| 23 | **P14** | IO/PU | Not used |
| 24 | **P4** | IO/PD | Not used |
| 25 | **P15** | IO/PU | Not used |
| 26 | **P5** | IO | Not used (no internal pulling – MUST be pulled-up externally) |
| 27 | **P16** | IO/PU | Not used |
| 28 | **P6** | I/PU | Not used |

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 29 | **P17** | IO/PU | Not used |
| 30 | **P7** | IO/PU | Not used |
| 31 | **TS** | O/PD | External transmission amplifier enable |
| 32 | **P9** | O/PD | **TXD** - UART transmit serial data output |
| 33 | **P10** | I/PD | **RXD** - UART receive serial data input |
| 34 | **P18** | IO/PU | Not used |
| 35 | **P19** | IO/PU | Not used |
| 36 | **P11** | IO/PD | Not used |
| 37 | **P20** | IO/PU | Not used |
| 38 | **P21** | IO/PU | Not used |
| 39 | **P22** | IO/PU | Not used |
| 40 | **GND_D** | Power | Ground (digital) |
| 41 | **IFLT** | A | PLL loop filter connection |
| 42 | **XOUT** | O/A | Crystal oscillator output |
| 43 | **XIN** | I/A | Crystal oscillator input |
| 44 | **VDDC** | Power | +1.8V core power supply (must be connected to VREG pin, #10) |
| 45 | **PRE_BOUT** | O/A | Pre-Amplifier buffered output |
| 46 | **PRE_INN** | I/A | Pre-Amplifier differential input |
| 47 | **PRE_INP** | I/A | Pre-Amplifier differential input |
| 48 | **VDDA** | Power | +3.3V power supply voltage (analog) |
| 49 | **INT4** | O/A | Not used. MUST be left unconnected (NO external pulling) |
| 50 | **GND_A** | Power | Ground (analog) |
| 51 | **VREF** | I/A | Channel amplifiers reference voltage |
| 52 | **INT5** | O/A | Not used. MUST be left unconnected (NO external pulling) |
| 53 | **AMP1_IN** | I/A | Channel 1 amplifier input |
| 54 | **AMP1_OUT** | O/A | Channel 1 amplifier output |
| 55 | **AMP2_OUT** | O/A | Channel 2 amplifier output |
| 56 | **AMP2_IN** | I/A | Channel 2 amplifier input |
| 57 | **AMP3_IN** | I/A | Channel 3 amplifier input |
| 58 | **CH3_OUT** | O/A | Channel 3 amplifier output |
| 59 | **CH3_INP** | I/A | Channel 3 ADC differential input |
| 60 | **CH3_INN** | I/A | Channel 3 ADC differential input |
| 61 | **FB3** | A | Channel 3 ADC external feedback |
| 62 | **CH2_INP** | I/A | Channel 2 ADC differential input |
| 63 | **CH2_INN** | I/A | Channel 2 ADC differential input |
| 64 | **FB2** | A | Channel 2 ADC external feedback |

Please refer to the following section for IMPORTANT NOTES about pulling pins externally.

## 1.2 Pulling Pins Externally

The guidelines for external pulling are described in the following table. Pins that are marked "Must" under the "Requirement" Column MUST be pulled externally. Pins that are marked "Not allowed" should NOT be pulled externally. Other pins may be left unconnected or pulled in the same direction of their internal pulling.

**Table 3 - Pulling Pins Externally**

| Pin # | Name | Function | Internal Pulling | External Pulling | | | |
|---|---|---|---|---|---|---|---|
| | | | | Requirement | Direction | Resistor [ohm] | Note |
| 18 | **P1** | SCL | DOWN | **Must** | UP | 1k | |
| 19 | **P2** | SDA | UP | **Must** | UP | 4.7k | |
| 20 | **nRESET** | RESET | UP | **Must** | DOWN | 1k | |
| 22 | **P3** | Not Used | DOWN | **Optional** | DOWN | 4.7k | |
| 24 | **P4** | Not Used | DOWN | **Optional** | DOWN | 4.7k | |
| 26 | **P5** | Not Used | None | **Must** | UP | 4.7k | |
| 28 | **P6** | Not Used | UP | **Optional** | UP | 4.7k | |
| 32 | **P9** | TXD | DOWN | **Optional** | DOWN | 4.7k | |
| 34 | **P18** | Not Used | UP | **Must** | DOWN | 1k | |
| 49 | **INT4** | Not Used | None | **Not allowed** | ---- | ---- | Must be left unconnected |
| 52 | **INT5** | Not Used | None | **Not allowed** | ---- | ---- | Must be left unconnected |
| Other digital I/O pins marked "Not Used" | | | UP | **Optional** | UP | 4.7k | Type xx/PU pins |
| | | | DOWN | **Optional** | DOWN | 4.7k | Type xx/PD pins |

"UP" – to VDD
"DOWN" – to GND

**IMPORTANT NOTE:**

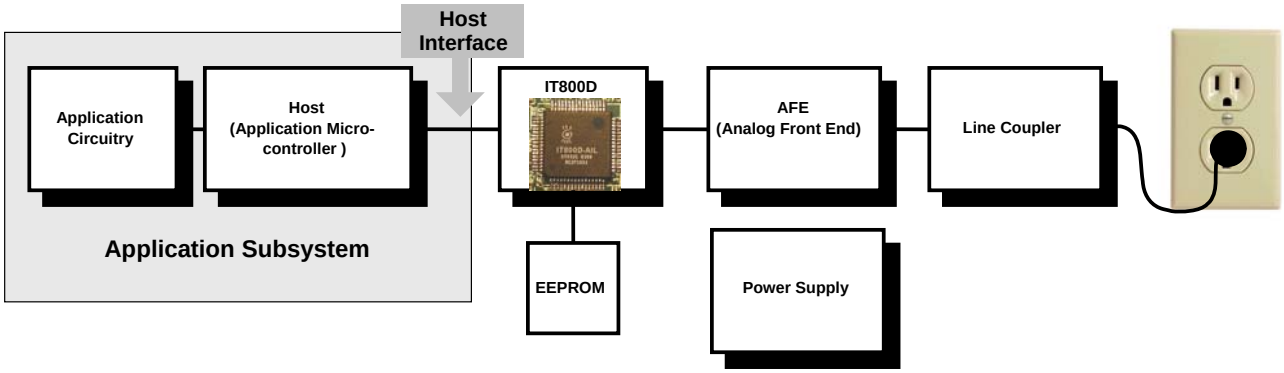
DO NOT use external pulling in an opposite direction to the internal pulling **unless otherwise is so described in the above table**. Such opposite pulling or pulling in the opposite direction to the one mentioned in the table above may cause unpredictable behavior of the device. The same is applicable to the pull resistor value – please use the values mentioned in the table above.

# 2. General Overview

## 2.1 IT800D Based PLC Device

The following figure illustrates a PLC (Power Line Communication) device:

**Figure 2: IT800D PLC Device General Block Diagram**




Such a device is consisted of the following parts:

1. **Application Circuitry** – this section is part of the "Application Subsystem", implementing the specific application and varies accordingly. The application circuitry provides the user interface for the device (switches, LEDs, thermostats etc').

2. **Host** – this entity is also part of the "Application Subsystem", typically implemented using a general-purpose simple micro-controller. The Host controls the behavior of the device. It must also implement a software interface that allows the device application to communicate with and control the IT800D over the UART Host Interface.

3. **IT800D** – The IT800D is optimally designed to provide the best performance over the power line medium. PLC capabilities are added to a device by integrating the IT800D into the circuitry of that device. The IT800D handles the channel access on behalf of the device, in addition to handling the entire communication over the power line. The Host can configure the various communication parameters.

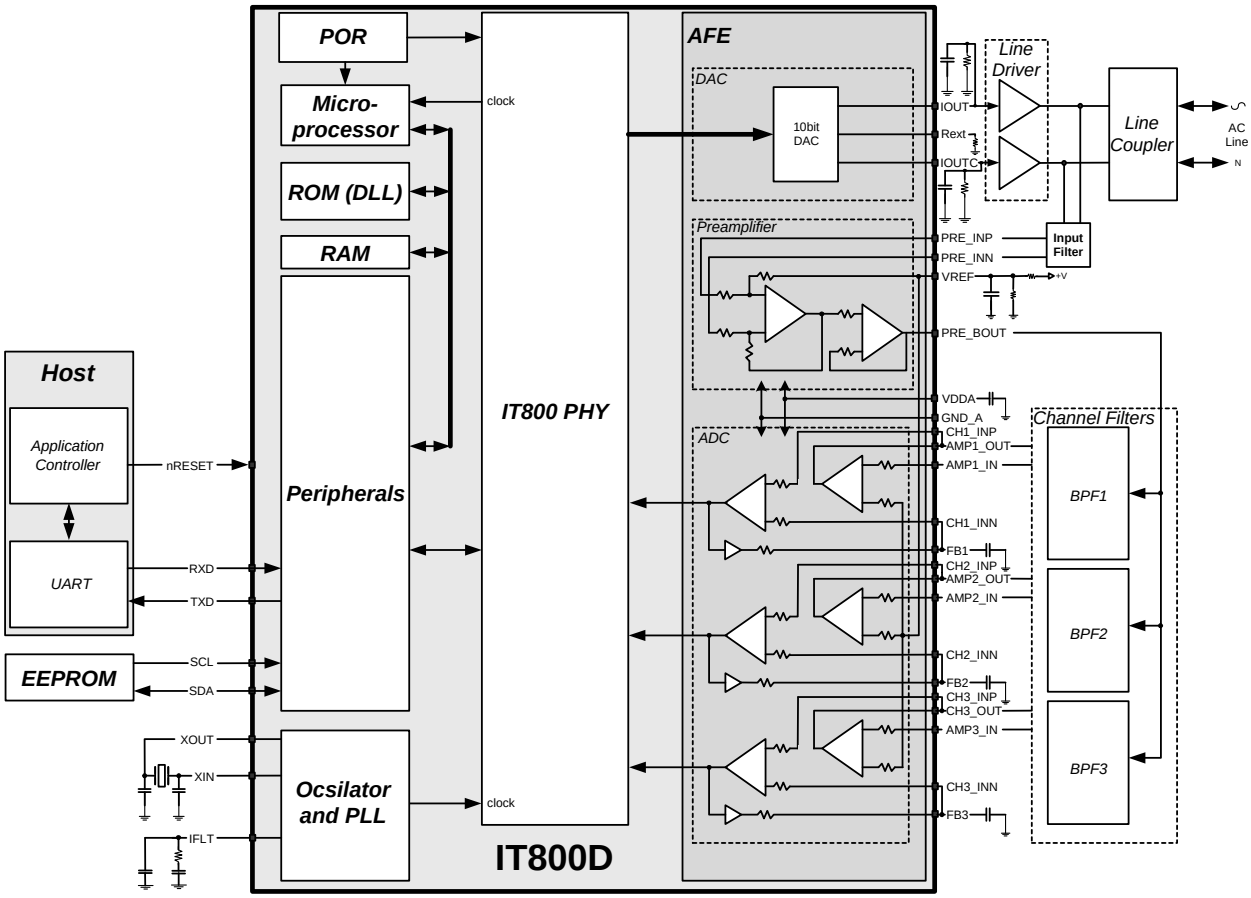
4. **Analog Front End and Line Coupler** – these parts sit between the IT800D and the physical network, connecting the device to the physical network medium (the power line). The AFE includes reception and transmission paths, with the required filtering and amplification. The Line Coupler couples the data to the power line.

5. **Power Supply –** The power supply may be part of the application subsystems or a separate block, providing the required power to the IT800D and AFE.

## 2.2 IT800D General Block Diagram

The following figure describes the block diagram of the IT800D chip and the external circuitry:

**Figure 3: IT800D General Block Diagram and External Circuitry**




Detailed information is provided in the following sections.

# 3. Detailed Description

## 3.1 Digital IO Pins

The internal structure of the digital IO pins enables bidirectional operation but the pins are pre-configured as Inputs (I), Outputs (O) or bidirectional (IO), according to the functionality of each pin (refer to Table 2). Pins that are pulled-up internally are marked PU and those pulled-down internally are marked PD. These pins are further described in the following sections.

nRESET (#20) and P5 (#26) pins have a different internal structure, as described in sections 3.1.3 and 3.1.4 respectively.

**Note**

All the I/O pins function as inputs during RESET.

### 3.1.1 xx/PU Pin

A PU pin is a 3.3V TTL level compatible pin with pull-up resistor as described in the following figure and table:

**Figure 4: xx/PU Pin**

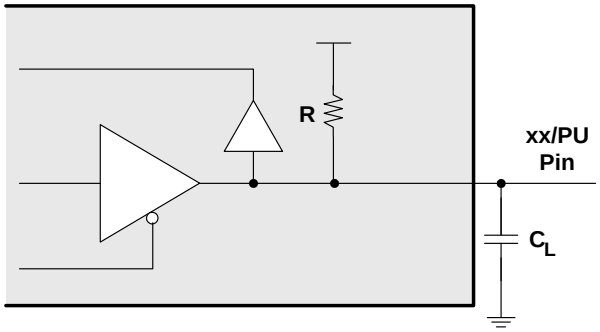



**Table 4: xx/PU Pin Specifications**

| Rating | Symbol | Minimum | Nominal | Maximum | Unit |
|---|---|---|---|---|---|
| Load capacitance | $C_L$ | | | 100 | pF |
| Internal Pull-up Resistor | R | 10 | | 30 | kΩ |

### 3.1.2 xx/PD Pin

A PD pin is a 3.3V TTL level compatible pin with pull-down resistor, as described in the following figure and table:

**Figure 5: xx/PD Pin**

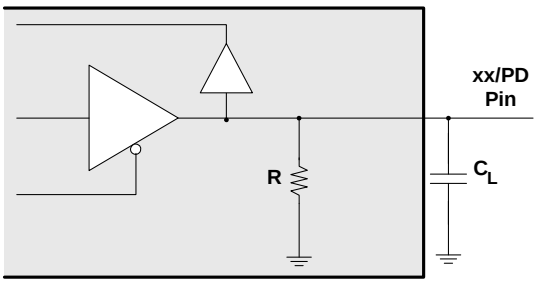



**Table 5: xx/PD Pin Specifications**

| Rating | Symbol | Minimum | Nominal | Maximum | Unit |
|---|---|---|---|---|---|
| Load capacitance | $C_L$ | | | 100 | pF |
| Internal Pull-down Resistor | R | 10 | | 20 | kΩ |

### 3.1.3 nRESET Pin

The nRESET pin is a 3.3V TTL level compatible Schmitt input with a pull-up resistor, as shown in the following figure and table:

**Figure 6: nRESET Pin**

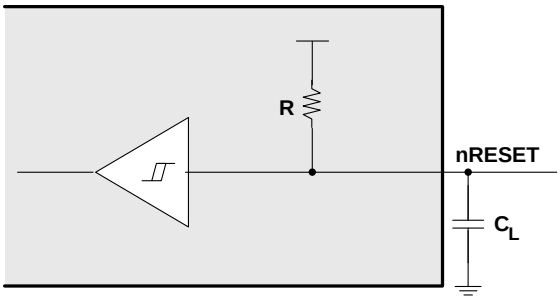



**Table 6: nRESET Pin Specifications**

| Rating | Symbol | Minimum | Nominal | Maximum | Unit |
|---|---|---|---|---|---|
| Load capacitance | $C_L$ | | | 5 | pF |
| Internal Pull-up Resistor | R | 10 | | 30 | kΩ |

For further information on the RESET scheme refer to section 3.7.

### 3.1.4 P5 (#26) Pin

P5 pin is a 3.3V TTL level compatible pin with NO internal pulling resistor, as described in the following figure and table:

**Figure 7: P5 (#26) Pin**

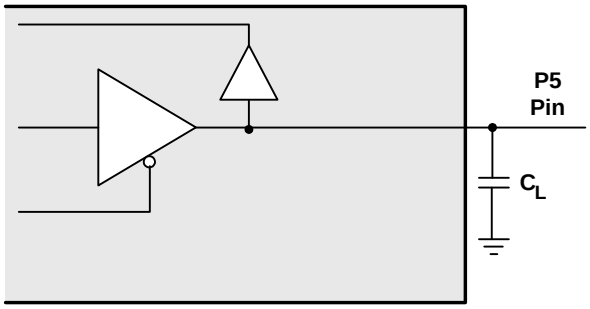



**Table 7: P5 Pin Specifications**

| Rating | Symbol | Minimum | Nominal | Maximum | Unit |
|---|---|---|---|---|---|
| Load capacitance | $C_L$ | | | 100 | pF |

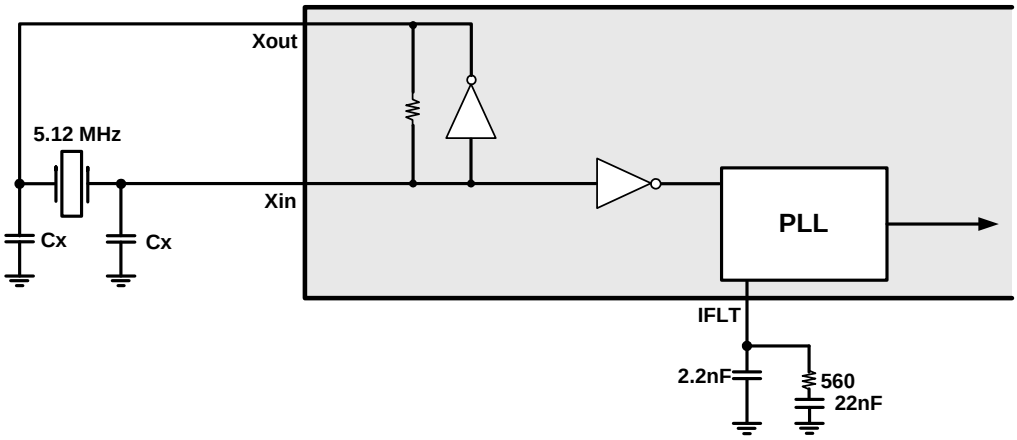
**IMPORTANT NOTE:**

This pin **MUST** be pulled-UP externally to VDD **via a resistor** (4k7 recommended).

## 3.2 IT800D Clock Circuit

The external and internal circuitry of the clock mechanism is shown in the following figure:

**Figure 8: IT800D Clock Circuit**




**Notes:**

1. Recommended value for Cx is 18pF (this value may depend on the specific crystal characteristics).
2. The crystal should be located as close as possible to Xin and Xout pins.

The following table describes the required specifications of the external crystal:

**Table 8: Crystal Specifications**

| Parameter | Minimum | Nominal | Maximum | Unit |
|---|---|---|---|---|
| Operating Frequency | | 5.12<br>(3.84 for CA2) | | MHz |
| Overall Accuracy | | 150 | | PPM |
| Drive Level | | | 150 | µW |
| Equivalent Series Resistance | | | 100 | Ω |
| Motional Capacitance | 3 | | | fF |
| Shunt Capacitance | | | 7 | pF |
| Load Capacitance | 15 | | 20 | pF |

## 3.3 Host Interface

The IT800D logical interface (command language), is implemented over a UART physical interface. The UART Physical interface is described in the following sections.

The logical interface (command language) is described in a separate document (refer to the "IT800D Host Interface Command Set User Guide", Yitran reference: IT800-UM-017-Rx.x for full details of the logical interface). Important guidelines regarding the logical interface are also described in the following section.

### 3.3.1 Interface General Guidelines

While implementing the Host interface software, the guidelines below should be followed:

1. **Full-Duplex Operation** – while implementing the Host interface software, it is important to note that the communication over this interface is full duplex. While the Host transfers information to the IT800D, the latter may transfer information to the Host simultaneously. Therefore the Host software should be designed to handle such full-duplex operation.

2. **Received Packet/Command Response** – the IT800D transfers a response to each Host command, and the Host should not transfer another command to the IT800D prior to getting the response for the previous one. The Host software should be implemented in such manner, that it can handle both responses and received packets in any scenario (e.g. while waiting to get a command response).

3. **Unique Transfer Task** – it is required to ensure that only a single transfer task is implemented by the Host to avoid multiple simultaneous transfers (example: configuration during transmission or vice versus).

Complete details of the logical interface and its implementation are provided in the Command Set document mentioned above.

### 3.3.2 UART

The Host physical interface includes the UART connections and the nRESET line, as described in the following figure and table:

**Figure 9: Host Interface Overview**

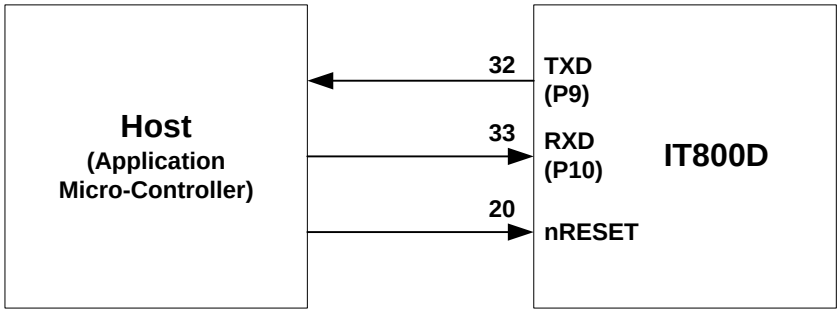



**Table 9: Host Interface Pins**

| Pin Name | Pin Number | Interface Function | Description |
|---|---|---|---|
| P9 | 32 | TXD | UART data output (IT800D → Host) |
| P10 | 33 | RXD | UART data input (Host → IT800D) |
| nRESET | 20 | nRESET | RESET (active low) |

#### 3.3.2.1 Communication Parameters

The communication parameters of the UART are described in the following table:

**Table 10: UART Communication Parameters**

| Parameter | Value |
|---|---|
| Communication Rate [bps] | 38400<br>(28800 for CA2) |
| Data [bits] | 8 |
| Parity [bits] | 0 |
| Stop [bits] | 1 |
| Flow Control | Off |

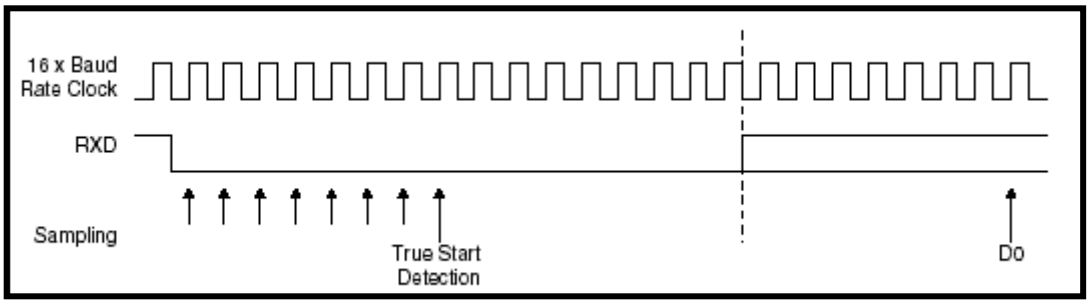
### 3.3.2.2 Receiver

The UART detects the start of a received character by sampling the RXD signal until it detects a valid start bit. A low level (space) on RXD is interpreted as a valid start bit if it is detected for more then 7 cycles of the sampling clock, which is 16 times the baud rate. Hence, a space, which is longer then 7/16 of the bit period, is detected as a valid start bit. A space, which is 7/16 of the bit period or shorter, is ignored and the receiver continuous to wait for a valid start bit.

When a valid start bit has been detected, the receiver samples the RXD at the theoretical mid-point of each bit. It is assumed that each bit lasts 16 cycles of the sampling clock (1-bit period), so the sampling point is 8 cycles (0.5 bit period) after the start bit. The first sampling point is therefore 24 cycles (1.5 bit period) after the falling edge of the start bit was detected. Each subsequent bit is sampled 16 cycles (1 bit period) after the previous one.

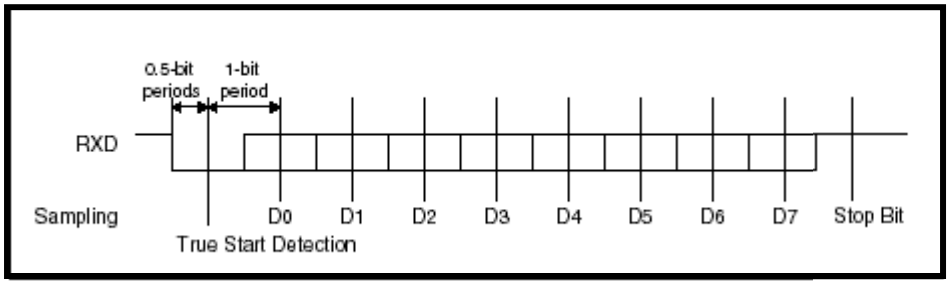
Since the baud rate clock is set to 38,400 bps (28800 for CA2), then the bit period is 26usec (34.67usec for CA2). See the examples in the following figures.

**Figure 10: UART – Start Bit Detection**




Source: ATMEL

**Figure 11: UART – Character Reception**

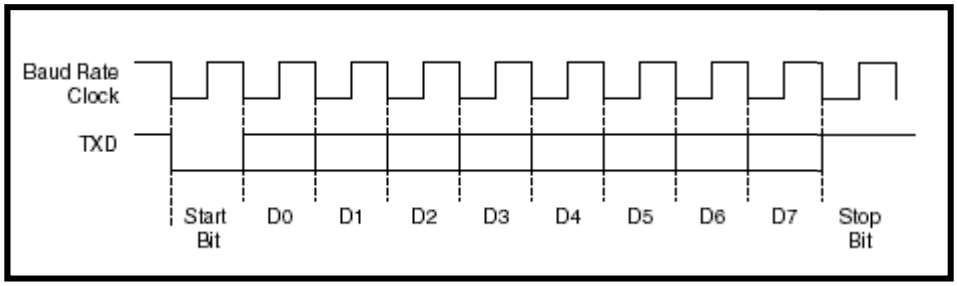



Source: ATMEL

#### 3.3.2.3 Transmitter

Start bit, data bits and stop bits are serially shifted, lowest significant bit first. See the example in following figure (the Baud Rate Clock is an INTERNAL signal).

**Figure 12: UART - Character Transmission**

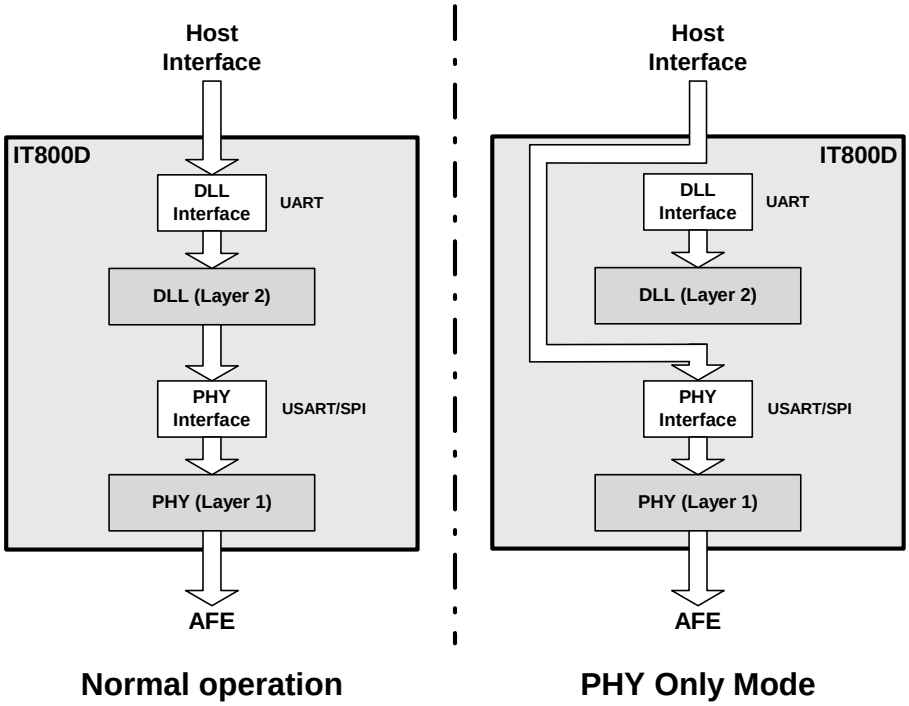



Source: ATMEL

## 3.4 PHY Only (IT800P) Operation Mode

The IT800D can be set to operate in PHY Only mode. In this mode the device only the PHY layer is activated (same is previously implemented in the IT800P device). Host interface in PHY Only mode changes accordingly to the functionality of the PHY layer interface, as described in the following figure:

**Figure 13: Host Interface in Normal Operation and in PHY Only Mode**




Setting the device to operate in this mode is done in the initialization process upon power up or RESET. The information of the required initialization process and the description of the IT800D chip in its PHY Only mode are provided in the "IT800D PHY Only Mode" Application Note (Yitran reference: IT800-AN-016-Rx.x, for the availability of this document please contact: support@yitran.com and refer to the Important Note below).
Once the IT800D is set to operate in this mode it should be regarded as a PHY device as long as RESET is not applied and the power is not turned off (the default mode is the normal operation with DLL and PHY activated, therefore initialization for PHY Only mode must be implemented upon RESET and power-up to keep using the PHY Only mode).

**Important Note:**

Operation in PHY Only Mode is not recommended. Since the DLL handles the channel access procedure, using the IT800D as such assures coexistence with other IT800D and IT800SCP based products, **regardless** of the vendor, protocol and the application. There is NO such coexistence if the device is used in PHY Only Mode.

## 3.5 External EEPROM

### 3.5.1 Overview

An external EEPROM is required to store DLL parameters. A 24Cxx serial EEPROM should be used. It possible to avoid the EEPROM altogether ONLY in FCC compatible designs, where the default values stored in the IT800D may be used. In this case (no EEPROM), changes made to the default parameters by the Host microcontroller are lost in case of RESET or power-down (Host must re-update them).

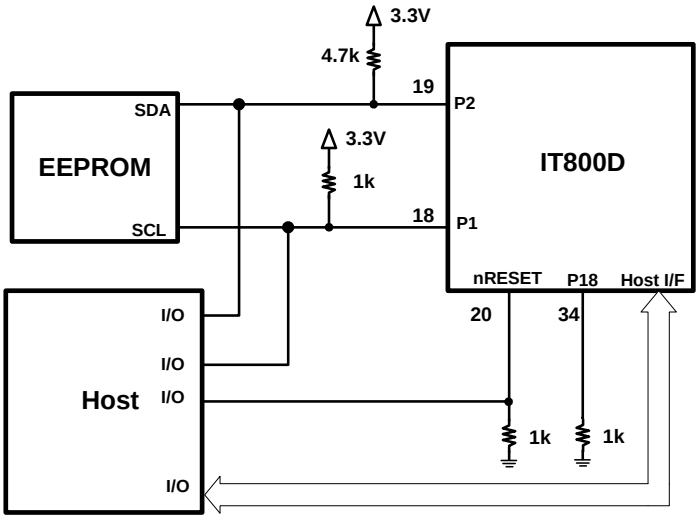
**Important Note:**

The EEPROM device used must have a 64-Byte page write mode.

### 3.5.2 The Required Circuitry

The required EEPROM connection to the IT800D and the Host (application micro-controller) is shown in the following figure:

**Figure 14: IT800D, Host and EEPROM Circuitry**




When the Host controller applies RESET to the IT800D ('0' to nRESET, pin #20), the device enters an initialization process (refer to section 3.8). The external EEPROM may enforce a different level on P2-SDA than the one required for proper initialization of the IT800D. Applying RESET to the IT800D while the EEPROM enforces a wrong level may lead to an improper initialization of the IT800D and setting of the IT800D to an undefined mode.

The circuitry above with the procedure that is described in the following section, allows the Host to release the EEPROM and prevent it from enforcing a wrong level on P2-SDA.

### 3.5.3 EEPROM RESET Procedure

The procedure to RESET the EEPROM includes the following **steps**:

1. Two of the Host I/O pins should be connected to P1-SCL (#18) and P2-SDA (#19). During normal operation these pins should be set to high impedance state or as inputs.

2. The Host applies RESET to the IT800D (sets the level of nRESET at '0'). Only after applying RESET (during the period $T_{START}$ - refer to the following figure), the Host I/O pins connected to P1-SCL and P2-SDA should be set to their required functionality (output/input).

3. The Host then clocks the EEPROM on P1-SCL line. Up to 9 clock cycles should be applied, while monitoring the level of P2-SDA in each cycle, when P1-SCL is '1' (during the period $T_{HIGH}$). The clock cycles should be applied until a level of '1' is detected on P2-SDA.

4. The Host sets P2-SDA as output and creates an "EEPROM Start" condition by applying a level '1' to '0' transition on P2-SDA, while P1-SCL level is '1'.

5. The Host sets its I/O pins connected to the EEPROM as inputs/high-impedance again and continues with the IOS (Initial Operation Sequence) of the IT800D (refer to section 3.8).

.

The following figure and table describe the required procedure (the above-mentioned steps 1-5) and the required timing information.

**Figure 15: EEPROM RESET - Host Procedure Timing Diagram**

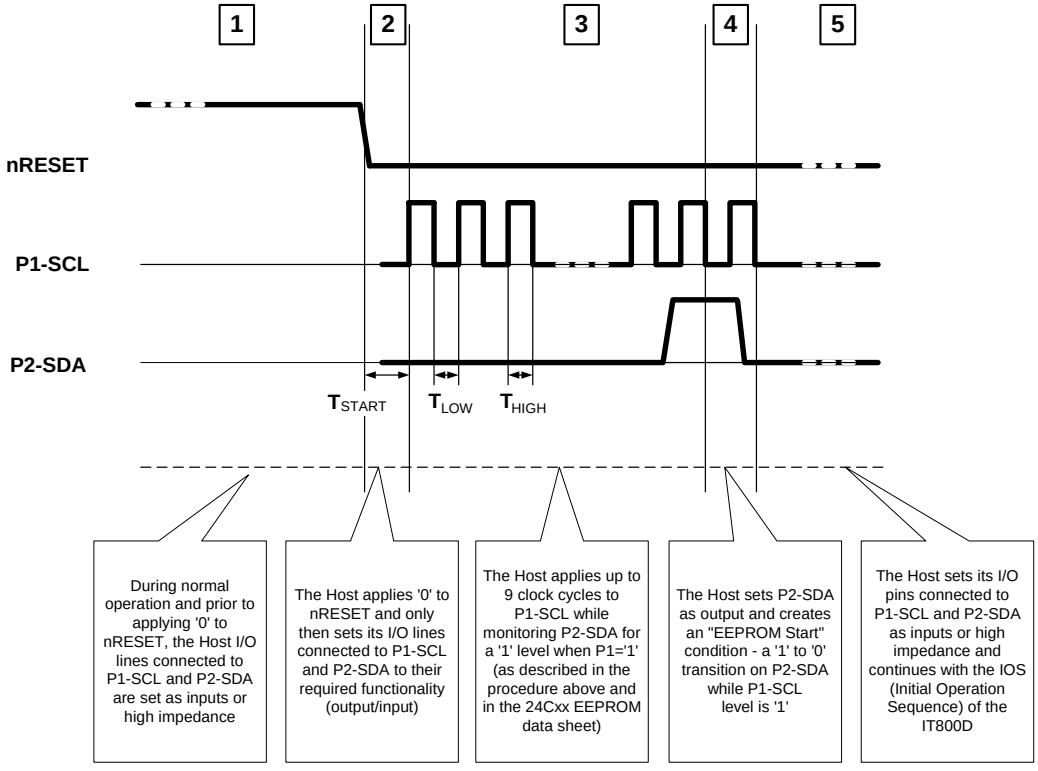


**Table 11: EEPROM RESET - Host Procedure Timing Parameters**

| Parameter | Minimum | Nominal | Maximum | Units |
|---|---|---|---|---|
| $T_{START}$ | 8 | | | µS |
| $T_{LOW}$ | 5 | | | µS |
| $T_{HIGH}$ | 5 | | | µS |

An example for a generic C-code implementation of the required workaround procedure is described in the following figure:

**Figure 16: EEPROM RESET - Generic C-code**

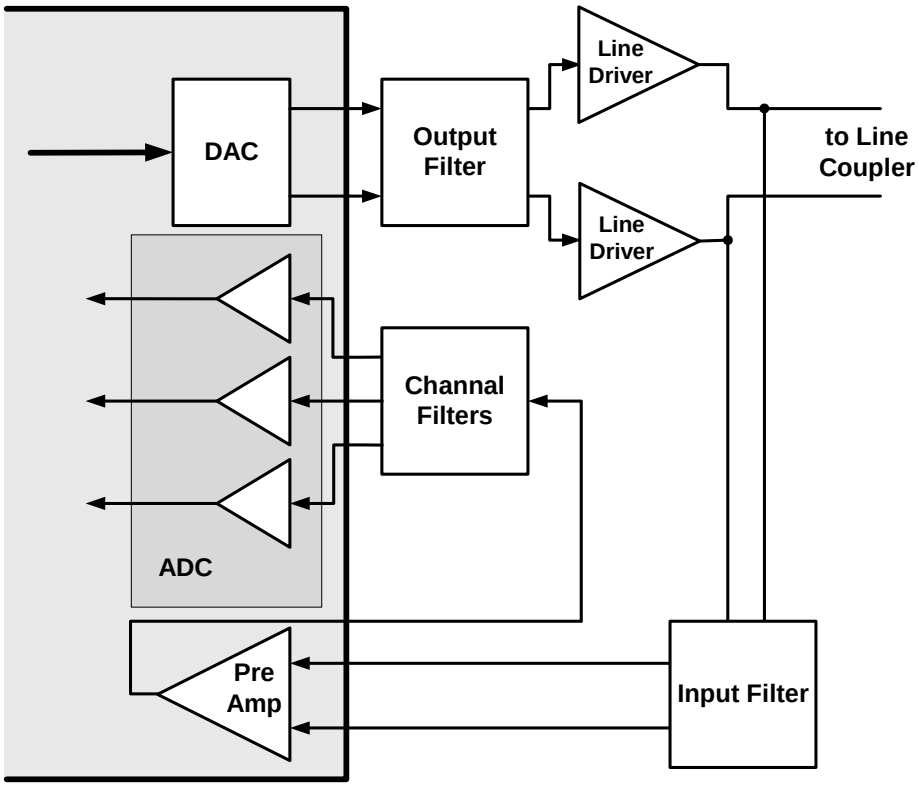
```
static void s_ResetEEPROM( void )
  {
  int i, c;

  D8CHal_DisableOutputPAD2(); // set the SDA line of the serial EEPROM as input
  D8CHal_ClearPAD1();         // clear the SCL line

  D8CHal_Delay(4);          // wait for 8 uS

  for( i = 0, c = 1; ((i < 9) && (c != 0)); i++ ) // send up to 9 clocks to the
                                                     serial EEPROM
    {
    D8CHal_SetPAD1(); // set SCL line
    D8CHal_Delay(2);  // wait for 4 uS

    if( !D8CHal_GetPAD2() ) // check if the SDA line is high
      {
      D8CHal_Delay(2.5);     // if the SDA line is low, wait for 5 uS
      D8CHal_ClearPAD1(); // clear the SCL line, end the cycle
      D8CHal_Delay(2.5);     // wait for 5 uS
      }
    else
      {
      D8CHal_EnableOutputPAD2(); // configure the SDA line as the controller
                                    output
      D8CHal_ClearPAD2();       // create the start condition by
setting SDA low
      D8CHal_Delay(1);         // wait for 2 uS
      D8CHal_ClearPAD1();     // clear the SCL line, end the cycle
      D8CHal_Delay( 2 );     // wait for 4 uS
      c = 0;                // exit the EEPROM reset sequence
      }
    }
  }
```

## 3.6 AFE (Analog Front End)

The AFE circuitry includes reception and transmission paths and sits between the IT800D and the Line Coupler.

The following figure provides a general description of the AFE block diagram:

**Figure 17: AFE General Block Diagram**




The on-chip AFE includes a DAC (Digital to Analog Converter) in the transmission path and a Pre-amplifier and a ADC (Analog to Digital Converter) in the reception path.

The various parts of the on-chip AFE are described in the following sections.

The external portion of the AFE is detailed in the "IT800 Reference Design" documents (Yitran reference: IT800-RD-011-Rxx and IT800-RD-012-Rxx).

### 3.6.1 DAC (Digital to Analog Converter)

The DAC is part of the transmission path. This block is a current mode 10-Bit Digital to Analog converter, which uses an internal current reference to generate two complementary current outputs. An internal band-gap reference and an external resistor generate the internal current reference. The circuitry of the DAC is described in the following figure:

**Figure 18: DAC – Digital to Analog Converter**

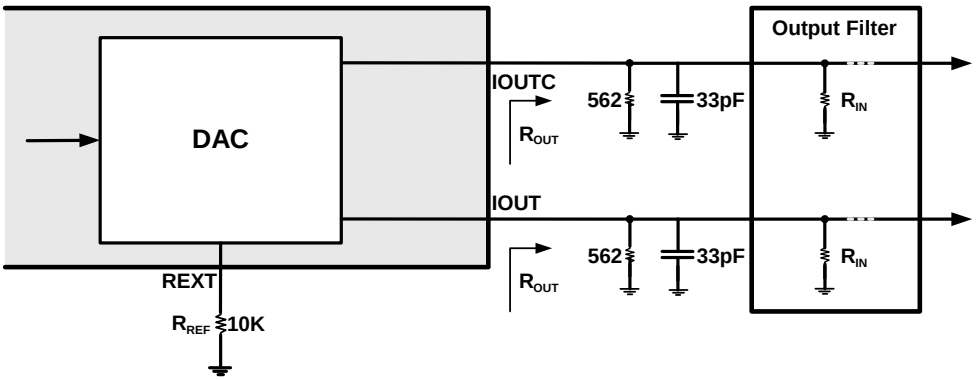



**Table 12: DAC Specifications**

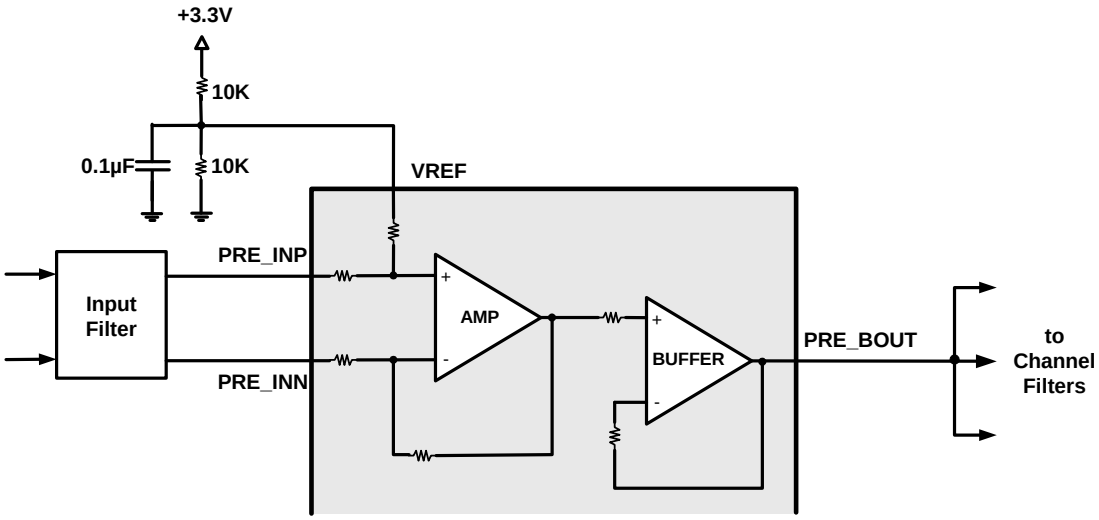
| Parameter | Symbol | Minimum | Nominal | Maximum | Unit |
|---|---|---|---|---|---|
| Internal Voltage Reference | $V_{REF}$ | 1.1 | 1.2 | 1.4 | V |
| Internal Current Range | $I_{REF}$ | 80 | 125 | 200 | µA |
| External Reference Resistor | $R_{REF}$ | | 10 | | kΩ |
| Output Resistor (from IOUTC to the ground) | $R_{OUT}$ | | 390 | 500 | Ω |
| Maximum Output Voltage | | | | 1 | V |
| Full Scale Output Current | | 1.4 | 2 | 2.8 | mA |

$R_{OUT}$ equals to the total external equivalent resistance at the IOUT and IOUTC pins. The 562Ω resistors were selected to comply with the $R_{OUT}$ allowed value-range (refer to the table above), taking into account the input impedance of the external Output Filter ($R_{IN}$). For more details on the external Output Filter refer to the "IT800 Reference Design" documents (Yitran reference: IT800-RD-011-Rxx and IT800-RD-012-Rxx).

### 3.6.2 Pre-Amplifier

The external Input Filter is connected to the pre-amplifier, which is part of the reception path. The pre-amplifier is composed of two stages: amplification stage and buffering stage. The pre-amplifier and its circuitry are described in the following figure:

**Figure 19 : Pre Amplifier**

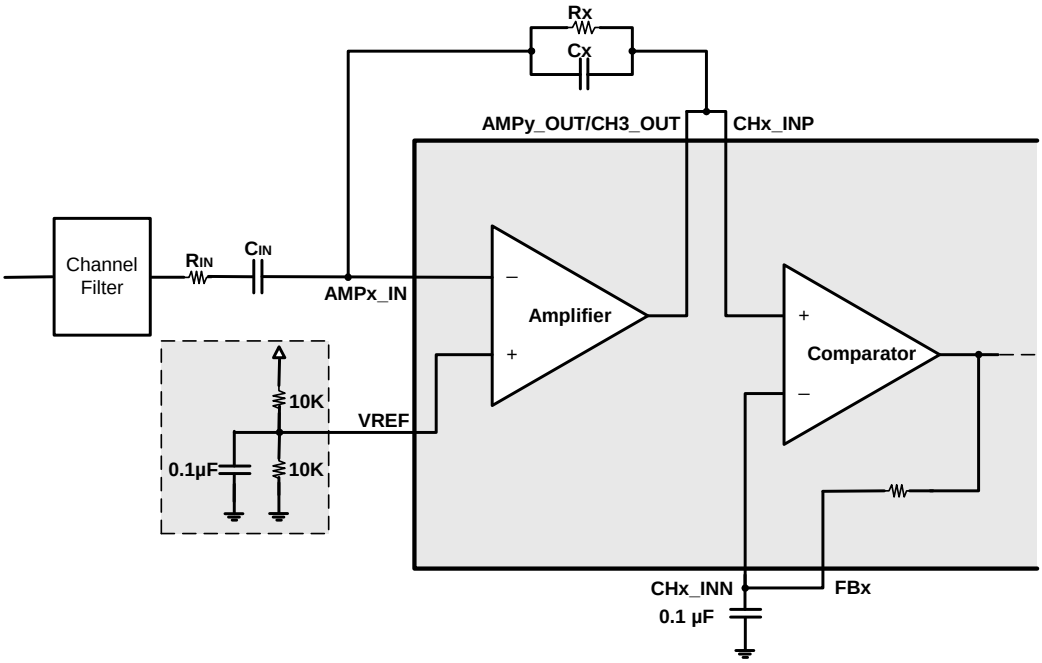



For more details on the Input Filter and Channel Filters please refer to the "IT800 Reference Design" documents (Yitran Reference: IT800-RD-011-Rxx and IT800-RD-012-Rxx).

### 3.6.3 ADC (Analog to Digital Converter)

The output of each external channel filter in the reception path is connected to a 1-bit ADC input. There are three similar ADC units incorporated in the chip. The ADC is built of an amplifier stage followed by a comparator stage. The ADC and its circuitry are described in the following figure:

**Figure 20 : ADC Block Diagram**




The values of the required external components are detailed in the "IT800 Reference Design" documents (Yitran reference: IT800-RD-011-Rxx and IT800-RD-012-Rxx).

**Notes**:

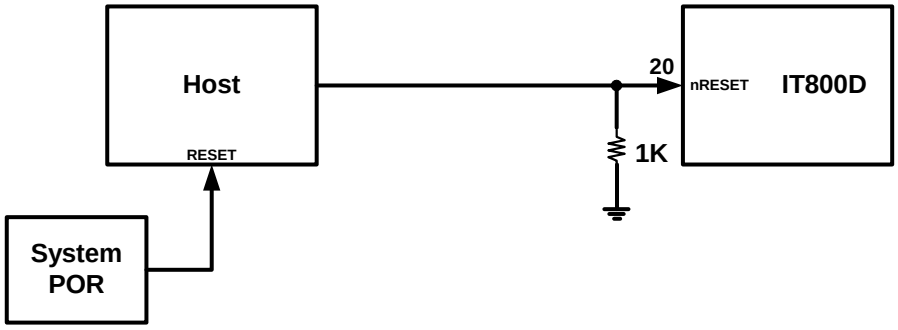
1. VREF input is a single input, which is common to all three ADC units.

2. In gt-B (Europe indoor) compliant design only one channel is used (in this design AMP2_IN and AMP3_IN are tied to ground via a resistor).

## 3.7 Recommended RESET Scheme

The following figure describes the recommended hardware RESET scheme:

**Figure 21: Recommended RESET Scheme**




The guidelines for the RESET scheme shown in the figure above are the following:

1. **External pull-down resistor** (1k) – such a pull-down, connected to the nRESET pin of the IT800D, is required. This pull-down ensures that the IT800D is in RESET state during Host stabilization period upon Power On or Host RESET.

2. **Hierarchal system RESET implementation** – the RESET hierarchy should be such, that the system POR (Power On RESET) applies RESET to the Host and the Host then applies RESET to the IT800D.

### 3.7.1 Applying RESET to the Device

When the Host applies RESET to the IT800D ('0' to nRESET pin), the device enters an initialization sequence. Improper levels on the IT800D interface pins during RESET may result in level conflict and may set the IT800D to improper operation mode. To verify proper initialization of the IT800D the Host should follow these guidelines for applying RESET to the IT800D:

1. Set the Host IO pins connected to the IT800D to high impedance state or as inputs **prior** to applying RESET to the IT800D.

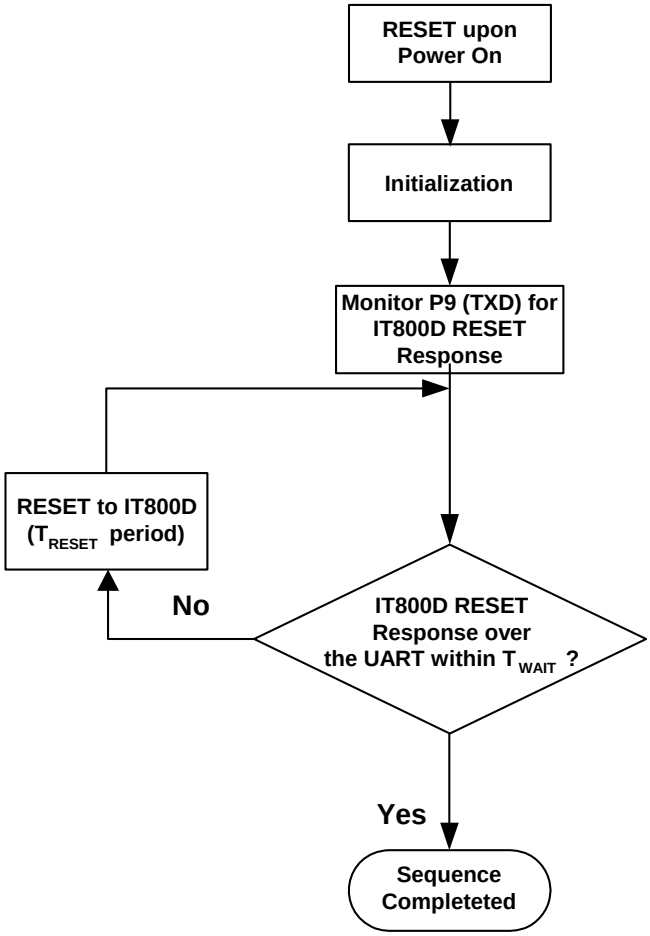
2. Repeat steps 2-3 of the Initial Operation Sequence (IOS) described in section 3.8.2.

## 3.8 Initial Operation Sequence (IOS)

### 3.8.1 Sequence Overview

Upon **Power-On** and **RESET** the Host must implement the Initial Operation Sequence (IOS) for proper operation of the device. The IOS is described in the following figure and in the following sections:

**Figure 22: Initial Operation Sequence (IOS) Flow**




During the IOS the Host is required to set its IO pins connected to the IT800D to high impedance state or as inputs (with proper external pulling as described in section 1.2). The IT800D IO pins change their functionality from inputs (during RESET) to their normal operation function (upon the rising edge of nRESET) and this is required to ensure that there are no level conflicts at this stage.

The Host must keep its IO pins as inputs or in high impedance state during the entire Initialization stage. IOS for Hosts with no such ability is described in a separate Application Note.

### 3.8.2 IOS Detailed

The IT800D Initial Operation Sequence procedure is consisted of the following **steps**:

1 **RESET Upon Power On** - nRESET must be kept at '0' level while the Host powers up (external pull-down is required – refer to Figure 21 and section 1.2). The '0' level should be further kept during $T_{RESET}$ period after the power supply is stable. During this period the Host should set its pins connected to the IT800D interface to high impedance state or as inputs. Proper external pulling should be provided as described in section 1.2, to set the required levels for initialization (the Host may verify these levels by sensing them if it sets its pins as inputs). The required levels are described in the following table:

**Table 13: Required Pin Levels for Initialization**

| Pin Name | Pin Number | Interface Function | Required Level |
|---|---|---|---|
| P1 | 18 | SCL | **'1'** |
| P2 | 19 | SDA | **'1'** |
| P3 | 22 | None | **'0'** |
| P4 | 24 | None | **'0'** |
| P6 | 28 | None | **'1'** |
| P9 | 32 | TXD | **'0'** |

2 **Initialization** – the Host then applies '1' to nRESET for $T_{INIT1}$ period and '0' for $T_{INIT2}$ period, while its IO pins connected to the IT800D interface are still set as inputs or high impedance**,** as described in step 1 above. The initialization of the IT800D takes place upon the rising edge of nRESET at the end of $T_{INIT2}$ period and is set by the external and internal pull resistors.

3 **Monitor TXD** – the IT800D UART is ready $T_{TXD\_HIGH}$ period after the rising edge of nRESET. The level of P9 (TXD) is set to '1' when the UART is configured and ready. The Host should expect to receive from the IT800D a RESET response within $T_{WAIT}$ period. This response is sent over the UART TXD line (P9) and it signals a successful IOS completion. The response is described in the "IT800D Host Interface Command Set User Guide"(Yitran reference: IT800-UM-017-Rx.x. Note that additional soft configuration/initialization may be required as described in that document).

If the Host fails to receive the RESET response within $T_{WAIT}$ then it should repeat steps 2-3 above.

IOS timing information is provided in the following section.

### 3.8.3 IOS Timing

The following figure and table describe the timing parameters of the Initial Operation Sequence:

**Figure 23: Initial Operation Sequence (IOS) Timing**

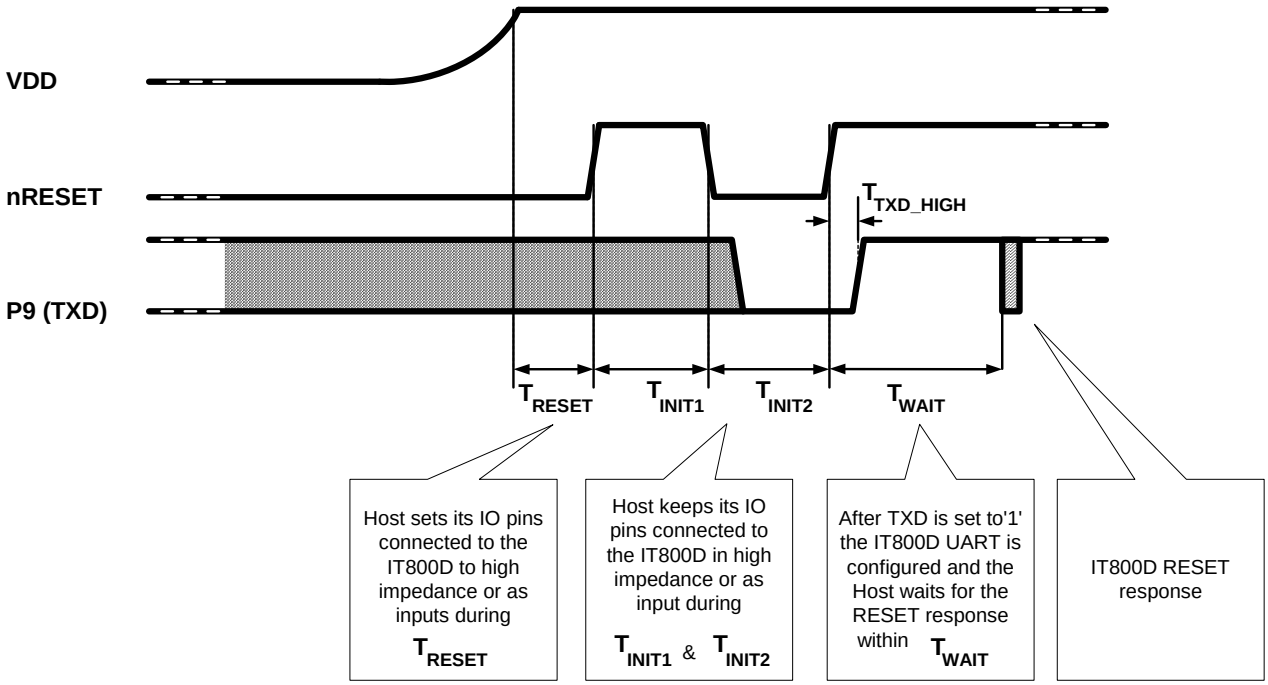



**Table 14: Initial Operation Sequence (IOS) Timing Parameters**

| Parameter | Description | Minimum | Nominal | Maximum | Units |
|---|---|---|---|---|---|
| $T_{RESET}$ | Host and IT800D stabilization period upon power on | 1 | | | Sec |
| $T_{INIT1}$ | Initialization stage 1 | 10 | | | µS |
| $T_{INIT2}$ | Initialization stage 2 | 10 | | | µS |
| $T_{TXD-HIGH}$ | IT800D UART stabilization | | | 5 | mSec |
| $T_{WAIT}$ | RESET response wait time | | | 500 | mSec |

# 4. Electrical Characteristics

## 4.1 Absolute Maximum Ratings

(*) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

| | |
|---|---|
| Power supply voltage, VDDA (max) | 3.6V |
| Power supply voltage, VDD (max) | 3.6V |
| Power supply voltage, VDDA (min) | -0.3V |
| Power supply voltage, VDD (min) | -0.3V |
| Input voltage, $V_I$ (max) | VDD+0.3V,3.6V Max. |
| Input voltage, $V_I$ (min) | -0.3V |
| Storage temperature range | -60°C to 150°C |

## 4.2 Recommended Operating Conditions

| Rating | Symbol | Minimum | Nominal | Maximum | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | VDDA | 3.1 | 3.3 | 3.5 | V |
| Power Supply Voltage | VDD | 3.1 | 3.3 | 3.5 | V |
| Power Supply Voltage (1) | VDDC | 1.65 | 1.8 | 2.0 | V |
| High Level Input Voltage | $V_{IH}$ | 2 | | VDD+0.3 / 3.6 | V |
| Low Level Input Voltage | $V_{IL}$ | -0.3 | | 0.8 | V |
| High Level Output Voltage | $V_{OH}$ | VDD-0.4 | | | V |
| Low Level Output Voltage | $V_{OL}$ | | | 0.4 | V |
| Source and Sink Current (2) | $I_{DO}$ | | | 4 | mA |
| Operating Frequency (3) | $F_{OSC}$ | | 5.12<br>(3.84 for CA2) | | MHz |
| Crystal Overall Accuracy (3) | | | 150 | | PPM |
| Operating Temperature Range | $T_0$ | -40 | 25 | +85 | °C |

**Note:** (1) VDDC is supplied ONLY by the internal voltage regulator and should be connected to VREG output.
(2) Digital I/O pins
(3) For the required crystal specifications please refer to Table 8 in section 3.2.

## 4.3 Supply Current

T = 25°C, VDD = VDDA = 3.3V

| Parameter | | Test conditions | Minimum | Nominal | Maximum | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | VDD Total Supply Current | $F_{OSC}$ = 5.12MHz | | 65 | 100 | mA |

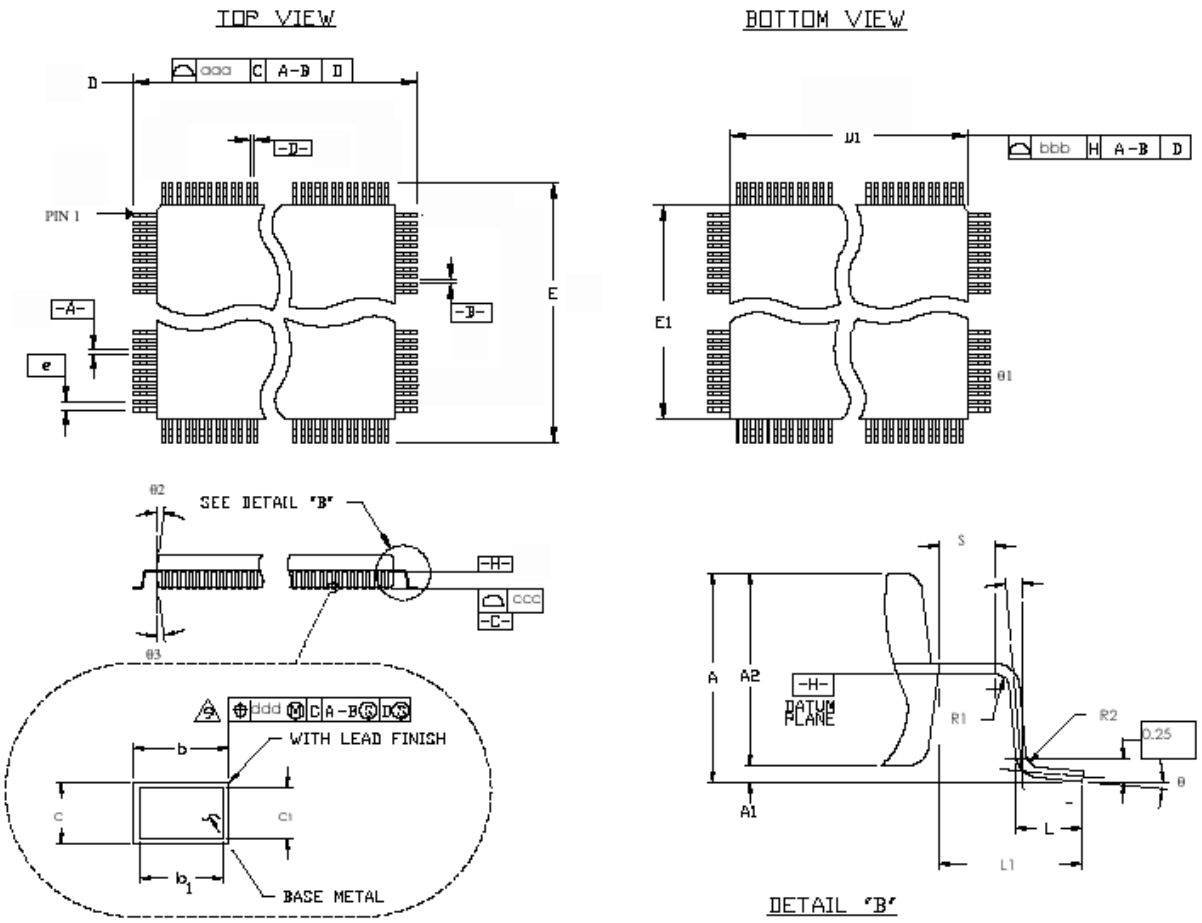
**Note**:

VDD_D and VDD_A must both be supplied simultaneously

# 5. Package Information

## 5.1 IT8000xxx-xxL (64 Pin LQFP)

**Figure 24: 64 LQFP Package**



Common dimensions (mm):

| Symbol | Min | Nom | Max |
|---|---|---|---|
| c | 0.09 | | 0.2 |
| c1 | 0.09 | | 0.16 |
| L | 0.45 | 0.6 | 0.75 |
| L1 | | 1.00 REF | |
| R2 | 0.08 | | 0.2 |
| R1 | 0.08 | | |
| S | 0.2 | | |
| θ | 0° | 3.5° | 7° |
| θ1 | 0° | | |
| θ2 | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° |
| A | | | 1.6 |
| A1 | 0.05 | | 0.15 |
| A2 | 1.35 | 1.4 | 1.45 |
| Tolerances of form and position | | | |
| aaa | | 0.2 | |
| bbb | | 0.2 | |

| D | D1 | E | E1 | B | | | b1 | | | e | ccc | ddd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BSC | BSC | BSC | BSC | Min | Nom | Max | Min | Nom | Max | BSC | | |
| 12.0 | 10.0 | 12.0 | 10.0 | 0.17 | 0.22 | 0.27 | 0.17 | 0.2 | 0.23 | 0.50 | 0.10 | 0.08 |

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