# Design Rule Verification Report

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|---|---|
| **Date:** | 10/2/2022 |
| **Time:** | 9:27:13 PM |
| **Elapsed Time:** | 00:00:02 |
| **Filename:** | C:\Users\Public\Documents\Altium\Lab1\3 Breakout Board\BB3_PCB.PcbDoc |

| | |
|---|---|
| **Warnings:** | 0 |
| **Rule Violations:** | 0 |

## Summary

| **Warnings** | **Count** |
|---|---|
| **Total** | **0** |

| **Rule Violations** | **Count** |
|---|---|
| Clearance Constraint (Gap=0.152mm) (All),(All) | 0 |
| Short-Circuit Constraint (Allowed=No) (All),(All) | 0 |
| Un-Routed Net Constraint ( (All) ) | 0 |
| Modified Polygon (Allow modified: No), (Allow shelved: No) | 0 |
| Width Constraint (Min=0.152mm) (Max=2mm) (Preferred=0.152mm) (All) | 0 |
| Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm) (Entries=4) (All) | 0 |
| Hole Size Constraint (Min=0.305mm) (Max=6.223mm) (All) | 0 |
| Hole To Hole Clearance (Gap=0.254mm) (All),(All) | 0 |
| Minimum Solder Mask Sliver (Gap=0.254mm) (Disabled)(All),(All) | 0 |
| Silk To Solder Mask (Clearance=0.254mm) (Disabled)(IsPad),(All) | 0 |
| Silk to Silk (Clearance=0.254mm) (Disabled)(All),(All) | 0 |
| Net Antennae (Tolerance=0mm) (Disabled)(All) | 0 |
| Board Clearance Constraint (Gap=0mm) (All) | 0 |

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|---|---|
| Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All) | 0 |
| **Total** | **0** |