Xilinx Answer 71453
QDMA Performance Report

Important Note: This downloadable PDF of an Answer Record is provided to enhance its usability and readability. It is important to note that Answer Records are Web-based content that are frequently updated as new information becomes available. You are reminded to visit the Xilinx Technical Support Website and review (Xilinx Answer 71453) for the latest version of this Answer.

Revision History

The following table shows the revision history for this document.

Date	Version	Description
28-Feb-2023	2.0	QDMA5.0 2023.1 performance report

Overview

Xilinx QDMA (Queue Direct Memory Access) Subsystem for PCI Express® (PCIe®) is a high-performance DMA for use with the PCI Express® 3.x Integrated Block(s) which can work with AXI Memory Mapped or Streaming interfaces and uses multiple queues optimized for both high bandwidth and high packet count data transfers. (Please refer QDMA Subsystem for PCI Express v5.0 - PG302 for additional details).

Xilinx provides two reference drivers for QDMA IP

- Linux Kernel driver (Linux Driver)
- DPDK Poll Mode driver (DPDK Driver)

This performance report provides the measurement of the DMA bandwidth of the QDMA IP using the reference Linux and DPDK drivers. This report provides the measured DMA bandwidth with different DMA configurations that can be extrapolated to target application.

The reference design is targeted at PCIe Gen 3 x16 design on Xilinx QDMA5.0 VU9P device on VCU1525 board. The reference design can be ported to other Xilinx cards too.

***Note**: The QDMA DPDK Driver and Linux Driver are hosted at https://github.com/Xilinx/dma_ip_drivers/,under directory QDMA. For known issues and other information on QDMA IP see (Xilinx Answer 70927).*

Audience

The pre-requisite for understanding this document is that the user has gone through the following in Xilinx Answer 70928:

- QDMA Subsystem for PCI Express v5.0 - PG302,
- QDMA Linux kernel reference driver user guide and
- DPDK driver User guide

System Overview

The system overview is presented in the

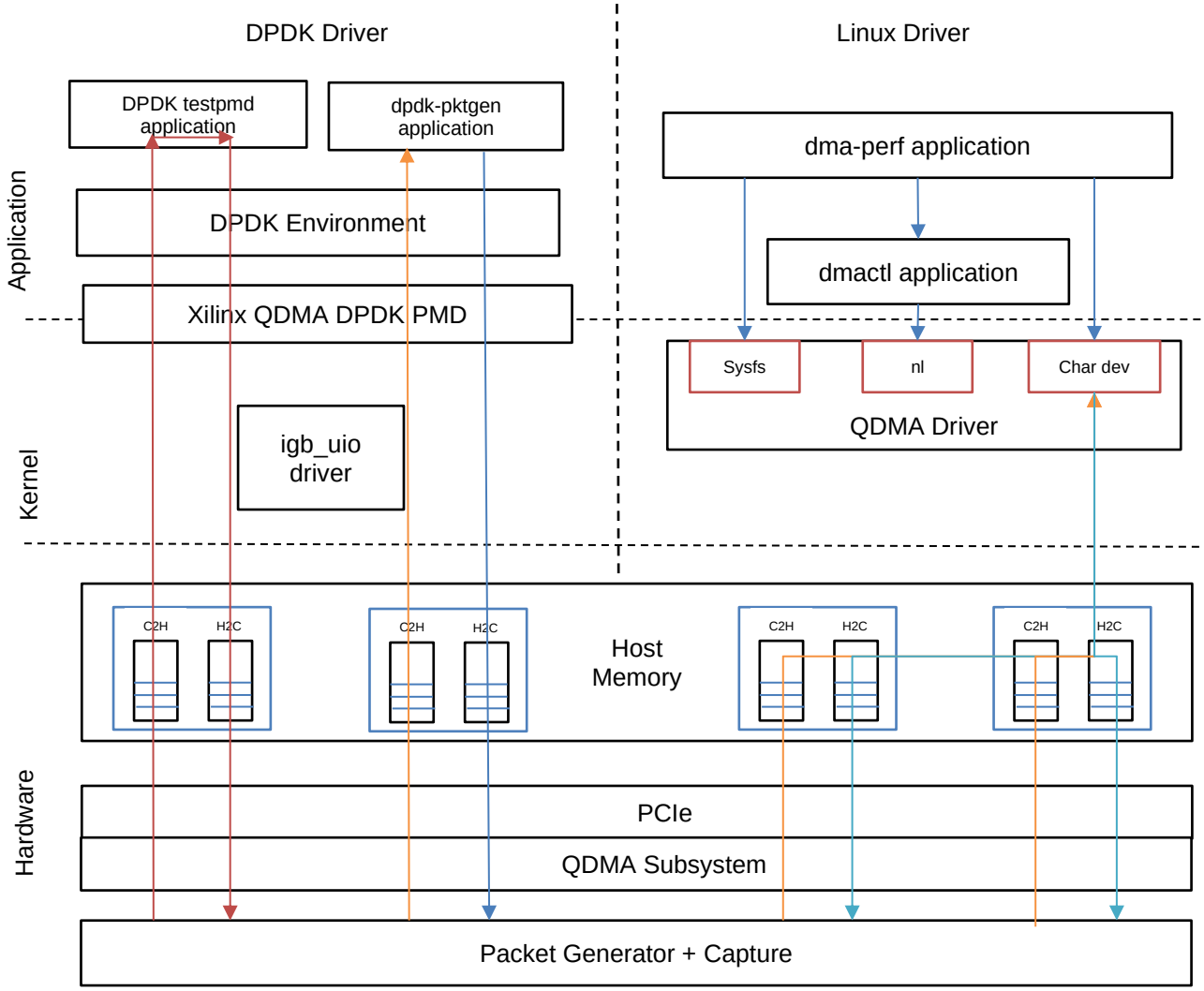


Figure 1: System Diagram

Hardware

Xilinx provides sample reference designs for Streaming (ST) mode and Memory Mapped (MM) mode.

ST performance reference design consists of an AXI Stream-only packet generator in the C2H direction and performance / latency measurement tools in both C2H and H2C directions. The reference design will generate a known data pattern (timestamp) and send a user-specified packet length on the C2H direction when there is an available descriptor. This data pattern can be looped back into the H2C direction by the application and measured for performance and latency. Please refer the Example Design section in QDMA Subsystem for PCI Express v5.0 - PG302 on how to configure the packet generator and read the data collected by the measurement counters through the AXI Lite Master BAR (BAR# 2).

For MM mode BRAM and DDR based reference design are provided. For more information on reference design refer QDMA Subsystem for PCI Express v5.0 - PG302.

For details regarding register maps and the limitations of the design, please refer to the Reference Design RTL.

Software

Linux Kernel Reference Device Driver

The Xilinx Linux kernel reference driver v2023.1.1 is used for collecting the performance numbers.

Xilinx-developed custom tool “dma-perf” is used to collect the performance metrics for unidirectional and bidirectional traffic.

The QDMA Linux kernel reference driver is a PCIe device driver, it manages the QDMA queues in the HW. The driver creates a character device for each queue pair configured,

Standard IO tools such as ‘fio’ can be used for performing IO operations using the char device interface.

However, most of the tools are limited to sending / receiving 1 packet at a time and wait for the processing of the packet to complete, so they are not able to keep the driver/ HW busy enough for performance measurement. Although fio also supports asynchronous interfaces, it does not continuously submit IO requests while polling for the completion parallelly.

To overcome this limitation, Xilinx developed dma-perf tool. It leverages the asynchronous functionality provided by libaio library. Using libaio, an application can submit IO request to the driver and the driver returns the control to the caller immediately (i.e., non-blocking). The completion notification is sent separately, so the application can then poll for the completion and free the buffer upon receiving the completion.

For more information on the dma-perf tools please refer to the QDMA Linux kernel reference driver user guide hosted at QDMA Linux kernel reference driver user guide

DPDK Poll Mode Driver

The Xilinx reference QDMA DPDK 2023.1.1 driver is based on DPDK v22.11. The DPDK driver is tested by binding the PCIe functions with igb_uio kernel driver.

The dpdk-pktgen application is used to perform uni-directional performance measurement and the testpmd application is used for the Bi-directional forwarding performance measurement.

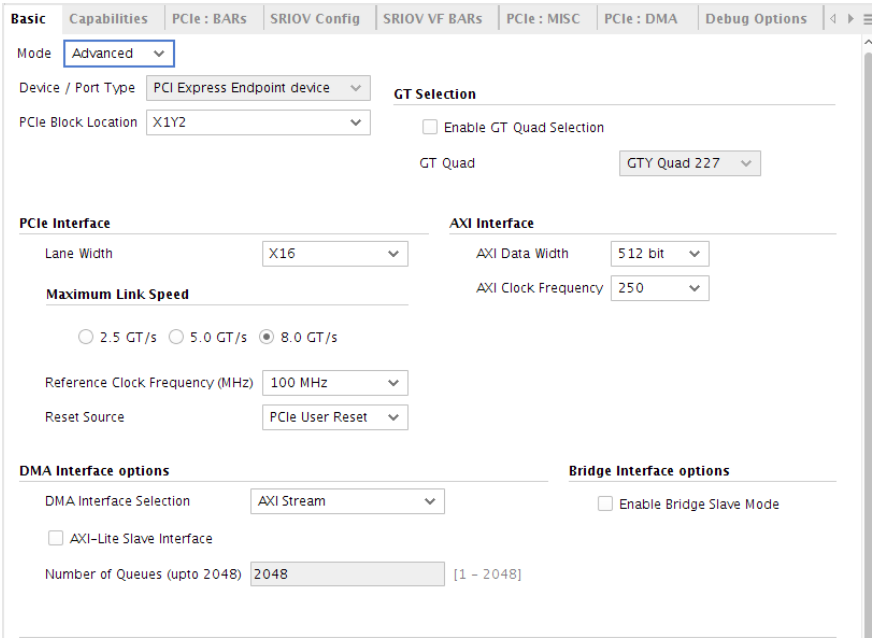
Generating Reference Design

The Reference Design bitfile used in this Performance report is available for immediate download into a VCU1525 design. For users who are using a different card, the Reference Design can be generated by following these steps:

Create a Vivado project and add/configure a QDMA IP with the following settings – All options not mentioned below can be left at their default settings:

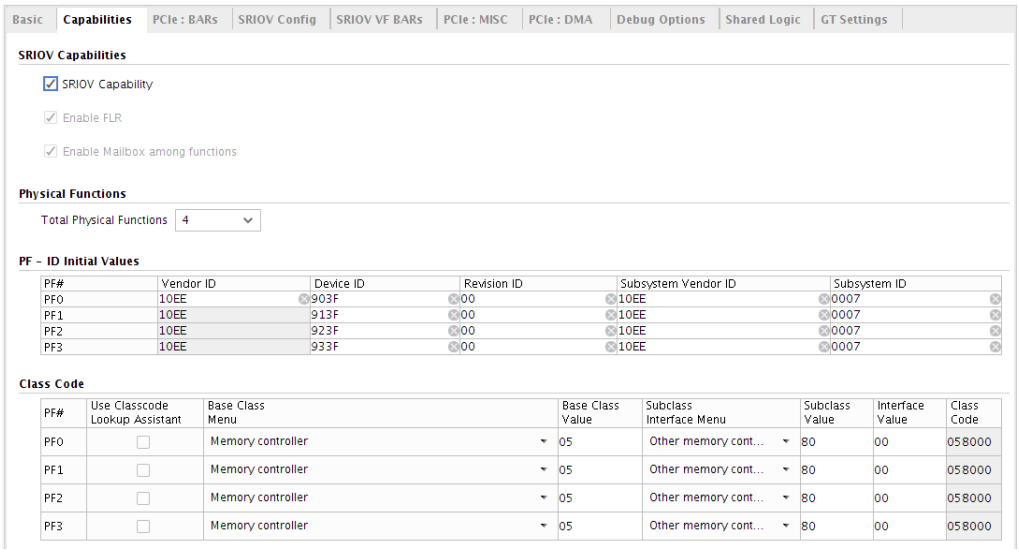
Basic Tab:

- **Mode:** Advanced
  - Lane Width & Link Speed: X16 Gen3 (8.0 GT/s)
  - DMA Interface Selection: AXI Stream



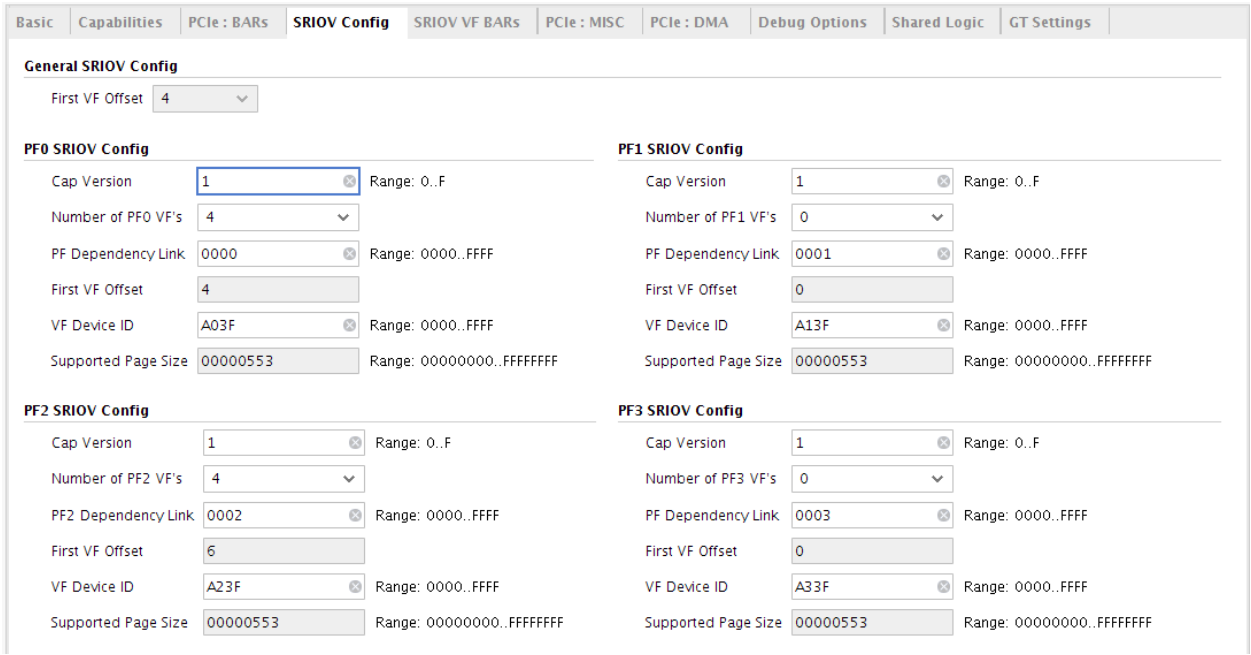
Capabilities Tab:

- Enable SRIOV Capability
- Total Physical Functions: 4



SRIOV Config:

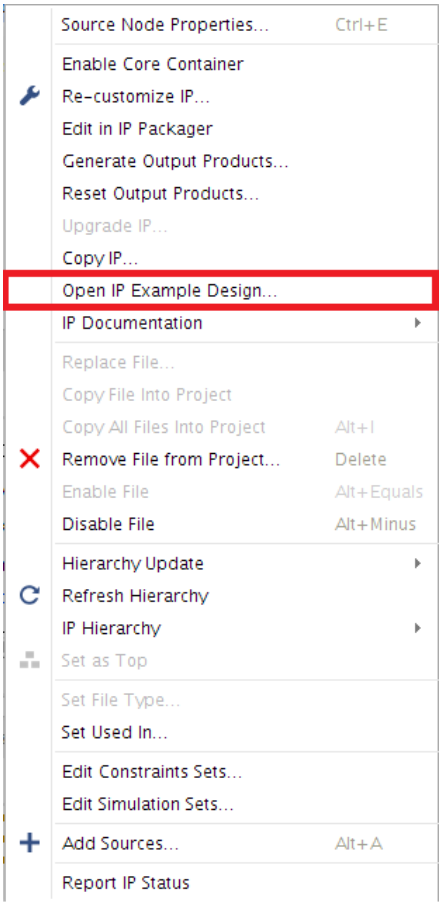
- Number of PF0 VFs: 4
- Number of PF2 VFs: 4



Note: The Reference Design used in this report is an SRIOV capable design with 4PFs and 252VFs. It is not mandatory to enable this feature to use the reference design or achieve the performance reported in this document.

1. Run the following command in the Tcl console to enable Performance Reference Design:
   set_property CONFIG.performance_exdes {true} [get_ips <QDMA_ip_name>]

2. Right click the QDMA IP and choose “Open IP Example Design”



Measurement

For DPDK driver performance analysis, below performance measurements are taken with dpdk-pktgen and testpmd DPDK applications on PF-0 and VF-0 for this report.

- ST Mode DMA Performance of PF-0 on Host (i.e. Run DPDK performance application on the PF-0 in the Host):
  - C2H only DMA performance using dpdk-pktgen application
  - H2C only DMA performance using dpdk-pktgen application
  - Bi-directional (forwarding) DMA performance using testpmd application
- ST Mode DMA Performance of VF-0 on VM (i.e. Run DPDK application on the PF-0 in the Host which is mainly used for mailbox communication and run DPDK performance application on the VF-0 in the VM):
  - C2H only DMA performance using dpdk-pktgen application
  - H2C only DMA performance using dpdk-pktgen application
  - Bi-directional (forwarding) DMA performance using testpmd application

For Linux Kernel Reference Driver performance analysis, below performance measurements are taken with the dma-perf tool on PF-0 for host tests and 1 VF created on PF0 for VM tests with driver in the auto (i.e., interrupt aggregation + poll) mode for this report.

- ST Mode DMA Performance
  - ST-C2H only
  - ST-H2C only
  - ST-H2C & ST-C2H bi-directional
- MM Mode DMA Performance with BRAM Design
  - MM-C2H only
  - MM-H2C only
  - MM-H2C & MM-C2H bi-directional

DMA Overheads

The PCIe bandwidth utilization is higher than DMA bandwidth as this number excludes PCIe protocol overheads. In addition to PCIe overhead, DMA will have its own overhead to communicate with the driver as listed below.

- CIDX update by driver affects C2H and forwarding performance
- PIDX update by driver affects H2C and forwarding performance
- 16B H2C descriptor affects H2C and forwarding performance
- 8B C2H descriptor affects C2H and forwarding performance
- C2H completion can be 8B or 16B or 32B or 64B sent for every packet to pass the meta-data.
- Status descriptor writes affect both C2H and H2C performance
- Memory controller overhead in Memory-mapped mode.

When possible, QDMA reduces various TLP overheads by coalescing reads and writes. QDMA is highly customizable, the overheads can be reduced by customizing the solution to be specific to an application.

DMA Bandwidth Performance Measurement

The packets per second (PPS) numbers reported by the application are noted and the DMA bandwidth performance is calculated as below:

- ***DMA Bandwidth Performance = PPS * DMA Packet size in bytes * 8***

For NIC use case the performance can be extrapolated as follows:

- ***Ethernet Performance = PPS * (DMA Packet size in bytes + Preamble bytes + Inter-frame gap bytes + FCS) * 8***

Every Ethernet packet includes Preamble of 8 bytes, Inter-frame Gap of 12 bytes, FCS of 4 bytes and the DMA packet size can be 4 bytes less than the network packet size as the FCS 4 bytes can be stripped off by the MAC and as a result are not DMA'ed.

Latency Measurement

Latency measurement is calculated using the performance counters provided by the Traffic Generator Reference Design. The reference design maintains the minimum and average latency counters. It determines the time taken for a packet to traverse from the C2H path to the H2C path via the testpmd application using a 64-bit timestamp embedded in the packet.

Test Environment

The test setup is as outlined in **Figure 1**. Table 2 lists the AMD system settings used for the performance measurement.

Item	Description
CPU	AMD EPYC 7302 16-Core Processor
Vendor	Supermicro
Model	H12SSW-NT
No of Sockets	1
No of logical Cores	32
Threads Per Core	2
RAM	64GB (8 x 8GB, Fully populated DIMMS)
DUT	Xilinx VU9P device based VCU1525 board
Performance design	QDMA 5.0 bitstream
PCIe Setting	MPS=256, MRRS=512, Extended Tag Enabled, Relaxed Ordering Enabled
Additional settings (Recommended)	Fully populated memory channels Use the CPU slot on which PCIe slot is used
Other Setting (Recommended)	Tx queue depth = 2048, Rx queue depth = 2048, Packet buffer size = 4096, Burst size = 64
Operating System	Ubuntu 18.04.4 LTS, Kernel 4.15.0-166-generic
Linux Driver Specifc Settings	
Boot setting for Linux driver	iommu=pt amd_iommu=on nohz=off numa_balancing=disable nmi_watchdog=1 audit=0 nosoftlockup hpet=disable tsc=reliable selinux=0 processor.max_cstate=0 pci=realloc
BIOS Version	V1.1
BIOS setting	ACS, IOMMU, ARI, AER enabled. SMU Common Options -> “Determinism Control” set to *Performance*
VM Settings for Linux VF Performance	VM RAM = 32G, Number of cores for VM = 32
DPDK driver specific settings:	
Boot Setting	default_hugepagesz=1GB hugepagesz=1G hugepages=30 iommu=pt amd_iommu=on pci=realloc
DPDK Version	22.11
Performance setting	isolcpus=1-16 Disable iptables/ip6tables service Disable irqbalance service Disable cpuspeed service Point scaling-governor to performance

Table 1: Performance System Settings for AMD setup

There could be some variation in performance with other AMD setups based on system settings.

Table 2 lists the Intel system settings used for the performance measurement.

Item	Description
CPU	Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz
Vendor	Supermicro
odel	X11SPi-TF
No of Sockets	1
Number of Physical Cores	28
Threads Per Core	2
No of logical Cores	56
RAM	48GB (6 x 8GB)
DUT	Xilinx VU9P device based VCU1525 board
PCIe Setting	MPS=256, MRRS=512, Extended Tag Enabled, Relaxed Ordering Enabled
Additional settings (Recommended)	Fully populated memory channels Use the CPU slot on which PCIe slot is used
Other Setting (Recommended)	Tx queue depth = 2048, Rx queue depth = 2048, Packet buffer size = 4096, Burst size = 64
Operating System	Ubuntu 20.04.3 LTS, Kernel 5.4.0-109-generic
Linux Driver Specifc Settings	
Boot Setting	"intel_idle.max_cstate=0 processor.max_cstate=0 intel_pstate=disable rcu_nocb_poll audit=0 pci=realloc nosoftlockup iommu=pt intel_iommu=on"
BIOS Version	2.1
BIOS Settings	ACS, IOMMU, ARI enabled. Power Technology is set to Custom, Power Performance Tuning – OS controls EPB
VM Settings for Linux VF Performance	VM RAM = 32G, Number of cores for VM = 32
DPDK driver specific settings:	
Boot Setting	default_hugepagesz=1GB hugepagesz=1G hugepages=30 iommu=pt intel_iommu=on pci=realloc transparent_hugepages=never isolcpus=0-16 rcu_nocbs=0-16 nohz=on nohz_full=0-16 numa_balancing=disable nmi_watchdog=1 audit=0 nosoftlockup hpet=disable tsc=reliable selinux=0
DPDK Version	22.11
Performance setting	Disable iptables/ip6tables service Disable irqbalance service Disable cpuspeed service Point scaling-governor to performance

Table 2: Performance System Settings for Intel Setup

There could be some variation in performance with other Intel setups based on system settings.

Following are the additional DPDK Performance tuning settings that could be used.

PCIe MRRS

Performance System Settings listed in Table 1 uses PCIe MRRS (Max Read Request) of 512, with which all performance data has been collected. However, depending on the system in use (motherboard, PCIe root ports and its capability, etc.), system specific tuning might be needed. For example, if line-rate is not observed for packet size 4K on a system then, PCIe MRRS could be tuned to 2048.

CPU isolation and additional kernel settings

If the system in use runs additional apps then, it is always good to set aside CPU cores for dpdk workload. Below additional kernel command-line parameters could be added to GRUB boot settings:

```
isolcpus=1-<n> nohz_full=1-<n> rcu_nocbs=1-<n>
```

where:
`isolcpus` isolates cpus 1 to <n> from kernel scheduling so that they are set aside for dedicated tasks like dpdk.
`nohz_full` will put cpus 1 to <n> in adaptive-ticks mode so as not to interrupt them with scheduling-clock interrupts.
`rcu_nocbs` will fence off cpus 1 to <n> from random interruptions of softirq RCU callbacks.

Now, use from these CPUs 1 to <n> in DPDK testpmd, pktgen command-lines to make sure that the DPDK apps use these dedicated CPUs.

Disable CPU power savings from kernel command-line

Sometimes, disabling CPU power savings from BIOS alone may not always make the CPU(s) run on full horse-power. As an additional confirmation, disable power savings from kernel command-line too

```
processor.max_cstate=0 intel_idle.max_cstate=0 intel_pstate=disable
```

Above will disable power savings on CPUs and disable intel_idle as well as intel_pstate cpu frequency scaling driver. Further, always double-confirm from '`cat /proc/cpuinfo | grep -i Mhz`' output that all the intended CPUs are operating at max speed.

NOTE:
1. Above tuning parameters may not always be needed. And one should be thoroughly aware about the system in use, and the kind of apps/workload running on the system before applying any of these parameters.
2. Some parameters are specific to Intel x86-64 and may not work for ARM, PPC or AMD based systems. Always consult respective CPU's manual and related Linux parameters for the same.
3. These parameters were NOT used for the performance numbers published in this guide.

lspci output

```
65:00.0 Memory controller: Xilinx Corporation Device 903f
        Subsystem: Xilinx Corporation Device 0007
        Control: I/O+ Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr+ Stepping- SERR+ FastB2B- DisINTx+
        Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort- >SERR- <PERR- INTx-
        Latency: 0, Cache Line Size: 32 bytes
        Interrupt: pin A routed to IRQ 308
        Region 0: Memory at 38bffff60000 (64-bit, prefetchable) [size=128K]
        Region 2: Memory at 38bffffd3000 (64-bit, prefetchable) [size=4K]
        Capabilities: [40] Power Management version 3
                Flags: PMEClk- DSI- D1- D2- AuxCurrent=0mA PME(D0-,D1-,D2-,D3hot-,D3cold-)
                Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-
        Capabilities: [60] MSI-X: Enable+ Count=8 Masked-
                Vector table: BAR=0 offset=00010000
                PBA: BAR=0 offset=00014000
        Capabilities: [70] Express (v2) Endpoint, MSI 00
                DevCap: MaxPayload 1024 bytes, PhantFunc 0, Latency L0s <64ns, L1 <1us
                        ExtTag+ AttnBtn- AttnInd- PwrInd- RBE+ FLReset+ SlotPowerLimit 0.000W
                DevCtl: Report errors: Correctable+ Non-Fatal+ Fatal+ Unsupported-
                        RlxdOrd+ ExtTag+ PhantFunc- AuxPwr- NoSnoop+ FLReset-
                        MaxPayload 256 bytes, MaxReadReq 512 bytes
                DevSta: CorrErr+ UncorrErr- FatalErr- UnsuppReq+ AuxPwr- TransPend+
                LnkCap: Port #0, Speed 8GT/s, Width x16, ASPM not supported, Exit Latency L0s unlimited, L1 unlimited
                        ClockPM- Surprise- LLActRep- BwNot- ASPMOptComp+
                LnkCtl: ASPM Disabled; RCB 64 bytes Disabled- CommClk+
                        ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-
                LnkSta: Speed 8GT/s, Width x16, TrErr- Train- SlotClk+ DLActive- BWMgmt- ABWMgmt-
                DevCap2: Completion Timeout: Range BC, TimeoutDis+, LTR-, OBFF Not Supported
                DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis-, LTR-, OBFF Disabled
                LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-
                         Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-
                         Compliance De-emphasis: -6dB
                LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+, EqualizationPhase1+
                         EqualizationPhase2+, EqualizationPhase3+, LinkEqualizationRequest-
        Capabilities: [100 v1] Advanced Error Reporting
                UESta:  DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq- ACSViol-
                UEMsk:  DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq+ ACSViol-
                UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO- CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+ ECRC- UnsupReq- ACSViol-
                CESta:  RxErr- BadTLP- BadDLLP- Rollover- Timeout- NonFatalErr+
                CEMsk:  RxErr- BadTLP- BadDLLP- Rollover- Timeout- NonFatalErr+
                AERCap: First Error Pointer: 00, GenCap- CGenEn- ChkCap- ChkEn-
        Capabilities: [140 v1] Single Root I/O Virtualization (SR-IOV)
                IOVCap: Migration-, Interrupt Message Number: 000
                IOVCtl: Enable- Migration- Interrupt- MSE- ARIHierarchy+
                IOVSta: Migration-
                Initial VFs: 4, Total VFs: 4, Number of VFs: 0, Function Dependency Link: 00
                VF offset: 4, stride: 1, Device ID: a03f
                Supported Page Size: 00000553, System Page Size: 00000001
                Region 0: Memory at 000038bffffb0000 (64-bit, prefetchable)
                Region 2: Memory at 000038bffffcc000 (64-bit, prefetchable)
                VF Migration: offset: 00000000, BIR: 0
        Capabilities: [180 v1] Alternative Routing-ID Interpretation (ARI)
                ARICap: MFVC- ACS-, Next Function: 1
                ARICtl: MFVC- ACS-, Function Group: 0
        Capabilities: [1c0 v1] #19
        Kernel driver in use: igb_uio
```

Figure 2: lspci output of the PCIe function being tested

QDMA Settings

The QDMA IP is highly configurable. This section lists only a subset of the available settings limited to the tests carried out in this report.

Configuration Option	Description
Number of Queues	The QDMA IP supports up to 2048 queues. The number of queues for a given test are specified when starting the software application. ***Benchmarking is done for 1, 2, 4 and 8 queues.***
Packet Size	Tests accept a range of packet sizes along with a packet size increment. ***Benchmarking is done with packet size in the range of 64B to 4KB for streaming queue performance and 64B to 32KB for memory mapped queue performance***
Completion Descriptor size	Completion queue descriptors can be configured to 8-byte, 16-byte, 32-byte or 64-byte. ***Benchmarking is done with 16B descriptor format.***
Descriptor Prefetch	Prefetch causes descriptors to be opportunistically prefetched so that descriptors are available before the packet is received. ***Benchmarking is done with prefetch enabled***.
Prefetch Cache depth	Prefetch cache depth is selectable from Vivado when building the design. Supported values are 8, 16, 32, 64. The Prefetch cache can support that many active queues at any given time. ***Benchmarking is done with prefetch cache depth set to 64.***
Completion Coalesce Buffer depth	Completion coalesce buffer depth is selectable from Vivado when building the design. Supported values are 8, 16, 32. ***Benchmarking is done with completion coalesce buffer depth set to 32.***

Table 3: QDMA Settings

Performance Benchmark Results

DPDK Driver

This section provides the performance results captured using DPDK driver in streaming mode using the customized bitstream provided in release package.

QDMA currently has a limitation that the packet buffers be aligned to 256 bytes boundary for optimal DMA performance. Since the mbuf data pointers in DPDK need not be aligned to 256 bytes boundary, the higher packet size performance for DPDK reported below is slightly lower than that reported for Linux driver. This alignment limitation in QDMA IP will be fixed in future IP releases.

Streaming Mode C2H and H2C performance test

Below dpdk-pktgen command-lines were used for performance measurement.

- The '-9' option is the extension added by Xilinx to enable dpdk-pktgen to support packet sizes beyond 1518 bytes.
- The dpdk-pktgen application was also modified to disable the packet classification.

The '-a' EAL option is specified to enable or disable prefetch and to change the completion descriptor length.
In the table below, 3b:00.0 represents PCIe function in "bus:device.function" format.

# of queues	dpdk-pktgen command line
1	./build/app/pktgen -l 0-2 -n 4 -a 3b:00.0,desc_prefetch=1,cmpt_desc_len=16 -- -P -m "[1:2].0" -9
2	./build/app/pktgen -l 0-4 -n 4 -a 3b:00.0,desc_prefetch=1,cmpt_desc_len=16 -- -P -m "[1-2:3-4].0" -9
4	./build/app/pktgen -l 0-8 -n 4 -a 3b:00.0,desc_prefetch=1,cmpt_desc_len=16 -- -P -m "[1-4:5-8].0" -9
8	./build/app/pktgen -l 0-16 -n 4 -a 3b:00.0,desc_prefetch=1,cmpt_desc_len=16 -- -P -m "[1-8:9-16].0" -9

Table 4: Command-line for dpdk-pktgen application

For H2C performance tests the C2H traffic is disabled and H2C packets are generated using dpdk-pktgen application. The EAL option (-a) is ***not*** required to be specified in the command lines.

Streaming Mode Forwarding performance test

The testpmd application is executed with the below command-line options for different queue configurations.

# of queues	testpmd command line

1	./build/app/testpmd -cf -n4 -a 3b:00.0,desc_prefetch=1,cmpt_desc_len=16 -- -i --nb-cores=2 --rxq=1 --txq=1 --rxd=2048 --txd=2048 --burst=64 --mbuf-size=4224
2	./build/app/testpmd -cff -n4 -a 3b:00.0,desc_prefetch=1,cmpt_desc_len=16 -- -i --nb-cores=3 --rxq=2 --txq=2 --rxd=2048 --txd=2048 --burst=64 --mbuf-size=4224
4	./build/app/testpmd -cfff -n4 -a 3b:00.0,desc_prefetch=1,cmpt_desc_len=16 -- -i --nb-cores=5 --rxq=4 --txq=4 --rxd=2048 --txd=2048 --burst=64 --mbuf-size=4224
8	./build/app/testpmd -cffff -n4 -a 3b:00.0,desc_prefetch=1,cmpt_desc_len=16 -- -i --nb-cores=9 --rxq=8 --txq=8 --rxd=2048 --txd=2048 --burst=64 --mbuf-size=4224

Table 5: Command-line for testpmd application

QDMA Performance metrics on AMD System

PF Performance

ST C2H Performance

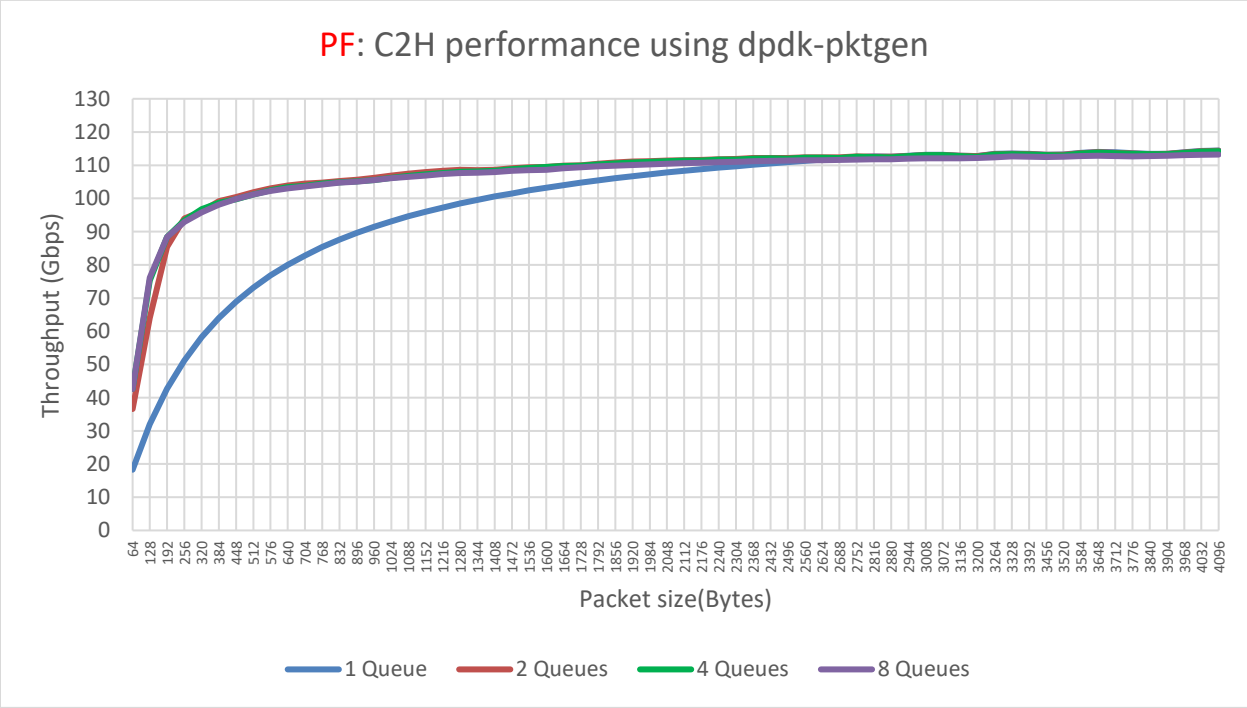


Figure 3: DPDK Driver – QDMA5.0 PF ST C2H performance in Gbps

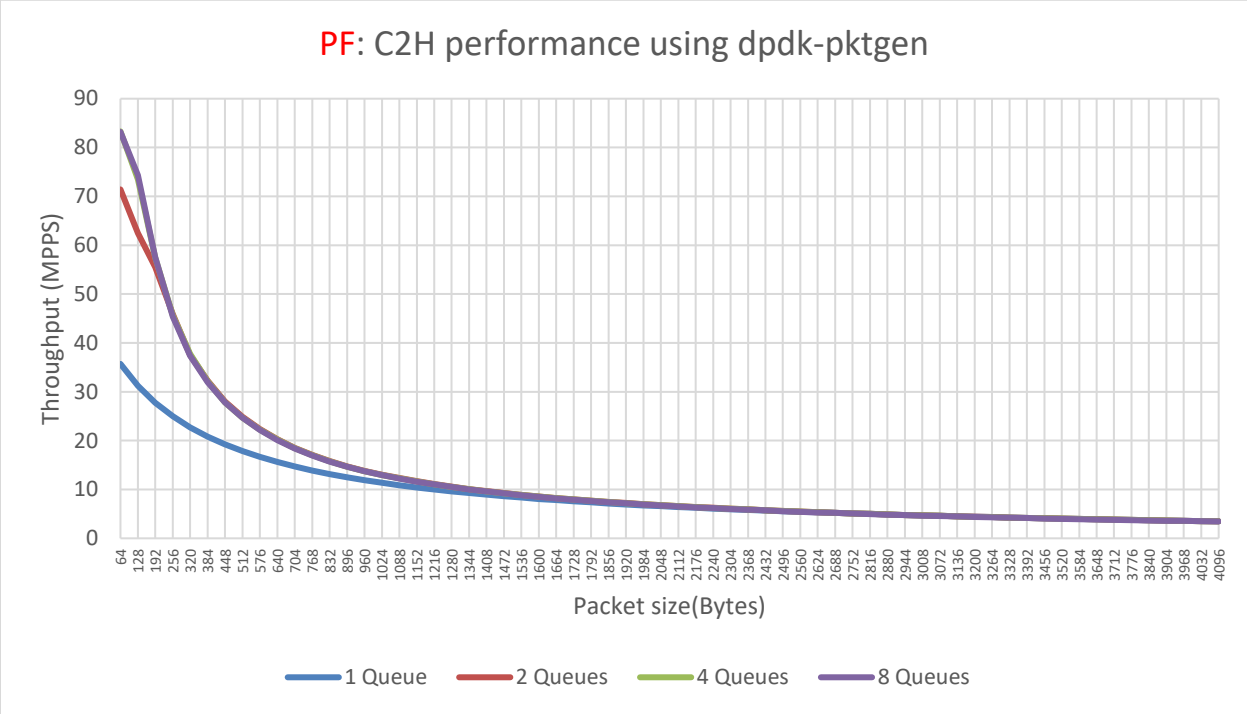


Figure 4: DPDK Driver – QDMA5.0 PF ST C2H performance in Mpps

ST H2C Performance

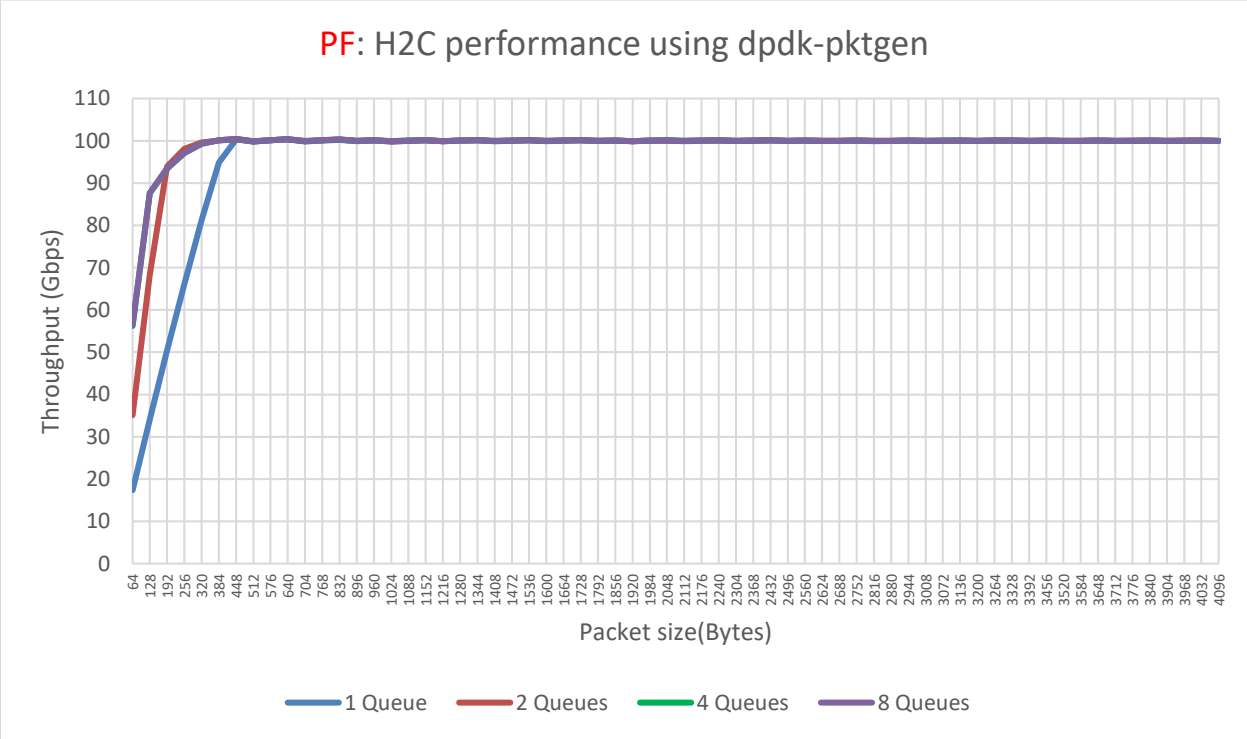


Figure 5: DPDK Driver – QDMA5.0 PF ST H2C Performance in Gbps

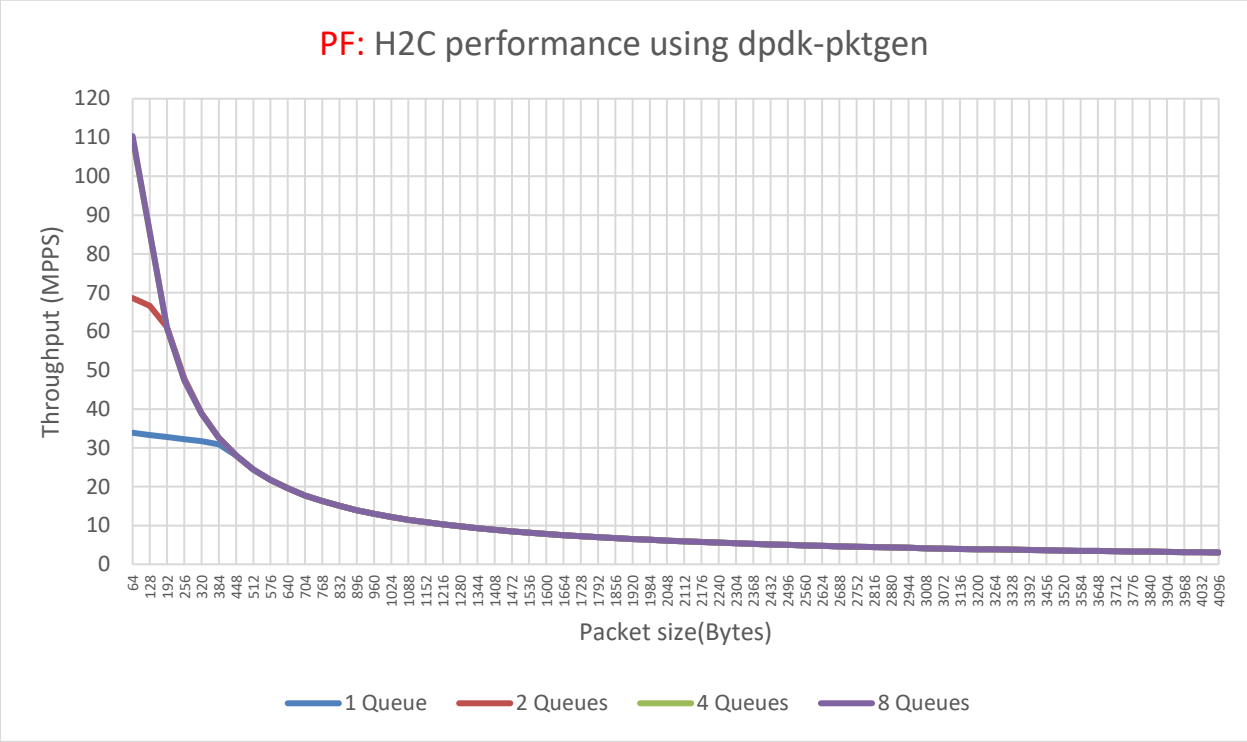


Figure 6: DPDK Driver – QDMA5.0 PF ST H2C Performance in Mpps

ST Forwarding Performance

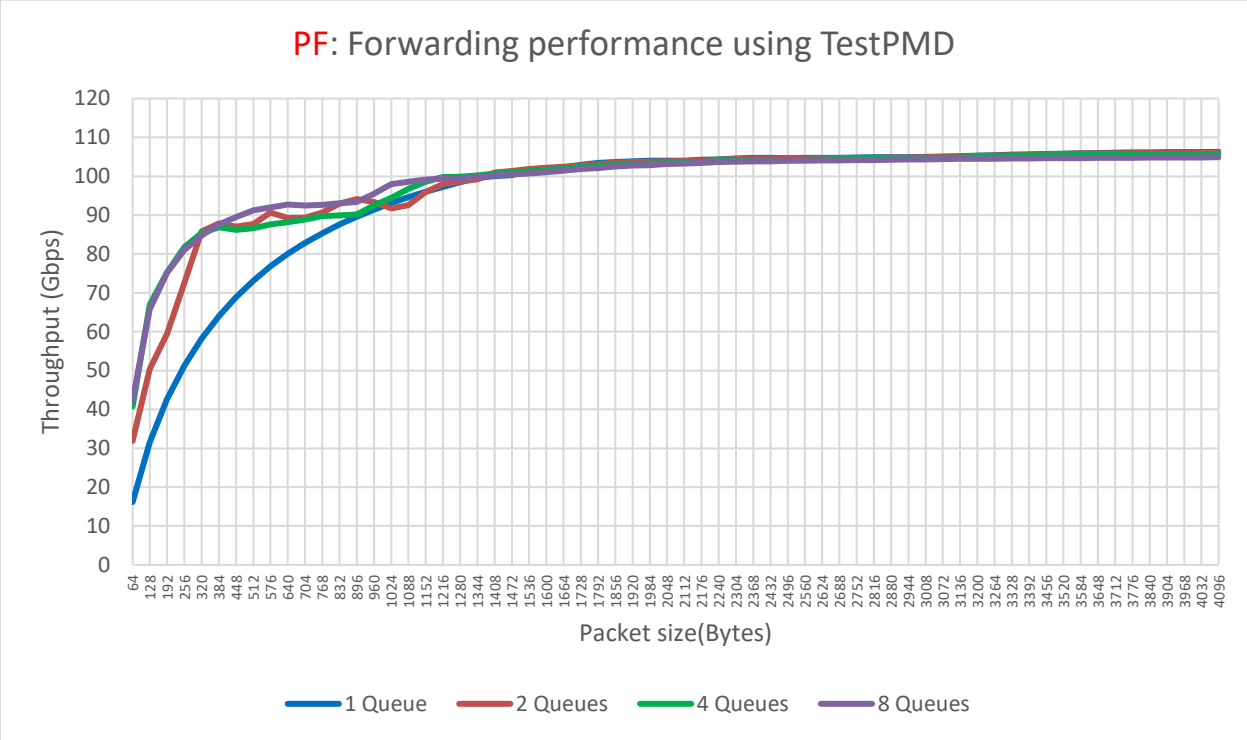


Figure 7: DPDK Driver – QDMA5.0 PF Forwarding performance in Gbps

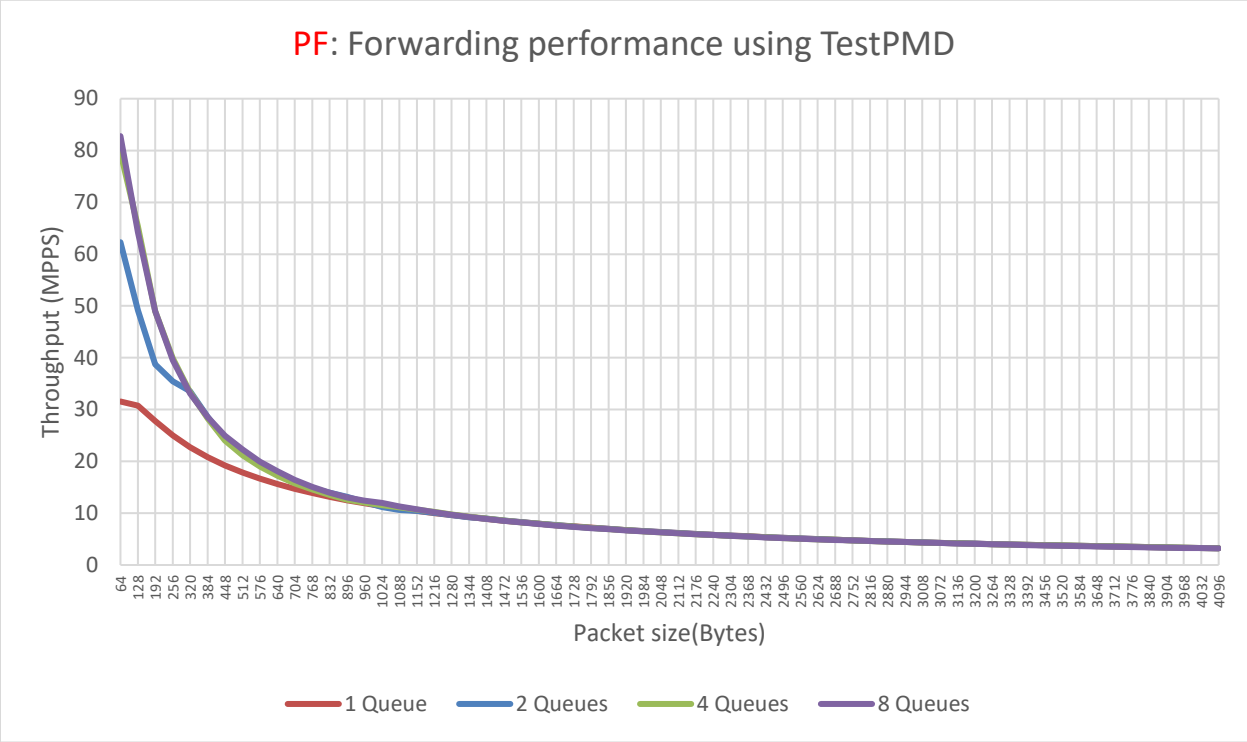


Figure 8: DPDK Driver – QDMA5.0 PF Forwarding performance in Mpps

Packet Size (Bytes)	8 queues		4 queues		2 queues		1 queue	
	Packet rate (Mpps)	Throughput (Gbps)	Packet rate (Mpps)	Throughput (Gbps)	Packet rate (Mpps)	Throughput (Gbps)	Packet rate (Mpps)	Throughput (Gbps)
64	82.78	42.38	79.63	40.77	62.30	31.90	31.56	16.16
128	64.26	65.81	65.35	66.91	49.17	50.35	30.75	31.49
192	48.95	75.18	48.98	75.23	38.72	59.47	27.77	42.65
256	39.55	81.00	39.91	81.73	35.43	72.55	25.00	51.20
320	33.10	84.74	33.36	85.40	33.52	85.80	22.73	58.18
384	28.52	87.63	28.27	86.84	28.59	87.82	20.83	64.00
448	24.98	89.53	24.05	86.19	24.29	87.07	19.23	68.92
512	22.28	91.25	21.15	86.65	21.42	87.73	17.86	73.14
576	19.97	92.01	19.01	87.60	19.67	90.64	16.67	76.80
640	18.11	92.71	17.23	88.19	17.44	89.29	15.63	80.00
704	16.41	92.44	15.78	88.85	15.86	89.34	14.71	82.82
768	15.08	92.67	14.60	89.72	14.75	90.64	13.89	85.33
832	13.98	93.05	13.51	89.90	13.97	92.99	13.16	87.58
896	13.02	93.34	12.58	90.20	13.13	94.14	12.50	89.60
960	12.44	95.55	12.06	92.59	12.16	93.38	11.90	91.43
1024	11.96	97.98	11.53	94.48	11.20	91.73	11.36	93.09
1088	11.32	98.55	11.11	96.74	10.64	92.59	10.87	94.61
1152	10.75	99.11	10.69	98.53	10.41	95.95	10.42	96.00

1216	10.22	99.39	10.26	99.78	10.08	98.01	10.00	97.28
1280	9.71	99.40	9.76	99.92	9.63	98.66	9.62	98.46
1344	9.28	99.76	9.32	100.25	9.23	99.24	9.26	99.56
1408	8.90	100.22	8.94	100.74	8.96	100.98	8.88	100.02
1472	8.53	100.47	8.58	101.06	8.61	101.40	8.52	100.33
1536	8.20	100.72	8.24	101.25	8.29	101.82	8.27	101.65
1600	7.90	101.07	7.94	101.63	7.98	102.17	7.97	101.96
1664	7.62	101.47	7.66	102.02	7.70	102.44	7.68	102.30
1728	7.37	101.83	7.40	102.36	7.43	102.74	7.44	102.90
1792	7.12	102.12	7.16	102.67	7.19	103.06	7.22	103.44
1856	6.90	102.50	6.93	102.92	6.97	103.47	6.98	103.69
1920	6.69	102.79	6.71	103.11	6.75	103.68	6.76	103.86
1984	6.48	102.87	6.51	103.28	6.54	103.78	6.55	103.99
2048	6.30	103.14	6.31	103.38	6.34	103.83	6.35	103.99
2112	6.11	103.29	6.13	103.49	6.15	103.88	6.16	104.02
2176	5.94	103.46	5.96	103.67	5.98	104.10	5.99	104.21
2240	5.78	103.64	5.79	103.81	5.82	104.23	5.82	104.33
2304	5.63	103.73	5.64	103.99	5.66	104.40	5.67	104.55
2368	5.48	103.80	5.50	104.12	5.52	104.56	5.53	104.73
2432	5.34	103.84	5.35	104.17	5.38	104.58	5.38	104.71
2496	5.21	103.97	5.22	104.20	5.24	104.56	5.24	104.69
2560	5.08	104.00	5.09	104.26	5.11	104.60	5.11	104.72
2624	4.96	104.06	4.97	104.33	4.98	104.63	4.99	104.75
2688	4.84	104.11	4.85	104.38	4.87	104.68	4.87	104.77
2752	4.73	104.18	4.74	104.40	4.76	104.73	4.76	104.81
2816	4.63	104.20	4.64	104.45	4.65	104.75	4.65	104.87
2880	4.53	104.26	4.54	104.50	4.55	104.80	4.55	104.91
2944	4.43	104.30	4.44	104.57	4.45	104.85	4.46	104.94
3008	4.34	104.34	4.35	104.64	4.36	104.90	4.36	104.99
3072	4.25	104.39	4.26	104.74	4.27	104.99	4.28	105.07
3136	4.16	104.46	4.18	104.85	4.19	105.08	4.19	105.17
3200	4.08	104.47	4.10	104.97	4.11	105.21	4.11	105.30
3264	4.00	104.50	4.02	105.07	4.03	105.33	4.04	105.41
3328	3.93	104.55	3.96	105.33	3.96	105.42	3.96	105.53
3392	3.85	104.58	3.88	105.38	3.89	105.52	3.89	105.62
3456	3.78	104.62	3.81	105.41	3.82	105.62	3.82	105.73
3520	3.72	104.65	3.74	105.44	3.75	105.69	3.76	105.84
3584	3.65	104.68	3.68	105.47	3.69	105.87	3.69	105.92
3648	3.59	104.74	3.61	105.49	3.63	105.90	3.63	105.98
3712	3.53	104.73	3.55	105.52	3.57	105.92	3.57	106.07
3776	3.47	104.75	3.49	105.55	3.51	105.96	3.51	106.16
3840	3.41	104.79	3.44	105.56	3.45	105.96	3.46	106.17
3904	3.36	104.80	3.38	105.58	3.39	105.99	3.40	106.19

3968	3.30	104.83	3.33	105.61	3.34	106.01	3.35	106.21
4032	3.25	104.86	3.28	105.64	3.29	106.05	3.29	106.25
4096	3.20	104.91	3.22	105.67	3.24	106.07	3.24	106.28

Table 6: DPDK Driver – QDMA5.0 PF Forwarding performance test results

VF Performance

ST C2H Performance

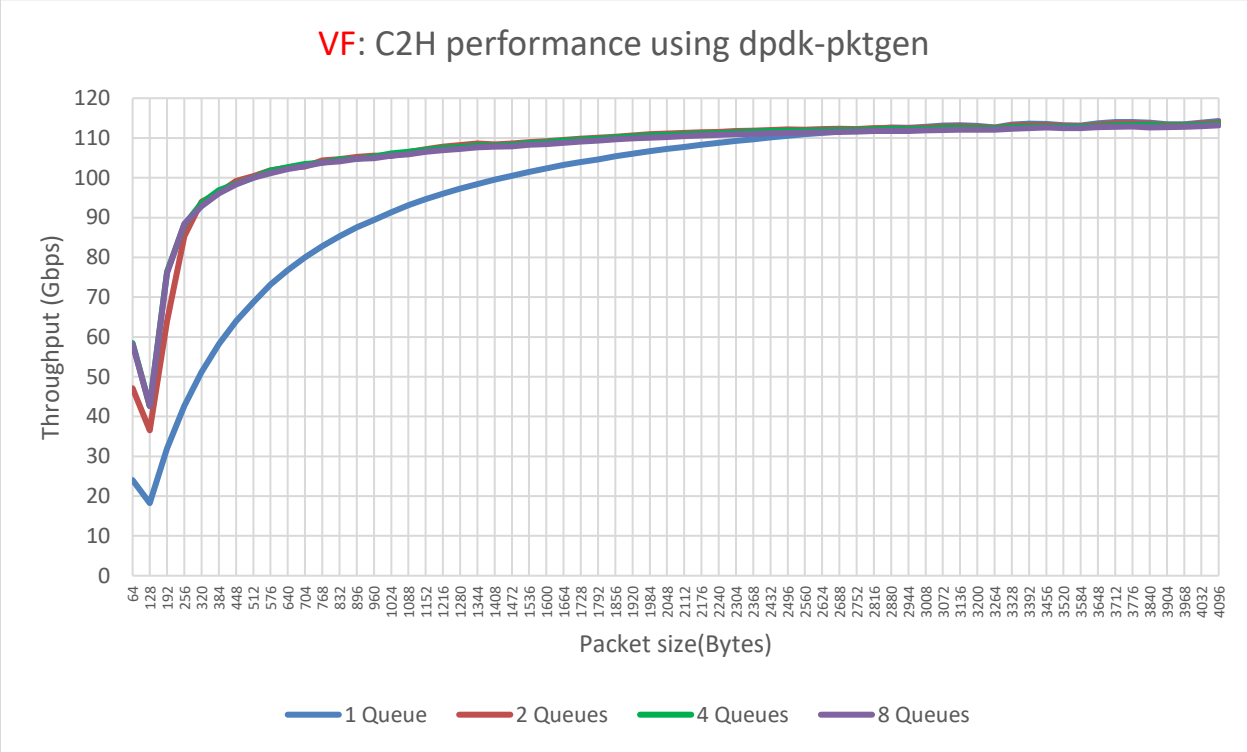


Figure 9: DPDK Driver – QDMA5.0 VF ST C2H performance in Gbps

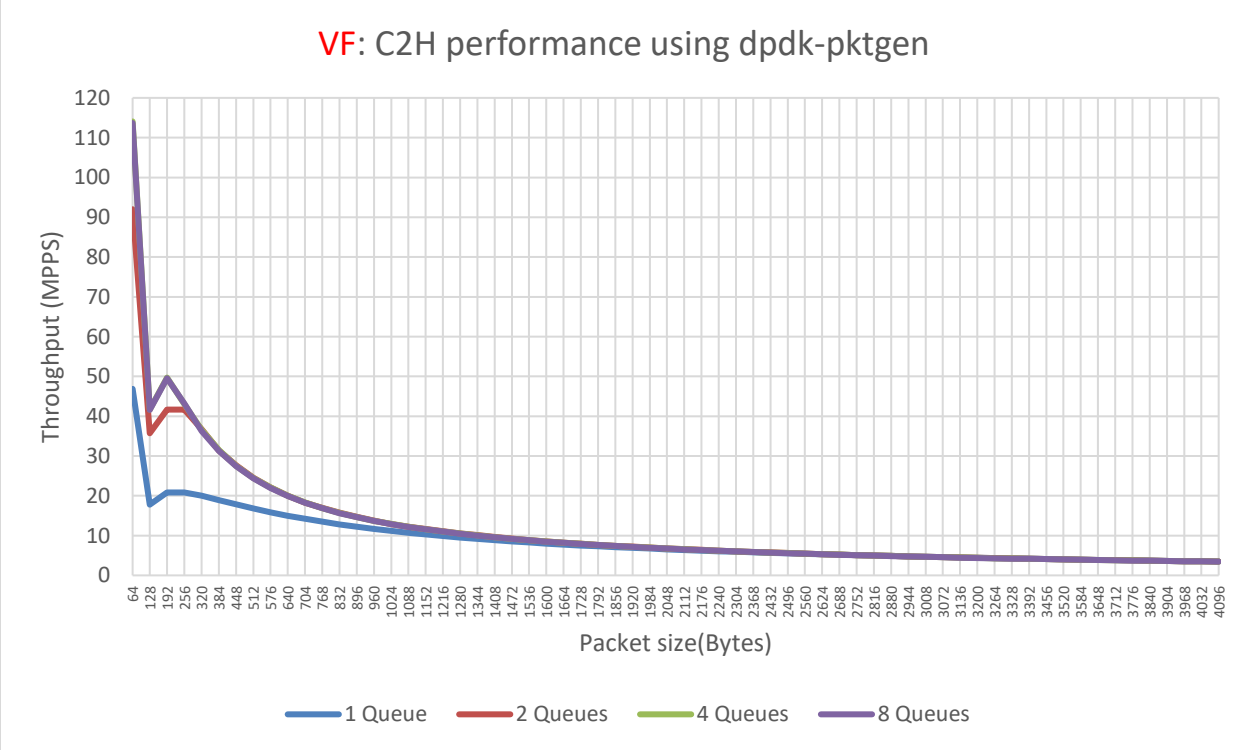


Figure 10: DPDK Driver – QDMA5.0 VF ST C2H performance in Mpps

ST H2C Performance

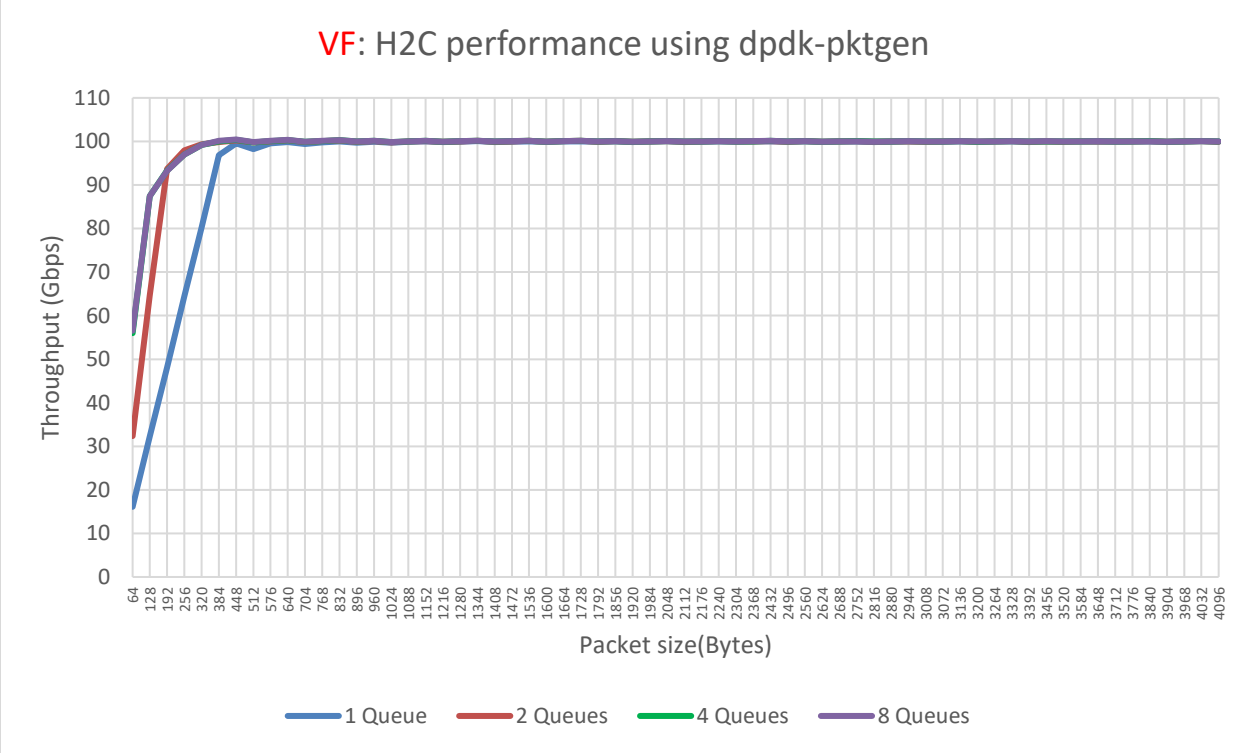


Figure 11: DPDK Driver – QDMA5.0 VF ST H2C Performance in Gbps

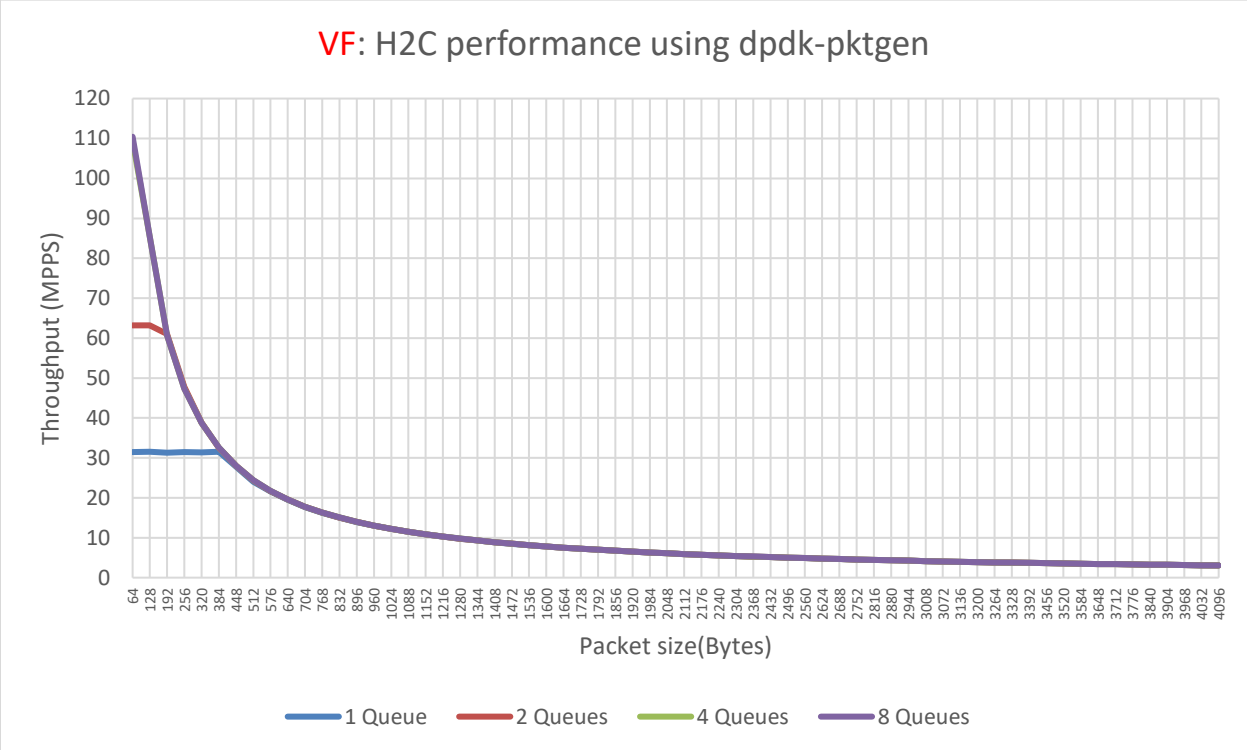


Figure 12: DPDK Driver – QDMA5.0 VF ST H2C Performance in Mpps

QDMA Performance metrics on Intel System

PF Performance

ST C2H Performance

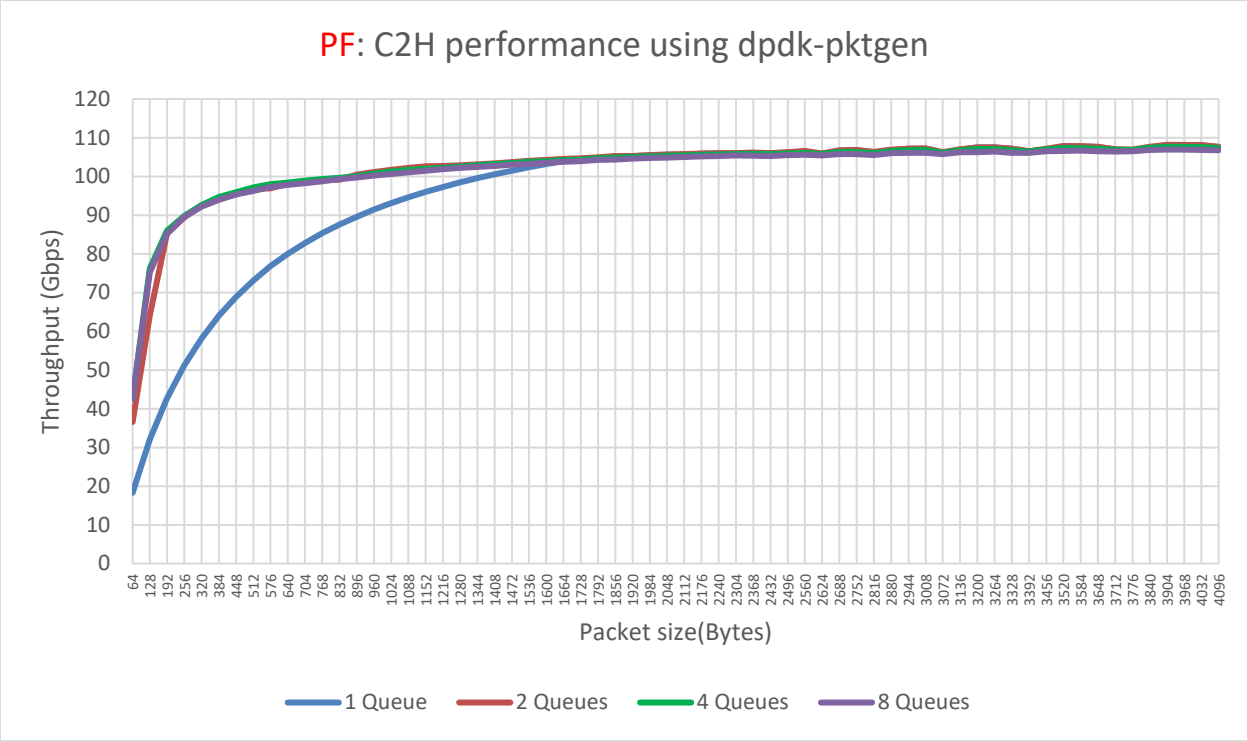


Figure 13: DPDK Driver – QDMA5.0 PF ST C2H performance in Gbps

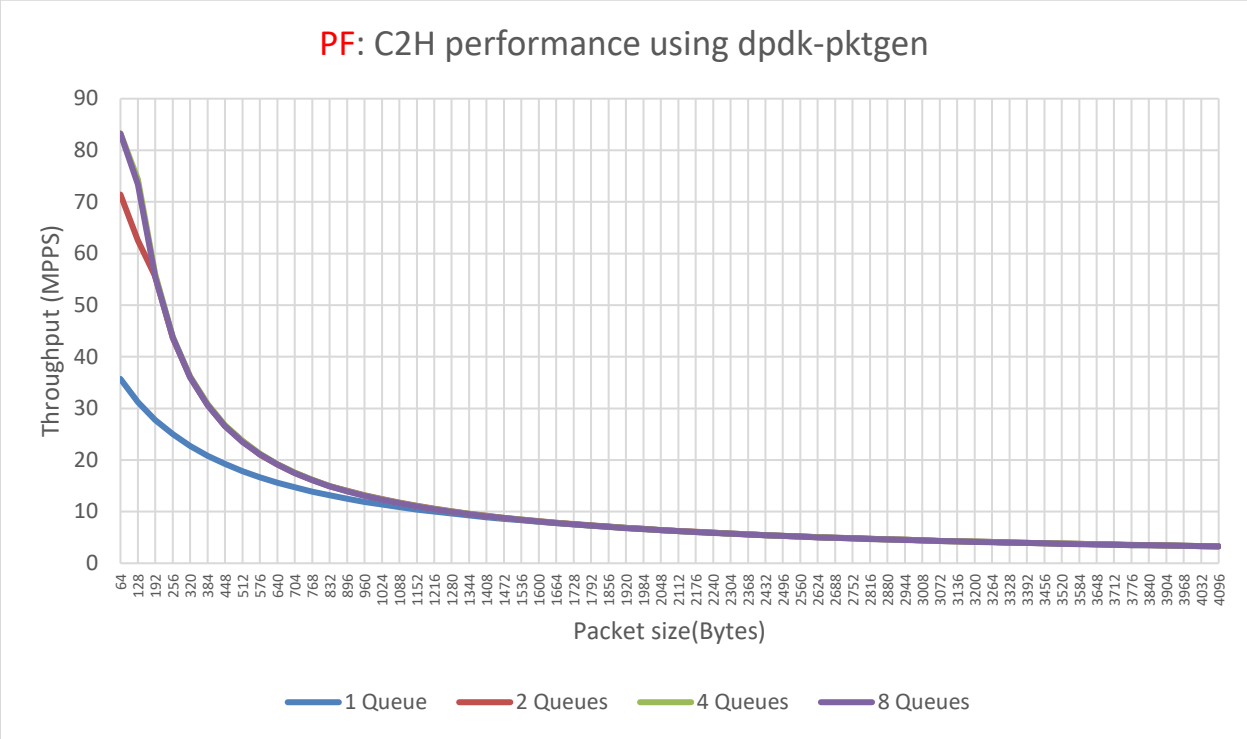


Figure 14: DPDK Driver – QDMA5.0 PF ST C2H performance in Mpps

ST H2C Performance

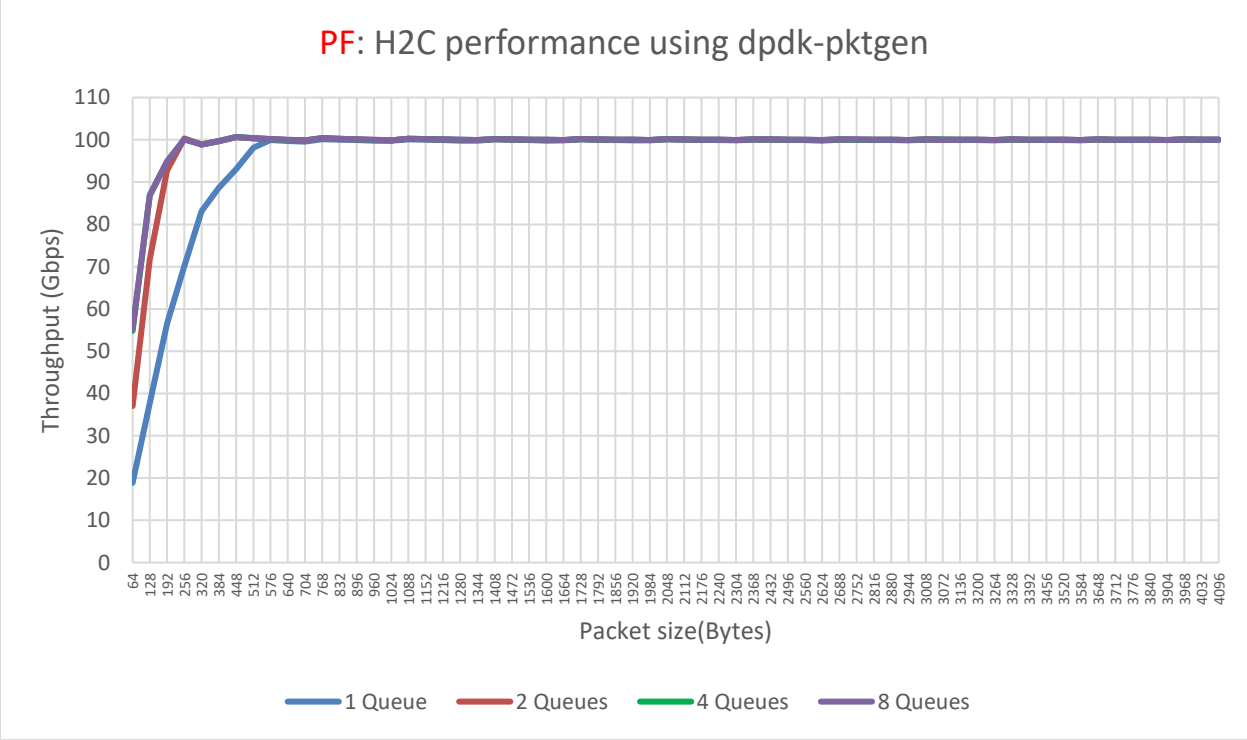


Figure 15: DPDK Driver – QDMA5.0 PF ST H2C Performance in Gbps

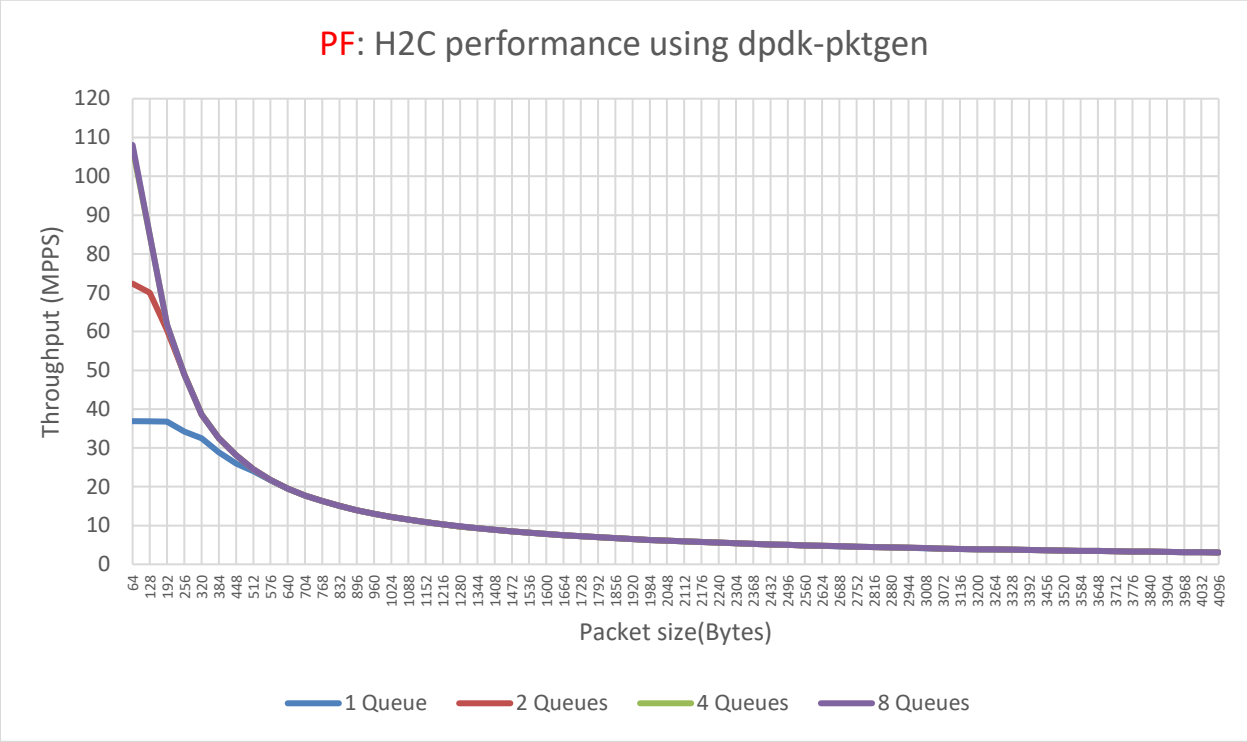


Figure 16: DPDK Driver – QDMA5.0 PF ST H2C Performance in Mpps

ST Forwarding Performance

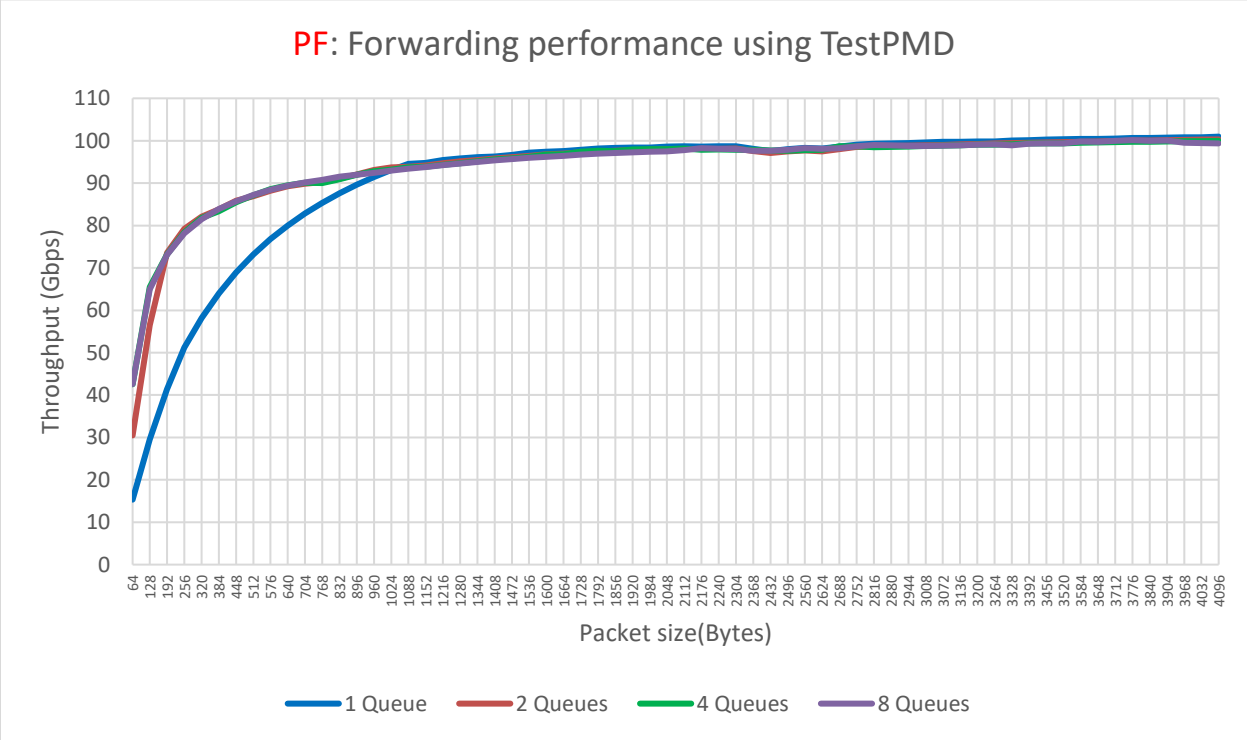


Figure 17: DPDK Driver – QDMA5.0 PF Forwarding performance in Gbps

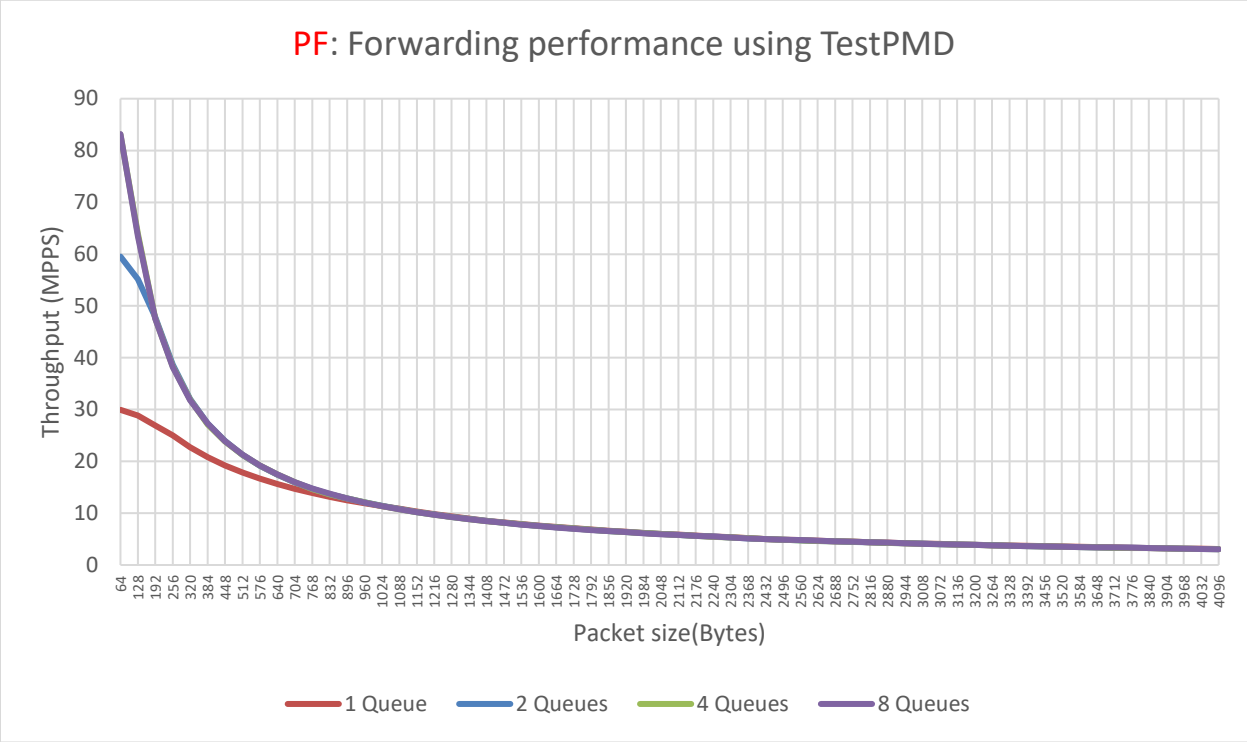


Figure 18: DPDK Driver – QDMA5.0 PF Forwarding performance in Mpps

Packet Size (Bytes)	8 queues		4 queues		2 queues		1 queue	
	Packet rate (Mpps)	Throughput (Gbps)	Packet rate (Mpps)	Throughput (Gbps)	Packet rate (Mpps)	Throughput (Gbps)	Packet rate (Mpps)	Throughput (Gbps)
64	83.17	42.58	83.09	42.54	59.53	30.48	29.95	15.33
128	63.41	64.93	63.94	65.47	55.18	56.51	28.82	29.52
192	47.58	73.08	47.64	73.18	47.87	73.53	26.96	41.40
256	38.17	78.17	38.28	78.39	38.69	79.24	25.00	51.20
320	31.82	81.46	31.93	81.75	32.05	82.05	22.73	58.18
384	27.32	83.92	27.13	83.34	27.28	83.79	20.83	64.00
448	23.92	85.74	23.85	85.48	23.96	85.86	19.23	68.92
512	21.29	87.22	21.27	87.13	21.22	86.91	17.86	73.14
576	19.18	88.40	19.22	88.58	19.14	88.21	16.67	76.80
640	17.46	89.37	17.48	89.51	17.43	89.22	15.62	80.00
704	16.01	90.18	15.99	90.08	15.96	89.88	14.71	82.82
768	14.78	90.80	14.65	90.03	14.69	90.25	13.89	85.33
832	13.75	91.51	13.66	90.93	13.68	91.04	13.16	87.58
896	12.83	91.97	12.83	91.95	12.84	92.05	12.50	89.60
960	12.04	92.46	12.08	92.79	12.13	93.14	11.90	91.42
1024	11.35	92.99	11.38	93.19	11.44	93.73	11.36	93.07
1088	10.73	93.38	10.77	93.73	10.78	93.84	10.86	94.51
1152	10.18	93.82	10.19	93.88	10.22	94.15	10.28	94.78

1216	9.69	94.27	9.70	94.32	9.73	94.65	9.81	95.44
1280	9.24	94.62	9.25	94.72	9.29	95.11	9.36	95.84
1344	8.84	94.99	8.85	95.15	8.88	95.45	8.94	96.16
1408	8.46	95.34	8.48	95.56	8.51	95.84	8.55	96.27
1472	8.12	95.64	8.14	95.84	8.16	96.14	8.21	96.67
1536	7.81	95.94	7.83	96.18	7.85	96.42	7.91	97.21
1600	7.52	96.20	7.55	96.70	7.56	96.77	7.61	97.43
1664	7.24	96.41	7.27	96.80	7.28	96.96	7.33	97.58
1728	7.00	96.73	7.05	97.45	7.03	97.23	7.08	97.86
1792	6.76	96.93	6.81	97.64	6.80	97.52	6.85	98.18
1856	6.54	97.11	6.57	97.56	6.58	97.64	6.62	98.33
1920	6.33	97.23	6.37	97.92	6.37	97.77	6.41	98.38
1984	6.14	97.42	6.18	98.04	6.17	97.87	6.20	98.42
2048	5.95	97.51	5.98	98.04	5.98	97.98	6.02	98.60
2112	5.79	97.81	5.81	98.16	5.80	98.05	5.84	98.68
2176	5.64	98.21	5.62	97.84	5.63	98.09	5.66	98.61
2240	5.47	98.10	5.46	97.93	5.48	98.11	5.51	98.71
2304	5.32	98.05	5.31	97.88	5.33	98.17	5.35	98.67
2368	5.15	97.64	5.17	97.89	5.15	97.57	5.18	98.07
2432	5.02	97.64	5.02	97.74	4.99	97.08	5.01	97.57
2496	4.90	97.87	4.89	97.66	4.88	97.45	4.91	97.98
2560	4.79	98.20	4.78	97.80	4.77	97.75	4.80	98.33
2624	4.67	98.10	4.66	97.83	4.64	97.49	4.68	98.17
2688	4.57	98.20	4.59	98.66	4.56	98.02	4.59	98.63
2752	4.48	98.67	4.48	98.71	4.48	98.53	4.50	99.08
2816	4.39	98.96	4.37	98.45	4.38	98.64	4.41	99.27
2880	4.29	98.93	4.28	98.55	4.29	98.76	4.31	99.36
2944	4.19	98.75	4.19	98.62	4.20	98.85	4.22	99.43
3008	4.10	98.75	4.10	98.77	4.11	98.95	4.14	99.56
3072	4.02	98.88	4.02	98.84	4.03	99.03	4.06	99.73
3136	3.94	98.95	3.94	98.92	3.95	99.15	3.98	99.77
3200	3.87	99.04	3.87	99.05	3.88	99.26	3.90	99.82
3264	3.80	99.12	3.79	99.08	3.80	99.35	3.82	99.80
3328	3.72	98.92	3.72	99.17	3.73	99.41	3.76	100.02
3392	3.66	99.29	3.66	99.34	3.67	99.54	3.69	100.14
3456	3.59	99.36	3.59	99.37	3.60	99.57	3.63	100.25
3520	3.53	99.34	3.53	99.39	3.54	99.67	3.56	100.36
3584	3.48	99.83	3.47	99.49	3.48	99.76	3.50	100.40
3648	3.42	99.77	3.41	99.57	3.42	99.85	3.44	100.44
3712	3.37	99.96	3.36	99.65	3.36	99.89	3.38	100.50
3776	3.31	100.13	3.30	99.72	3.31	100.02	3.33	100.63
3840	3.26	100.01	3.25	99.78	3.26	100.04	3.28	100.69
3904	3.20	100.09	3.20	99.82	3.21	100.14	3.23	100.76

3968	3.14	99.52	3.15	99.89	3.16	100.17	3.18	100.81
4032	3.08	99.47	3.10	99.93	3.11	100.25	3.12	100.79
4096	3.03	99.34	3.05	99.97	3.06	100.31	3.08	100.97

Table 7: DPDK Driver – QDMA5.0 PF Forwarding performance test results

VF Performance

ST C2H Performance

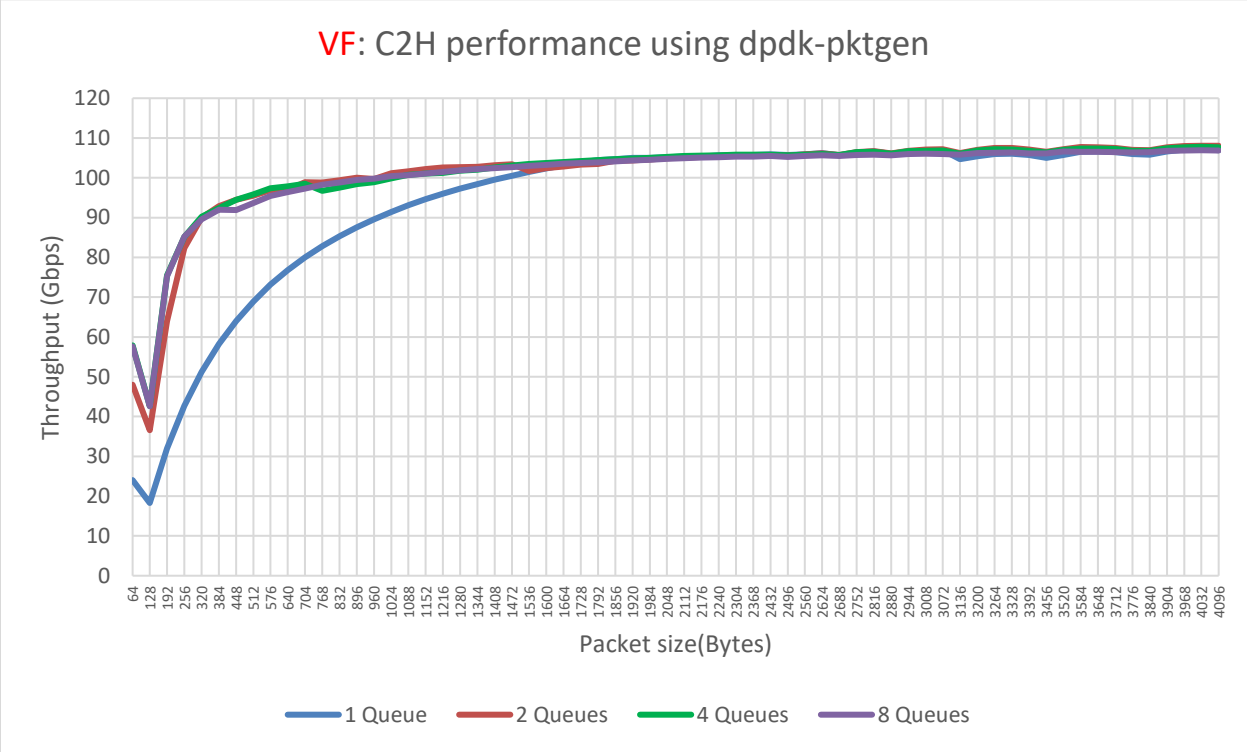


Figure 19: DPDK Driver – QDMA5.0 VF ST C2H performance in Gbps

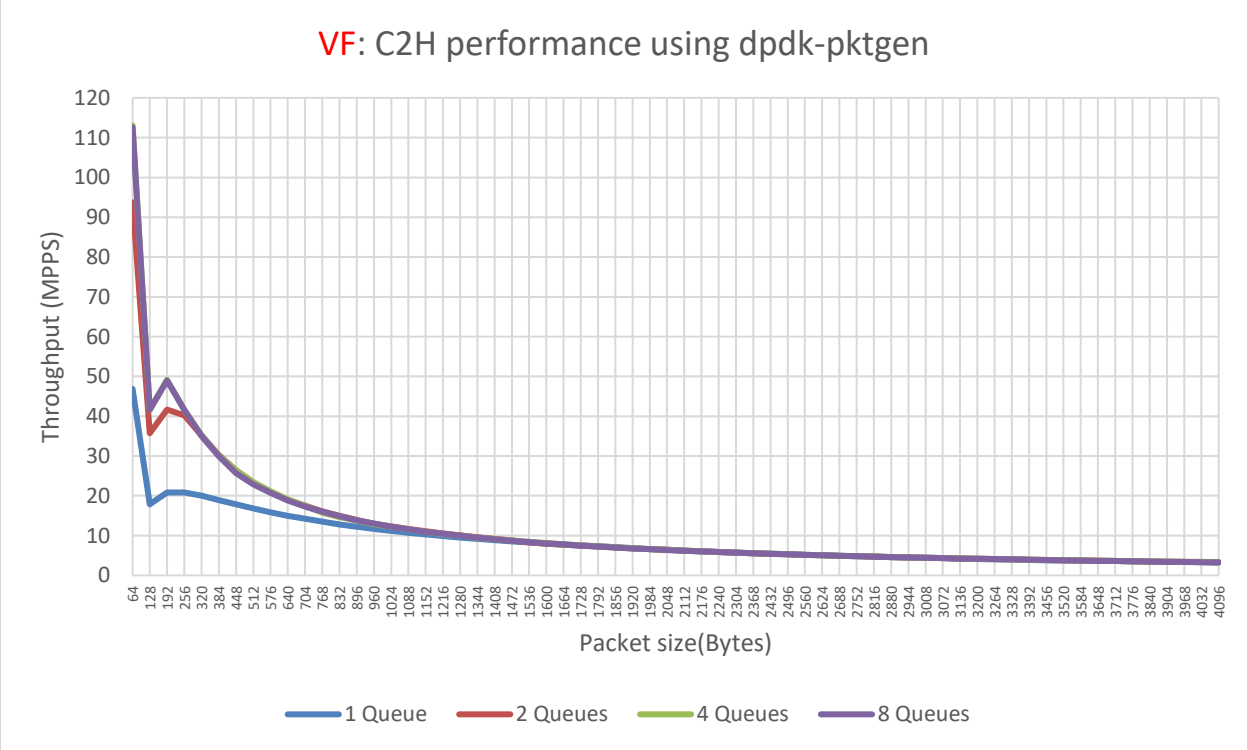


Figure 20: DPDK Driver – QDMA5.0 VF ST C2H performance in Mpps

ST H2C Performance

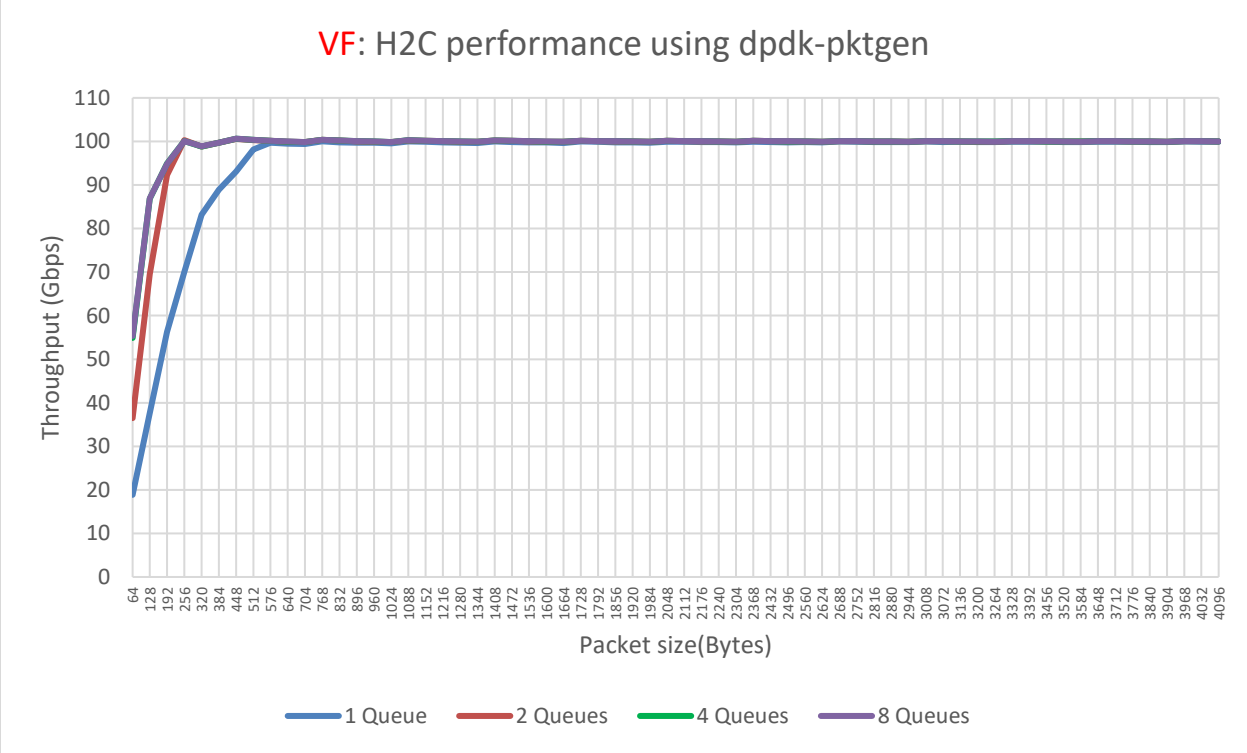


Figure 21: DPDK Driver – QDMA5.0 VF ST H2C Performance in Gbps

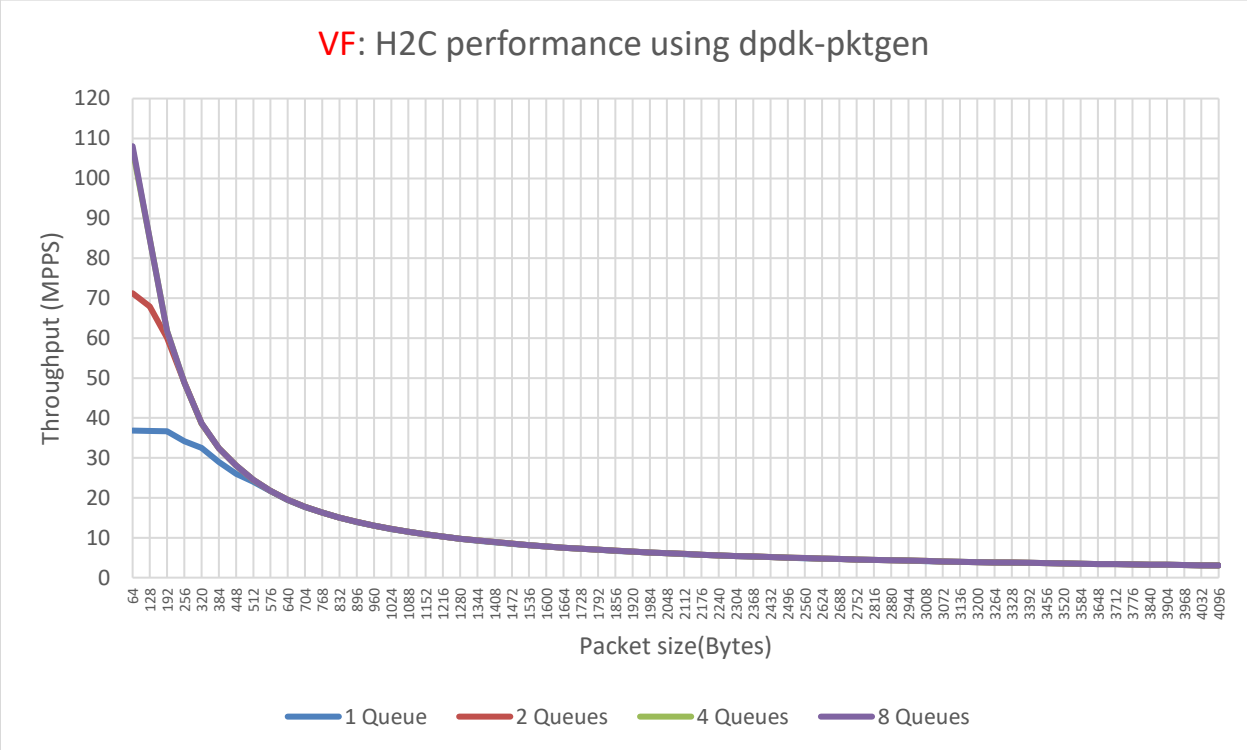


Figure 22: DPDK Driver – QDMA5.0 VF ST H2C Performance in Mpps

Latency Measurements

The provided Reference Design and Bitfile can be used to measure latency in any system when traffic is ongoing. When it is enabled, C2H data payload will be replaced with a known counter value (as a timestamp) and will be measured on the H2C side once the testpmd application has looped the data back. The difference in value between the data payload received at the H2C side and the current counter value will be the sum of C2H and H2C latency.

Latency measurement can be done by following these steps:

- Set the number of clock cycles within each **Measurement window** (see register offset below). The counters will gather data within this time window and take a snapshot of the result for users to read. Default value is 1s (0xEE6B280).
    - **Note: The u**ser must make sure to wait long enough for the measurement window to fill up completely after reset or in between readings before reading the next counter values, otherwise zero or the previous value will be returned.
    - All eight (8) counters must be read at least once, or reset through the Control register, before a new reading will be presented
- Set the mode bit [1] in **Control** (see register offset below) to 1 to allow continuous packet measurement. A value of 0 is currently not supported (reserved).
- Set the reset bit [0] in **Control** (see register offset below) to 1 and then 0 to reset the counters and start measurement.

The module will have four different measurement counters:

- **Max_latency**: Max latency number measured within the measurement window.
- **Min_latency:** Min latency number measured within the measurement window.
- **Sum_latency:** Sum of all latency numbers measured within the measurement window.
- **Pkt_rcvd:** Number of packets received within the measurement window.

Note: Average latency can be measured by taking the sum_latency divided by pkt_rcvd.

Latency Counters Register Offset:

- **0x104:** Measurement window [63:32]
- **0x100:** Measurement window [31:0]
- **0x108:** Control
- **0x110:** Max_latency [63:32]
- **0x10C:** Max_latency [31:0]
- **0x118:** Min_latency [63:32]
- **0x114:** Min_latency [31:0]
- **0x120:** Sum_latency [63:32]
- **0x11C:** Sum_latency [31:0]
- **0x128:** Pkt_rcvd [63:32]
- **0x124:** Pkt_rcvd [31:0]

Linux Kernel Reference Driver

The data below are collected with indirect interrupt (i.e., interrupt aggregation) mode.

Streaming Mode Performance

The dma-perf config files used for the below streaming mode tests are part of the linux reference kernel driver source, hosted at GitHub https://github.com/Xilinx/dma_ip_drivers, under directory QDMA/linux-kernel/apps/dma-perf/dmaperf_config

- C2H unidirectional: st-c2h-pfetch1.zip
- H2C unidirectional: st-h2c.zip
- C2H & H2C bi-directional: st-bi.zip

QDMA Performance metrics on AMD System

PF Performance

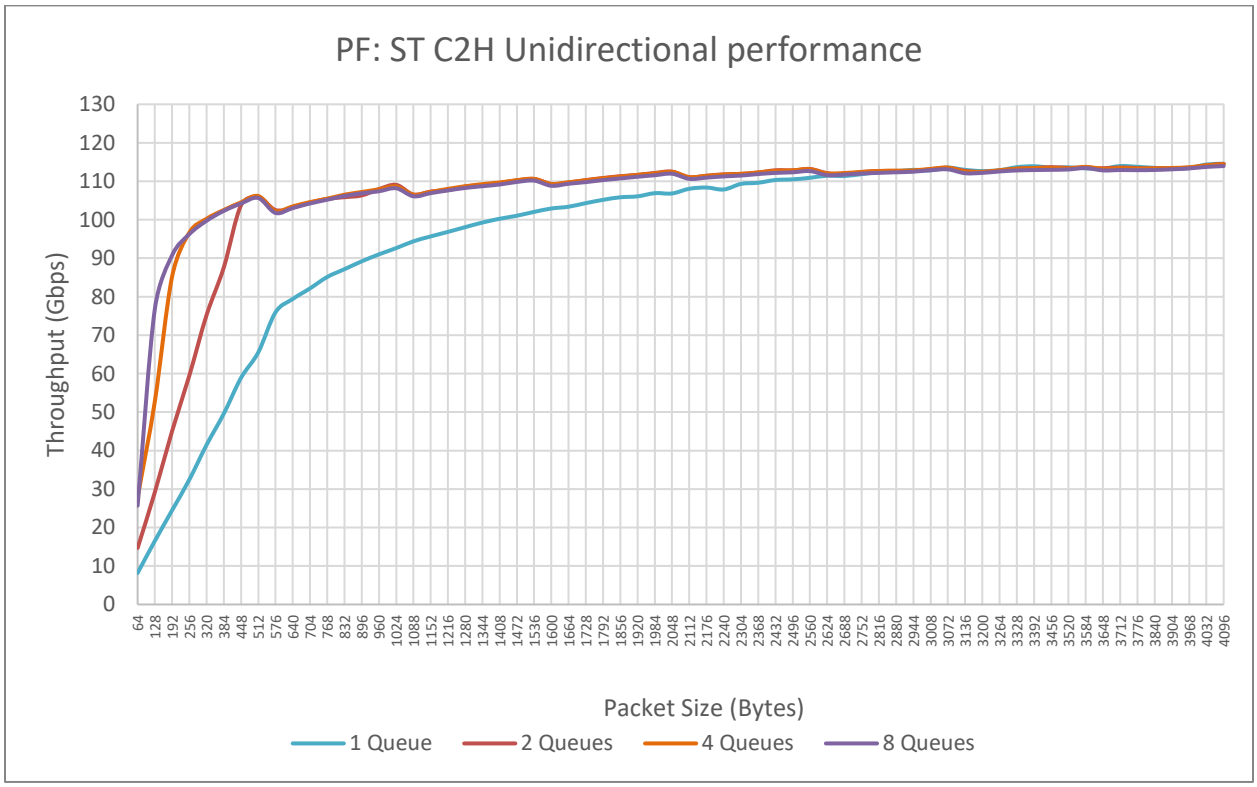


Figure 23: Linux Kernel Reference Driver – QDMA5.0 ST C2H Unidirectional Performance

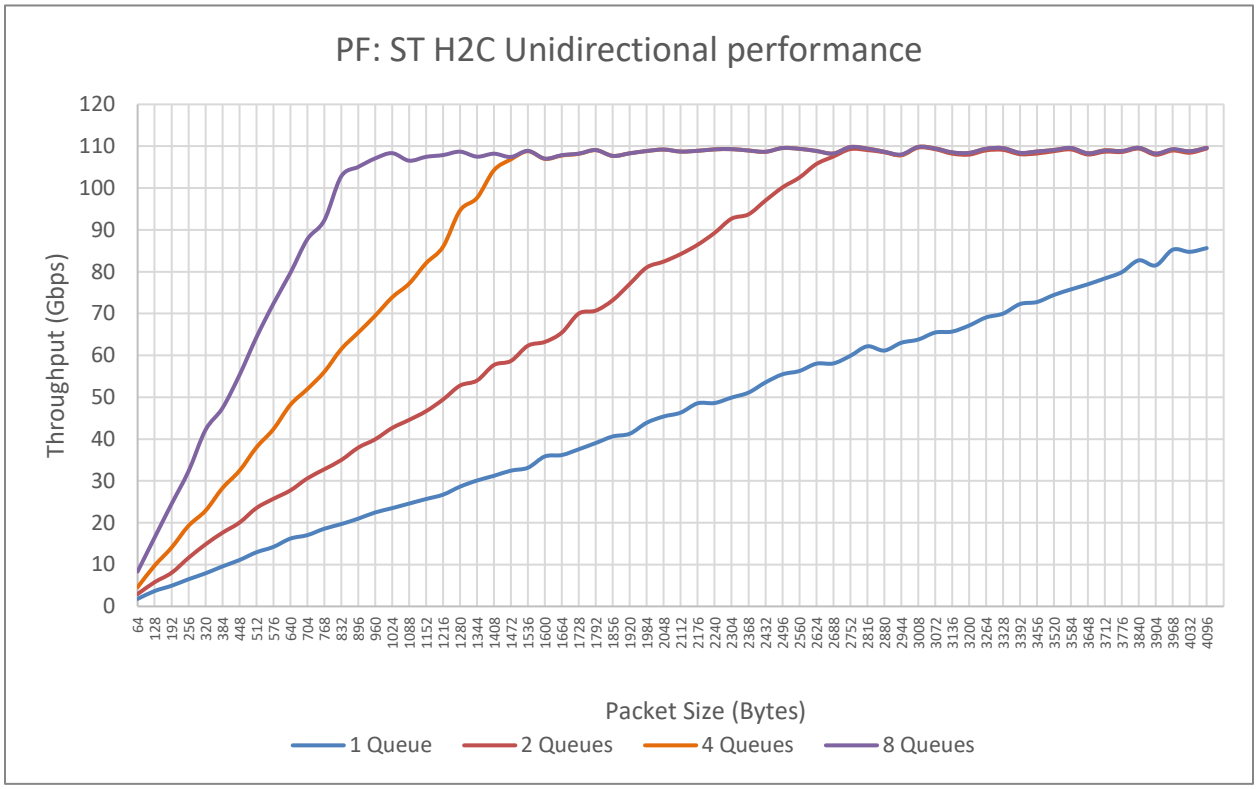


Figure 24 Linux Kernel Reference Driver – QDMA5.0 ST H2C Unidirectional performance

The above H2C graph shows the QDMA IP can achieve line rate at small packet size (with 8 queues). When less number of queues are involved the results are not optimal because there are not enough IO requests in flight to fill the pipeline, especially in the single queue scenario. The “dma-perf” tool and the driver are still being optimized for these cases.

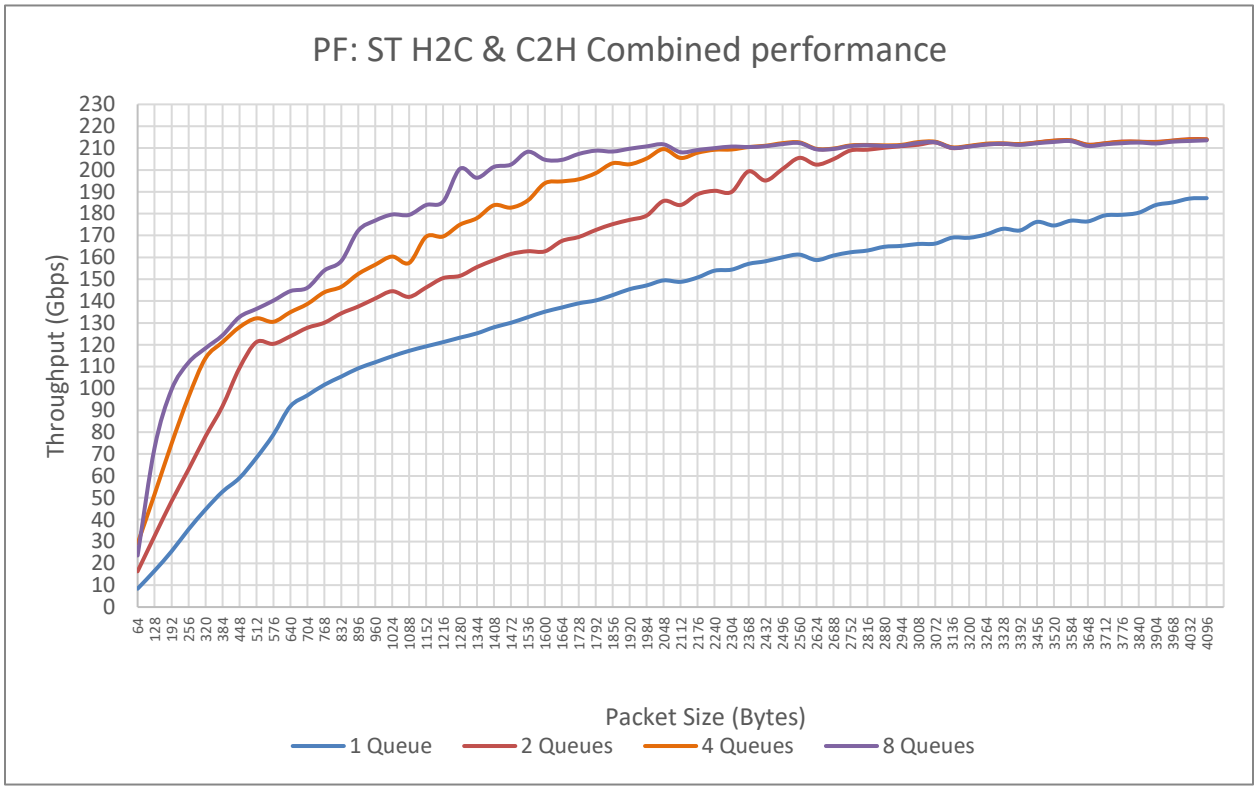


Figure 25: Linux Kernel Reference Driver – QDMA5.0 ST combined performance with Bidirectional traffic

Bi-directional ST performance numbers are taken with traffic being enabled in both H2C and C2H direction simultaneously.

VF Performance

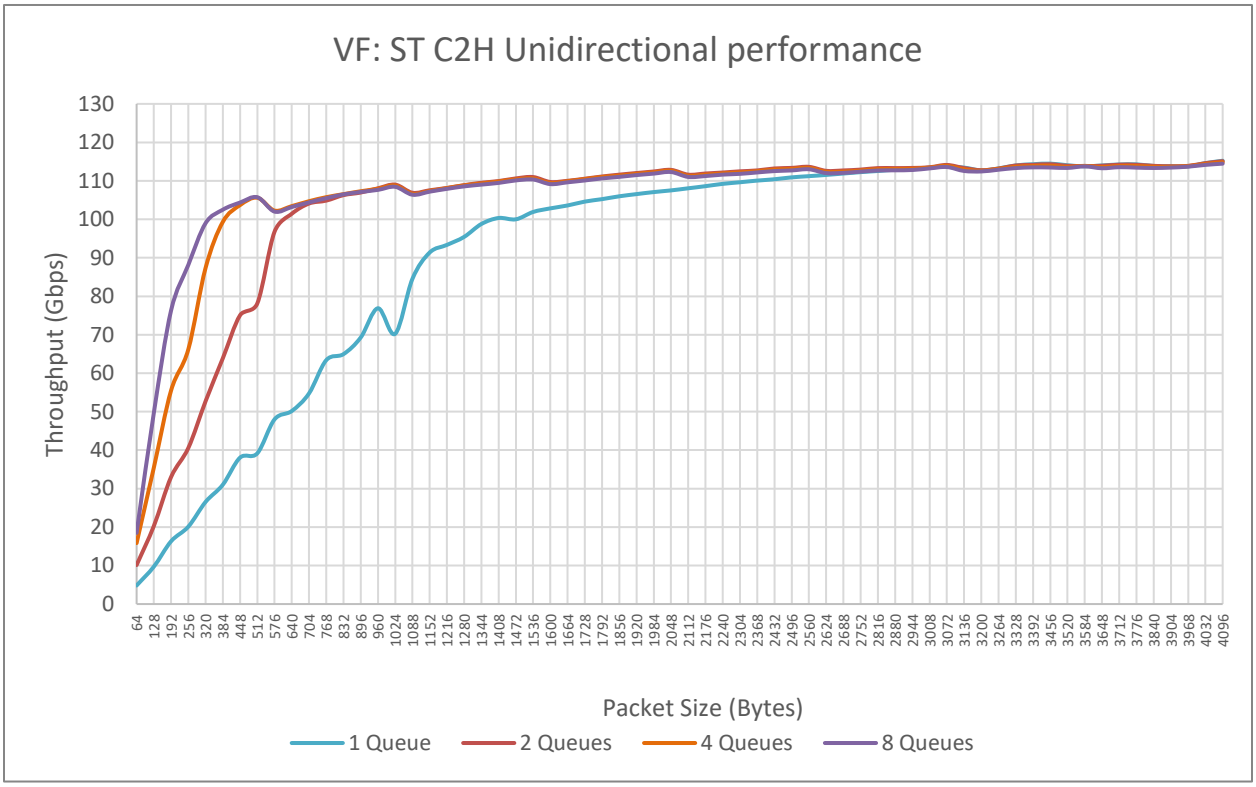


Figure 26: Linux Kernel Reference Driver – QDMA5.0 ST VF C2H Unidirectional Performance

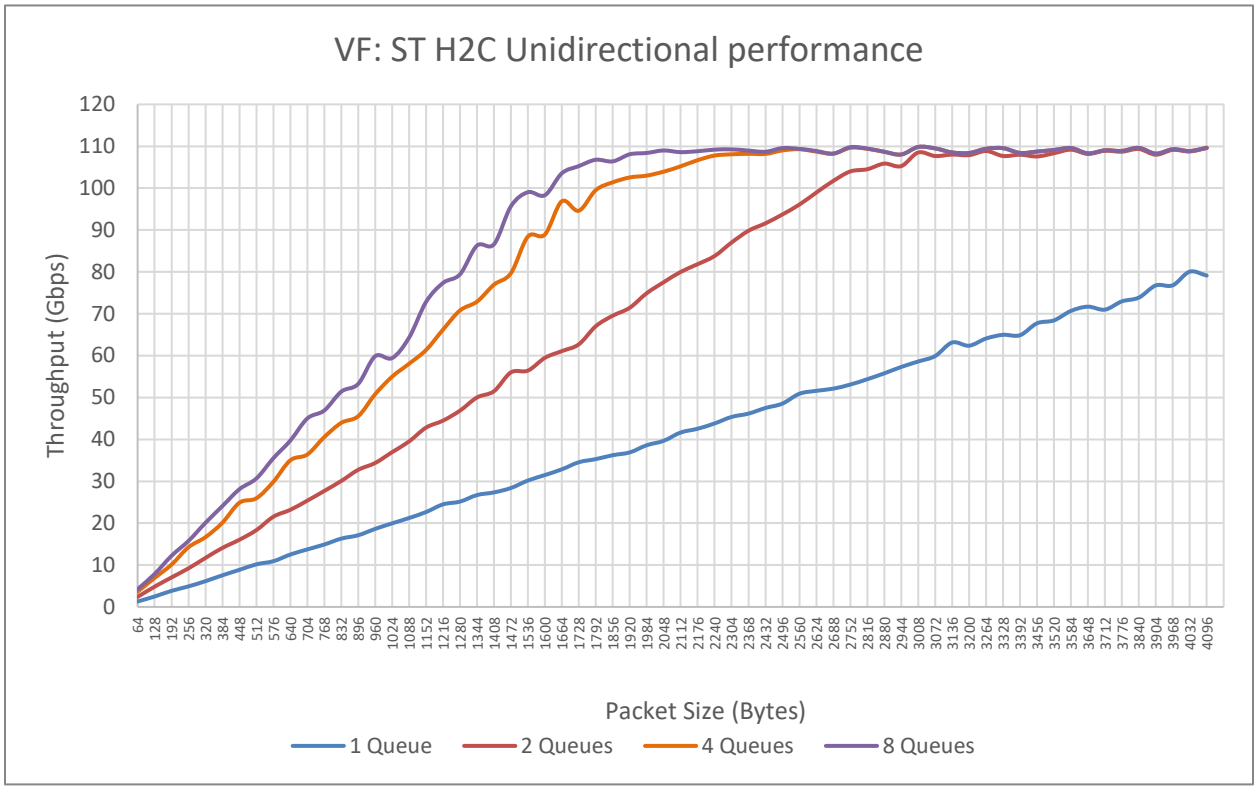


Figure 27: Linux Kernel Reference Driver – QDMA5.0 ST VF H2C Unidirectional Performance

The above H2C graph shows the QDMA IP can achieve line rate at small packet size (with 8 queues). When less number of queues are involved the results are not optimal because there are not enough IO requests in flight to fill the pipeline, especially in the single queue scenario. The “dma-perf” tool and the driver are still being optimized for these cases.

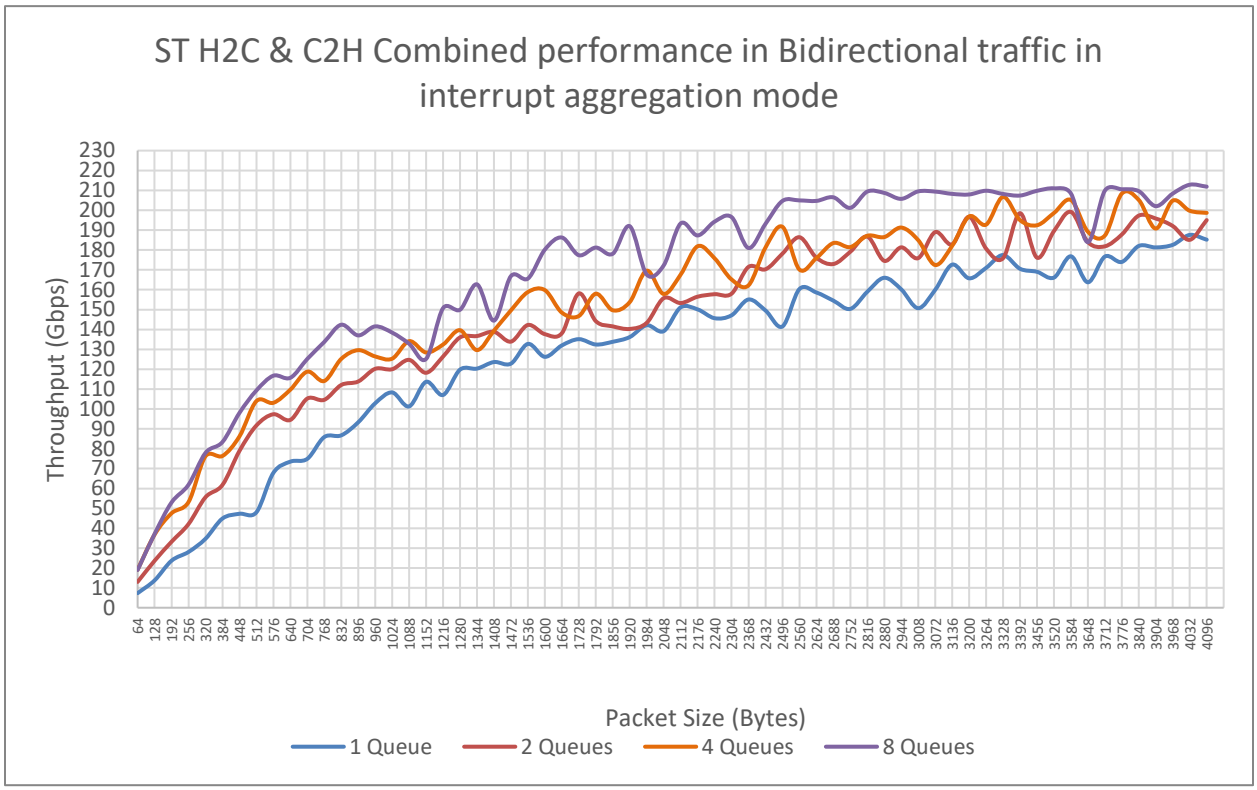


Figure 28: Linux Kernel Reference Driver – QDMA5.0 ST VF combined performance with Bidirectional traffic

Bi-directional ST performance numbers are taken with traffic being enabled in both H2C and C2H direction simultaneously.

PF Performance

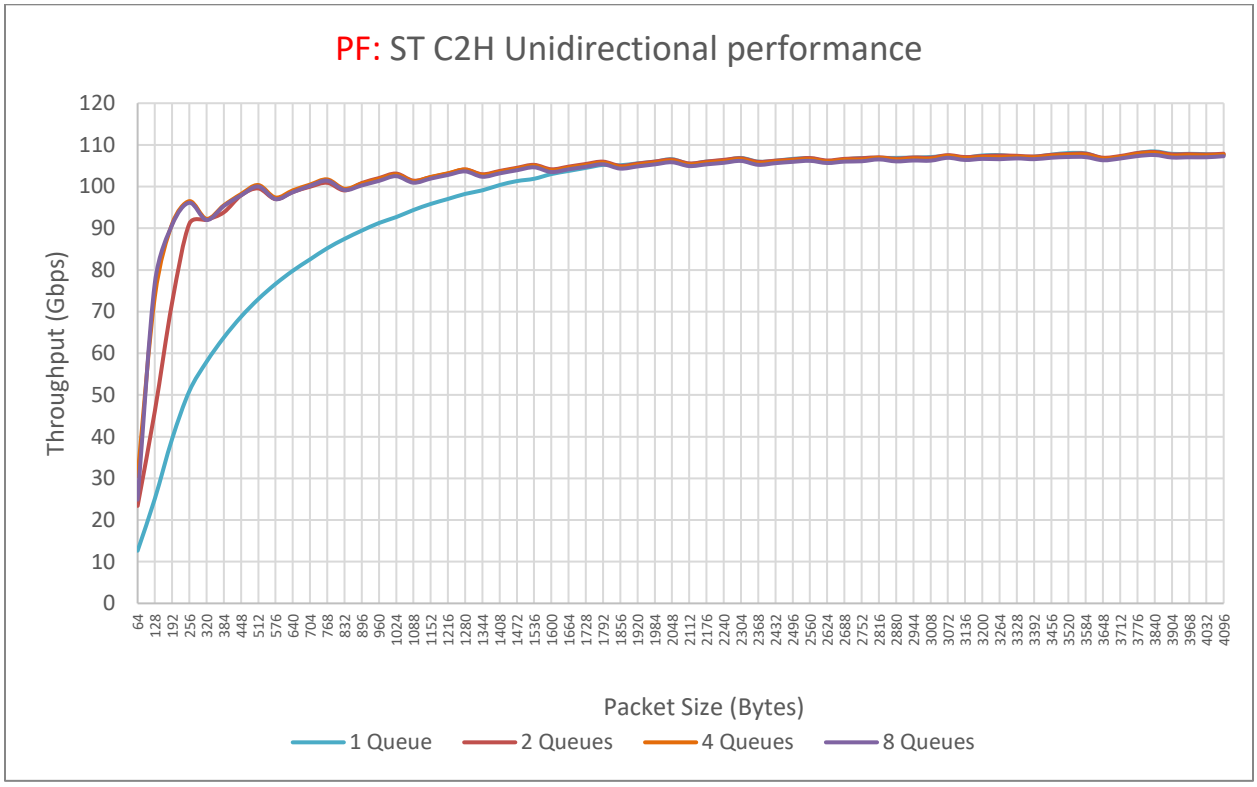


Figure 29: Linux Kernel Reference Driver – QDMA5.0 ST C2H Unidirectional Performance

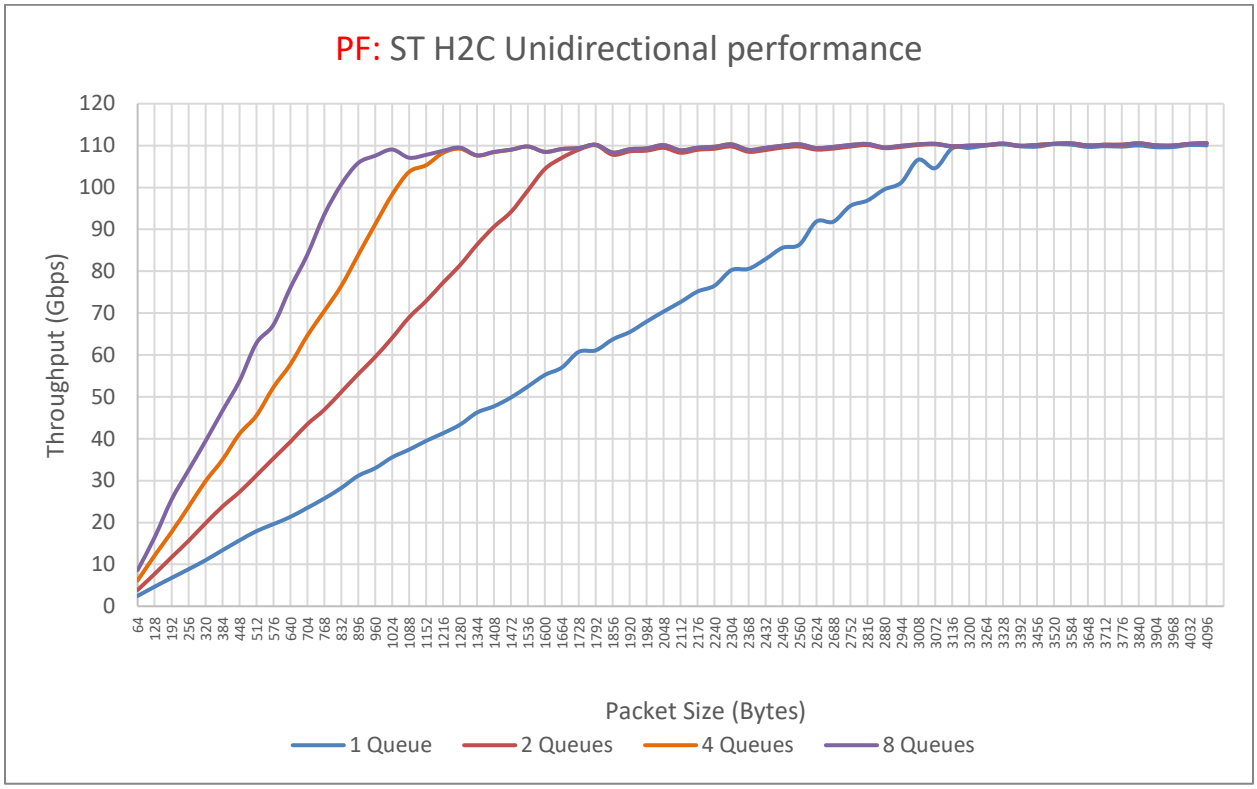


Figure 30: Linux Kernel Reference Driver – QDMA5.0 ST H2C Unidirectional performance

The above H2C graph shows the QDMA IP can achieve line rate at small packet size (with 8 queues). When less number of queues are involved the results are not optimal because there are not enough IO requests in flight to fill the pipeline, especially in the single queue scenario. The “dma-perf” tool and the driver are still being optimized for these cases.

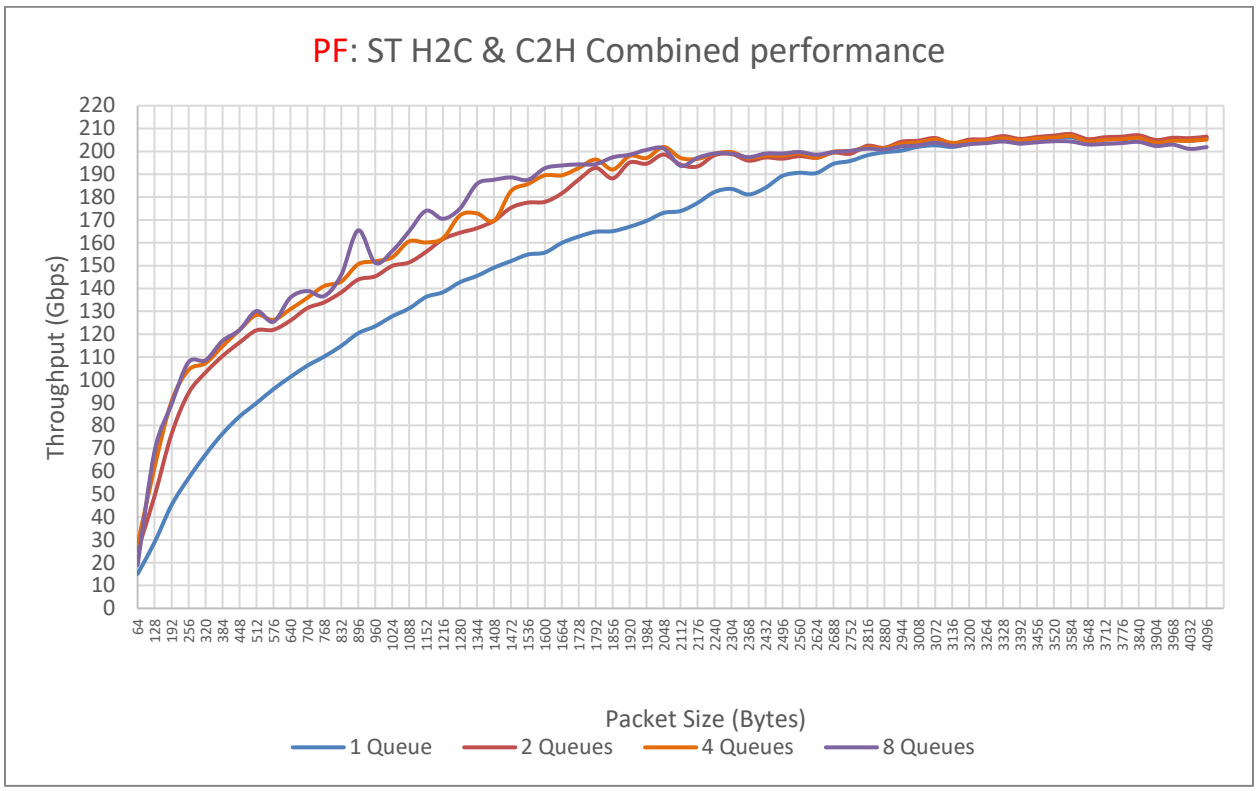


Figure 31: Linux Kernel Reference Driver – QDMA5.0 ST combined performance with Bidirectional traffic

Bi-directional ST performance numbers are taken with traffic being enabled in both H2C and C2H direction simultaneously.

VF Performance

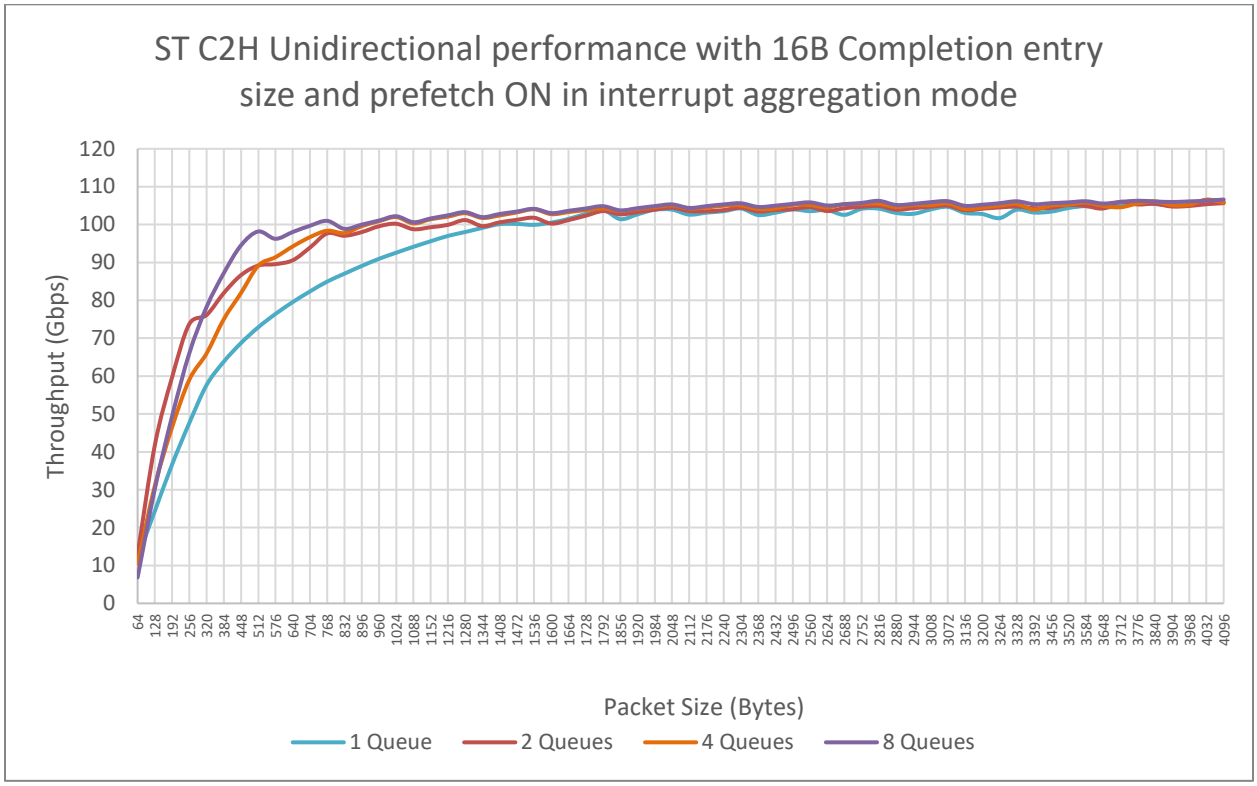


Figure 32: Linux Kernel Reference Driver – QDMA5.0 ST VF C2H Unidirectional Performance

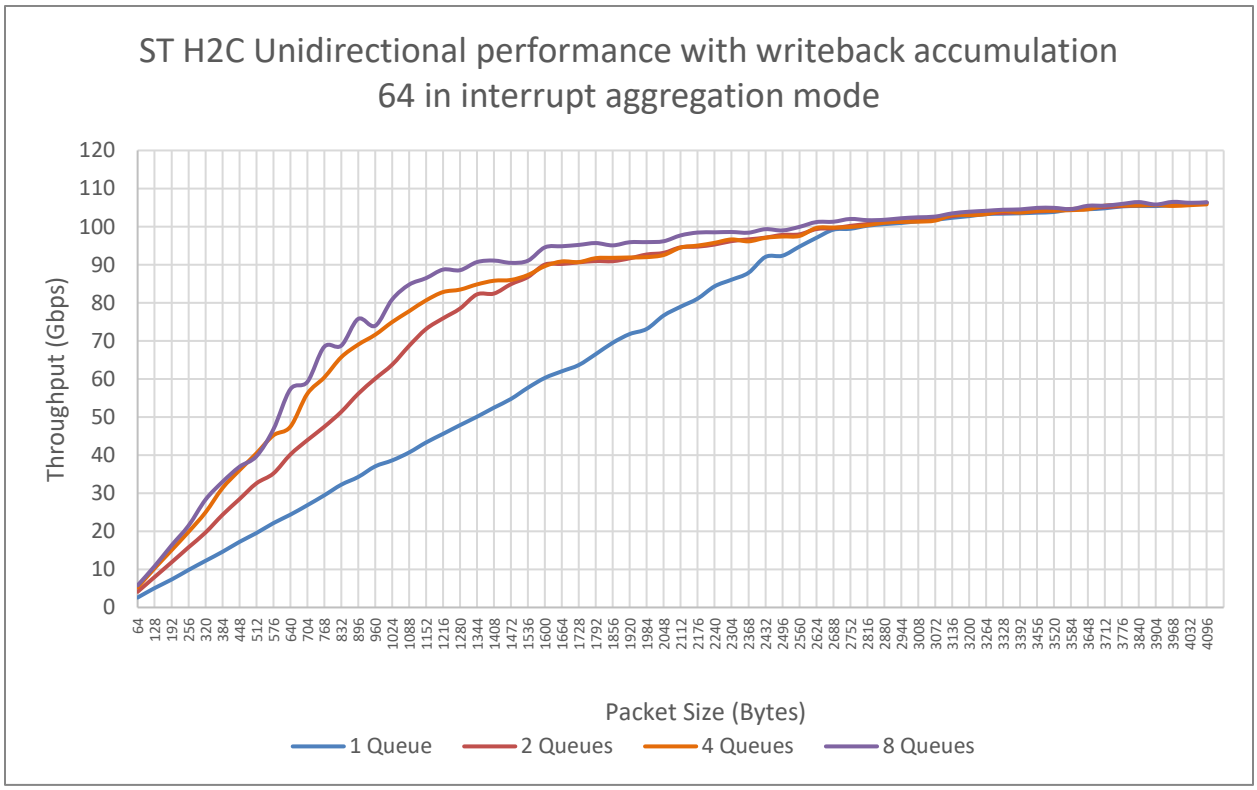


Figure 33: Linux Kernel Reference Driver – QDMA5.0 ST VF H2C Unidirectional Performance

The above H2C graph shows the QDMA IP can achieve line rate at small packet size (with 8 queues). When less number of queues are involved the results are not optimal because there are not enough IO requests in flight to fill the pipeline, especially in the single queue scenario. The “dma-perf” tool and the driver are still being optimized for these cases.

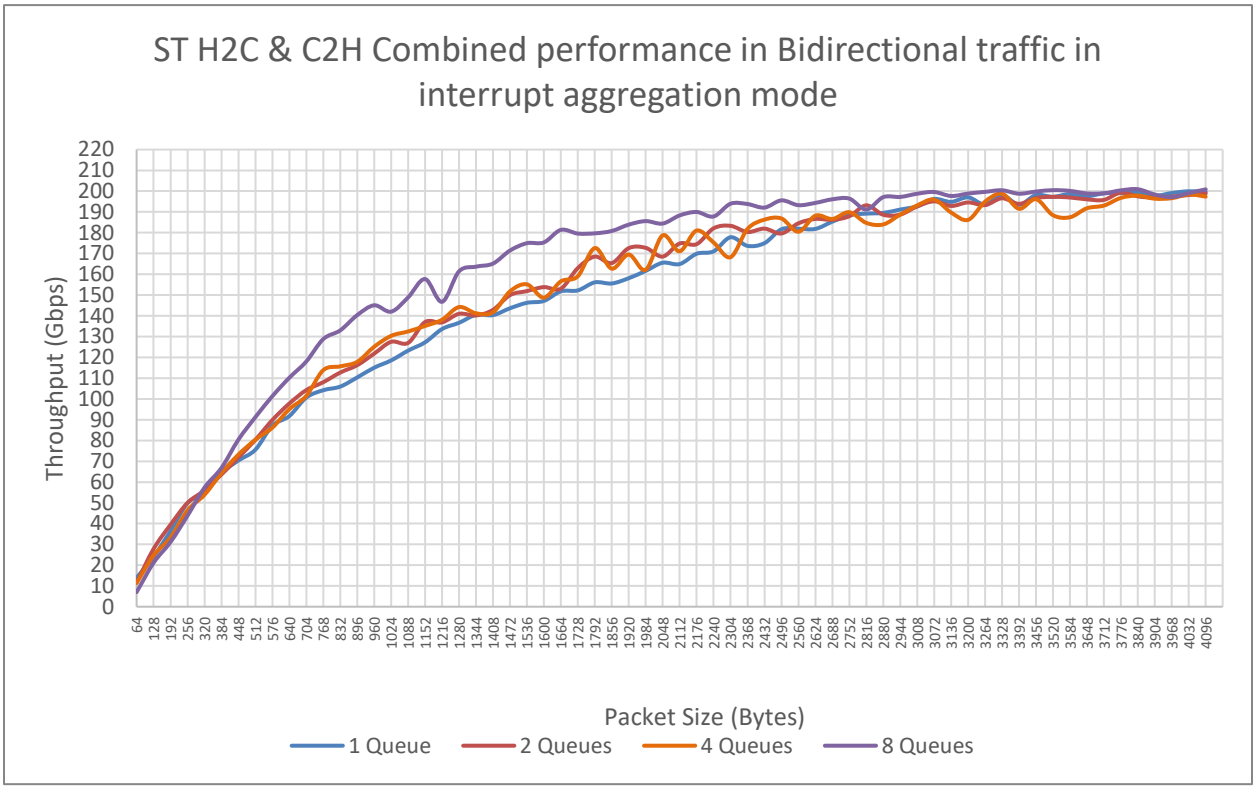


Figure 34: Linux Kernel Reference Driver – QDMA5.0 ST VF combined performance with Bidirectional traffic

Bi-directional ST performance numbers are taken with traffic being enabled in both H2C and C2H direction simultaneously.

Memory Mapped Mode Performance BRAM Design

The data below are collected with BRAM. If using DDR memory the memory controller overhead needs to be taken into consideration.

The dma-perf config files used for the above memory-map mode tests are part of the linux reference kernel driver source, hosted at GitHub https://github.com/Xilinx/dma_ip_drivers, under directory QDMA/linux-kernel/apps/dma-perf/dmaperf_config:

- C2H unidirectional: mm-c2h.zip
- H2C unidirectional: mm-h2c.zip
- C2H & H2C bi-directional: mm-bi.zip

QDMA Performance metrics on AMD System

PF Performance

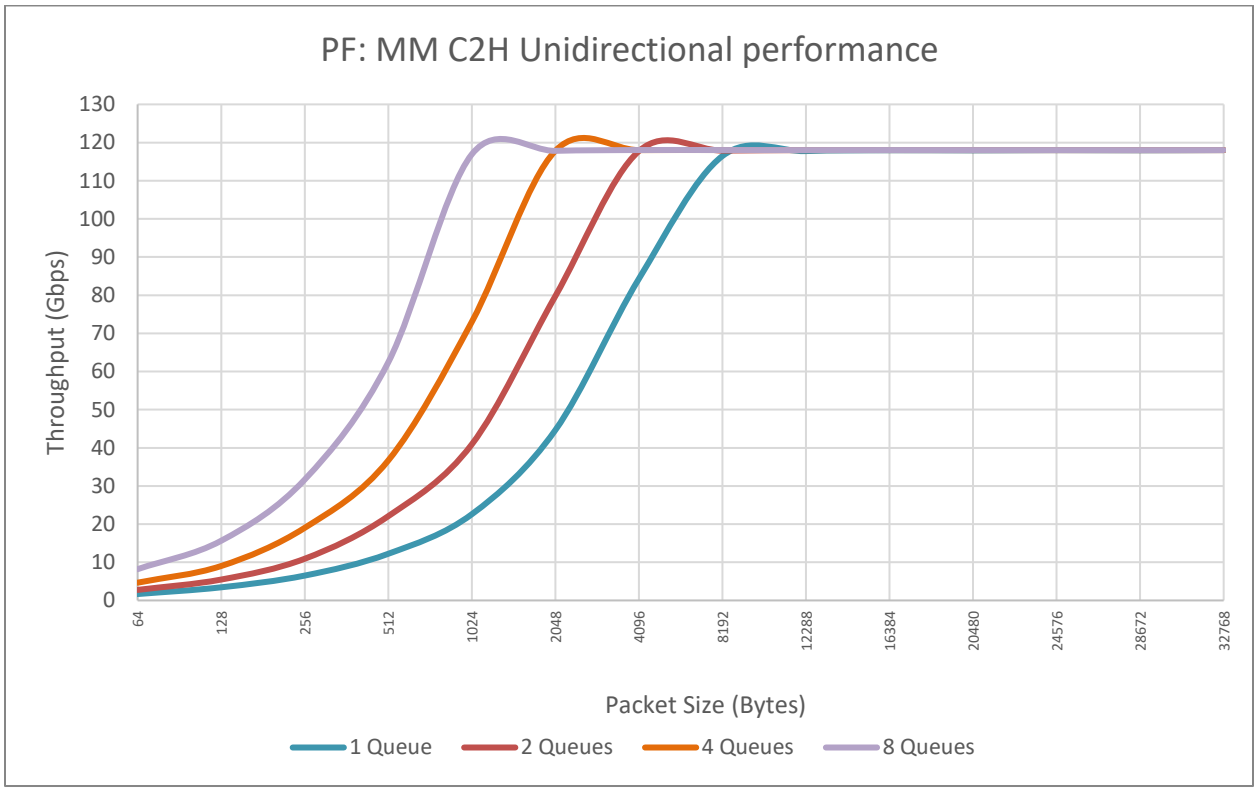


Figure 35: Linux Kernel Reference Driver –QDMA 5.0 BRAM design MM C2H unidirectional performance

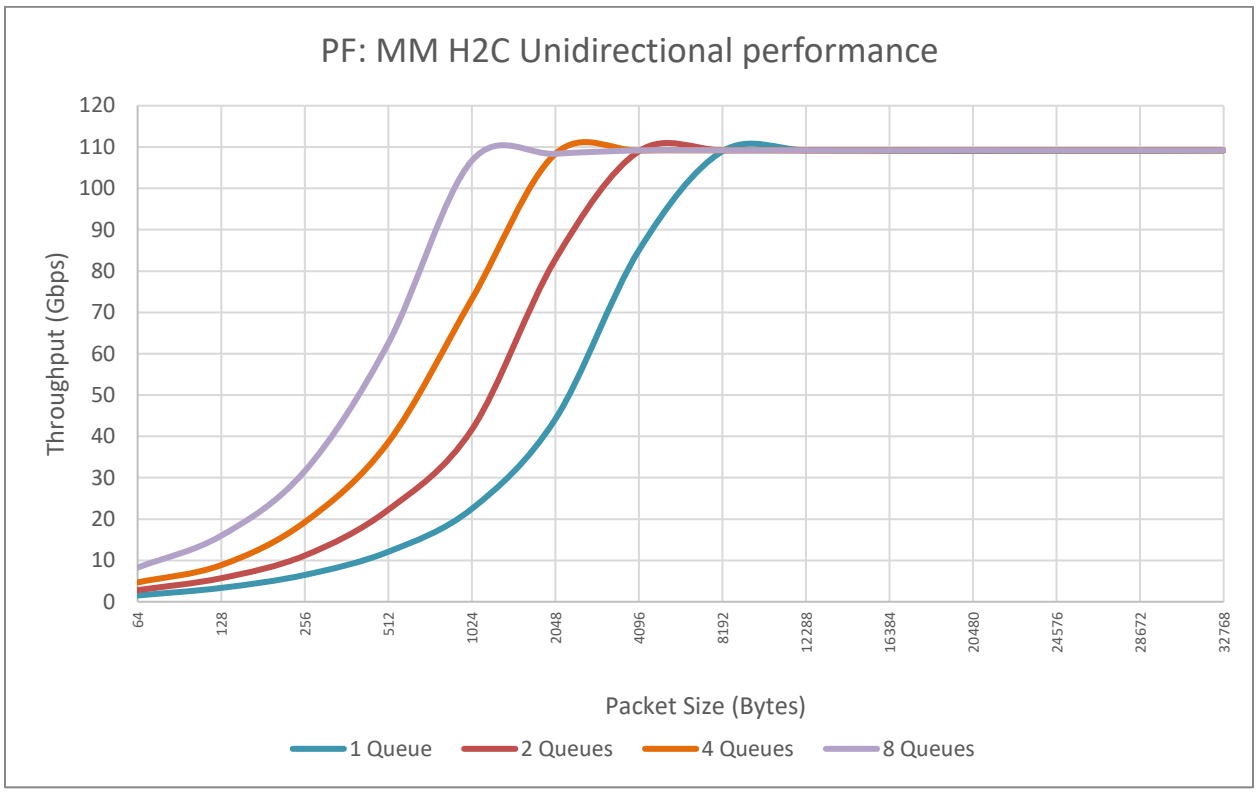


Figure 36: Linux Kernel Reference Driver – QDMA5.0 BRAM design MM H2C unidirectional performance

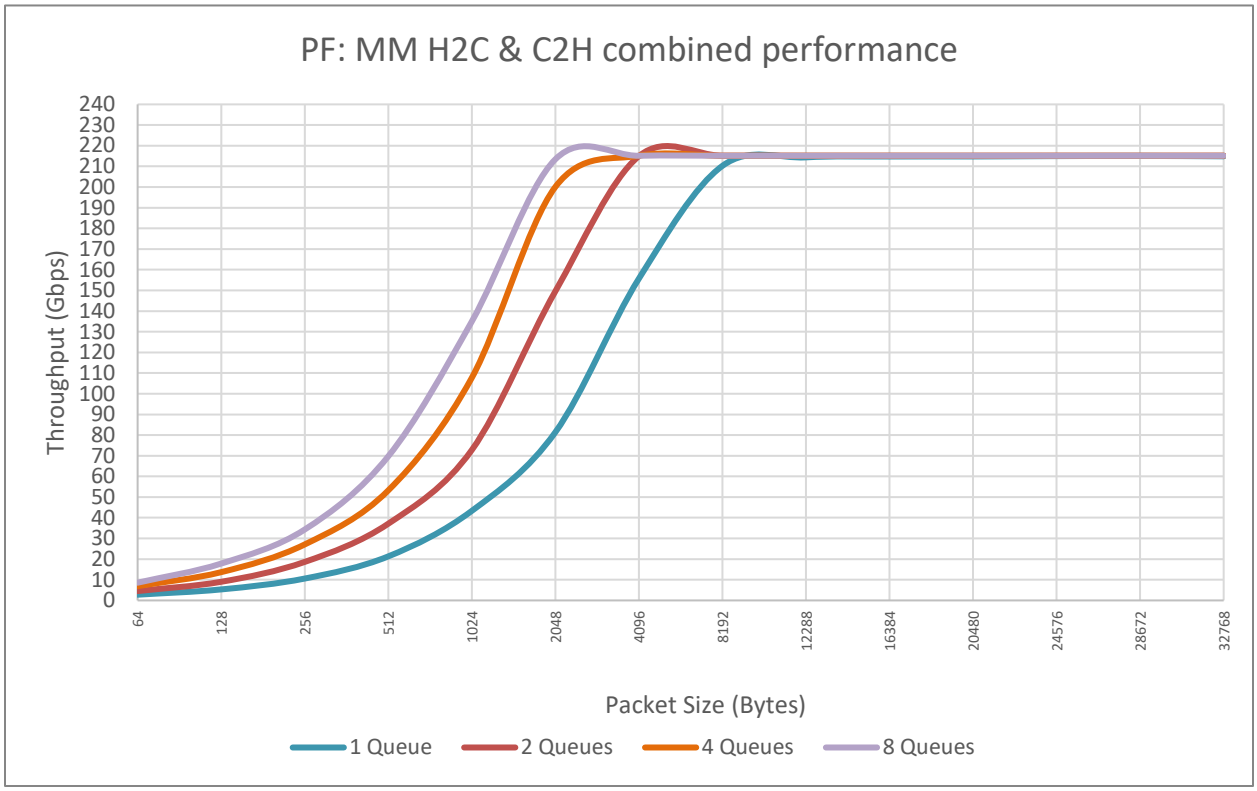


Figure 37: Linux Kernel Reference Driver – QDMA 5.0 BRAM design MM combined bidirectional performance

Bi-directional MM performance numbers are taken with traffic being enabled in both H2C and C2H direction simultaneously.

VF Performance

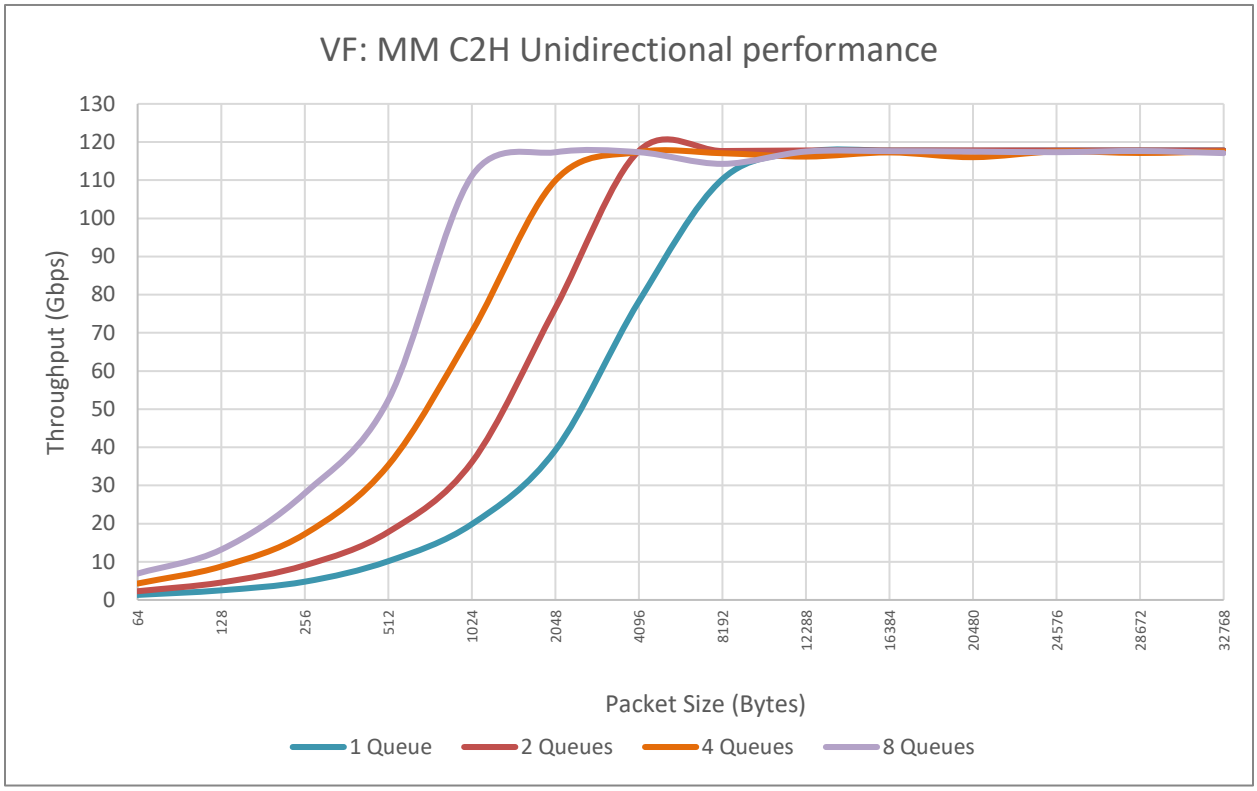


Figure 38: Linux Kernel Reference Driver –QDMA5.0 VF BRAM design MM C2H unidirectional performance

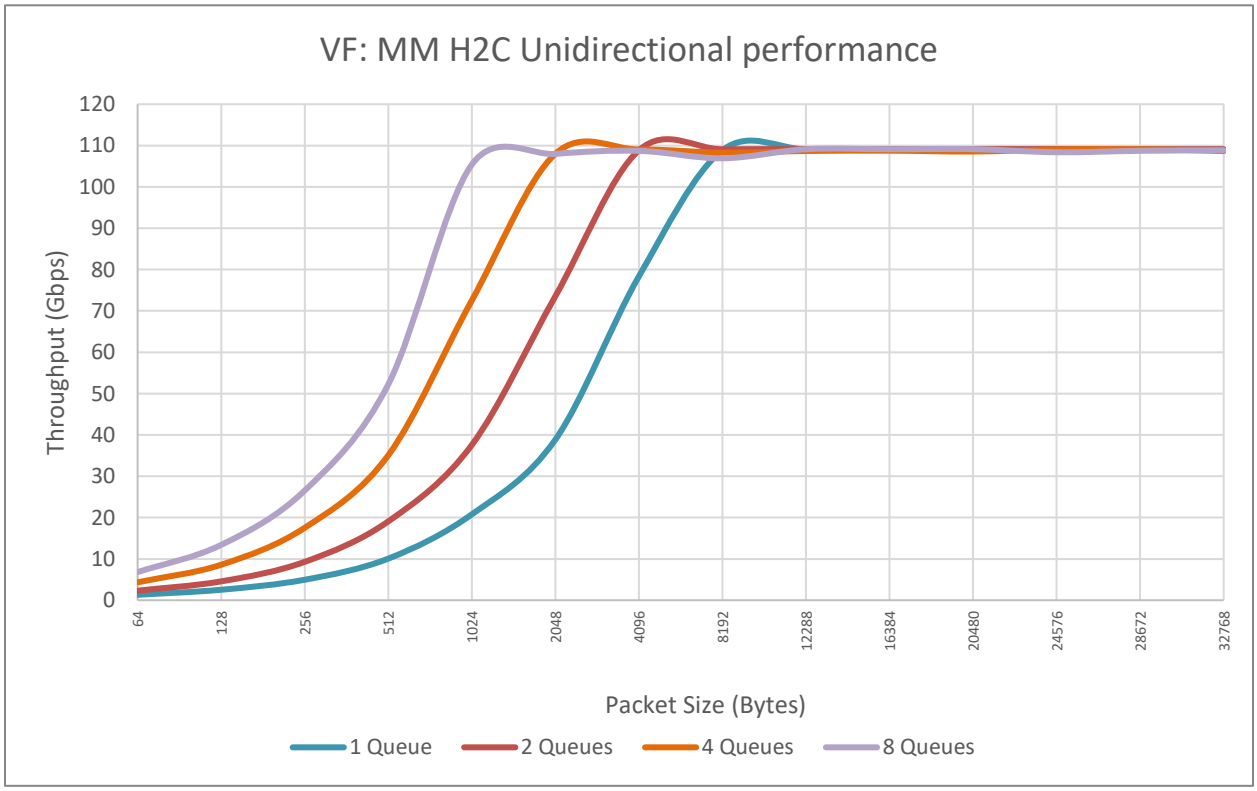


Figure 39: **Linux Kernel Reference Driver – QDMA5.0 VF BRAM design VF MM H2C unidirectional performance**

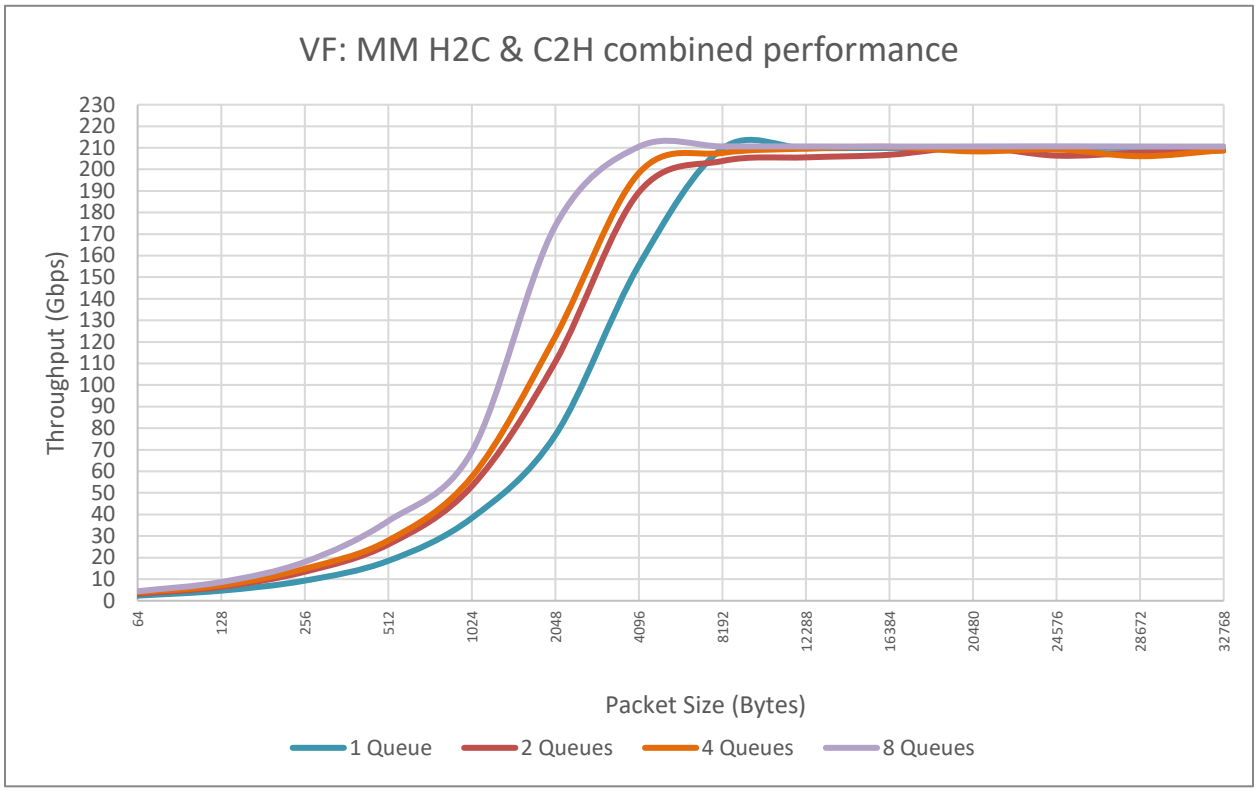


Figure 40: Linux Kernel Reference Driver – QDMA 5.0 VF BRAM design MM combined bidirectional performance

Bi-directional MM performance numbers are taken with traffic being enabled in both H2C and C2H direction simultaneously.

QDMA Performance metrics on Intel System

PF Performance

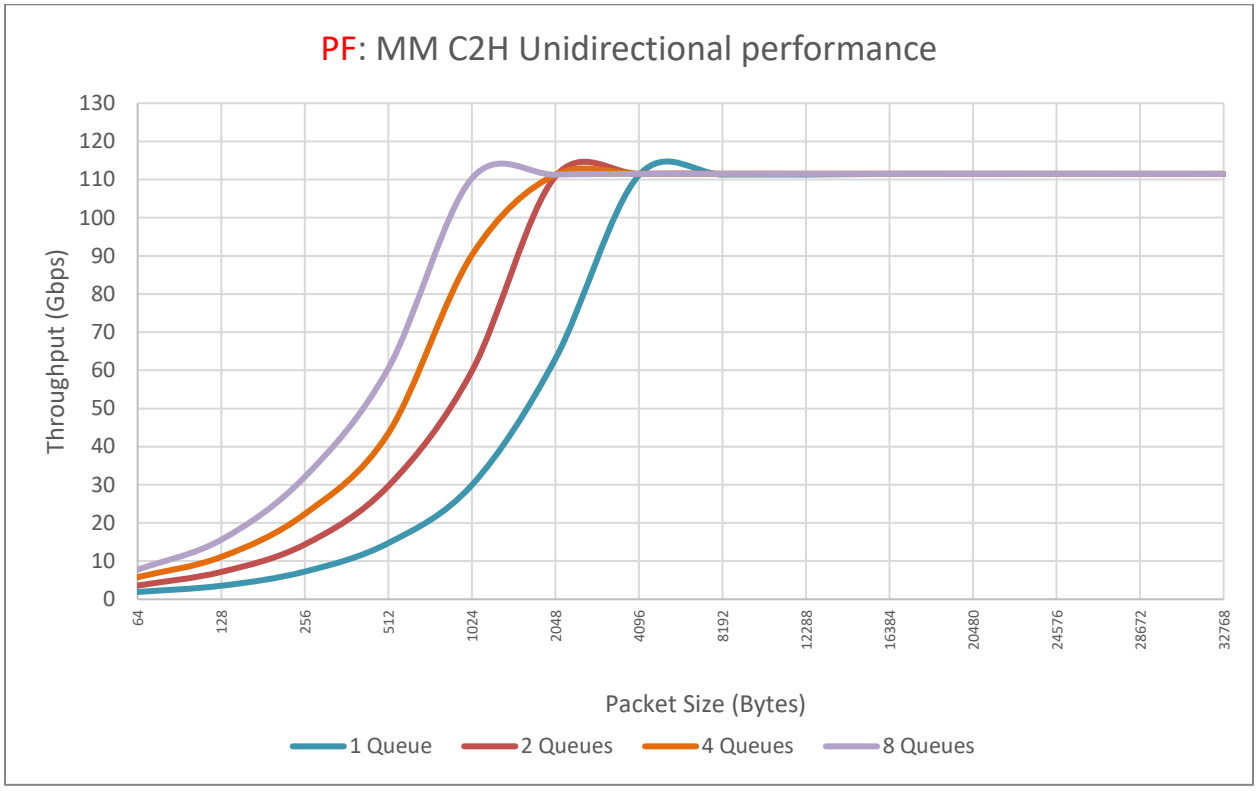


Figure 41: Linux Kernel Reference Driver –QDMA 5.0 BRAM design MM C2H unidirectional performance

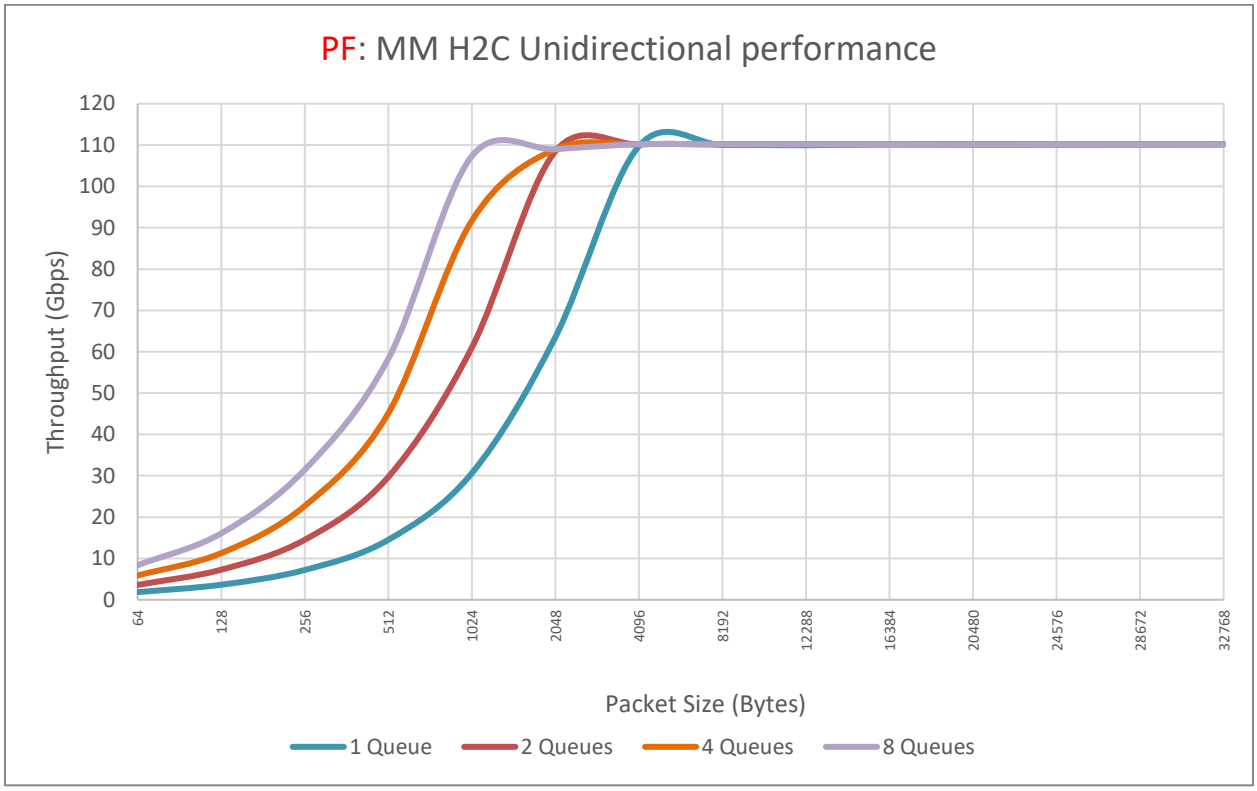


Figure 42: Linux Kernel Reference Driver – QDMA5.0 BRAM design MM H2C unidirectional performance

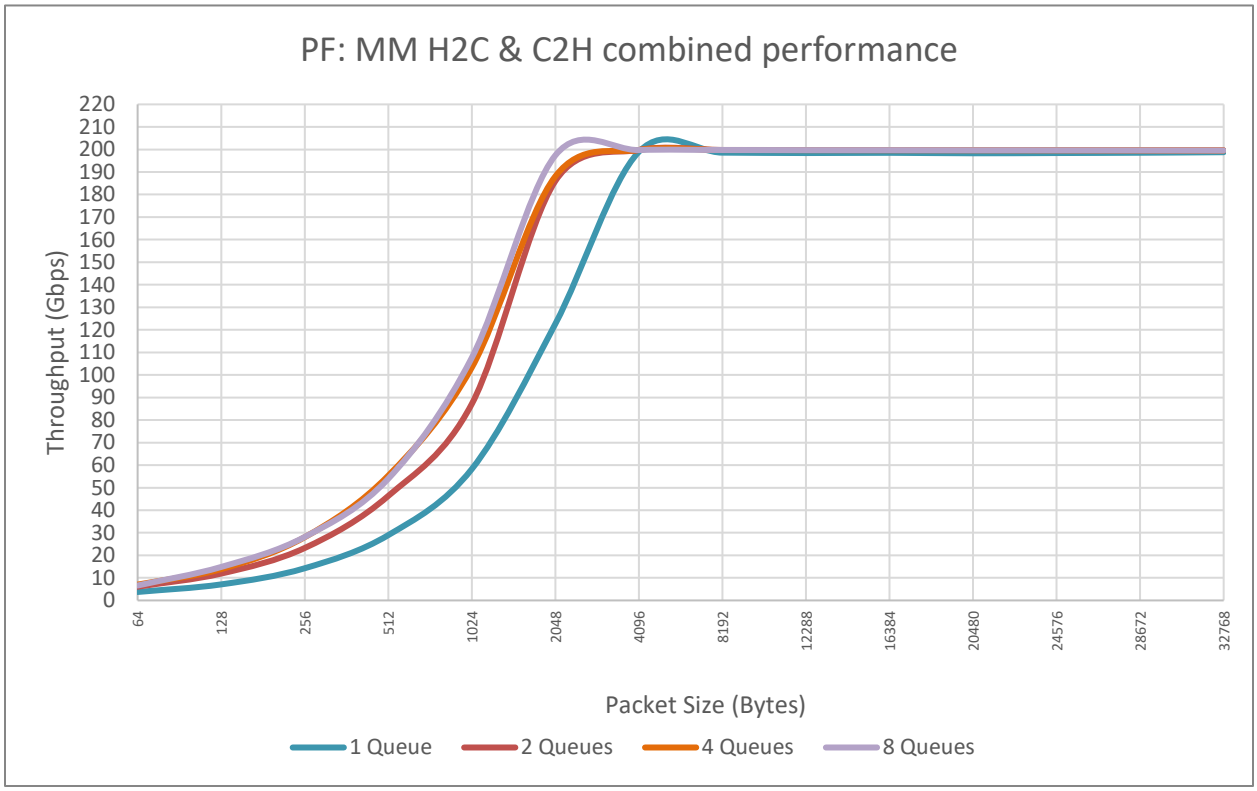


Figure 43: Linux Kernel Reference Driver – QDMA 5.0 BRAM design MM combined bidirectional performance

Bi-directional MM performance numbers are taken with traffic being enabled in both H2C and C2H direction simultaneously.

VF Performance

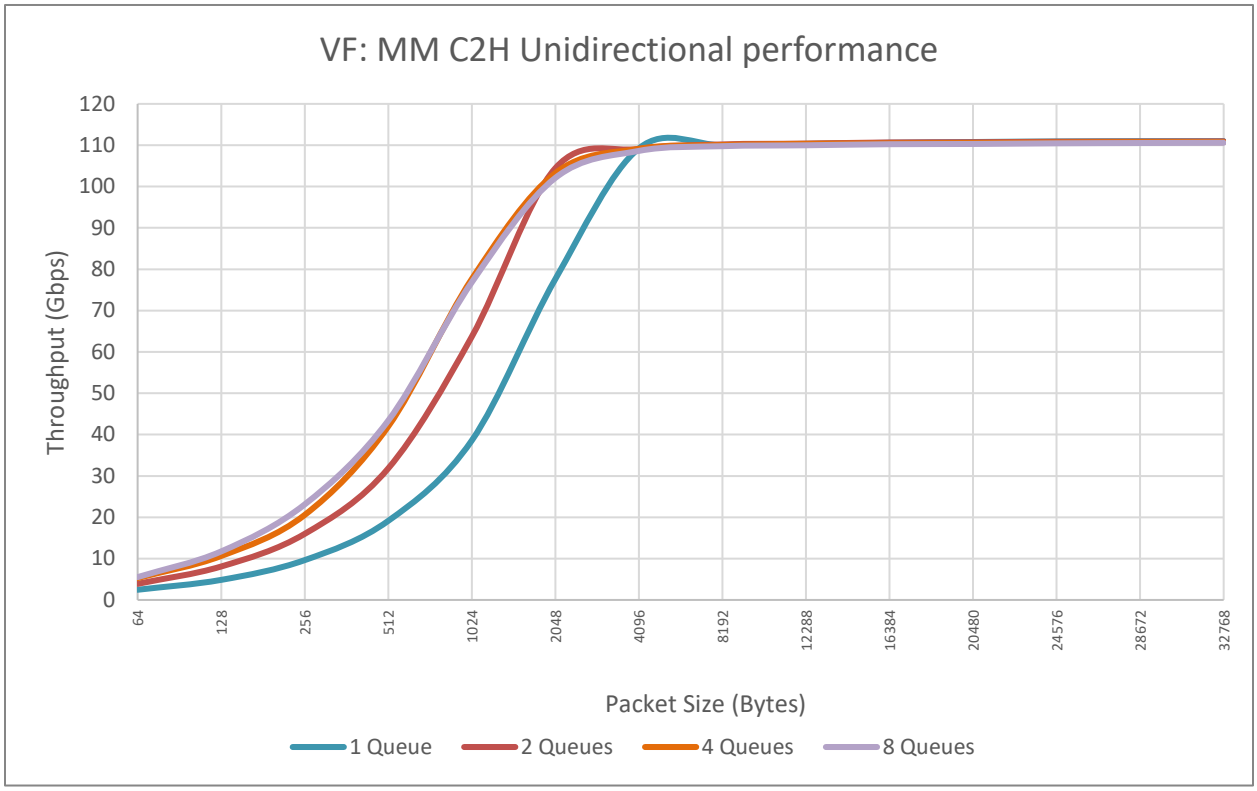


Figure 44: Linux Kernel Reference Driver –QDMA5.0 VF BRAM design MM C2H unidirectional performance

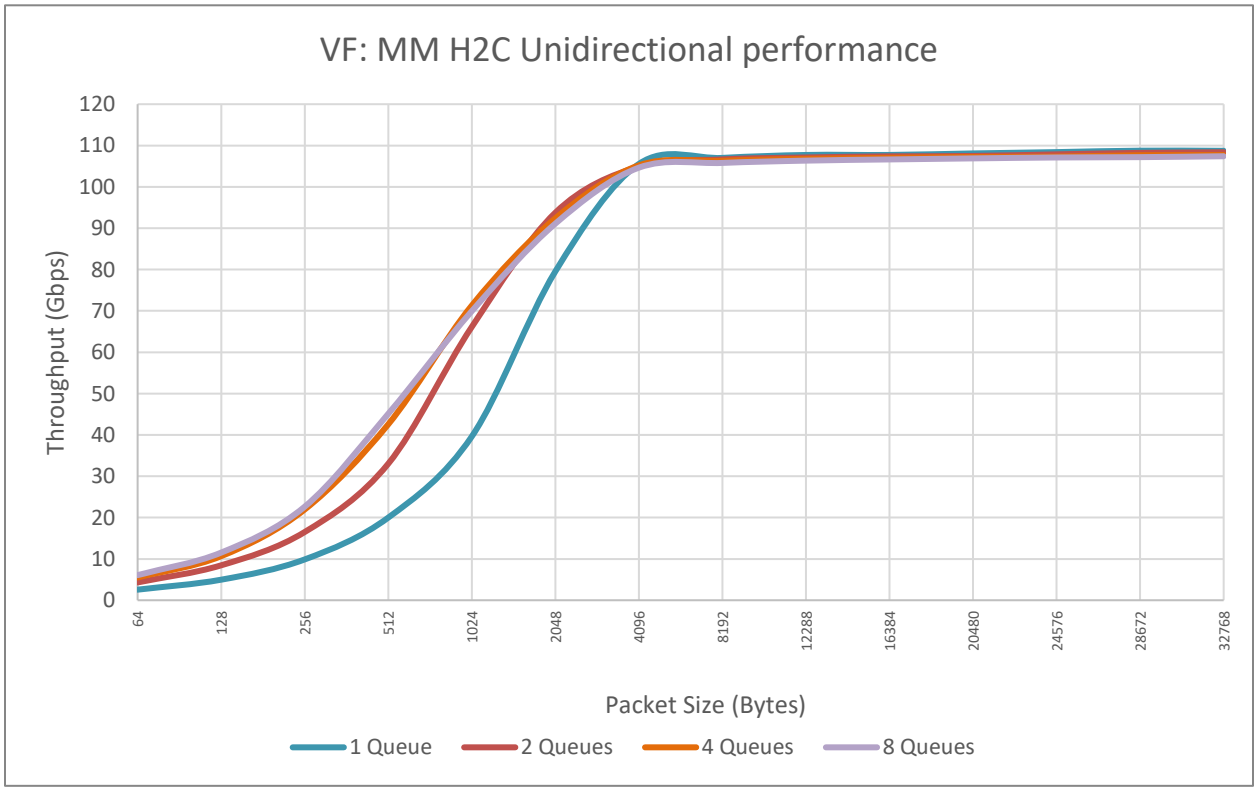


Figure 45: Linux Kernel Reference Driver – QDMA5.0 VF BRAM design VF MM H2C unidirectional performance

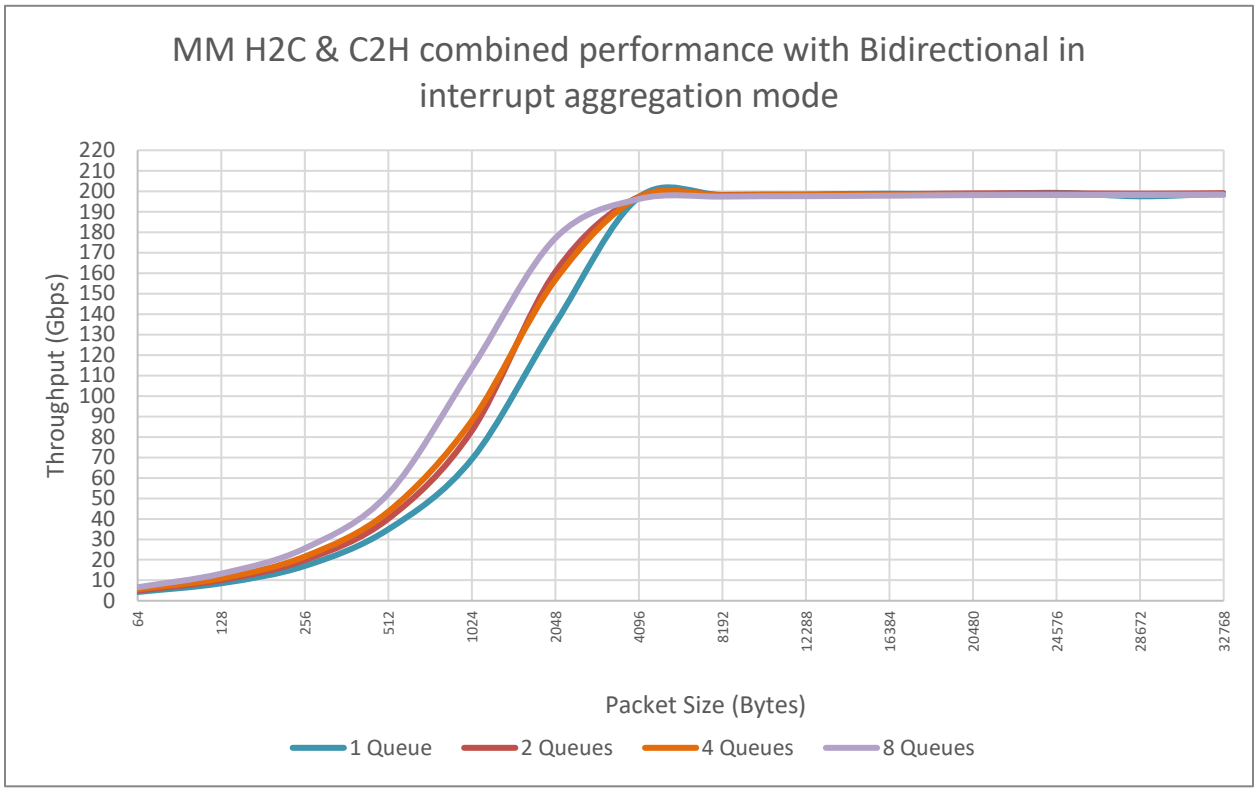


Figure 46: Linux Kernel Reference Driver – QDMA 5.0 VF BRAM design MM combined bidirectional performance

Bi-directional MM performance numbers are taken with traffic being enabled in both H2C and C2H direction simultaneously.

Summary

The QDMA IP provides many capabilities that allow for very high throughput and efficiency. At the same time however, there are factors that impact performance, such as packet size, DMA overhead, system latency, and settings such as MPS, MRRS, etc.

This report provides enough data to choose the number of queues needed to achieve optimal performance depending on the application.

Typically, networking applications optimize for small packet performance and so can use more queues to saturate the Ethernet interface, while compute or storage applications might optimize for 4KB performance and saturate with fewer queues. As the report suggests, more queues help achieve small packet performance, but the max number of queues cannot exceed the number of threads available for the application.

For the streaming mode this report suggests that 4 and more queues with prefetch enabled results in the high performance for different packet sizes.

For the memory mapped mode, the QDMA IP easily achieves the line rate with the typical 4K workload even with a single queue when using BRAM. If DDR is desired, more queues may be needed to obtain the best performance. This would highly depend on the memory configuration and the access pattern. For example, concurrent read and write to the same memory bank would greatly reduce the efficiency and should be avoided if possible.

The bi-directional performance should be expected to be lower than uni-directional H2C and C2H, because the PCIe RQ interface is shared.

In a multi-socket machine where NUMA is enabled, the latency for DMA reads can be prohibitively high, causing lower performance. Caution must be taken in the driver to avoid using the memory far away from the CPU core.

Based on knowledge of the application, it is possible to further reduce the DMA and TLP overheads to achieve better throughput than in the document.

References

These documents provide supplemental material useful with this performance report.

- QDMA Subsystem for PCI Express v5.0 - PG302
- dpdk-pktgen application
- UltraScale+ Devices Integrated Block for PCI Express v1.3