Problem Statement

Statement: Design a 5-stage (as discussed in the lecture) pipeline RISC processor (with hazard detection and data forwarding unit as necessary) that can execute the following instructions:

0000 SW reg1, 7(reg2)
0004 NOR reg3, reg4, reg5
0008 ADDI reg6, reg3, 1078
0012 AND reg8, reg7, reg6
0016 OR reg9, reg8, reg3

Initialize the register file with the following data
reg1 = 90966 reg2 = 5
reg4 = FE331 reg5 = 45432
reg7 = 23211

The instruction format is as follows:

31 28	27 24	23 20	19 16	15 0
OPCODE	Dest Reg (WN)	Source Reg 1 (RN1)	Source Reg 2 (RN2)	Immediate value

Opcode for each instruction:
Instruction 1: 0000
Instruction 2: 0001
Instruction 3: 0011
Instruction 4: 0111
Instruction 5: 1111

The processor has the following control signals:

- ALUSrc - Select the second input of ALU
- ALUOp (2 bits) - Control ALU operation
- MR - Read data from memory
- MW - Write data into memory
- MReg - Move data from memory to register
- EnIM - Read instruction memory contents
- EnRW - Write data into the register file
- FA - Forward A mux control (used in data forwarding circuitry)
- FB - Forward B mux control (used in data forwarding circuitry)
- IFIDWrite - Disable IF/ID change (used in hazard detection circuit)

- PCWrite - Disable PC change (used in hazard detection circuit)
- ST - Control signal of mux which changes all control signals to zero (used in hazard detection circuit)

Initialize PC with all zeros. The instruction memory is of size 32 bytes, and the processor has 16 registers, numbered from reg0 to reg15, and the registers are 32 bits wide. A read operation from the instruction memory outputs 4 consecutive bytes of information (starting from the byte address provided to the memory) at the positive edge of the clock if the EnIM control signal is high. Assume that the register file has two 32-bit read ports: RD1 and RD2, for data reading and one 32-bit write port: WD, for data writing. At the rising edge of the clock, the read ports RD1 and RD2 output the data from the registers whose addresses are available at RN1 and RN2, respectively. At the falling edge of a clock, data is written via the write port WD to the register file whose address is present at WN if the EnRW signal is true. Design the data memory size as per the requirement. All the data are in hexadecimal format unless specified.

Draw the detailed architecture-level diagram of the processor, depicting all the blocks (e.g., register file, instruction memory, ALU, PC, combinational functional blocks, hazard detection unit, forwarding unit, etc.). Describe each block individually, and create behavioral verilog models for each architectural block separately. Build the top-level structural model of the processor by instantiating and interconnecting the individual architectural blocks. Specify the size and format of all pipeline registers including the fields holding the decoded control signals as well as data. Show all the input, output, and control signal waveforms in the report.