**Code:**

from tabulate import tabulate

NUMBER\_OF\_INPUTS = 4

def format\_input(power):

binary\_str = [format(i, '0'+str(power)+'b') for i in range(2\*\*power)]

binary = []

for i in range(len(binary\_str)):

binary.append([int(x) for x in binary\_str[i]])

return binary

def GATE(inp, thresh, neg=False):

output = -1

weights = [1 for i in range(len(inp))]

measured\_output = sum([inp[i]\*weights[i] for i in range(len(inp))])

if(measured\_output > thresh):

if neg:

output = 0

else:

output = 1

else:

if neg:

output = 1

else:

output = 0

return output

inputs = format\_input(NUMBER\_OF\_INPUTS)

outputs\_or = []

outputs\_nor = []

outputs\_and = []

outputs\_nand = []

for i in inputs:

outputs\_or.append([i, GATE(i, 0.5)]) # OR GATE

outputs\_nor.append([i, GATE(i, 0.5, True)]) # NOR GATE

outputs\_and.append([i, GATE(i, NUMBER\_OF\_INPUTS-1)]) # AND GATE

outputs\_nand.append([i, GATE(i, NUMBER\_OF\_INPUTS-1, True)]) # NAND GATE

print("OR GATE: ")

print(tabulate(outputs\_or, headers=['inputs', 'outputs']))

print("NOR GATE: ")

print(tabulate(outputs\_nor, headers=['inputs', 'outputs']))

print("AND GATE: ")

print(tabulate(outputs\_and, headers=['inputs', 'outputs']))

print("NAND GATE: ")

print(tabulate(outputs\_nand, headers=['inputs', 'outputs']))

**Outputs:**

OR GATE:

inputs outputs

------------ ---------

[0, 0, 0, 0] 0

[0, 0, 0, 1] 1

[0, 0, 1, 0] 1

[0, 0, 1, 1] 1

[0, 1, 0, 0] 1

[0, 1, 0, 1] 1

[0, 1, 1, 0] 1

[0, 1, 1, 1] 1

[1, 0, 0, 0] 1

[1, 0, 0, 1] 1

[1, 0, 1, 0] 1

[1, 0, 1, 1] 1

[1, 1, 0, 0] 1

[1, 1, 0, 1] 1

[1, 1, 1, 0] 1

[1, 1, 1, 1] 1

NOR GATE:

inputs outputs

------------ ---------

[0, 0, 0, 0] 1

[0, 0, 0, 1] 0

[0, 0, 1, 0] 0

[0, 0, 1, 1] 0

[0, 1, 0, 0] 0

[0, 1, 0, 1] 0

[0, 1, 1, 0] 0

[0, 1, 1, 1] 0

[1, 0, 0, 0] 0

[1, 0, 0, 1] 0

[1, 0, 1, 0] 0

[1, 0, 1, 1] 0

[1, 1, 0, 0] 0

[1, 1, 0, 1] 0

[1, 1, 1, 0] 0

[1, 1, 1, 1] 0

AND GATE:

inputs outputs

------------ ---------

[0, 0, 0, 0] 0

[0, 0, 0, 1] 0

[0, 0, 1, 0] 0

[0, 0, 1, 1] 0

[0, 1, 0, 0] 0

[0, 1, 0, 1] 0

[0, 1, 1, 0] 0

[0, 1, 1, 1] 0

[1, 0, 0, 0] 0

[1, 0, 0, 1] 0

[1, 0, 1, 0] 0

[1, 0, 1, 1] 0

[1, 1, 0, 0] 0

[1, 1, 0, 1] 0

[1, 1, 1, 0] 0

[1, 1, 1, 1] 1

NAND GATE:

inputs outputs

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[0, 0, 0, 0] 1

[0, 0, 0, 1] 1

[0, 0, 1, 0] 1

[0, 0, 1, 1] 1

[0, 1, 0, 0] 1

[0, 1, 0, 1] 1

[0, 1, 1, 0] 1

[0, 1, 1, 1] 1

[1, 0, 0, 0] 1

[1, 0, 0, 1] 1

[1, 0, 1, 0] 1

[1, 0, 1, 1] 1

[1, 1, 0, 0] 1

[1, 1, 0, 1] 1

[1, 1, 1, 0] 1

[1, 1, 1, 1] 0