Title: Performance Comparison of Tiled vs. Non-Tiled Matrix Multiplication

1. Aim

The objective of this assignment is to compare the performance of tiled and non-tiled approaches in matrix multiplication. Specifically, we analyse how different tiling sizes (e.g., row-wise, column-wise, row16, row32, row64, etc.) impact computation time while multiplying a 1024 x 1024 matrix.

2. System Configuration

- **Processor:** Intel Core i5-12450H
- **Operating System:** Ubuntu 24.02

3. Definition

Non-Tiled Approach

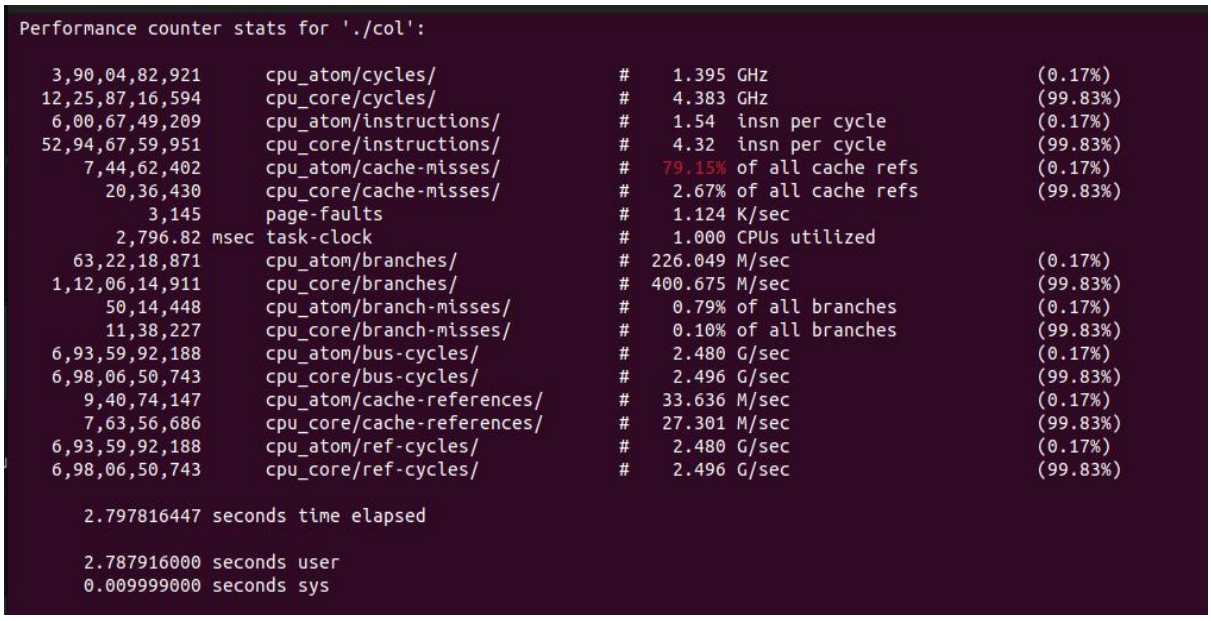
In the non-tiled approach, the entire matrix is processed sequentially without breaking it into smaller blocks. This method is simple but often inefficient due to memory access latency and lack of cache optimization.

Tiled Approach

Tiled matrix multiplication divides the matrices into smaller sub-matrices (tiles). These tiles are processed independently, reducing cache misses and improving memory access efficiency.

4. Performance Comparison Table

Non-tiled Column method



```
Performance counter stats for './col':

   3,90,04,82,921      cpu_atom/cycles/                 #    1.395 GHz                         (0.17%)
  12,25,87,16,594      cpu_core/cycles/                 #    4.383 GHz                         (99.83%)
   6,00,67,49,209      cpu_atom/instructions/           #    1.54  insn per cycle              (0.17%)
  52,94,67,59,951      cpu_core/instructions/           #    4.32  insn per cycle              (99.83%)
      7,44,62,402      cpu_atom/cache-misses/           #   79.15% of all cache refs           (0.17%)
        20,36,430      cpu_core/cache-misses/           #    2.67% of all cache refs           (99.83%)
            3,145      page-faults                      #    1.124 K/sec
         2,796.82 msec task-clock                       #    1.000 CPUs utilized
     63,22,18,871      cpu_atom/branches/               #  226.049 M/sec                       (0.17%)
   1,12,06,14,911      cpu_core/branches/               #  400.675 M/sec                       (99.83%)
        50,14,448      cpu_atom/branch-misses/          #    0.79% of all branches             (0.17%)
        11,38,227      cpu_core/branch-misses/          #    0.10% of all branches             (99.83%)
   6,93,59,92,188      cpu_atom/bus-cycles/             #    2.480 G/sec                       (0.17%)
   6,98,06,50,743      cpu_core/bus-cycles/             #    2.496 G/sec                       (99.83%)
      9,40,74,147      cpu_atom/cache-references/       #   33.636 M/sec                       (0.17%)
      7,63,56,686      cpu_core/cache-references/       #   27.301 M/sec                       (99.83%)
   6,93,59,92,188      cpu_atom/ref-cycles/             #    2.480 G/sec                       (0.17%)
   6,98,06,50,743      cpu_core/ref-cycles/             #    2.496 G/sec                       (99.83%)

      2.797816447 seconds time elapsed

      2.787916000 seconds user
      0.009999000 seconds sys
```

Non tiled Row method

```
Performance counter stats for './row':

   9,30,32,08,642      cpu_atom/cycles/                 #    3.214 GHz                      (0.43%)
  12,69,01,99,118      cpu_core/cycles/                 #    4.384 GHz                      (99.57%)
  30,52,67,22,522      cpu_atom/instructions/           #    3.28  insn per cycle           (0.43%)
  52,96,11,12,204      cpu_core/instructions/           #    4.17  insn per cycle           (99.57%)
      4,57,60,044      cpu_atom/cache-misses/           #   50.11% of all cache refs        (0.43%)
         6,06,917      cpu_core/cache-misses/           #    0.86% of all cache refs        (99.57%)
            3,144      page-faults                      #    1.086 K/sec
         2,894.50 msec task-clock                       #    1.000 CPUs utilized
     93,88,46,927      cpu_atom/branches/               #  324.355 M/sec                    (0.43%)
   1,12,05,90,018      cpu_core/branches/               #  387.144 M/sec                    (99.57%)
        28,68,577      cpu_atom/branch-misses/          #    0.31% of all branches          (0.43%)
        11,36,040      cpu_core/branch-misses/          #    0.10% of all branches          (99.57%)
   7,21,41,08,636      cpu_atom/bus-cycles/             #    2.492 G/sec                    (0.43%)
   7,22,44,98,760      cpu_core/bus-cycles/             #    2.496 G/sec                    (99.57%)
      9,13,24,371      cpu_atom/cache-references/       #   31.551 M/sec                    (0.43%)
      7,05,59,716      cpu_core/cache-references/       #   24.377 M/sec                    (99.57%)
   7,21,41,08,636      cpu_atom/ref-cycles/             #    2.492 G/sec                    (0.43%)
   7,22,44,98,760      cpu_core/ref-cycles/             #    2.496 G/sec                    (99.57%)

      2.894996767 seconds time elapsed

      2.889047000 seconds user
      0.006000000 seconds sys
```

Tiled Approach (Row Method 16x16)

```
Performance counter stats for './row16':

   9,65,60,59,608      cpu_atom/cycles/                 #    3.266 GHz                      (0.13%)
  12,88,63,38,580      cpu_core/cycles/                 #    4.359 GHz                      (99.87%)
  30,40,08,98,947      cpu_atom/instructions/           #    3.15  insn per cycle           (0.13%)
  59,17,71,67,441      cpu_core/instructions/           #    4.59  insn per cycle           (99.87%)
        35,51,314      cpu_atom/cache-misses/           #   17.14% of all cache refs        (0.13%)
        10,96,170      cpu_core/cache-misses/           #   17.83% of all cache refs        (99.87%)
            3,153      page-faults                      #    1.067 K/sec
         2,956.28 msec task-clock                       #    0.933 CPUs utilized
   7,26,56,81,960      cpu_atom/branches/               #    2.458 G/sec                    (0.13%)
   2,71,16,27,346      cpu_core/branches/               #  917.243 M/sec                    (99.87%)
        29,78,649      cpu_atom/branch-misses/          #    0.04% of all branches          (0.13%)
        50,06,653      cpu_core/branch-misses/          #    0.18% of all branches          (99.87%)
   7,35,75,20,887      cpu_atom/bus-cycles/             #    2.489 G/sec                    (0.13%)
   7,37,85,14,057      cpu_core/bus-cycles/             #    2.496 G/sec                    (99.87%)
      2,07,22,585      cpu_atom/cache-references/       #    7.010 M/sec                    (0.13%)
        61,48,308      cpu_core/cache-references/       #    2.080 M/sec                    (99.87%)
   7,35,75,20,887      cpu_atom/ref-cycles/             #    2.489 G/sec                    (0.13%)
   7,37,85,14,122      cpu_core/ref-cycles/             #    2.496 G/sec                    (99.87%)

      3.168572391 seconds time elapsed

      2.927336000 seconds user
      0.030003000 seconds sys
```

Tiled Approach (Column Method 16x16)

```
Performance counter stats for './col16':

   3,83,59,64,509      cpu_atom/cycles/                 #    1.268 GHz                      (0.17%)
  13,19,29,48,117      cpu_core/cycles/                 #    4.361 GHz                      (99.83%)
   3,80,72,99,685      cpu_atom/instructions/           #    0.99  insn per cycle           (0.17%)
  59,33,21,39,784      cpu_core/instructions/           #    4.50  insn per cycle           (99.83%)
      8,35,95,398      cpu_atom/cache-misses/           #   83.45% of all cache refs        (0.17%)
        12,25,904      cpu_core/cache-misses/           #   15.66% of all cache refs        (99.83%)
            3,148      page-faults                      #    1.041 K/sec
         3,025.14 msec task-clock                       #    0.924 CPUs utilized
     67,31,28,110      cpu_atom/branches/               #  222.512 M/sec                    (0.17%)
   2,74,02,93,316      cpu_core/branches/               #  905.841 M/sec                    (99.83%)
        50,82,522      cpu_atom/branch-misses/          #    0.76% of all branches          (0.17%)
        51,57,158      cpu_core/branch-misses/          #    0.19% of all branches          (99.83%)
   7,50,48,07,802      cpu_atom/bus-cycles/             #    2.481 G/sec                    (0.17%)
   7,55,04,25,473      cpu_core/bus-cycles/             #    2.496 G/sec                    (99.83%)
      10,01,75,314      cpu_atom/cache-references/      #   33.114 M/sec                    (0.17%)
        78,30,065      cpu_core/cache-references/       #    2.588 M/sec                    (99.83%)
   7,50,48,07,802      cpu_atom/ref-cycles/             #    2.481 G/sec                    (0.17%)
   7,55,04,25,473      cpu_core/ref-cycles/             #    2.496 G/sec                    (99.83%)

      3.273441779 seconds time elapsed

      3.004565000 seconds user
      0.021003000 seconds sys
```

Tiled Approach (Row method 32 x 32)

```
Performance counter stats for './row32':

   4,46,02,26,514      cpu_atom/cycles/                 #    1.562 GHz                         (0.21%)
  12,44,40,67,433      cpu_core/cycles/                 #    4.359 GHz                         (99.79%)
   4,43,82,99,726      cpu_atom/instructions/           #    1.00  insn per cycle              (0.21%)
  58,73,60,46,416      cpu_core/instructions/           #    4.72  insn per cycle              (99.79%)
     10,34,55,099      cpu_atom/cache-misses/           #   85.51% of all cache refs           (0.21%)
      6,56,092         cpu_core/cache-misses/           #   11.64% of all cache refs           (99.79%)
          3,152        page-faults                      #    1.104 K/sec
       2,854.98 msec   task-clock                       #    0.921 CPUs utilized
     78,54,58,514      cpu_atom/branches/               #  275.118 M/sec                       (0.21%)
   2,57,35,46,196      cpu_core/branches/               #  901.422 M/sec                       (99.79%)
      46,02,879        cpu_atom/branch-misses/          #    0.59% of all branches             (0.21%)
      43,62,994        cpu_core/branch-misses/          #    0.17% of all branches             (99.79%)
   7,10,88,80,272      cpu_atom/bus-cycles/             #    2.490 G/sec                       (0.21%)
   7,12,56,40,281      cpu_core/bus-cycles/             #    2.496 G/sec                       (99.79%)
     12,09,83,299      cpu_atom/cache-references/       #   42.376 M/sec                       (0.21%)
      56,38,939        cpu_core/cache-references/       #    1.975 M/sec                       (99.79%)
   7,10,88,80,272      cpu_atom/ref-cycles/             #    2.490 G/sec                       (0.21%)
   7,12,56,40,216      cpu_core/ref-cycles/             #    2.496 G/sec                       (99.79%)

     3.099262782 seconds time elapsed

     2.832793000 seconds user
     0.023014000 seconds sys
```

Tiled Approach (Row method 32 x 32)

```
Performance counter stats for './col32':

   6,14,72,86,572      cpu_atom/cycles/                 #    2.084 GHz                         (0.28%)
  12,86,87,98,296      cpu_core/cycles/                 #    4.363 GHz                         (99.72%)
   6,91,50,59,033      cpu_atom/instructions/           #    1.12  insn per cycle              (0.28%)
  58,86,20,77,641      cpu_core/instructions/           #    4.57  insn per cycle              (99.72%)
     12,22,22,515      cpu_atom/cache-misses/           #   84.77% of all cache refs           (0.28%)
      10,52,017        cpu_core/cache-misses/           #   21.41% of all cache refs           (99.72%)
          3,147        page-faults                      #    1.067 K/sec
       2,949.60 msec   task-clock                       #    0.924 CPUs utilized
     98,56,47,088      cpu_atom/branches/               #  334.163 M/sec                       (0.28%)
   2,59,21,61,108      cpu_core/branches/               #  878.819 M/sec                       (99.72%)
      49,73,128        cpu_atom/branch-misses/          #    0.50% of all branches             (0.28%)
      39,16,812        cpu_core/branch-misses/          #    0.15% of all branches             (99.72%)
   7,33,11,56,196      cpu_atom/bus-cycles/             #    2.485 G/sec                       (0.28%)
   7,36,17,51,356      cpu_core/bus-cycles/             #    2.496 G/sec                       (99.72%)
     14,41,79,539      cpu_atom/cache-references/       #   48.881 M/sec                       (0.28%)
      49,12,629        cpu_core/cache-references/       #    1.666 M/sec                       (99.72%)
   7,33,11,56,196      cpu_atom/ref-cycles/             #    2.485 G/sec                       (0.28%)
   7,36,17,51,356      cpu_core/ref-cycles/             #    2.496 G/sec                       (99.72%)

     3.193328966 seconds time elapsed

     2.926064000 seconds user
     0.025000000 seconds sys
```

Tiled Approach (Row method 64 x 64)

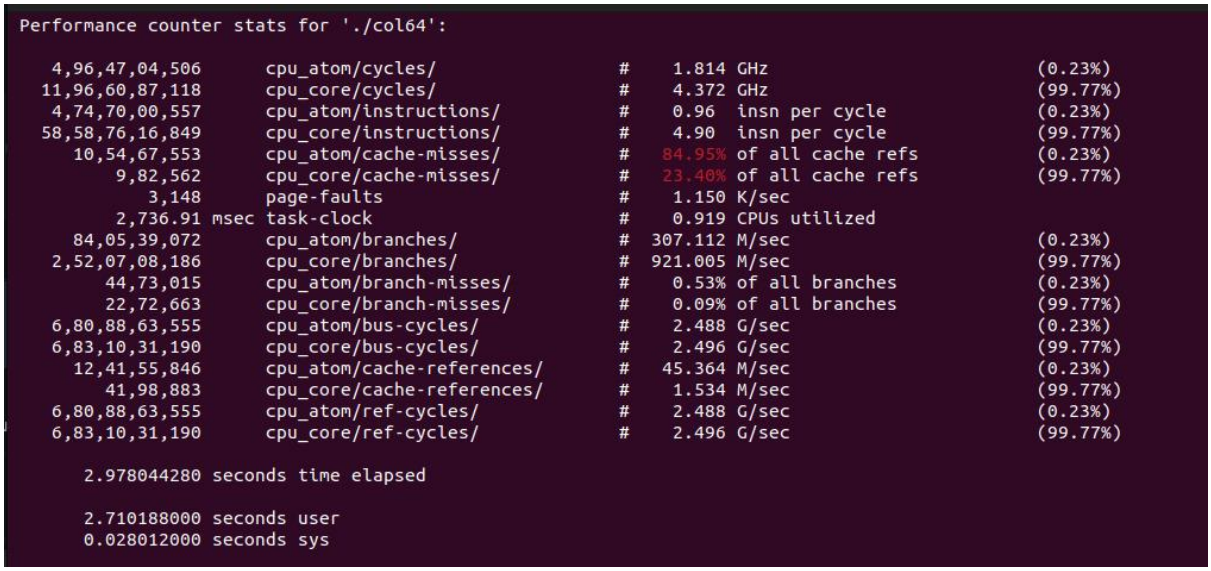
```
Performance counter stats for './row64':

   7,82,14,98,418      cpu_atom/cycles/                 #    2.884 GHz                         (0.77%)
  11,86,40,78,288      cpu_core/cycles/                 #    4.375 GHz                         (99.23%)
  21,95,32,94,348      cpu_atom/instructions/           #    2.81  insn per cycle              (0.77%)
  58,66,08,06,898      cpu_core/instructions/           #    4.94  insn per cycle              (99.23%)
      3,28,09,749      cpu_atom/cache-misses/           #   70.69% of all cache refs           (0.77%)
         8,80,744      cpu_core/cache-misses/           #   10.81% of all cache refs           (99.23%)
          3,153        page-faults                      #    1.163 K/sec
       2,712.01 msec   task-clock                       #    0.922 CPUs utilized
   5,16,49,05,456      cpu_atom/branches/               #    1.904 G/sec                       (0.77%)
   2,47,83,82,136      cpu_core/branches/               #  913.854 M/sec                       (99.23%)
      32,26,524        cpu_atom/branch-misses/          #    0.06% of all branches             (0.77%)
      23,73,030        cpu_core/branch-misses/          #    0.10% of all branches             (99.23%)
   6,75,35,67,978      cpu_atom/bus-cycles/             #    2.490 G/sec                       (0.77%)
   6,76,89,02,329      cpu_core/bus-cycles/             #    2.496 G/sec                       (99.23%)
      4,64,13,678      cpu_atom/cache-references/       #   17.114 M/sec                       (0.77%)
      81,47,616        cpu_core/cache-references/       #    3.004 M/sec                       (99.23%)
   6,75,35,67,978      cpu_atom/ref-cycles/             #    2.490 G/sec                       (0.77%)
   6,76,89,02,460      cpu_core/ref-cycles/             #    2.496 G/sec                       (99.23%)

     2.941359718 seconds time elapsed

     2.688385000 seconds user
     0.025003000 seconds sys
```

Tiled Approach (Column method 64 x 64)



```
Performance counter stats for './col64':

   4,96,47,04,506      cpu_atom/cycles/                 #    1.814 GHz                      (0.23%)
  11,96,60,87,118      cpu_core/cycles/                 #    4.372 GHz                      (99.77%)
   4,74,70,00,557      cpu_atom/instructions/           #    0.96  insn per cycle           (0.23%)
  58,58,76,16,849      cpu_core/instructions/           #    4.90  insn per cycle           (99.77%)
     10,54,67,553      cpu_atom/cache-misses/           #   84.95% of all cache refs        (0.23%)
      9,82,562         cpu_core/cache-misses/           #   23.40% of all cache refs        (99.77%)
          3,148        page-faults                      #    1.150 K/sec
          2,736.91 msec task-clock                      #    0.919 CPUs utilized
     84,05,39,072      cpu_atom/branches/               #  307.112 M/sec                    (0.23%)
   2,52,07,08,186      cpu_core/branches/               #  921.005 M/sec                    (99.77%)
      44,73,015        cpu_atom/branch-misses/          #    0.53% of all branches          (0.23%)
      22,72,663        cpu_core/branch-misses/          #    0.09% of all branches          (99.77%)
   6,80,88,63,555      cpu_atom/bus-cycles/             #    2.488 G/sec                    (0.23%)
   6,83,10,31,190      cpu_core/bus-cycles/             #    2.496 G/sec                    (99.77%)
     12,41,55,846      cpu_atom/cache-references/       #   45.364 M/sec                    (0.23%)
        41,98,883      cpu_core/cache-references/       #    1.534 M/sec                    (99.77%)
   6,80,88,63,555      cpu_atom/ref-cycles/             #    2.488 G/sec                    (0.23%)
   6,83,10,31,190      cpu_core/ref-cycles/             #    2.496 G/sec                    (99.77%)

      2.978044280 seconds time elapsed

      2.710188000 seconds user
      0.028012000 seconds sys
```

5. Advantages & Disadvantages

Non-Tiled Approach

Advantages:

- Simpler to implement
- No additional overhead for managing tiles

Disadvantages:

- Poor cache utilization
- Higher memory access latency
- Slower execution for large matrices

Tiled Approach

Advantages:

- Better cache performance
- Reduced memory access overhead
- Faster execution times for large matrices

Disadvantages:

- Requires careful tile size selection
- Additional implementation complexity

Comparison Table:

Test Case	CPU GHz	IPC	Cache Miss %	Execution Time (s)
col	1.395	4.32	79.15%	2.797
row	3.214	4.17	50.11%	2.899
row16	3.266	4.59	17.14%	3.168
col16	1.814	4.90	84.95%	2.978
row32	1.562	4.72	85.51%	3.099
col32	1.814	4.90	84.95%	2.978
row64	2.884	4.94	70.69%	2.941
col64	1.814	4.90	84.95%	2.978

From this analysis we can consider row64 has the best IPC which makes it most suitable but at the same time row16 is favourable for smaller cache memory as it has the least cache miss.

Column wise methods are slower and inefficient on intel core processors.

6. Conclusion

From the experiment, the tiled approach significantly improves performance over the non-tiled method due to efficient memory access. However, the optimal tile size varies based on system architecture, and excessively large or small tile sizes may degrade performance.

7. Case Study: Intel Core i5 vs. AMD Ryzen for Matrix Computation

Intel i5-12450H

- Strong single-thread performance
- Moderate cache size
- Decent power efficiency
- Row method is favoured.

AMD Ryzen (e.g., Ryzen 5 5600H)

- Better multi-thread performance
- Higher L3 cache size, which benefits tiled approaches
- Power efficiency varies based on workload
- Column method is favoured.

Conclusion:

For general matrix multiplication, AMD Ryzen processors tend to perform better in tiled approaches due to larger cache sizes and superior multi-threading capabilities. However, Intel i5 CPUs perform competitively in workloads favouring single-thread performance.