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S.E. (Comp.) Semester - I

DIGITAL ELECTRONICS AND LOGIC DESIGN

(For END SEM Exam - 70 Marks)

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S.E. (Computer Engineering) Semester - I

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PREFACE

The importance of **Digital Electronics and Logic Design** is well known in various engineering fields. Overwhelming response to our books on various subjects inspired us to write this book. The book is structured to cover the key aspects of the subject **Digital Electronics and Logic Design**.

The book uses plain, lucid language to explain fundamentals of this subject. The book provides logical method of explaining various complicated concepts and stepwise methods to explain the important topics. Each chapter is well supported with necessary illustrations, practical examples and solved problems. All the chapters in the book are arranged in a proper sequence that permits each topic to build upon earlier studies. All care has been taken to make students comfortable in understanding the basic concepts of the subject.

Representative questions have been added at the end of each section to help the students in picking important points from that section.

The book not only covers the entire scope of the subject but explains the philosophy of the subject. This makes the understanding of this subject more clear and makes it more interesting. The book will be very useful not only to the students but also to the subject teachers. The students have to omit nothing and possibly have to cover nothing more.

We wish to express our profound thanks to all those who helped in making this book a reality. Much needed moral support and encouragement is provided on numerous occasions by our whole family. We wish to thank the **Publisher** and the entire team of **Technical Publications** who have taken immense pain to get this book in time with quality printing.

Any suggestion for the improvement of the book will be acknowledged and well appreciated.

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Dedicated to God

SYLLABUS

Digital Electronics and Logic Design (210245)

Credit	Examination Scheme and Marks
03	End_Semester (TH) : 70 Marks

Unit III Sequential Logic Design

Flip-Flop : SR, JK,D,T, Preset and Clear, Master Slave JK Flip Flops, Truth Tables and Excitation tables, Conversion from one type to another type of Flop-Flop. Registers: SISO, SIPO, PISO, PIPO, Shift Registers, Bidirectional Shift Register, Ring Counter, Universal Shift Register. Counters : Asynchronous Counter, Synchronous Counter, BCD Counter, Johnson Counter, Modulus of the counter (IC7490). Synchronous Sequential Circuit Design :Models- Moore and Mealy, State diagram and State Table, Design Procedure, Sequence Generator and detector. **(Chapters - 4, 5, 6, 7)**

Unit IV Algorithmic State Machines and Programmable Logic Devices

Algorithmic State Machines : Finite State Machines (FSM) and ASM, ASM charts, notations, construction of ASM chart and realization for sequential circuits. PLDS : PLD, ROM as PLD, Programmable Logic Array (PLA), Programmable Array Logic (PAL), Designing combinational circuits using PLDs. **(Chapters - 8, 9)**

Unit V Logic Families

Classification of logic families : Unipolar and Bipolar Logic Families, Characteristics of Digital ICs : Fan-in, Fan-out, Current and voltage parameters, Noise immunity, Propagation Delay, Power Dissipation, Figure of Merits, Operating Temperature Range, power supply requirements. **Transistor-Transistor Logic** : Operation of TTL NAND Gate (Two input), TTL with active pull up, TTL with open collector output, Wired AND Connection, Tristate TTL Devices, TTL characteristics. **CMOS** : CMOS Inverter, CMOS characteristics, CMOS configurations- Wired Logic, Open drain outputs. **(Chapter - 10)**

Unit VI Introduction to Computer Architecture

Introduction to Ideal Microprocessor - Data Bus, Address Bus, Control Bus. Microprocessor based Systems - Basic Operation, Microprocessor operation, Block Diagram of Microprocessor.

Functional Units of Microprocessor - ALU using IC 74181, Basic Arithmetic operations using ALU IC 74181, 4-bit Multiplier circuit using ALU and shift registers. Memory Organization and Operations, digital circuit using decoder and registers for memory operations. **(Chapter - 11)**

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UNIT - III

4

Flip-Flops

Syllabus

SR, JK,D,T, Preset and Clear, Master Slave JK Flip Flops, Truth Tables and Excitation tables, Conversion from one type to another type of Flop-Flop.

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4.1	<i>Introduction</i>	May-17,19,	Marks 4
4.2	<i>One-Bit Memory Cell</i>			
4.3	<i>Latches</i>			
4.4	<i>Flip-Flops</i>	May-05,06,07,11,12,13,	Marks 10
4.5	<i>Excitation Tables</i>	Dec.-05,06,10	
4.6	<i>Conversion from One Type to Another Type of Flip-Flop</i>	Dec.-13, May-15,	Marks 2
4.7	<i>Applications of Flip-Flops</i>	May-06,10,12, Dec.-16,17,19	Marks 4

4.1 Introduction

SPPU : May-17,19

There are many applications in which digital outputs are required to be generated in accordance with the sequence in which the input signals are received. This requirement cannot be satisfied using a combinational logic system. These applications require outputs to be generated that are not only dependent on the present input conditions but they also depend upon the past history of these inputs. The past history is provided by feedback from the output back to the input.

Fig. 4.1.1 shows the block diagram of sequential circuit/Finite State Machine (FSM). As shown in the Fig. 4.1.1, memory elements are connected to the combinational circuit as a feedback path.

The information stored in the memory elements at any given time defines the **present state** of the sequential circuit. The present state and the external inputs determine the outputs and the **next state** of the sequential circuit. Thus we can specify the sequential circuit by a time sequence of external inputs, internal states (present states and next states), and outputs. The counters and registers are the common examples of sequential circuits.

The memory element used in sequential circuits is a flip-flop which is capable of storing 1-bit binary information.

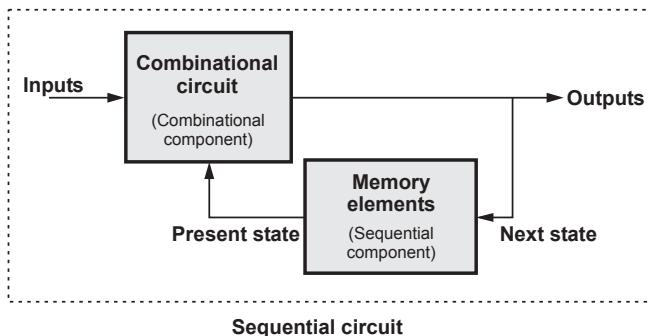


Fig. 4.1.1 Block diagram of sequential circuit / FSM

4.1.1 Comparison between Combinational and Sequential Logic Circuits

Sr. No.	Combinational circuits	Sequential circuits
1.	In combinational circuits, the output variables are at all times dependent on the combination of input variables.	In sequential circuits, the output variables depend not only on the present input variables but they also depend upon the past history of these input variables.
2.	Memory unit is not required in combinational circuits.	Memory unit is required to store the past history of input variables in the sequential circuit.
3.	Combinational circuits are faster in speed because the delay between input and output is due to propagation delay of gates.	Sequential circuits are slower than the combinational circuits.

4.	Combinational circuits are easy to design.	Sequential circuits are comparatively harder to design.
5.	Parallel adder is a combinational circuit.	Serial adder is a sequential circuit.

Table 4.1.1 Comparison between combinational and sequential circuits**4.1.2 Clock**

A clock signal is a particular type of signal that oscillates between a high and a low state and is utilized to co-ordinate actions of circuits. It is produced by a clock generator. The most common clock signal is in the form of a square wave with a 50 % duty cycle, usually with a fixed, constant frequency as shown in Fig. 4.1.2. Circuits using the clock signal for synchronization may become active at either the rising edge, falling edge or in the case of double data rate, both in the rising and in the falling edges of the clock cycle.

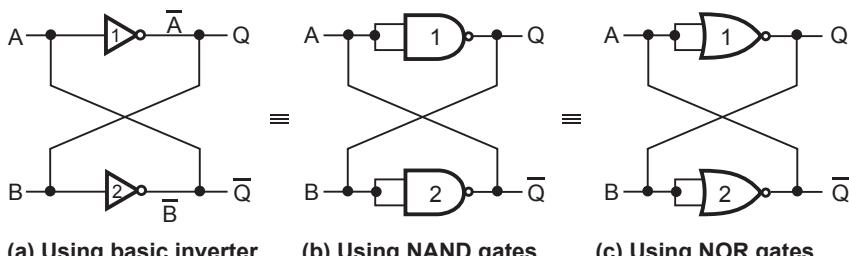
The time required to complete one cycle is called '**clock period**' or '**clock cycle**'. Ideally, the clock signal should have sharp transitions from one level to other as shown in Fig. 4.1.2.

**Fig. 4.1.2 Clock signal****Review Questions**

1. Define sequential logic circuit.
2. What is flip-flop?
3. Give the comparison between combinational and sequential logic circuits.
4. What is clock? State its use.

SPPU : May-17,19, Marks 4**4.2 One-Bit Memory Cell**

The Fig. 4.2.1 shows the basic bistable element used in latches and flip-flops. The basic bistable element has two outputs Q and \bar{Q} . It has two cross-coupled inverters, i.e., the output of the first inverter is connected as an input to the second inverter and the output of second inverter is connected as an input to the first inverter.

**Fig. 4.2.1 Basic bistable element (1-bit memory cell)**

The basic bistable element circuit has two stable states logic 0 and logic 1, hence the name 'bistable'. To illustrate this, assume $A = 0$. When $A = 0$, the output of inverter 1 is 1 (\bar{A}), i.e., $Q = 1$. Since the output of inverter 1 is the input to the inverter 2, $\bar{A} = B = 1$. Consequently, the output of inverter 2, i.e., \bar{B} is 0. Since the output of the inverter 2 is connected to the input of the inverter 1, $\bar{Q} = \bar{B} = A = 0$. We have assumed same value for A. Thus, the circuit is stable with $\bar{Q} = A = \bar{B} = 0$ and $Q = \bar{A} = B = 1$. Using similar explanation it is easy to show that if it is assumed that $A = 1$, the basic bistable element is stable with $\bar{Q} = A = \bar{B} = 1$ and $Q = \bar{A} = B = 0$. This is a second stable condition of the basic bistable element.

The two stable states of basic bistable elements are used to store two binary elements, 0 and 1. In positive logic system, state $Q = 1$ is used to store logic 1, and state $Q = 0$ is used to store logic 0. It is important to note that the two outputs are complementary. That is when $Q = 0$, $\bar{Q} = 1$; and when $Q = 1$, $\bar{Q} = 0$.

From the above discussion we can note following things about the basic bistable element.

1. The outputs Q and \bar{Q} are always complementary.
2. The circuit has two stable states. The state corresponds to $Q = 1$ is referred to as **1 state** or **set state** and state corresponds to $Q = 0$ is referred to as **0 state** or **Reset state**.
3. If the circuit is in the set (1) state, it will remain in the set state and if the circuit is in the reset (0) state, it will remain in the reset state. This property of the circuit shows that it can store 1-bit of digital information. Therefore, the circuit is called a **1-bit memory cell**.
4. The 1-bit information stored in the circuit is locked or latched in the circuit. Therefore, this circuit is also referred to as a **latch**.

Review Question

1. Explain the operation of one-bit memory cell.

4.3 Latches

4.3.1 SR Latch

Fig. 4.3.1 shows SR latch which is 1-bit memory cell. As shown in the Fig. 4.3.1, two inverters 3 and 4 are connected to enter the digital information. Input for gate 3 is **S** and input for gate 4 is **R**. This latch is also called **RS latch**.

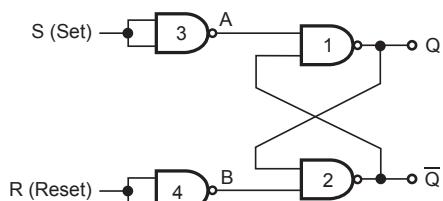


Fig. 4.3.1 SR latch

For understanding the circuit operation, we must first determine the output of NAND gate whose one of the input is logic 0 and accordingly we have to determine the output of other NAND gate in the cross coupled circuit. Because the output of NAND gate is 1 if any one input is 0. The circuit operation is as follows. In Fig. 4.3.2, the output of shaded NAND gate is determined first, and the 0 input that decides the output of shaded NAND as 1 is shown in bold.

Case 1 : $S = R = 0$

In this case, $\bar{S} = \bar{R} = 1$. If Q is 1, Q and \bar{R} inputs for NAND gate 2 are both 1 and hence output $\bar{Q} = 0$. Since $\bar{Q} = 0$ and $\bar{S} = 1$, the output of NAND gate 1 is 1, i.e. $Q = 1$.

If Q is 0, Q and \bar{R} inputs for NAND gate 2 are 0 and 1, and hence output $\bar{Q} = 1$. Since $\bar{Q} = 1$ and $\bar{S} = 1$, the output of NAND gate 1 is 0, i.e., $Q = 0$.

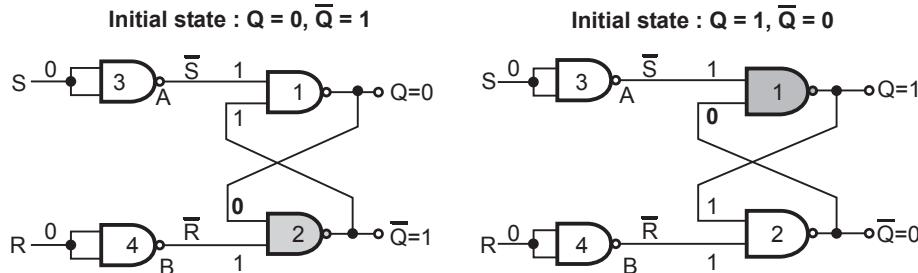


Fig. 4.3.2

This shows that when $S = R = 0$, the outputs do not change.

Case 2 : $S = 1$ and $R = 0$

In this case, $\bar{S} = 0$ and $\bar{R} = 1$. Since $\bar{S} = 0$, the output of NAND gate 1, $Q = 1$ (Recall that, for NAND any one or more input is 0, the output is 1) For NAND gate 2, both inputs Q and \bar{R} are 1, thus output $\bar{Q} = 0$.

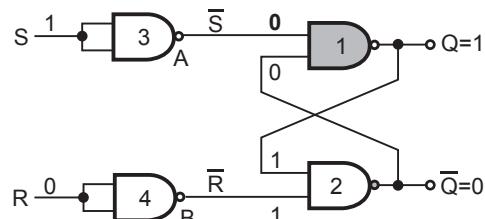


Fig. 4.3.3

The inputs $S = 1$ and $R = 0$, makes $Q = 1$, i.e., **set** state.

Case 3 : $S = 0$ and $R = 1$

In this case, $\bar{S} = 1$ and $\bar{R} = 0$. Since $\bar{R} = 0$, the output of NAND gate 2, $\bar{Q} = 1$. For NAND gate 1, both inputs \bar{Q} and \bar{S} are 1, thus output $Q = 0$.

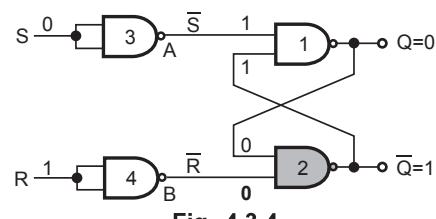


Fig. 4.3.4

The inputs $S = 0$ and $R = 1$, makes $Q = 0$, i.e., **reset** state.

Case 4 : S = 1 and R = 1

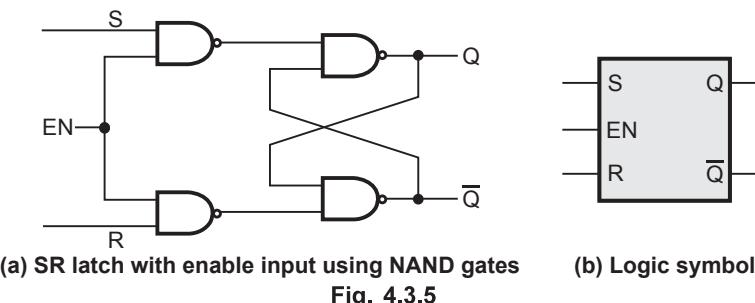
When S = R = 1, both the outputs Q and \bar{Q} try to become 1 which is not allowed and therefore, this input condition is prohibited.

4.3.2 Gated SR Latch

In the SR latch we have seen that output changes occur immediately after the input changes occur i.e. the latch is sensitive to its S and R inputs at all times. However, it can easily be modified to create a latch that is sensitive to these inputs only when an enable input is active. Such a latch with enable input is known as **gated SR latch**. It is as shown in the Fig. 4.3.5. The Table 4.3.1 shows the truth table for gated latch. As shown by truth table, the circuit behaves like a SR latch when EN = 1, and retains its previous state when EN = 0.

EN	S	R	Q_n	Q_{n+1}	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	X	Indeterminate
1	1	1	1	X	
0	X	X	0	0	No Change (NC)
0	X	X	1	1	

Table 4.3.1 Truth table for SR latch with enable input



(a) SR latch with enable input using NAND gates (b) Logic symbol

Fig. 4.3.5

4.3.3 Gated D Latch

Looking at the truth table of the SR latch we can realize that when both inputs are same the output either does not change or it is invalid (Inputs \rightarrow 00, no change and inputs \rightarrow 11, invalid). In many practical applications, these input conditions are not required. These input conditions can be avoided by making them complement of each other. This modified SR latch is known as D latch.

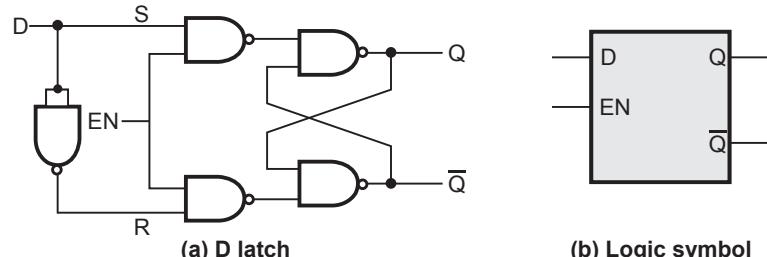


Fig. 4.3.6 shows the D latch. The NAND gates 1,

Fig. 4.3.6

2, 3 and 4 form the basic SR latch with enable input. The fifth NAND gate is used to provide the complemented inputs.

As shown in the Fig. 4.3.6, D input goes directly to the S input, and its complement is applied to the R input, through gate 5. Therefore, only two input conditions exists, either $S = 0$ and $R = 1$ or $S = 1$ and $R = 0$. The truth table for D latch is as shown in the Table 4.3.2.

As shown in the truth table, the Q output follows the D input. For this reason D latch is sometimes called **transparent latch**.

Looking at the truth table for D latch with enable input and simplifying Q_{n+1} function by k-map we get the characteristic equation for D latch with enable input as $Q_{n+1} = EN \cdot D + \bar{EN} \cdot Q_n$. This is illustrated in Fig. 4.3.7.

EN	D	Q_n	Q_{n+1}	State
1	0	X	0	Reset
1	1	X	1	Set
0	X	X	Q_n	No Change (NC)

Table 4.3.2 Truth table for D latch

EN	D Q_n			
	00	01	11	10
0	Q_n	Q_n	Q_n	Q_n
1	0	0	1	1

$$Q_{n+1} = EN \cdot D + \bar{EN} \cdot Q_n$$

Fig. 4.3.7 Characteristic equation

Review Questions

1. What is SR latch ? Explain it's operation.
2. What is gated SR latch ?
3. Explain the working of gated D latch with truth table and characteristic equation.

4.4 Flip-Flops

SPPU : May-05,06,07,11,12,13, Dec.-05,06,10

4.4.1 Latches Vs Flip-Flops

Latches and flip-flops are the basic building blocks of the most sequential circuits. The main difference between latches and flip-flops is in the method used for changing their state.

A simple latch forms the basis for the flip-flop. Latches are controlled by enable signal, and they are level triggered, either positive level triggered or negative level triggered. The output state is free to change according to the S and R input values, when active level is maintained at the enable input. Flip-flops are different from latches. Flip-flops are pulse or clock edge triggered instead of level triggered.

4.4.2 Level and Edge Triggering

Level Triggering

In the level triggering, the output state is allowed to change according to input(s) when active level (either positive or negative) is maintained at the enable input. There are two types of level triggered latches :

- **Positive level triggered** : The output of flip-flop responds to the input changes only when its enable input is 1 (HIGH).

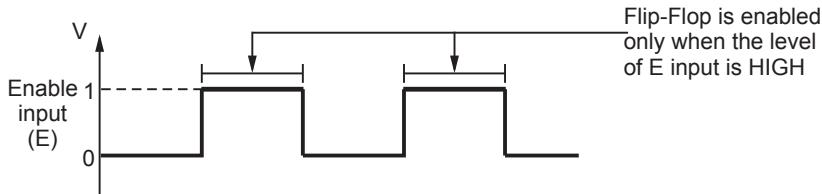


Fig. 4.4.1 Positive level triggering

- **Negative level triggered** : The output of flip-flop responds to the input changes only when its enable input is 0 (LOW).

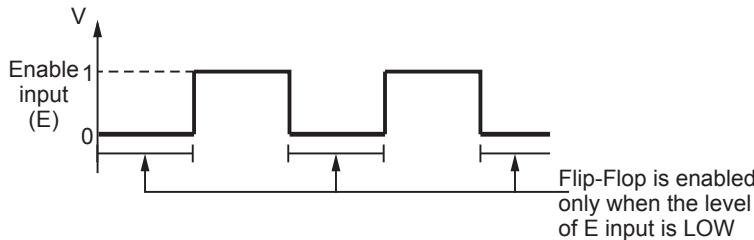


Fig. 4.4.2 Negative level triggering

Edge Triggering

In the edge triggering, the output responds to the changes in the input only at the positive or negative edge of the clock pulse at the clock input. There are two types of edge triggering.

- **Positive edge triggering** : Here, the output responds to the changes in the input only at the positive edge of the clock pulse at the clock input.

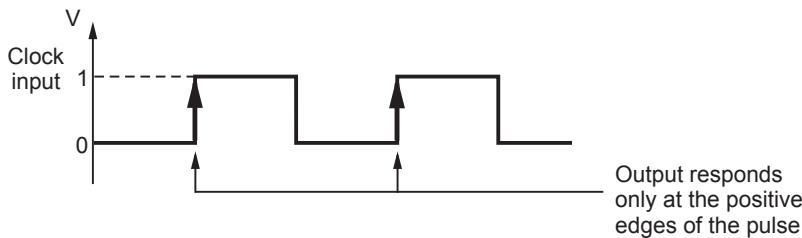


Fig. 4.4.3 Positive edge triggering

- **Negative edge triggering** : Here, the output responds to the changes in the input only at the negative edge of the clock pulse at the clock input.

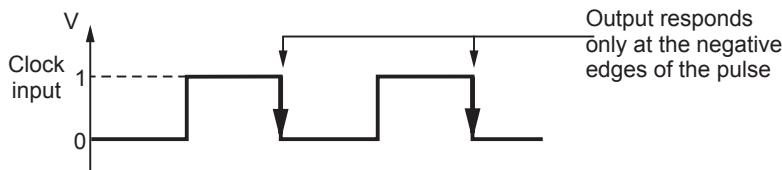


Fig. 4.4.4 Negative edge triggering

4.4.3 SR Flip-Flop

Positive Edge Triggered SR Flip-Flop

The Fig. 4.4.5 shows the positive edge triggered clocked SR flip-flop. The circuit is similar to SR latch except enable signal is replaced by the Clock Pulse (CP) followed by the positive edge detector circuit. The edge detector circuit is a differentiator. The Fig. 4.4.7 shows input and output waveforms for positive edge triggered clocked SR flip-flop. As shown in Fig. 4.4.7 the circuit output responds to the S and R inputs only at the positive edges of the clock pulse. At any other instants of time, the SR flip-flop will not respond to the changes in input.

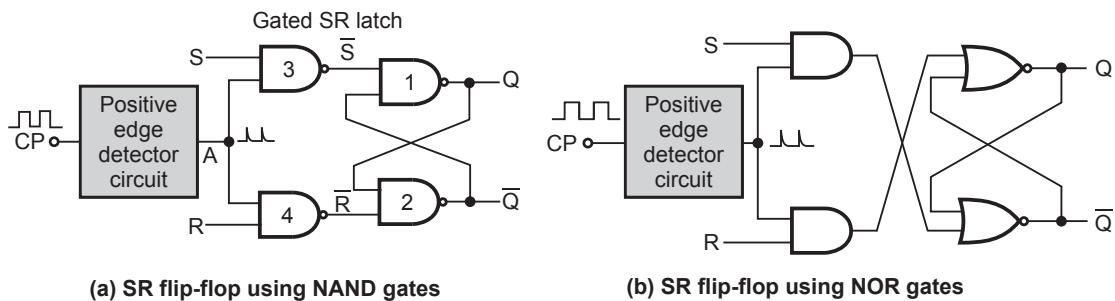
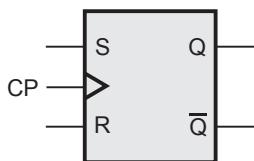


Fig. 4.4.5 Clocked SR flip-flop

The Fig. 4.4.6 shows the logic symbol and truth table of clocked SR flip-flop.



(a) Logic symbol

CP	S	R	Q_n	Q_{n+1}	State
\uparrow	0	0	0	0	No Change(NC)
\uparrow	0	0	1	1	
\uparrow	0	1	0	0	
\uparrow	0	1	1	0	Reset
\uparrow	1	0	0	1	
\uparrow	1	0	1	1	Set
\uparrow	1	1	0	X	
\uparrow	1	1	1	X	Indeterminate
0	X	X	0	0	No Change(NC)
0	X	X	1	1	

(b) Truth table for positive edge clocked SR flip-flop

SR	Q _n	0	1
00	0	0	1
01	0	0	0
11	X	X	X
10	1	1	0

$$Q_{n+1} = S + \bar{R} Q_n$$

(c) Characteristic equation

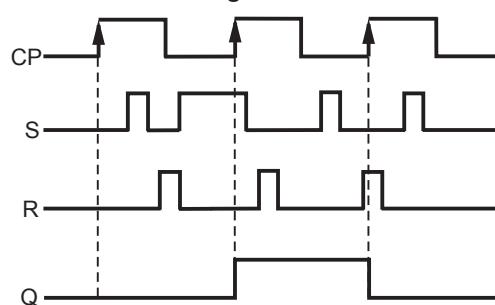
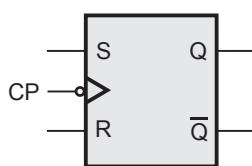


Fig. 4.4.7 Input and output waveforms for positive edge triggered clocked SR flip-flop

- Case 1 :** If $S = R = 0$ and the clock pulse is applied, the output do not change, i.e. $Q_{n+1} = Q_n$. This is indicated in the first row of the truth table.
- Case 2 :** If $S = 0, R = 1$ and the clock pulse is applied, $Q_{n+1} = 0$. This is indicated in the second row of the truth table.
- Case 3 :** If $S = 1, R = 0$ and the clock pulse is applied, $Q_{n+1} = 1$. This is indicated in the third row of the truth table.
- Case 4 :** If $S = R = 1$ and the clock pulse is applied, the state of the flip-flop is undefined and therefore is indicated as indeterminate in the fourth row of the truth table.

Negative Edge Triggered SR Flip-Flop

In the negative edge triggered SR flip-flop, the negative edge detector circuit is used and the circuit output responds at the negative edges of the clock pulse. The Fig. 4.4.8 and Fig. 4.4.9 shows the logic symbol, truth table, and input and output waveforms for negative edge triggered SR flip-flop. The bubble at the clock input indicates that the flip-flop is negative edge triggered.



(a) Logic symbol

CP	S	R	Q_n	Q_{n+1}	State
↓	0	0	0	0	No change(NC)
↓	0	0	1	1	
↓	0	1	0	0	Reset
↓	0	1	1	0	
↓	1	0	0	1	Set
↓	1	0	1	1	
↓	1	1	0	X	Indeterminate
↓	1	1	1	X	
0	X	X	0	0	No change(NC)
0	X	X	1	1	

(b) Truth Table for negative edge clocked SR flip-flop

Fig. 4.4.8

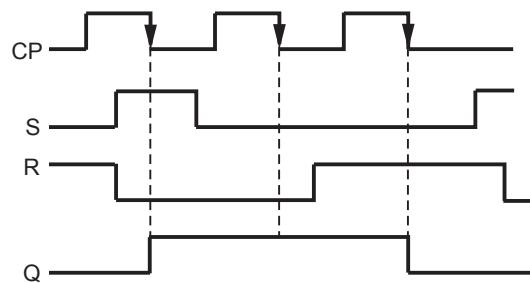


Fig. 4.4.9 Input and output waveforms for negative edge triggered clocked SR flip-flop

Example 4.4.1 Realize SR flip-flop using NOR gates.

Solution :

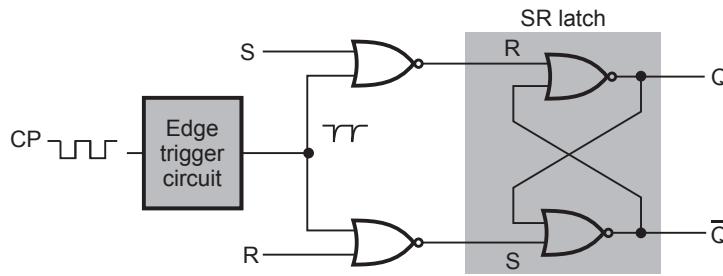
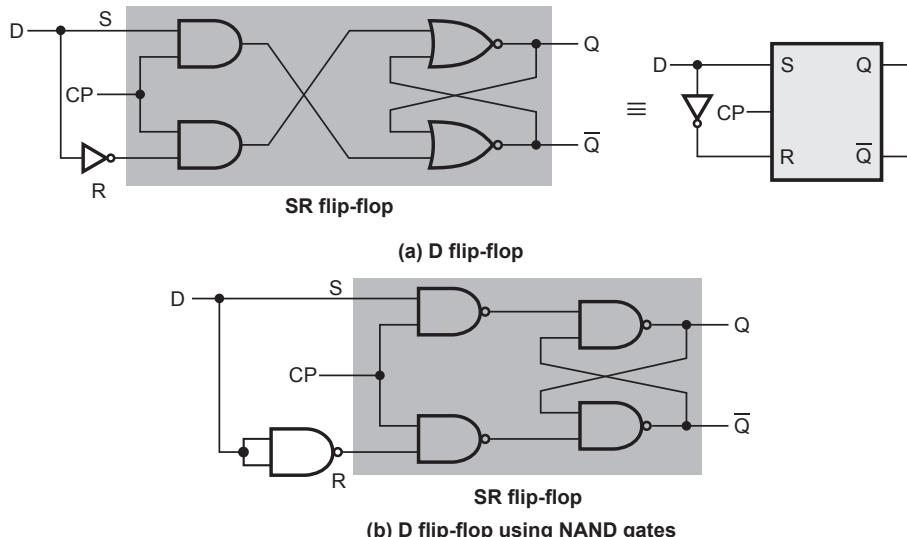


Fig. 4.4.10 Negative edge-triggered SR flip-flop using only NOR gates

4.4.4 D Flip-Flop

The Fig. 4.4.11 shows the logic diagrams of D flip-flop. The basic building block of D flip-flop is a SR flip-flop. The SR flip-flop has two data inputs S and R. The S input is made high to store 1 in the flip-flop and R input is made high to store 0 in the flip-flop.



(b) D flip-flop using NAND gates

Fig. 4.4.11

Looking at the truth table of the SR flip-flop we can realize that when both inputs are same the output either does not change or it is invalid (Inputs \rightarrow 00, no change and inputs \rightarrow 11, invalid). In many practical applications, these input conditions are not required. These input conditions can be avoided by making them complement of each other. This modified SR flip-flop is known as D flip-flop.

As shown in the Fig. 4.4.11, the D input goes directly to the S input, and its complement is applied to the R input. Due to these connections, only two input

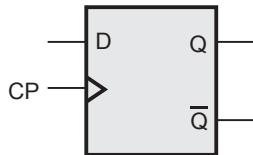


Fig. 4.4.12 (a) Logic symbol

CP	D	Q_{n+1}
\uparrow	0	0
\uparrow	1	1
0	X	Q_n

Fig. 4.4.12 (b) Truth table of D flip-flop

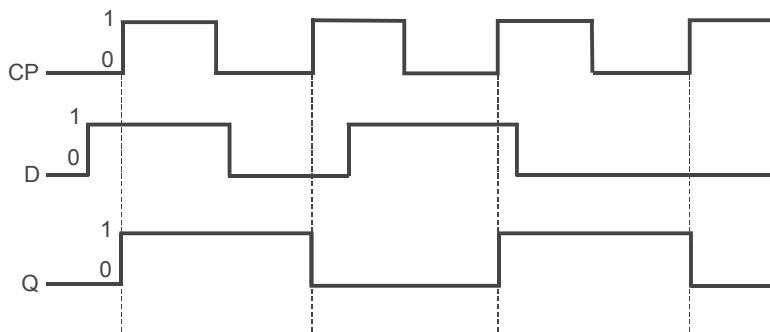


Fig. 4.4.12 (c) Input and output waveforms of clocked D flip-flop

conditions exists, either $S = 0$ and $R = 1$ or $S = 1$ and $R = 0$. The truth table for D flip-flop consider only these two conditions and it is as shown in the Fig. 4.4.12 (b).

Looking at the truth table for D flip-flop we can realize that Q_{n+1} function follows D input at the positive going edges of the clock pulses. Hence the characteristic equation for D flip-flop is $Q_{n+1} = D$. However, the output Q_{n+1} is delayed by one clock period. Thus, D flip-flop is also known as **delay flip-flop**.

If we connect the \bar{Q} output of D flip-flop to its D input as shown in the Fig. 4.4.13, the output of D flip-flop will change either from 0 to 1 or from 1 to 0 at every positive edge of the D flip-flop.

Such change in the output is known as **toggling** of the flip-flop output.

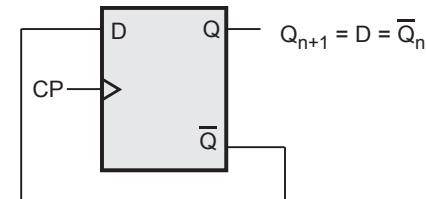
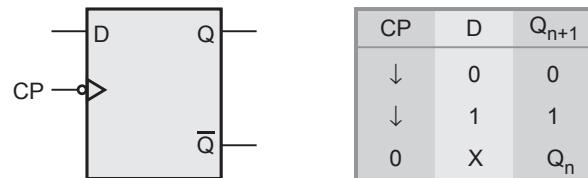


Fig. 4.4.13

Negative Edge Triggered D Flip-Flop

In the previous explanation we have seen the output of D flip-flop is sensitive at the positive edge of the clock input. In case of negative edge triggering, the output is sensitive at the negative edge of the clock input. The Fig. 4.4.14 shows the logic symbol and truth table for negative edge triggered D flip-flop and Fig. 4.4.15 shows input and output waveforms for negative edge triggered D flip-flop. The bubble at the clock input indicates that the flip-flop is negative edge triggered.



(a) Logic symbol

(b) Truth table of D flip-flop

Fig. 4.4.14

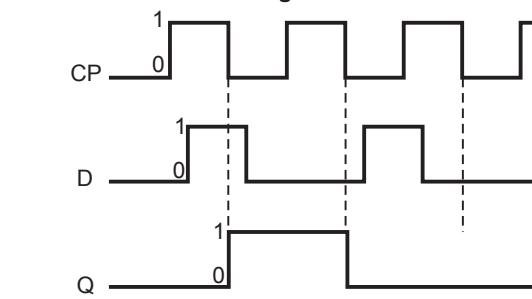


Fig. 4.4.15 Input output waveforms of negative edge triggered D flip-flop

4.4.5 JK Flip-Flop

The uncertainty in the state of an SR flip-flop when $S = R = 1$ can be eliminated by converting it into a JK flip-flop. The data inputs are J and K which are ANDed with Q and \bar{Q} , respectively, to obtain S and R inputs, as shown in the Fig. 4.4.16. Thus, $S = J \cdot \bar{Q}$ and $R = K \cdot Q$.

Let us see the operation of JK flip-flop.

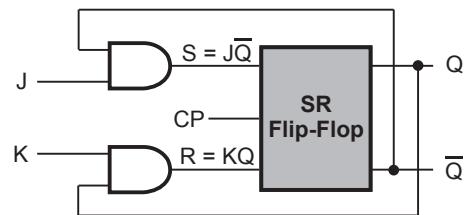


Fig. 4.4.16 JK flip-flop using SR flip-flop

Case 1 : $J = K = 0$

When $J = K = 0$, $S = R = 0$ and according to truth table of SR flip-flop there is no change in the output.

When inputs $J = K = 0$, output does not change.

Case 2 : $J = 1$ and $K = 0$

$Q = 0, \bar{Q} = 1$: When $J = 1, K = 0$ and $Q = 0$, $S = 1$ and $R = 0$. According to truth table of SR flip-flop it is **set** state and the output Q will be 1.

$Q = 1, \bar{Q} = 0$: When $J = 1, K = 0$ and $Q = 1$, $S = 0$ and $R = 0$. Since $SR = 00$, there is no change in the output and therefore, $Q = 1$ and $\bar{Q} = 0$.

The inputs $J = 1$ and $K = 0$, makes $Q = 1$, i.e. **set** state.

Case 3 : $J = 0$ and $K = 1$

$Q = 0, \bar{Q} = 1$: When $J = 0, K = 1$ and $Q = 0$, $S = 0$ and $R = 0$. Since $SR = 00$, there is no change in the output and therefore, $Q = 0$ and $\bar{Q} = 1$.

$Q = 1, \bar{Q} = 0$: When $J = 0, K = 1$ and $Q = 1$, $S = 0$ and $R = 1$. According to truth table of SR flip-flop it is a **reset** state and the output Q will be 0.

The inputs $J = 0$ and $K = 1$, makes $Q = 0$, i.e., **reset** state.

Case 4 : $J = K = 1$

$Q = 0, \bar{Q} = 1$: When $J = K = 1$ and $Q = 0$, $S = 1$ and $R = 0$. According to truth table of SR flip-flop it is a set state and the output Q will be 1.

$Q = 1, \bar{Q} = 0$: When $J = K = 1$ and $Q = 1$, $S = 0$ and $R = 1$. According to truth table of SR flip-flop it is a reset state and the output Q will be 0.

The input $J = K = 1$, toggles the flip-flop output.

The Fig. 4.4.17 shows the logic symbol, truth table and timing diagram of positive edge triggered JK flip-flop.

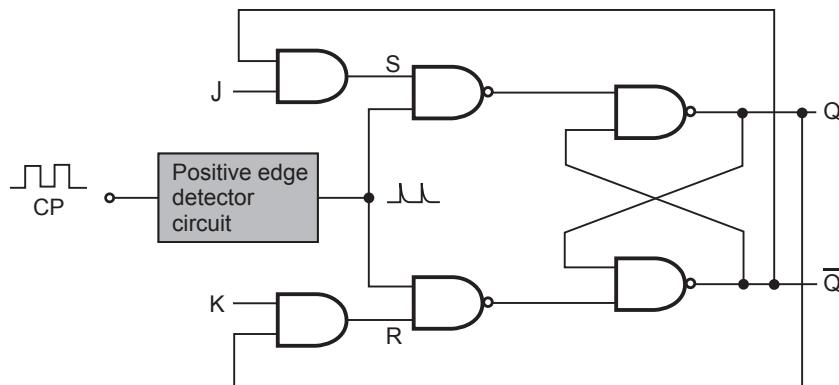


Fig. 4.4.17 (a) Clocked JK flip-flop

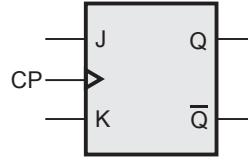


Fig. 4.4.17 (b) Logic symbol

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n

Fig. 4.4.17 (c) Truth table

Q_n	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$$Q_{n+1} = \bar{Q}_n J + Q_n \bar{K} = J \bar{Q}_n + \bar{K} Q_n$$

Fig. 4.4.17 (d) Characteristics equation

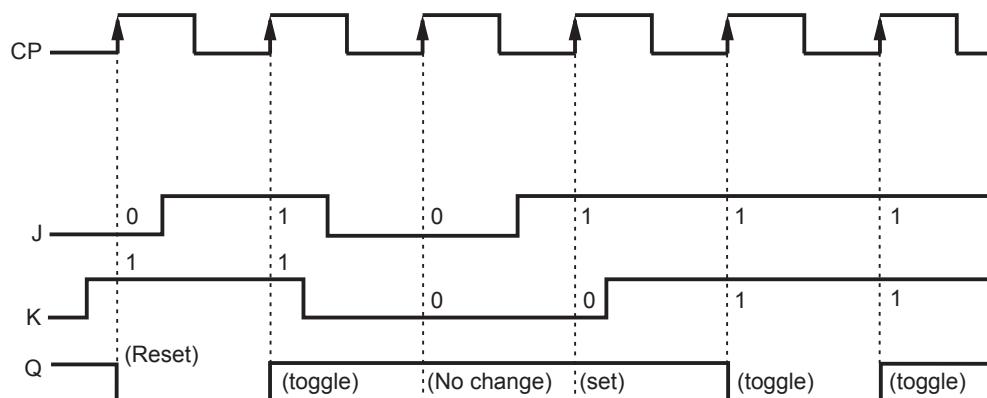


Fig. 4.4.18 Input and output waveforms for positive edge triggered JK flip-flop

Example 4.4.2 Construct a clocked JK flip-flop which is triggered at the positive edge of the clock pulse from a clocked SR flip-flop consisting of NOR gates.

Solution :

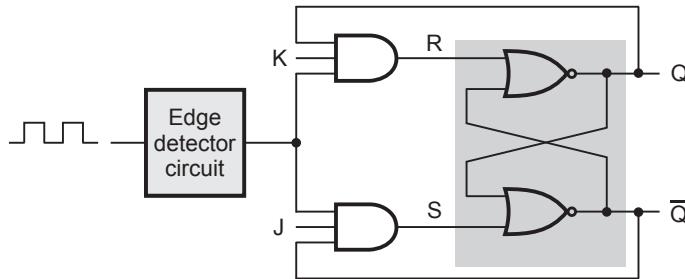


Fig. 4.4.19

4.4.5.1 JK Flip-Flop using NAND Gates

In the previous section we have seen the operation of JK flip-flop using SR flip-flop and AND gates. It is not necessary to use the AND gates of Fig. 4.4.17 (a), since the same function can be performed by adding an extra input terminal to NAND gates 3 and 4 of Fig. 4.4.20. The Fig. 4.4.20 shows the modified circuit of JK flip-flop which has only NAND gates.

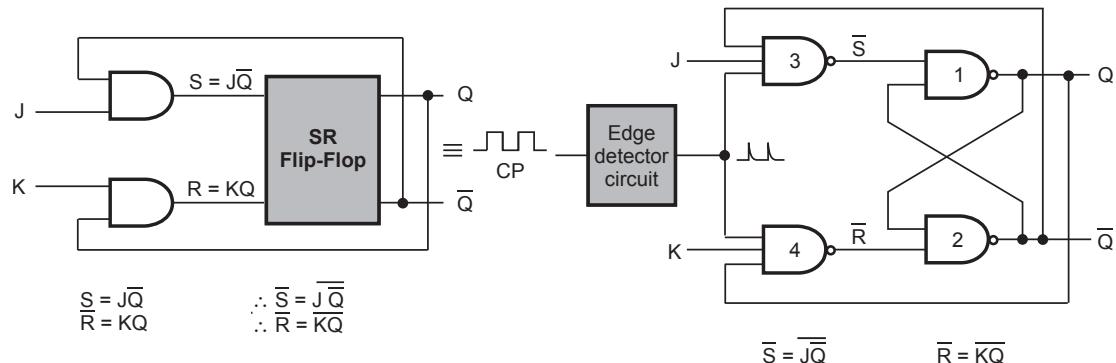


Fig. 4.4.20 JK flip-flop using NAND gates

4.4.5.2 Race-around Condition

In JK flip-flop, when $J = K = 1$, the output toggles (output changes either from 0 to 1 or from 1 to 0). Consider that initially $Q = 0$ and $J = K = 1$. After a time interval Δt equal to the propagation delay through two NAND gates in series, the output will change to $Q = 1$ and after another time interval of Δt the output will change back to $Q = 0$. This toggling will continue until the flip-flop is enabled and $J = K = 1$. At the end of clock pulse the flip-flop is disabled and the value of Q is uncertain. This situation is referred to as the **race-around condition**. This is illustrated in Fig. 4.4.21. This condition exists when $t_p \geq \Delta t$. Thus by keeping $t_p < \Delta t$ we can avoid race around condition.

We can keep $t_p < \Delta t$ by keeping the duration of edge less than Δt . A more practical method for overcoming this difficulty is the use of the Master-Slave (MS) configuration.

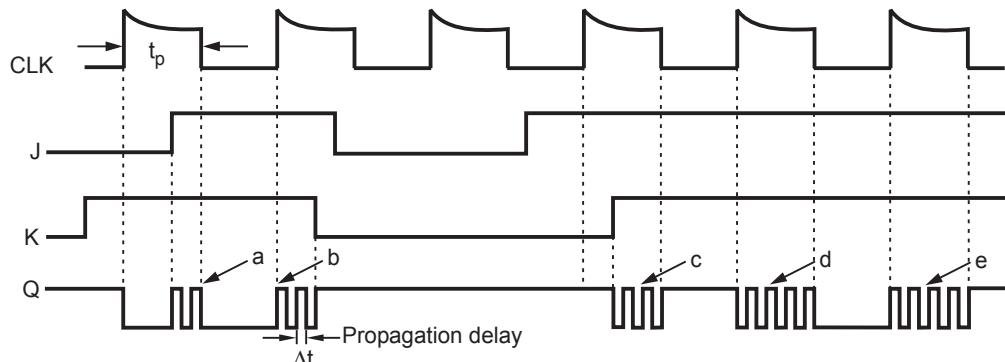


Fig. 4.4.21 Input and output waveforms for clocked JK flip-flop

Example 4.4.3 Realize a JK flip-flop using only NOR gates.

Solution :

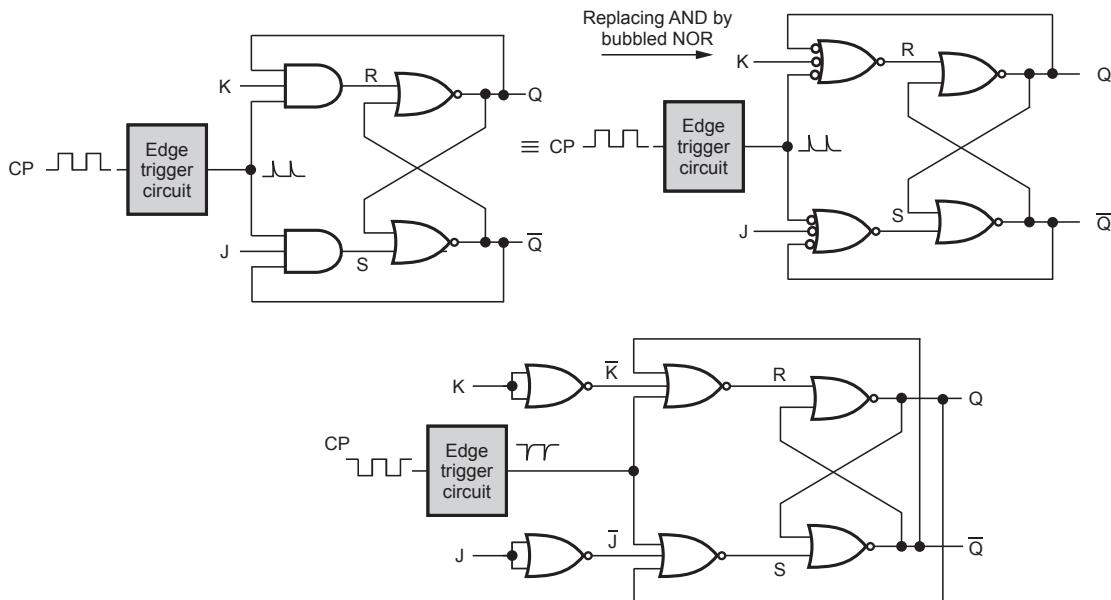


Fig. 4.4.22 Negative edge triggered JK flip-flop using only NOR gates

4.4.6 Master-Slave SR Flip-Flop

A master-slave flip-flop is constructed from two flip-flops. One circuit serves as a master and the other as a slave, and the overall circuit is referred to as a CP master-slave flip-flop. Fig. 4.4.23 shows SR master-slave flip-flop. It

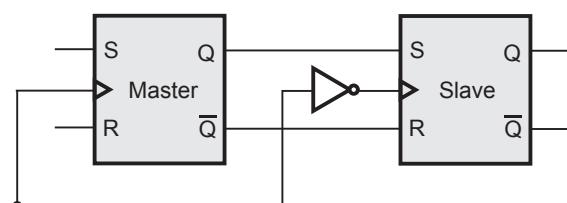


Fig. 4.4.23 Master-slave SR flip-flop

consists of a master flip-flop, a slave flip-flop, and an inverter. Both the flip-flops are

positive level triggered, but inverter connected at the clock input of the slave flip-flop forces it to trigger at the negative level.

The output state of the master flip-flop is determined by the S and R inputs at the positive clock pulse. The output state of the master is then transferred as an input to the slave flip-flop. The slave flip-flop uses this input at the negative clock pulse to determine its output state. The Fig. 4.4.24 illustrates the operation of the master-slave flip-flop.

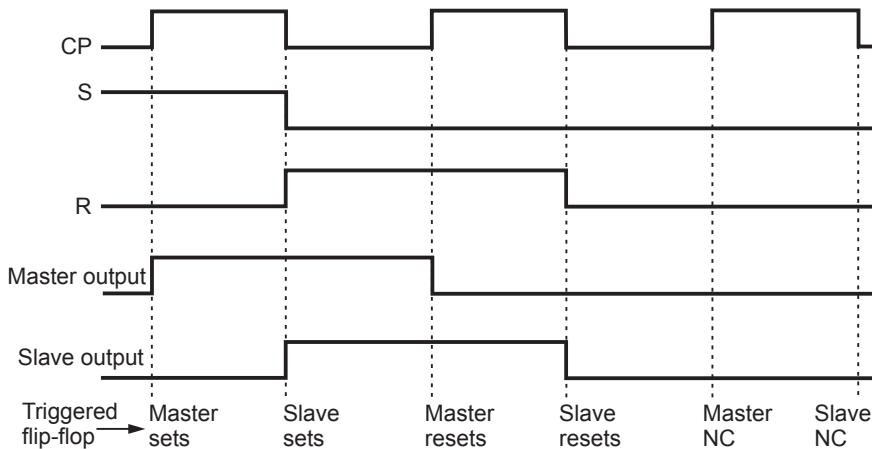


Fig. 4.4.24 Input and output waveforms for master-slave flip-flop

4.4.7 Master-Slave JK Flip-Flop

- Fig. 4.4.25 shows the master-slave JK flip-flop. Positive clock pulses are applied to first flip-flop and inverted (negative) clock pulses are applied to second flip-flop.
- When $CK = 1$, the first flip-flop is enabled and the outputs Q_M and \bar{Q}_M responds to the inputs of J and K according to the Table 1. At this time, the second flip-flop is inhibited because its clock is low, $\bar{CK} = 0$.

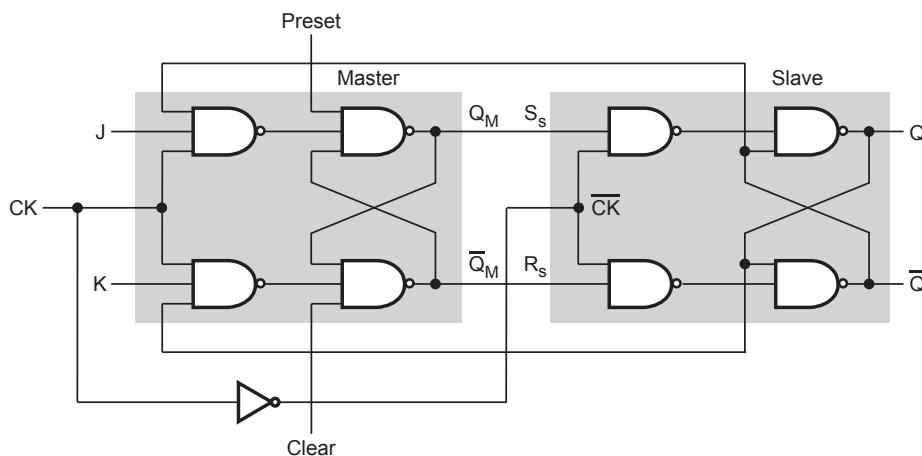


Fig. 4.4.25 Master - slave JK flip - flop

- When CK goes Low ($\overline{CK} = 1$), the first flip-flop is inhibited and second flip-flop is enabled. At this time, the output of second flip-flop (Q and \overline{Q}) follow the outputs Q_M and \overline{Q}_M , respectively.
- Since the second flip-flop follows the first one, it is referred to as the **slave** and the first one as the **master**.
- In master-slave JK flip-flop state change occurs when flip-flop goes through both positive transition (first half) of clock and negative transition of the clock (second half). Thus, race-around condition does not exist in the master-slave JK flip-flop.

4.4.8 T Flip-Flop

T flip-flop is also known as '**Toggle flip-flop**'. The T flip-flop is a modification of the JK flip-flop. As shown in the Fig. 4.4.26, the T flip-flop is obtained from a JK flip-flop by connecting both inputs, J and K together.

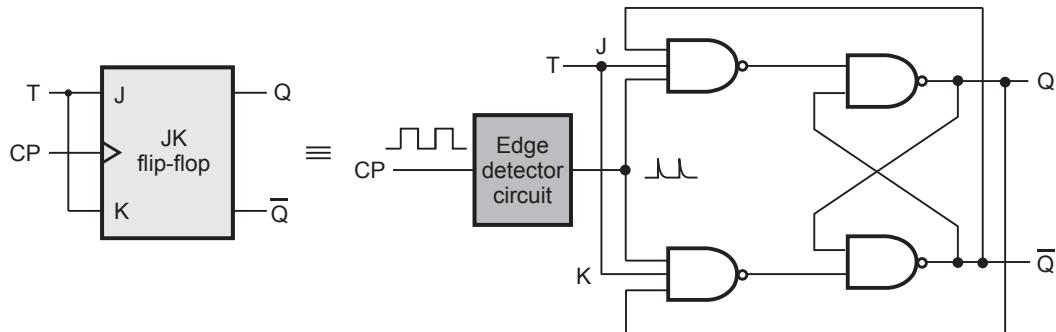
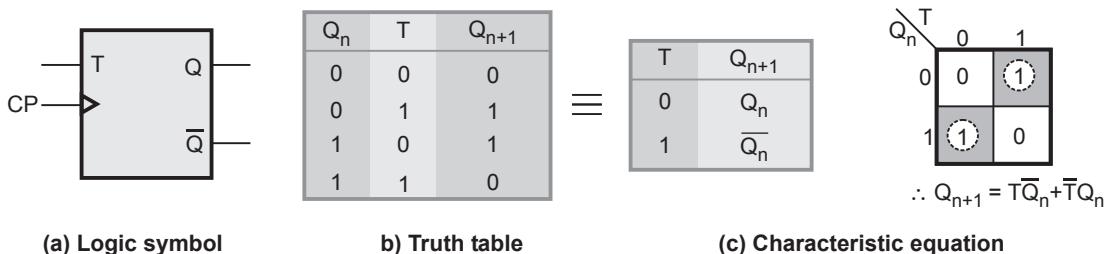


Fig. 4.4.26 T flip-flop using NAND gates

When $T = 0$, $J = K = 0$ and hence there is no change in the output. When $T = 1$, $J = K = 1$ and hence output toggles.

The Fig. 4.4.27 shows logic symbol, truth table and the characteristic equation for T flip-flop.



(a) Logic symbol

(b) Truth table

(c) Characteristic equation

Fig. 4.4.27

Example 4.4.4 Refer Fig. 4.4.28 and determine the Q output waveform if the flip-flop starts out RESET.

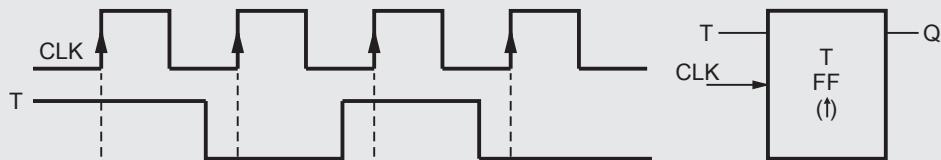


Fig. 4.4.28

Solution :

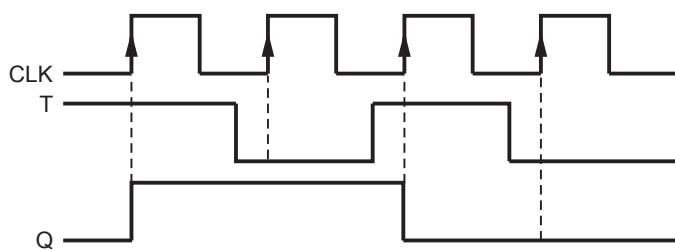


Fig. 4.4.29

4.4.9 Preset and Clear

For the flip-flops discussed so far, the SR, D, JK, and T, the inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse; that is, the data are transferred synchronously with the clock.

When power is turned ON, the state of the flip-flop is uncertain. It may come to set ($Q = 1$) or reset ($Q = 0$) state. In many applications, it is necessary to initially set or reset the flip-flop. Such initial state of flip-flop can be accomplished by using the direct or asynchronous inputs of the flip-flop. These inputs are : Preset (\bar{P}) and Clear (\bar{C}). They can be applied at any time between clock pulses and are not in synchronism with the clock.

The Fig. 4.4.30 shows the SR and D flip-flops with preset and clear inputs. These are active-low inputs and thus when $\bar{P} = \bar{C} = 1$, the circuit operates in accordance with the truth table of SR flip-flop. If $\bar{P} = 1$ and $\bar{C} = 0$, the flip-flop is reset and $\bar{P} = 0$ and $\bar{C} = 1$, the flip-flop is set.

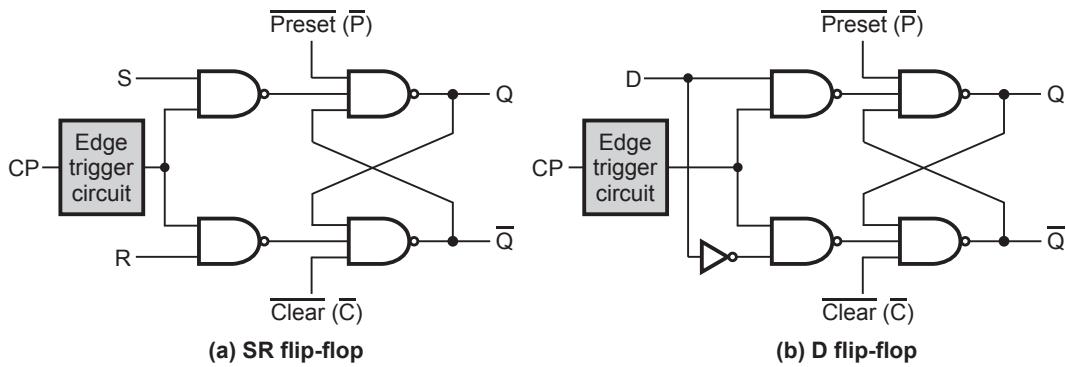
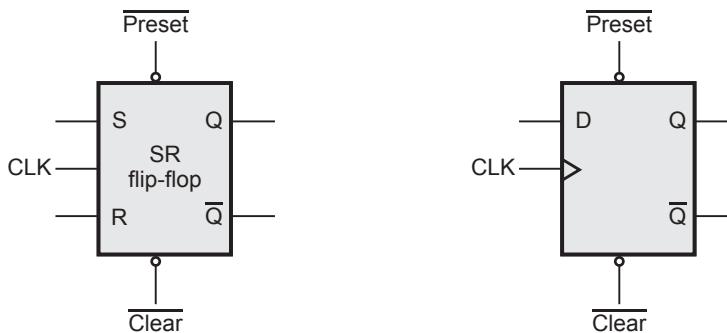


Fig. 4.4.30



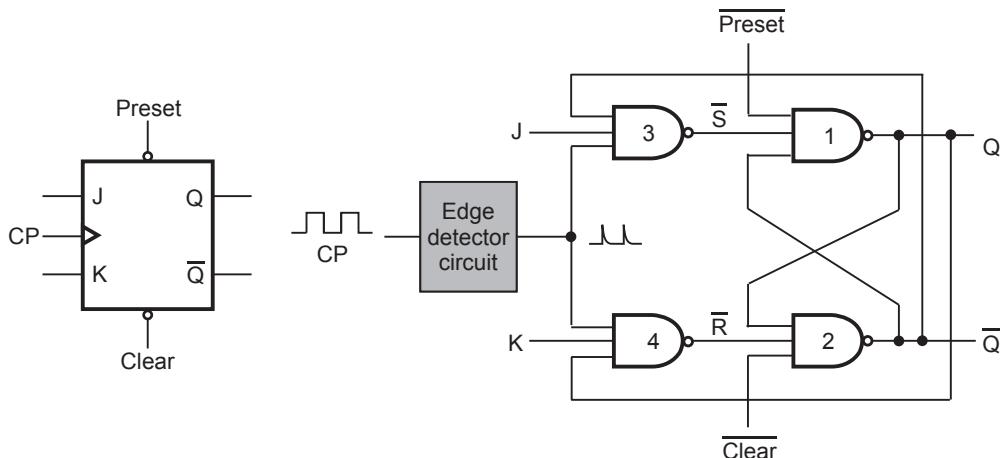
(a) Logic symbol for SR flip-flop

(b) Logic symbol for D flip-flop

Fig. 4.4.31 Logic symbol

Note Condition $\bar{P} = \bar{C} = 0$ must not be used, since this leads to an uncertain state.

The JK flip-flop with preset and clear is shown in Fig. 4.4.32. If preset and clear inputs are 1, the circuit operates in accordance with the truth table of JK flip-flop given



(a) Logic symbol

(b) JK flip-flop with active high preset and clear
Fig. 4.4.32

in the Fig. 4.4.17 (c). If preset = 0 and clear = 1, the output of NAND gate 1 will certainly be 1. Consequently, all the three inputs to NAND gate 2 will be 1 which will make $\bar{Q} = 0$. Hence making preset = 0 sets the flip-flop. Here, preset signal is active when it is low, hence it is active low signal. Similarly, low (0) on the clear input resets the flip-flop making $\bar{Q} = 1$.

A logic symbol for a JK flip-flop with active low preset and clear inputs is shown in the Fig. 4.4.32 (a). These inputs are active low, therefore they must both be kept high for synchronous operation. The Fig. 4.4.33 illustrates the operation of active low preset and clear inputs.

During clock pulse 1 and 2 the Preset is low, keeping the flip-flop set regardless of the synchronous inputs. For clock pulses 3, 4, 5 and 6, toggle operation occurs because J and K both are high with preset and clear inactive. For clock pulse 7, the Clear input is low, keeping the flip-flop reset regardless of the synchronous inputs.

Assume $J = K = 1$

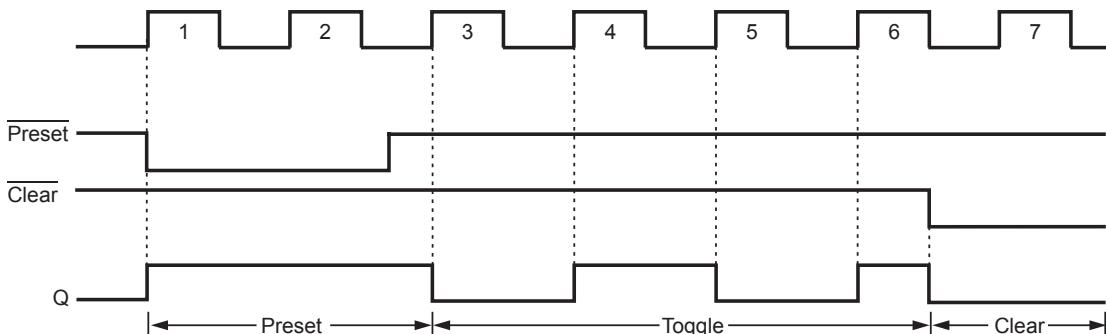


Fig. 4.4.33 Input and output waveforms showing operation of active low preset and clear inputs

In some IC packages preset and clear inputs are active high. In those cases preset and clear input must both be kept low for synchronous operation.

Review Questions

1. Differentiate between latches and flip-flops.
2. Explain the different types of triggering methods used for flip-flops.
3. What is SR flip-flop.
4. What is S-R flip-flop ? Explain working of clocked SR flip-flop. What is edge triggering ?
5. Explain the clocked SR flip-flop using NAND gates.
6. Explain the D flip-flop.
7. If Q output of a D-type flip-flop is connected to D input, it acts as a toggle switch. State whether true or false ? Justify your answer.

SPPU : May-12, Marks 4

SPPU : May-11, Marks 10

8. Justify name Delay for D flip-flop.
9. Explain the application of D flip-flop. **SPPU : May-06, Marks 2**
10. Draw and explain the operation of JK flip-flop using logic gates with waveforms.
11. Draw the JK flip-flop using NAND gates.
12. What is Race-around condition ? Explain with the help of timing diagram. How is it removed in basic flip-flop circuit ? **SPPU : May-05,07, Dec.-05, Marks 8**
13. Discuss method to avoid race around condition in JK flip-flop. **SPPU : Dec.-05, May-07, Marks 4**
14. What do you mean by Master-Slave JK Flip-flop ? Explain the advantage of this Flip-flop. Draw suitable circuit diagram and timing diagram. **SPPU : Dec.-06, Marks 10**
15. What is the advantage of M-S flip-flop ? Explain working of MS J-K flip-flop in detail. **SPPU : Dec.-10, Marks 8**
16. Justify name toggle for T flip-flop giving truth table and waveforms.
17. Draw and explain the operation of T flip-flop.
18. Explain the application of T flip-flop. **SPPU : May-06, Marks 2**
19. Explain the use of reset and preset inputs.

4.5 Excitation Tables

SPPU : Dec.-13, May-15

During the design process we know, from the transition table, the sequence of states, i.e., the transition from each present state to its corresponding next state. From this information we wish to find the flip-flop input conditions that will cause the required transition. For this reason, we need a table that lists the required inputs for a given change of state. Such a table is known as an excitation table of the flip-flop.

We can derive the excitation tables for flip-flops from their truth tables. The excitation table consists of two columns Q_n and Q_{n+1} , and a column for each input to show how the required transition can be achieved. Let us see the truth tables and excitation tables for RS, JK, D and T flip-flops.

4.5.1 SR Flip-Flop

Table 4.5.1 (a) and (b) show the truth table and excitation tables for SR flip-flop, respectively. As shown in the table, there are four possible transitions from the present state to the next state. For each transition, the required input

S	R	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	*

(a) SR truth table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

(b) SR excitation table

Table 4.5.1

condition is derived from the information available in the truth table. Let us see the process by examining each case.

Note The symbol "X" in the table represents a don't care condition, i.e., it indicates that to get required output it does not matter whether the input is either 1 or 0.

0 → 0 Transition : The present state of the flip-flop is 0 and is to remain 0 when a clock pulse is applied. Looking at truth table of SR flip-flop we can understand that, this can happen either when $R = S = 0$ (no-change condition) or when $R = 1$ and $S = 0$. Thus, S has to be at 0, but R can be at either level. The table indicates this with a "0" under S and an "X" (don't care) under R.

0 → 1 Transition : The present state is 0 and is to change to 1. This can happen only when $S = 1$ and $R = 0$ (set condition). Therefore, S has to be 1 and R has to be 0 for this transition to occur.

1 → 0 Transition : The present state is 1 and is to change to a 0. This can happen only when $S = 0$ and $R = 1$ (reset condition). Therefore, S has to be 0 and R has to be 1 for this transition to occur.

1 → 1 Transition : The present state is 1 and is to remain 1. This can happen either when $S = 1$ and $R = 0$ (set condition) or when $S = 0$ and $R = 0$ (no change condition). Thus R has to be 0, but S can be at either level. The table indicates this with a "X" under S and "0" under R.

4.5.2 JK Flip-Flop

The truth table and excitation table for JK flip-flop are shown in Table 4.5.2 (a) and (b) respectively. Let us examine each case.

0 → 0 Transition : When both present state and next state are 0, the J input must remain at 0 and the K input can be either 0 and 1.

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

(a) JK truth table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(b) JK excitation table

Table 4.5.2

0 → 1 Transition : The present state is 0 and is to change to 1. This can happen either when $J = 1$ and $K = 0$ (set condition) or when $J = K = 1$ (toggle condition). Thus, J has to be 1, but K can be at either level for this transition to occur.

1 → 0 Transition : The present state is 1 and is to change to 0. This can happen either when $J = 0$ and $K = 1$ or when $J = K = 1$. Thus, K has to be 1 but J can be at either level.

1 → 1 Transition : When both present state and next are 1, the K input must remain at 0 while the J input can be 0 or 1.

As seen from Table 4.5.2, the excitation table for JK flip-flop has more don't care conditions than the excitation table for RS flip-flop. The don't care terms usually simplify the function. Therefore, the combinational circuits using JK flip-flops for the input functions are likely to be simpler than those using RS flip-flops.

4.5.3 D Flip-Flop

The Table 4.5.3 (a) and (b) show the truth table and excitation table for D flip-flop, respectively. In D flip-flop, the next state is always equal to the D input and it is independent of the present state. Therefore, D must be 0 if Q_{n+1} has to be 0, and 1 if Q_{n+1} has to be 1, regardless of the value of Q_n .

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

(a) D truth table (b) D excitation table

Table 4.5.3

4.5.4 T Flip-Flop

The Table 4.5.4 (a) and (b) show the truth table and the excitation table for T flip-flop, respectively. We know that when input $T = 1$, the state of the flip-flop is complemented; when $T = 0$, the state of the flip-flop remains unchanged. Therefore, for $0 \rightarrow 0$ and $1 \rightarrow 1$ transitions T must be 0 and for $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions T must be 1.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Table 4.5.4

Review Questions

- Derive the excitation tables for SR, D, JK and T flip-flop.
- Draw the excitation table of S-R flip-flop.
- Draw the excitation table of J-K flip-flop.

SPPU : Dec.-13, Marks 2

SPPU : May-15, Marks 2

4.6 Conversion from One Type to Another Type of Flip-Flop

SPPU : May-06,10,12, Dec.-16,17,19

It is possible to convert one flip-flop into another flip-flop with some additional gates or simply doing some extra connection. Let us see few conversions among flip-flops.

4.6.1 SR Flip-Flop to D Flip-Flop

The excitation table for above conversion is as shown in Table 4.6.1.

Input	Present state	Next state	Flip-flop inputs	
D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

Table 4.6.1

K- map simplification

Logic diagram

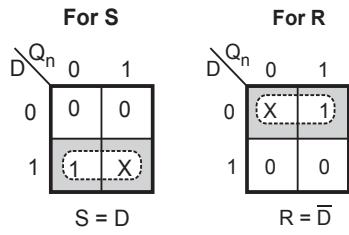


Fig. 4.6.1

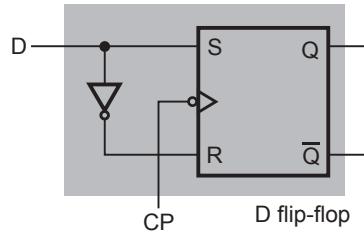


Fig. 4.6.2 SR to D flip-flop conversion

4.6.2 SR Flip-Flop to JK Flip-Flop

SPPU : May-10

The excitation table for above conversion is as shown in Table 4.6.2.

Inputs		Present state	Next state	Flip-flop inputs	
J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

Table 4.6.2

K-map simplification

For S				For R			
K	Q _n	00	01	11	10	K	Q _n
0	J	0	X	0	0	0	X
1	J	1	X	0	1	1	0

$S = J \bar{Q}_n$

$R = K Q_n$

Fig. 4.6.3

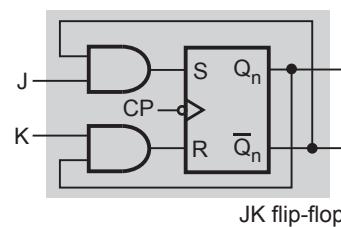
Logic diagram

Fig. 4.6.4 SR to JK flip-flop conversion

4.6.3 SR Flip-Flop to T Flip-Flop

The excitation table for above conversion is as shown in the Table 4.6.3.

Input	Present state	Next state	Flip-flop inputs	
			S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

Table 4.6.3

K-map simplification

For S		For R	
T	Q _n	T	Q _n
0	0	0	1
0	1	X	0
1	0	0	1
1	1	0	0

$S = T \bar{Q}_n$

$R = T Q_n$

Fig. 4.6.5

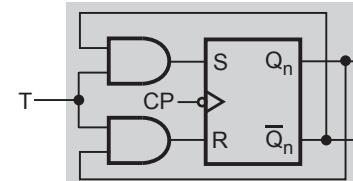
Logic diagram

Fig. 4.6.6 SR to T flip-flop conversion

If we apply clock pulses to the circuit, the circuit output will toggle from 0 to 1 and 1 to 0. Thus, we can build 1-bit counter using SR flip-flop by converting it to T flip-flop.

Example 4.6.1 Prepare the truth table for the circuit of Fig. 4.6.7 and show that it acts as a T-type flip-flop.

for the circuit of Fig. 4.6.7 and show that it acts as a T-type flip-flop.

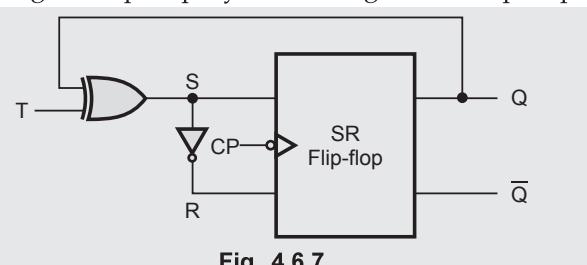


Fig. 4.6.7

Solution : For SR flip-flop,

$$\begin{aligned}
 Q_{n+1} &= S + \bar{R} Q_n && \dots \text{Characteristics equation} \\
 &= S + S Q_n \\
 &= S(1 + Q_n) = S
 \end{aligned}$$

$\therefore R = \bar{S}$

We have, $S = Q_n \oplus T$

$$\begin{aligned}
 \therefore Q_{n+1} &= Q_n \oplus T \\
 &= T \bar{Q}_n + \bar{T} Q_n && \dots \text{Characteristic equation of T flip-flop}
 \end{aligned}$$

C_p	T	Q_n	S = Q_n ⊕ T	R = \bar{S}	Q_{n+1} = S
↓	0	0	0	1	0
↓	0	1	1	0	1
↓	1	0	1	0	1
↓	1	1	0	1	0

Table 4.6.4 Truth table for the given circuit

Looking at column 1 and column 5 of the Table 4.6.4 we can conclude that when $T = 0$, the output does not change and when $T = 1$, the output toggles. Thus, the given circuit acts as a T flip-flop. This is another way of implementing T flip-flop using SR flip-flop.

4.6.4 JK Flip-Flop to T Flip-Flop

The excitation table for above conversion is as shown in Table 4.6.5.

Input	Present state	Next state	Flip-flop inputs	
T	Q_n	Q_{n+1}	J_A	K_A
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

Table 4.6.5

K-map simplification

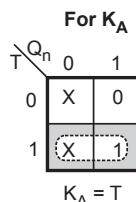
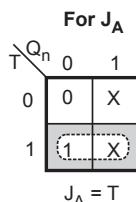


Fig. 4.6.8

Logic diagram

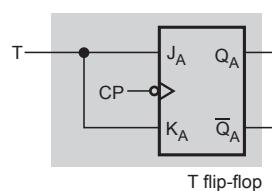


Fig. 4.6.9 JK to T flip-flop conversion

4.6.5 JK Flip-Flop to D Flip-Flop

The excitation table for above conversion is as shown in the Table 4.6.6.

Input	Present state	Next state	Flip-flop inputs	
D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

Table 4.6.6

K - map simplification

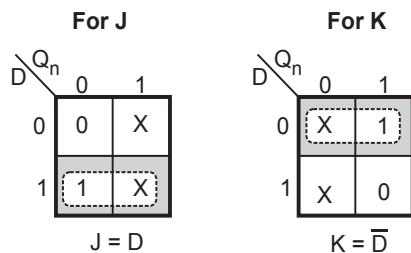


Fig. 4.6.10

Logic diagram

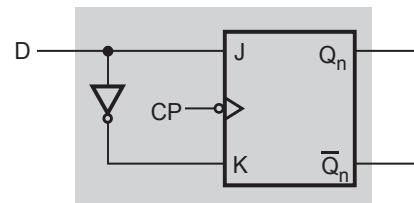


Fig. 4.6.11 JK to D flip-flop conversion

4.6.6 D Flip-Flop to T Flip-Flop

The excitation table for above conversion is as shown in the Table 4.6.7.

Input	Present state	Next state	Flip-flop input
T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Table 4.6.7

K - map simplification

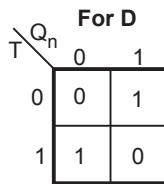


Fig. 4.6.12

Logic diagram

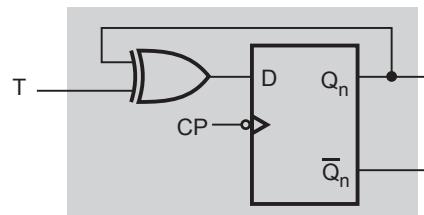


Fig. 4.6.13 D to T flip-flop conversion

$$D = \bar{T}Q_n + T\bar{Q}_n = T \oplus Q_n$$

Example 4.6.2 Analyze the circuit and prove that it is equivalent to T flip-flop.

Solution : To analyze the circuit means to derive the truth table for it.

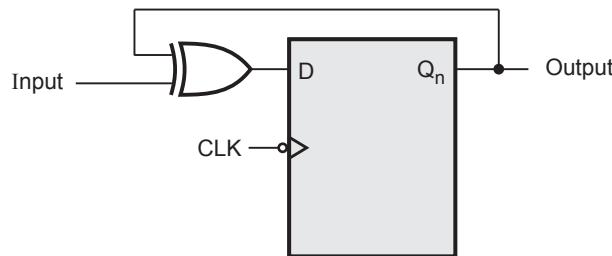


Fig. 4.6.14

We have, $D = \text{Input} \oplus Q_n$

CLK	Input	Q_n	$D = \text{Input} \oplus Q_n$	Q_{n+1}
↓	0	0	0	0
↓	0	1	1	1
↓	1	0	1	1
↓	1	1	0	0

} When input is 0
 } output does not change
 } When input is 1
 } output toggles

Table 4.6.8 Truth table for given circuit

In the above circuit, output does not change when input is 0 and it toggles when input is 1. This is the characteristics of T flip-flop. Hence, the given circuit is T flip-flop constructed using D flip-flop.

4.6.7 T Flip-Flop to D Flip-Flop

The excitation table for above conversion is as shown in the Table 4.6.9.

Input	Present state	Next state	Flip-flop input
D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 4.6.9

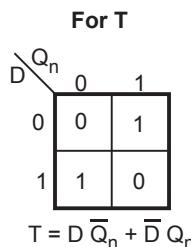
K-map simplification

Fig. 4.6.15

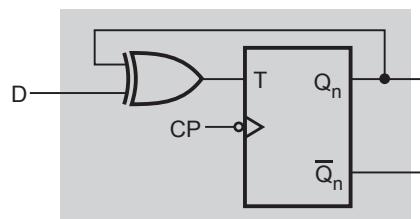
Logic diagram

Fig. 4.6.16 T to D flip-flop conversion

4.6.8 JK Flip-Flop to SR Flip-Flop

The excitation table for above conversion is as shown in Table 4.6.10.

Inputs	Present state	Next state	Flip-flop inputs	
S R	Q_n	Q_{n+1}	J	K
0 0	0	0	0	X
0 0	1	1	X	0
0 1	0	0	0	X
0 1	1	0	X	1
1 0	0	1	1	X
1 0	1	1	X	0
1 1	0	X	X	X
1 1	1	X	X	X

Table 4.6.10 Excitation table for JK to SR conversion

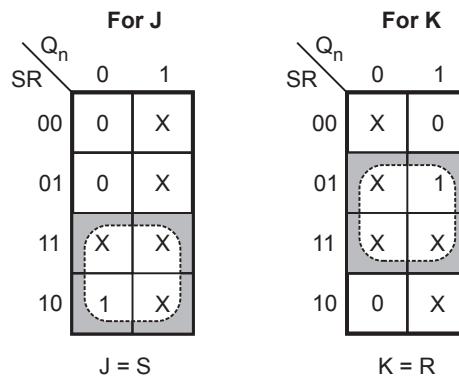
K-map simplification

Fig. 4.6.17

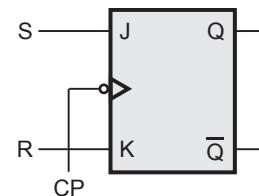
Logic diagram

Fig. 4.6.18 JK to SR

4.6.9 D Flip-Flop to SR Flip-Flop

The excitation table for above conversion is as shown in the Table 4.6.11.

Inputs	Present state	Next state	Flip-flop input
S R	Q_n	Q_{n+1}	D
0 0	0	0	0
0 0	1	1	1

0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	X	X
1	1	1	X	X

Table 4.6.11 Excitation table for D to SR conversion

K - map simplification

For D				
RQ _n		00	01	11
S	0	0	1	0
1	1	1	X	X

$$D = \overline{R} Q_n + S$$

Fig. 4.6.19

Logic diagram

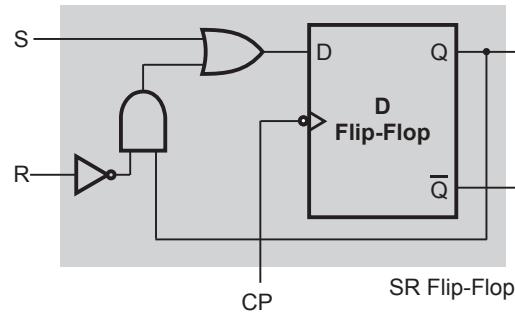


Fig. 4.6.20 D to SR flip-flop conversion

4.6.10 T Flip-Flop to SR Flip-Flop

The excitation table for conversion of T FF into an SR FF is as shown in the Table 4.6.12.

Inputs	Present state		Next state		Flip-flop input
	S	R	Q _n	Q _{n+1}	
0 0	0		0	0	0
0 0		1	1	1	0
0 1	0		0	0	0
0 1		1	1	0	1
1 0	0		1	1	1
1 0		1	1	1	0
1 1	0		X	X	x
1 1		1	X	X	x

Table 4.6.12 Excitation table for T to SR conversion

K - map simplification

For D				
JK		00	01	11
J	K	0	1	0
1	1	1	1	0

(a) $\overline{K} Q$ and $J \overline{Q}$

Logic diagram

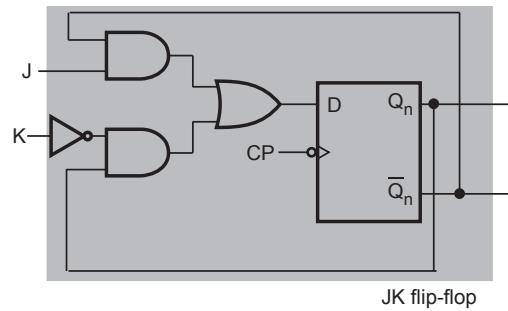
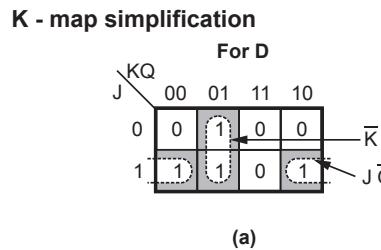


Fig. 4.6.21

4.6.11 D Flip-Flop to JK Flip-Flop

The excitation table for conversion of D flip-flop to JK flip-flop :

Inputs		Present state	Next state	Flip-flop input
J	K	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0



Logic diagram

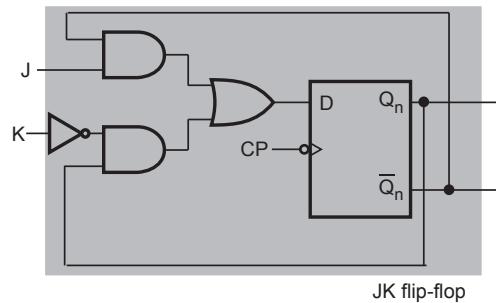


Fig. 4.6.22

Review Questions

1. Convert SR flip-flop to D flip-flop.
 2. Convert SR flip-flop to JK flip-flop.
 3. Convert SR flip-flop to T flip-flop.
 4. Convert JK flip-flop to T flip-flop.
 5. Convert JK flip-flop to D flip-flop.
 6. Convert D flip-flop to T flip-flop.
 7. Convert T flip-flop to D flip-flop.
 8. Convert JK flip-flop to SR flip-flop.
 9. Convert D flip-flop to SR flip-flop.

SPPU : May-12,Dec.-16 Marks 2

SPPU : May-10,12, Marks 4

SPPU : May-12, Marks 2

SPPU : May-06,Dec.-16,19, Marks 2

SPPU : May-06, Marks 3

SPPU : Dec.-17, Marks 2

4.7 Applications of Flip-Flops

Some of the important applications of flip-flops are :

- It can be used as a memory element.
 - It can be used to eliminate key debounce.

- It is used as a basic building block in sequential circuits such as counters and registers.
- It can be used as a delay element.

4.7.1 Bounce Elimination Switch

For interfacing keys to the digital systems, usually push button keys are used. These push button keys when pressed bounces a few times, closing and opening the contacts before providing a steady reading, as shown in the Fig. 4.7.1. Reading taken during bouncing period may be faulty. This problem is known as **key debounce**. The problem of key debounce is undesirable and it must be avoided.

One way to avoid key debounce problem is to use SR latch. The circuit used to avoid keybounce with SR latch is called a **switch or contact debouncer**. The Fig. 4.7.2 shows the switch debouncer circuit and its waveforms. When key is at position A, the output of SR latch is logic 1, and when key is at position B, the output of SR latch is logic 0. It is important to note that, when

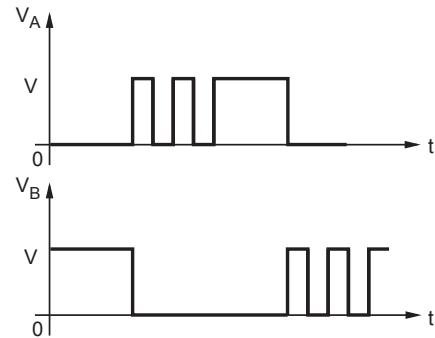
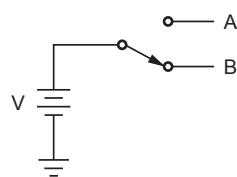


Fig. 4.7.1 Effect of key debounce

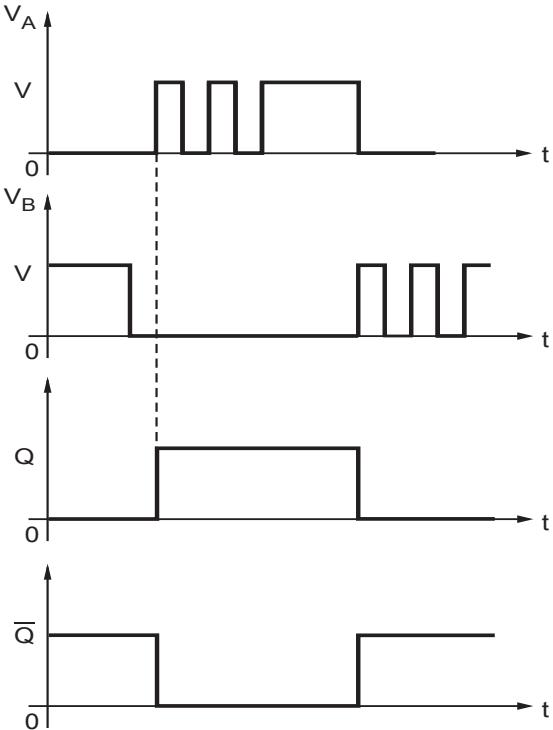


Fig. 4.7.2 Waveforms of switch debouncer

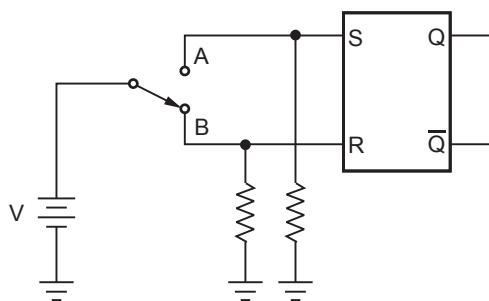


Fig. 4.7.2 (a) Switch debouncer

key is in between A and B, SR inputs are 00 and hence output does not change, preventing debouncing of key output. In other words, we can say that the output does not change during transition period, eliminating key debounce.

4.7.2 Registers

A group of flip-flops connected together forms a **register**. A register is used solely for storing and shifting data which is in the form of 1s and/or 0s, entered from an external source. Fig. 4.7.3 shows 3-bit register using three D flip-flops. Preset, reset and clock inputs are connected in parallel and 3-bit input is applied to D inputs of the flip-flop. During positive edge of the clock, D inputs of the flip-flops are stored within the flip-flop and are available at the outputs of D flip-flops.

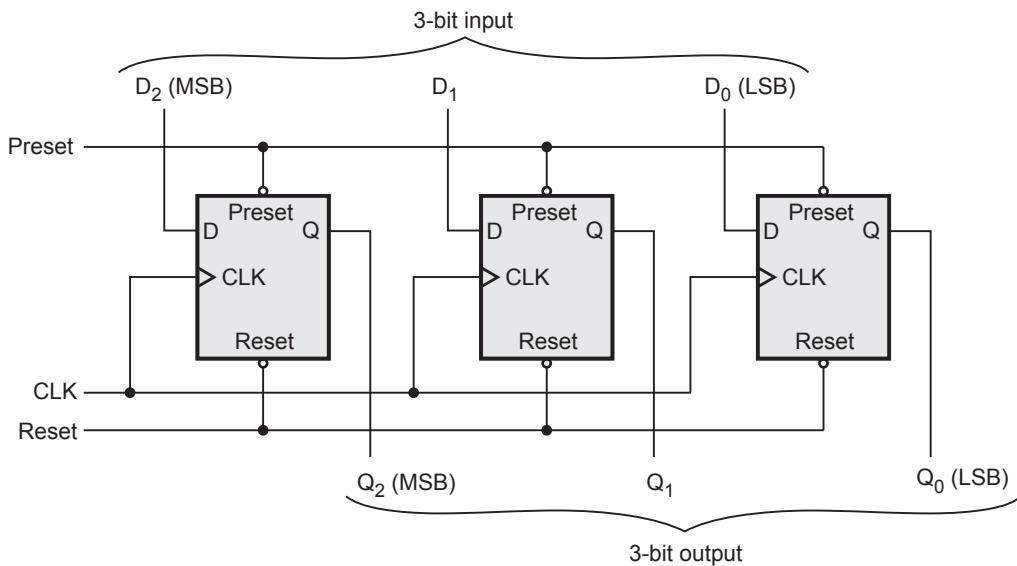


Fig. 4.7.3 Register

4.7.3 Counters

A **counter** is a register capable of counting the number of clock pulses arriving at its clock input. Count represents the number of clock pulses arrived. On arrival of each clock pulse, the counter is incremented by one. In case of down counter, it is decremented by one.

Fig. 4.7.4 shows 3-bit counter. It consists of three flip-flops. A counter with n flip-flops has 2^n possible states. Therefore, the 3-bit counter can count from decimal 0 to 7.

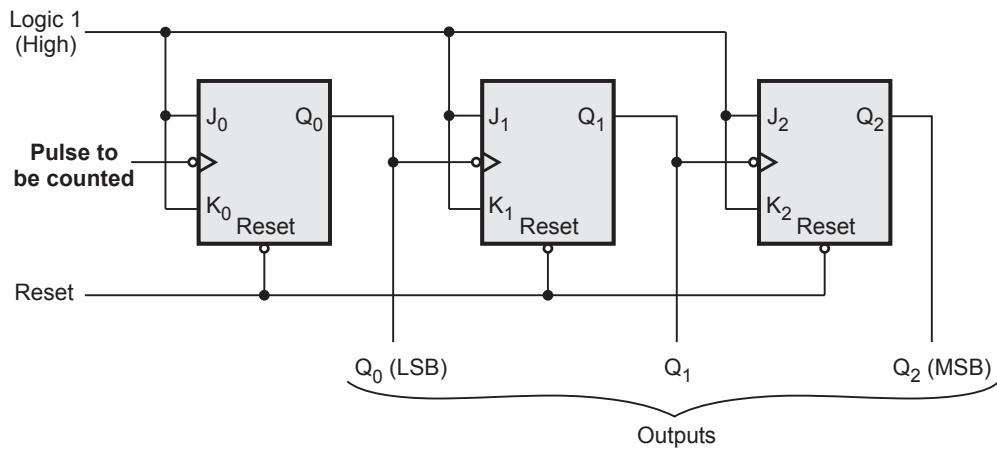


Fig. 4.7.4 Counter

Review Questions

1. Lists the applications of flip-flops.
2. How keyboard debouncing is eliminated using flip-flop ? Explain with suitable circuit diagram.



Notes

UNIT - III

5

Registers

Syllabus

SISO, SIPO, PISO, PIPO, Shift Registers, Bidirectional shift Register, Universal shift Register

Contents

5.1	<i>Introduction</i>	
5.2	<i>Shift Registers</i>	
5.3	<i>Types of Shift Registers</i>	<i>May-05,06,08,10,14,</i> <i>Dec.-05,08,11,12,14 , . . . Marks 10</i>
5.4	<i>Universal Shift Register</i>	<i>Dec.-06,07, May-07 , . . . Marks 10</i>
5.5	<i>Applications of Shift Registers</i>	<i>May-10, Marks 4</i>

5.1 Introduction

We have seen that a flip-flop is nothing but a binary cell capable of storing one bit information, and can be connected together to perform counting operations. Such a group of flip-flops is called **counter**. We have also seen that group of flip-flops can be used to store a word, which is called **register**.

A flip-flop can store 1-bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.

5.1.1 Buffer Register

Fig. 5.1.1 shows the simplest register

constructed with four D flip-flops. This register is also called **buffer register**. Each D flip-flop is triggered with a common negative edge clock pulse.

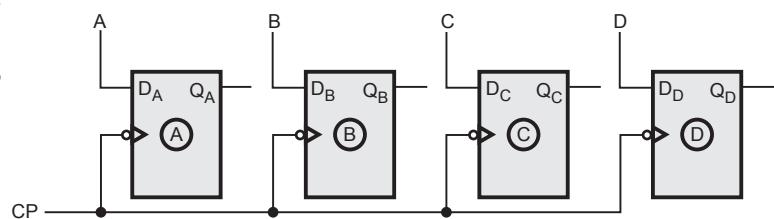


Fig. 5.1.1 Buffer register

The input bits set up the flip-flops for loading. Therefore, when the first negative clock edge arrives, the stored binary information becomes,

$$Q_A Q_B Q_C Q_D = ABCD$$

In this register, four D flip-flops are used. So it can store 4-bit binary information. Thus the number of flip-flop stages in a register determines its total storage capacity.

5.1.2 Controlled Buffer Register

We can control input and output of the register by connecting tri-state devices at the input and output sides of register as shown in Fig. 5.1.2. So this register is called '**controlled buffer register**'.

Here, tri-state switches are used to control the operation. When you want to store data in the register,

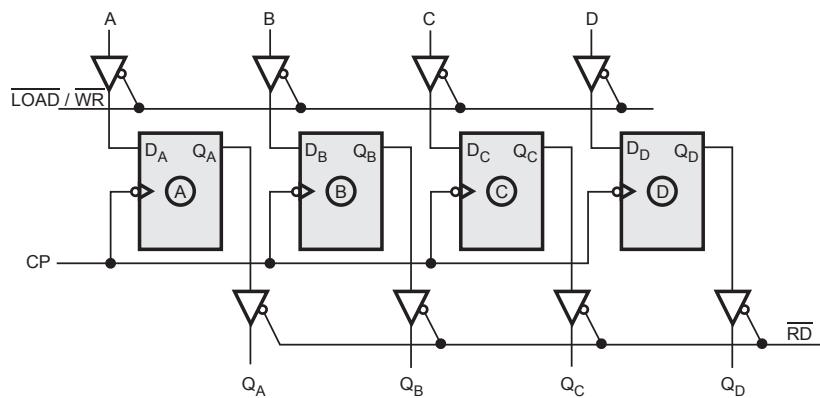


Fig. 5.1.2 Controlled buffer register

you have to make $\overline{\text{LOAD}}$ or $\overline{\text{WR}}$ signal low to activate the tri-state buffers. When you want the data at the output, you have to make $\overline{\text{RD}}$ signal low to activate the buffers. Controlled buffer registers are commonly used for temporary storage of data within a digital system.

As seen above the 4-bit register can store 4-bit binary information. In general, n-bit register can store n-bit binary information.

Example 5.1.1 Determine the number of flip-flops needed to construct a register capable of storing,

- i) A 6-bit binary number
- ii) Decimal numbers up to 32
- iii) Hexadecimal numbers up to F
- iv) Octal numbers up to 10.

Solution :

- i) A 6-bit binary number requires register with 6 flip-flops.
- ii) $(32)_{10} = (100000)_2$. The number of bits required to represent 32 in binary are six, therefore, 6 flip-flops are needed to construct a register capable of storing 32 decimal.
- iii) $(F)_{16} = (1111)_2$. The number of bits required to represent $(F)_{16}$ in binary are four, therefore four flip-flops are needed to construct a register capable of storing $(F)_{16}$.
- iv) $(10)_8 = (1000)_2$. The number of bits required to represent $(10)_8$ in binary are four, therefore, four flip-flops are needed to construct a register capable of storing $(10)_8$.

Review Questions

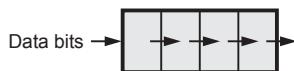
1. What is register ?
2. What is buffer register ?
3. Draw and explain 4-bit controlled buffer register.

5.2 Shift Registers

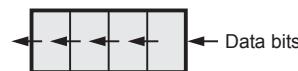
The binary information (data) in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to a group of registers called '**shift registers**'. They are very important in applications involving the storage and transfer of data in a digital system.

Fig. 5.2.1 gives the symbolical representation of the different types of data movement in shift register operations.

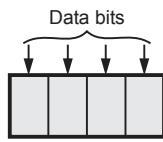
According to the data movement in a register, let us see some of the types of shift registers.



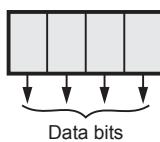
(a) Serial shift right, then out



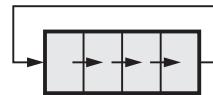
(b) Serial shift left, then out



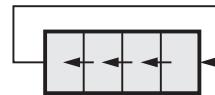
(c) Parallel shift in



(d) Parallel shift out



(e) Rotate right



(f) Rotate left

Fig. 5.2.1 Basic data movement in registers

Review Question

1. List the basic types of shift registers in terms of data movements.

5.3 Types of Shift Registers

SPPU : May-05,06,08,10,14, Dec.-05,08,11,12,14

5.3.1 Serial In Serial Out (SISO) Shift Register

Shift Left Mode

Fig. 5.3.1 shows serial-in serial-out shift-left register.

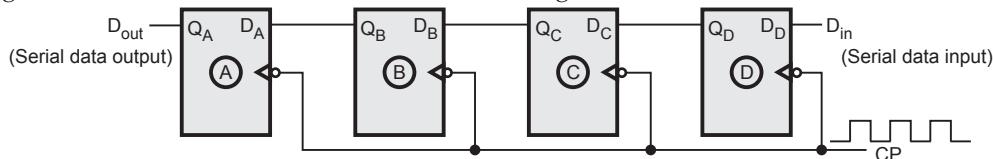
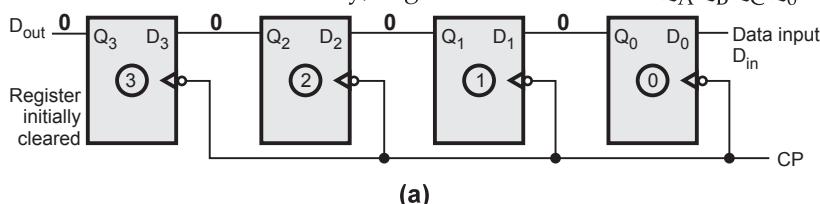
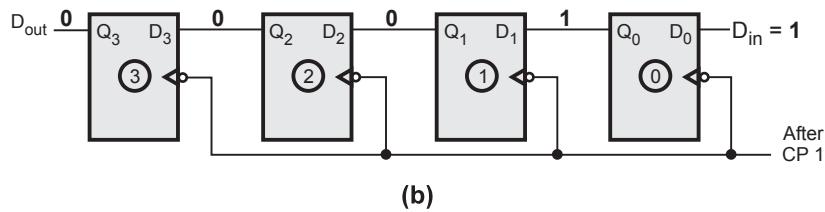


Fig. 5.3.1 Shift-left register

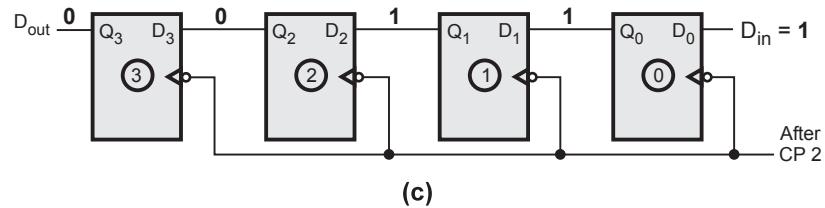
We will illustrate the entry of the four bit binary number 1111 into the register, beginning with the left-most bit. Initially, register is cleared. So $Q_A Q_B Q_C Q_D = 0 0 0 0$



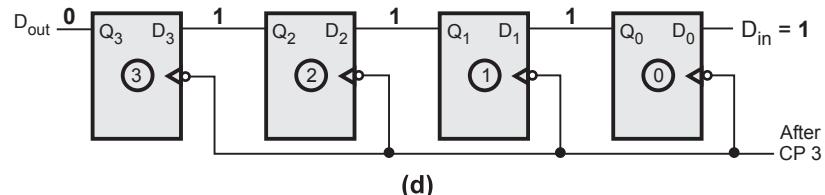
- a) When data 1 1 1 1 is applied serially, i.e. left-most 1 is applied as D_{in} , $D_{in} = 1$, $Q_3 Q_2 Q_1 Q_0 = 0 0 0 0$. The arrival of the first falling clock edge sets the right-most flip-flop, and the stored word becomes, $Q_3 Q_2 Q_1 Q_0 = 0 0 0 1$



- b) When the next negative clock edge hits, the Q₁ flip-flop sets and the register contents become, Q₃Q₂Q₁Q₀ = 0 0 1 1



- c) The third negative clock edge results in, Q₃Q₂Q₁Q₀ = 0 1 1 1



- d) The fourth falling clock edge gives, Q₃Q₂Q₁Q₀ = 1 1 1 1.

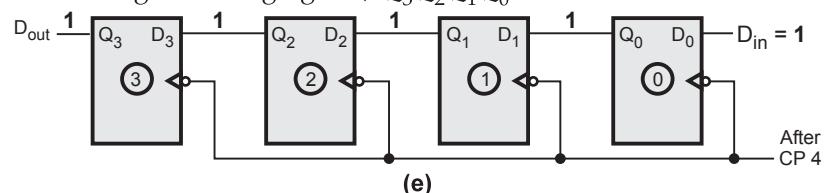


Fig. 5.3.2 Four bits 1111 being serially entered into shift-left register

The Table 5.3.1 summarizes the shift left operation.

CP	Q ₃	Q ₂	Q ₁	Q ₀	D _{in}
Initially	0	0	0	0	1
↓ 1 st	0	0	0	1	1
↓ 2 nd	0	0	1	1	1
↓ 3 rd	0	1	1	1	1
↓ 4 th	1	1	1	1	1

Table 5.3.1 Shift left operation

The Fig. 5.3.3 shows waveforms for shift left operation

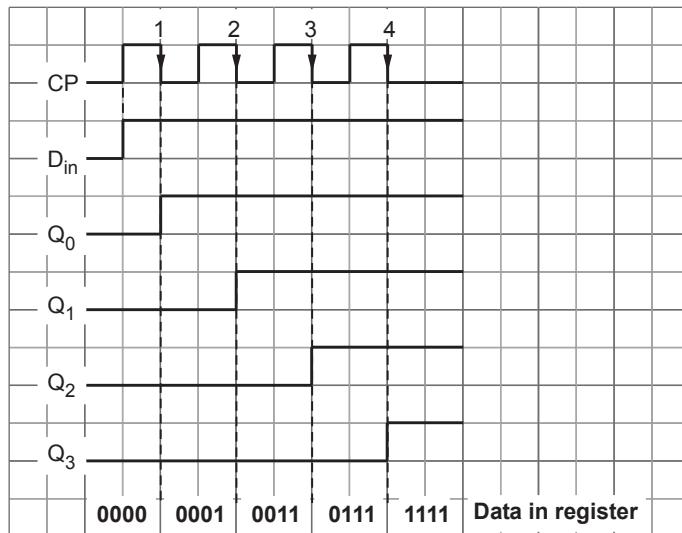


Fig. 5.3.3 Waveforms for shift left register

Shift Right Mode

Fig. 5.3.4 shows serial-in serial-out shift-left register.

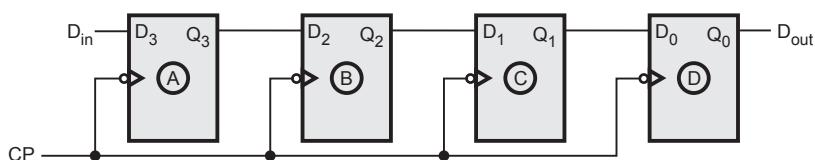
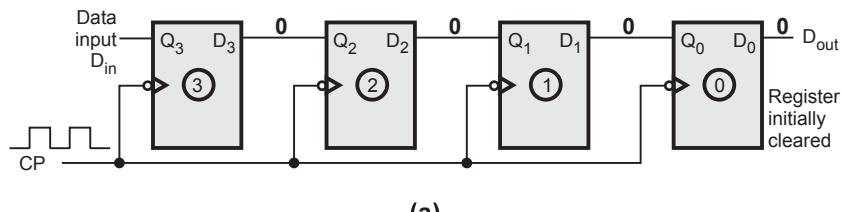


Fig. 5.3.4 Shift-right register

We will illustrate the entry of the four bit binary number 1111 into the register, beginning with the left-most bit.

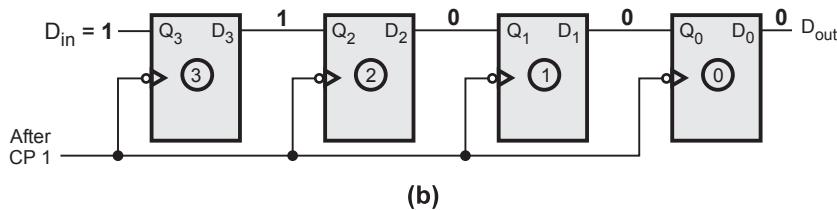
Initially, register is cleared. So $Q_3Q_2Q_1Q_0 = 0\ 0\ 0\ 0$



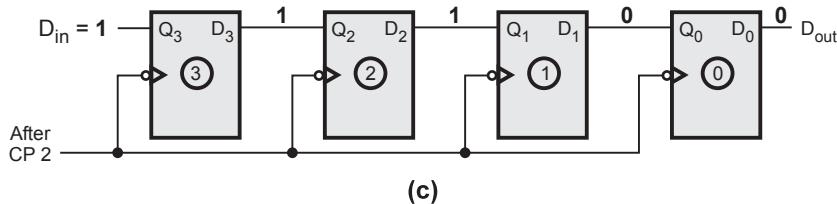
a) When data 1 1 1 1 is applied serially, i.e. left-most 1 is applied as D_{in} ,

$$D_{in} = 1, Q_3Q_2Q_1Q_0 = 0\ 0\ 0\ 0$$

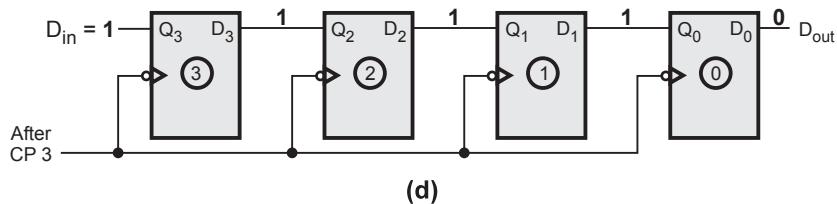
The arrival of the first falling clock edge sets the left-most flip-flop, and the stored word becomes, $Q_3Q_2Q_1Q_0 = 1\ 0\ 0\ 0$



- b) When the next falling clock edge hits, the Q₂ flip-flop sets and the register contents become, Q₃Q₂Q₁Q₀ = 1100



- c) The third falling clock edge results in, Q₃Q₂Q₁Q₀ = 1110.



- d) The fourth falling clock edge gives, Q₃Q₂Q₁Q₀ = 1111.

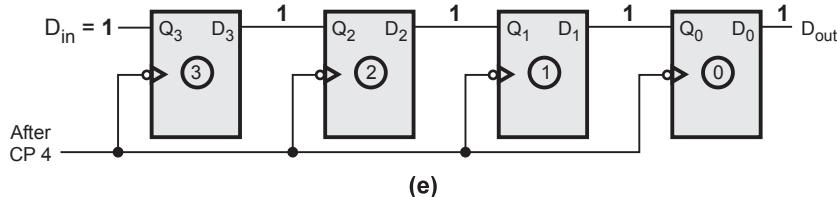


Fig. 5.3.5 Four bits 1111 being serially entered into shift-right register

Table 5.3.2 summarizes the shift right operation.

CP	D _{in}	Q ₃	Q ₂	Q ₁	Q ₀
Initially		1	0	0	0
↓ 1 st	1	1	0	0	0
↓ 2 nd	1	1	1	0	0
↓ 3 rd	1	1	1	1	0
↓ 4 th	1	1	1	1	1

Table 5.3.2 Shift right operation

The Fig. 5.3.6 shows waveforms for shift right operation.

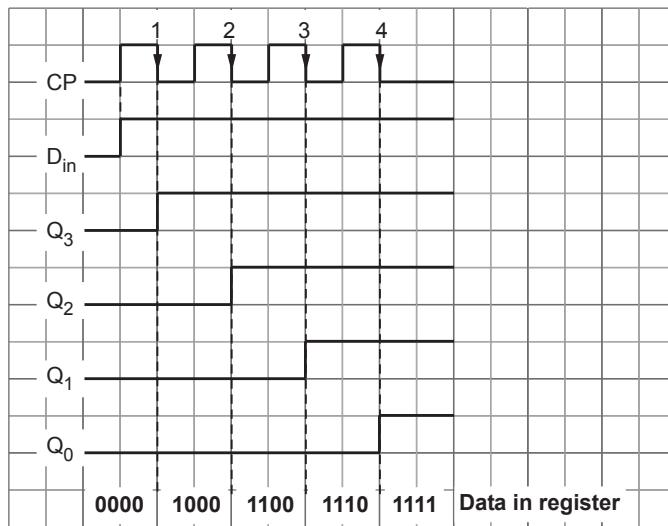


Fig. 5.3.6 Waveforms for shift right register

5.3.2 Serial In Parallel Out (SIPO) Shift Register

In this case, the data bits are entered into the register in the same manner as discussed in the last section, i.e. serially. But the output is taken in parallel. Once the data are stored, each bit appears on its respective output line and all bits are available simultaneously, instead of on a bit-by-bit basis as with the serial output as shown in Fig. 5.3.7.

CP	Q ₃	Q ₂	Q ₁	Q ₀
-	NC	NC	NC	NC
↓	D ₃	D ₂	D ₁	D ₀

Table 5.3.3 Truth table

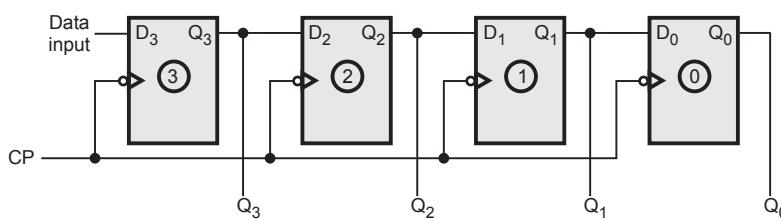


Fig. 5.3.7 A Serial In Parallel Out (SIPO) shift register

5.3.3 Parallel In Serial Out (PISO) Shift Register

SPPU : May-10, Marks 6

In this type, the bits are entered in parallel i.e simultaneously into their respective stages on parallel lines.

Fig. 5.3.8 illustrates a four-bit parallel in serial out register. There are four input lines A₃, A₂, A₁, A₀ for entering data in parallel into the register. SHIFT/LOAD is the control input which allows shift or loading data operation of the register. When SHIFT/LOAD

is low, gates G_1 , G_2 , G_3 are enabled, allowing each input data bit to be applied to D input of its respective flip-flop. When a clock pulse is applied, the flip-flops with D = 1 will SET and those with D = 0 will RESET. Thus all four bits are stored simultaneously.

When SHIFT/LOAD is high, gates G_1 , G_2 , G_3 are disabled and gates G_4 , G_5 , G_6 are enabled. This allows the data bits to shift right from one stage to the next. The OR gates at the D-inputs of the flip-flops allow either the parallel data entry operation or shift operation, depending on which AND gates are enabled by the level on the SHIFT/LOAD input.

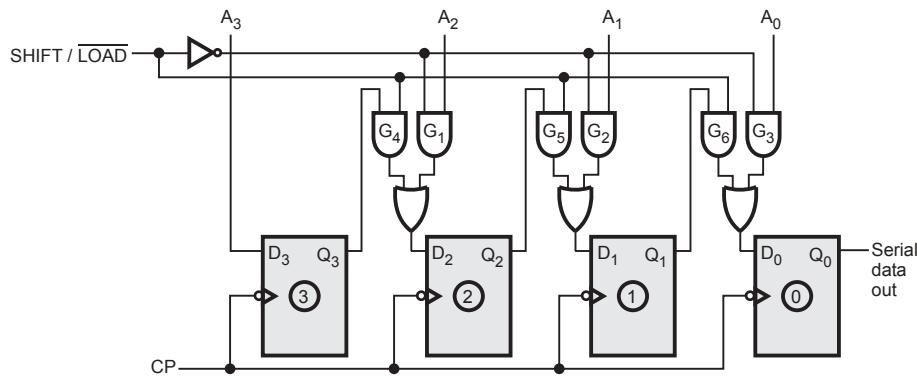


Fig. 5.3.8 Parallel In Serial Out (PISO) shift register

5.3.4 Parallel In Parallel Out (PIPO) Shift Register

From the third and second types of registers, it is cleared that how to enter the data in parallel i.e. all bits simultaneously into the register and how to take data out in parallel from the register. In 'parallel in parallel out register', there is simultaneous entry of all data bits and the bits appear on parallel outputs simultaneously. Fig. 5.3.9 shows this type of register.

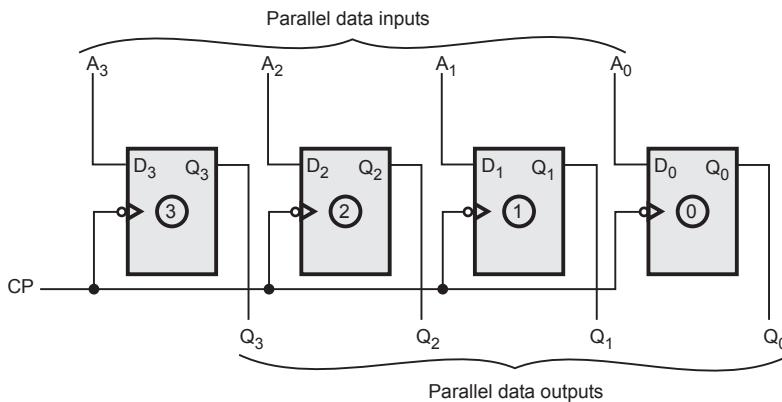


Fig. 5.3.9 Parallel In Parallel Out (PIPO) shift register

5.3.5 Bidirectional Shift Register

This type of register allows shifting of data either to the left or to the right side. It can be implemented by using logic gate circuitry that enables the transfer of data from one stage to the next stage to the right or to the left, depending on the level of a control line. Fig. 5.3.10 illustrates a four-bit bidirectional register. The **RIGHT/LEFT** is the control input signal which allows data shifting either towards right or towards left. A high on this line enables the shifting of data towards right and a low enables it towards left. When **RIGHT/LEFT** signal is high, gates G_1, G_2, G_3, G_4 are enabled. The state of the **Q** output of each flip-flop is passed through the **D** input of the following flip-flop. When a clock pulse arrives, the data are shifted one place to the right. When the **RIGHT/LEFT** signal is low, gates G_5, G_6, G_7, G_8 are enabled. The **Q** output of each flip-flop is passed through the **D** input of the preceding flip-flop. When clock pulse arrives, the data are shifted one place to the left.

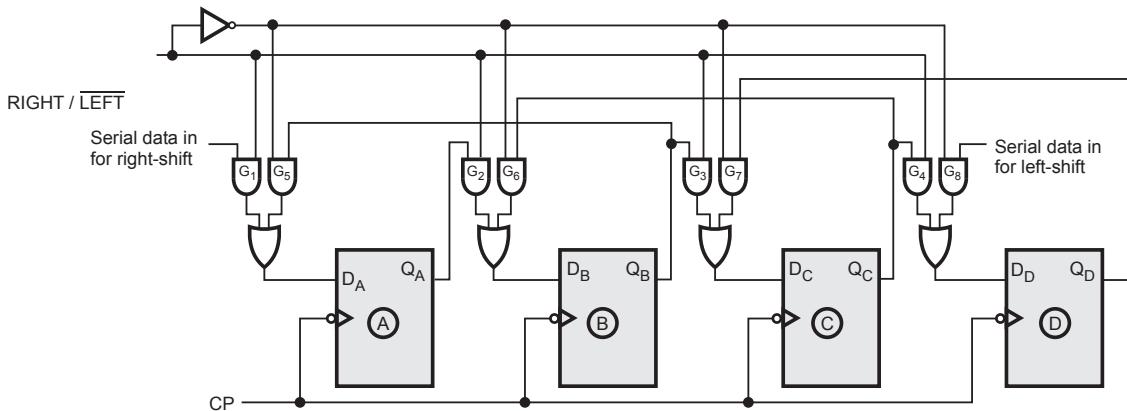


Fig. 5.3.10 4-bit bidirectional shift register

Bidirectional Shift Register with Parallel Load

We have seen that shift register can be used for converting serial data into parallel data, and vice versa. When parallel load capability is added to the shift register, the data entered in parallel can be taken out in serial fashion by shifting the data stored in the register. Such a register is called bidirectional shift register with parallel load. Fig. 5.3.11 shows bidirectional shift register with parallel load.

As shown in the Fig. 5.3.11, the **D** input of each flip-flop has three sources : Output of left adjacent flip-flop, output of right adjacent flip-flop and parallel input. Out of these three sources one source is selected at a time and it is done with the help of decoder. The decoder select lines (SL_1 and SL_0) select the one source out of three as shown in the Table 5.3.4.

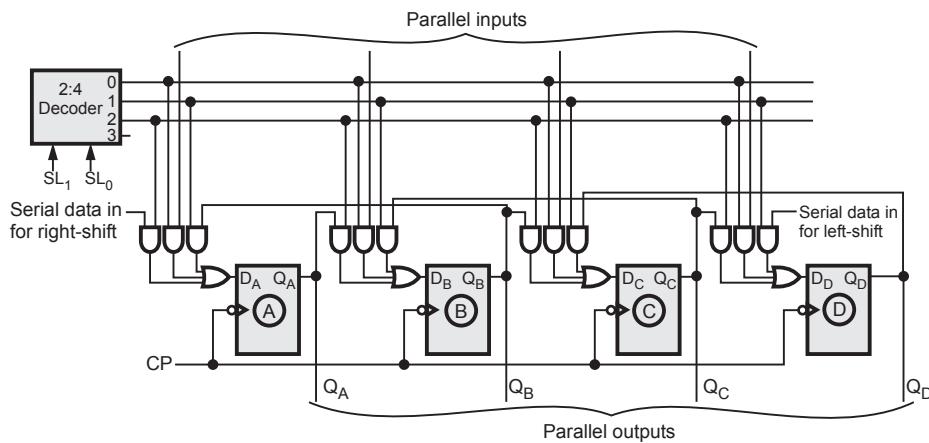


Fig. 5.3.11 4-bit bidirectional shift register with parallel load

When select lines are 00 (i.e. $SL_1 = 0$ and $SL_0 = 0$), data from the parallel inputs is loaded into the 4-bit register. When select lines are 01 (i.e. $SL_1 = 0$ and $SL_0 = 1$), data within the register is shifted 1-bit left. When select lines are 10 (i.e. $SL_1 = 1$ and $SL_0 = 0$), data within the register is shifted 1-bit right.

SL_1	SL_0	Selected source
0	0	Parallel input
0	1	Output of right adjacent FF
1	0	Output of left adjacent FF

Table 5.3.4

Review Questions

1. Draw the logical diagram of a 4-bit shift register. Explain how shift left and shift right operations are performed.
2. Explain modes of operation of shift register.
3. Explain with a neat diagram working of parallel in serial out 4-bit shift register. Draw necessary timing diagram. SPPU : May-10, Marks 6
4. Draw and explain the circuit diagram of 3-bit register with the following facilities :
 - 1) Serial left shift 2) Serial right shift
 - 3) Parallel In-Serial-Out 4) Reset. SPPU : May-05, Marks 10
5. Draw and explain the circuit diagram of 3-bit register with the following facility
 - i) Parallel in serial output ii) Reset. SPPU : Dec.-08, Marks 6
6. Explain how shift registers are used as serial to parallel converters. SPPU : Dec.-08, Marks 3
7. Draw and explain 5-bit shift register having parallel in and serial in (left to right) facilities. Explain any one application of such register. SPPU : May-08, Marks 8
8. Explain serial to parallel shift register with neat circuit diagram and timing diagram. SPPU : Dec.-08, Marks 3; Dec.-12, Marks 8

9. Explain with the help of neat diagram, the operation of 3-bit bidirectional shift register.

SPPU : Dec.-05, Marks 8

10. Draw the circuit and explain the function of 4-bit bidirectional shift register.

SPPU : May-06, Dec.-11, Marks 8

11. Explain with neat diagram working of parallel in serial out 4-bit shift register. Draw necessary timing diagram.

SPPU : May-14 , Marks 6

12. Explain with neat diagram working of serial-in serial-out 4-bit shift register. Draw necessary timing diagram.

SPPU : Dec.-14, Marks 6

5.4 Universal Shift Register

SPPU : Dec.-06,07, May-07

A register capable of shifting in one direction only is a unidirectional shift register. A register capable of shifting in both directions is a bidirectional shift register. If the register has both shifts (right shift and left shift) and parallel load capabilities, it is referred to as **universal shift register**.

The Fig. 5.4.1 shows the 4-bit universal shift register. It has all the capabilities listed above. It consists of four flip-flops and four multiplexers. The four multiplexers have two common selection inputs S_1 and S_0 , and they select appropriate input for D flip-flop. The Table 5.4.1 shows the register operation depending on the selection inputs of multiplexers. When $S_1S_0 = 00$, input 0 is selected and the present value of the register is applied to the D inputs of the flip-flops. This results no change in the register value. When $S_1S_0 = 01$, input 1 is selected and circuit connections are such that it operates as a right shift register. When $S_1S_0 = 10$, input 2 is selected and circuit connections are such that it operates as a left shift register. Finally, when $S_1S_0 = 11$, the binary information on the parallel input lines is transferred into the register simultaneously and it is a parallel load operation. (Refer Fig. 5.4.1 on next page)

Mode control		Register operation
S_1	S_0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Table 5.4.1 Mode control and register operation

Example 5.4.1 Draw the logic diagram of a 4-bit shift register with four D flip-flops and four 4×1 multiplexer with mode selection inputs S_1 and S_0 . The register operates as follows.

S_1	S_0	Register operation
0	0	No change
0	1	Complement
1	0	Clear to 0
1	1	Load parallel data

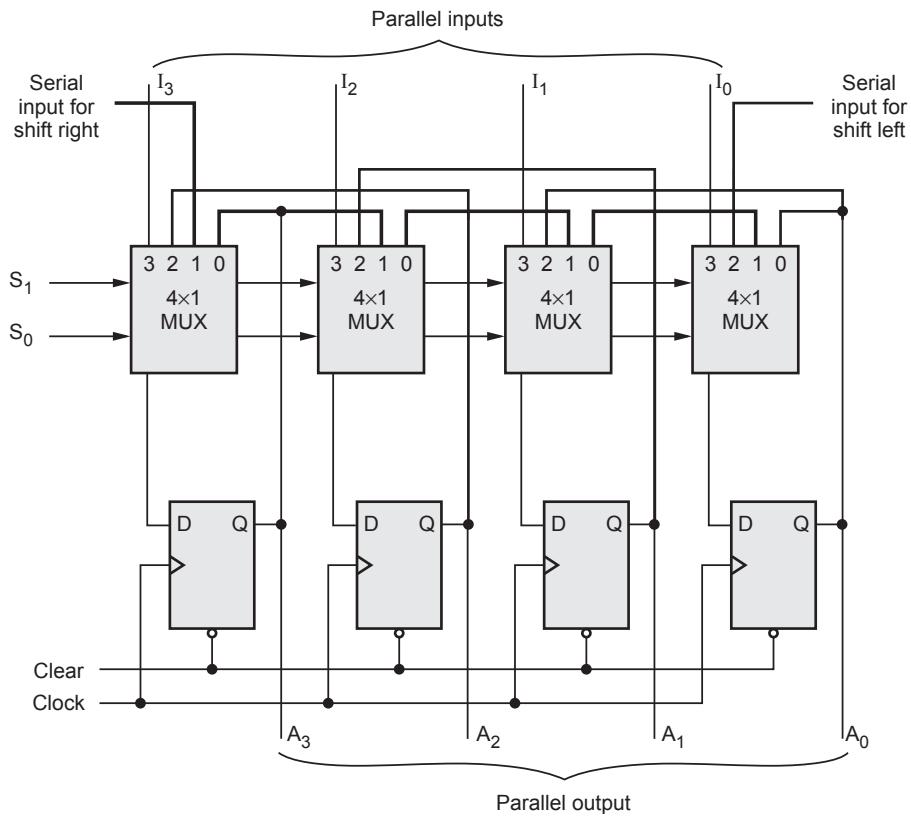


Fig. 5.4.1 4-bit universal shift register

Solution : The Fig. 5.4.2 shows the register that does the given operations.

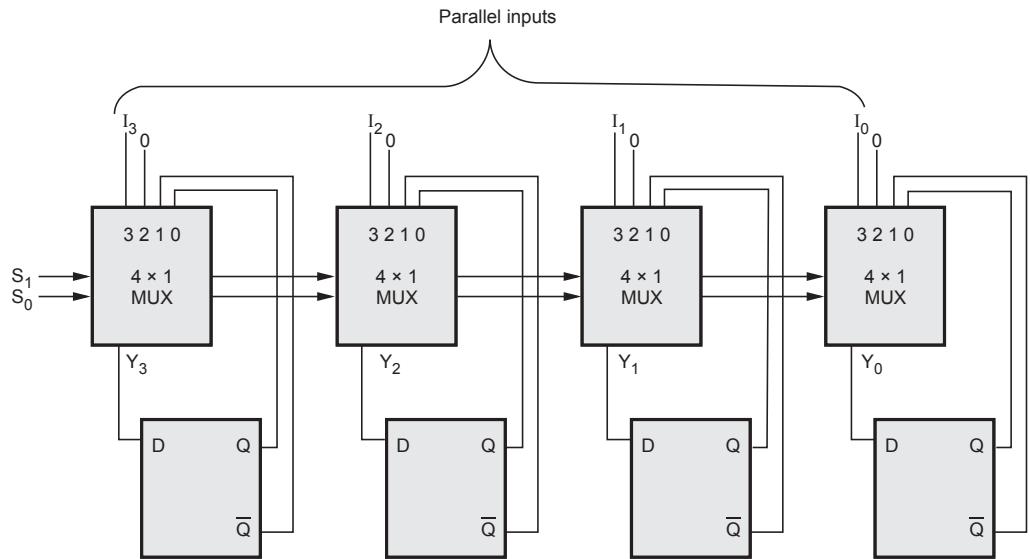


Fig. 5.4.2

Review Questions

1. Explain with the help of neat diagram the operation of 3-bit universal shift register.
2. Draw and explain 4-bit shift register having shift left, shift right and parallel in facilities. Use suitable multiplexers in your circuit. Explain any one application of such register.

SPPU : Dec.-06, Marks 8

3. Design 4-bit shift register with the following facilities : **SPPU : May-07, Dec.-07, Marks 10**

- i) Shift-left (if $L1 = 0$ and $L0 = 0$)
- ii) Shift-right (if $L1 = 0$ and $L0 = 1$)
- iii) Parallel-in (if $L1 = 1$ and $L0 = 1$)

Control signals 'L1 L0' will select one of the possible operation.

5.5 Applications of Shift Registers**SPPU : May-10**

We have seen that primary use of shift register is temporary data storage and bit manipulations. Some of the common applications of shift registers are as discussed below.

5.5.1 Delay Line

A Serial-In-Serial-Out (SISO) shift register can be used to introduce time delay Δt in digital signals. The time delay can be given as

$$\Delta t = N \times \frac{1}{f_c}$$

where N is the number of stages (i.e. flip-flops) and f_c is the clock frequency.

Thus, an input pulse train appears at the output delayed by Δt . The amount of delay can be controlled by the clock frequency or by the number of flip-flops in the shift register.

5.5.2 Serial-to-Parallel Converter

A Serial-In-Parallel-Out (SIPO) shift register can be used to convert data in the serial form to the parallel form.

5.5.3 Parallel-to-Serial Converter

A Parallel-In-Serial-Out (PISO) shift register can be used to convert data in the parallel form to the serial form.

5.5.4 Shift Register Counters

A shift register can also be used as a counter. A shift register with the serial output connected back to the serial input is called **shift register counter**. Because of such a

connection, special specified sequences are produced as the output. The most common shift register counters are the ring counter and the Johnson counter.

5.5.5 Pseudo-Random Binary Sequence (PRBS) Generator

Another important application of shift register is a pseudo-random binary sequence generator. Here, suitable feedback is used to generate pseudo-random sequence. The term random here means that the outputs do not cycle through a normal binary count sequence. The term pseudo here refers to the fact that the sequence is not truly random because it does cycle through all possible combinations once every $2^n - 1$ clock cycles, where n represents the number of shift register stages (number of flip-flops).

5.5.6 Sequence Generator

The shift register can be used to generate a particular bit pattern repetitively. The Fig. 5.5.1 shows the basic block diagram of a sequence generator. Here, left

most flip-flop input accept the serial input and the right most flip-flop gives serial data output. It is important to note that the serial data output signal is connected as a serial data in. On every clock pulse the data shift operation takes place. We get the loaded bit pattern at the serial output in a sequence. Same bit pattern is again loaded in the register since serial output is connected serial in of the register. Thus, the circuit generates a particular bit pattern repetitively.

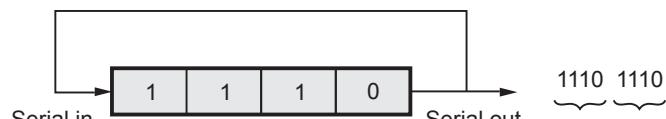


Fig. 5.5.1 4-bit sequence generator

5.5.7 Sequence Detector

The shift register can be used to detect the desired sequence. The detection process requires two registers : one register stores the bit pattern to be detected i.e. R_1 and other register accepts the input data stream i.e. R_2 . Input data stream enters a shift register as serial data in and leaves as serial out. In every clock cycle, bit-wise comparisons of these two registers are done using EX-NOR gates as shown in the Fig. 5.5.2. We know that, the two-input EX-NOR gate gives logic high output when both inputs are either low or high, i.e. when both are equal. When outputs of all the EX-NORs gates are logic high we can say that all bits are

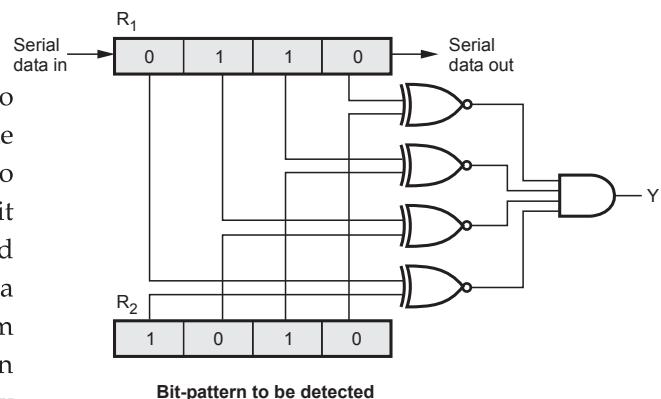


Fig. 5.5.2 4-bit sequence detector

matched and hence the desired bit pattern is detected. The final output which indicates that the pattern is detected is taken from four-input AND gate.

The 4-bit sequence detector shown in Fig. 5.5.2 can be made programmable by loading the desired 4-bit data in the register R_2 .

Review Question

1. Give any four applications of shift registers.

SPPU : May-10, Marks 4

UNIT - III

6

Counters

Syllabus

Asynchronous counter, Synchronous Counter, BCD Counter, Ring Counter, Johnson Counter Modulus of the counter (IC 7490).

Contents

6.1	<i>Introduction</i>	May-07,12,13, Dec.-12,18, · Marks 4
6.2	<i>Ripple / Asynchronous Counters</i>	May-07,08,11, Dec.-05,07, Marks 8
6.3	<i>Design of Ripple (Asynchronous) Counters</i>	Dec.-07, May-07, Marks 4
6.4	<i>Synchronous Counters.</i>	May-07,08,10, Dec.-10,12, Marks 10
6.5	<i>Design of Synchronous Counters</i>	May-12,14,15,18, Dec.-13,19, Marks 6
6.6	<i>Lock-Out</i>	Dec.-11,15,18, May-13, · Marks 6
6.7	<i>IC 7490 (Decade Binary Counter)</i>	Dec.-04,05,06,10,11,12,17, May-07,11,12,13,15,17, · Marks 10
6.8	<i>Ring Counter</i>	Dec.-08,10,19, May-11 · Marks 10
6.9	<i>Johnson or Twisting Ring or Switch Tail Counter</i>	Dec.-08,17,18, Marks 4

6.1 Introduction

SPPU : May-07,12,13, Dec.-12, 18

A group of flip-flops connected together forms a **register**. A register is used solely for storing and shifting data which is in the form of 1s and/or 0s, entered from an external source. It has no specific sequence of states except in certain very specialized applications. A **counter** is a register capable of counting the number of clock pulses arriving at its clock input. Count represents the number of clock pulses arrived. On arrival of each clock pulse, the counter is incremented by one. In case of down counter, it is decremented by one.

The Fig. 6.1.1 shows the logic symbol of a binary counter. External clock is applied to the clock input of the counter. The counter can be positive edge triggered or negative edge triggered. The

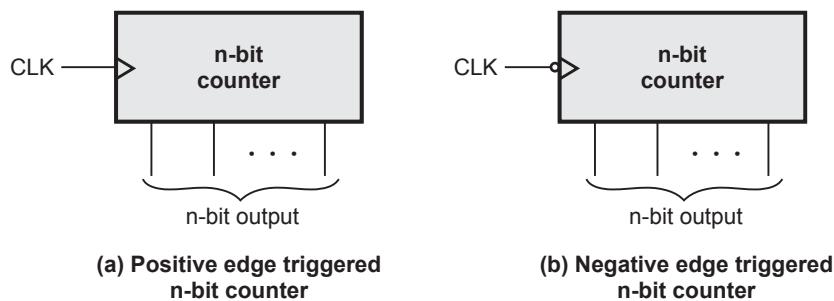


Fig. 6.1.1 Logic symbol of counter

n-bit binary counter has n flip-flops and it has 2^n distinct states of outputs. For example, 2-bit counter has 2 flip-flops and it has $4(2^2)$ distinct states : 00, 01, 10 and 11. Similarly, the 3-bit binary counter has 3 flip-flops and it has $8(2^3)$ distinct states : 000, 001, 010, 011, 100, 101 110 and 111.

The maximum count that the binary counter can count is 2^{n-1} . For example, in 2-bit binary counter, the maximum count is $2^2 - 1 = 3$ (11 in binary). After reaching the maximum count the counter resets to 0 on arrival of the next clock pulse and it starts counting again.

Synchronous Counter : When counter is clocked such that each flip-flop in the counter is triggered at the same time, the counter is called synchronous counter.

Asynchronous Counter / Ripple Counter : A binary asynchronous/ripple counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the clock input of the next higher-order flip-flop. The flip-flop holding the least significant bit receives the incoming clock pulses.

The Table 6.1.1 shows the comparison between synchronous and asynchronous counters.

Sr. No.	Asynchronous counters	Synchronous counters
1.	In this type of counter flip-flops are connected in such a way that output of first flip-flop drives the clock for the next flip-flop.	In this type there is no connection between output of first flip-flop and clock input of the next flip-flop.
2.	All the flip-flops are not clocked simultaneously.	All the flip-flops are clocked simultaneously.
3.	Logic circuit is very simple even for more number of states.	Design involves complex logic circuit as number of states increases.
4.	Main drawback of these counters is their low speed as the clock is propagated through number of flip-flops before it reaches last flip-flop.	As clock is simultaneously given to all flip-flops there is no problem of propagation delay. Hence they are high speed counters and are preferred when number of flip-flops increases in the given design.

Table 6.1.1 Synchronous Vs asynchronous counters

Modulus of Counter

The total number of counts or stable states a counter can indicate is called 'Modulus'. For instance, the modulus of a four-stage counter would be 16_{10} , since it is capable of indicating 0000_2 to 1111_2 . The term 'modulo' is used to describe the count capability of counters. For example, mod 6 counter goes through states 0 to 5 and mod 4 counter goes through states 0 - 3.

Example 6.1.1 Draw the state diagram of MOD-10 counter.

Solution :

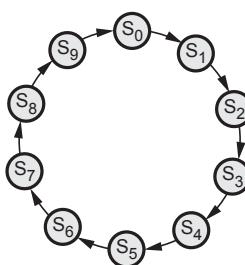


Fig. 6.1.2

Example 6.1.2 Assume that the 5-bit binary counter starts in the 00000 state. What will be the count after 144 input pulses ?

Solution : $(144)_{10} = (1001\ 0000)_2$

Since counter is a 5-bit counter, it resets after $2^5 = 32$ clock pulses.

$$\begin{array}{r}
 & \frac{4}{32)144} \\
 & \quad - 128 \\
 & \quad \hline
 & \quad 16
 \end{array}$$

Therefore, counter resets four times and then it counts remaining 16 clock pulses. Thus, the count will be $(10000)_2$, i.e., 16 in decimal.

In general,

$$\text{Count} = \text{Remainder of } \left[\frac{\text{Number of input pulses}}{2^n} \right] \text{ in binary}$$

where n = Number of counter bits

Review Questions

1. What is counter ?
2. State types of counters.
3. Compare synchronous and asynchronous counter.
4. What is MOD counter ?
5. Differentiate between synchronous and asynchronous counters.

SPPU : May-13, Marks 2

SPPU : May-07,12, Dec.-12,18, Marks 4

6.2 Ripple / Asynchronous Counters

SPPU : May-07,08,11, Dec.-05,07

A binary ripple/asynchronous counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the clock input of the next higher-order flip-flop. The flip-flop holding the least significant bit receives the incoming clock pulses. A complementing flip-flops can be obtained from a JK flip-flop with the J and K inputs tied together as shown in the Fig. 6.2.1 or from a T flip-flop. A third alternative is to use a D flip-flop with the complement output connected to the D input. In this way, the D input is always the complement of the present state and the next clock pulse will cause the flip-flop to complement. Let us see the ripple counter using JK flip-flop.

Fig. 6.2.1 (a) shows 2-bit asynchronous counter using JK flip-flops. As shown in Fig. 6.2.1 (a), the clock signal is connected to the clock input of only first stage flip-flop. The clock input of the second stage flip-flop is triggered by the Q_A output of the first stage. Because of the inherent propagation delay time through a flip-flop, a transition of the input clock pulse and a transition of the Q_A output of first stage can never occur at exactly the same time. Therefore, the two

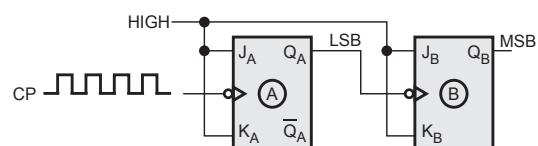


Fig. 6.2.1 (a) A two-bit asynchronous binary counter

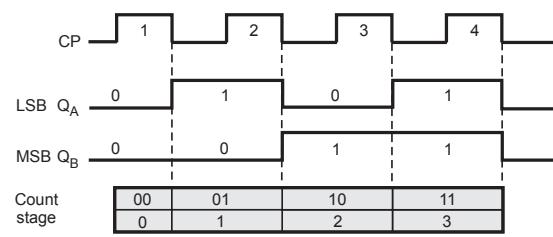


Fig. 6.2.1 (b) Timing diagram for the counter of Fig. 6.2.1 (a)

flip-flops are never simultaneously triggered, which results in asynchronous counter operation.

Fig. 6.2.1 (b) shows the timing diagram for two-bit asynchronous counter. It illustrates the changes in the state of the flip-flop outputs in response to the clock. J and K input of JK flip-flops are tied to logic HIGH hence output will toggle for each negative edge of the clock input.

Example 6.2.1 Extend the counter shown in Fig. 6.2.1 (a) for 3-stages, and draw output waveforms.

Solution :

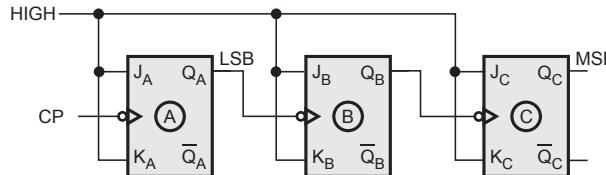


Fig. 6.2.2 (a) Logic diagram

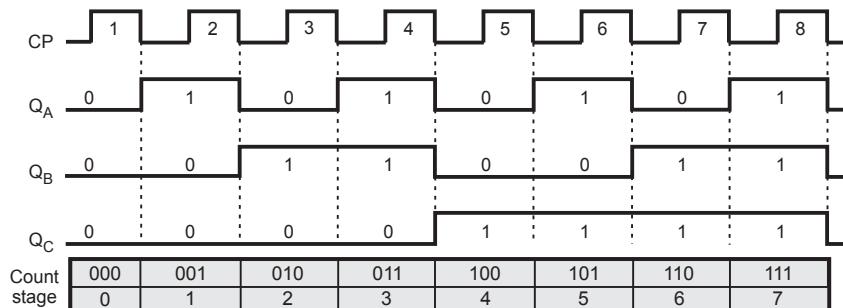


Fig. 6.2.2 (b) Output waveforms for 3-bit asynchronous counter

In Fig. 6.2.2 (b), timing diagram for 3-bit asynchronous counter we have not considered the propagation delays of flip-flops, for simplicity. If we consider the propagation delays of flip-flops we get timing diagram as shown in Fig. 6.2.3.

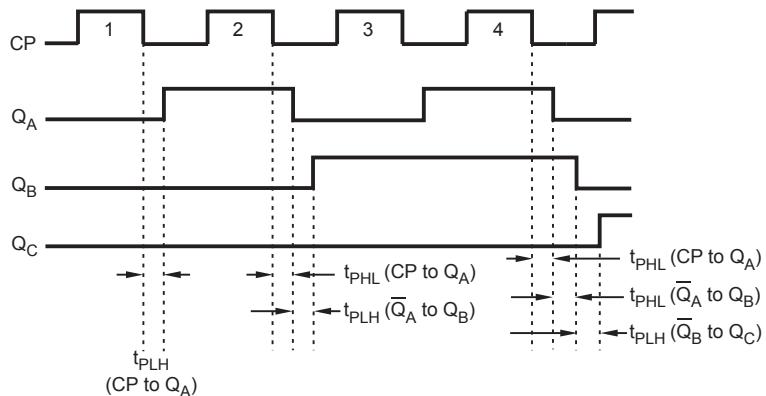


Fig. 6.2.3 Propagation delays in a ripple clocked binary counter

The timing diagram shows propagation delays. We can see that propagation delay of the first stage is added in the propagation delay of second stage to decide the transition time for third stage. This cumulative delay of an asynchronous counter is a major

disadvantage in many applications because it limits the rate at which the counter can be clocked and creates decoding problems.

Example 6.2.2 Draw the logic diagram for 3-stage asynchronous counter with negative edge triggered flip-flops.

Solution : When flip-flops are negatively edge triggered, the Q output of previous stage is connected to the clock input of the next stage. Fig. 6.2.4 shows 3-stage asynchronous counter with negative edge triggered flip-flops.

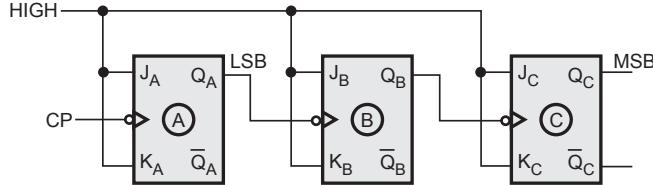


Fig. 6.2.4 Logic diagram of 3-stage negative edge triggered counter

Example 6.2.3 A counter has 14 stable states 0000 through 1101. If the input frequency is 50 kHz what will be its output frequency ?

$$\text{Solution : } \frac{50 \text{ kHz}}{14} = 3.57 \text{ kHz}$$

Example 6.2.4 The t_{pd} for each flip-flop is 50 ns, determine the maximum operating frequency for MOD-32 ripple counter.

Solution : We know that MOD-32 uses five flip-flops. With $t_{pd} = 50$ ns, the f_{\max} for ripple counter can be given as,

$$f_{\max}(\text{ripple}) = \frac{1}{5 \times 50 \text{ ns}} = 4 \text{ MHz}$$

Example 6.2.5 Draw the logic diagram for 4-stage asynchronous counter with positive edge triggered flip-flops. Also draw necessary timing diagram. Is there any frequency division concept in it.

SPPU : Dec.-07, May-08, Marks 8

Solution : When flip-flops are positive edge triggered, the \bar{Q} output of previous stage is connected to the clock input of the next stage. Fig. 6.2.5 shows 4-stage asynchronous counter with positive edge triggered flip-flops.

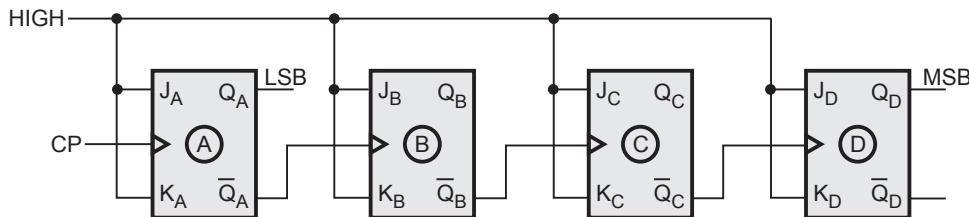


Fig. 6.2.5 Logic diagram of 4-stage positive edge triggered ripple counter

The Fig. 6.2.6 shows the timing diagram for 4-bit ripple up counter using positive edge triggered JK-FFs.

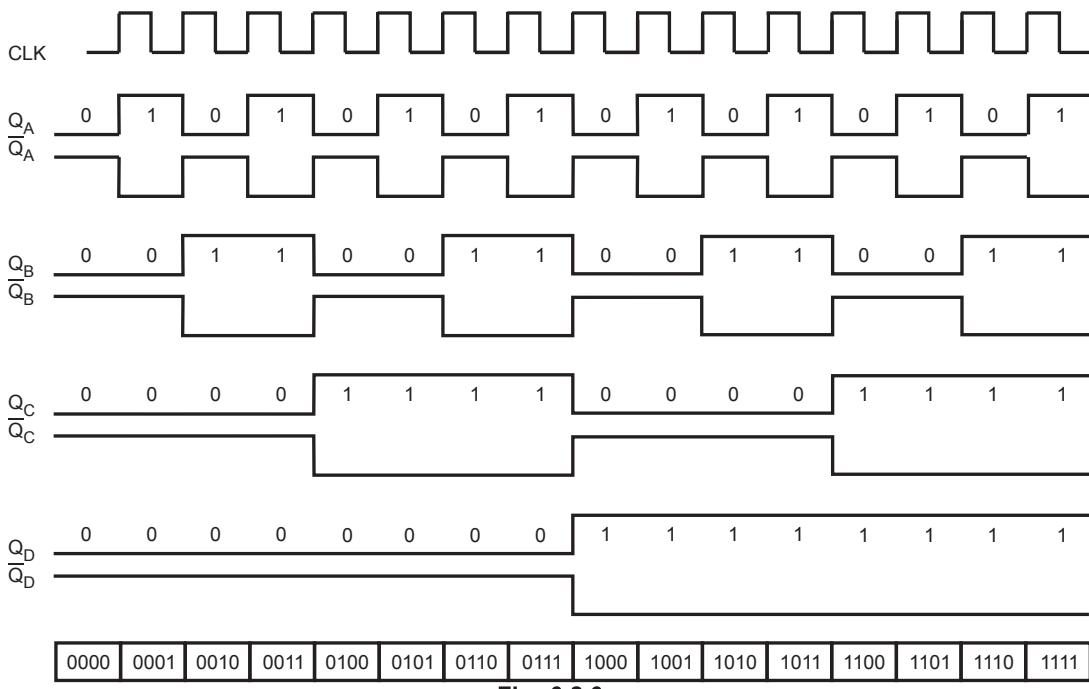


Fig. 6.2.6

From the timing diagram we can observe that

- Frequency at output $Q_A = \frac{F_{CLK}}{2}$
- Frequency at output $Q_B = \frac{Q_A}{2} = \frac{F_{CLK}}{4}$
- Frequency at output $Q_C = \frac{Q_B}{2} = \frac{Q_A}{4} = \frac{F_{CLK}}{8}$
- Frequency at output $Q_D = \frac{Q_C}{2} = \frac{Q_B}{4} = \frac{Q_A}{8} = \frac{F_{CLK}}{16}$

In general we can say that the frequency at the MSB output of counter is $\frac{F_{CLK}}{2^N}$

where N represents number of stages/bits of the counter.

6.2.1 Asynchronous / Ripple Down Counter

In the last section we have seen that the output of counter is incremented by one for each clock transition. Therefore, we call such counters as up **counters**. In this section we see the asynchronous/ripple down counter. The down counter will count downward from a maximum count to zero.

The Fig. 6.2.7 shows the 4-bit asynchronous down counter using JK flip-flops. Here, the clock signal is connected to the clock input of only first flip-flop. This connection is same as asynchronous/ripple up counter. However, the clock input of the remaining

flip-flops is triggered by the \bar{Q}_A output of the previous stage instead of Q_A output of the previous stage.

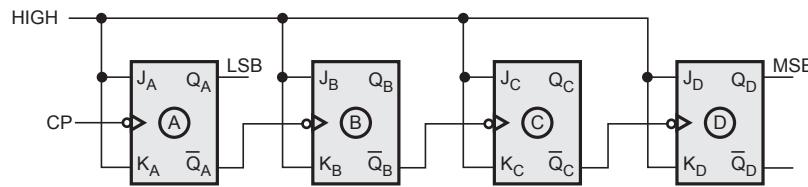


Fig. 6.2.7 4-bit asynchronous down counter

The Fig. 6.2.8

shows the timing diagram for 4-bit asynchronous down counter. It illustrates the changes in the state of the flip-flop outputs in response to the clock. Again the J and K inputs of JK flip-flops are tied to logic HIGH hence output will toggle for each negative edge of the clock input.

Down counters are not as widely used as up counters. They are used in situations where it must be known when a desired number of input pulses has occurred. In these situations the down counter is preset to the desired number and then allowed to count down as the pulses are applied. When the counter reaches the zero state it is detected by a logic gate whose output then indicates that the preset number of pulses have occurred.

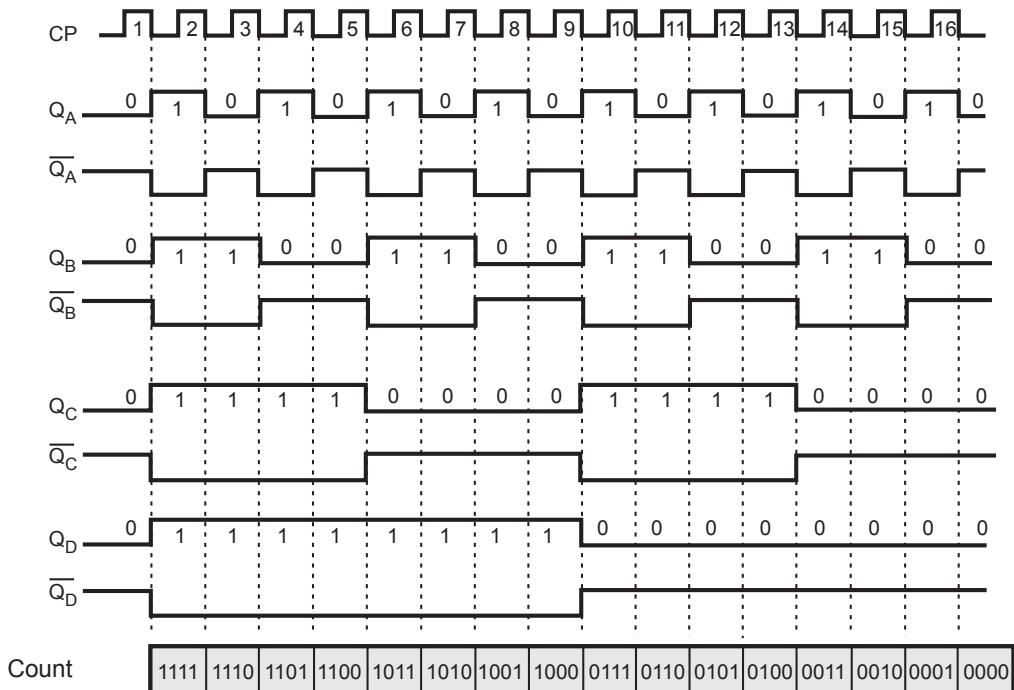


Fig. 6.2.8 Timing diagram of 4-bit asynchronous down counter

Example 6.2.6 For the ripple counter shown in Fig. 6.2.9, show the complete timing diagram for eight clock pulses, showing the clock, Q_0 and Q_1 waveforms.

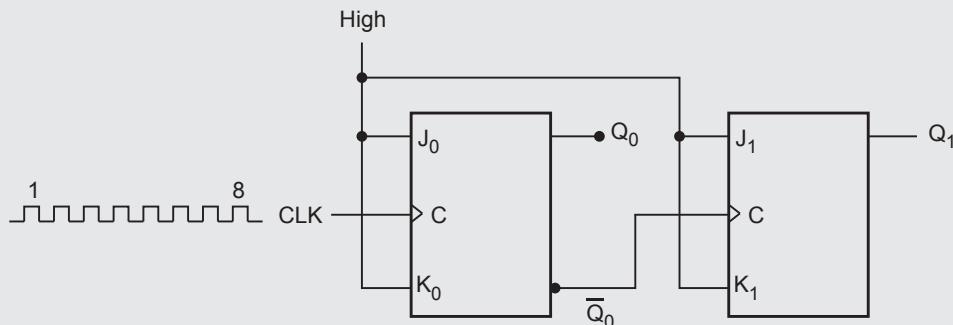


Fig. 6.2.9

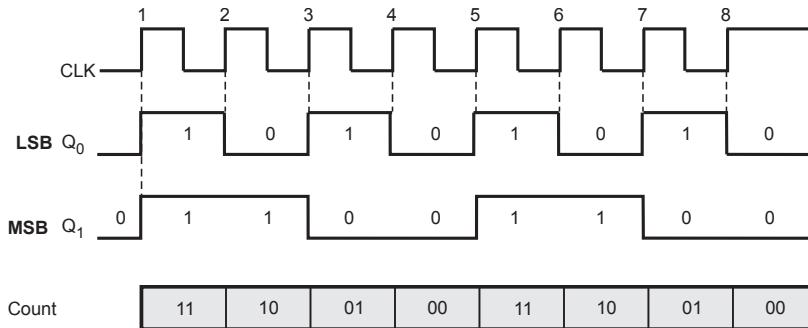
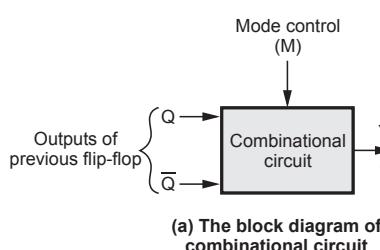
Solution :

Fig. 6.2.9 (a)

6.2.2 Asynchronous Up / Down Counter

To form an asynchronous up/down counter one control input say M is necessary to control the operation of the up/down counter. When M = 0, the counter will count up and when M = 1, the counter will count down. To achieve this the M input should be used to control whether the normal flip-flop

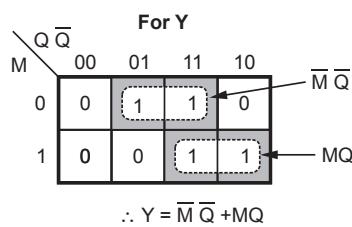


Inputs	Output
M Q Q	Y
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	1
1 0 0	0
1 0 1	0
1 1 0	1
1 1 1	1

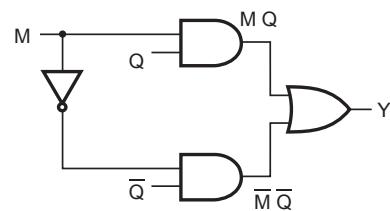
M = 0 } $Y = \bar{Q}$ for down counting
 M = 1 } $Y = Q$ for up counting

(b) Truth table

Fig. 6.2.10



a) K-map simplification



b) Logic diagram

Fig. 6.2.11

output (Q) or the inverted flip-flop output (\bar{Q}) is fed to drive the clock signal of the

successive stage flip-flop, as shown in Fig. 6.2.10 (a). The truth table for such combinational circuit is shown in Fig. 6.2.10 (b).

The Fig. 6.2.12 shows the 3-bit up/down counter that will count from 000 up to 111 when the mode control input M is 1 and from 111 down to 000 when mode control input M is 0.

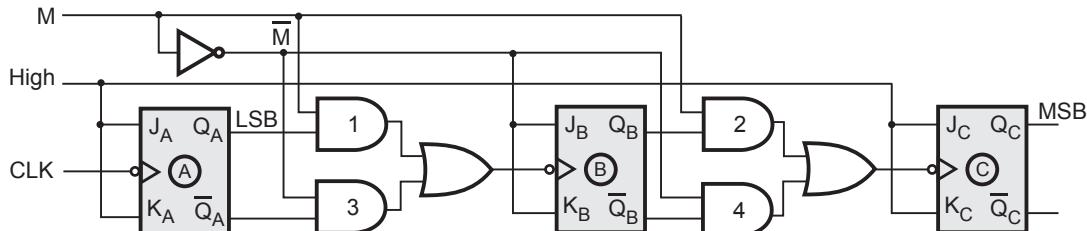


Fig. 6.2.12 3-bit asynchronous up/down counter

A logic 1 on M enables AND gates 1 and 2 and disables AND gates 3 and 4. This allows the Q_A and Q_B outputs to drive the clock inputs of their respective next stages. So that counter will count up. When M is logic 0, AND gates 1 and 2 are disabled and AND gate 3 and 4 are enabled. This allows the \bar{Q}_A and \bar{Q}_B outputs to drive the clock inputs of their respective next stages so that counter will count down. The Fig. 6.2.13 shows the timing diagram for 3-bit up/down ripple counter. (See Fig. 6.2.13 on next page).

Example 6.2.7 Design a 4-bit up/down ripple counter with a control for up/down counting.

Solution : The 4-bit counter needs four flip-flops. The circuit for 4-bit up/down ripple counter is similar to 3-bit up/down ripple counter except that 4-bit counter has one more flip-flop and its clock driving circuiting.

The Fig. 6.2.14 shows the 4-bit up/down ripple counter.

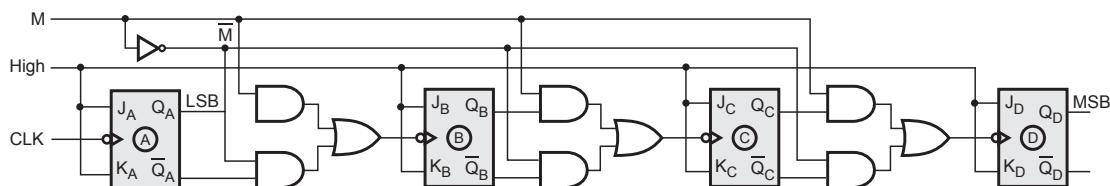


Fig. 6.2.14 4-bit asynchronous up/down counter

6.2.3 Decoding Gates

Decoding gates are used to indicate whether counter has reached to particular state. The outputs of the counter are connected to the AND gate as inputs and the output of the AND gate goes high for particular state. Let us see the Fig. 6.2.14 (a). Here, the output of decoding gate goes high when counter outputs are C = 1, B = 1 and A = 1. In

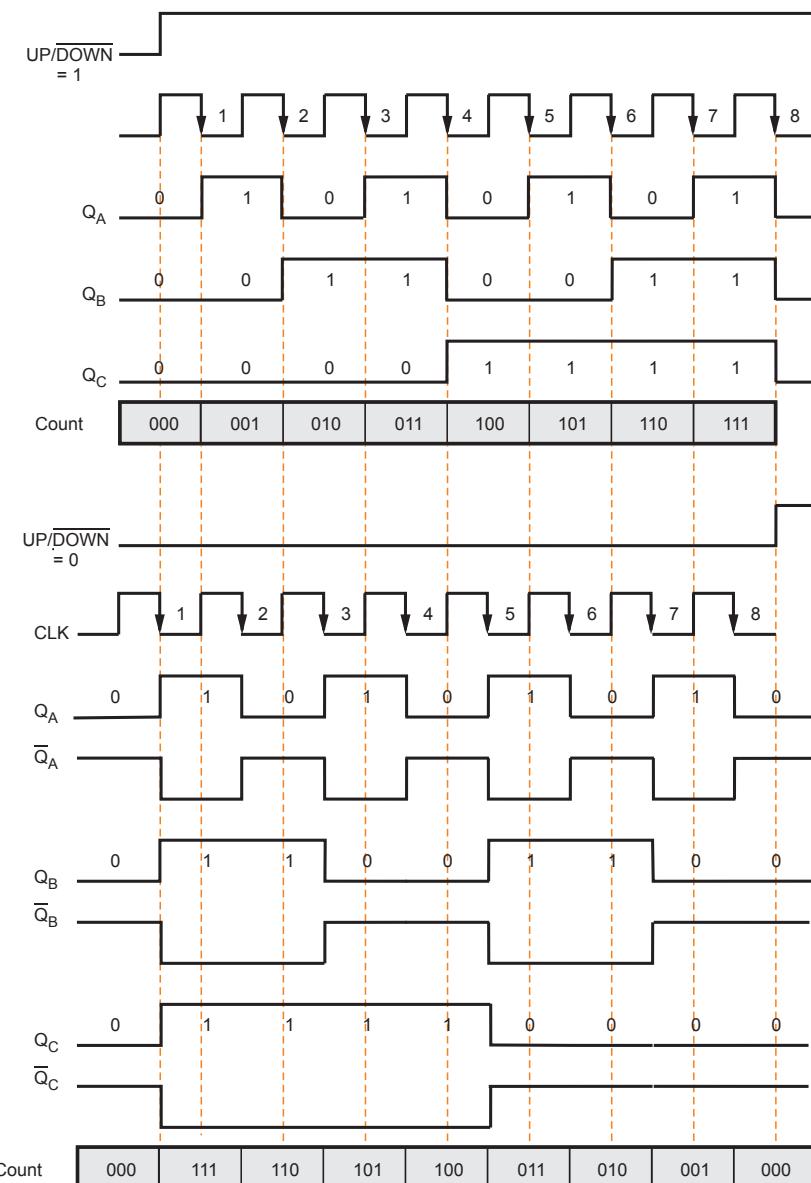


Fig. 6.2.13 Timing diagram for 3-bit UP/ DOWN ripple counter

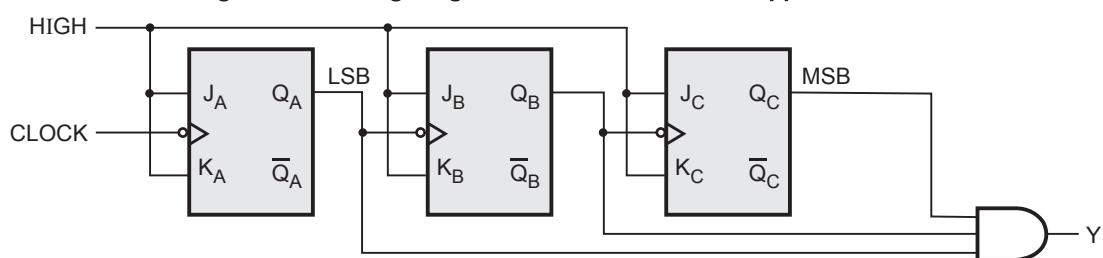


Fig. 6.2.15 (a) Decoding gate to indicate state 7 (111)

Fig. 6.2.15 (b) the output of decoding gate goes high when counter outputs are C = 1, B = 0 and A = 0.

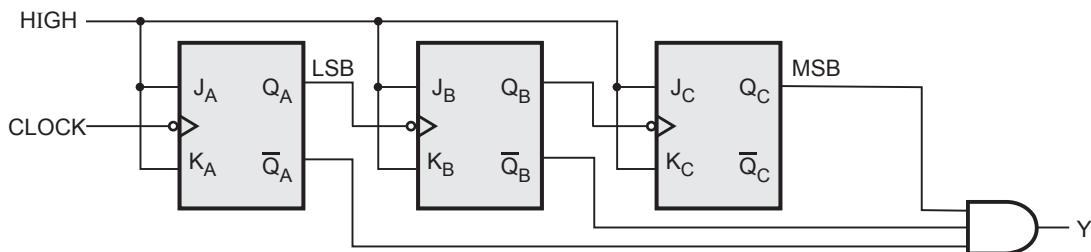


Fig. 6.2.15 (b) Decoding gate to indicate state 4 (100)

Similarly, we can connect corresponding outputs to decoding gate inputs to indicate desired state. The Fig. 6.2.16 gives these connections for all possible state detection for 3-bit counter.

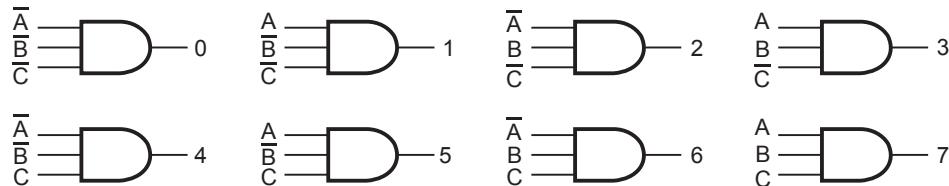


Fig. 6.2.16 Decoding gate connections

6.2.4 Problem Faced by Ripple Counters (Glitch Problem)

We know that, due to the propagation delay the output flip-flop is delayed by time t_p . This is illustrated in the waveform shown in Fig. 6.2.17 shows the waveform of the circuit which decodes state 7. Here, the output of flip-flop A triggers the flip-flop B,

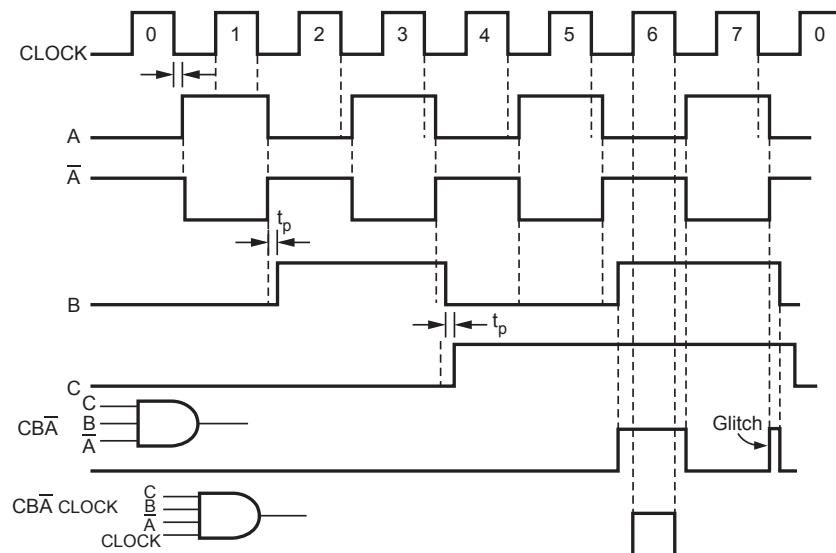


Fig. 6.2.17 Elimination of glitch

hence the B waveform is delayed by one flip-flop delay time (t_p) from the negative transition of A. Similarly, the C waveform is delayed by t_p from each negative transition of B.

Let us observe the output waveform when the counter progresses from state 7 to state 0. At point X, A goes low (\bar{A} goes high); however, because of flip-flop delay time, B does not go low until point Y. Thus between points X and Y we have the condition C = 1, B = 1 and A = 1. As a result, the output is high between points X and Y. This undesirable output is known as **glitch**. We can avoid the glitch on the output waveform by connecting clock as a fourth input to the decoding gate along with inputs A, B and C. This is illustrated in the Fig. 6.2.16.

Review Questions

1. *What do you mean by ripple counter ?* SPPU : May-08, Marks 2
2. *Draw and explain 3-bit asynchronous up counter using flip-flops and explain with output waveforms.* SPPU : May-07, Marks 6
3. *Draw 4-bit asynchronous counter. Also explain timing diagram for the same.* SPPU : May-11, Marks 8
4. *Draw and explain 3-bit up/down asynchronous counter.*
5. *What do you mean by decoding gates ?*
6. *Explain the problem of glitches in asynchronous counter circuits and solution for the same.* SPPU : Dec.-07, Marks 4
7. *Explain using suitable waveforms : Problems faced by ripple counter.* SPPU : Dec.-05, Marks 6

6.3 Design of Ripple (Asynchronous) Counters

SPPU : Dec.-07, May-07

The steps involved in the design of asynchronous counter are :

1. Determine the number of flip-flops needed.
2. Choose the type of flip-flops to be used : T or JK. If T flip-flops are used connect T input of all flip-flops to logic 1. If JK flip-flops are used connect both J and K inputs of all flip flops to logic 1.
Such connection toggles the flip-flop output on each clock transition.
3. Write the truth table for the counter.
4. Derive the reset logic by K-map simplification.
5. Draw the logic diagram.

Example 6.3.1 Design BCD ripple counter using JK flip-flop.

SPPU : Dec.-07

Solution : **Step 1 :** Determine the number of flip-flops needed. The BCD counter goes through states 0-9, i.e. total 10 states. Thus, $N = 10$ and for $2^n \geq N$, we need $n = 4$, i.e. 4 flip-flops required.

Step 2 : Type of flip-flops to be used : JK

Step 3 : Write the truth table for the counter

CLK	D	C	B	A	Output of reset logic Y
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
-	1	0	1	0	0
-	1	0	1	1	0
-	1	1	0	0	0
-	1	1	0	1	0
-	1	1	1	0	0
-	1	1	1	1	0

Note : The reset input (CLR) of each Flip-Flop is active-low input. By making CLR input of all Flip-Flops logic 0, we can reset the counter. Thus reset logic is designed such a way that for invalid states, $Y = 0$ and counter resets.

Valid states

Invalid states

Table 6.3.1 Truth table for BCD counter

Step 4 : Derive reset logic

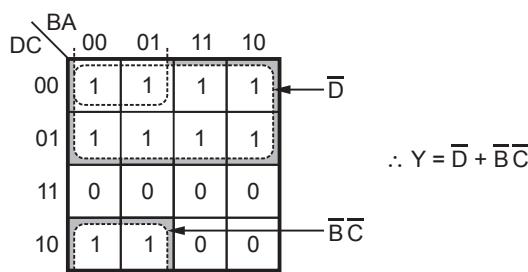


Fig. 6.3.1

Step 5 : Draw logic diagram.

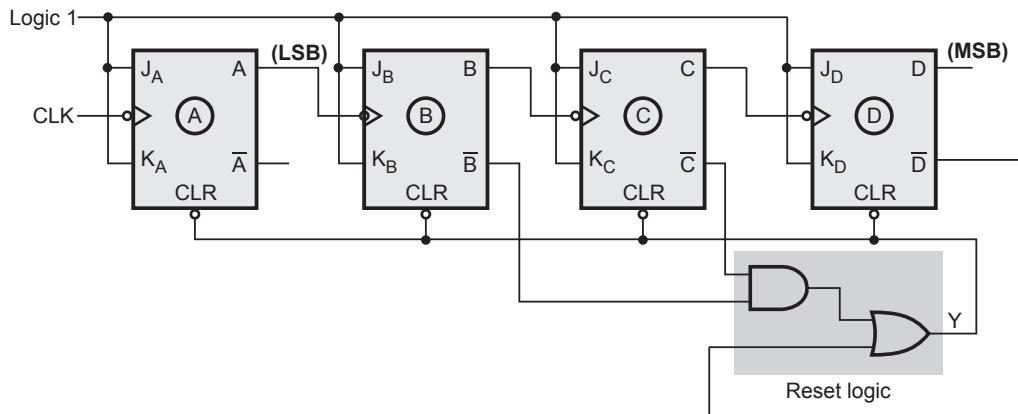


Fig. 6.3.2 Logic diagram of BCD ripple counter

Example 6.3.2 Design a 3-bit asynchronous ripple counter using T flip-flops and explain its operation.

Solution : The Fig. 6.3.3 shows a 3-bit asynchronous ripple counter using T flip-flops. As shown in Fig. 6.3.3, the clock input of only first stage flip-flop. The clock input of the second stage flip-flop is triggered by the Q_A output of the first stage and third stage flip-flop is triggered by the Q_A output of second stage. Because of the inherent propagation delay time through a flip-flop, a transition of the input clock pulse and a transition of the Q_A output of previous stage can never occur at exactly the same time. Therefore, flip-flops are never simultaneously triggered, which results in asynchronous counter operation.

Since, T input is connected to logic 1 each flip-flop toggles at clock input. The Fig. 6.3.4 shows the timing diagram for 3-bit asynchronous counter.

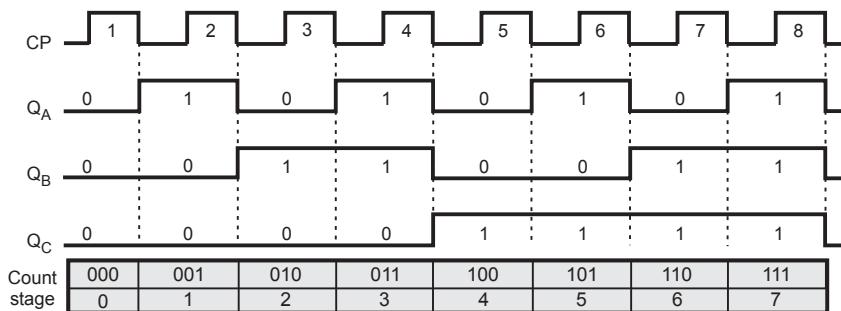


Fig. 6.3.4 Output waveforms for 3-bit asynchronous counter

Example 6.3.3 Design mod 6 ripple counter using T flip-flops.

Solution :

Step 1 : Determine the number of flip-flop required. Here, counter goes through 0 - 5 states, i.e., total 6 states. Thus $N = 6$ and for $2^n \geq N$ we need $n = 3$, i.e. 3 flip-flops.

Step 2 : Type of flip-flops to be used : T

Step 3 : Write the truth table for counter

CLK	C	B	A	Output of reset logic Y
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
-	1	1	0	0
-	1	1	1	0

Fig. 6.3.5

Step 4 : Derive reset logic

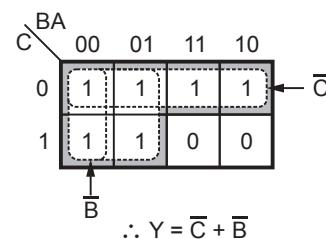


Fig. 6.3.6

Step 5 : Draw logic diagram

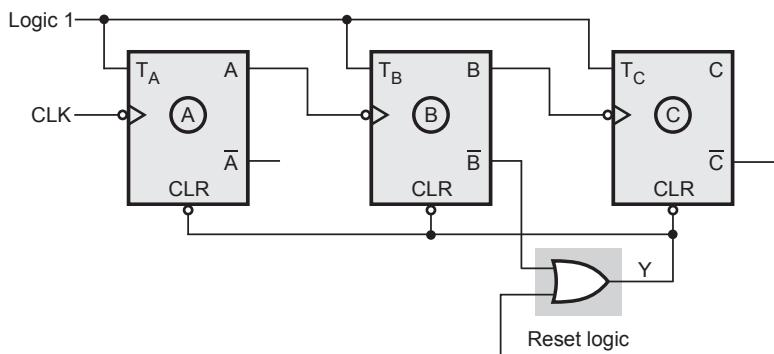


Fig. 6.3.7

Review Question

1. Design 3-bit down ripple counter. Draw waveforms.

SPPU : May-07, Marks 4

6.4 Synchronous Counters

SPPU : May-07,08,10, Dec.-10,12

When counter is clocked such that each flip-flop in the counter is triggered at the same time, the counter is called as synchronous counter.

6.4.1 2-bit Synchronous Binary Up Counter

Fig. 6.4.1 shows two stage synchronous counter.

Here, clock signal is connected in parallel to clock inputs of both the flip-flops. But the Q_A output of first stage is used to drive the J and K inputs of the second stage. Let us see the operation of the circuit. Initially, we assume

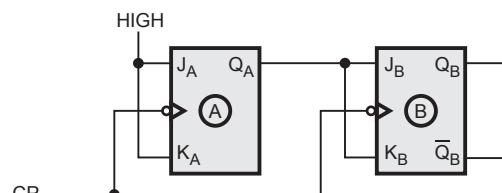


Fig. 6.4.1 A two-bit synchronous binary counter

that the $Q_A = Q_B = 0$. When positive edge of the first clock pulse is applied, flip-flop A will toggle because $J_A = K_A = 1$, whereas flip-flop B output will remain zero because $J_B = K_B = 0$. After first clock pulse $Q_A = 1$ and $Q_B = 0$. At negative going edge of the second clock pulse both flip-flops will toggle because they both have a toggle condition on their J and K inputs ($J_A = K_A = J_B = K_B = 1$). Thus after second clock pulse, $Q_A = 0$ and $Q_B = 1$. At negative going edge of the third clock pulse flip-flop A toggles making $Q_A = 1$, but flip-flop B remains set i.e. $Q_B = 1$. Finally, at the leading edge of the fourth clock pulse both flip-flops toggle as their JK inputs are at logic 1. This results $Q_A = Q_B = 0$ and counter recycled back to its original state. The timing details of above operation is shown in Fig. 6.4.2.

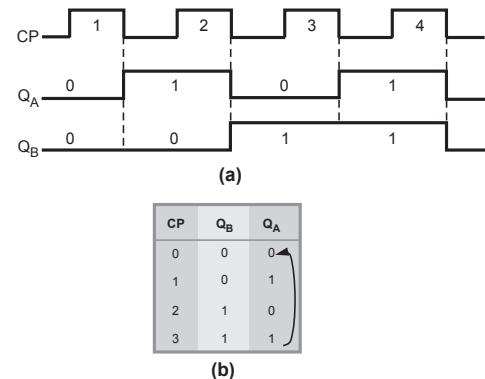


Fig. 6.4.2 Timing diagram and state sequence for the 2-bit synchronous counter

6.4.2 3-bit Synchronous Binary Up Counter

Fig. 6.4.3 (a) shows 3-bit synchronous binary counter and its timing diagram. The state sequence for this counter is shown in Table 6.4.1.

Looking at Fig. 6.4.3 (b), we can see that Q_A changes on each clock pulse as we progress from its original state to its final state and then back to its original state. To produce this operation, flip-flop A is held in the toggle mode by connecting J and K inputs to HIGH. Now let us see what flip-flop B does. Flip-flop B toggles, when Q_A is 1. When Q_A is a 0, flip-flop B is in the no-change mode and remains in its present state. Looking at the Table 6.4.1 we can notice that flip-flop C has to change its state only when

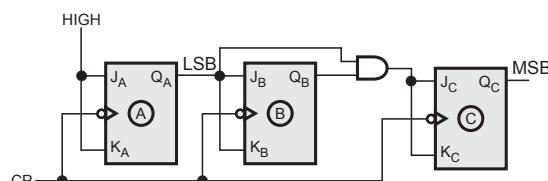


Fig. 6.4.3 (a) A three-bit synchronous binary counter

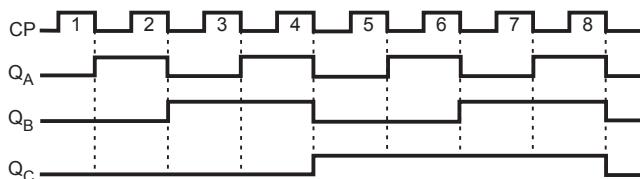


Fig. 6.4.3 (b) Timing diagram for 3-bit synchronous binary counter

CP	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Table 6.4.1 State sequence for 3-bit binary counter

Q_B and Q_A both are at logic 1. This condition is detected by AND gate and applied to the J and K inputs of flip-flop C. Whenever both Q_A and Q_B are HIGH, the output of the AND gate makes the J and K inputs of flip-flop C HIGH and flip-flop C toggles on the following clock pulse. At all other times, the J and K inputs of flip-flop C are held LOW by the AND gate output and flip-flop does not change state.

6.4.3 4-bit Synchronous Binary Up Counter

Fig. 6.4.4 (a) shows logic diagram and timing diagram for 4-bit synchronous binary counter. As HIGH

counter is implemented with negative edge triggered flip-flops, the transitions occur at the negative edge of the clock.

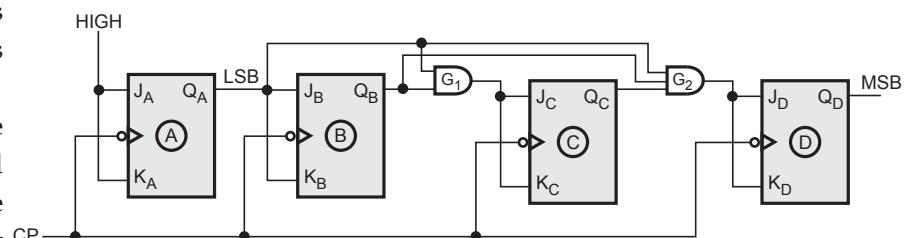


Fig. 6.4.4 (a)

pulse. In this circuit, first three flip-flops work same as 3-bit counter discussed previously.

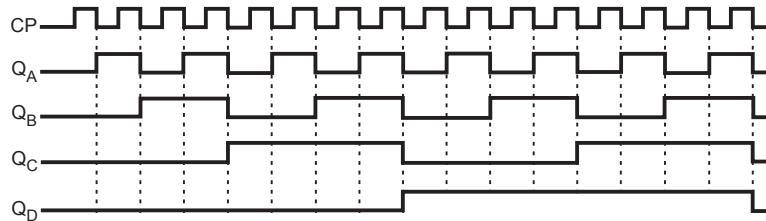


Fig. 6.4.4 (b) A four-bit synchronous binary counter and timing diagram

For the fourth stage, flip-flop has to change the state when $Q_A = Q_B = Q_C = 1$. This condition is decoded by 3-input AND gate G_2 . Therefore, when $Q_A = Q_B = Q_C = 1$, flip-flop D toggles and for all other times it is in no change condition.

Example 6.4.1 Determine f_{max} for the 4-bit synchronous counter if t_{pd} for each flip-flop is 50 ns and t_{pd} for each AND gate is 20 ns. Compare this with f_{max} for a MOD-16 ripple counter.

Solution : For a synchronous counter the total delay that must be allowed between input clock pulses is equal to flip-flop t_{pd} + AND gate t_{pd} . Thus $T_{clock} \geq 50 + 20 = 70$ ns and so the counter has

$$f_{\max} = \frac{1}{70\text{ ns}} = 14.3 \text{ MHz}$$

We know that MOD-16 ripple counter used four flip-flops. With flip-flop $t_{pd} = 50$ ns, the f_{max} for ripple counter can be given as,

$$f_{max}(\text{ripple}) = \frac{1}{4 \times 50 \text{ ns}} = 5 \text{ MHz}$$

6.4.4 Synchronous Down and Up/Down Counters

SPPU : May-10, Marks 10

We have seen that a ripple counter could be made to count down by using the inverted output of each flip-flop to drive the next flip-flops in the counter. A parallel/synchronous down counter can be constructed in a similar manner that is, by using the inverted FF outputs to drive the following JK inputs. For example, the parallel up counter of Fig. 6.4.4 (a) can be converted to a down counter by connecting the \bar{Q}_A , \bar{Q}_B , \bar{Q}_C and \bar{Q}_D outputs in place of Q_A , Q_B , Q_C and Q_D respectively. The counter will then proceed through the following sequence as input pulses are applied :

To form a parallel up/down counter the control input (UP/DOWN) is used to control whether the normal flip-flop outputs or the inverted flip-flop outputs are fed to the J and K inputs of the following flip-flops. The Fig. 6.4.5 shows 3-bit up/down counter that will count from 000 up to 111 when the Up/DOWN control input is 1 and from 111 down to 000 when the Up/DOWN control input is 0.

A logic 1 on the Up/DOWN enables AND gates 1 and 2 and disables AND gates 3 and 4. This allows the Q_A and Q_B outputs through to the J and K inputs of the next flip-flops so that the counter will count up as pulses are applied. When Up/DOWN line is logic 0, AND gates 1 and 2 are disabled and AND gates 3 and 4 are enabled. This allows the \bar{Q}_A and \bar{Q}_B outputs through to the J and K inputs of the next flip-flops so that the counter will count down as pulses are applied.

1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
.	.	.	.
.	.	.	.
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0

Fig. 6.4.5

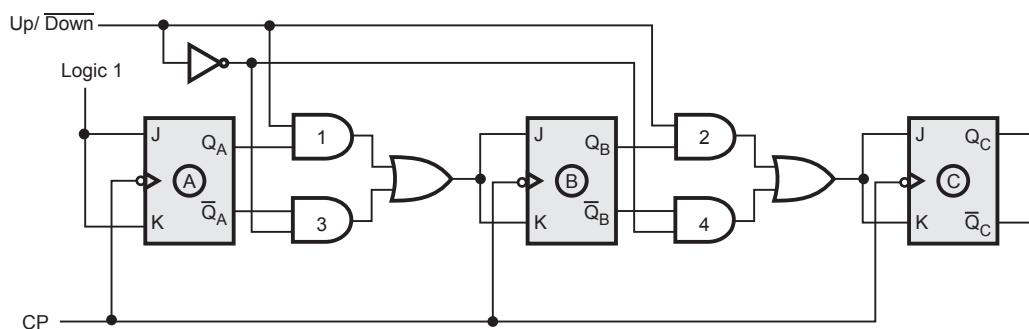


Fig. 6.4.6 3-bit synchronous/parallel up/down counter

Fig. 6.4.7 shows the timing diagram for 3-bit up-down counter.

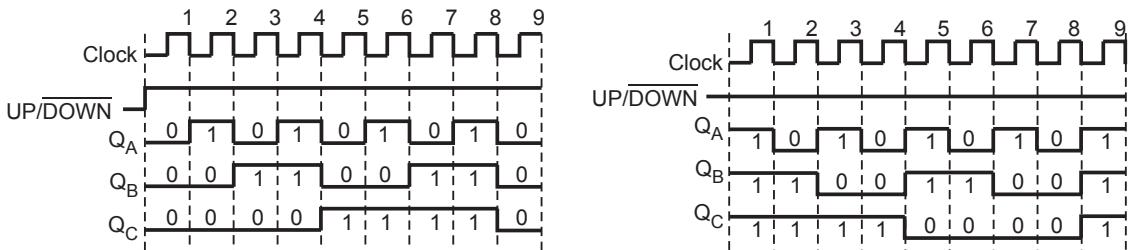


Fig. 6.4.7 Timing diagram

Review Questions

1. What do you mean by ripple counter ? SPPU : May-08, Marks 2
2. Draw and explain 3-bit asynchronous up counter using flip-flops and explain with output waveforms. SPPU : May-07, Dec.-12, Marks 6
3. Draw and explain the working of 3-bit UP/DOWN synchronous counter.
4. Draw a 4-bit synchronous counter. Also explain timing diagram for the same. SPPU : Dec.-10, Marks 10

6.5 Design of Synchronous Counters

SPPU : May-12,14,15,18, Dec.-13, 19

1. Determine the number of flip-flops needed. If n represents number of flip-flops $2^n \geq$ number of states in the counter.
2. Choose the type of flip-flops to be used.
3. Using excitation table for selected flip-flop determine the excitation table for the counter.
4. Use K-map or any other simplification method to derive the flip-flop input functions.
5. Draw the logic diagram.

Example 6.5.1 Design a MOD-5 synchronous counter using JK flip-flops and implement it. Also draw the timing diagram. SPPU : May-14, 15, Marks 6

Solution : **Step 1 :** Determine the number of flip-flop needed

Flip-flops required are

$$2^n \geq N$$

Here $N = 5 \therefore n = 3$ i.e. three flip-flops are required.

Step 2 : Type of flip-flop to be used : JK

Step 3 : Determine the excitation table for the counter.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1

Table 6.5.1 Excitation table for JK flip-flop

Present state		Next state			Flip-flop inputs						
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

Table 6.5.2 Excitation table for counter

Step 4 : K-map simplification

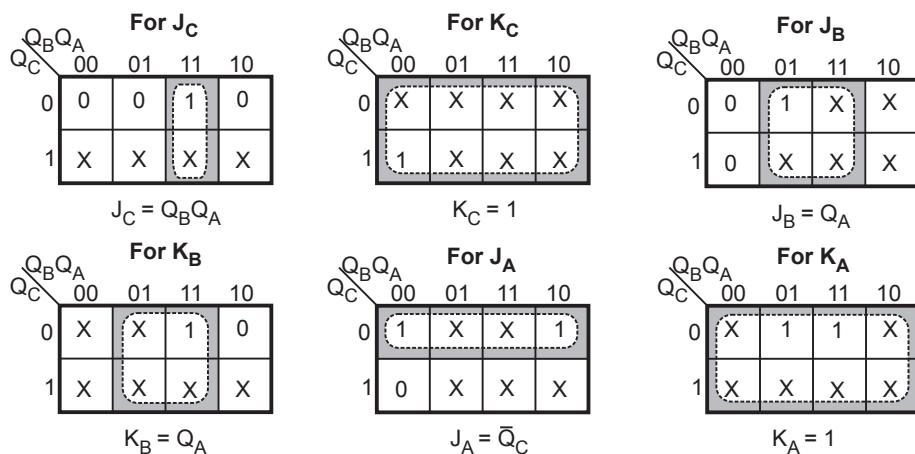


Fig. 6.5.1

Step 5 : Draw the logic diagram

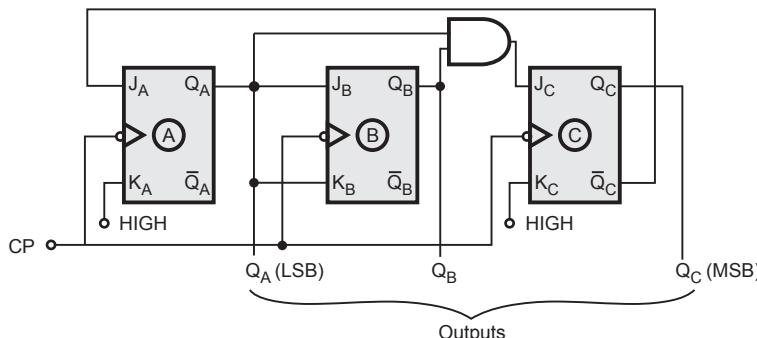


Fig. 6.5.2 (a) MOD-5 synchronous counter

Timing Diagram

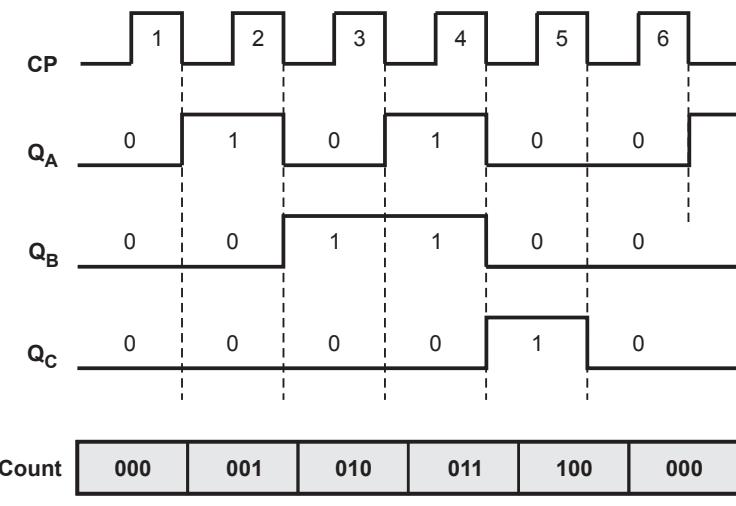


Fig. 6.5.2 (b)

Example 6.5.2 Design divide by 6 counter using T-flip-flops. Write state table and reduce the expression using K-map.

Solution :

Step 1 : Determine the number of flip-flops needed.

For designing mod 6 counter using the formula

$$2^n \geq N$$

Here $N = 6 \therefore n = 3$ i.e. 3 flip-flops are required.

Step 2 : Type of flip-flops to be used : T

Step 3 : Determine the excitation table for counter.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Table 6.5.3 Excitation table for T-flip-flop

CP	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_C	T_B	T_A
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
2	0	1	0	0	1	1	0	0	1
3	0	1	1	1	0	0	1	1	1
4	1	0	0	1	0	1	0	0	1
5	1	0	1	0	0	0	1	0	1

Table 6.5.4 Excitation table for counter

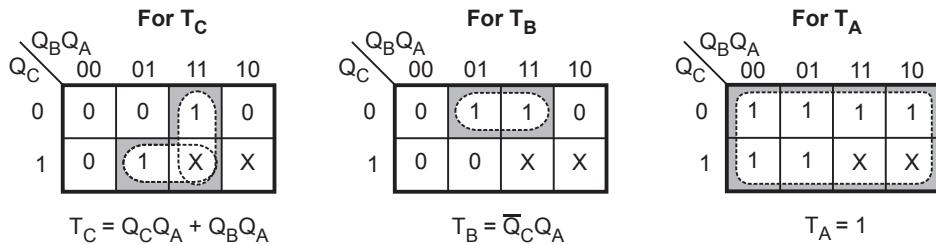
Step 4 : K-map simplification.

Fig. 6.5.3

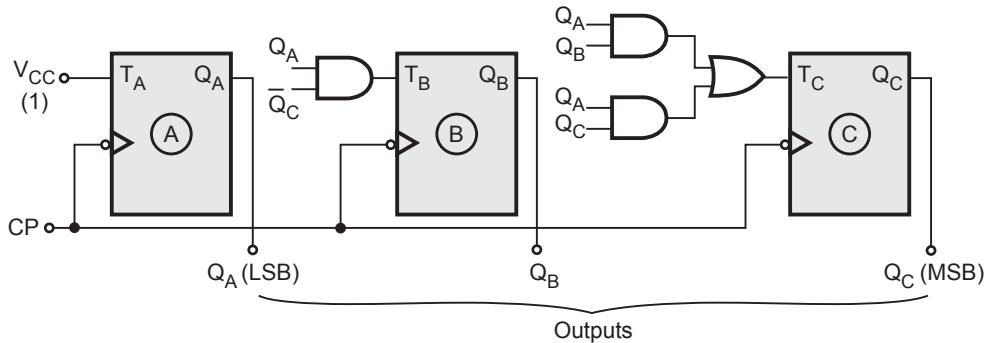
Step 5 : Draw the logic diagram.

Fig. 6.5.4 Logic diagram

Example 6.5.3 Design a synchronous decade counter using D flip-flop.

Solution : The decade counter is a mod-10 counter. It has ten states : 0 - 9.

Step 1 : Determine the number of flip-flops needed.

We know that $2^n \geq N$.
Here, $N = 10 \therefore n = 4$
i.e. 4 flip-flops needed.

Step 2 : Types of flip-flops to be used : D

Step 3 : Determine the excitation table for counter.

Present state				Next state			
Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

Table 6.5.5 Excitation table for counter

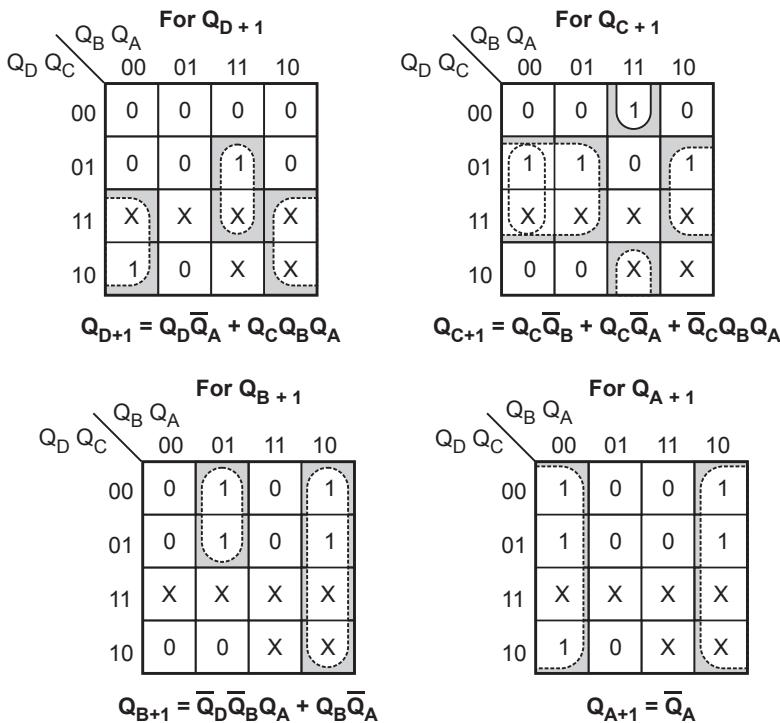
Step 4 : K-map simplification

Fig. 6.5.5

$$\begin{aligned}
 Q_{D+1} &= Q_D \bar{Q}_A + Q_C Q_B Q_A \\
 Q_{D+1} &= Q_D \bar{Q}_A + Q_C Q_B Q_A \\
 Q_{C+1} &= Q_C \bar{Q}_B + Q_C \bar{Q}_A + \bar{Q}_C Q_B Q_A \\
 Q_{B+1} &= \bar{Q}_D \bar{Q}_B Q_A + Q_B \bar{Q}_A \\
 Q_{A+1} &= \bar{Q}_A
 \end{aligned}$$

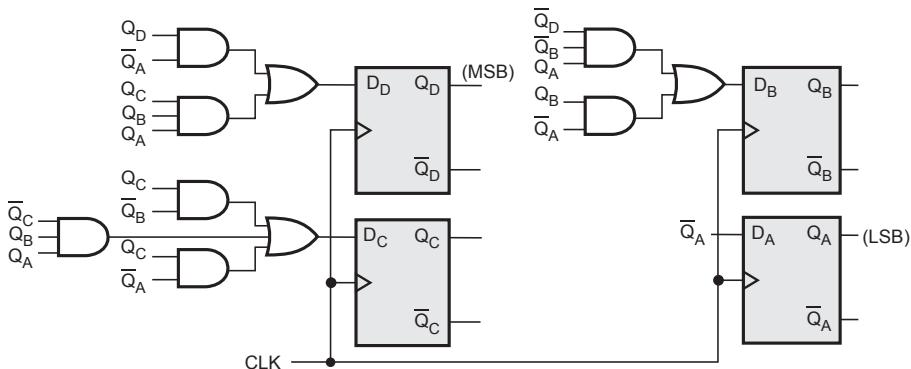
Step 5 : Draw the logic diagram.

Fig. 6.5.6 Logic diagram

Example 6.5.4 Design 3-bit synchronous counter using T flip-flop. **SPPU : May-18, Marks 4**

Solution :

Present state			Next state			Flip-flop inputs		
A	B	C	A^+	B^+	C^+	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

K-map simplification

		For T_A				
		BC	00	01	11	10
A		0	0	0	1	0
1		1	0	0	1	0

$T_A = BC$

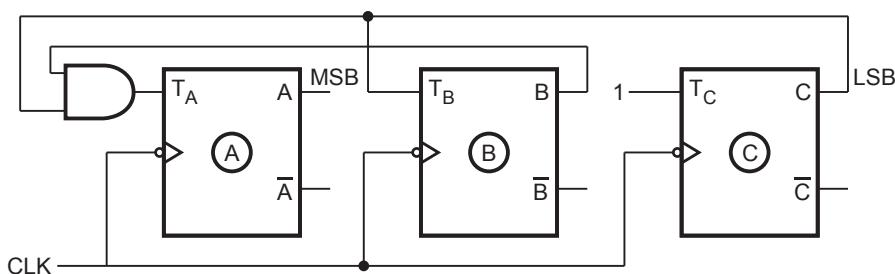
		For T_B				
		BC	00	01	11	10
A		0	0	1	1	0
1		1	0	1	1	0

$T_B = C$

		For T_C				
		BC	00	01	11	10
A		0	1	1	1	1
1		1	1	1	1	1

$T_C = I$

Logic diagram



Example 6.5.5 Design 2 bit synchronous UP counter using MS-JK flip-flop. Draw the circuit diagram.

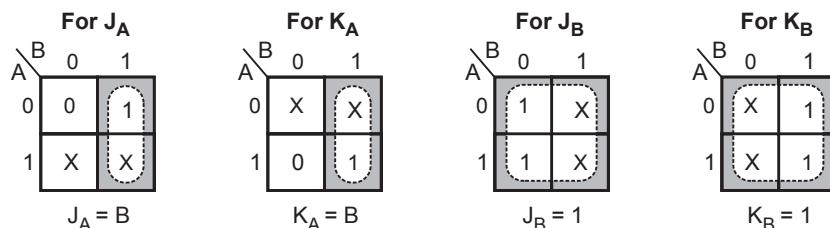
SPPU : Dec.-19, Marks 4

Solution :

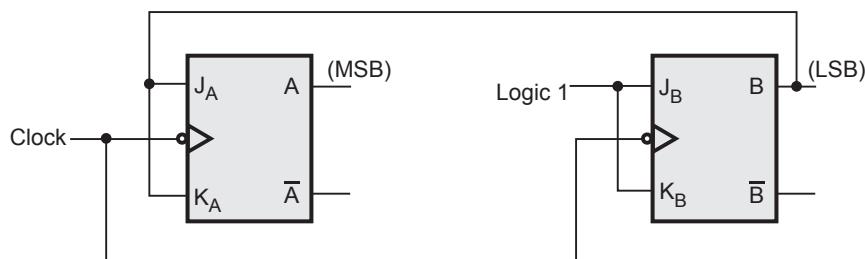
Excitation table :

Present state		Next state		Flip-flop inputs			
A	B	A^+	B^+	J_A	K_A	J_B	K_B
0	0	0	1	0	\times	1	\times
0	1	1	0	1	\times	\times	1
1	0	1	1	\times	0	1	\times
1	1	0	0	\times	1	\times	1

K-map simplification :



Logic diagram :



Examples for Practice

Example 6.5.7 : Design a 3 bit synchronous gray code counter using T flip-flop.

Example 6.5.8 : The following sequence is to be realized by a counter consisting of 3 JK FF's.

A ₁	0	0	0	0	1	1	0
A ₂	0	1	1	0	0	1	0
A ₃	0	1	0	1	1	0	0

Design the counter.

Example 6.5.9 : Design and explain the working of a mod-11 counter.

Example 6.5.10 : Design mod-6 synchronous counter using JK flip-flops and implement it.

Review Questions

1. Explain the steps in design of synchronous counter with the help of example.

2. Design 3-bit synchronous up-counter using MS JK flip-flops.

SPPU : May-12, Marks 6

3. Design Mod-5 synchronous counter using JK FFs.

SPPU : Dec.-13, Marks 4

4. Design a MOD-5 synchronous counter using JK FF and implement it. Also draw timing diagram.

SPPU : May-14, Marks 6

6.6 Lock-Out

SPPU : Dec.-11,15,18, May-13

In a counter if the next state of some unused state is again an unused state and if by chance the counter happens to find itself in the unused states and never arrived at a used state then the counter is said to be in the lockout conditions. This is illustrated in the Fig. 6.6.1. The counter which never goes in lockout condition is called **self starting counter**.

The circuit that goes in lockout condition is called **bushless circuit**.

To make sure that the

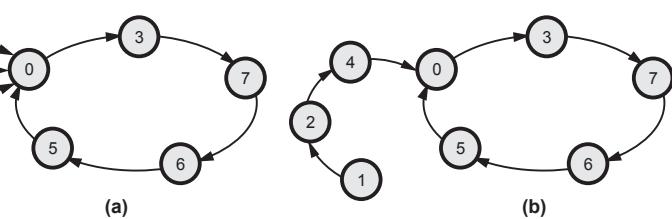
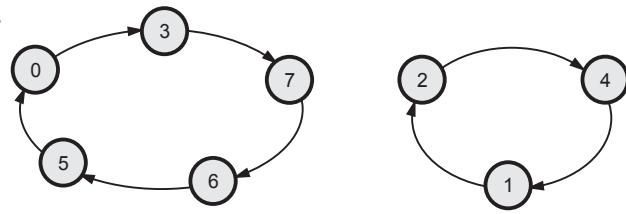


Fig. 6.6.2 State diagram for removing lockout

counter will come to the initial state from any unused state, the additional logic circuit is

necessary. To ensure that the lock out does not occur, the counter should be designed by forcing the next state to be the initial state from the unused states as shown in Fig. 6.6.2.

For example, as shown in Fig. 6.6.2, actually it is not necessary to force all unused states into initial state. Forcing any one state is sufficient. Because if counter initially goes to unused state which is not forced, it will go to another unused state. This will continue until it reaches the forced unused state. Once forced unused state is reached next state is used state, and circuit is lock free circuit. This is illustrated in Fig. 6.6.2 (b).

Example 6.6.1 Design a synchronous counter for

$4 \rightarrow 6 \rightarrow 7 \rightarrow 3 \rightarrow 1 \rightarrow 4 \dots$

Avoid lockout condition. Use JK type design.

SPPU : Dec.-15, Marks 6

Solution : Step 1 : State diagram

Here, states 5, 2 and 0 are forced to go into 6, 3 and 1 state, respectively to avoid lockout condition.

Step 2 : Excitation table

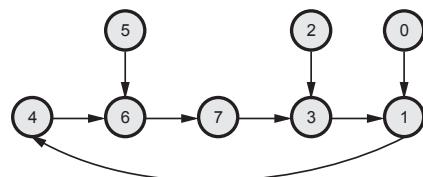


Fig. 6.6.3

Present states			Next states			Flip-flop inputs					
A	B	C	A_{+1}	B_{+1}	C_{+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	1	0	0	1	X	0	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	0	0	1	0	X	X	1	X	0
1	0	0	1	1	0	X	0	1	X	0	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	1	1	X	1	X	0	X	0

Table 6.6.1

Step 3 : K-map simplification

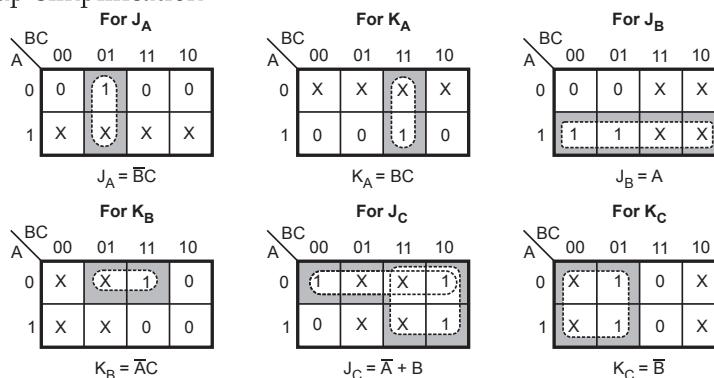


Fig. 6.6.4

Step 4 : Logic diagram

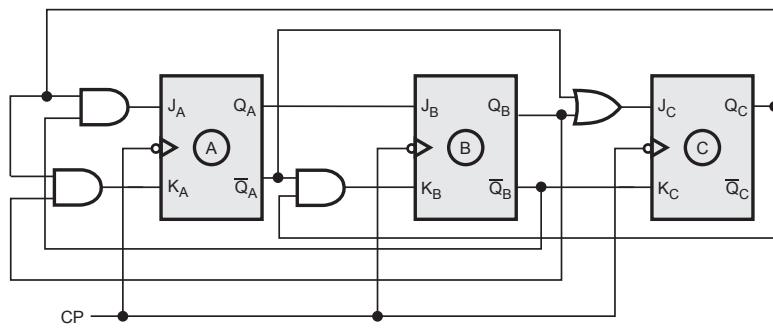


Fig. 6.6.5

Example 6.6.2 Design synchronous counter which will go through the following step, using JK flip-flop. (Avoid lock out condition.).

Solution : The Fig. 6.6.6 shows the state diagram for the given counter. To avoid lock-out condition states 1, 4 and 6 are forced to enter into state 3.

Flip-flop excitation table is as shown below.

Present state			Next state		
A	B	C	A_{+1}	B_{+1}	C_{+1}
0	0	0	1	1	1
0	0	1	0	1	1
0	1	0	1	0	1
0	1	1	0	0	0
1	0	0	0	1	1
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	0	1	0

Table 6.6.2

K-map simplification

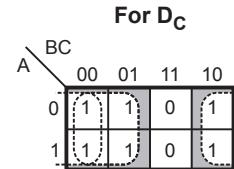
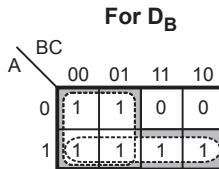
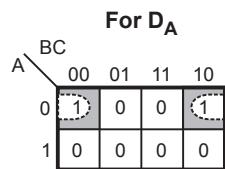


Fig. 6.6.7

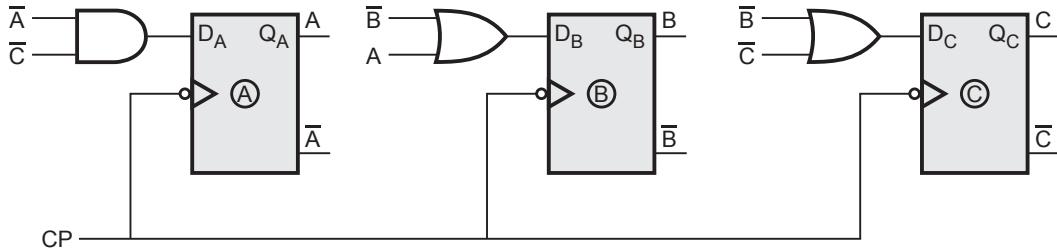
Logic diagram

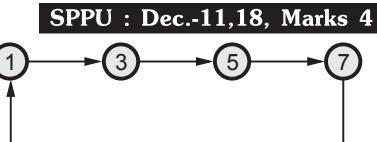
Fig. 6.6.8

Review Questions

1. What is lockout condition ?
2. What is a self starting counter ?
3. How to avoid lockout condition.
4. Design sequence generator using JK FFs. Avoid lockout condition.

SPPU : May-13, Marks 6

SPPU : May-13, Marks 2



SPPU : Dec.-11,18, Marks 4

6.7 IC 7490 (Decade Binary Counter)

SPPU : Dec.-04,05,06,10,11,12,17, May-07,11,12,13,15,17

IC 7490 is a decade binary counter. It consists of four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide by five.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

1. BCD Decade (8421) Counter : The B input must be externally connected to the Q_A output and A input receives the incoming count and a BCD count sequence is produced.

2. Symmetrical Bi-quinary Divide-by-Ten Counter : The Q_D output must be externally connected to the A input. The input count is then applied to the B input and a divide-by-ten square wave is obtained at output Q_A .

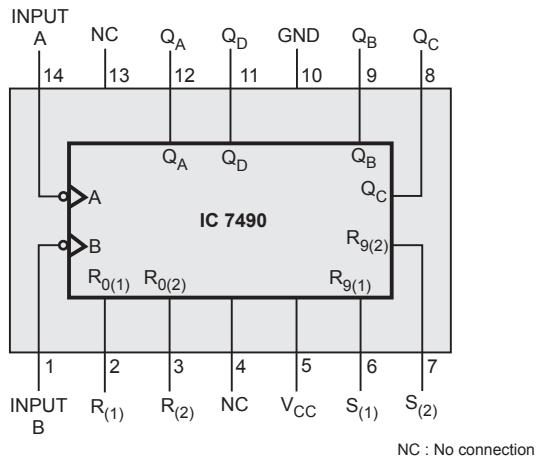


Fig. 6.7.1 Connection diagram for 7490

3. Divide-by-Two and Divide-by-Five Counter : No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (A as the input and Q_A as the output). The B input is used to obtain binary divide-by-five operation at the Q_D output.

Table 6.7.1 shows function tables and Fig. 6.7.2 shows logic diagram for IC7490.

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Table 6.7.1 (a) BCD count sequences
(Note 1)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Table 6.7.1 (b) BCD Bi-quinary (5-2) (Note 2)

Reset Inputs				Outputs			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

Table 6.7.1 (c) Reset/Count function table

H : HIGH Level

L : LOW Level

X : Don't Care

Note 1 : Output Q_A is connected to input B for BCD count.

Note 2 : Output Q_D is connected to input A for bi-quinary count.

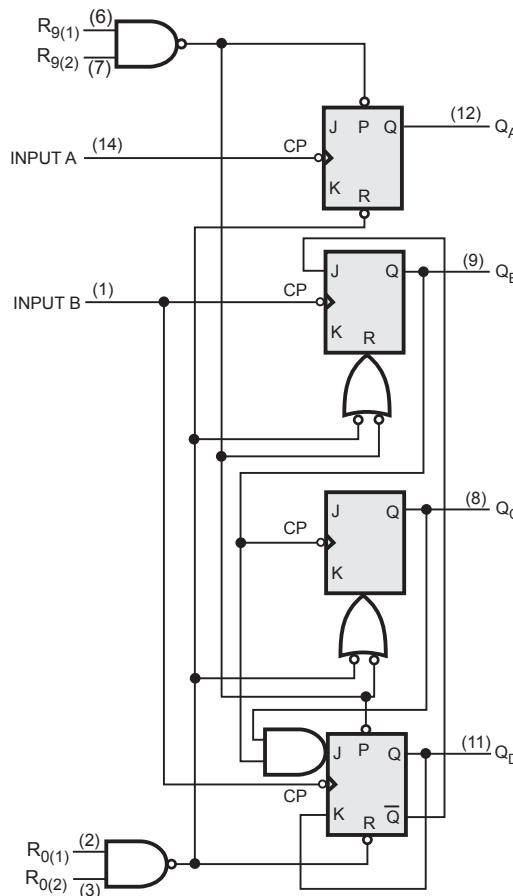


Fig. 6.7.2 Internal block diagram of 7490

Example 6.7.1 Draw basic internal architecture of IC 7490. Design a divide-by-20 counter using IC 7490.

SPPU : May-15, Dec.-11, Marks 8

Solution : Internal structure of 7490 ripple counter IC is as shown in Fig. 6.7.3.

We know that, one IC can work as mod-10 (BCD) counter. Therefore we need two ICs. The counter will go through states 0-19 and should be reset on state 20. i.e.

Q _D	Q _C	Q _B	Q _A	Q _D	Q _C	Q _B	Q _A
0	0	1	0	0	0	0	0

$\underbrace{7490 \ (2)}$ $\underbrace{7490 \ (1)}$

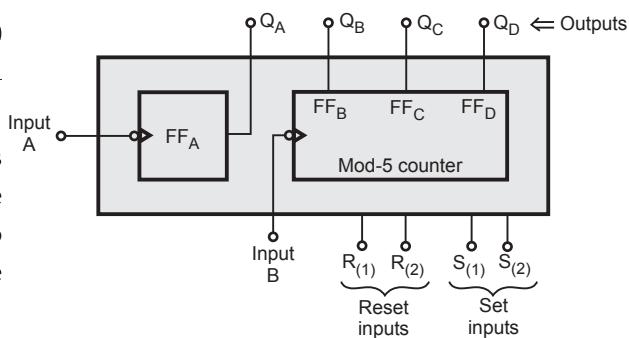


Fig. 6.7.3 Basic internal structure of IC 7490

The diagram of divide-by-20 counter using IC 7490 is as shown in Fig. 6.7.4.

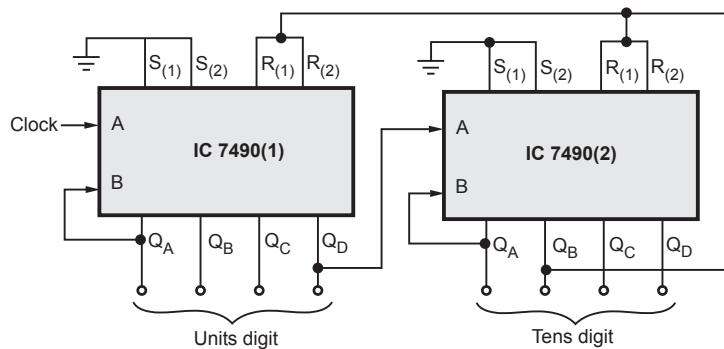


Fig. 6.7.4 Divide-by-20 counter using IC 7490

Example 6.7.2 Design a divide-by-96 counter using 7490 ICs.

SPPU : Dec.-05, Marks 6

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide by 100 counter. To get a divide-by-96 counter, the counter is reset as soon as it becomes 1001 0110. The diagram is shown in Fig. 6.7.5.

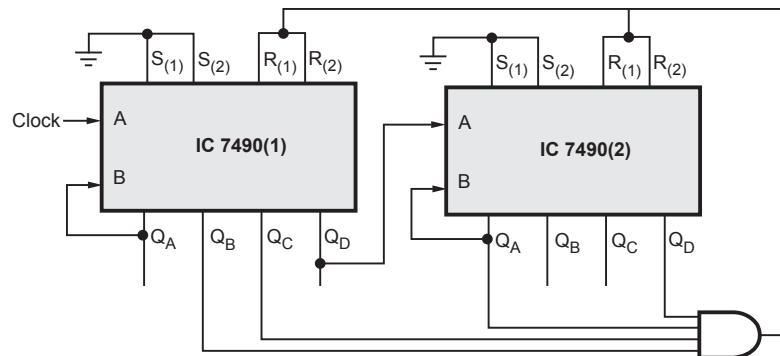


Fig. 6.7.5 Divide-by-96 counter

Example 6.7.3 Design divide-by-93 counter using the same IC.

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide-by-100 counter. To get a divide-by-93 counter, the counter is reset as soon as it becomes 1001 0011. The diagram is shown in the Fig. 6.7.6.

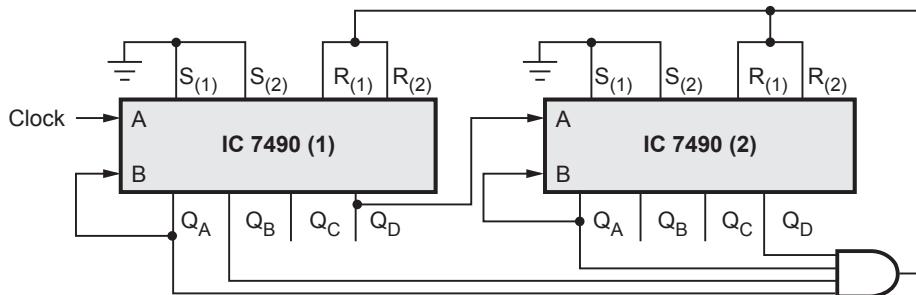


Fig. 6.7.6 Divide-by-93 counter

Example 6.7.4 Design MOD-78 counter using IC 7490.

SPPU : Dec.-06, Marks 6

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide-by-100 counter. To get a divide by 78 or MOD-78 counter, the counter is reset as soon as it becomes 0111 1000 as shown in Fig. 6.7.7.

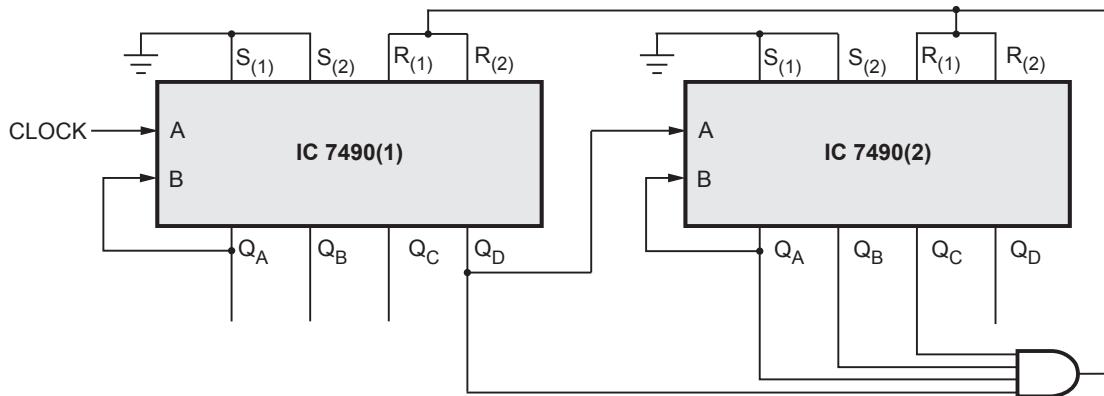


Fig. 6.7.7

Example 6.7.5 Design Mod 8 counter using 7490.

SPPU : May-07, Marks 6

Solution : MOD 8 ripple counter using 7490 :

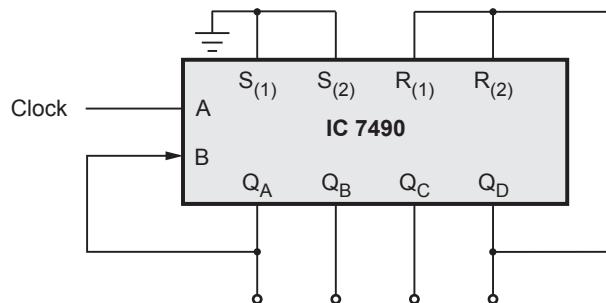


Fig. 6.7.8

Example 6.7.6 In 7490, if Q_D output is connected to A input and pulses at B input. Find count sequence and waveform of output Q_A .

Solution : If the Q_D output is connected to A input of 7490 IC and, input clock is applied to B input divide by ten square wave is obtained at output Q_A .

Clock	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H

4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Table 6.7.2

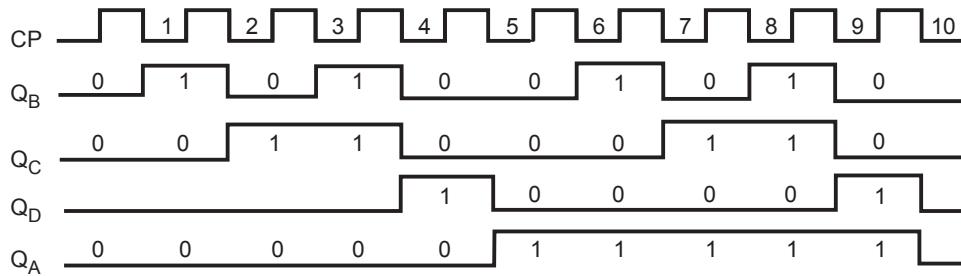


Fig. 6.7.9 Waveforms

Example 6.7.7 Design a mod 25 counter using IC 7490.

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide-by-100 counter. To get a divide-by-25 counter, the counter is reset as soon as it becomes 0010 0101. The diagram is shown in Fig. 6.7.10.

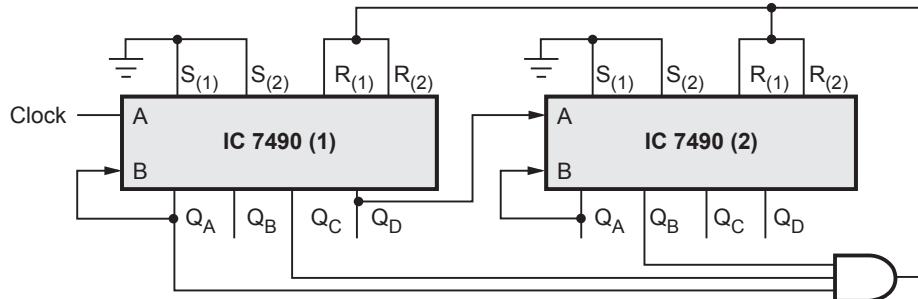


Fig. 6.7.10

Example 6.7.8 Design Mod - 24 counter using 7490.

SPPU : May-17, Marks 2

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide-by-100 counter. To get a divide-by-24 counter, the counter is reset as soon as it becomes 0010 0100. The diagram is shown in Fig. 6.7.11.

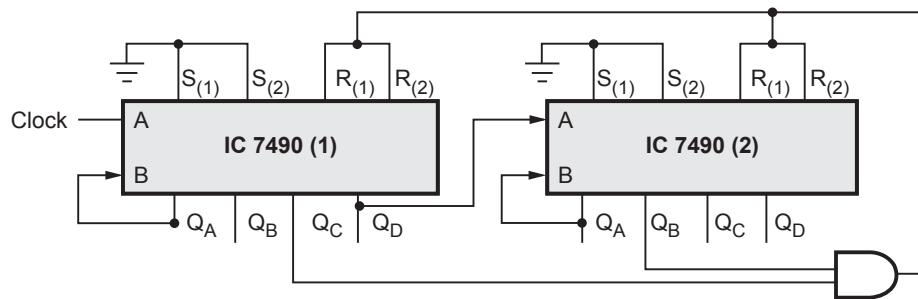


Fig. 6.7.11

Review Questions

1. Draw basic internal architecture of IC 7490 and explain its operation.

SPPU : Dec.-04,11,17, May-13 Marks 4

2. Draw internal block diagram of 7490. Mention how to use it for designing decade-counter.

SPPU : May-07, Marks 4

3. What is advantage of MOD counter ? Explain working of MOD-17 and MOD-24 counter with detail diagram using IC-7490.

SPPU : Dec.-10, Marks 8

4. What is advantage of MOD counter ? Explain working of MOD-27 and MOD-13 counter with detail diagram.

SPPU : May-11, Marks 10

5. Explain the internal diagram of IC 7490. Design MOD 7 and MOD 98 counter using 7490.

SPPU : May-12, Marks 8

6. Design the following using IC7490 :

- i) MOD 97 counter ii) MOD 45 counter.

SPPU : Dec.-12, Marks 8

7. Design MOD 56 counter using IC 7490 & necessary logic gates.

SPPU : May-13, Marks 4

6.8 Ring Counter

SPPU : Dec.-08,10,19, May-11

Fig. 6.8.1 shows the logic diagram for four-bit ring counter. As shown in the Fig. 6.8.1, the Q output of each stage is connected to the D input of the next stage and

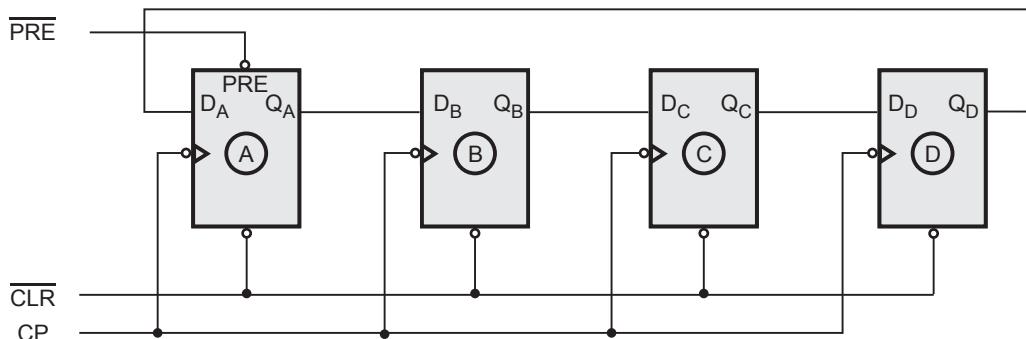


Fig. 6.8.1 Four-bit ring counter

the output of last stage is fed back to the input of first stage. The $\overline{\text{CLR}}$ followed by $\overline{\text{PRE}}$ makes the output of first stage to '1' and remaining outputs are zero, i.e. Q_A is one and Q_B, Q_C, Q_D are zero.

The first clock pulse produces $Q_B = 1$ and remaining outputs are zero. According to the clock pulses applied at the clock input CP, a sequence of four states is produced. These states are listed in Table 6.8.1.

As shown in Table 6.8.1, 1 is always retained in the counter and simply shifted 'around the ring', advancing one stage for each clock pulse. In this case four stages of flip-flops are used. So a sequence of four states is produced and repeated. Fig. 6.8.2 gives the timing sequence for a four-bit ring counter.

The ring counter can be used for counting the number of pulses. The number of pulses counted is read by noting which flip-flop is in state 1. No decoding circuitry is required. Since there is one pulse at the output for each of the N clock pulses, this circuit is also referred to as a divide-by-N-counter or an $N : 1$ scalar. Ring counters can be instructed for any desired MOD number, that is MOD-N ring counter requires N flip-flops.

Clock pulse	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0

Table 6.8.1 Ring counter sequence 4-bits

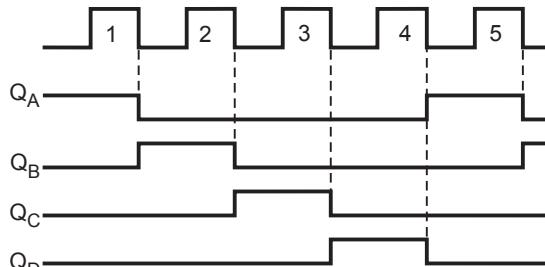


Fig. 6.8.2 Timing sequence for a four-bit ring counter

Review Questions

1. Draw and explain the working of 4-bit ring counter using D flip-flop.

SPPU : Dec.-19, Marks 6

2. Write a short note on ring counter.

SPPU : Dec.-08, Marks 3

3. Explain ring counter with design having initial state '01011', from initial state explain all possible states in that ring.

SPPU : Dec.-10, Marks 10

4. Explain ring counter design for the initial condition '10110' also explain twisted ring counter in brief.

SPPU : May-11, Marks 8

6.9 Johnson or Twisting Ring or Switch Tail Counter

SPPU : Dec.-08,17,18

In a Johnson counter, the Q output of each stage of flip-flop is connected to the D input of the next stage. The single exception is that the complement output of the last flip-flop is connected back to the D-input of the first flip-flop as shown in Fig. 6.9.1.

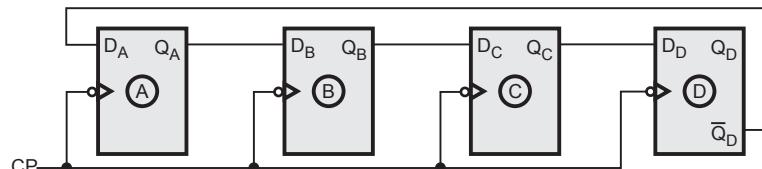


Fig. 6.9.1 Four-bit Johnson counter

Note Johnson counter can be implemented with SR or JK flip-flops as well.

As shown in Fig. 6.9.1 there is a feedback from the rightmost flip-flop complement output to the leftmost flip-flop input. This arrangement produces a unique sequence of states.

Initially, the register (all flip-flops) is cleared. So all the outputs, Q_A, Q_B, Q_C, Q_D are zero. The output of last stage, Q_D is zero. Therefore complement output of last stage, \bar{Q}_D is one. This is connected back to the D input of first stage. So D_A is one. The first falling clock edge produces $Q_A = 1$ and $Q_B = 0, Q_C = 0, Q_D = 0$ since D_B, D_C, D_D are zero. The next clock pulse produces $Q_A = 1, Q_B = 1, Q_C = 0, Q_D = 0$. The sequence of states is summarized in Table 6.9.1. After 8 states the same sequence is repeated.

In this case, four-bit register is used. So the four-bit sequence has a total of eight states. Fig. 6.9.2 gives the timing sequence for a four-bit Johnson counter.

If we design a counter of five-bit sequence, it has a total of ten states, as shown in Table 6.9.2.

Clock pulse	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Table 6.9.1 Four-bit Johnson sequence

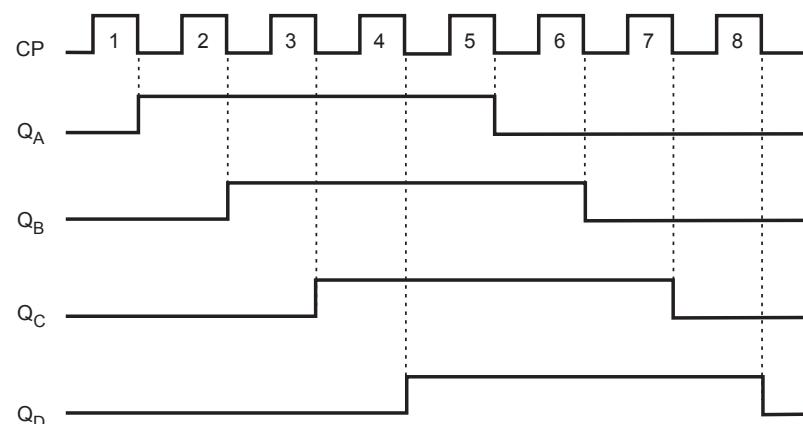


Fig. 6.9.2 Timing sequence for a four-bit Johnson counter

So in general we can say that, an n -stage Johnson counter will produce a modulus of $2 \times n$, where n is the number of stages (i.e. flip-flops) in the counter. Thus, Johnson counter requires only half the number of flip-flops compared to the standard ring counter. However, it requires more flip-flop than binary counter. As shown in tables, the counter will 'fill up' with 1s from left to right and then it will 'fill up' with 0s again. Another advantage of this type of sequence is that it is readily decoded with two input AND gates. Table 6.9.3 gives the count sequence and required decoding.

Clock pulse	Q _A	Q _B	Q _C	Q _D	Q _E
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

Table 6.9.2 Five-bit Johnson sequence

Clock pulse	Q _A	Q _B	Q _C	Q _D	AND Gate required for output
0	0	0	0	0	$\bar{Q}_A \bar{Q}_D$
1	1	0	0	0	$Q_A \bar{Q}_B$
2	1	1	0	0	$Q_B \bar{Q}_C$
3	1	1	1	0	$Q_C \bar{Q}_D$
4	1	1	1	1	$Q_A Q_D$
5	0	1	1	1	$\bar{Q}_A Q_B$
6	0	0	1	1	$\bar{Q}_B Q_C$
7	0	0	0	1	$\bar{Q}_C Q_D$

Table 6.9.3 Count sequence and required decoding

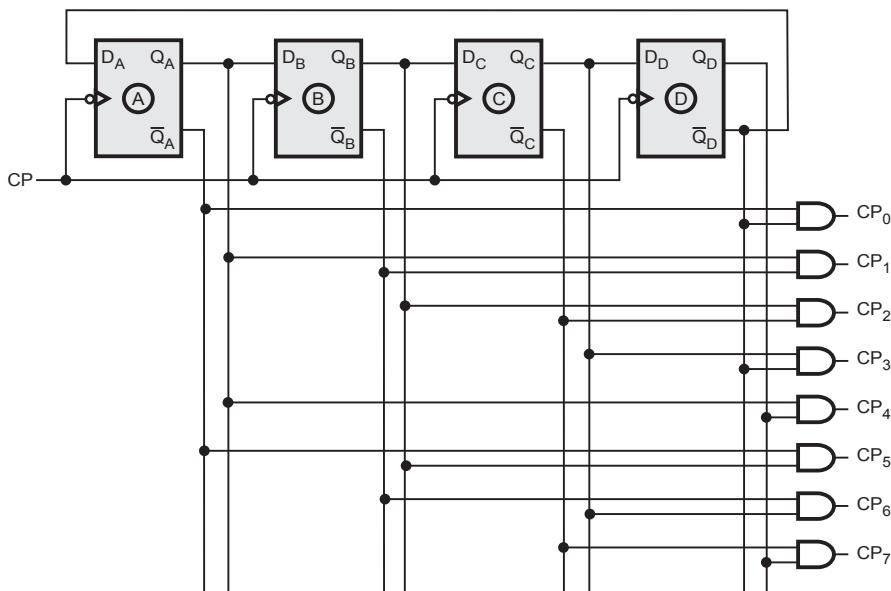


Fig. 6.9.3 Johnson counter with decoder

Example 6.9.1 Draw and explain ring counter using JK flip-flop (timing diagram is expected)

SPPU : Dec.-18, Marks 4

Solution : Fig. 6.9.4 shows the logic diagram for four bit ring counter. As shown in the Fig. 6.9.4, the Q output of each stage is connected to the J input of the next stage and the same signal after inversion connected to the K-input of the next stage. The output of the last stage is fed back to inputs of the first stage. The $\overline{\text{CLR}}$ followed by $\overline{\text{PRE}}$ makes the output of first stage to '1' and remaining outputs are zero, i.e. Q_A is one and Q_B, Q_C, Q_D are zero.

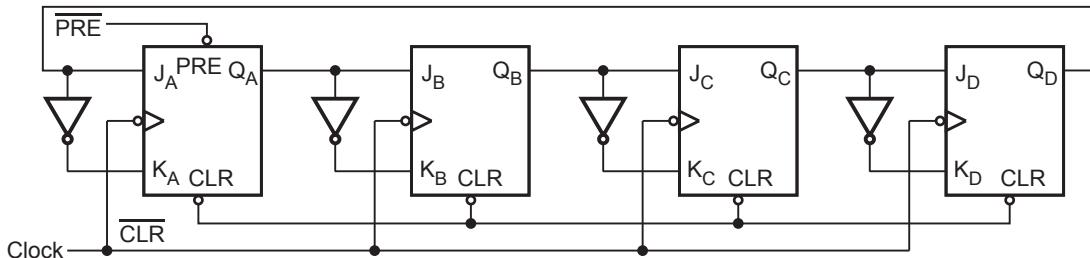


Fig. 6.9.4 Four-bit ring counter

The first clock pulse produces $Q_B = 1$ and remaining outputs are zero. According to the clock pulses applied at the clock input CP, a sequence of four states is produced. These states are listed in Table 6.9.4.

Clock pulse	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0

Table 6.9.4

As shown in Table 6.9.4, 1 is always retained in the counter and simply shifted 'around the ring', advancing one stage for each clock pulse. In this case four stages of flip-flops are used. So a sequence of four states is produced and repeated. Fig. 6.9.5 gives the timing sequence for a four-bit ring counter.

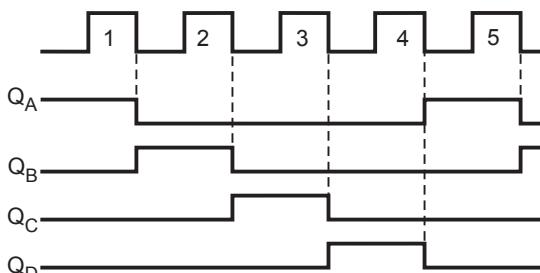


Fig. 6.9.5 Timing sequence for a four-bit ring counter

Review Questions

1. *What is the difference between ring counter and Johnson's counter ?*
2. *Draw the neat circuit diagram of 3-bit Johnson's counter. Draw the relevant output waveforms.*
3. *Write a short note on Johnson's counter.*

SPPU : Dec.-08,17, Marks 3

Notes

UNIT - III

7

Synchronous Sequential Circuit Design

Syllabus

Models-Moore and Mealy, State diagram and State Table, Design Procedure, Sequence generator and detector.

Contents

7.1	<i>Clocked Sequential Circuits</i>	May-10,12,13,	
	Dec.-10,12,16	Marks 4
7.2	<i>Design of Clocked Sequential Circuits</i>	Dec.-05,07,08,10,12,13,14,	
	May-05,06,11,12,13,	Marks 10
7.3	<i>Sequence Generator</i>	May-2000,02,06,08,12,18,	
	Dec.-06,07,08,12,13	Marks 8
7.4	<i>Sequence Detector</i>	May-06,07,10,12,13,14,	
	Dec.-05,06,07,08,10,12,13,	
	15,16,	Marks 12

7.1 Clocked Sequential Circuits

SPPU : May-10,12,13, Dec.-10,12,16

In synchronous or clocked sequential circuits, clocked flip-flops are used as memory elements, which change their individual states in synchronism with the periodic clock signal. Therefore, the change in states of flip-flops and change in state of the entire circuit occurs at the transition of the clock signal. The states of the output of the flip-flop in the sequential circuit gives the state of the sequential circuit.

Present state : The status of all state variables, at some time t , before the next clock edge, represents condition called **present state**.

Next state : The status of all state variables, at some time, $t + 1$, represents a condition called **next state**.

The synchronous or clocked sequential circuits are represented by two models.

- **Moore model** : The output depends only on the present state of the flip-flops.
- **Mealy model** : The output depends on both the present state of the flip-flop(s) and on the input (s).

7.1.1 Moore Model

As mentioned earlier, when the output of the sequential circuit depends only on the present state of the flip-flop, the sequential circuit is referred to as **Moore model**. Let us see one example of Moore model.

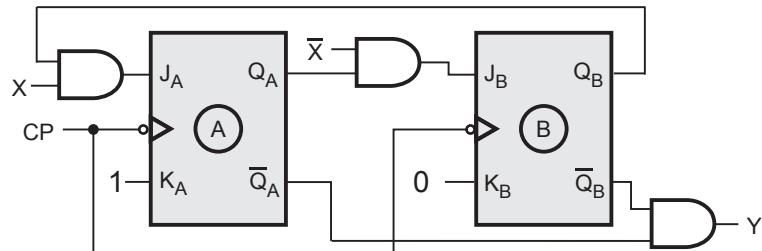


Fig. 7.1.1 Example of Moore model

Fig. 7.1.1 shows a sequential circuit which consists of two JK flip-flops and AND gate. The circuit has one input X and one output Y.

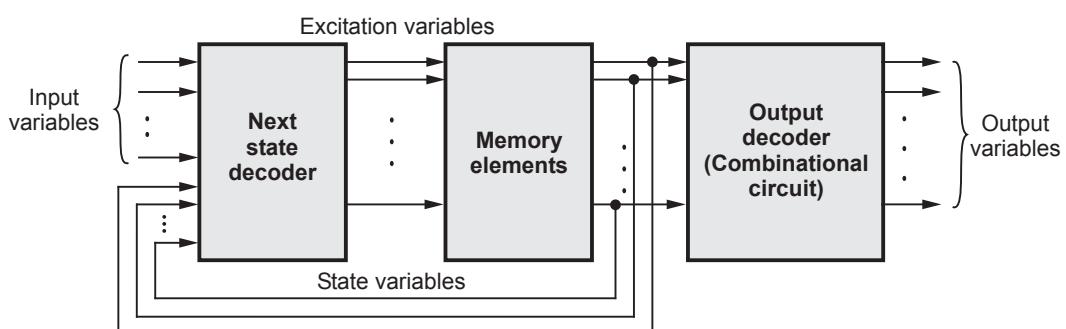


Fig. 7.1.2 Moore circuit model with an output decoder

As shown in the Fig. 7.1.1, input is used to determine the inputs of the flip-flops. It is not used to determine the output. The output is derived using only present states of the flip-flops or combination of it (in this case $Y = Q_A Q_B$).

In general form the Moore model can be represented with its block schematic as shown in Fig. 7.1.2.

7.1.2 Mealy Model

When the output of the sequential circuit depends on both the present state of flip-flop(s) and on the input(s), the sequential circuit is referred to as **Mealy model**. Fig. 7.1.3 shows the sample Mealy model. As shown in the Fig. 7.1.3, the output of the circuit is derived from the combination of present state of flip-flops and input (s) of the circuit.

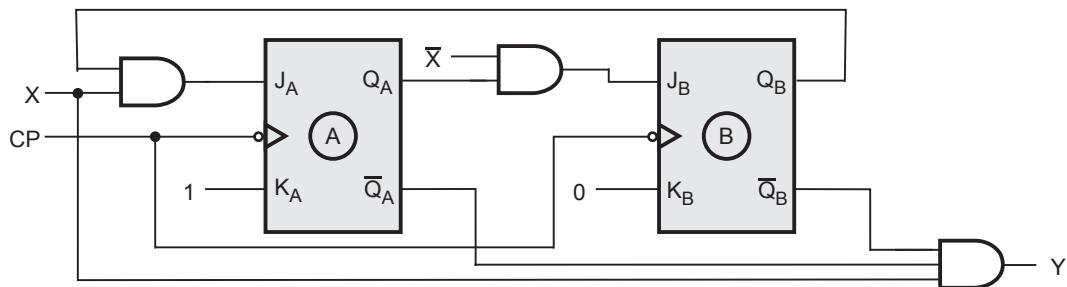


Fig. 7.1.3 Example of Mealy model

Looking at Fig. 7.1.3, we can easily realize that, changes in the input within the clock pulses can not affect the state of the flip-flop. However, they can affect the output of the circuit. Due to this, if the input variations are not synchronized with the clock, the derived output will also not be synchronized with the clock and we get false output (as it is a synchronous sequential circuit). The false outputs can be eliminated by allowing input to change only at the active transition of the clock (in our example HIGH-to-LOW). In general form the Mealy model can be represented with its block schematic as shown in Fig. 7.1.4.

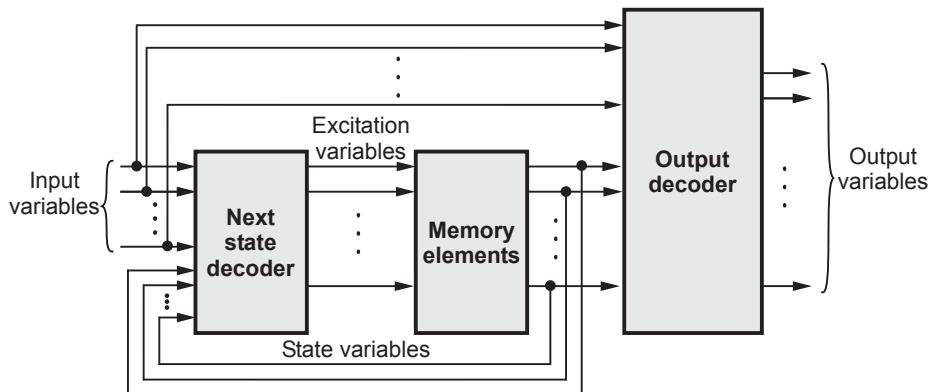


Fig. 7.1.4 Mealy circuit model

7.1.3 Moore vs Mealy Circuit Models

Sr. No.	Moore model	Mealy model
1.	Its output is a function of present state only.	Its output is a function of present state as well as present input.
2.	Input changes does not affect the output.	Input changes may affect the output of the circuit.
3.	Moore model requires more number of states for implementing same function.	It requires less number of states for implementing same function.

Table 7.1.1

7.1.4 Representations of Sequential Circuits

7.1.4.1 State Diagram

State diagram is a pictorial representation of a behaviour of a sequential circuit. Fig. 7.1.5 shows a state diagram. The state is represented by the circle, and the transition between states is indicated by directed lines connecting the circles. A directed line connecting a circle with itself indicates that next state is same as present state. The binary number inside each circle identifies the state represented by the circle. The directed lines are labelled with two binary numbers separated by a symbol '/'. The input value that causes the state transition is labelled first and the output value during the present state is labelled after the symbol '/'.

In case of Moore circuit, the directed lines are labelled with only one binary number representing the state of the input that causes the state transition. The output state is indicated within the circle, below the present state because output state depends only on present state and not on the input. Fig. 7.1.6 shows the state diagram for Moore circuit.

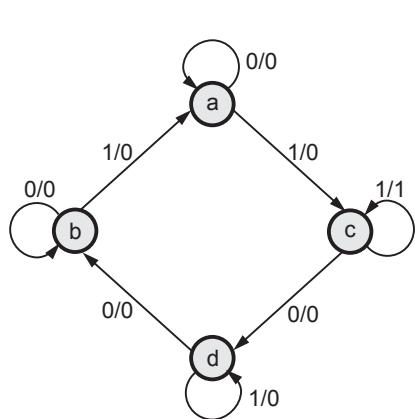


Fig. 7.1.5 State diagram for Mealy circuit

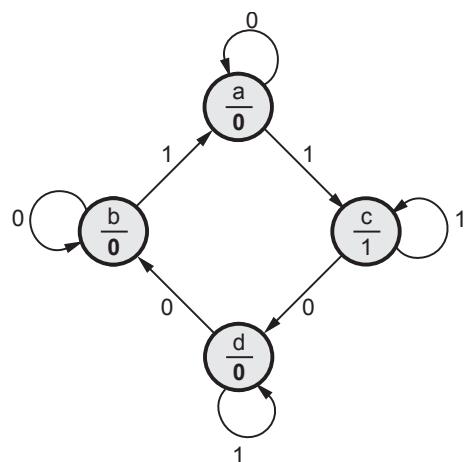


Fig. 7.1.6 State diagram for Moore circuit

7.1.4.2 State Table

Although the state diagram provides a description of the behaviour of a sequential circuit that is easy to understand, to proceed with the implementation of the circuit, it is convenient to translate the information contained in the state diagram into a tabular form called **state synthesis table** or simply **state table**. Table 7.1.2 (a) shows the state table for the state diagram shown in Fig. 7.1.5. It represents relationship between input, output and flip-flop states. It consists of three sections labeled present state, next state, and output. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state is state of the flip-flop after the application of a clock pulse, and the output section gives the values of the output variables during the present state. Both the next state and output sections have two columns representing two possible input conditions : $X = 0$ and $X = 1$.

Present state	Next state		Output	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
AB	AB	AB	Y	Y
a	a	c	0	0
b	b	a	0	0
c	d	c	0	1
d	b	d	0	0

Table 7.1.2 (a)

Present state	Next state		Output
	$X = 0$	$X = 1$	
AB	AB	AB	
a	a	c	0
b	b	a	0
c	d	c	1

Table 7.1.2 (b)

In case of Moore circuit the output section has only one column since output does not depend on input. The Table 7.2.2 (b) shows the state table for Moore circuit whose state diagram is shown in Fig. 7.1.6.

7.1.4.3 Transition Table

A transition table takes the state table one step further. The state diagram and state table represent state using symbols or names. In the transition table specific state variable values are assigned to each state. Assignment of values to state variables is called **State assignment**. Like state table transition table also represents relationship between input, output and flip-flop states. The Fig. 7.1.7 shows the transition table.

Present state	Next state		Output	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
A B	AB	AB	Y	Y
0 0	0 0	1 0	0	1
0 1	1 1	0 0	0	0
1 0	1 0	0 1	1	0
1 1	0 0	1 0	1	0

Fig. 7.1.7

Here, AB are the state variables. The AB = 00 represents one state, AB = 01 represents second state and so on.

Example 7.1.1 What does the word 'Finite' signify in the terms finite state machine ? State advantages and disadvantages of a finite state machine. SPPU : May-10, Marks 4

Solution : The word 'Finite' signifies a finite or limited number of possible states in the terms finite state machine (FSM).

Advantages of finite state machine

- Simple to understand
- Predictable for given a set of inputs and a known current state, the state transition can be predicted, allowing for easy testing.
- Due to their simplicity, FSMs are quick to design, quick to implement and quick in execution.
- FSMs are relatively flexible.
- Easy to transfer from a meaningful abstract representation to a coded implementation.

Disadvantages of FSM

- The predictable nature of deterministic FSMs can be unwanted in some domains such as computer games.
- Larger systems implemented using a FSM can be difficult to manage and maintain.
- Not suited to all problem domains, should only be used when a systems behavior can be decomposed into separate states, transitions and conditions need to be known up front and be well defined.
- The conditions for state transitions are ridged, meaning they are fixed.

Review Questions

1. What is a state ?
2. Define present state and next state.
3. Draw and explain the block diagram of Moore model.
4. What is Moore machine ?
5. Draw and explain the block diagram of Mealy model.
6. What is a Mealy machine ? Give an example.
7. Compare Moore and Mealy circuits.
8. Explain state table.
9. Explain state diagram.
10. What is transition table ?

SPPU : Dec.-10, Marks 4

SPPU : May-12, Dec.-16, Marks 4

SPPU : Dec.-10, 12, May-12, Marks 4

SPPU : Dec.-12, May-13, Marks 2

SPPU : Dec.-12, May-13, Marks 2

7.2 Design of Clocked Sequential Circuits

SPPU : Dec.-05,07,08,10,12,13,14, May-05,06,11,12,13

The recommended steps for the design of a clocked synchronous sequential circuit are as follows :

1. It is necessary to first obtain the state table from the given circuit information such as a state diagram, a timing-diagram, or other pertinent information.
2. The number of states may be reduced by state reduction technique if the sequential circuit can be categorized by input-output relationships independent of the number of states.
3. Assign binary values to each state in the state table.
4. Determine the number of flip-flops needed and assign a letter symbol to each.
5. Choose the type of flip-flop to be used.
6. From the state table, derive the circuit excitation and output tables.
7. Using the K-map or any other simplification method, derive the circuit output functions and the flip-flop input functions.
8. Draw the logic diagram.

Let us see the details of various steps involved in the design of clocked sequential circuits.

7.2.1 State Reduction

The state reduction technique basically avoids the introduction of redundant states. The reduction in redundant states reduce the number of required flip-flops and logic gates, reducing the cost of the final circuit. The two states are said to be redundant or equivalent, if every possible set of inputs generate exactly same output and same next state. When two states are equivalent, one of them can be removed without altering the input-output relationship.

Let us illustrate the state reduction technique with an example. We start with a sequential circuit whose specification is given in the state diagram of Fig. 7.2.1. As shown in the diagram, the states are denoted by letter symbols instead of their binary values, because in state reduction technique internal states are not important; but only input-output sequences are important.

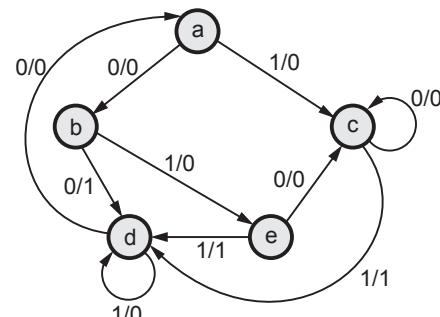


Fig. 7.2.1 State diagram

Step 1 : Determine the state table for given state diagram

Table 7.2.1 shows the state table for given state diagram

Present state	Next state		Output	
	X = 0	X = 1	X = 0	X = 1
a	b	c	0	0
b	d	e	1	0
c	c	d	0	1
d	a	d	0	0
e	c	d	0	1

Table 7.2.1 State table

Step 2 : Find equivalent states

As mentioned earlier, in equivalent states every possible set of inputs generate exactly same output and same next state. In the given circuit there are two input combinations : $X = 0$ and $X = 1$. Looking at the state table for two present states that go to the same next state and have the same output for both input combinations, we can easily find that states c and e are equivalent. This is because, c and e both states go to states c and d and have outputs of 0 and 1 for $X = 0$ and $X = 1$, respectively. Therefore, state e can be removed and replaced by c. The final reduced table is shown in Table 7.2.2. The state diagram for the reduced table consists of only four states and is shown in Fig. 7.2.2.

Present state	Next state		Output	
	X = 0	X = 1	X = 0	X = 1
a	b	c	0	0
b	d	c	1	0
c	c	d	0	1
d	a	d	0	0

Table 7.2.2 Reduced state table

Examples for Understanding

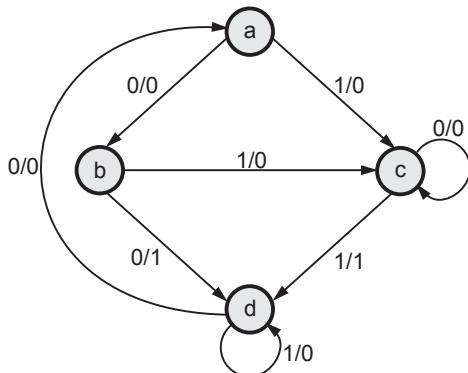


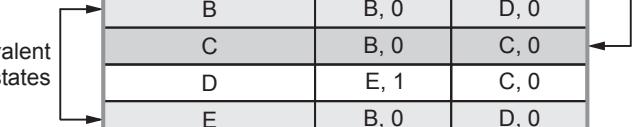
Fig. 7.2.2 Reduced state diagram

Example 7.2.1 Minimize the state table shown given below.

Present state	Next state, Z (Output)	
	X (Input)	
	0	1
A	B,0	C,0

<i>B</i>	<i>B,0</i>	<i>D,0</i>
<i>C</i>	<i>B,0</i>	<i>C,0</i>
<i>D</i>	<i>E,1</i>	<i>C,0</i>
<i>E</i>	<i>B,0</i>	<i>D,0</i>

Solution : Step 1 : Find equivalent states. The Table 7.2.3 shows the equivalent states in the given state table. The states A and C, and states B and E generate exactly same output and same next state. Hence, state A and C are equivalent and similarly states B and E are equivalent.



Present state	Next state, Z(output)	
	X = 0	X = 1
A	B, 0	C, 0
B	B, 0	D, 0
C	B, 0	C, 0
D	E, 1	C, 0
E	B, 0	D, 0

Table 7.2.3 Equivalent states

Step 2 : Replace redundant states with equivalent states.

∴ Replace C by A and replace E by B, and remove states C and E.

Now, there are no equivalent states and hence Table 7.2.3 (a) shows the minimized state table.

Present state	Next state, Z (output)	
	X = 0	X = 1
A	B, 0	A, 0
B	B, 0	D, 0
D	B, 1	A, 0

Table 7.2.3 (a) Minimized state table

Example 7.2.2 Minimize the state table shown given below :

Present state	Next state, Z (Output)	
	X (Input)	
	0	1
A	A, 0	B, 0
B	C, 0	D, 0
C	A, 0	D, 0
D	E, 0	F, 1
E	A, 0	F, 1
F	G, 0	F, 1
G	A, 0	F, 1

Solution : Step 1 : Find equivalent states

Step 2 : Replace redundant state with equivalent state.

Therefore, replace G by E and remove state G. Looking at Table 7.2.4 (b), we find that states D and F are equivalent. Therefore, replace F by D and remove state F. Now, there are no equivalent states and hence Table 7.2.4 (c) shows the minimized state table.

Present state	Next state, Z(output)	
	X = 0	X = 1
A	A, 0	B, 0
B	C, 0	D, 0
C	A, 0	D, 0
D	E, 0	F, 1
E	A, 0	F, 1
F	G, 0	F, 1
G	A, 0	F, 1

Equivalent states

Table 7.2.4 (a) Equivalent states

Present state	Next state, Z(output)	
	X = 0	X = 1
A	A, 0	B, 0
B	C, 0	D, 0
C	A, 0	D, 0
D	E, 0	F, 1
E	A, 0	F, 1
F	E, 0	F, 1

Equivalent states

Table 7.2.4 (b) Equivalent states

Present state	Next state, Z (Output)	
	X = 0	X = 1
A	A, 0	B, 0
B	C, 0	D, 0
C	A, 0	D, 0
D	E, 0	D, 1
E	A, 0	D, 1

Table 7.2.4 (c) Minimized state table

7.2.2 State Assignment

SPPU : Dec.-13

In sequential circuits we know that the behaviour of the circuit is defined in terms of its inputs, present states, next states and outputs. To generate desired next state at particular present state and inputs, it is necessary to have specific flip-flop inputs. These flip-flop inputs are described by a set of Boolean functions called flip-flop input functions. To determine the flip-flop input functions, it is necessary to represent states in the state diagram using binary values instead of alphabets. This procedure is known as state assignment. We must assign binary values to the states in such a way that it is possible to implement flip-flop input

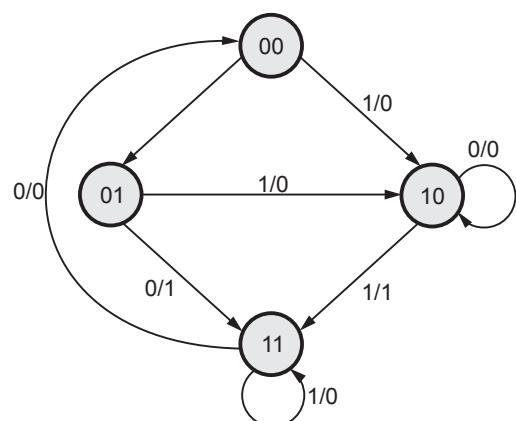


Fig. 7.2.3 State diagram with binary states

functions using minimum logic gates. Fig. 7.2.3 shows the state diagram shown in Fig. 7.2.3 after state assignments.

Rules for state assignments

There are two basic rules for making state assignments.

Rule 1 : States having the **same** NEXT STATES for a given input condition should have assignments which can be grouped into logically adjacent cells in a K-map.

Fig. 7.2.3 shows the example for Rule 1. As shown in the Fig. 7.2.4, there are four states whose next state is same. Thus states assignments for these states are 100, 101, 110 and 111 which can be grouped into logically adjacent cells in a K-map.

Rule 2 : States that are the NEXT STATES of a single state should have assignment which can be grouped into logically adjacent cells in a K-map.

Fig. 7.2.5 shows the example for Rule 2. As shown in the Fig. 7.2.5, for state 000, there are four next states. These states are assigned as 100, 101, 110 and 111 so that they can be grouped into logically adjacent cells in a K-map and table shows the state table with assigned states.

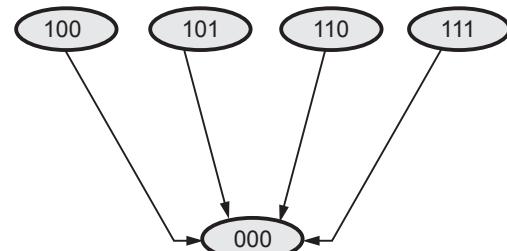


Fig. 7.2.4 Example of using Rule 1

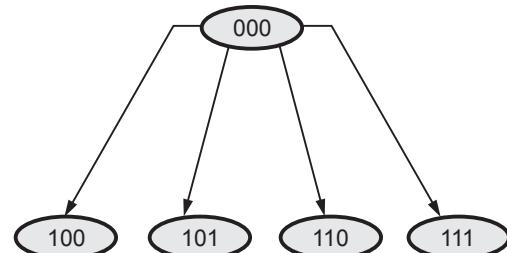


Fig. 7.2.5 Example of using Rule 2

Present state	Next state		Output	
	X = 0	X = 1	X = 0	X = 1
00	01	10	0	0
01	11	10	1	0
10	10	11	0	1
11	00	11	0	0

Table 7.2.5 State table with assigned states

7.2.3 Choice of Flip-Flops and Derivation of Next State and Output

From the state assigned state table shown in Table 7.2.5, we can derive the logic expression for the next state and output functions. But first we have to decide on the type of flip-flops that will be used in the circuit. The most straightforward choice is to use D flip-flops, because in this case the values of next state are simply clocked into the flip-flops to become the new values of present state. For other types of flip-flops, such as JK, T and RS the relationship between the next-state variable and inputs to a flip-flop is not as straightforward as D flip-flop. For other types of flip-flops we have to refer excitation table of flip-flop to find flip-flop inputs. This is illustrated in the following example.

Example 7.2.3 A sequential circuit has one input and one output. The state diagram is shown in Fig. 7.2.6. Design the sequential circuit with a) D flip-flops b) T flip-flops c) RS flip-flops and d) JK- flip-flops.

Solution : The state table for the state diagram shown in Fig. 7.2.6 is as given in Table 7.2.6.

As seen from the state table there are no equivalent states. Therefore, no reduction is the state diagram. The state table shows that circuit goes through four states, therefore we require 2 flip-flops (number of states = 2^m , where m = number of flip-flops). Since two flip-flops are required first is denoted as A and second is denoted as B.

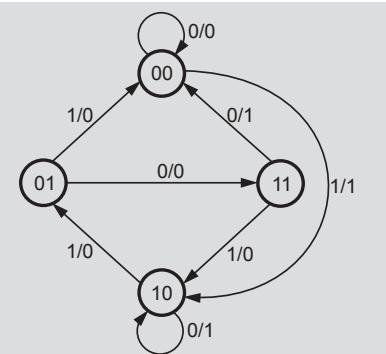


Fig. 7.2.6

1. Design using D flip-flops

As mentioned earlier, for D flip-flops next states are nothing but the new present states. Thus, we can directly use next states to determine the flip-flop input with the help of K-map simplification.

Present state		Next state		Output	
		X = 0	X = 1	X = 0	X = 1
A	B	AB	AB	Y	Y
0	0	0 0	1 0	0	1
0	1	1 1	0 0	0	0
1	0	1 0	0 1	1	0
1	1	0 0	1 0	1	0

Table 7.2.6

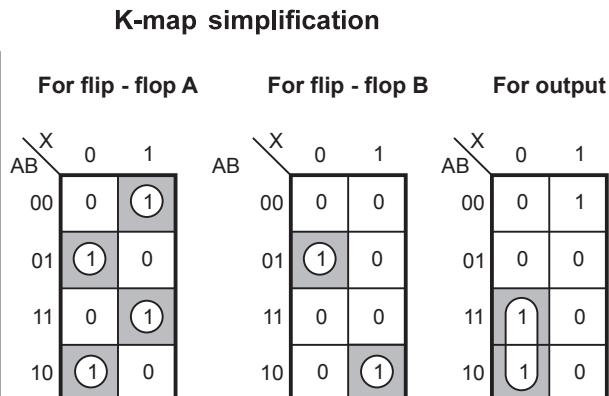


Fig. 7.2.7

$$D_A = \overline{A} \overline{B} X + \overline{A} \overline{B} \overline{X} + A B X + A \overline{B} \overline{X} \quad \text{and}$$

$$D_B = \overline{A} B \overline{X} + A \overline{B} X$$

$$Y = \overline{A} \overline{B} X + A \overline{X}$$

With these flip-flop input functions and circuit output function we can draw the logic diagram. (See Fig. 7.2.8 on next page)

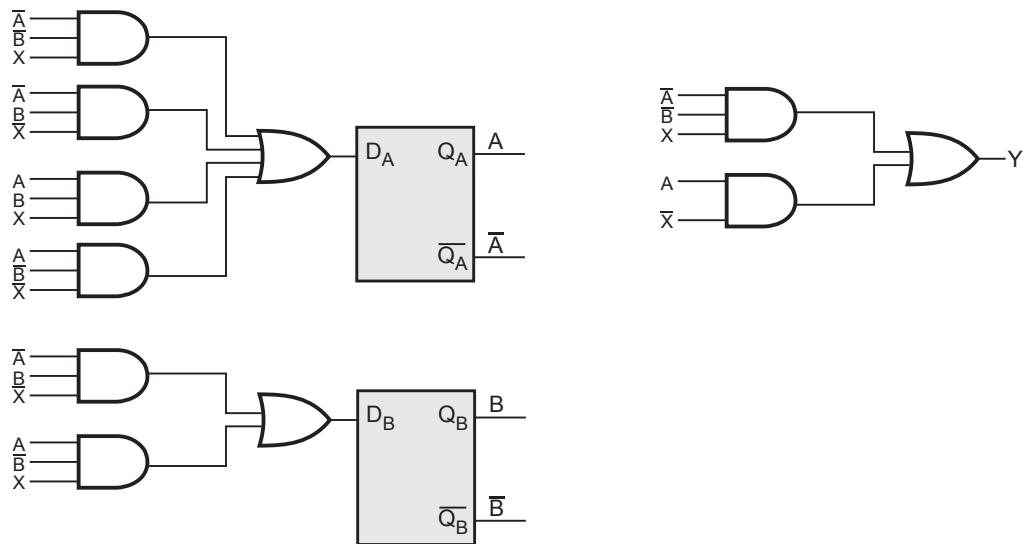


Fig. 7.2.8 Logic diagram of given sequential circuit using D flip-flop

2. Design using T flip-flops

Using the excitation table for T flip-flop shown in Table 7.2.7 we can determine the excitation table for the given circuit as shown in Table 7.2.8.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Table 7.2.7 Excitation table for T flip-flop

The first row of circuit excitation table shows that there is no change in the state for both flip-flops. The transition from $0 \rightarrow 0$ for T flip-flop requires input T to be at logic 0. The second row shows that flip-flop A has transition $0 \rightarrow 1$. It requires the input T_A to be at logic 1. It requires the input T_A to be at logic 1. Similarly, we can find inputs for each flip-flop for each row in the table by referring present state, next state and excitation table.

Let us use K-map simplification to determine the flip-flop input functions and circuit output functions.

Present state	Input		Next state		Flip-flop inputs		Output	
	A	B	X	A	B	T_A	T_B	
0 0	0	0	0	0	0	0	0	0
0 0	0	0	1	1	0	1	0	1
0 1	0	1	0	1	1	1	0	0
0 1	0	1	1	0	0	0	1	0
1 0	1	0	0	1	0	0	0	1
1 0	1	0	1	0	1	1	1	0
1 1	1	1	0	0	0	1	1	1

Table 7.2.8 Circuit excitation table

Therefore, input function for

$$T_A = B\bar{X} + \bar{B}X,$$

$$T_B = AB + BX + AX, \text{ and}$$

$$\text{Circuit output function} = A\bar{X} + \bar{A}\bar{B}X$$

With these flip-flop input functions and circuit output function we can draw the logic diagram as follows :

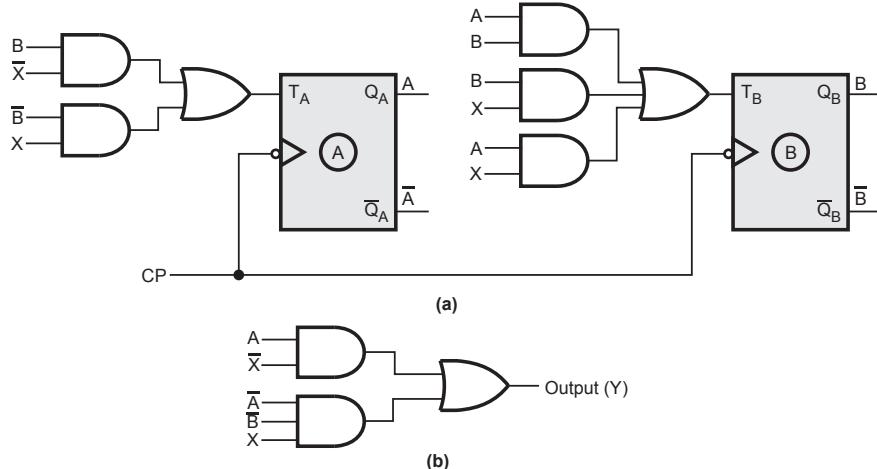


Fig. 7.2.10 Logic diagram of given sequential circuit using T flip-flops

3. Design using RS flip-flops

Using the excitation table for RS flip-flop shown in Table 7.2.9 we can determine the excitation table for the given circuit as shown in Table 7.2.10.

Q _n	Q _{n+1}	R	S
0	0	X	0
0	1	0	1
1	0	1	0
1	1	0	X

Table 7.2.9 Excitation table for RS flip-flop

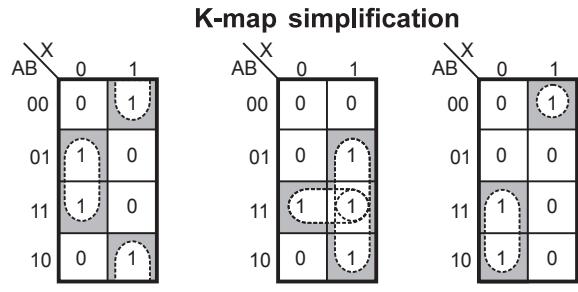


Fig. 7.2.9

Present state	Input	Next state	Flip-flop inputs				Output
			A	B	R _A	S _A	
0 0	0	0 0	X	0	X	0	0
0 0	1	1 0	0	1	X	0	1
0 1	0	1 1	0	1	0	X	0
0 1	1	0 0	X	0	1	0	0
1 0	0	1 0	0	X	X	0	1
1 0	1	0 1	1	0	0	1	0
1 1	0	0 0	1	0	1	0	1
1 1	1	1 0	0	X	1	0	0

Table 7.2.10

The first row of circuit excitation table shows that there is no change in the state for both flip-flops. The transition from $0 \rightarrow 0$ for RS flip-flop requires inputs R and S to be X and 0, respectively. Similarly, we can determine inputs for each flip-flop for each row in the table by referring present state, next state and excitation table. Let us use K-map simplification to determine the flip-flop input functions and circuit output functions.

Therefore input function for

$$R_A = AB\bar{X} + A\bar{B}X$$

$$S_A = \bar{A}B\bar{X} + \bar{A}\bar{B}X$$

$$R_B = AB + BX$$

$$S_B = A\bar{B}X \text{ and,}$$

$$\text{Circuit output function} = A\bar{X} + \bar{A}\bar{B}X$$

With these flip-flop input functions and circuit output function we can draw the logic diagram as follows :

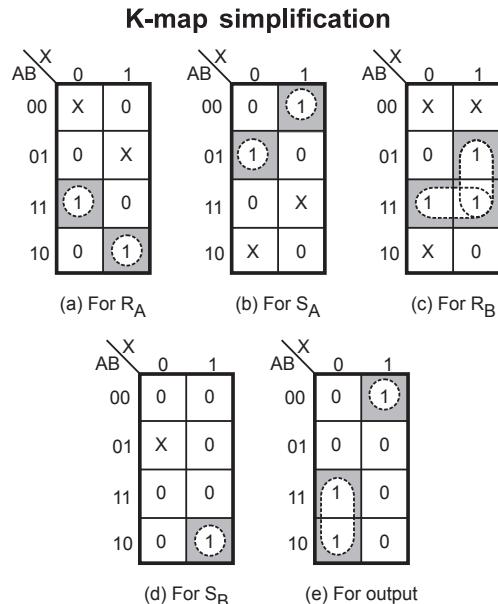


Fig. 7.2.11

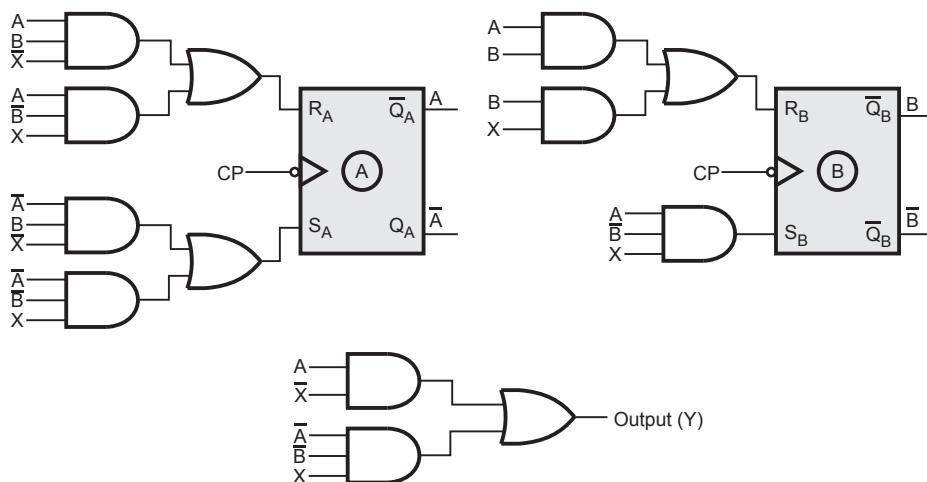


Fig. 7.2.12 Logic diagram of given sequential circuit using RS flip-flop

4. Design using JK flip-flops

Using the excitation table for JK flop-flop shown in Table 7.2.11 we can determine the excitation table for the given circuit as shown in Table 7.2.12.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Table 7.2.11 Excitation table for JK flip-flop

Present state		Input	Next state		Flip-flop inputs				Output
A	B	X	A	B	J_A	K_A	J_B	K_B	Y
0	0	0	0	0	0	X	0	X	0
0	0	1	1	0	1	X	0	X	1
0	1	0	1	1	1	X	X	0	0
0	1	1	0	0	0	X	X	1	0
1	0	0	1	0	X	0	0	X	1
1	0	1	0	1	X	1	1	X	0
1	1	0	0	0	X	1	X	1	1
1	1	1	1	0	X	0	X	1	0

Table 7.2.12

The first row of circuit excitation table shows that there is no change in the state for both flip-flops. The transition from 0 → 0 for JK flip-flop requires inputs J and K to be 0 and X, respectively. Similarly, we can determine inputs for each flip-flop for each row in the table by referring present state, next state and excitation table. Let us use K-map simplification to determine the flip-flop input functions and circuit output functions.

K-map simplification

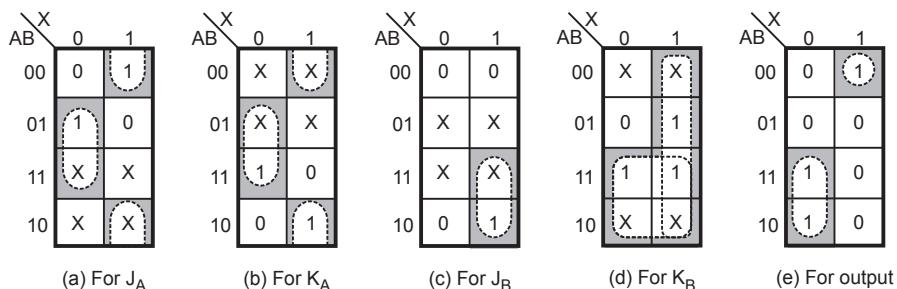


Fig. 7.2.13

Therefore, input function for

$$J_A = B\bar{X} + \bar{B}X$$

$$K_A = B\bar{X} + \bar{B}X$$

$$J_B = AX$$

$$K_B = A + X$$

$$\text{Circuit output function} = A\bar{X} + \bar{A}\bar{B}X$$

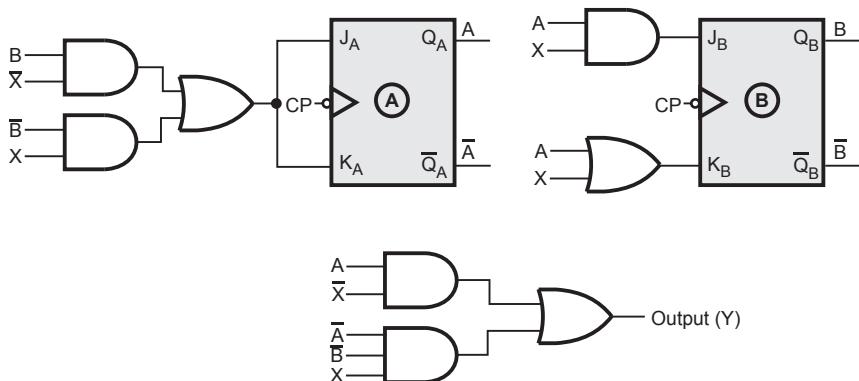


Fig. 7.2.14 Logic diagram of given sequential circuit using JK flip-flop

7.2.4 State Assignment Problem

Example 7.2.4 Design a sequential circuit for a state diagram shown in Fig. 7.2.15.

Solution :

Step 1 : Assign binary values to each state. Using random state assignment we get

$a = 000$, $b = 001$, $c = 010$, $d = 011$ and $e = 100$. The excitation table with these assignments is as given in Table 7.2.13.

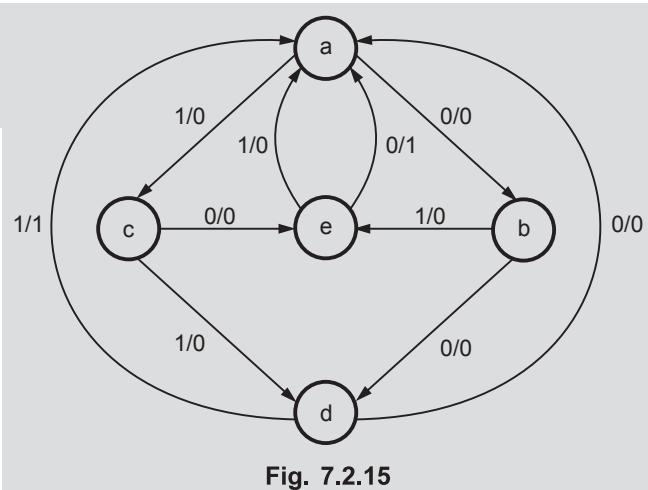


Fig. 7.2.15

Step 2 : Find number of flip-flops needed. Since there are five states we require $2^n \geq 5$
 $\therefore n = 3$ flip-flops.

Let us use D flip-flops

Step 3 : Derive the excitation table.

Present state			Input	Next state			Output
A_n	B_n	C_n	X	A_{n+1}	B_{n+1}	C_{n+1}	Z
0	0	0	0	0	0	1	0
0	0	0	1	0	1	0	0
0	0	1	0	0	1	1	0
0	0	1	1	1	0	0	0

0	1	0	0	1	0	0	0
0	1	0	1	0	1	1	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	1
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

Table 7.2.13

Step 4 : Derive circuit output and flip-flop input functions using K-map simplification

		C _n	X			
		00	01	11	10	
A _n	B _n	00	0	0	1	0
		01	1	0	0	0
A _n	B _n	11	X	X	X	X
		10	0	0	X	X

$$D_A = B_n \bar{C}_n \bar{X} + \bar{B}_n C_n X$$

		C _n	X			
		00	01	11	10	
A _n	B _n	00	0	1	0	1
		01	0	1	0	0
A _n	B _n	11	X	X	X	X
		10	0	0	X	X

$$D_B = \bar{A}_n \bar{C}_n X + \bar{B}_n C_n \bar{X}$$

		C _n	X			
		00	01	11	10	
A _n	B _n	00	1	0	0	1
		01	0	1	0	0
A _n	B _n	11	X	X	X	X
		10	0	0	X	X

$$D_C = \bar{A}_n \bar{B}_n \bar{X} + B_n \bar{C}_n X$$

Fig. 7.2.16 (a)

The random assignments require:

- 7 three input AND functions
 - 1 two input AND function
 - 4 two input OR functions
-
- 12 gates with 31 inputs

Step 5 : State assignment using rules.

Now we will apply the state assignment rules and compare the results.

Looking at Fig. 7.2.16 (a) and (b).

Rule 1 says that : e and d must be adjacent, and

		C _n	X			
		00	01	11	10	
A _n	B _n	00	0	0	0	0
		01	0	0	1	0
A _n	B _n	11	X	X	X	X
		10	1	0	X	X

$$Z = B_n C_n X + A_n \bar{X}$$

Fig. 7.2.16 (b)

b and c must be adjacent

Rule 2 says that : b and c must be adjacent, and
e and d must be adjacent

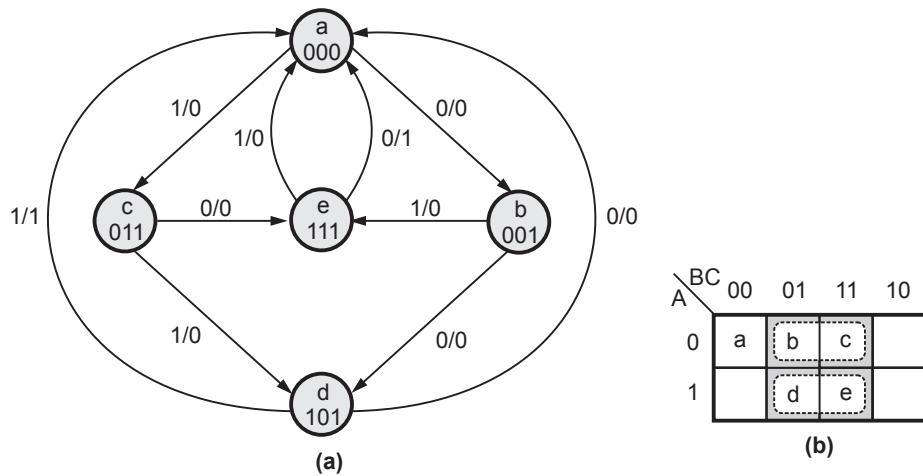


Fig. 7.2.17 (a) State diagram after applying Rules 1 and 2

(b) K-map showing b-c d-e adjacent to each other

Step 6 : Derive excitation table

Applying Rule 1 Rule 2 to the state diagram we get the excitation table as shown in the Table 7.2.14.

Present state			Input	Next state			Output
A_n	B_n	C_n	X	A_{n+1}	B_{n+1}	C_{n+1}	Z
0	0	0	0	0	0	1	0
0	0	0	1	0	1	1	0
0	0	1	0	1	0	1	0
0	0	1	1	1	1	1	0
0	1	0	0	X	X	X	X
0	1	0	1	X	X	X	X
0	1	1	0	1	1	1	0
0	1	1	1	1	0	1	0
1	0	0	0	X	X	X	X
1	0	0	1	X	X	X	X

1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	0	0	0	1
1	1	1	1	0	0	0	0

Table 7.2.14

Step 7 : Derive circuit output and flip-flop input functions using K-map simplification.

		C _n X	00	01	11	10
		A _n B _n	00	01	11	10
00	00	0	0	1	1	
00	01	X	X	1	1	
01	11	X	X	0	0	
01	10	X	X	0	0	

$$A_{n+1} = D_A = \bar{A}_n C_n$$

		C _n X	00	01	11	10
		A _n B _n	00	01	11	10
00	00	0	1	1		0
00	01	X	X	0	1	
01	11	X	X	0	0	
01	10	X	X	0	0	

$$B_{n+1} = D_B = \bar{A}_n \bar{B}_n X + \bar{A}_n B_n \bar{X}$$

		C _n X	00	01	11	10
		A _n B _n	00	01	11	10
00	00	1	1	1	1	
00	01	X	X	1	1	
01	11	X	X	0	0	
01	10	X	X	0	0	

$$C_{n+1} = D_C = \bar{A}_n$$

Fig. 7.2.18 (a)

The state assignments using Rule 1 and 2 require :

- | | | |
|-----------------------------|---------------------------|--------------------------|
| 4 three input AND functions | 1 two input AND functions | 2 two input OR functions |
| 7 gates with 18 inputs | | |

Thus by simply applying Rules 1 and 2 good results have been achieved.

		C _n X	00	01	11	10
		A _n B _n	00	01	11	10
00	00	0	0	0	0	0
00	01	X	X	0	0	
01	11	X	X	0	1	
01	10	X	X	1	0	

$$Z = A_n B_n \bar{X} + A_n \bar{B}_n \bar{X}$$

Fig. 7.2.18 (b)

7.2.5 Design with Unused States

There are occasions when a sequential circuit may use less than the available these maximum number of states. We can consider the unused states as don't care conditions and can be used to simplify the input functions to flip-flops.

Let us consider one example. First we will design the given sequential circuit without using unused states and then we will design the given sequential circuit using unused states.

Example 7.2.5 Design the sequential circuit for the state diagram shown in Fig. 7.2.19 use JK flip-flops.

Solution : Step 1 : Derive excitation table

The excitation table for given state diagram is as follows

Present state	Input	Next state			Flip-flop inputs						Output				
		A	B	C	X	A	B	C	J _A	K _A	J _B	K _B	J _C	K _C	Y
0 0 1	0	0	1	0	0	X	1	X	X	X	1				1
0 0 1	1	0	1	1	0	X	1	X	X	X	0				1
0 1 0	0	0	0	1	0	X	X	1	1	1	X				0
0 1 0	1	0	1	0	0	X	X	0	0	0	X				1
0 1 1	0	1	0	0	1	X	X	1	X	1					1
0 1 1	1	1	1	0	1	X	X	0	X	1					0
1 0 0	0	1	1	0	X	0	1	X	0	X	0				0
1 0 0	1	0	0	1	X	1	0	X	1	X					1
1 1 0	0	1	1	0	X	0	X	0	0	0	X				1
1 1 0	1	0	1	0	X	1	X	0	0	0	X				0

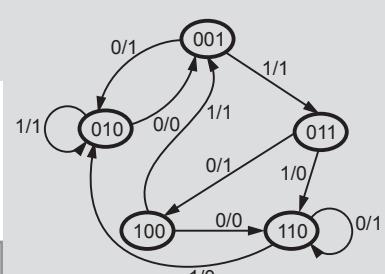


Fig. 7.2.19

Table 7.2.15

Step 2 : K-map simplification for JK inputs and circuit output

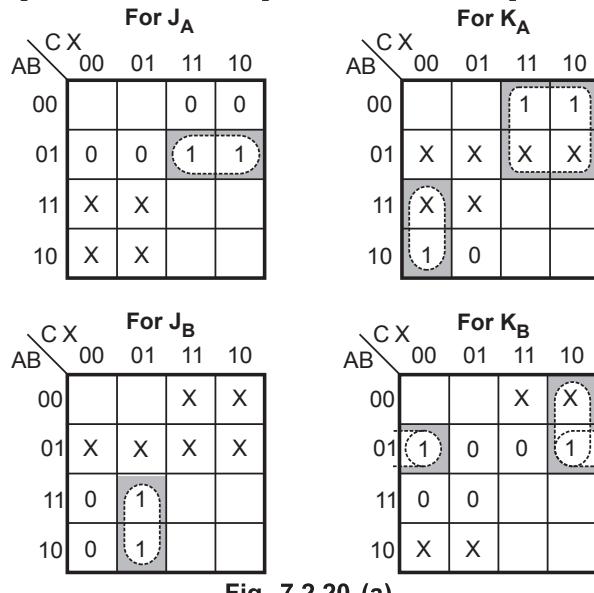


Fig. 7.2.20 (a)

		For J_C				For K_C				For Output						
		AB	00	01	11	10	AB	00	01	11	10	AB	00	01	11	10
C	X	00		X	X		00		1	0		00		1	1	
0	1	01	1	0	X	X	01	X	X	1	1	01	0	1	0	1
1	0	11	0	0			11	X	X			11	1	0		
0	1	10	0	1			10	X	X			10	0	1		

Fig. 7.2.20 (b)

Therefore, input functions for

$$J_A = \overline{ABC}$$

$$K_A = A\overline{C}\overline{X} + \overline{AC}$$

$$J_B = A\overline{C}X$$

$$K_B = \overline{AB}\overline{X} + \overline{AC}\overline{X}$$

$$J_C = \overline{AB}\overline{X} + A\overline{B}\overline{C}X$$

$$K_C = \overline{AB} + \overline{AC}X \text{ and}$$

Circuit output function, $Y = AB\overline{C}\overline{X} + \overline{ABC} + A\overline{B}\overline{C}X + \overline{A}\overline{B}C + \overline{AC}\overline{X}$

Step 3 : Draw logic diagram.

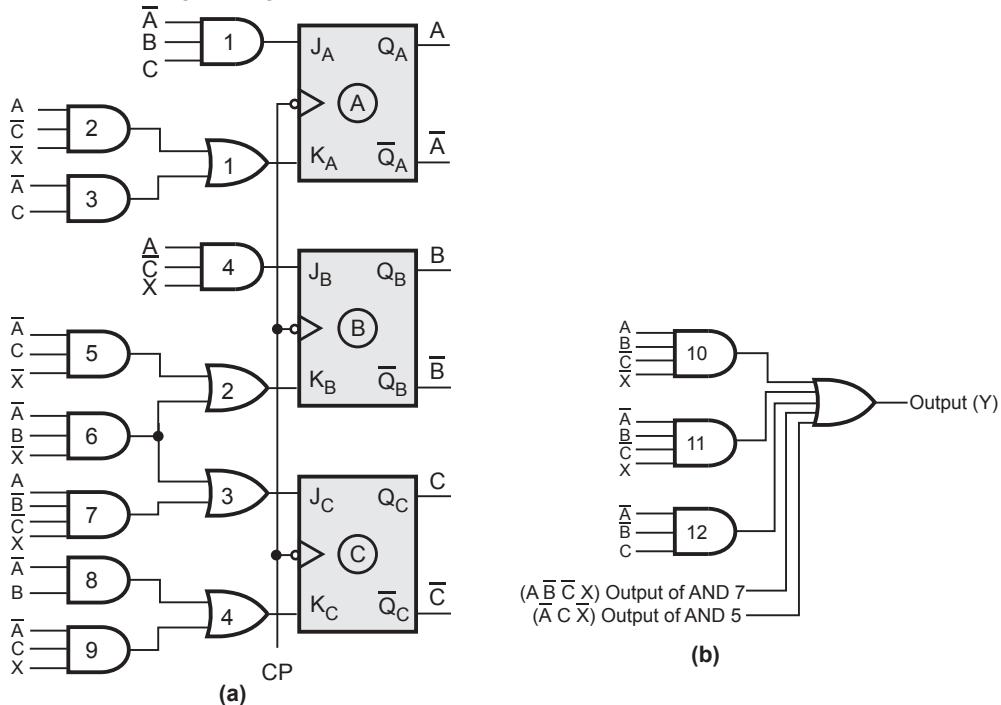


Fig. 7.2.21

Step 4 : Derive circuit output and flip-flop inputs considering unused states.

Let us see the circuit design with the use of unused states. These unused states 000, 101 and 111 are considered as a don't cares and are used to simplify the K-maps as follows :

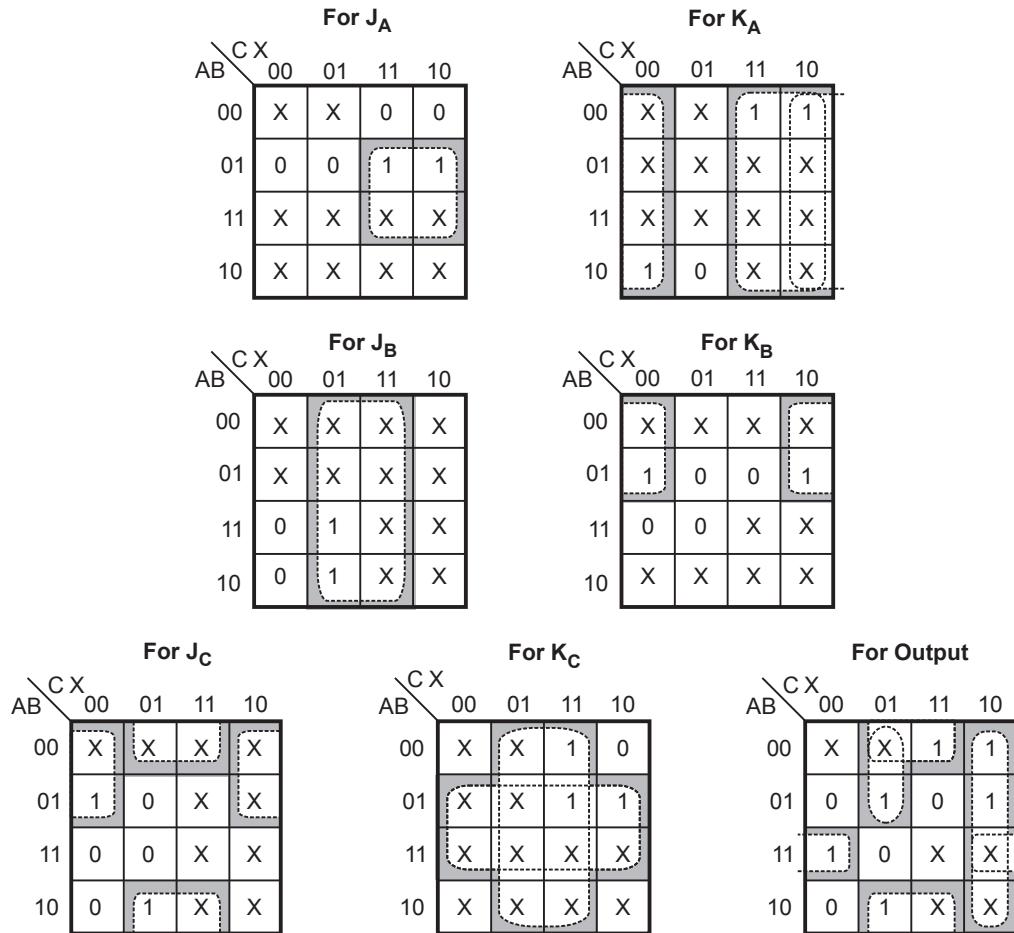


Fig. 7.2.22

Therefore, input functions for

$$J_A = BC$$

$$K_A = \bar{X} + C$$

$$J_B = X$$

$$K_B = \bar{A} \bar{X}$$

$$J_C = \bar{A} \bar{X} + \bar{B} X \quad \text{and} \quad K_C = B + X$$

The circuit output function $Y \equiv AB\bar{X} + A\bar{C}X + \bar{B}X + C\bar{X}$

Step 5 : Draw logic diagram.

From the above logic diagram it can be realized that using unused state as don't cares we can further simplify the flip-flop input functions and circuit output function.

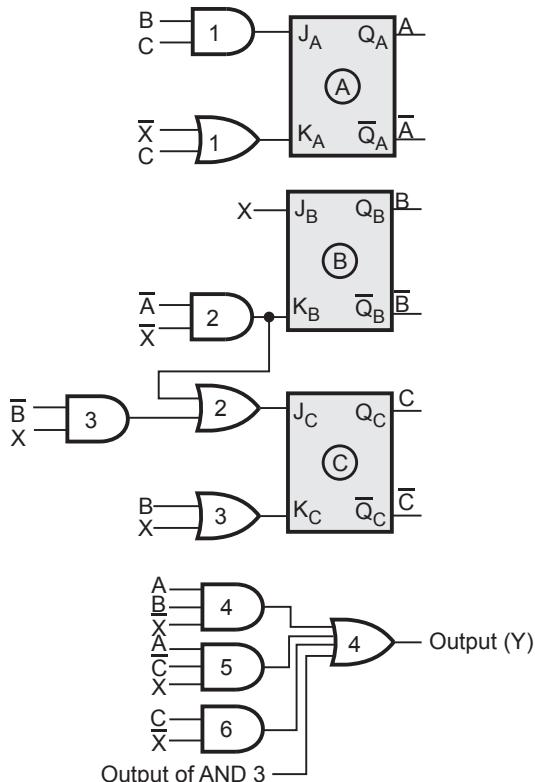


Fig. 7.2.23 Logic diagram

Examples with Solutions

Example 7.2.6 Design a synchronous sequential circuit using JK for the given state diagram.

Solution : Step 1 : Since $N = 4$. Number of flip-flops needed = 2

Step 2 : Flip-flops to be used : JK

Step 3 : Determine the excitation table.

Present state	Input	Next state	Flip-flop inputs			
A	B	X	A ⁺	B ⁺	J _A	K _A
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	1	0	1	X

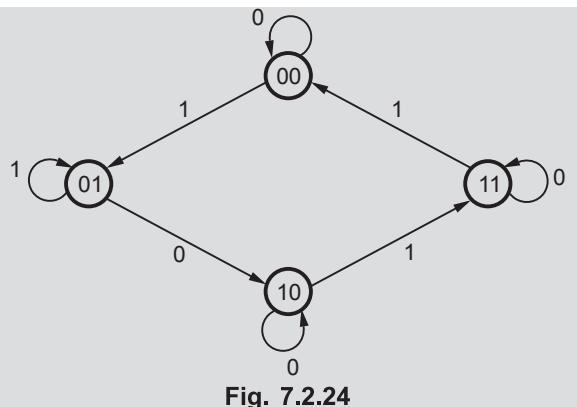


Fig. 7.2.24

0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

Step 4 : K-map simplification

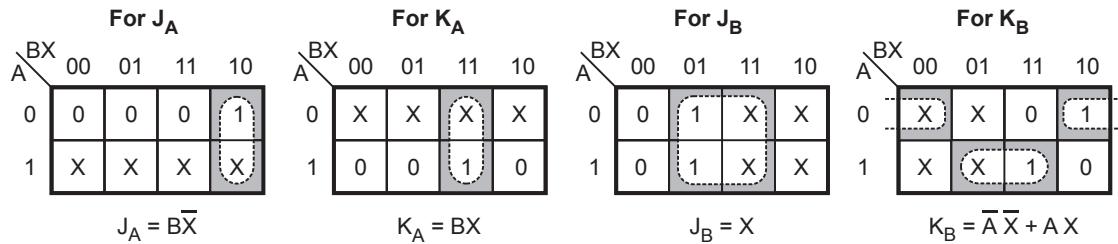


Fig. 7.2.25

Step 5 : Logic diagram

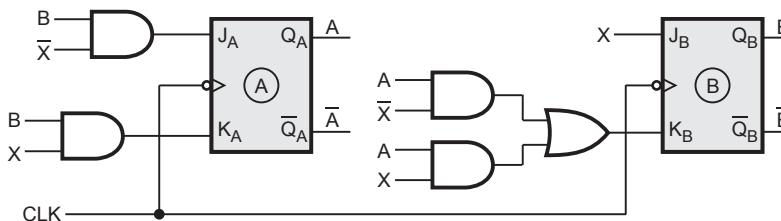


Fig. 7.2.26

Example 7.2.7 Design the sequential circuit using JK flip-flops, for state diagram shown in Fig. 7.2.27. **SPPU : Dec.-10, May-05,11, Marks 8**

Solution : The state table for the given state diagram is as follows.

Input X	Present State	Next State	Output Y
0	S_0	S_0	0
0	S_1	S_2	1
0	S_2	S_1	1
0	S_3	S_0	1
1	S_0	S_1	0
1	S_1	S_3	0
1	S_2	S_0	1
1	S_3	S_1	0

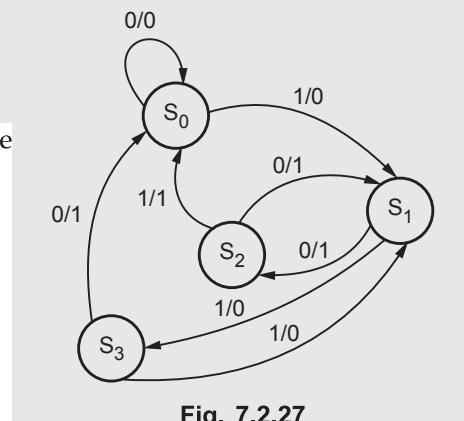
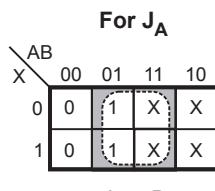


Fig. 7.2.27

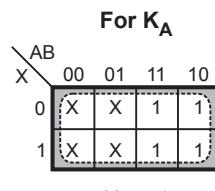
Assigning states $S_0 = 00$, $S_1 = 01$, $S_2 = 10$ and $S_3 = 11$ we have,

Input	Present State		Next State		Flip-Flop Excitation Table				Output
	A	B	A_{+1}	B_{+1}	J_A	K_A	J_B	K_B	
0	0	0	0	0	0	X	0	X	0
0	0	1	1	0	1	X	X	1	1
0	1	0	0	1	X	1	1	X	1
0	1	1	0	0	X	1	X	1	1
1	0	0	0	1	0	X	1	X	0
1	0	1	1	1	1	X	X	0	0
1	1	0	0	0	X	1	0	X	1
1	1	1	0	1	X	1	X	0	0

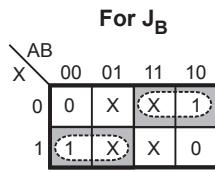
K-map simplification



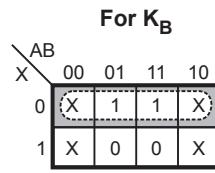
$$J_A = B$$



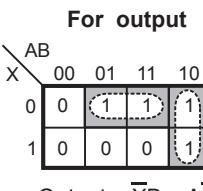
$$K_A = 1$$



$$J_B = \bar{X}A + X\bar{A} = A \oplus X$$



$$K_B = \bar{X}$$



$$\text{Output} = \bar{X}B + A\bar{B}$$

Fig. 7.2.28

Logic diagram

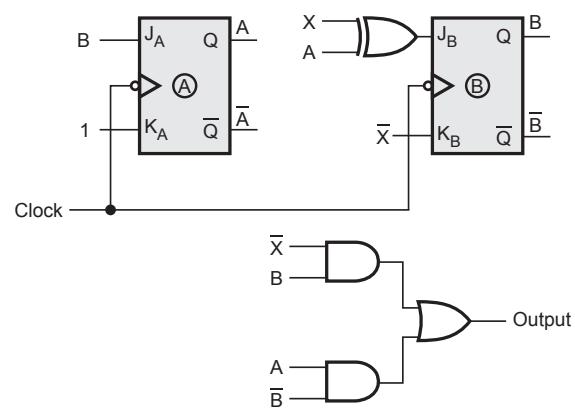


Fig. 7.2.29

Example 7.2.8 Implement the following state diagram using D flip-flop.

SPPU : Dec.-12, Marks 10

Solution : The excitation table for the given state diagram is shown in the Table 7.2.16. Since D flip-flops are used, flip-flop excitations are same as next states.

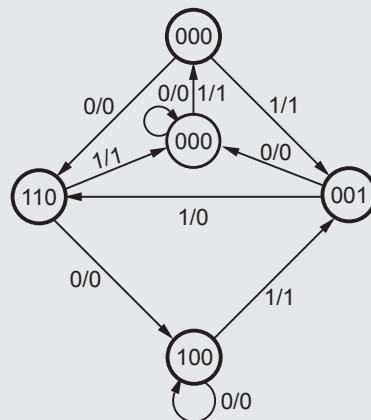


Fig. 7.2.30

Input X	Present state			Next state			Output Y
	A	B	C	A ⁺	B ⁺	C ⁺	
0	0	0	0	1	1	0	0
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X	X	X	X
0	1	0	0	1	0	0	0
0	1	0	1	X	X	X	X
0	1	1	0	1	0	0	0
0	1	1	1	X	X	X	X
1	0	0	0	0	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	0	0	0	1
1	0	1	1	X	X	X	X
1	1	0	0	0	0	1	1
1	1	0	1	X	X	X	X
1	1	1	0	0	1	0	1
1	1	1	1	X	X	X	X

K-map Simplification

		For D _A			
BC	XA	00	01	11	10
00	00	1	0	X	0
00	01	1	X	X	1
01	00	0	X	X	0
01	01	0	1	X	0
11	00	0	0	X	0
10	00	0	0	X	0

$$D_A = \overline{X} \overline{B} \overline{C} + \overline{X}A + XC$$

		For D _B			
BC	XA	00	01	11	10
00	00	1	1	X	1
00	01	0	X	X	0
01	00	0	X	X	1
01	01	0	1	X	0
11	00	0	0	X	1
10	00	0	1	X	0

$$D_B = \overline{X} \overline{A} + C + XAB$$

		For D _C			
BC	XA	00	01	11	10
00	00	0	0	X	0
00	01	0	X	X	0
01	00	0	0	X	0
01	01	1	X	X	0
11	00	1	X	X	0
10	00	1	0	X	0

$$D_C = X \overline{B} \overline{C}$$

		For Y			
BC	XA	00	01	11	10
00	00	0	0	X	0
00	01	0	X	X	0
01	00	0	0	X	1
01	01	1	X	X	1
11	00	1	X	X	1
10	00	1	0	X	1

$$Y = X \overline{C}$$

Table 7.2.16 Excitation table

Fig. 7.2.31

Implementation

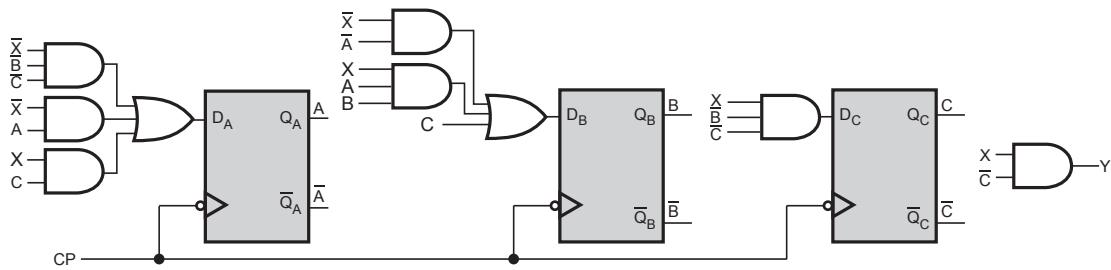


Fig. 7.2.32

Example 7.2.9 Using J-K flip-flops, design a synchronous counter that has the following sequence : 0 → 2 → 5 → 6 → 0
undesired states 1, 3, 4, 7 must always go to 0 on the next clock pulse.

SPPU : May-05, Marks 10

Solution :

Excitation table

Present state	Next state			Flip-flop inputs								
	A	B	C	A_{+1}	B_{+1}	C_{+1}	J_A	K_A	J_B	K_B	J_C	K_C
0 0 0	0	1	0	0	X	1	X	0	X			
0 0 1	0	0	0	0	X	0	X	X	X	1		
0 1 0	1	0	1	1	X	X	1	1	X			
0 1 1	0	0	0	0	X	X	1	X	1			
1 0 0	0	0	0	X	1	0	X	0	X			
1 0 1	1	1	0	X	0	1	X	X	X	1		
1 1 0	0	0	0	X	1	X	1	0	X			
1 1 1	0	0	0	X	1	X	1	X	1			

K-map simplification

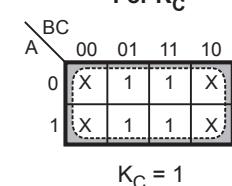
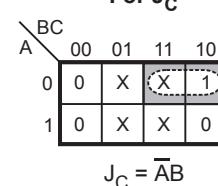
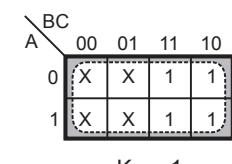
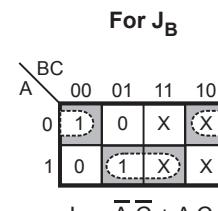
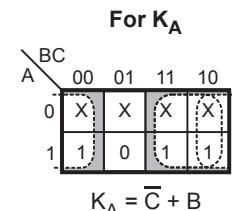
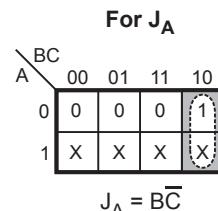


Table 7.2.17

Fig. 7.2.33

Logic diagram

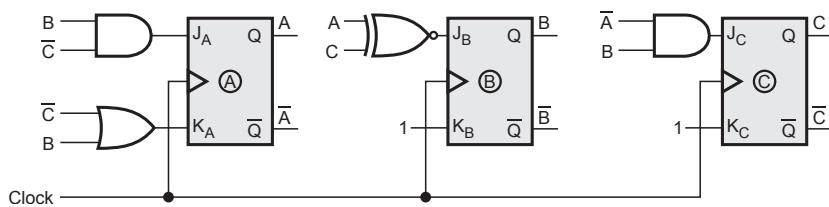


Fig. 7.2.34

Example 7.2.10 Design and implement 4-bit binary counter (using D flip-flops) which counts all possible odd numbers only.

SPPU : Dec.-05, Marks 8

Solution : The state diagram for given problem is as shown in the Fig. 7.2.35.

Excitation table

Present state				Next state			
Q_A	Q_B	Q_C	Q_D	Q_A+	Q_B+	Q_C+	Q_D+
0	0	0	0	×	×	×	×
0	0	0	1	0	0	1	1
0	0	1	0	×	×	×	×
0	0	1	1	0	1	0	1
0	1	0	0	×	×	×	×
0	1	0	1	0	1	1	1
0	1	1	0	×	×	×	×
0	1	1	1	1	0	0	1
1	0	0	0	×	×	×	×
1	0	0	1	1	0	1	1
1	0	1	0	×	×	×	×
1	0	1	1	1	1	0	1
1	1	0	0	×	×	×	×
1	1	0	1	1	1	1	1
1	1	1	0	×	×	×	×
1	1	1	1	0	0	0	1

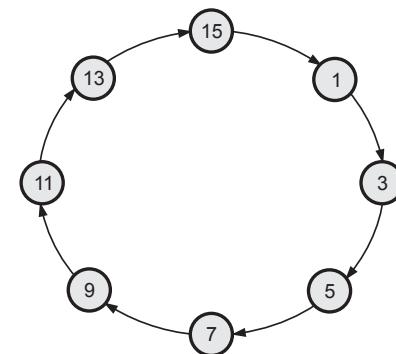


Fig. 7.2.35 State diagram

K-map simplification

For D_A			
Q_A	Q_B	Q_C	Q_D
00	0	0	0
01	0	1	1
11	1	0	0
10	1	1	0

$$D_A = Q_A \bar{Q}_C + Q_A \bar{Q}_B + \bar{Q}_A Q_B Q_C$$

For D_B			
Q_A	Q_B	Q_C	Q_D
00	0	1	X
01	1	0	X
11	1	0	X
10	0	1	X

$$D_B = Q_B \bar{Q}_C + \bar{Q}_B Q_C$$

For D_C			
Q_A	Q_B	Q_C	Q_D
00	1	0	X
01	1	0	X
11	0	1	X
10	0	1	X

$$D_C = \bar{Q}_C$$

For D_D			
Q_A	Q_B	Q_C	Q_D
00	1	1	X
01	1	1	X
11	1	1	X
10	1	1	X

$$D_D = 1$$

Fig. 7.2.36

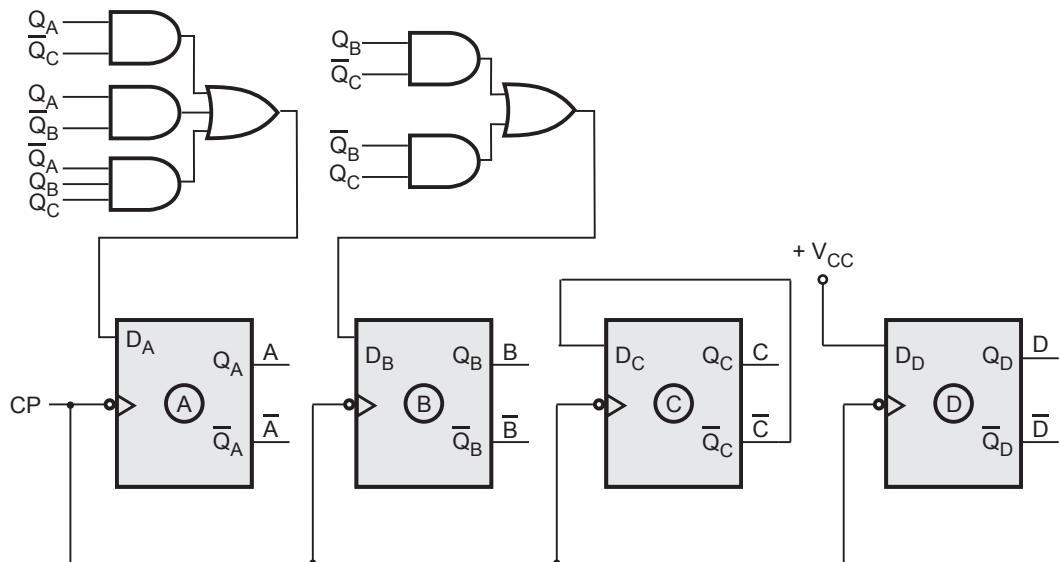
Logic diagram

Fig. 7.2.37

Example 7.2.11 Design a non-sequential counter using J-K flip-flop; as per following state diagram.

SPPU : May-06, Marks 8

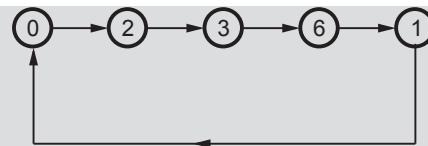
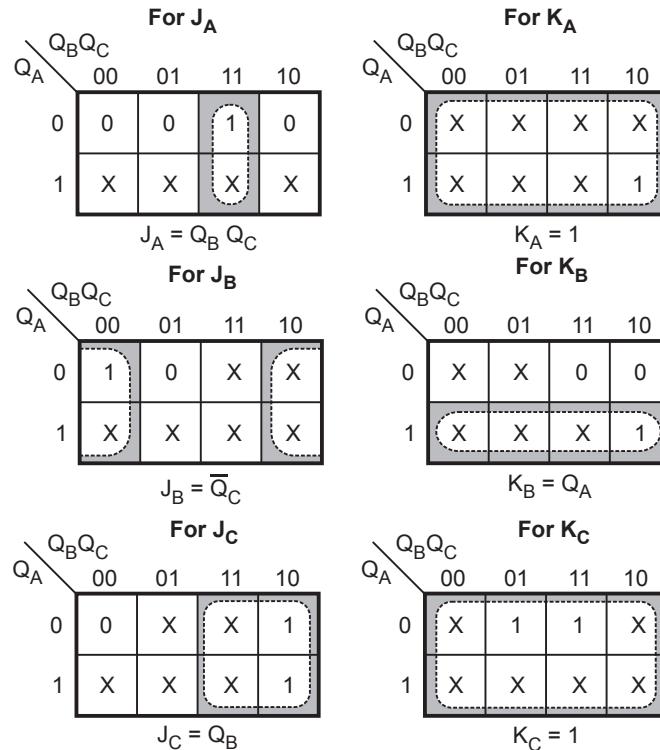


Fig. 7.2.38

Solution : Excitation table

Present state			Next state			Flip-flop inputs					
Q_A	Q_B	Q_C	Q'_A	Q'_B	Q'_C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	0	0	x	1	x	0	x
0	0	1	0	0	0	0	x	0	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	1	0	1	x	x	0	x	1
1	0	0	x	x	x	x	x	x	x	x	x
1	0	1	x	x	x	x	x	x	x	x	x
1	1	0	0	0	1	x	1	x	1	1	x
1	1	1	x	x	x	x	x	x	x	x	x

K-map simplification



Logic diagram

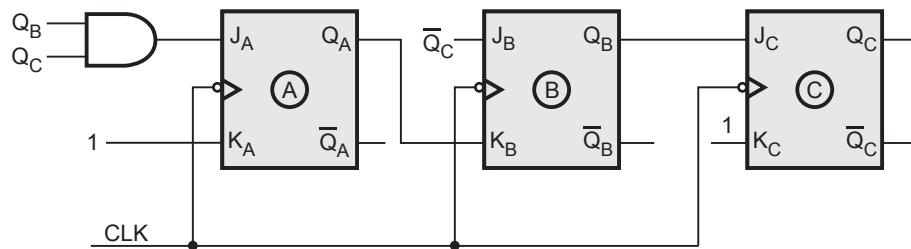


Fig. 7.2.38 (a)

Example 7.2.12 Design the circuit to generate the sequence :

$0 \rightarrow 2 \rightarrow 5 \rightarrow 4 \rightarrow 7 \rightarrow 3$

SPPU : May-12,13, Dec.-08, Marks 8

Solution : Excitation table

Present state			Next state			Flip-flop inputs					
Q _A	Q _B	Q _C	Q _{A+1}	Q _{B+1}	Q _{C+1}	J _A	K _A	J _B	K _B	J _C	K _C
0	0	0	0	1	0	0	X	1	X	0	X
0	0	1	X	X	X	X	X	X	X	X	X
0	1	0	1	0	1	1	X	X	1	1	X

0	1	1	0	0	0	0	X	X	1	X	1
1	0	0	1	1	1	X	0	1	X	1	X
1	0	1	1	0	0	X	0	0	X	X	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	0	1	1	X	1	X	0	X	0

K-map simplification

For J_A

	Q_B	Q_C	00	01	11	10
0	0	0	0	X	0	1
1	X	4	X	5	X	7
						2

$$J_A = Q_B \bar{Q}_C$$

For K_A

	Q_B	Q_C	00	01	11	10
0	X	0	X	1	X	X
1	0	4	0	5	1	7
						6

$$K_A = Q_B$$

For K_B

	Q_B	Q_C	00	01	11	10
0	1	0	X	1	X	X
1	1	4	0	5	X	X
						2

$$J_B = \bar{Q}_C$$

	Q_B	Q_C	00	01	11	10
0	X	0	X	1	1	2
1	X	4	X	5	0	7
						6

$$K_B = \bar{Q}_A$$

For J_C

	Q_B	Q_C	00	01	11	10
0	0	0	X	1	X	1
1	1	4	X	5	X	X
						6

$$J_C = Q_A + Q_B$$

For K_C

	Q_B	Q_C	00	01	11	10
0	X	0	X	1	1	2
1	X	4	1	5	0	7
						6

$$K_C = \bar{Q}_A + \bar{Q}_B$$

Fig. 7.2.39 (a)

Logic diagram

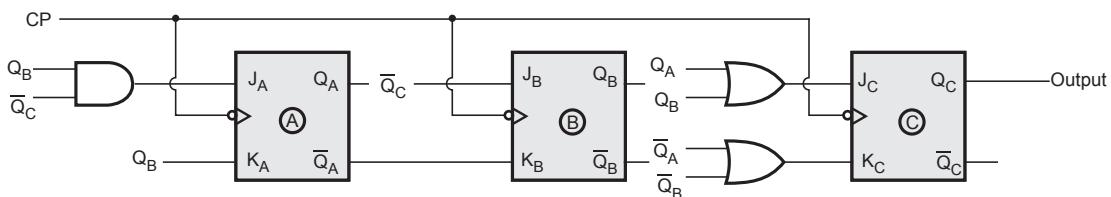


Fig. 7.2.39 (b)

Example 7.2.13 Design sequence generator to generate sequence 1-9-2-7-3-6 using JK flip-flop.

SPPU : Dec.-07, Marks 8

Solution : Excitation table

Present state				Next state				Flip-flop inputs							
Q_A	Q_B	Q_C	Q_D	Q_{A+1}	Q_{B+1}	Q_{C+1}	Q_{D+1}	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
0	0	0	0	×	×	×	×	×	×	×	×	×	×	×	×
0	0	0	1	1	0	0	1	1	×	0	×	0	×	0	0
0	0	1	0	0	1	1	1	0	0	1	1	0	0	1	x
0	0	1	1	0	1	1	0	0	0	1	1	0	0	x	1
0	1	0	0	×	×	×	×	0	0	0	0	0	0	0	0
0	1	0	1	×	×	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	1	0	1	1	x
0	1	1	1	0	0	1	1	0	0	0	1	0	0	x	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	0	1	0	0	1	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

K-map simplification

		For J_A				
		$Q_C Q_D$	00	01	11	10
$Q_A Q_B$		00	X	1	0	0
01		X	X	0	0	
11		X	X	X	X	
10		X	X	X	X	

$$J_A = \bar{Q}_C$$

		For K_A				
		$Q_C Q_D$	00	01	11	10
$Q_A Q_B$		00	X	X	X	X
01		X	X	X	X	
11		X	X	X	X	
10		X	1	X	X	

$$K_A = 1$$

		For J_B				
		$Q_C Q_D$	00	01	11	10
$Q_A Q_B$		00	X	0	1	1
01		X	X	X	X	
11		X	X	X	X	
10		X	0	X	X	

$$J_B = Q_C$$

		For K_B				
		$Q_C Q_D$	00	01	11	10
$Q_A Q_B$		00	X	X	X	X
01		X	X	1	1	
11		X	X	X	X	
10		X	X	X	X	

$$K_B = 1$$

		For J_C				
		$Q_C Q_D$	00	01	11	10
$Q_A Q_B$		00	X	0	X	X
01		X	X	X	X	
11		X	X	X	X	
10		X	1	X	X	

$$J_C = Q_A$$

		For K_C				
		$Q_C Q_D$	00	01	11	10
$Q_A Q_B$		00	X	X	0	0
01		X	X	0	1	
11		X	X	X	X	
10		X	X	X	X	

$$K_C = Q_B \bar{Q}_D$$

		For J_D				
		$Q_C Q_D$	00	01	11	10
$Q_A Q_B$		00	X	X	X	1
01		X	X	X	1	
11		X	X	X	X	
10		X	X	X	X	

$$J_D = 1$$

		For K_D				
		$Q_C Q_D$	00	01	11	10
$Q_A Q_B$		00	X	0	1	X
01		X	X	0	X	
11		X	X	X	X	
10		X	1	X	X	

$$K_D = Q_A + \bar{Q}_B Q_C$$

Logic diagram

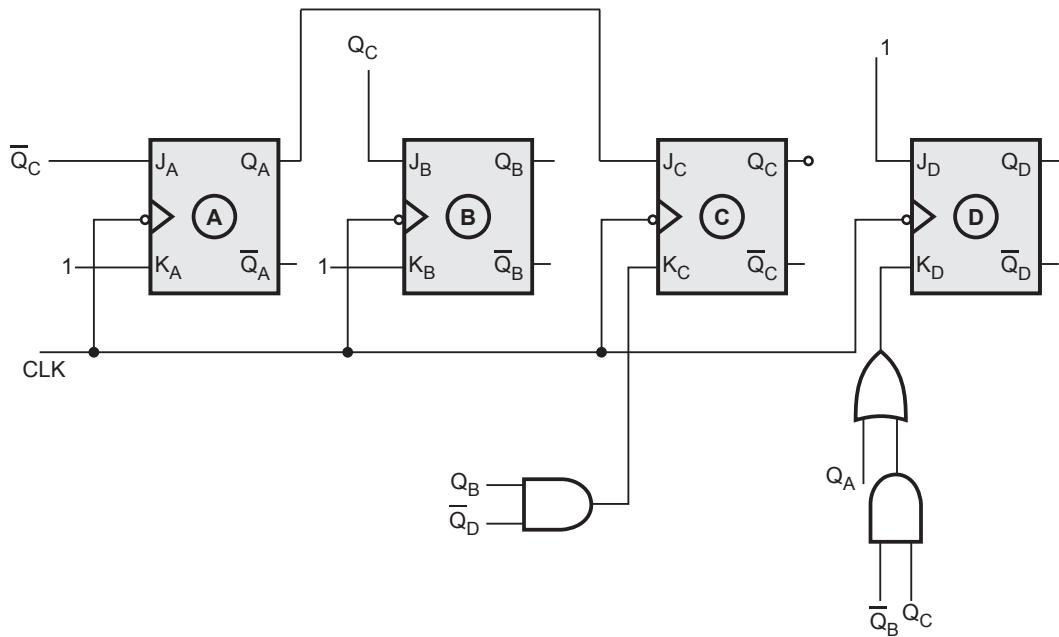


Fig. 7.2.40

Example 7.2.14 Design given sequence generator using J-K FF. Sequence is

1 → 3 → 5 → 6 → 7 → 1

SPPU : Dec.-14, Marks 6

Solution : Excitation table

P S			N S			Flip-flop Inputs					
A	B	C	A+	B+	C+	J _A	K _A	J _B	K _B	J _C	K _C
0	0	0	×	×	×	×	×	×	×	×	×
0	0	1	0	1	1	0	×	1	×	×	0
0	1	0	×	×	×	×	×	×	×	×	×
0	1	1	1	0	1	1	×	1	1	0	0
1	0	0	×	×	×	×	×	1	1	1	1
1	0	1	1	1	0	1	0	1	1	1	1
1	1	0	1	1	1	1	0	1	0	1	1
1	1	1	0	0	1	1	1	1	1	1	0

K-map simplification

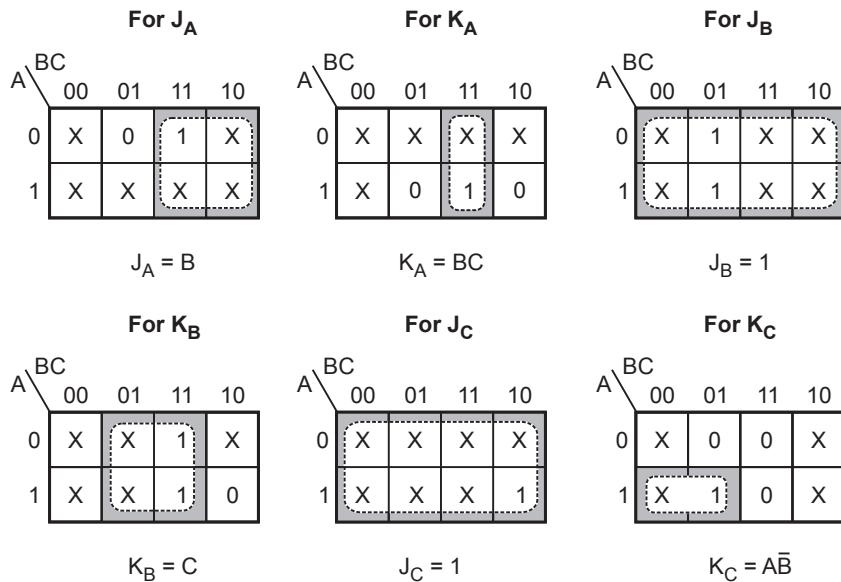


Fig. 7.2.41 (a)

Logic diagram

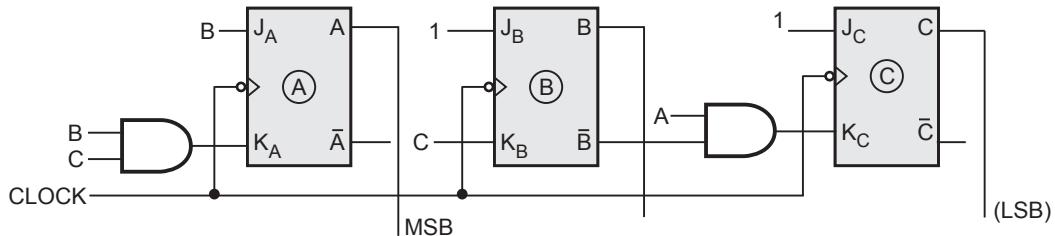


Fig. 7.2.41 (b)

Review Questions

1. Give recommended steps for the design of a clocked synchronous sequential networks.

2. Why is state reduction necessary?

3. Explain the state assignment rules.

SPPU : Dec.-13, Marks 3

4. Explain the procedure of state minimisation using Merger graph and Merger table.

5. Explain state reduction.

SPPU : Dec.-13, Marks 3

6. Explain state assignment.

SPPU : Dec.-12, Marks 12

7. Explain the steps involved in the reduction of state table.

8. Explain : 1) State table 2) State diagram

3) Rules for state reduction 4) State assignment.

SPPU : Dec.-10, May-13, Marks 8

7.3 Sequence Generator

SPPU : May-2000,02,06,08,12,18, Dec.-06,07,08,12,13

7.3.1 Sequence Generator using Counters

A sequential circuit which generates a prescribed sequence of bits, in synchronism with a clock, is referred to as a sequence generator. Fig. 7.3.1 shows the basic structure of a sequence generator using counters.

For the design of sequence generator, we must determine the required number of flip-flops and the logic circuit for next state decoder.

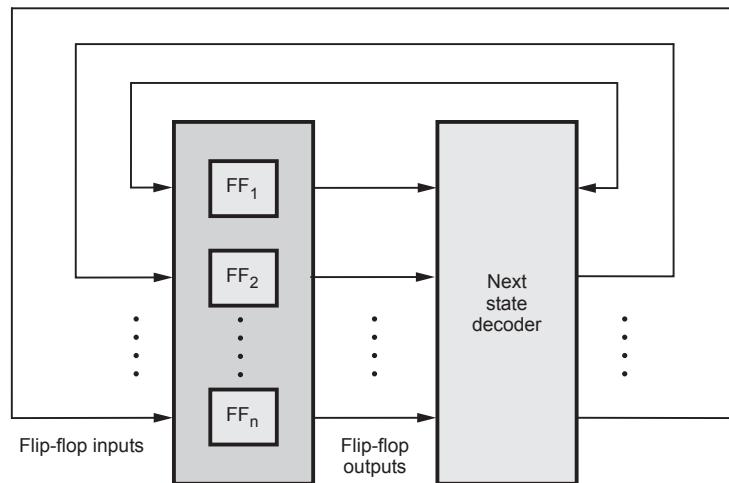


Fig. 7.3.1 Basic structure of a sequence generator

Number of flip-flops required

Number of flip-flops required to generate particular sequence can be determined as follows :

- Find the number of 1s in the sequence.
- Find the number of 0s in the sequence.
- Take the maximum out of two.
- If N is the required number of flip-flops, choose minimum value of n to satisfy equation given below.

$$\max(0s, 1s) \leq 2^n - 1$$

Examples with Solutions

Example 7.3.1 Find the number of flip-flops required to generate the sequence 1101011.

Solution : The given sequence number of 0s are 2 and number of 1s are 5. Therefore equation becomes,

$$\therefore \max(2, 5) \leq 2^n - 1$$

$$\therefore 5 \leq 2^n - 1$$

$$\therefore n = 4$$

Once the number of flip-flops are decided, we have to assign unique states corresponding to each bit in the given sequence such that flip-flop representing least significant bit generates the given sequence. (Usually, the output of the flip-flop representing least significant bit is used to generate the given sequence).

Example 7.3.2 Find the state assignments for sequence 1101011.

Solution : We have already seen that this sequence requires four flip-flops. Assuming the output of D flip-flop as a desired sequence state assignments are shown in Table 7.3.1.

A	B	C	D	States
0	0	0	1	1
0	0	1	1	3
0	0	0	0	0
0	1	0	1	5
0	0	1	0	2
0	1	1	1	7
1	0	0	1	9

Table 7.3.1

Example 7.3.3 Design a pulse-train generator to generate a pulse train 110011..... using 'D' flip-flop.

SPPU : May-06, Marks 8

Solution : The minimum number of flip-flops can be given as $N \leq 2^{n-1}$.

Since max (0s, 1s) = 4, N = 4, therefore n = 3. Table 7.3.2 shows state encoding for given sequence using 3 flip-flops.

Therefore, design a circuit to get above state. In case of D flip-flop, flip-flop inputs are same as next states.

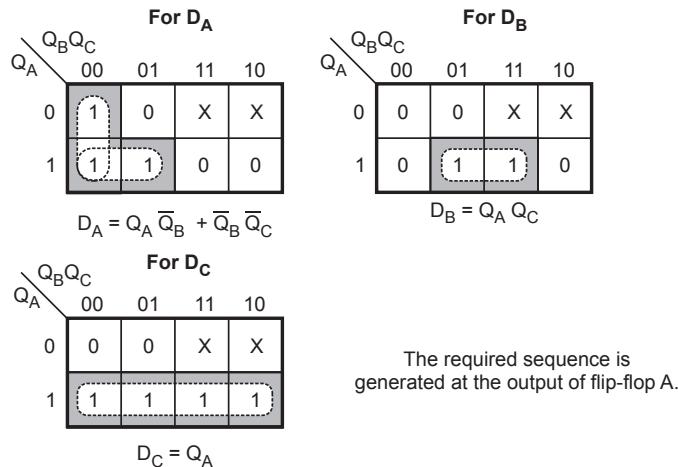
Excitation table

Present state			Next state/Flip-flop inputs		
Q _A	Q _B	Q _C	Q _A	Q _B	Q _C
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	x	x	x
0	1	1	x	x	x
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	1	0	1	1

CP	FF O/Ps			States
	Q _A	Q _B	Q _C	
1	1	1	1	7
2	1	1	0	6
3	0	0	1	1
4	0	0	0	0
5	1	0	0	4
6	1	0	1	5

Table 7.3.2

K-map simplification



Logic diagram

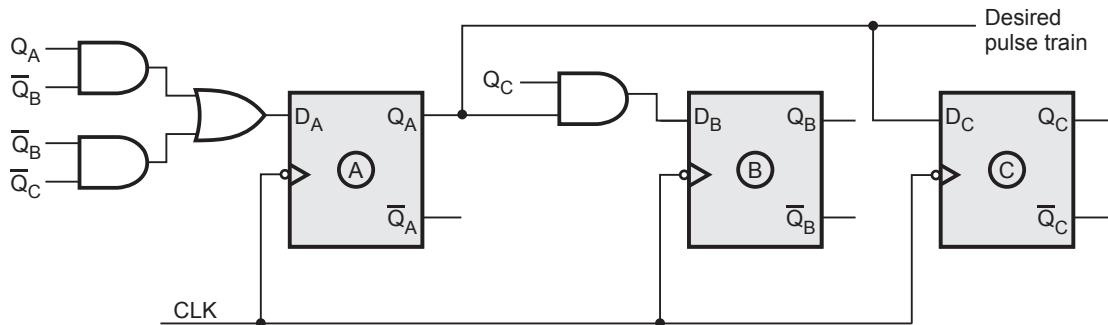


Fig. 7.3.2

7.3.2 Sequence Generator using Shift Register

The simplest way of designing sequence generator using shift register is to take shift register of n -bits where n is equal to the length of sequence. Then load the bit sequence in the shift register by parallel load operation and apply the clock signal.

The Fig. 7.3.3 illustrates the operation of such a sequence generator. Here, the sequence to be generated is 11001.

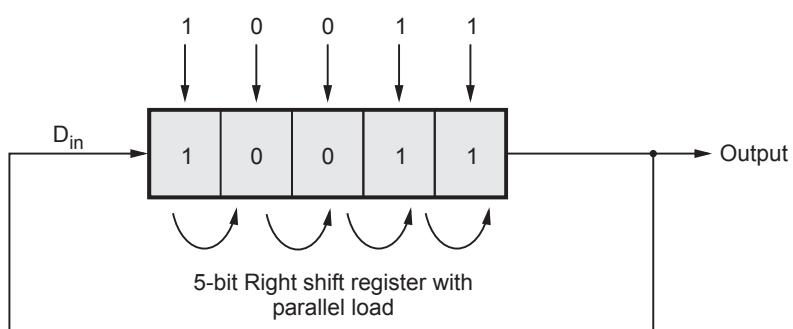


Fig. 7.3.3 Sequence generator

Another design approach is used for sequence generator to reduce the required number of flip-flop stages in the shift register. In this approach a shift register with a next state decoder and preset logic is used. The Fig. 7.3.4 shows the block diagram of this approach. Here, the output of the next state decoder is a function of Q_A, Q_B, \dots, Q_n and it is used to determine the D_{in} input for the shift right register. Initially, start button is pressed to activate parallel load operation. This loads initial value in the shift register. Then at each clock pulse shift register contents are shifted right by 1 bit position. The next state decoder circuit decodes the output and generates D_{in} input for the shift register such that output Q_A generates the desired sequence.

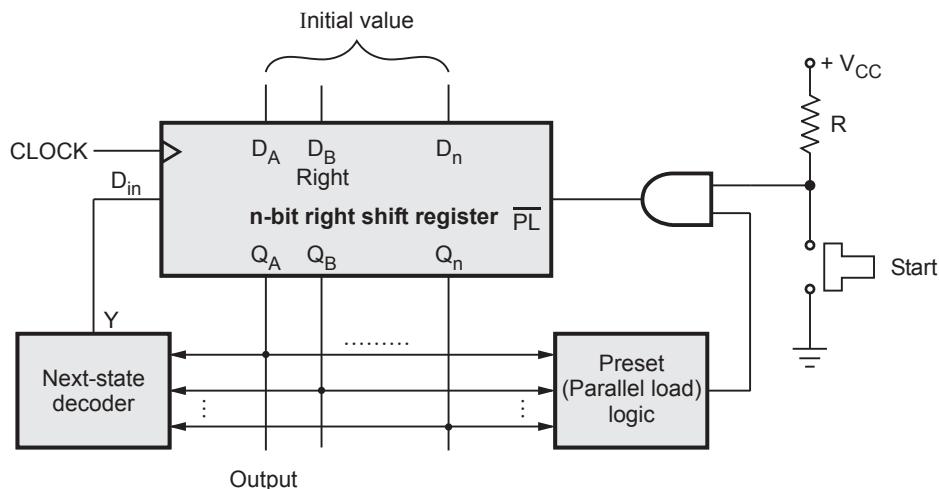


Fig. 7.3.4 Sequence generator using shift register

After completion of one complete sequence, the register is again loaded with initial value to start the next train of sequence.

Examples with Solutions

Example 7.3.4 Design a sequence generator to generate the sequence 1101011 by shift register method. SPPU : May-08, Dec.-08, Marks 8

Solution : In this approach, the minimum number of flip-flops n , required to generate a sequence of length N is given by

$$N \leq 2^n - 1$$

In this example, $N = 7$, therefore, the minimum value of n , which may generate this sequence is 3. However, it is not guaranteed to lead to a solution. Let us try with 3 flip-flops. The Table 7.3.3 shows sequence generation with three flip-flops.

CP	Flip-flop outputs			D _{in}	States
	Q _A	Q _B	Q _C		
1	1	0	0	1	4
2	1	1	0	0	6
3	0	1	1	1	3
4	1	0	1	0	5
5	0	1	0	1	2
6	1	0	1	—	5
—	—	—	—	—	—

State is repeated →

Table 7.3.3

As shown in the Table 7.3.4, the state 6 is repeated. This means that $n = 3$ is not sufficient. Let us try with 4 flip-flops. The table shows sequence generation with four flip-flops.

CP	Flip-flop outputs				D _{in}	Preset	States
	Q _A	Q _B	Q _C	Q _D			
Initial value	1	1	0	0	1	1	8
	2	1	1	0	0	1	12
	3	0	1	1	0	1	6
	4	1	0	1	1	1	11
	5	0	1	0	1	1	5
	6	1	0	1	0	1	10
Preset flip-flop	7	1	1	0	1	1	13
	1	1	1	0	X	0	14
	1	1	0	0	1	1	8

Table 7.3.4

K-map simplification for D_{in}

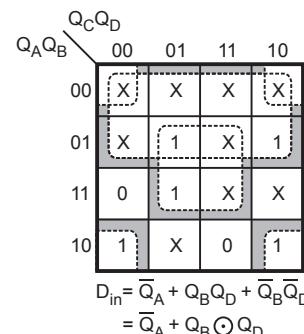


Fig. 7.3.5 (a)

Logic diagram

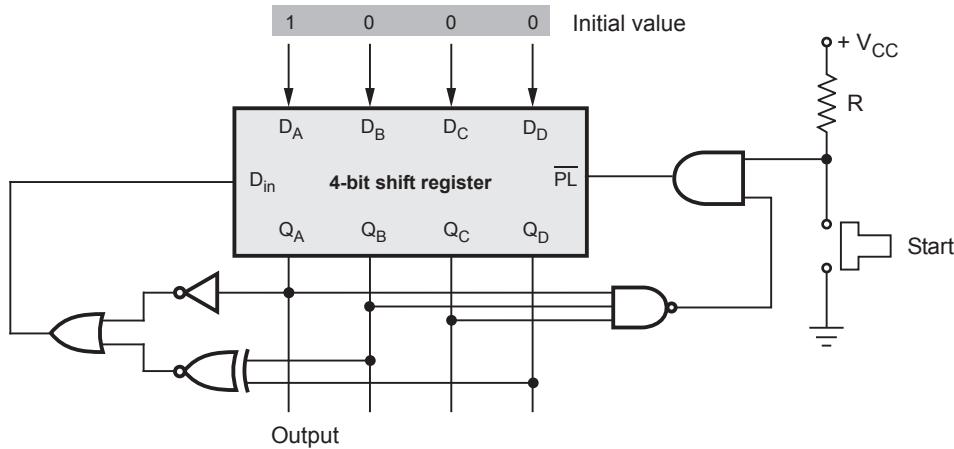


Fig. 7.3.5 (b)

Example 7.3.5 Design and implement the following sequence generator using shift register
1010

SPPU : Dec.-06, May-18, Marks 4

Solution : Here the sequence is 10 and it is repeated. Thus the length of the sequence $N = 2$. Let the number of flip-flops required n be.

$$N \leq 2^n - 1$$

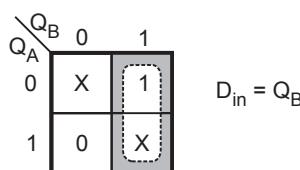
$$2 \leq 2^n - 1$$

$$\therefore n = 2$$

CP	Flip-flop outputs		D _{in}	States
	Q _A	Q _B		
1	1	0	0	2
2	0	1	1	1
1	1	0	0	2

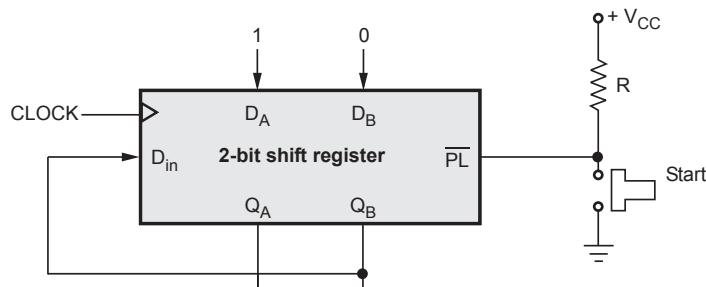
Fig. 7.3.6

K-map simplification for D_{in}



(a)

Logic diagram



(b)

Fig. 7.3.6

In the above circuit preset/parallel load logic is only required to load the initial value. After completion of one sequence, the shift register have the same initial value and hence it is not required to reload again.

Example 7.3.6 Design a pulse train generator using shift register for the following pulse train.

.....1 1 1 0 1 0

SPPU : May-2000, 02, Marks 8

Solution : The minimum number of flip-flops n can be given as

$$N \leq 2^n - 1$$

Here $N = 6$, therefore $n = 3$. The Table 7.3.5 shows sequence generation with three flip-flops.

CP	Flip-flop outputs			D _{in}	Preset	States
	Q _A	Q _B	Q _C			
1	1	0	0	1	1	4
2	1	1	0	1	1	6
3	1	1	1	0	1	7
4	0	1	1	1	1	3
5	1	0	1	0	1	5
6	0	1	0	0	1	2
Preset flip-flop	7	0	0	1	X	0
	1	1	0	0	1	4

Table 7.3.5

K-map simplification for D_{in}

$$\begin{aligned} D_{in} &= \bar{Q}_A Q_C + Q_A \bar{Q}_C \\ &= Q_A \oplus Q_C \end{aligned}$$

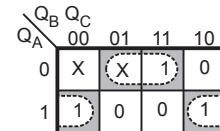


Fig. 7.3.7 (a)

Logic diagram

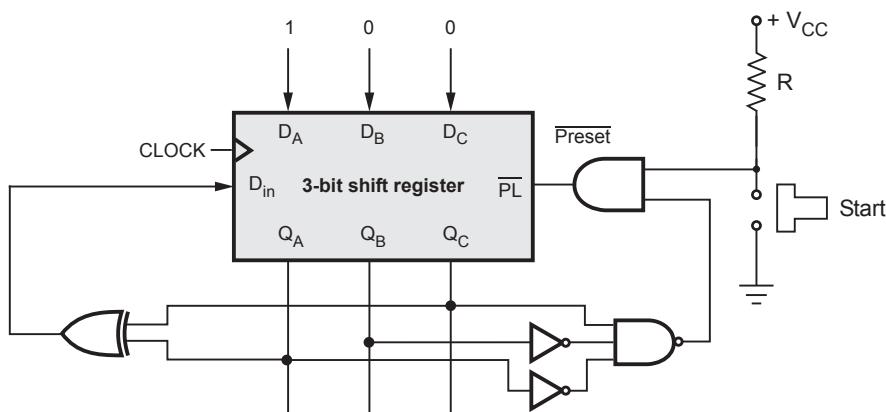


Fig. 7.3.7 (b)

Example 7.3.7 Design a pulse train generator circuit using shift register for the following pulse train.

..... 1 0 0 0 1 1 0

SPPU : Dec.-08, May-12, Marks 8

Solution : The minimum number of flip-flops n , required to generate sequence of length N is given by

$$N \leq 2^n - 1$$

Here, $N = 7$, therefore $n = 3$. The Table 7.3.6 (a) shows sequence generation with three flip-flops.

CP	Flip-flop outputs			D_{in}	States
	Q_A	Q_B	Q_C		
1	1	1	1	0	7
2	0	1	1	0	3
3	0	0	1	0	1
4	0	0	0	1	0
5	1	0	0	1	4
6	1	1	0	0	6
State is repeated	7	0	1	—	3

Table 7.3.6 (a)

As seventh state is repeated, $n = 3$ is not sufficient. Let us try with 4 flip-flops. The Table 7.3.6 (b) shows sequence generation with four flip-flops.

CP	Flip-flop outputs				D_{in}	$\overline{\text{Preset}}$	States
	Q_A	Q_B	Q_C	Q_D			
1	1	1	1	1	0	1	15
2	0	1	1	1	0	1	7
3	0	0	1	1	0	1	3
4	0	0	0	1	1	1	1
5	1	0	0	1	1	1	9
6	1	1	0	0	0	1	12
7	0	1	1	0	1	1	6
Preset flip-flop	1	1	0	1	1	0	11
	1	1	1	1	0	1	15

Table 7.3.6 (b)

K-map simplification for D_{in}

$$\therefore D_{in} = \overline{Q_A} \overline{Q_C} + Q_A \overline{Q_B} + Q_C \overline{Q_D}$$

$Q_A Q_B$	00	01	11	10
$Q_C Q_D$	00	1	0	X
00	X	X	0	1
01	X	X	0	1
11	0	X	0	X
10	X	1	X	X

Logic diagram

Fig. 7.3.8

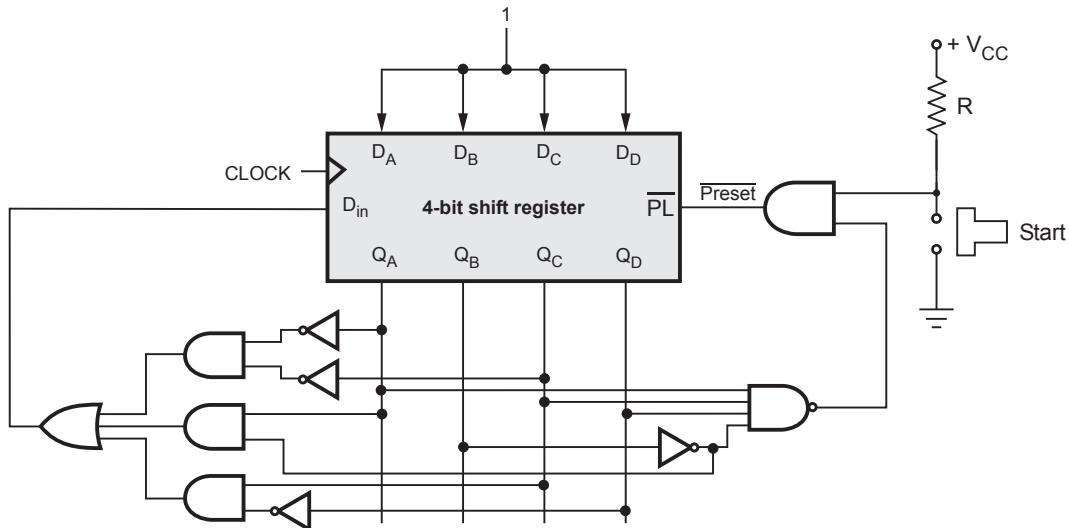


Fig. 7.3.9

Example 7.3.8 Design sequence generator using shift register to generate sequence 1101.

SPPU : Dec.-07, Marks 4

Solution : The minimum number of flip-flops n can be given as

$$N \leq 2^n - 1$$

Here $N = 4$, therefore $n = 3$. The Table 7.3.7 shows sequence generation with three flip-flops.

Preset flip-flop

CP	Flip-flop inputs			D_{in}	\overline{PL}	State s
	Q_A	Q_B	Q_C			
1	1	0	0	1	1	4
2	1	1	0	0	1	6
3	0	1	1	1	1	3
4	1	0	1	0	1	5
5	0	1	0	×	0	2
1	1	0	0	1	1	4

Table 7.3.7

K-map simplification for D_{in}

		$Q_B Q_C$		00	01	11	10
		0	1	X	X	1	X
Q_A	0	1	X	0	X	0	
	1						

$$D_{in} = \overline{Q}_B \overline{Q}_C + \overline{Q}_A$$

Fig. 7.3.10 (a)

Logic diagram

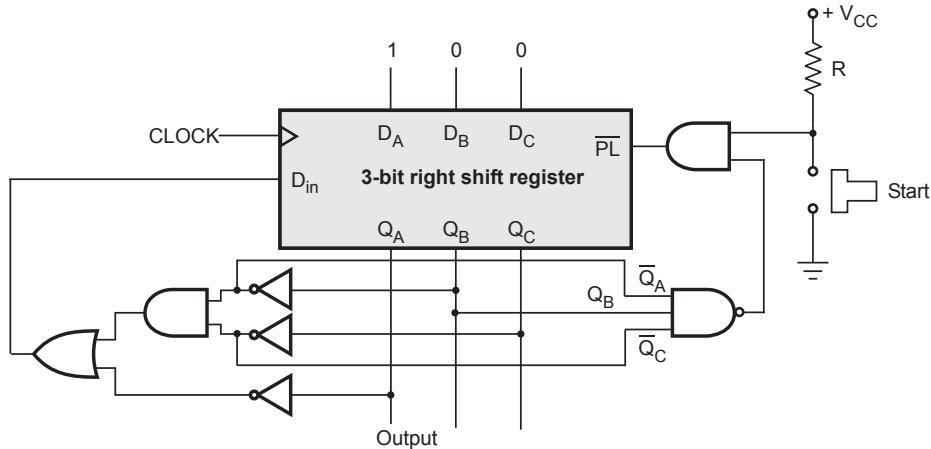


Fig. 7.3.10 (b)

Example for Practice

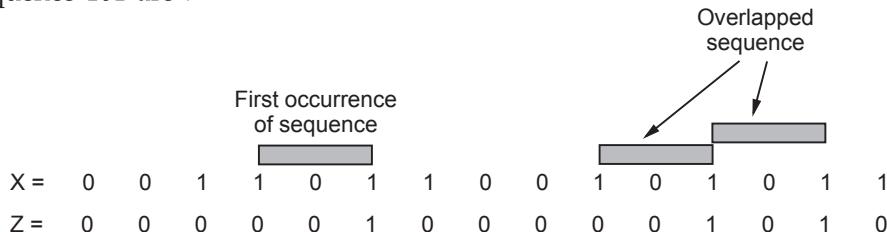
Example 7.3.9 Design pulse train generator using shift register to generate the following pulse
..... 10110.....

SPPU : Dec.-12,13, Marks 8

7.4 Sequence Detector

SPPU : May-06,07,10,12,13,14, Dec.-05,06,07,08,10,12,13,15,16

The specified input sequence can be detected using a sequential machine called **sequence detector**. In this circuit output goes high when a prescribed input sequence occurs. A typical input sequence and the corresponding output sequence for desired input sequence 101 are :



As shown above the detection of required input sequence can occur in a longer data string and the desired input sequence can overlap with another input sequence. It is assumed that input can change only between clock pulses. Once we know the sequence which is to be detected, we can draw the state diagram for it. Then from the state diagram we can design the circuit. It is possible to implement sequence detector using both types of sequential machines : Mealy machine and Moore machine. The following examples illustrate how to determine the state diagram from the given input sequence and then implement the sequence detector.

Illustrative Examples

Example 7.4.1 Design a Mealy type sequence detector to detect a serial input sequence of 101.

SPPU : Dec.-13, Marks 6

Solution : In a Mealy type design, the number of states in the state diagram are equal to the number of bits in the desired input sequence. In this example, we have three bits in the sequence so we have three states in the state diagram. Once the number of states are known we have to draw the direction lines with states of inputs and outputs. Let us start drawing direction lines, assuming state 'a' as an initial state.

1. State a

State a checks for 1. When input is 1, we have detected the first bit in the sequence, hence we have to go to the next state to detect the next bit in the sequence.

When input is 0, we have to remain in the state 'a' because bit 0 is not the first bit in the sequence. In both cases output is 0 since we have not yet detected all the bits in the sequence.

2. State b

When input is 0, we have detected the second bit in the sequence, hence we have to go to the next state to detect the next bit in the sequence. When input is 1, we have to remain in state b because 1 which we have detected may start the sequence. Output is still zero.

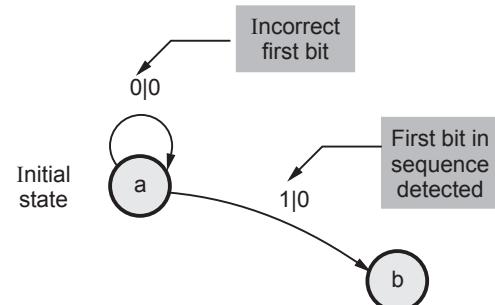


Fig. 7.4.1 (a)

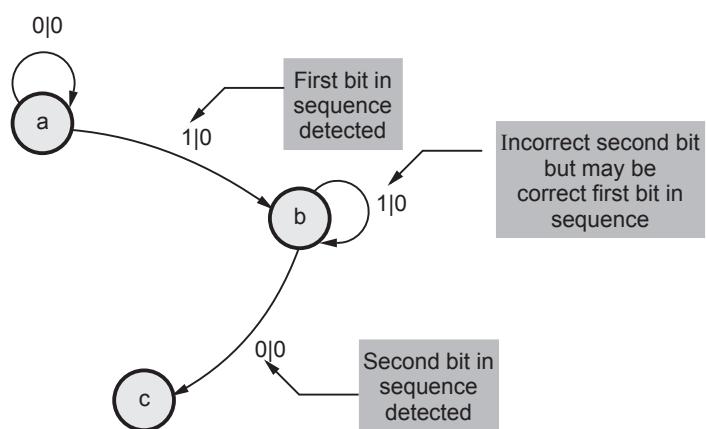


Fig. 7.4.1 (b)

3. State c

As explained for state a and state b, if desired bit is detected we have to go for next state otherwise we have to go to the previous state from where we can continue the desired sequence. When complete sequence is detected we have to make output HIGH and go to the initial state. This is illustrated in Fig. 7.4.1 (c).

From the above state diagram we can determine the state table as shown in Table 7.4.1 (a).

Present state	Next state		Output	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
a	a	b	0	0
b	c	b	0	0
c	a	b	0	1

Table 7.4.1 (a) State table

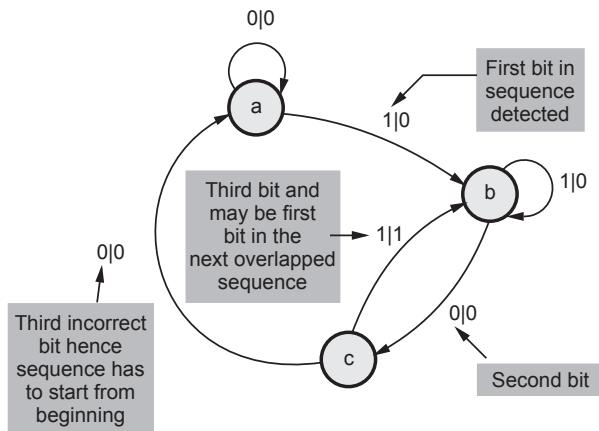


Fig. 7.4.1 (c)

Present state	Next state		Output Z					
	A	B	A^+	B^+	$X = 0$	$X = 1$	$X = 0$	$X = 1$
a	0	0	0	0	0	1	0	0
b	0	1	1	0	0	1	0	0
c	1	0	0	0	0	1	0	1

Table 7.4.1 (b) Excitation table

Since there are three states we need two flip-flops. Assigning state a = 00, state b = 01 and state c = 10 we can determine the excitation table as shown in Table 7.4.1 (b).

K-map simplification

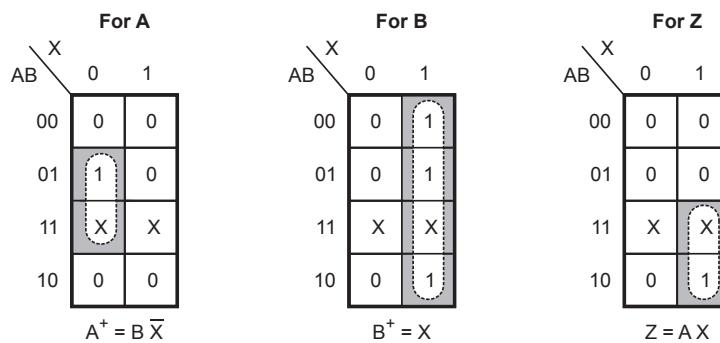


Fig. 7.4.2 (a)

Logic diagram

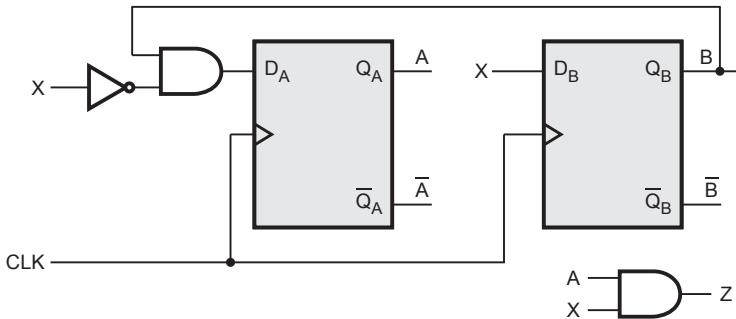


Fig. 7.4.2 (b)

Example 7.4.2 Design a Moore type sequence detector to detect a serial input sequence of 101.

SPPU : Dec.-13, Marks 6

Solution : In a Moore type design output depends only on flip-flop states. Therefore, in the state diagram of Moore machine, the output is written with the state instead of with the transition between the states. Apart from this the process of determining the state diagram is similar to that used for Mealy machine. Let us start with state 'a' as an initial state.

1. State a : When input is 1, we have detected the first bit in the sequence, hence we have to go to the next state to detect the next bit in the sequence.

When input is 0, we have to remain in the state 'a' because bit 0 is not the first bit in the sequence. In both cases output is 0 since we have not yet detected all the bits in the sequence.

2. State b : When input is 0, we have detected the second bit in the sequence, hence we have to go to the next state to detect the next bit in the sequence. When input is 1, we have to remain in state b because 1 which we have detected may start the sequence. Output is still zero.

3. State c : Now, when a 1 input occurs, the 101 sequence is completed and output must equal to 1. Here, we

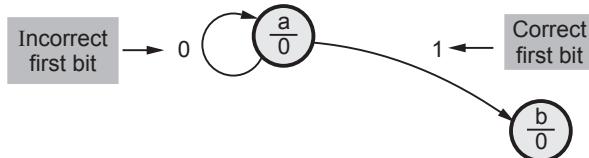


Fig. 7.4.3 (a)

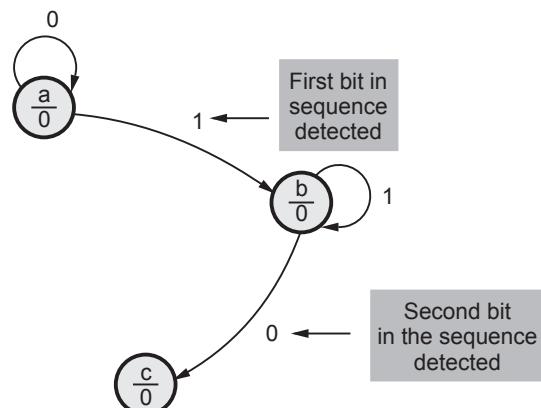


Fig. 7.4.3 (b)

cannot go back to state b (since output in state b is zero) and hence we have to create new state d with a output 1.

In case if input is zero, we have to restart checking of input sequence and hence we have to return to state a.

4. State d : Since the sequence is detected, this is the last state. When input is 1, we have detected the first bit in the next sequence, hence we have to go to state b.

When input is 0, we have detected the second bit in the overlapped sequence, hence we have to go to state c.

From the above state diagram we can determine the state table as shown in Table 7.4.2 (a).

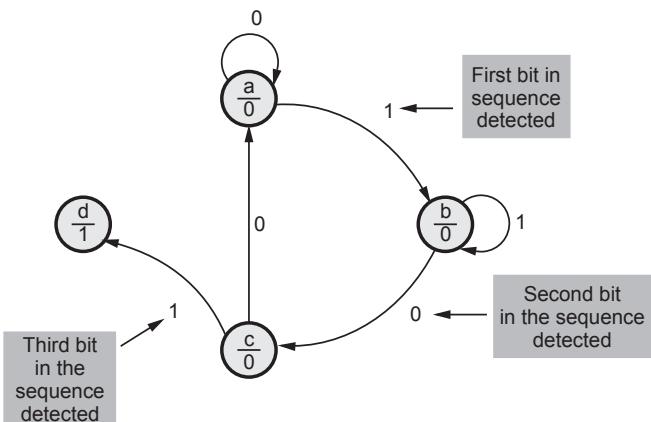


Fig. 7.4.3 (c)

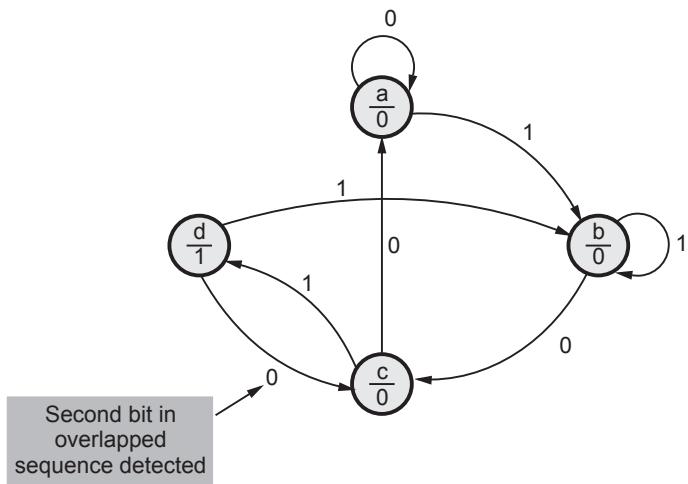


Fig. 7.4.3 (d)

Present state	Next state		Output Z
	X = 0	X = 1	
a	a	b	0
b	c	b	0
c	a	d	0
d	c	b	1

Table 7.4.2 (a) State table

Present state	Next state A ⁺ B ⁺		Output			
	A	B	X = 0	X = 1		
0	0	0	0	0	1	0
0	1	1	0	0	1	0
1	0	0	0	1	1	0
1	1	1	0	0	1	1

Table 7.4.2 (b) Excitation table

Since there are four states we need two flip-flops. Assigning state a = 00, b = 01, c = 10 and d = 11 we can determine the excitation table as shown in Table 7.4.2 (b).

K-map simplification

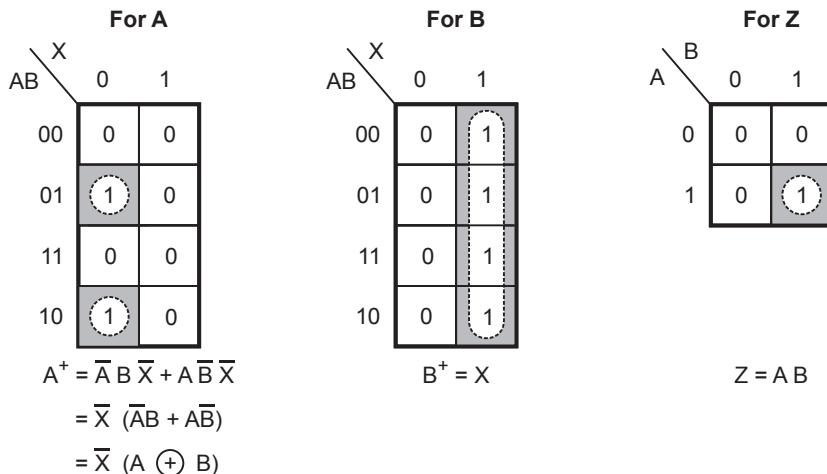


Fig. 7.4.4

Logic diagram

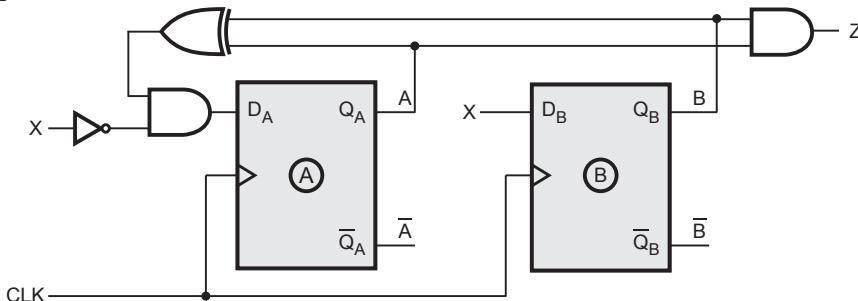


Fig. 7.4.5

Examples with Solutions

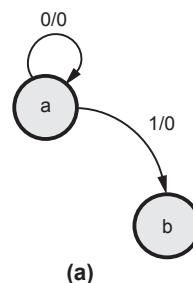
Example 7.4.3 Design a sequence detector to detect the following sequence using JK flip-flops.

(Use Mealy Machine) ... 110

SPPU : May-07,14, Dec.-08, Marks 4

Solution : The given sequence has 3-bit, so we require 3 states in the state diagram. Let us start drawing direction lines, assuming state 'a' is an initial state.

State a : When input is 1, we have detected the first bit in the sequence, hence we have to go to the next state to detect the next bit in the sequence. When input is 0, we have to remain in the state 'a' because bit 0 is not the first bit in the sequence. In both cases output is 0, since we have not yet detected all the bits in the sequence.



State b : When input is 1, we have detected the second bit in the sequence, hence we have to go to the next state to detect the next bit in the sequence. When input is 0, we have to go to the state 'a' to detect the first bit in the sequence, i.e. 1.

State c : When input is 0, we have detected the last bit in the sequence, hence we have to go to the initial state, to detect the next sequence and make output high indicating sequence is detected. When input is 1, we have to go to the state 'b' because 1 which we have detected may start the sequence.

Assuming state assignments as $a = 00$, $b = 01$ and $c = 10$, we can determine excitation table for above state diagram as shown in Table 7.4.3.

Input	Present state		Next state		Output	Flip-flop inputs				
	X	A_n	B_n	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B	
0	0	0	0	0	0	0	X	0	X	
0	0	1	0	0	0	0	X	X	1	
0	1	0	0	0	1	X	1	0	X	
1	0	0	0	1	0	0	X	1	X	
1	0	1	1	0	0	1	X	X	1	
1	1	0	0	1	0	X	1	1	X	

Table 7.4.3 Excitation table

K-map simplification

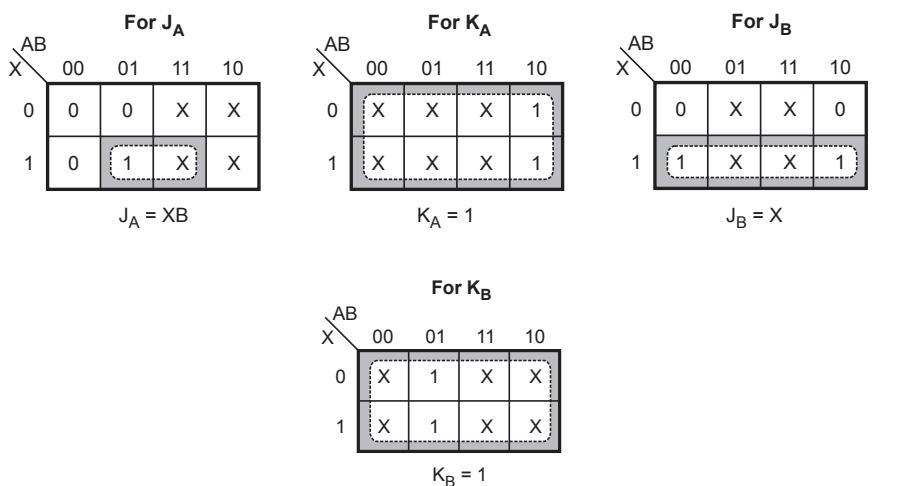


Fig. 7.4.7

Logic diagram

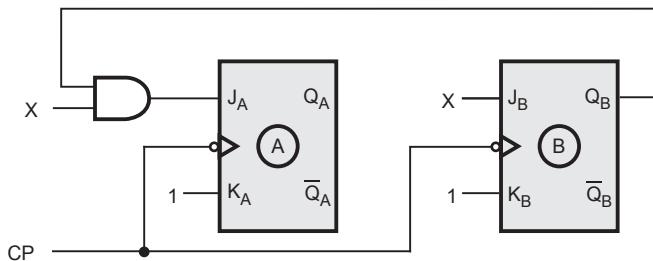


Fig. 7.4.8

Example 7.4.4 Design a sequence detector to detect sequence 1101. **SPPU : Dec.-07, Marks 8**

Solution : State diagram

In Moore model, output depends only on the present state and not on the input, so state diagram is as shown in the Fig. 6.4.9.

State table

Present state	Next state		Output
	X = 0	X = 1	
a	a	b	0
b	a	c	0
c	d	c	0
d	a	e	0
e	a	b	1

Table 7.4.4

State assignment

$$a = 000, \quad b = 001, \quad c = 010, \quad d = 011 \quad \text{and} \quad e = 100$$

State transition table

Present state	Input			Next state			Output	
	Q _A	Q _B	Q _C	X	Q _{A+}	Q _{B+}	Q _{C+}	
0 0 0				0	0	0	0	0
0 0 0				1	0	0	1	0
0 0 1				0	0	0	0	0
0 0 1				1	0	1	0	0

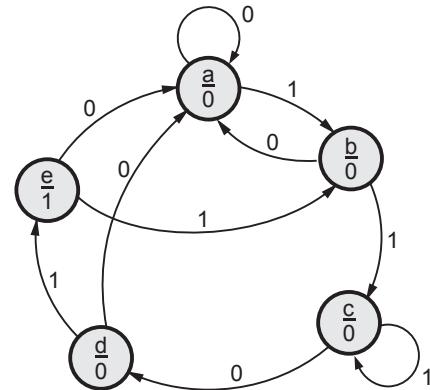


Fig. 7.4.9

0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	0
0	1	1	0	0	0	0	0
0	1	1	1	1	0	0	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	1	1
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

Table 7.4.5

K-map simplification

			For D_A				
		$Q_C X$	00	01	11	10	
Q_A	Q_B		00	0	0	0	0
00	00		0	0	0	0	0
01	01		0	0	1	0	0
11	X	X	X	X	X	X	X
10	01		0	0	X	X	X

$$D_A = Q_B Q_C X$$

			For D_B				
		$Q_C X$	00	01	11	10	
Q_A	Q_B		00	0	0	1	0
00	00		0	0	0	0	0
01	01		1	1	0	0	0
11	X	X	X	X	X	X	X
10	01		0	0	X	X	X

$$D_B = Q_B \bar{Q}_C + \bar{Q}_B Q_C X$$

			For D_C				
		$Q_C X$	00	01	11	10	
Q_A	Q_B		00	0	1	0	0
00	00		0	1	0	0	0
01	01		1	0	0	0	0
11	X	X	X	X	X	X	X
10	01		0	1	X	X	X

$$D_C = Q_B \bar{Q}_C \bar{X} + \bar{Q}_B \bar{Q}_C X$$

			For Y				
		$Q_C X$	00	01	11	10	
Q_A	Q_B		00	0	0	0	0
00	00		0	0	0	0	0
01	01		0	0	0	0	0
11	X	X	X	X	X	X	X
10	01		1	1	X	X	X

$$Y = Q_A$$

Fig. 7.4.10

Logic diagram

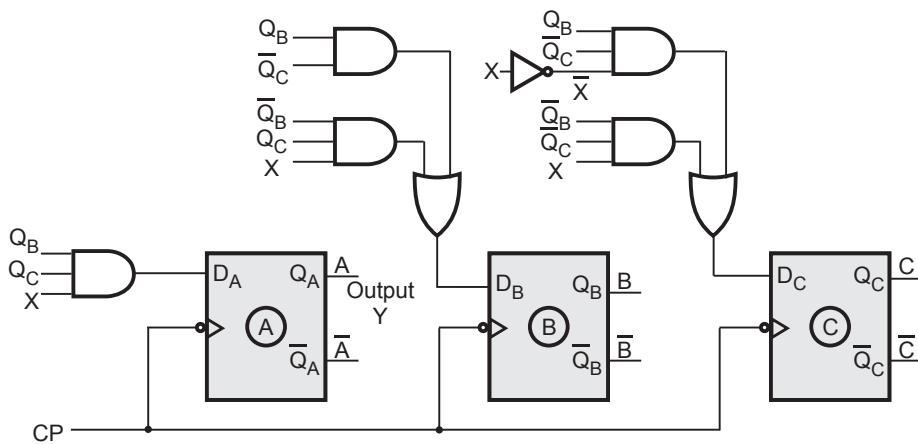


Fig. 7.4.11

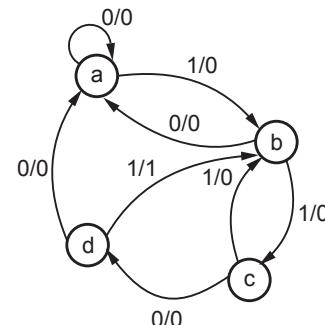
Example 7.4.5 Design a sequence detector using D-FFs to detect the following sequence based on Mealy machine : 1101.

SPPU : May-12, Marks 8

Solution : Sequence detector (1101) using mealy machine and D F/F :

State table :

Present state	Next state		Output Y	
	X = 0	X = 1		
a	a	b	0	0
b	a	c	0	0
c	d	b	0	0
d	a	b	0	1



Excitation table

Present state		Next State				Output	Y
		X = 0		X = 1			
Q_A	Q_B	Q_A ⁺	Q_B ⁺	Q_A ⁺	Q_B ⁺	X = 0	X = 1
0	0	0	0	0	1	0	0
0	1	0	0	1	0	0	0
1	0	1	1	0	1	0	0
1	1	0	0	0	1	0	1

K-map simplification

		For D_A				
		AB	00	01	11	10
X	0	0	0	0	1	
	1	0	1	0	0	

$$D_A = Q_A \bar{Q}_B \bar{X} + \bar{Q}_A Q_B X$$

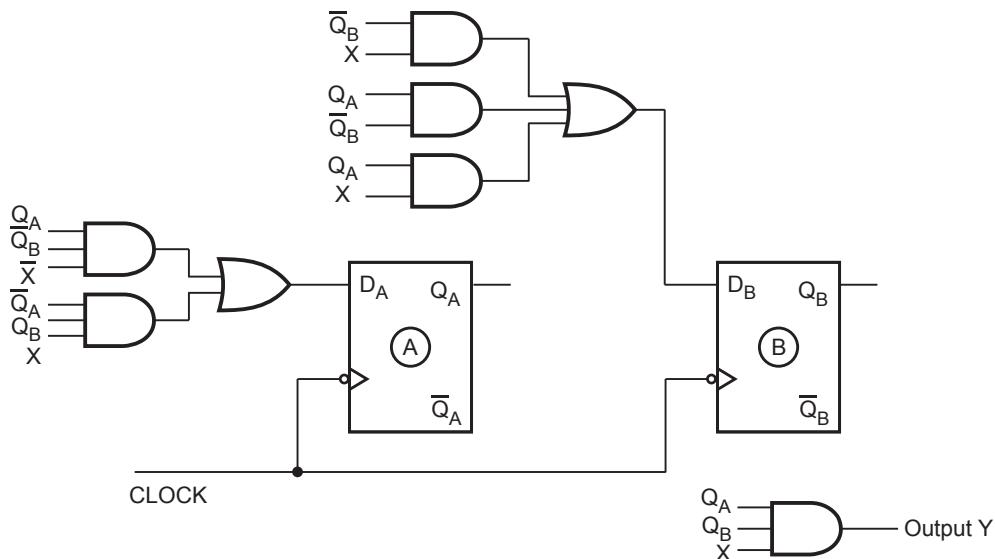
		For D_B				
		AB	00	01	11	10
X	0	0	0	0	1	
	1	1	0	1	1	

$$D_B = \bar{Q}_B X + Q_A X \bar{Q}_A \bar{Q}_B$$

		For Output Y				
		AB	00	01	11	10
X	0	0	0	0	0	
	1	0	0	1	0	

$$D_B = Q_A Q_B X$$

Implementation



Example 7.4.6 Design a sequential circuit using Mealy machine for detecting the sequence 1011.....

Use JK flip-flop.

SPPU : Dec.-12, Marks 8

Solution : State diagram

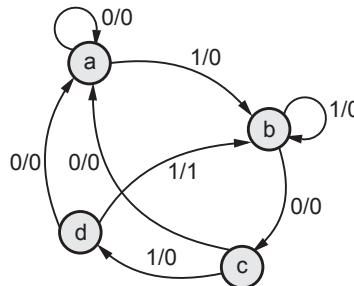


Fig. 7.4.12

State Table :

Input X	Present State		Next State		Output Y	Flip-flop inputs			
	A	B	A_+	B_+		J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	1	1	0	0	1	X	X	1
0	1	0	0	0	0	x	1	0	X
0	1	1	0	0	0	x	1	X	1
1	0	0	0	1	0	0	X	1	X
1	0	1	0	1	0	0	X	X	0
1	1	0	1	1	0	X	0	1	X
1	1	1	0	1	1	X	1	X	0

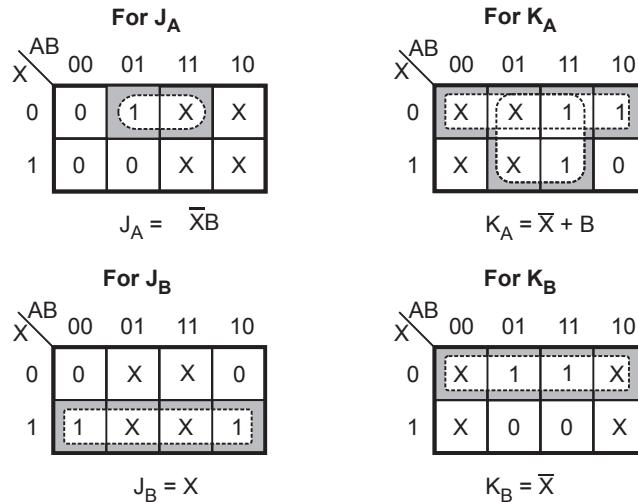
K-map Simplification

Fig. 7.4.13

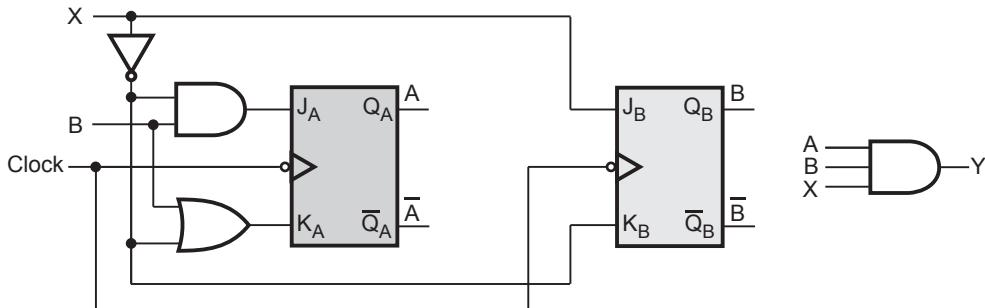
Logic diagram

Fig. 7.4.14

Example 7.4.7 Design a SEQUENCE DETECTOR using JK-flip-flops to detect the following sequence

..... 1 0 0 1

Use state diagram, state transition tables and K-map as design tools. Remove all redundant states and draw the final circuit diagram.

SPPU : Dec.-05.15, Marks 12

Solution : State table :

Present State	Next state		Output	
	X = 0	X = 1	X = 0	X = 1
a	a	b	0	0
b	c	b	0	0
c	d	b	0	0
d	a	b	0	1

Let a = 00, b = 01, c = 10 and d = 11

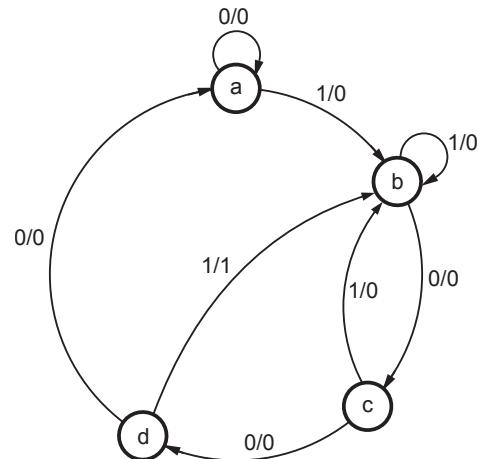
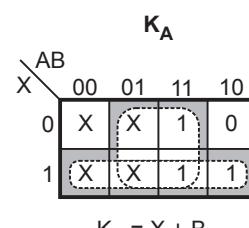
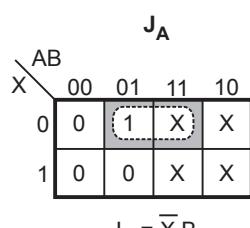


Fig. 7.4.15

Input	Present state		Next state		Flip-flop inputs				
	X	A	B	A ⁺	B ⁺	J _A	K _A	J _B	K _B
0	0	0	0	0	0	0	X	0	X
0	0	1	1	1	0	1	X	X	1
0	1	0	1	1	1	X	0	1	X
0	1	1	0	0	0	X	1	X	1
1	0	0	0	0	1	0	X	1	X
1	0	1	0	0	1	0	X	X	0
1	1	0	0	0	1	X	1	1	X
1	1	1	0	0	1	X	1	X	0

K-map simplification



		J _B						K _B					
		AB	00	01	11	10			AB	00	01	11	10
X	A	0	0	X	X	1	X	A	0	X	1	1	X
		1	1	X	X	1			1	X	0	0	X

$J_B = X + A$ $K_B = \bar{X}$

		J _B						K _B					
		AB	00	01	11	10			AB	00	01	11	10
X	A	0	0	0	0	0	X	A	0	0	0	0	0
		1	0	0	1	0			1	X	0	0	X

Output = XAB

Logic diagram :

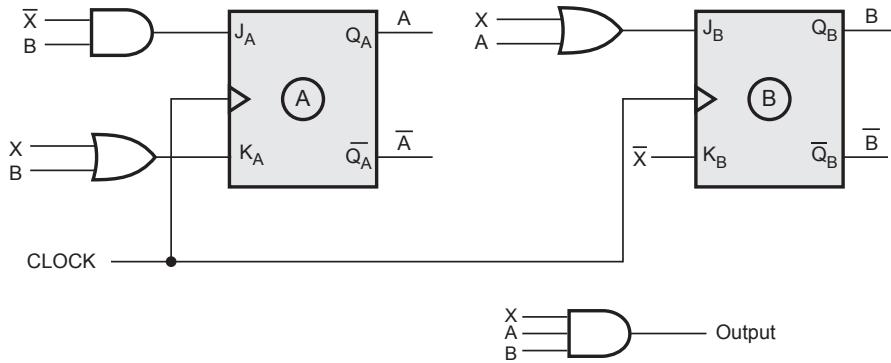


Fig. 7.4.16

Example 7.4.8 Design SEQUENCE DETECTOR using JK flip-flops to detect the following sequence :1 1 1....

Use state diagram, state transition tables and K-map as design tools. Remove all redundant states and draw the final circuit diagram.

SPPU : May-06, Marks 12

Solution : State assignment :

State name	Binary state
a	0 0
b	0 1
c	1 0

State diagram :

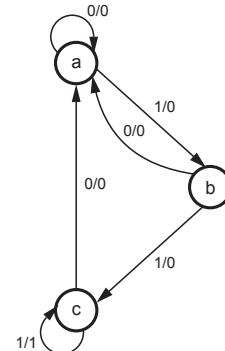


Fig. 7.4.17

State Transition Table :

Present State		I/P	Next State		O/P
A	B	X	A+	B+	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	0	1

Excitation Table of JK flip-flop

Q o/p	Next state	I/P	
		J	K
Present state			
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table of our circuit :

Present State	I/P	Next state	Flip-flop I/Ps								
			A	B	X	A+	B+	J _A	K _A	J _B	K _B
0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0	X	1	X	
0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	1	X	X	1	
1	0	0	0	0	0	0	0	0	0	0	0

K-map

For J _A					
A	BX	00	01	11	10
0	0	0	1	0	
1	0	X	X	X	X

$$\therefore J_A = BX$$

For K _A					
A	BX	00	01	11	10
0	0	0	X	X	0
1	0	0	0	X	X

$$K_A = 0$$

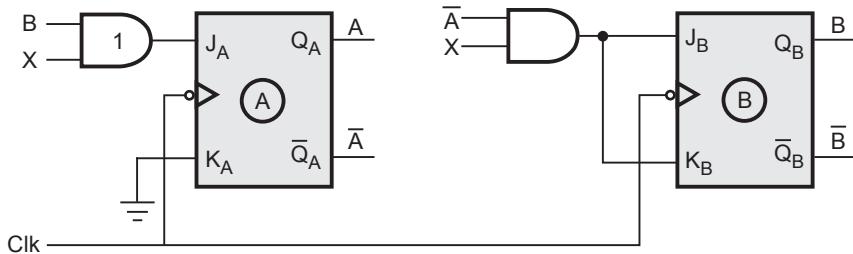
For J _B					
A	BX	00	01	11	10
0	0	1	X		
1	0	0	X	X	X

$$J_B = \bar{A}X$$

For K _B					
A	BX	00	01	11	10
0	0	X	1		
1	0	X	X	X	X

$$K_B = \bar{A}X$$

Fig. 7.4.18

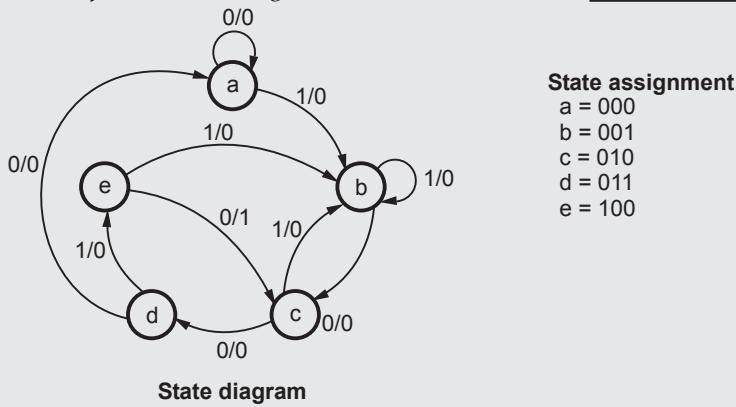
Logic Diagram**Fig. 7.4.19**

Example 7.4.9 Design a SEQUENCE DETECTOR using JK flip-flops to detect the following sequence :

----- 10010 -----

Use state diagram, state transition tables and K-map as design tools. Remove all redundant states and draw the final circuit diagram.

SPPU : Dec.-06, Marks 12

**Fig. 7.4.20****Solution :**

Input	Present state			Next state			Output	Flip-Flop Inputs						
	X	A	B	C	A ₊	B ₊	C ₊	J _A	K _A	J _B	K _B	J _C	K _C	
0	0	0	0	0	0	0	0	0	0	X	0	X	0	X
0	0	0	1	0	0	1	0	0	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	0	X	X	0	1	X
0	0	1	1	0	0	0	0	0	0	X	X	1	X	1
0	1	0	0	0	0	1	0	1	X	1	1	X	0	X
1	0	0	0	0	0	0	1	0	0	X	0	X	1	X
1	0	0	1	0	0	0	1	0	0	X	0	X	X	0
1	0	1	0	0	0	0	1	0	0	X	X	1	1	X
1	0	1	1	0	1	0	0	0	1	X	X	1	X	1
1	1	0	0	0	0	0	1	0	X	1	0	X	1	X

		For J_A						For K_A							
		XA	BC	00	01	11	10	XA	BC	00	01	11	10	XA	BC
		00	00	0	0	0	0	00	00	X	X	X	X	00	00
		01	X	4	5	X	X	01	1	4	X	5	X	01	1
		11	X	12	X	X	15	11	11	12	X	13	X	11	12
		10	0	8	9	1	10	10	8	X	X	9	X	11	10
		$J_A = XBC$				$K_A = \bar{B}$				$K_B = C + X$				$K_C = \bar{X} + B$	
		For J_B						For K_B							
		XA	BC	00	01	11	10	XA	BC	00	01	11	10	XA	BC
		00	00	0	1	X	X	00	X	0	X	1	0	00	00
		01	1	4	5	X	X	01	X	4	X	5	X	01	X
		11	0	12	X	X	14	11	X	12	X	13	X	11	X
		10	0	8	9	X	10	10	X	8	X	9	1	11	10
		$J_B = \bar{X}A + \bar{X}C$				$K_B = C + X$				$K_C = \bar{X} + B$					
		For J_C						For K_C							
		XA	BC	00	01	11	10	XA	BC	00	01	11	10	XA	BC
		00	00	0	X	1	X	00	X	0	1	1	0	00	00
		01	0	4	X	5	X	01	X	4	X	5	X	01	X
		11	1	12	X	X	14	11	X	12	X	13	X	11	X
		10	1	8	X	X	10	10	X	8	0	1	11	X	10
		$J_C = X + B$				$K_C = \bar{X} + B$				$Y = \bar{X}A$					
		For Y													
		XA	BC	00	01	11	10								
		00	00	0	0	0	0								
		01	1	4	X	X	X								
		11	0	12	X	X	X								
		10	0	8	9	0	10								
		$Y = \bar{X}A$													

Fig. 7.4.21

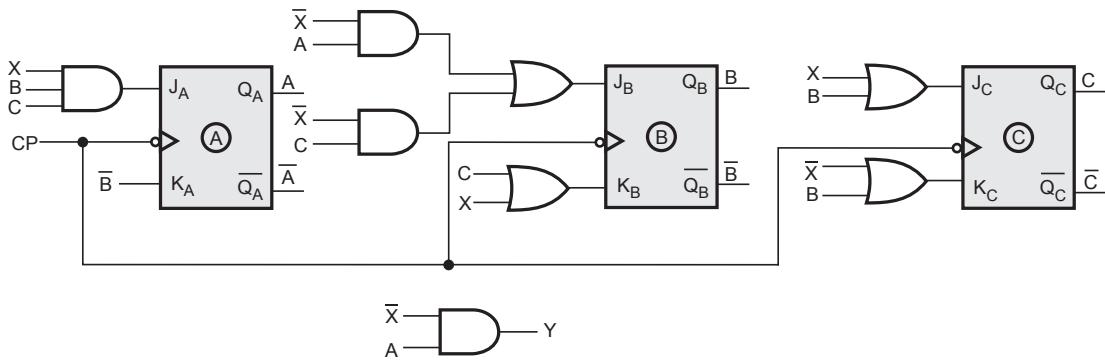


Fig. 7.4.22

Examples for Practice

Example 7.4.10 Design a sequential circuit using Mealy machine for detecting overlapping sequence 1101. Use JK flip-flops. **SPPU : May-10, Dec.-16, Marks 8**

(Ans. : Refer example 7.4.3 and apply similar procedure.)

Example 7.4.11 Design a sequence detector to detect a sequence 1101 (Using D FF and Mealy circuit). **SPPU : Dec.-10, Marks 8**

(Ans. : Refer similar example 7.4.1)

Example 7.4.12 Design and implement 1011 sequence detector using Mealy machine.

(Ans. : Refer example 7.4.3 and apply similar procedure.)

Example 7.4.13 Design a sequential circuit using Mealy machine for detecting the sequence ... 1001... Use JK Flip-flop **SPPU : May-13, Marks 10**

(Ans. : Refer example 7.4.3 and apply similar procedure.)



Notes

UNIT - IV

8

Algorithmic State Machines

Syllabus

Finite State Machines (FSM) and ASM, ASM charts, notations, construction of ASM chart and realization for sequential circuits.

Contents

8.1	<i>Introduction</i>	<i>Dec.-08,10,11,13,15,16, May-09,11,12,13,15,16,18,19,</i>	<i>Marks 8</i>
8.2	<i>Design of Simple Controller</i>	<i>Dec.-08,15, May-09,11,12,13,19,</i>	<i>Marks 8</i>
8.3	<i>ASM Examples : Sequence Generator, Types of Counters</i>	<i>Dec.-98,06,11,12,13,16,17,18,19, May-2000,05,06,07,08,12,14,16,17</i>	<i>Marks 16</i>

8.1 Introduction**SPPU : Dec.-08,10,11,13,15,16, May-09,11,12,13,15,16,18,19**

The main components of digital system are : Control logic and datapath. The relationship between these two is shown in the Fig. 8.1.1. The data processing path, commonly known as a **datapath**, manipulates data in registers according to system's requirements. The control logic initiates a sequence of commands to the datapath. It uses status conditions from the datapath as decision variables for determining the sequence of control signals.

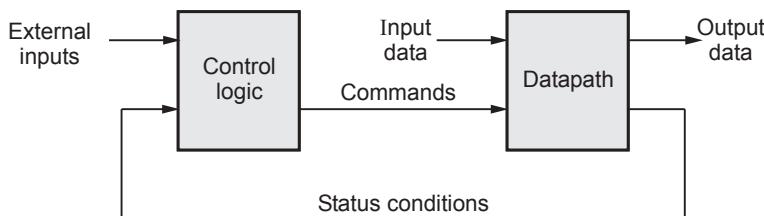


Fig. 8.1.1 Interaction between control logic and datapath

The control sequence and datapath tasks of a digital system are specified by means of a hardware algorithm. A hardware algorithm is a step-by-step procedure to implement the desired task with a selected circuit components. We know that, a flow chart is a convenient way to specify the sequence of procedural steps and decision paths for an algorithm. A special flowchart that has been developed specifically to define digital hardware algorithms is called an **Algorithmic State Machine** (ASM) chart. A state machine is another term used for sequential circuit.

The ASM chart resembles a conventional flow chart, but is interpreted somewhat differently. A conventional flow chart describes the sequence of procedural steps and decision paths for an algorithm without concern for their time relationship. An ASM chart describes the sequence of events as well as the timing relationship between the states of a sequential controller and the events that occur while going from one state to the next.

8.1.1 ASM Symbols / Notations

An ASM chart consists of three basic elements : The state box, the decision box, and the conditional box.

State box : A state in the control sequence is indicated by a state box, as shown in the Fig. 8.1.2.

As shown in the Fig. 8.1.2, rectangle shape is used to represent state box. (At the left of this box is the name of the state, such as A, B, Q₀, Q₂. On the right hand top corner of the box is a list of the flip-flop values that define that state. The circuit outputs that can occur whenever the circuit is in the corresponding state regardless of input values

are listed within the box.) Finally, a line drawn from state box, known as exit, indicates the path to the next state.

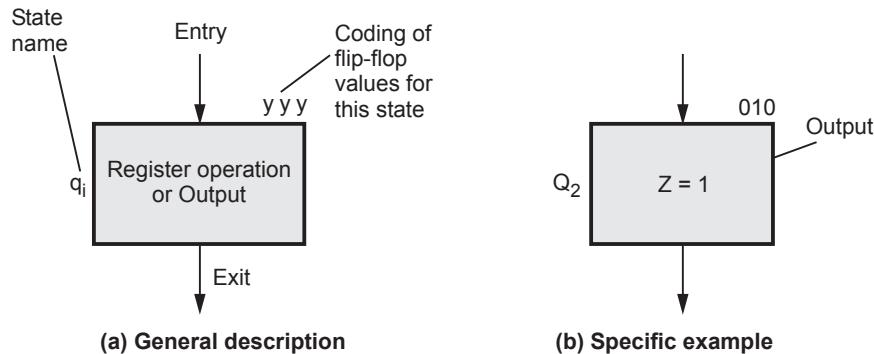


Fig. 8.1.2 State box

Decision box : The decision box describes the effect of an input on the control subsystem. It has a diamond shape box with two or more exit paths, as shown in the Fig. 8.1.3. The input condition to be tested is written inside the diamond box. Each value either 0 or 1 that may be assumed by an input or expression in a diamond is associated with an exit path from that diamond. These paths lead to the blocks corresponding to the next states of the circuit following the next clock pulse.

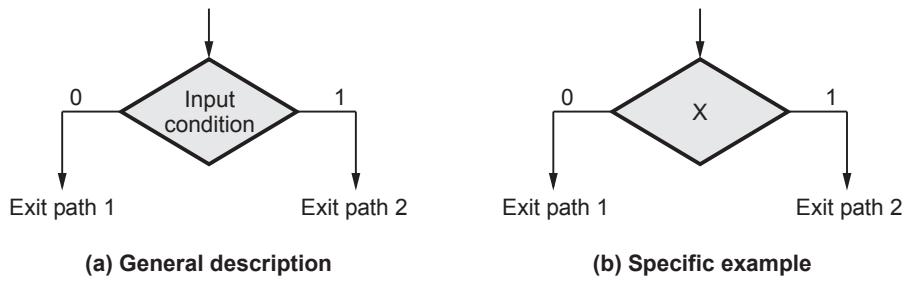


Fig. 8.1.3 Decision box

Conditional box : The state and decision boxes are familiar from use in conventional flowcharts. The third basic element, the conditional box, is unique to the ASM chart. It is an oval shape box. Its rounded corners differentiate it from the state box. The input path for the conditional box always comes from one of the exit paths of a decision box. The outputs that occur when the path to a conditional output box is satisfied are listed within the box.

The outputs that are not listed in either the state box or a conditional box in a particular ASM chart are always inactive when the circuit is in that state.

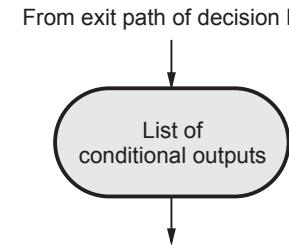


Fig. 8.1.4 Conditional box

Example 8.1.1 Draw the ASM chart for the following state diagram.

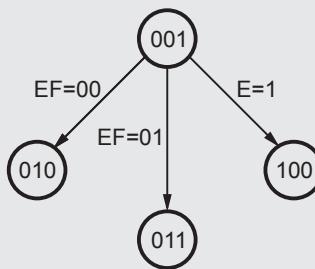


Fig. 8.1.5

Solution : ASM block : As shown in the Fig. 8.1.5 (a), an ASM block consists of one state box and all the conditional and decision boxes necessary to determine the path for next state box/boxes. It has one entrance and one or many exit paths. It describes the state of the system during one clock pulse interval.

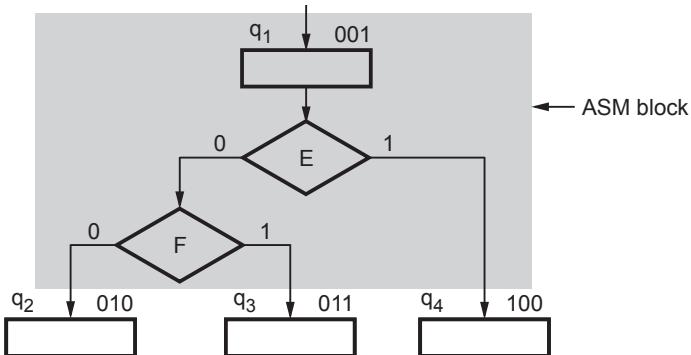


Fig. 8.1.5 (a)

8.1.2 Salient Features of ASM Chart

- An ASM chart describes the sequence of events as well as the timing relationship between the states of a sequential controller and the events that occur while going from one state to the next.
- Every block in an ASM chart specifies the operations that are to be performed during one common clock pulse.
- The operations specified within the state and conditional boxes in the block are performed in the datapath subsystem.
- The change from one state to next is performed in the control subsystem.
- An ASM chart consists of one or more interconnected blocks.
- An ASM block has one entrance and any number of exit paths represented by the structure of the decision boxes.
- Each block in the ASM chart describes the state of the system during one clock-pulse interval. When a digital system enters the state associated with a given ASM block, the outputs indicated within the state box becomes true. The conditions associated with the decision boxes are evaluated to determine which path or paths to be followed to enter into the next ASM block.

A **Link path** is a path through an ASM block from entrance to exit.

Review Questions

1. What is ASM chart ? **SPPU : Dec.-08,10,15,16, May-11,13,19, Marks 8**
2. How does ASM chart differ from conventional flowchart ? **SPPU : May-09,12, Marks 2**
3. List the features of ASM chart. **SPPU : May-12,15,16, Marks 4**
4. State and explain basic components of ASM chart. **SPPU : Dec.-11, May-13,15,16,18, Marks 6**
5. Mention application of ASM chart ? **SPPU : May-13, Dec.-15, Marks 2**
6. State and explain basic component of ASM chart. What is difference between ASM chart and conventional flow chart ? **SPPU : Dec.-13, Marks 7**

8.2 Design of Simple Controller

SPPU : Dec.-08,15, May-09,11,12,13,19

We have seen that, the control subsystem consists of sequential circuit. The process to implement the sequential circuit described by ASM charts consists of three steps :

- Translate the ASM chart to a state table.
 - Convert the state table to a transition table.
 - Develop Boolean expressions for circuit outputs and memory element inputs.
- Let us study these steps with an example.

Example 8.2.1 Develop an ASM chart and state table for a controllable waveform generator that will output any one of the four waveforms given in Fig. 8.2.1, as determined by the values of its two inputs x_1 and x_2 . The period of the first two waveforms is four clock cycles, the period of the third is three, and the period of the fourth waveform is two clock cycles, respectively. When an input change does occur, the new waveform may begin at any point in its period.

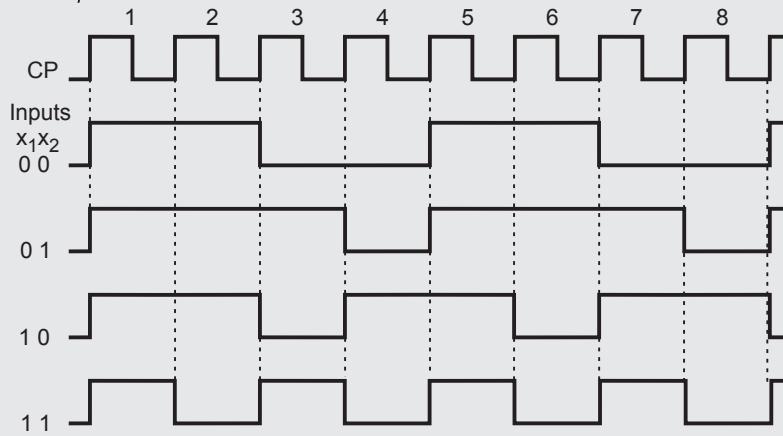


Fig. 8.2.1 Output waveforms

Solution : The ASM chart can be drawn for above waveform with four states, one for each clock cycle of the waveforms with the longest period. For each state the output will be conditional on the values of the input lines in effect at that time. Let us observe the different conditions at different states.

1. State Q_1 : In the first state, Q_1 , i.e. in the first clock cycle, all waveforms are at logic 1. Therefore, the output, $Z = 1$ and is listed in the state box for the first state, Q_1 .

2. State Q_2 : In the second state, Q_2 , i.e. in the second clock cycle, the output is 1 except for the waveform corresponding to inputs $x_1 x_2 = 11$. This condition can be tested by expression $x_1 \wedge x_2$ in the decision box. When the result of expression is 0, the inputs are other than $x_1 x_2 = 11$ and hence output $Z = 1$. This is represented by decision box and conditional box in state Q_2 .

3. State Q_3 : During the third state Q_3 , i.e. in the third clock pulse, the output will be 1, if $x_2 = 1$. The condition of x_2 is checked and accordingly output is made 1 by decision box and conditional box in state Q_3 . Looking at Fig. 8.2.2 we can realise that the output of third waveform in state Q_1 and state Q_4 is same, i.e. logic 1. In other words, in state Q_4 , the third waveform starts new cycle. Therefore, when $x_1 x_2 = 10$, the fourth state is not used and line goes back to first state to start the new cycle.

4. State Q_4 : In the fourth state Q_4 , i.e. in the fourth cycle, the output is always 0. From state Q_4 the circuit returns to Q_1 so that the waveforms may be repeated.

Let us express the ASM chart as a state table. We know that in the state tables we list the outputs along with the next states in the columns corresponding to each combination of input values. Fig. 8.2.3 shows state table for the ASM chart of waveform generator.

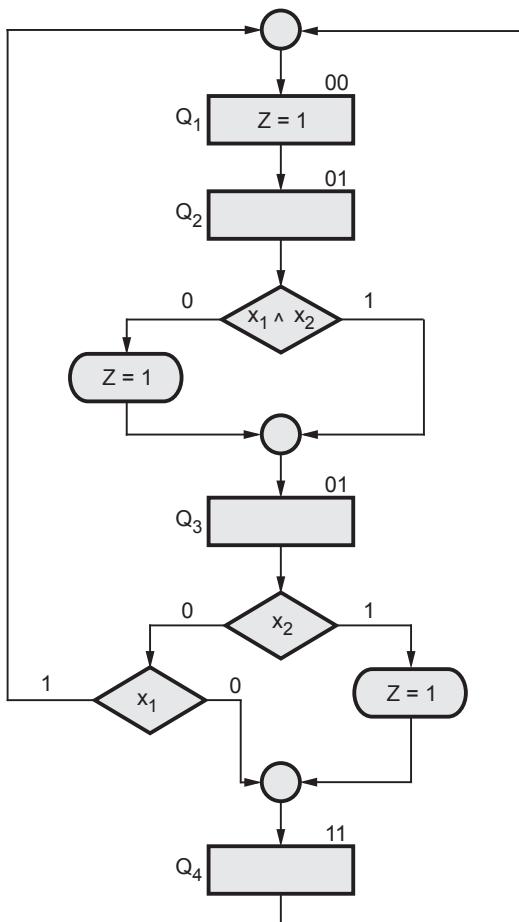


Fig. 8.2.2 ASM chart for waveform generator

Example 8.2.2 Determine the transition table for waveform generator from the state table given in Fig. 8.2.3.

Present state	x_1x_2			
	00	01	10	11
Q_1	$Q_2, 1$	$Q_2, 1$	$Q_2, 1$	$Q_2, 1$
Q_2	$Q_3, 1$	$Q_3, 1$	$Q_3, 1$	$Q_3, 0$
Q_3	$Q_4, 0$	$Q_4, 1$	$Q_1, 0$	$Q_4, 1$
Q_4	$Q_1, 0$	$Q_1, 0$	X	$Q_1, 0$

Fig. 8.2.3 State table

Solution : The state values for $Q_1 = 00$, $Q_2 = 01$, $Q_3 = 10$ and $Q_4 = 11$. Substituting these values in the state table we get transition table as shown in the Fig. 8.2.4.

Once the transition table is determined, the circuit can be realised by determining Boolean expressions for circuit outputs and memory element inputs.

Two methods are usually used for this purpose :

K-map simplification method

Multiplexer method

Present state	x_1x_2			
	00	01	10	11
00	01, 1	01, 1	01, 1	01, 1
01	10, 1	10, 1	10, 1	10, 0
10	11, 0	11, 1	00, 0	11, 1
11	00, 0	00, 0	X	00, 0

Fig. 8.2.4 Transition table

8.2.1 K-map Simplification Method

		Simplification for D_A				
		AB	00	01	11	10
AB	x_1x_2	00	0	0	0	0
		01	1	1	1	1
AB	x_1x_2	11	0	0	0	X
		10	1	1	1	0

$$D_A = \overline{AB} + A\overline{B}x_1 + A\overline{B}x_2$$

		Simplification for D_B				
		AB	00	01	11	10
AB	x_1x_2	00	1	1	1	1
		01	0	0	0	0
AB	x_1x_2	11	0	0	0	X
		10	1	1	1	0

$$D_B = \overline{A}\overline{B} + \overline{B}x_1 + \overline{B}x_2$$

		Simplification for Z				
		AB	00	01	11	10
AB	x_1x_2	00	1	1	1	1
		01	1	1	0	1
AB	x_1x_2	11	0	0	0	X
		10	0	1	1	0

$$Z = \overline{A}\overline{x}_1 + \overline{A}\overline{x}_2 + \overline{B}x_2$$

Fig. 8.2.5

We are familiar with the K-map simplification process. Let us find the Boolean expression for D_A , D_B (flip-flop inputs) and output Z using the transition table given in Fig. 8.2.5.

Logic diagram

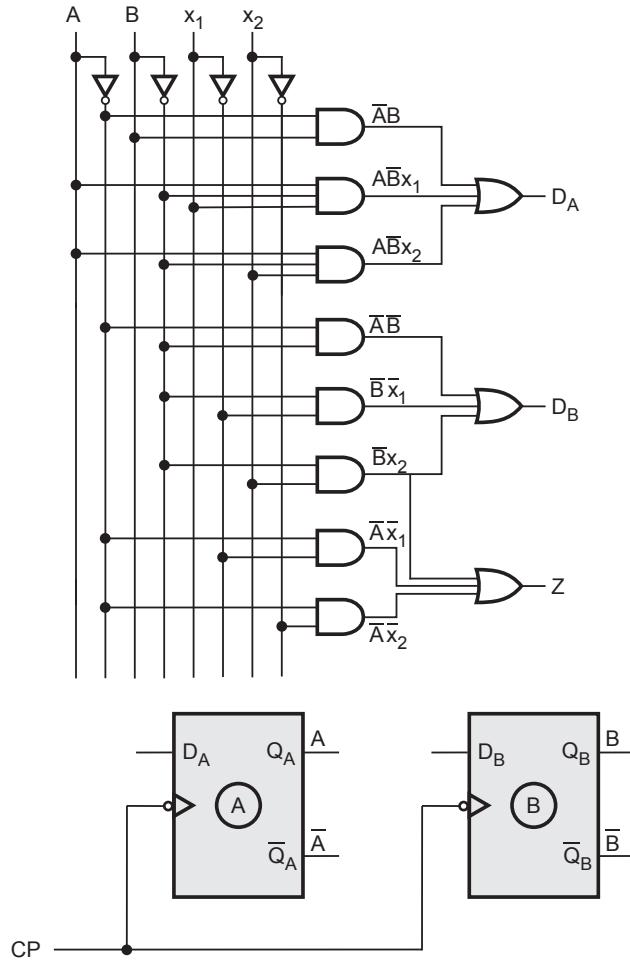


Fig. 8.2.6

8.2.2 Multiplexer Control Method

It is simpler and straight forward method for realisation of combinational circuit for any controller. In this method, the gates and flip-flops are replaced by multiplexers and registers, respectively. In this method there are three levels of components. The first level consists of multiplexers that determine the next state of the register. The second level contain a register that holds the present binary state. The third level has the decoder that provides a separate output for each control state. Sometimes combinational circuit is used in place of decoder.

Consider, for example, the ASM chart of Fig. 8.2.2. It consists of four state and two control inputs x_1 and x_2 . Fig. 8.2.7 shows three level implementation. It consists of two multiplexers, MUX 1 and MUX 2 ; a register with two flip-flops, A and B; and a combinational circuit to determine the output. The outputs of the register are used to select the inputs of the multiplexers. In this way, the present state of the register is used to select one of the inputs from each multiplexer. The outputs of the multiplexers are then applied to the D inputs of A and B. The purpose of each multiplexer is to produce an input to its corresponding flip-flop equal to the binary value of the next state.

The inputs of the multiplexers are determined from the decision boxes and state transitions given in the ASM charts (Refer Fig. 8.2.2). The present states, next states and conditions for transition can be tabulated for ASM chart given in Fig. 8.2.2, as shown in the Table 8.2.1.

No.	Present state		Next state		Condition of transition
1	(Q_1)	0	0	(Q_2)	0 1
2	(Q_2)	0	1	(Q_3)	1 0
3	(Q_3)	1	0	(Q_1)	0 0
				(Q_4)	1 1
4	(Q_4)	1	1	(Q_1)	0 0

Table 8.2.1

Inputs for Multiplexers

MUX 1	MUX 2
$0 \rightarrow 0$	$0 \rightarrow 1$
$1 \rightarrow 1$	$1 \rightarrow 0$
$2 \rightarrow \bar{x}_1 \bar{x}_2 + x_2$	$2 \rightarrow \bar{x}_1 \bar{x}_2 + x_2$
$3 \rightarrow 0$	$3 \rightarrow 0$

Table 8.2.2

Note MUX 1 generates input for flip-flop A and MUX 2 generates input for flip-flop B. The multiplexer input can be determined by including condition of transition corresponding to logic 1 bit position in the next state. Consider the transition from Q_1 to Q_2 . For flip-flop A the next state is 0, hence the corresponding input of multiplexer 1 is 0. For flip-flop B the next state is 1, hence the corresponding input of multiplexer 1 is the given condition of transition, i.e. 1.

Consider the transition from Q_3 to Q_1 or Q_4 . In this case, the next state for flip-flop A is 0 for Q_1 and 1 for Q_4 . Therefore, the condition of transition corresponding to Q_4 is taken as corresponding input of multiplexer 1 i.e. $\bar{x}_1 \bar{x}_2 + x_2$.

The equation for output Z can be directly derived from ASM chart. For this we have to observe the ASM chart and find the conditions when output is 1. For example, in state Q_1 , $Z = 1$ therefore Q_1 will appear in the equation for output Z. After collecting all the conditions where $Z = 1$ we get

$$Z = Q_1 + Q_2 \bar{x}_1 \bar{x}_2 + Q_3 x_2 = \bar{A} \bar{B} + \bar{A} B \bar{x}_1 \bar{x}_2 + A \bar{B} x_2$$

Logic diagram

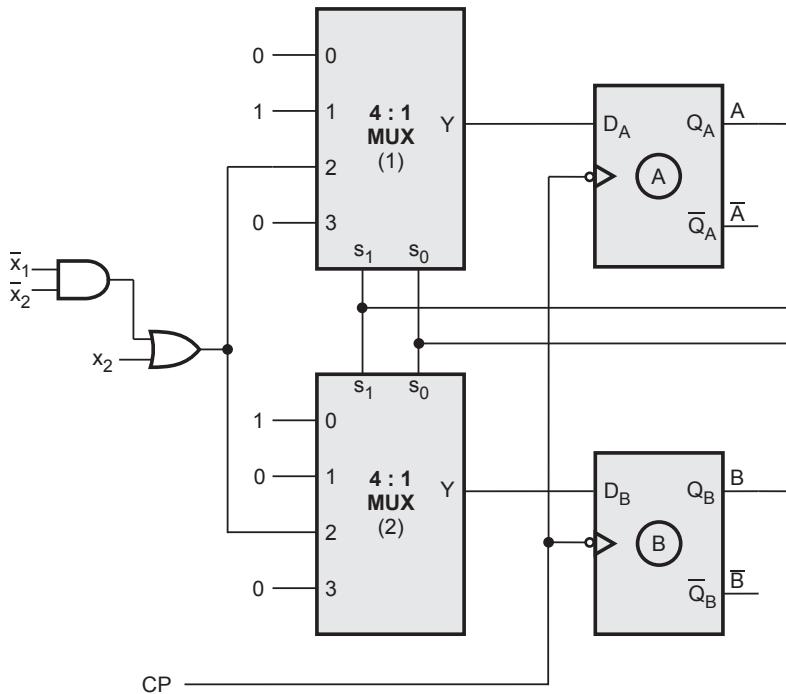


Fig. 8.2.7 (a)

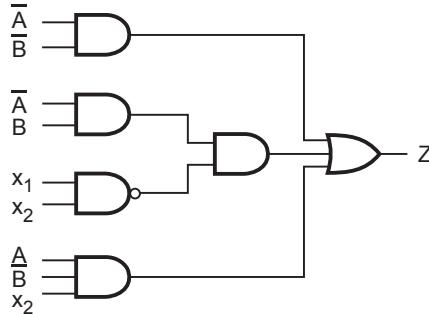


Fig. 8.2.7 (b)

Review Questions

1. Explain in detail, ASM technique of designing the sequential circuit.

SPPU : May-09,12, Marks 6

2. Explain the MUX controller method with the suitable example

SPPU : Dec.-08,15, May-11,19, Marks 8

3. What is ASM chart ? Design ASM chart for 3-bit octal number sequence with up-down conditions.

SPPU : May-11, Marks 8

4. Draw an ASM chart and state table for a sequential ring counter with suitable present state and conditional input.

SPPU : May-11, Marks 8

5. Draw an ASM chart for the 3-bit down counter having one enable line such that :
 $E = 1$ (counting enabled)
 $E = 0$ (counting disabled)
Also draw the state diagram.

SPPU : May-13, Marks 8

8.3 ASM Examples : Sequence Generator, Types of Counters

SPPU : Dec.-98,06,11,12,13,16,17,18,19, May-2000,05,06,07,08,12,14,16,17

Example 8.3.1 Draw an ASM chart for a 2-bit binary counter having enable line E such that : $E = 1$ (counting enabled) $E = 0$ (hold present count).

SPPU : Dec.-98,16,17,18, May-12, Marks 6

Solution :

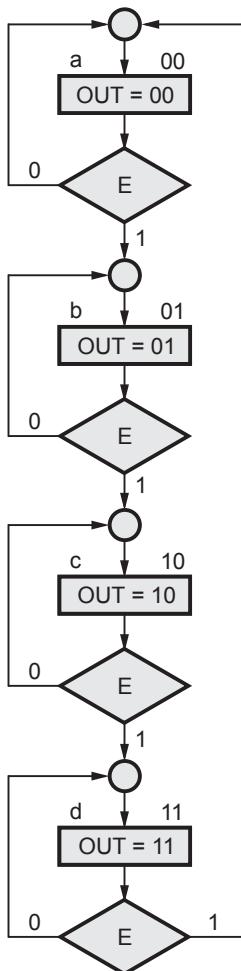


Fig. 8.3.1 ASM Chart

The output represents the output of the counter.

Example 8.3.2 Draw an ASM chart for 2-bit up/down counter having a mode control input M . For $M = 1$: Count up and $M = 0$: Count down.

Solution :

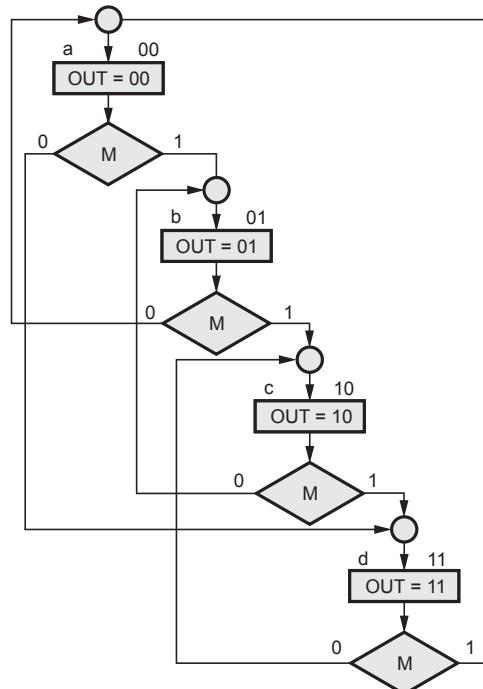


Fig. 8.3.2 ASM Chart

Example 8.3.3 Draw an ASM chart and state table for a 2-bit UP-DOWN counter having mode control input :

$M = 1$: Up counting

$M = 0$: DOWN counting

The circuit should generate a output 1 whenever count becomes minimum or maximum.

SPPU : May-05,14, Dec.-12, Marks 8

Solution : State diagram

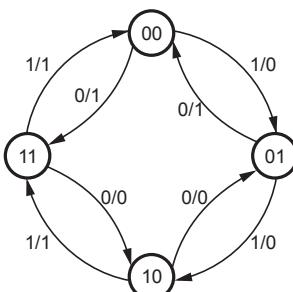


Fig. 8.3.3

ASM chart

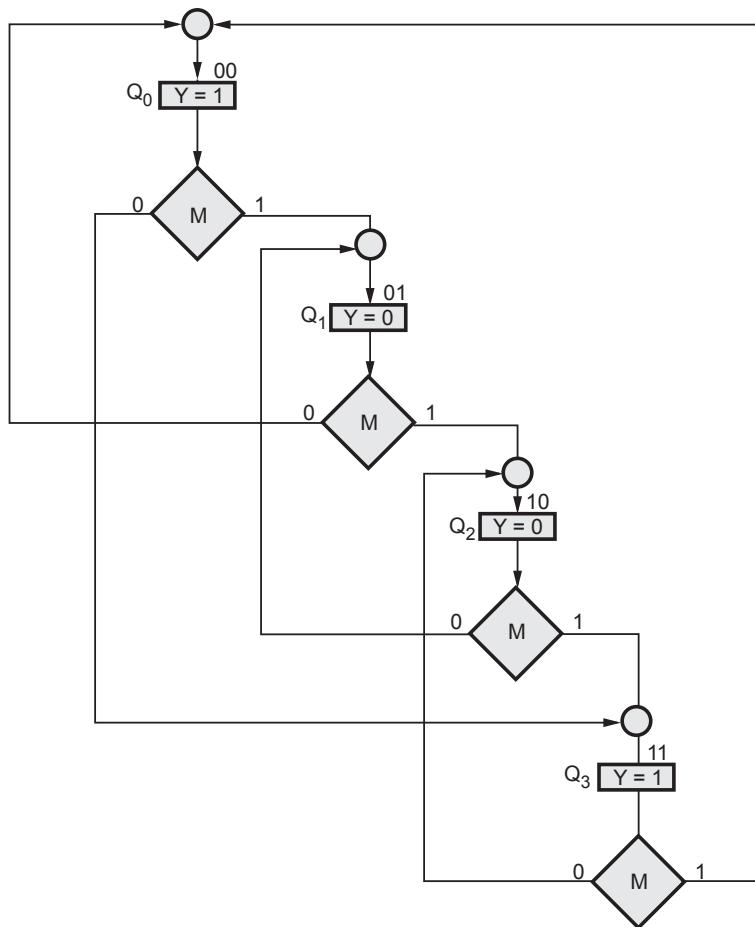


Fig. 8.3.4

Example 8.3.4 Draw an ASM chart for the synchronous circuit having the following description, "The circuit has a control input X, clock and outputs A and B. If $X = 1$, on every clock rising edge the code on BA changes from $00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 00$ and repeats. If $X = 0$, the circuit holds the present state.". SPPU : Dec.-11, Marks 10

Solution :

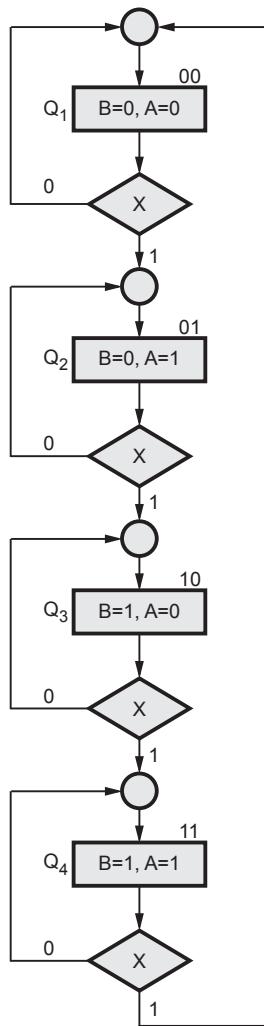


Fig. 8.3.5 ASM chart

Example 8.3.5 Draw an ASM chart and state diagram for the synchronous circuit having the following description :

The circuit has control input C , clock and outputs x , y and z .

i) If $C = 1$, on every clock rising edge the code on output x , y and z changes from $000 \rightarrow 010 \rightarrow 100 \rightarrow 110 \rightarrow 000$ and repeats.

ii) If $C = 0$, the circuit holds the present state.

SPPU : May-2000

Solution :

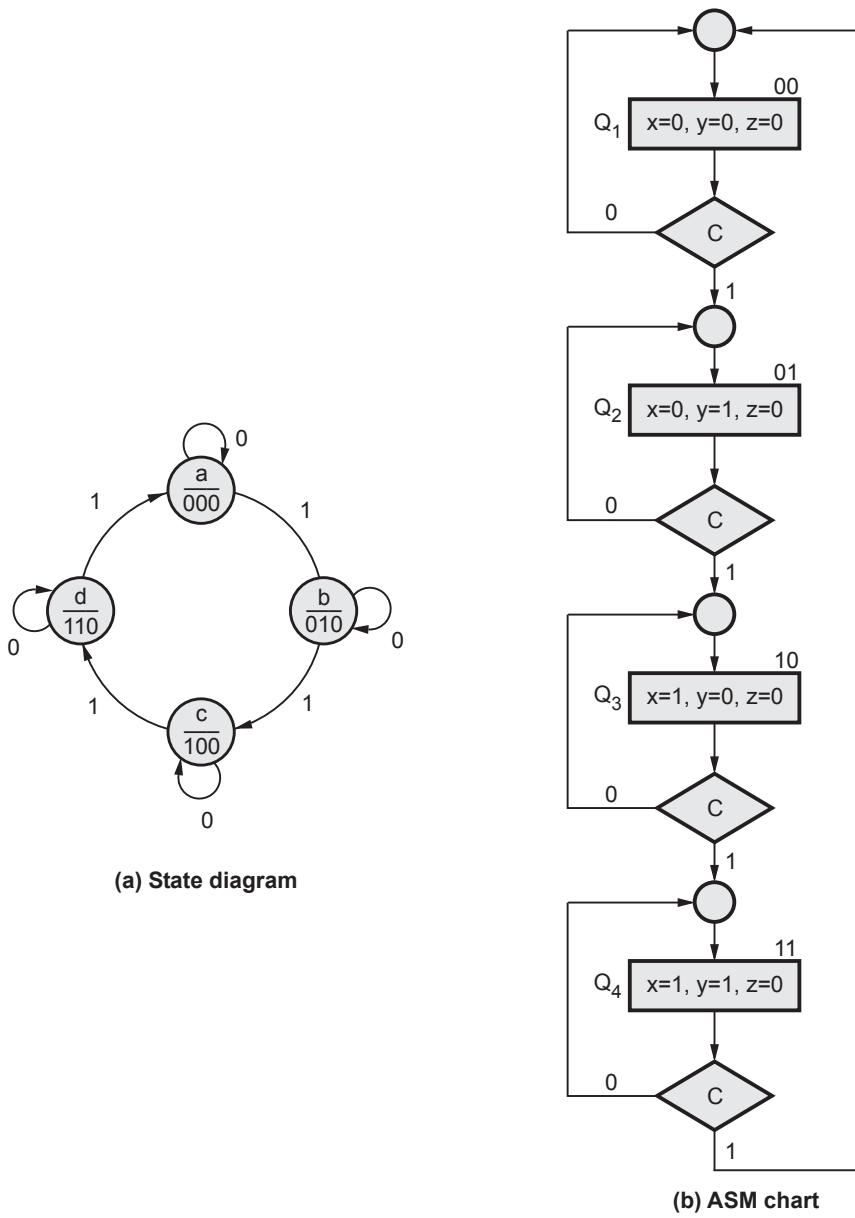


Fig. 8.3.6

Example 8.3.6 Draw ASM chart for the following state machine :

A two-bit up counter with output 'Q1Q0' and enable signal 'X' is to be design. If 'X' = 0, Counter changes the state as '00-01-10-11-00'. If 'X' = 1, Counter should remain in present state.

Design your circuit using JK-FF and suitable MUXs.

SPPU : May-06,07,14,17, Marks 7

Solution : Refer example 8.3.4 for ASM chart.

The Table 8.3.1 shows the multiplexer input conditions for given example.

Present state		Next state		Input condition	Multiplexer input	
A	B	A^+	B^+		MUX 1	MUX 2
0	0	0	0	\bar{X}	0	X
0	0	0	1	X		
0	1	0	1	\bar{X}	X	\bar{X}
0	1	1	0	X		
1	0	1	0	\bar{X}	1	X
1	0	1	1	X		
1	1	1	1	\bar{X}	\bar{X}	\bar{X}
1	1	0	0	X		

Table 8.3.1

Logic Diagram

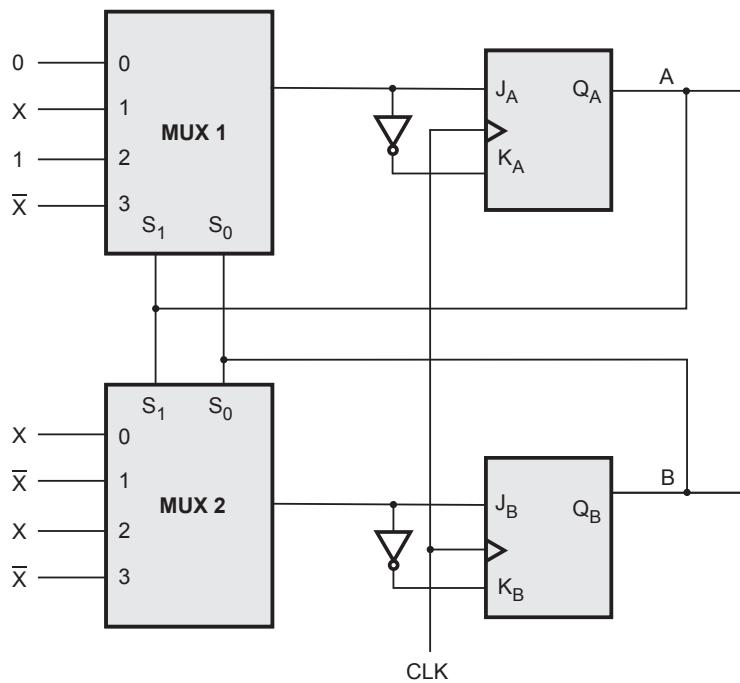


Fig. 8.3.7

Example 8.3.7 A sequential circuit has to count DOWN from '111' to '100'. The circuit also has an input 'X'. If $X = 0$ then the circuit will count DOWN and if $X = 1$ then they will remain in the current state. Draw an ASM chart and state table for this circuit and design the circuit to generate the output using MUX controller method.

SPPU : Dec.-06, Marks 16

Solution :

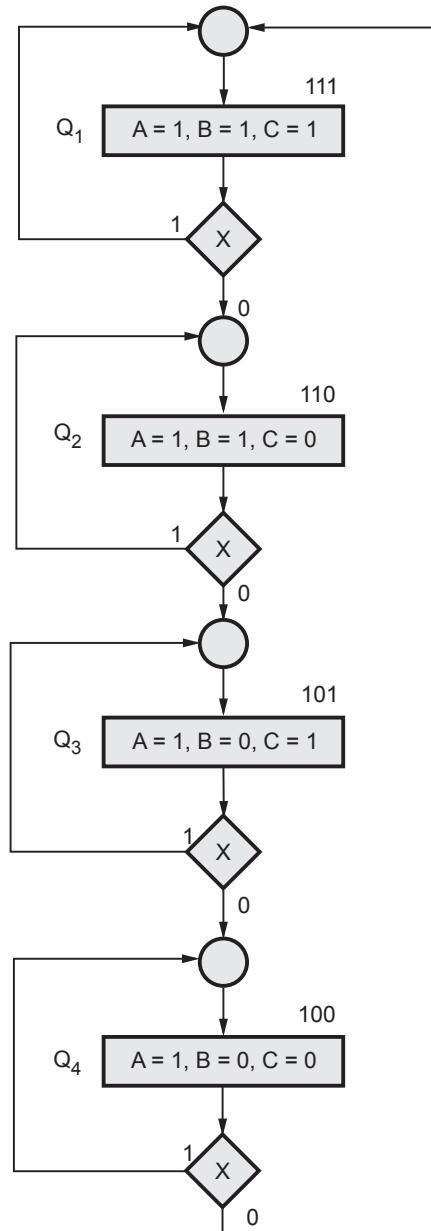


Fig. 8.3.8 ASM chart

The Table 8.3.2 shows the multiplexer input conditions for given example.

Present state			Next state			Input condition	Multiplexer input		
A	B	C	A^+	B^+	C^+		MUX 1	MUX 2	MUX
1	1	1	1	1	1	X			
1	1	1	1	1	0	\bar{X}	1	1	X
1	1	0	1	1	0	X			
1	1	0	1	0	1	\bar{X}	1	X	\bar{X}
1	0	1	1	0	1	X			
1	0	1	1	0	0	\bar{X}	1	0	X
1	0	0	1	0	0	X			
1	0	0	0	0	0	\bar{X}	X	0	0

Table 8.3.2

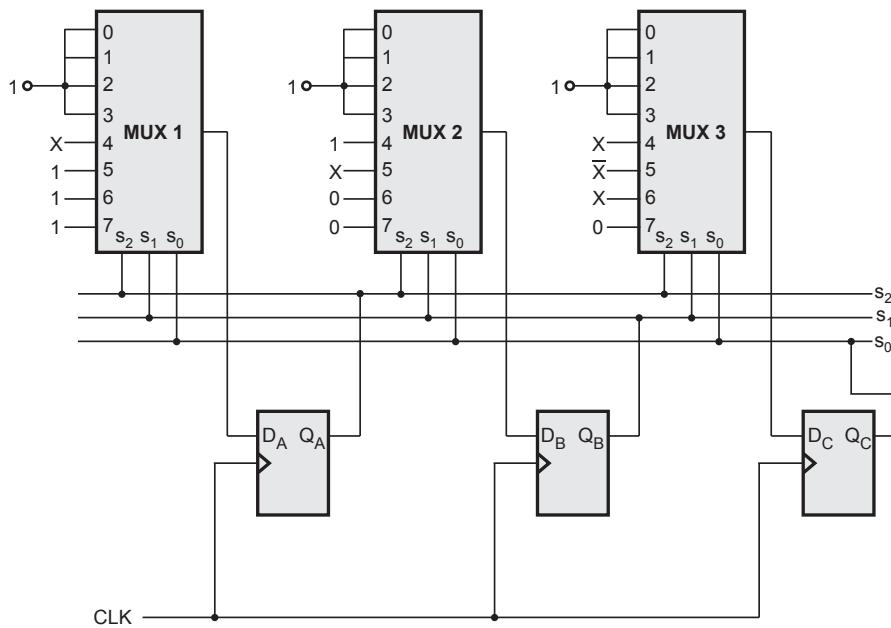


Fig. 8.3.9

It is important to note that unused inputs of multiplexer are connected to logic 1. Therefore, if circuit resets in any other state, the next state will be 111. The circuit will then start down counting if $X = 0$.

Example 8.3.8 A sequential circuit has to COUNT UP from 0 to 3. The circuit also has a control input, E. If $E = 0$, the circuit will remain in the current state and if $E = 1$, the circuit will go to the next state. Draw the necessary ASM chart and state diagram. Also design the circuit with the help of D flip-flops.

SPPU : May-08, Marks 16

Solution : ASM chart :

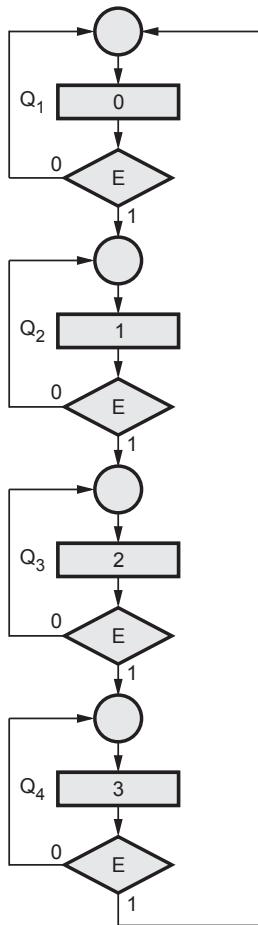


Fig. 8.3.10

State Table :

Input (E)	Present state		Next state		Flip-flop inputs	
	B	A	B	A	D_B	D_A
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	1	0	1	0
0	1	1	1	1	1	1
1	0	0	0	1	0	1
1	0	1	1	0	1	0
1	1	0	1	1	1	1
1	1	1	0	0	0	0

State diagram :

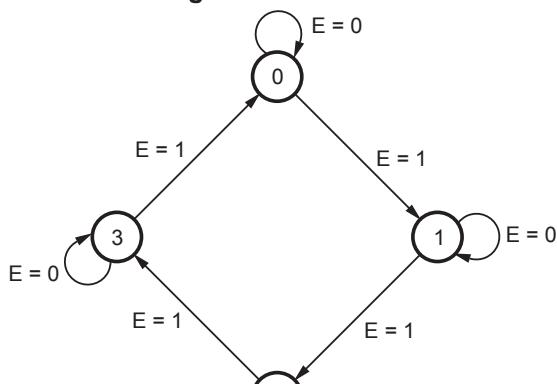
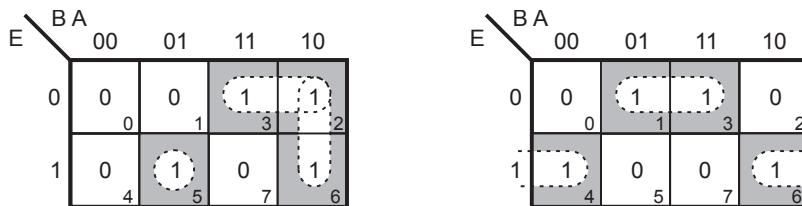


Fig. 8.3.11

K-map simplification :



$$D_B = \bar{E}\bar{B} + B\bar{A} + E\bar{B}A$$

$$D_A = \bar{E}A + E\bar{A}$$

$$E \oplus A$$

Fig. 8.3.12

Circuit diagram :

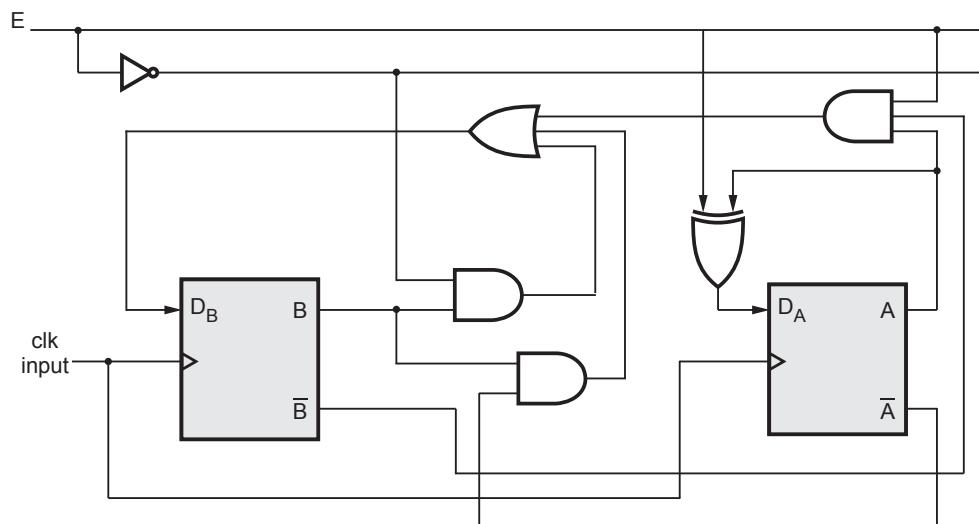


Fig. 8.3.13

Example 8.3.9 Design a sequence generator circuit to generate the sequence 1-3-5-7 using multiplexer controller based ASM approach.

Consideration :

- If control input $C = 0$, the sequence generator circuit in the same state.
- If control input $C = 1$, the sequence generator circuit goes into next state.

SPPU : Dec.-13, Marks 7

Solution :

Present state			Next state			Input condition	Multiplexer input		
A	B	C	A^+	B^+	C^+		MUX 1	MUX 2	MUX 3
0	0	1	0	0	1	\bar{X}	0	X	1
0	0	1	0	1	1	X			

0	1	1	0	1	1	\bar{X}	X	\bar{X}	1
0	1	1	1	0	1	X			
1	0	1	1	0	1	\bar{X}	1	X	1
1	0	1	1	1	1	X			
1	1	1	1	1	1	\bar{X}	\bar{X}	\bar{X}	1
1	1	1	0	0	1	X			

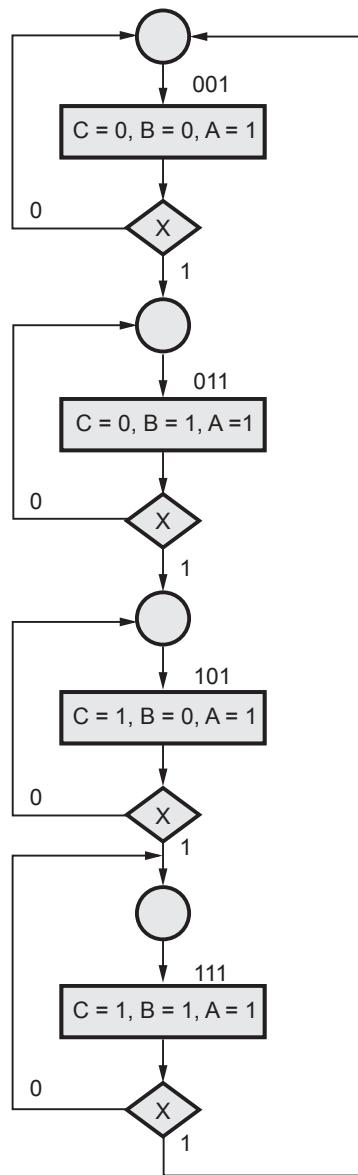


Fig. 8.3.14

Logic diagram

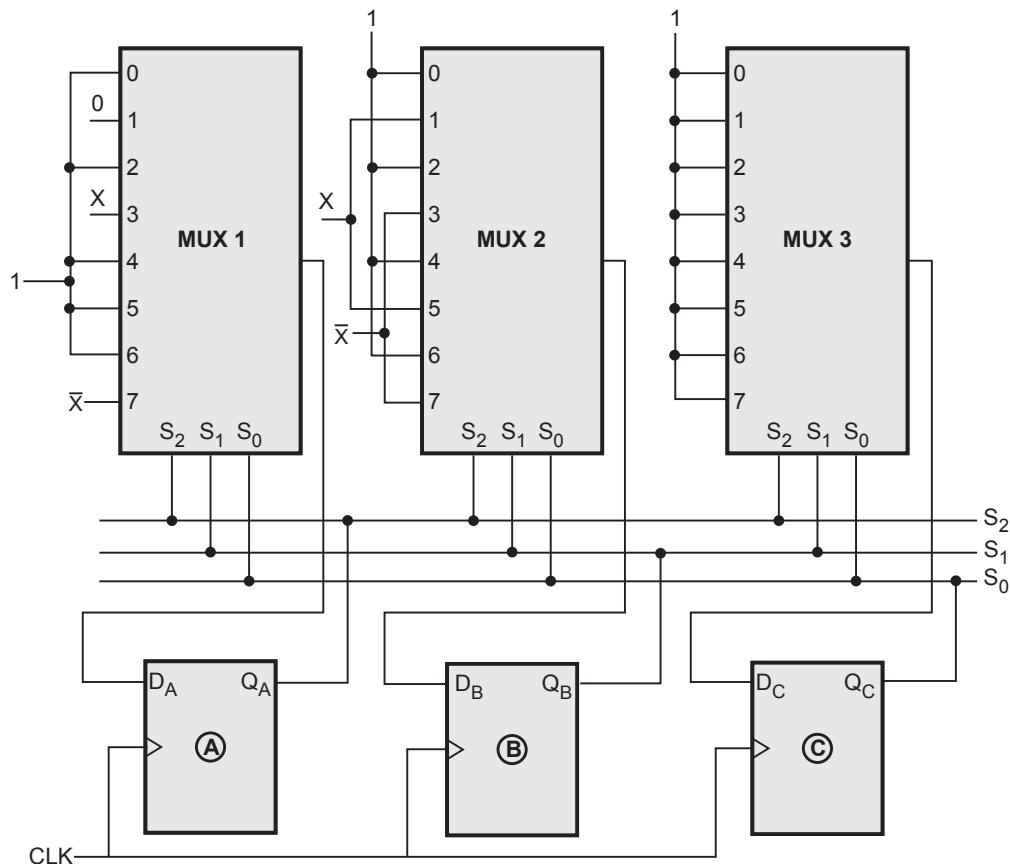


Fig. 8.3.15

Example 8.3.10 Draw an ASM chart for the 3-bit down counter having one enable line such that :

$E = 1$ (counting enabled)

$E = 0$ (counting disabled) Also draw the state diagram

SPPU : Dec.-19, Marks 6

Solution :

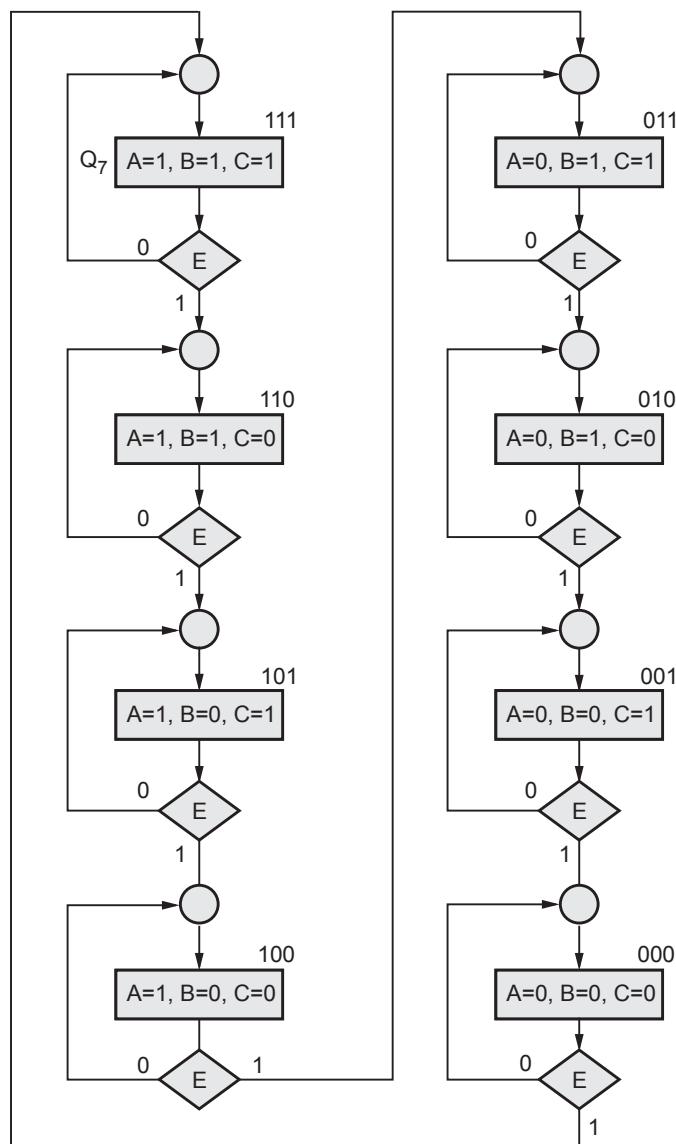


Fig. 8.3.16

State diagram

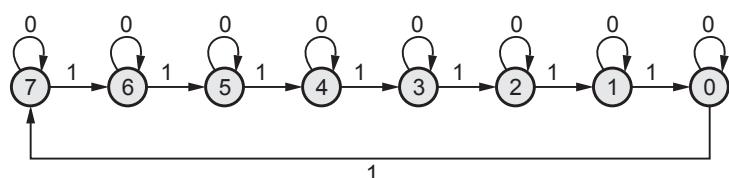


Fig. 8.3.17

Review Questions

1. Draw the ASM chart for the following state machine. A 2-bit up counter is to be designed with output Q, Q_0 and enable signal 'X'. If $X = 0$, then counter changes the state as 00 - 01 - 10 - 11 - 00. If 'X' = 1 then counter remains in same state.

Design the circuit using JK-FF and suitable MUX.

SPPU : May-14, Marks 7

2. Draw an ASM chart and state table for 2-bit up-down counter having mode control input M

When $M = 1$: UP counting

When $M = 0$: Down counting

The circuit should generate output whenever counter becomes minimum or maximum.

SPPU : May-14, Marks 7

3. Draw ASM chart for the following state machine :

A two bit up counter with output 'BA' and enable signal 'X' is to be designed. If 'X' = 0, counter changes the state as '00-01-11-00'. If 'X'=1, counter should remain in present state. Design the circuit using multiplexer controller method.

SPPU : May-16, Marks 8



UNIT IV

9

Programmable Logic Devices

Syllabus

PLD, ROM as PLD, Programmable Logic Array (PLA), Programmable Array Logic (PAL), Designing combinational circuits using PLDs.

Contents

9.1	<i>Introduction</i>	May-06,07,08,16,	
		Dec.-06,08,13,18, Marks 10
9.2	<i>PROM (Programmable Read Only Memory)</i>			
9.3	<i>PLA (Programmable Logic Array)</i>	Dec.-05,08,10,13,14,16,19,	
		May-10,13,14,16,17,18,19, Marks 8
9.4	<i>PAL (Programmable Array Logic)</i>	May-05,11,14,	
		Dec.-08,12,13,14,18, Marks 8
9.5	<i>Comparison between PROM, PLA and PAL</i>	Dec.-05,06,07,	
		May-06,07,08,15,16, Marks 4

9.1 Introduction

SPPU : May-06,07,08,16, Dec.-06,08,13,18

So far we have discussed various digital ICs for performing basic digital operations and other functions, such as adders, comparators, arithmetic logic unit, multiplexers, demultiplexers, code converters, shift registers, counters etc. These ICs, due to their fix function are known as **fixed function ICs**. These ICs are designed by their manufacturers and produced in large quantities to satisfy the needs of a wide variety of applications.

We have seen the design of digital circuits using fixed function ICs. There are two more approaches for the design of digital circuits.

- Use of Application Specific Integrated Circuits (ASICs)
- Use of Programmable Logic Devices (PLDs)

In the fixed function IC approach, we have to use various fixed function ICs to implement different functional blocks in the digital circuit. On the other hand, in ASIC, a single IC is designed and manufactured to implement the entire circuit. In the third approach programmable logic devices are used to implement logic functions. The main advantage of PLD approach is that PLDs can be easily configurable by the individual user for specific applications. The Table 9.1.1 shows the comparison between these three design approaches.

Comparison parameter	Fixed-function IC approach	ASIC approach	PLD approach
Development cost	Low	High	Low
Space required	Large	Minimum	Less
Power required	Large	Less	Less
Reliability	Less compared to other two approaches.	Highest	High
Circuit testing	Easy	Specialized testing methods are required with may increase cost and effort.	Easy
Design flexibility	Less	No	More
Modification in design	Possible with change in circuit and/or with change in components.	No	May be possible without any circuit or component changes but only by reconfiguring the device.
Design security	Lack of security i.e. circuit can easily be copied by others.	High	High
Design time	Less	More	Less

Table 9.1.1 Comparison between design approaches

PLDs can be reprogrammed in few seconds and hence gives more flexibility to experiment with designs. Reprogramming feature of PLDs also make it possible accept changes/modifications in the previously design circuits. These two main advantages and others discussed in Table 9.1.1 make PLDs very popular in digital design.

According to architecture, complexity and flexibility in programming PLDs are classified as

- PROMs : Programmable Read Only Memories
- PLAs : Programmable Logic Arrays
- PAL : Programmable Array Logic
- FPGAs : Field Programmable Gate Arrays
- CPLDs : Complex Programmable Logic Devices

Review Questions

1. Define PLD. SPPU : Dec.-18, Mark 1

2. State two advantages of PLD over fixed function IC and application specific IC.

3. What is PLD ? What do you mean by designing using PLDs ?

SPPU : Dec.-08, Marks 4

Explain with suitable examples. What are the advantages of designing using PLDs over designing discrete LSI components ? Explain.

SPPU : May-06, Dec.-06, Marks 10

4. What is ASIC ? Explain its advantages over conventional discrete circuits.

SPPU : May-07, Marks 8, May-08, Marks 6

5. What are different types of PLDs ?

SPPU : Dec.-13,18, May-16 Marks 3

9.2 PROM (Programmable Read Only Memory)

The Fig. 9.2.1 shows the block diagram of PROM. It consists of n -input lines and m -output lines. Each bit combination of the input variables is called an **address**. Each bit combination that comes out of the output lines is called a **word**. The number of bits per word is equal to the number of output lines, m . The address specified in binary number denotes one of the minterms of n variables. The number of distinct addresses possible with n -input variables is 2^n . An output word can be selected by a unique address and since there are 2^n distinct addresses in PROM, there are 2^n distinct words in the PROM. The word available on the output lines at any given time depends on the address value applied to the input lines.

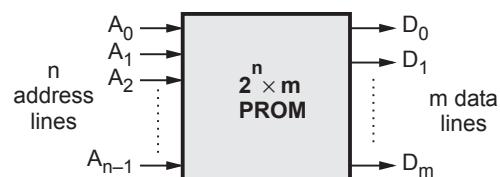


Fig. 9.2.1

Let us consider 64×4 PROM. The PROM consists of 64 words of 4-bits each. This means that there are four output lines and particular word from 64 words presently available on the output lines is determined from the six input lines. There are only six inputs in a 64×4 PROM because $2^6 = 64$ and with six variables, we can specify 64 addresses or minterms. For each address input, there is a unique selected word. Thus, if the input address is 000000, word number 0 is selected and applied to the output lines. If the input address is 111111, word number 63 is selected and applied to the output lines.

The Fig. 9.2.2 shows the internal logic construction of a 64×4 PROM. The six input variables are decoded in 64 lines by means of 64 AND gates and 6 inverters. Each output of the decoder represents one of the minterms of a function of six variables. The 64 outputs of the decoder are connected through fuses to each OR gate. Only four of these fuses are shown in the diagram, but actually each OR gate has 64 inputs and each input goes through a fuse that can be blown as desired.

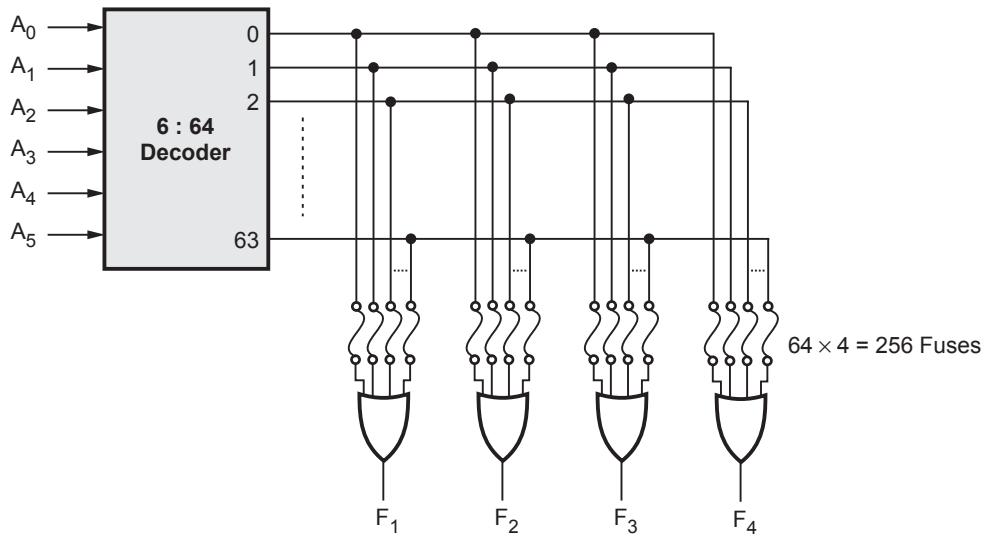


Fig. 9.2.2 Logic construction of 64×4 PROM

The PROM is a two level implementation in sum of minterms form. Let us see AND-OR and AND-OR-INVERTER implementation of PROM. Fig. 9.2.3 shows the 4×2 PROM with AND-OR and AND-OR-INVERTER implementations. (Refer Fig. 9.2.3 on next page)

9.2.1 AND Matrix

The Fig. 9.2.4 shows the AND matrix. It is used to form product terms. It has m AND gates with $2n$ -inputs and m -outputs, one for each AND gate. The Fig. 9.2.4 shows the AND gates formed by diodes and resistors structure. Each AND gate has all the

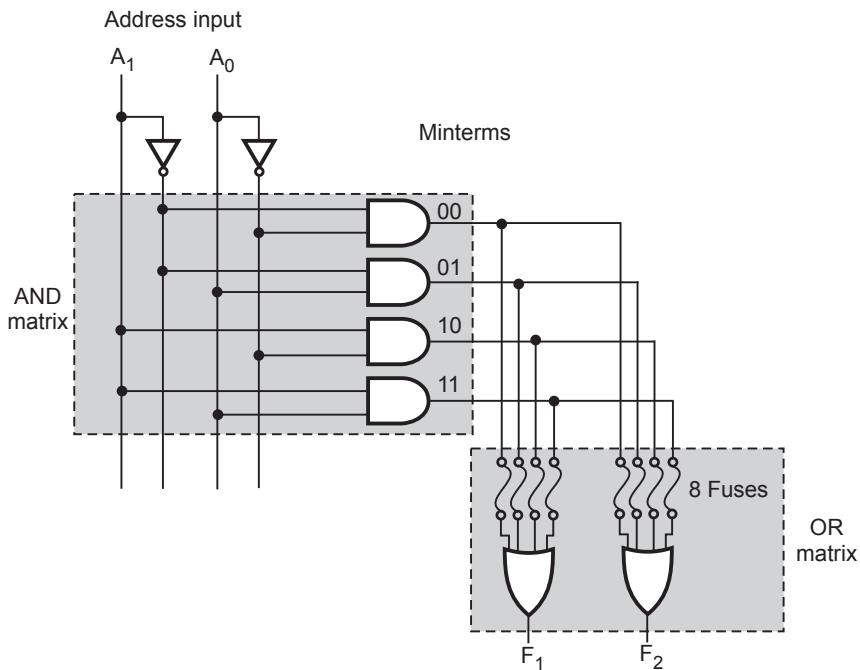


Fig. 9.2.3 (a) 4×2 PROM with AND-OR gates

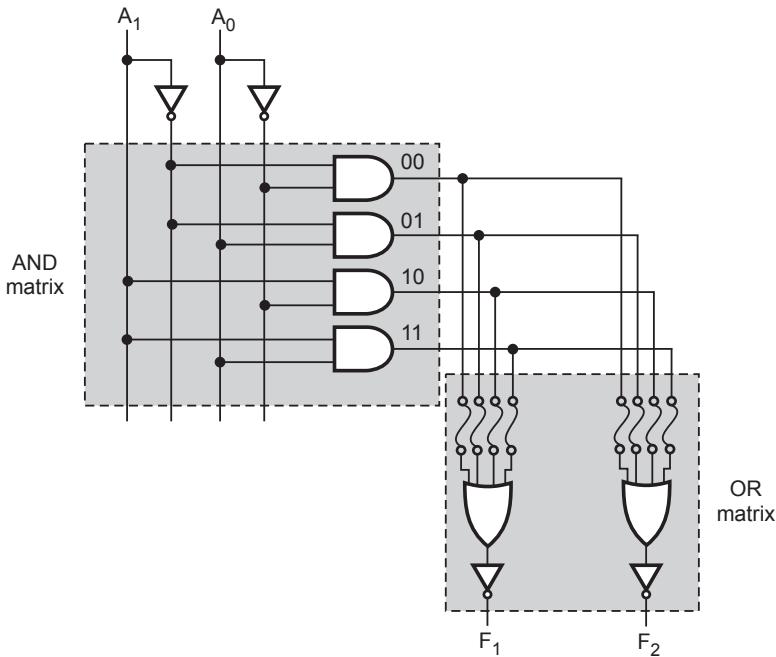


Fig. 9.2.3 (b) 4×2 PROM with AND-OR-INVERTER gates

input variables in complemented and uncomplemented form. There is a nichrome fuse link in series with each diode which can be burn out to disconnect particular input for

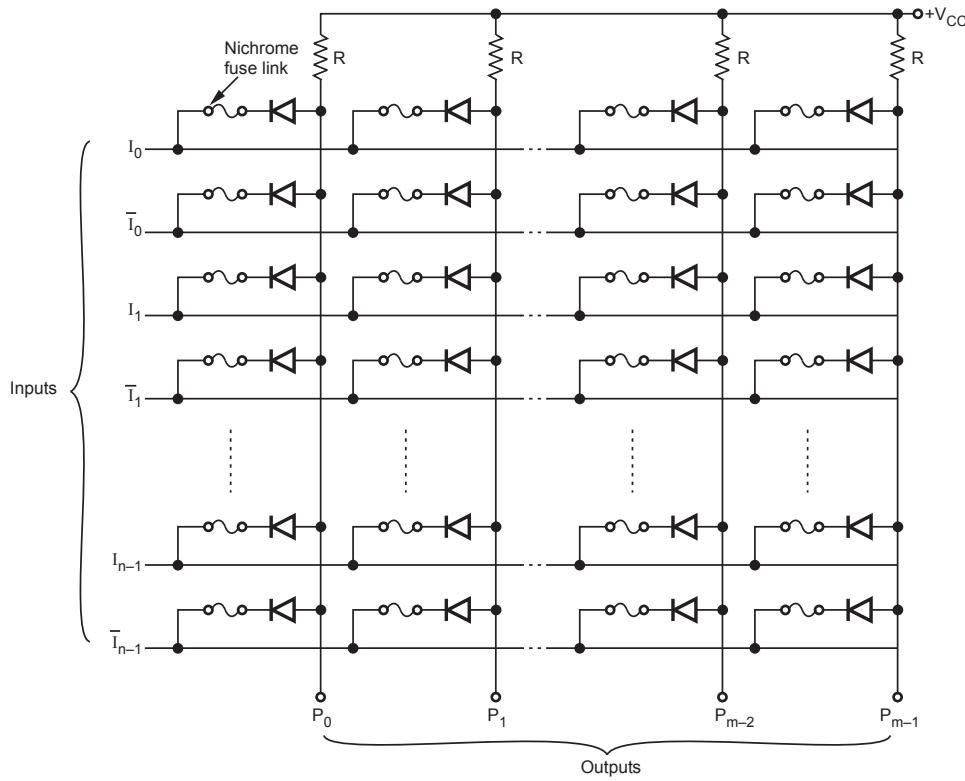


Fig. 9.2.4 Internal structure of AND matrix

that AND gate. Before programming, all fuse links are intact and the product term for each AND gate is given by

$$P = I_0 \cdot \bar{I}_0 \cdot I_1 \cdot \bar{I}_1 \dots \cdot I_{n-1} \cdot \bar{I}_{n-1}$$

The Fig. 9.2.5 shows the simplified and equivalent representation of input connections for one AND gate. The array logic symbol shown in Fig. 9.2.5 (b) uses a single horizontal line connected to the gate input and multiple vertical lines to indicate the individual inputs. Each intersection between horizontal line and vertical line indicates the fuse connection.

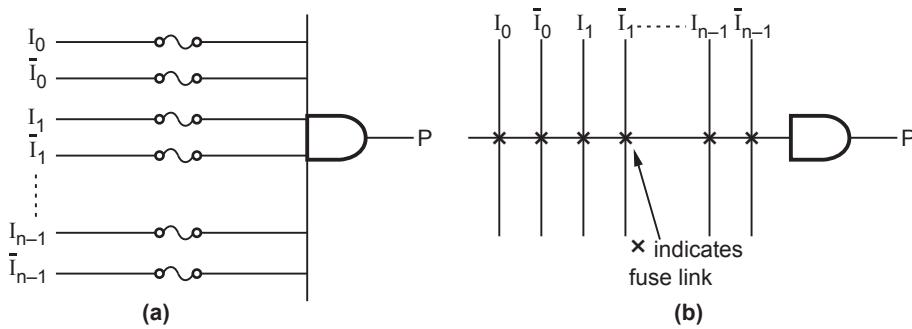


Fig. 9.2.5 Equivalent representation of AND gate

The Fig. 9.2.6 shows the simplified representation of AND matrix with input buffer.

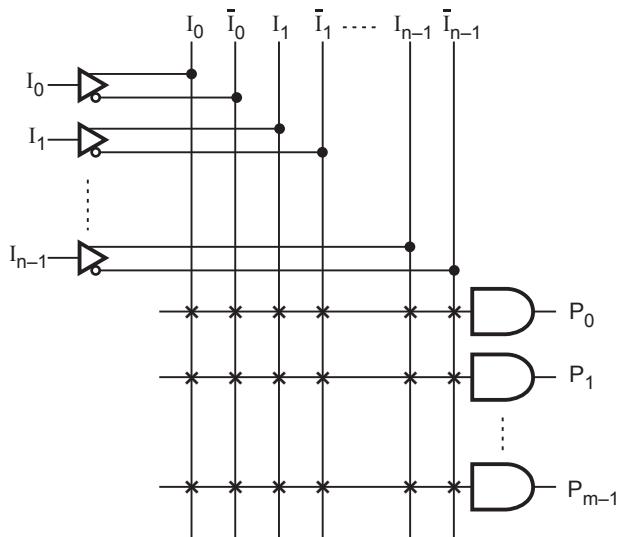


Fig. 9.2.6 Simplified representation of AND matrix with input buffer

9.2.2 OR Matrix

The OR matrix is provided to produce the logical sum of the product term outputs of the AND matrix. The Fig. 9.2.7 shows the OR gates formed by diodes and resistors structure. Each OR gate has all the product terms as input variables. There is a nichrome

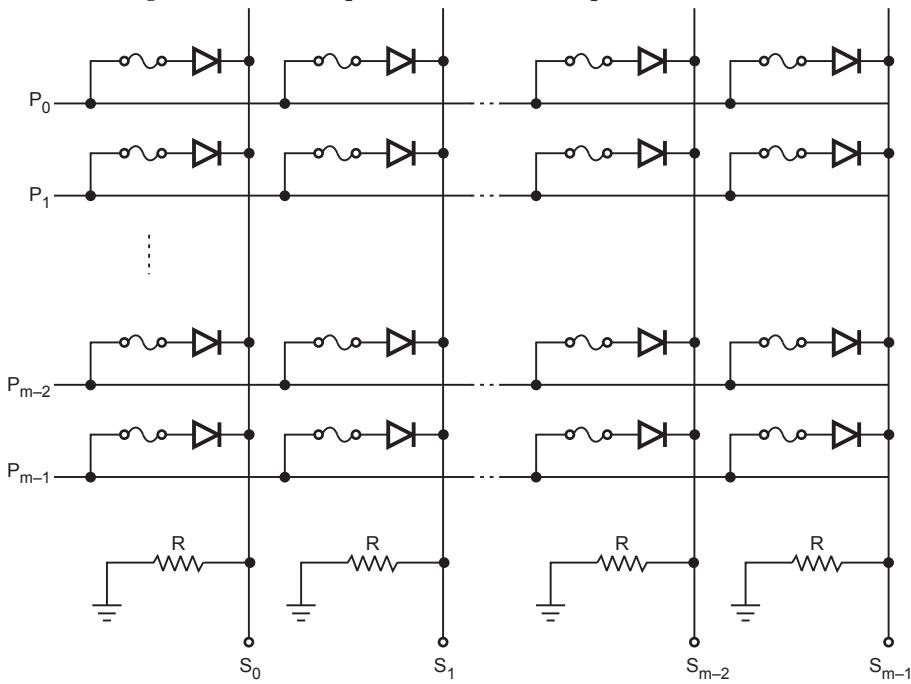


Fig. 9.2.7

fuse link in series with each diode which can be burn out to disconnect particular product term for that OR gate. Before programming, all fuse link in OR matrix are also intact and the sum term for each OR gate is given by,

$$S = P_0 + P_1 + \dots + P_{m-2} + P_{m-1}$$

The Fig. 9.2.8 shows the simplified and equivalent representation of input connections for one OR gate.

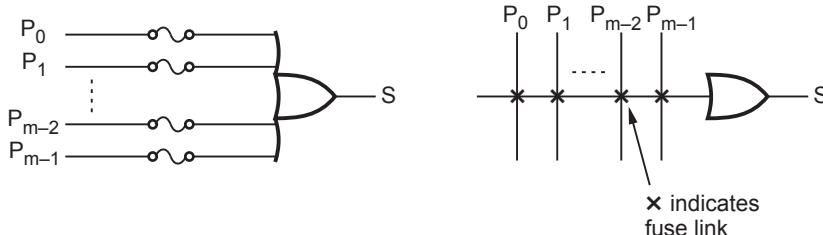


Fig. 9.2.8 Equivalent representation of OR gate

The Fig. 9.2.9 shows the simplified representation of OR matrix.

9.2.3 Invert / Non-invert Matrix

Invert/Non-invert matrix provides output in the complement or uncomplemented form. The user can program the output in either complement or uncomplement form as per design requirements. The typical circuits for invert/non-invert matrix is as shown in Fig. 9.2.10. In both the cases if fuse is intact the output is in its uncomplemented form; otherwise output is in the complemented form.

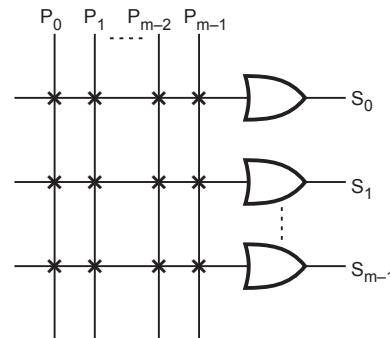


Fig. 9.2.9 Simplified representation of OR matrix

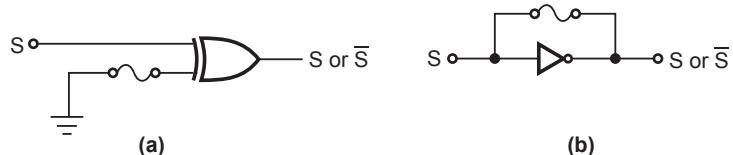


Fig. 9.2.10 Inverting and non-inverting circuits

9.2.4 Combinational Logic Implementation using PROM

Looking at the logic diagram of the PROM, we can realize that each output provides the sum of all the minterms of n-input variables. We know that any Boolean function can be expressed in sum of minterms form. By breaking the links of those minterms not included in the function, each PROM output can be made to represent the Boolean function of one of the output variables in the combinational circuit. For an n-input, m-output combinational circuit, we need a $2^n \times m$ PROM.

Illustrative Examples

Example 9.2.1 Using PROM realize the following expressions.

$$F_1(a, b, c) = \sum m(0, 1, 3, 5, 7)$$

$$F_2(a, b, c) = \sum m(1, 2, 5, 6)$$

Solution :

The given functions have three inputs. They generate $2^3 = 8$ minterms and since there are two functions, there are two outputs. The functions can be realized as shown in Fig. 9.2.11.

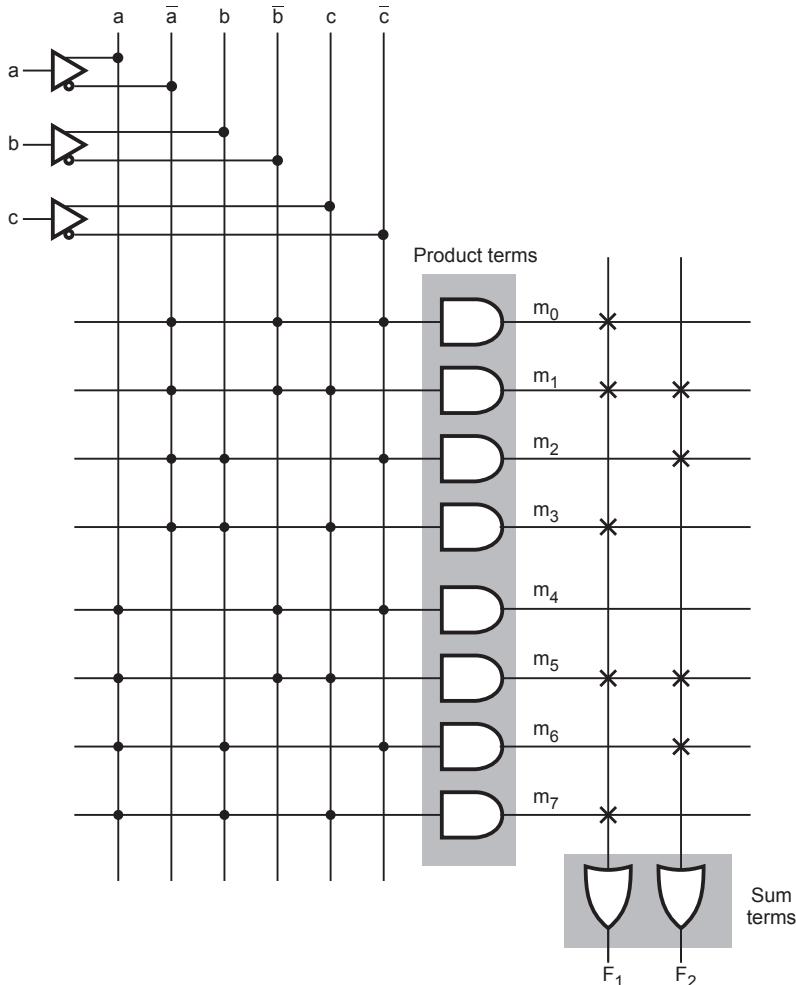
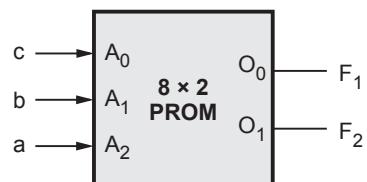


Fig. 9.2.11

The Fig. 9.2.12 shows the block diagram and truth table of PROM.



(a) Block diagram

A₂	A₁	A₀	F₁	F₂
0	0	0	1	0
0	0	1	1	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	1	0

(b) PROM truth table

Fig. 9.2.12

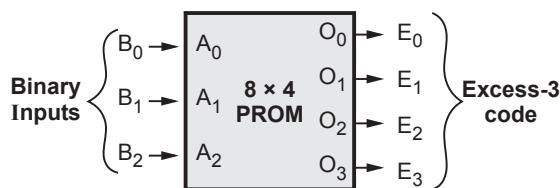
Example 9.2.2 Design a combinational circuit using a PROM. The circuit accepts 3-bit binary number and generates its equivalent Excess-3 code.

Solution : Let us derive the truth table for the given combination circuit. Table 9.2.1 shows the truth table.

In practice when we are designing combinational circuits with PROM, it is not necessary to show the internal gate connections of fuses inside the unit, as shown in the Fig. 9.2.13. (Refer Fig. 9.2.13 on next page). This was shown for demonstration purpose only. The designer has to only specify the PROM (inputs and outputs) and its truth table, as shown in the Fig. 9.2.14.

Inputs			Outputs			
B₂	B₁	B₀	E₃	E₂	E₁	E₀
0	0	0	0	0	1	1
0	0	1	0	1	0	0
0	1	0	0	1	0	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	0	0
1	1	0	1	0	0	1
1	1	1	1	0	1	0

Table 9.2.1 Truth table for 3-bit binary to excess-3 converter



(a) Block diagram

A₂	A₁	A₀	E₃	E₂	E₁	E₀
0	0	0	0	0	1	1
0	0	1	0	1	0	0
0	1	0	0	1	0	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	0	0
1	1	0	1	0	0	1
1	1	1	1	0	1	0

(b) PROM truth table

Fig. 9.2.14

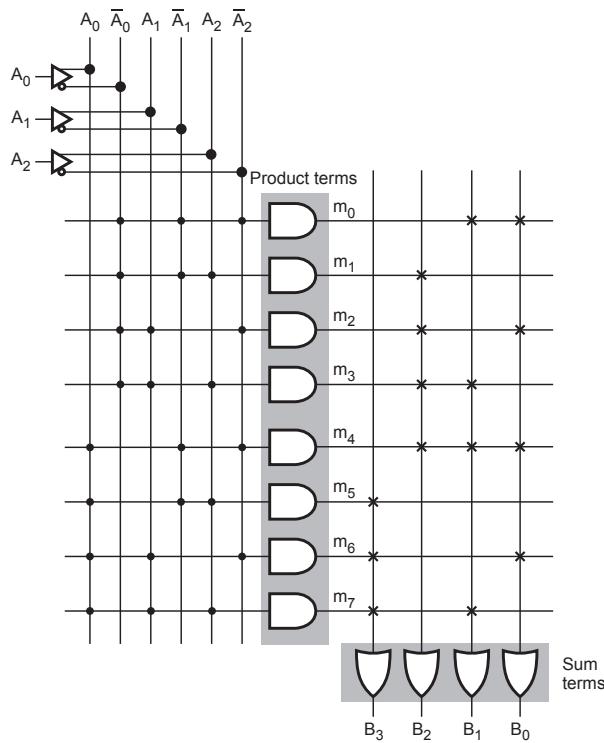
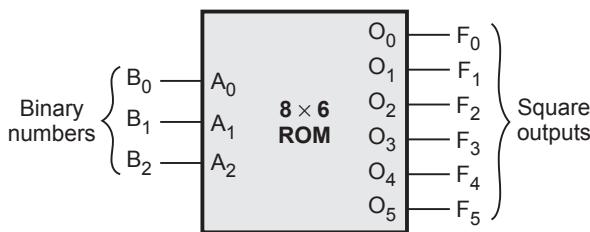


Fig. 9.2.13

Example 9.2.3 Design a combinational circuit using ROM. The circuit accepts 3-bit number and generates an output binary number equal to square of input number.

Solution :



(a) Block diagram

Binary input on address lines			Square of number on data lines								
B_2	B_1	B_0	F_5	F_4	F_3	F_2	F_1	F_0			
0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	1	0	0	0	0	0	1
1	0	0	0	1	0	0	0	0	0	0	0
1	0	1	0	1	1	0	0	0	0	0	1
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	1

(b) ROM truth table

Fig. 9.2.15

Example 9.2.4 Implement binary to excess 3 code converter using ROM.

Solution :

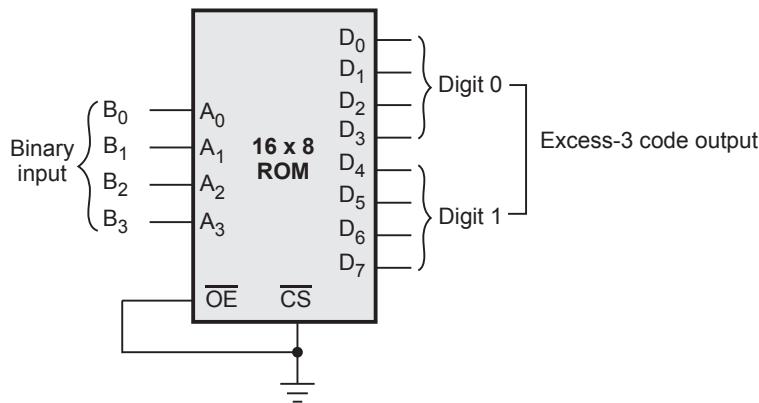


Fig. 9.2.16

Address				Memory contents							
A₃	A₂	A₁	A₀	D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
0	0	0	0	0	0	1	1	0	0	1	1
0	0	0	1	0	0	1	1	0	1	0	0
0	0	1	0	0	0	1	1	0	1	0	1
0	0	1	1	0	0	1	1	0	1	1	0
0	1	0	0	0	0	1	1	0	1	1	1
0	1	0	1	0	0	1	1	1	0	0	0
0	1	1	0	0	0	1	1	1	0	0	1
0	1	1	1	0	0	1	1	1	0	1	0
1	0	0	0	0	0	1	1	1	0	1	1
1	0	0	1	0	0	1	1	1	1	0	0
1	0	1	0	0	1	0	0	0	0	1	1
1	0	1	1	0	1	0	0	0	1	0	0
1	1	0	0	0	1	0	0	0	1	0	1
1	1	0	1	0	1	0	0	0	1	1	0
1	1	1	0	0	1	0	0	0	1	1	1
1	1	1	1	0	1	0	0	1	0	0	0

Table 9.2.2 ROM contents

Examples for Practice

Example 9.2.5 : Design a switching circuit that converts a 4 bit binary code into a 4 bit Gray code using ROM array.

Example 9.2.6 : Design a 3-bit gray to binary code converter using suitable ROM.

Review Question

1. Write a note on PROM as a PLD.

9.3 PLA (Programmable Logic Array)

SPPU : Dec.-05,08,10,13,14,16,19, May-10,13,14,16,17,18,19,

The combinational circuit do not use all the minterms every time. Occasionally, they have don't care conditions. Don't care condition when implemented with a PROM becomes an address input that will never occur. The result is that not all the bit patterns available in the PROM are used, which may be considered a waste of available equipment.

For cases where the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a **Programmable Logic Array (PLA)**. A PLA is similar to a PROM in concept; however it does not provide full decoding of the variables and does not generates all the minterms as in the PROM. The PLA replaces decoder by group of AND gates, each of which can be programmed to generate a product term of the input variables. In PLA, both AND and OR gates have fuses at the inputs, therefore in PLA both AND and OR gates are programmable. Fig. 9.3.1 shows the block diagram of PLA. It consists of n-inputs, output buffer with m outputs, m product terms, m sum terms, input and output buffers. The product terms constitute a group of m AND gates and the sum terms constitute a group of m OR gates, called OR matrix. Fuses are inserted between all n-inputs and their complement values to each of the AND gates. Fuses are also provided between the outputs of the

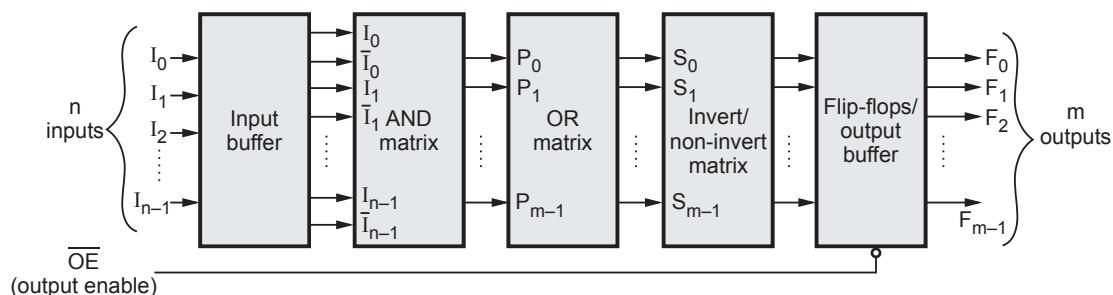


Fig. 9.3.1 Block diagram of a PLA

AND gates and the inputs of the OR gates. The third set of fuses in the output inverters allows the output function to be generated either in the AND-OR form or in the AND-OR-INVERT form. When inverter is bypassed by link we get AND-OR implementation. To get AND-OR-INVERTER implementation inverter link has to be disconnected.

9.3.1 Input Buffer

Input buffers are provided in the PLA to limit loading of the sources that drive the inputs. They also provide inverted and non-inverted form of inputs at its output. The Fig. 9.3.2 shows two ways of representing input buffer for single input.

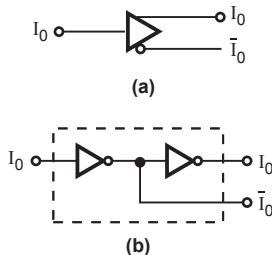


Fig. 9.3.2 Input buffer for single input line

9.3.2 Output Buffer

The driving capacity of PLA is increased by providing buffers at the output. They are usually TTL compatible. The Fig. 9.3.3 shows the tri-state, TTL compatible output buffer. The output buffer may provide totem-pole, open collector or tri-state output.

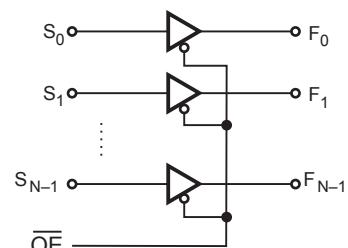


Fig. 9.3.3 Output buffers

9.3.3 Output through Flip-Flops

For the implementation of sequential circuits we need memory elements, flip-flops and combinational circuitry for deriving the flip-flop inputs. To satisfy both the needs some PLAs are provided with flip-flop at each output, as shown in the Fig. 9.3.4.

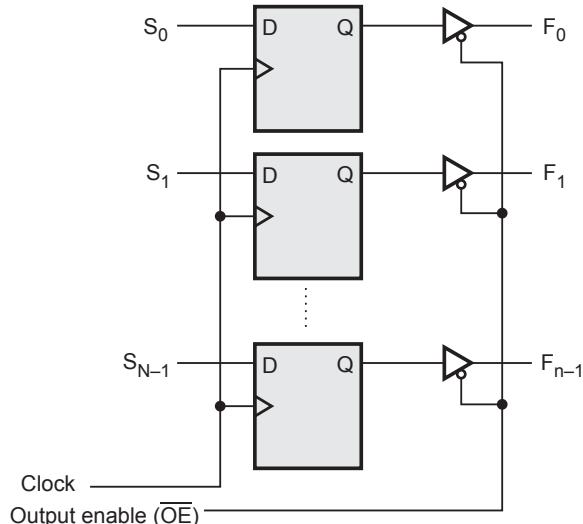


Fig. 9.3.4 PLA with flip-flop at the output

9.3.4 Implementation of Combination Logic Circuit using PLA

Like ROM, PLA can be **mask-programmable** or **field-programmable**. With a mask-programmable PLA, the user must submit a PLA program table to the manufacturer. This table is used by the vendor to produce a user-made PLA that has the required internal paths between inputs and outputs. A second type of PLA available is called a **field-programmable logic array** or FPLA. The FPLA can be programmed by the user by means of certain recommended procedures. FPLAs can be programmed with commercially available programmer units.

As mentioned earlier, user has to submit PLA program table to the manufacturers to get the user-made PLA. Let us study how to determine PLA program table with the help of example.

Illustrative Examples

Example 9.3.1 A combinational circuit is defined by the functions :

$$F_1 = \sum m(3, 5, 7), F_2 = \sum m(4, 5, 7)$$

Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs.

SPPU : May-14, Dec.-14, Marks 6

Solution :

Step 1 : Simplify the given Boolean functions

The Boolean functions are simplified, as shown in the Fig. 9.3.5. The simplified functions in sum of products are obtained from the maps are :

$$F_1 = AC + BC, \quad F_2 = A\bar{B} + AC$$

Step 2 : Write PLA program table

Therefore, there are three distinct product terms : AC , BC and $A\bar{B}$, and two sum terms. The PLA program table shown in Table 9.3.1 consists of three columns specifying product terms, inputs and outputs. The first column gives the lists of product terms numerically. The second

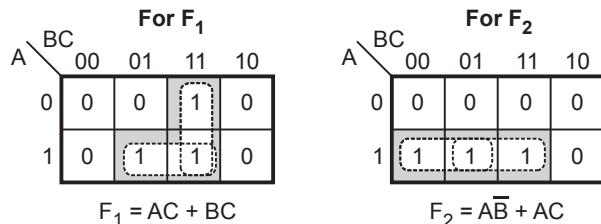


Fig. 9.3.5

Product term	Inputs		Outputs		
	A	B	C	F ₁	F ₂
AC	1	1	-	1	1
BC	2	-	1	1	-
A\bar{B}	3	1	0	-	1
				T	T
					T/C

Table 9.3.1 PLA program table

column specifies the required paths between inputs and AND gates. The third column specifies the required paths between the AND gates and the OR gates. Under each output variable, we write a T (for true) if the output inverter is to be bypassed, and C (for complement) if the function is to be complemented with the output inverter. The product terms listed on the left of first column are not the part of PLA program table they are included for reference only.

Step 3 : Implementation

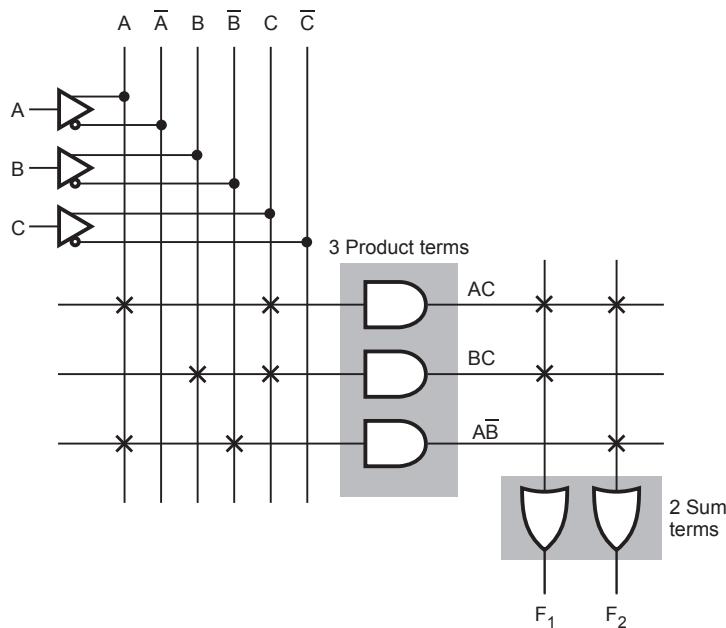


Fig. 9.3.6

Example 9.3.2 Draw a PLA circuit to implement the logic functions $\bar{A}BC + A\bar{B}C + A\bar{C}$ and $\bar{A}\bar{B}\bar{C} + BC$.

Solution :

Step 1 : Simplify the Boolean functions

$$\begin{aligned}
 \bar{A}BC + A\bar{B}C + A\bar{C} &= \bar{A}BC + A(\bar{B}C + \bar{C}) \\
 &= \bar{A}BC + A(\bar{B} + \bar{C}) \quad \because A + \bar{A}B = A + B \\
 &= \bar{A}BC + A\bar{B} + A\bar{C}
 \end{aligned}$$

Note : The second Boolean function is in simplified form.

Step 2 : Implementation (see Fig. 9.3.7 on next page)

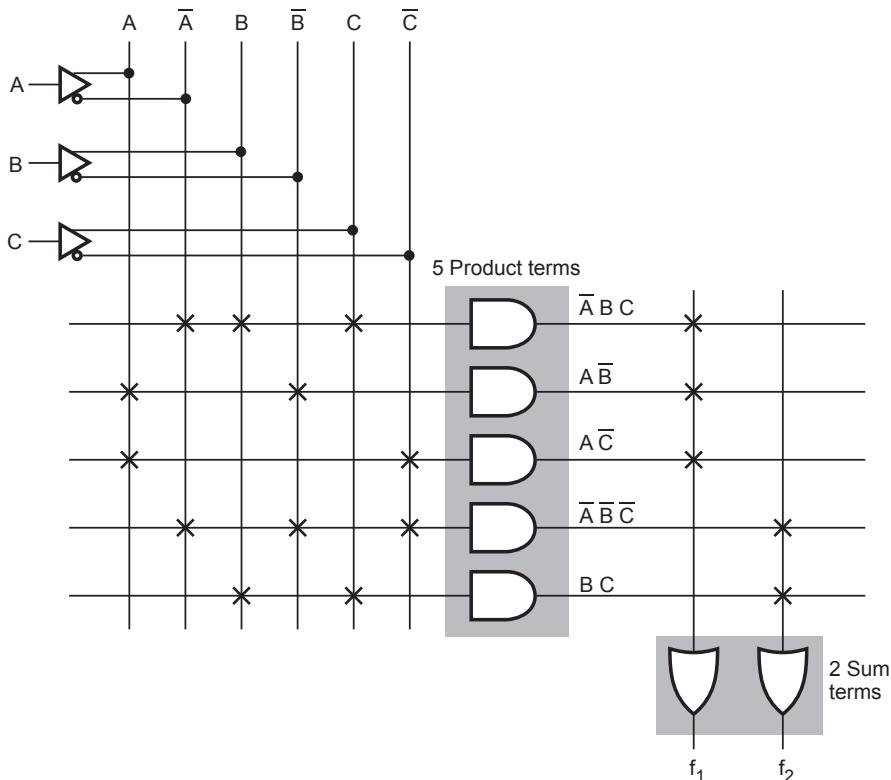


Fig. 9.3.7

Example 9.3.3 Implement the following multiboolian function using $3 \times 4 \times 2$ PLA PLD.

$$f_1(a_2, a_1, a_0) = \sum m(0, 1, 3, 5) \text{ and } f_2(a_2, a_1, a_0) = \sum m(3, 5, 7)$$

Solution : Step 1 : Simplify the Boolean functions.

$$\therefore f_1 = \bar{a}_2 \bar{a}_1 + \bar{a}_2 a_0 + \bar{a}_1 a_0$$

$$f_2 = a_2 a_0 + a_1 a_0$$

To implement functions f₁ and f₂ we require $3 \times 5 \times 2$ PLA and we have to implement them using $3 \times 4 \times 2$ PLA. Therefore, we have to examine product terms by grouping 0s instead of 1. That is product terms for complement of a function.

$$\therefore \bar{f}_1 = a_2 \bar{a}_0 + a_1 \bar{a}_0 + a_2 a_1$$

$$\bar{f}_2 = \bar{a}_2 \bar{a}_1 + a_1 \bar{a}_0 + a_2 \bar{a}_0$$

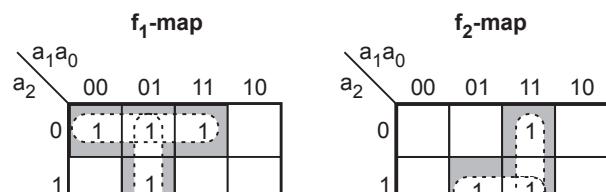


Fig. 9.3.8 K-map simplification

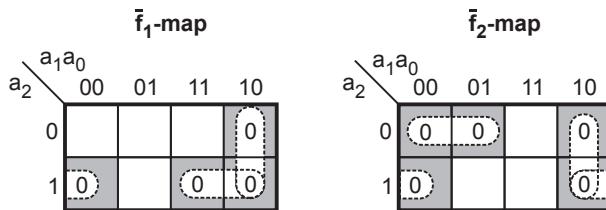


Fig. 9.3.9

Step 2 : Implementation

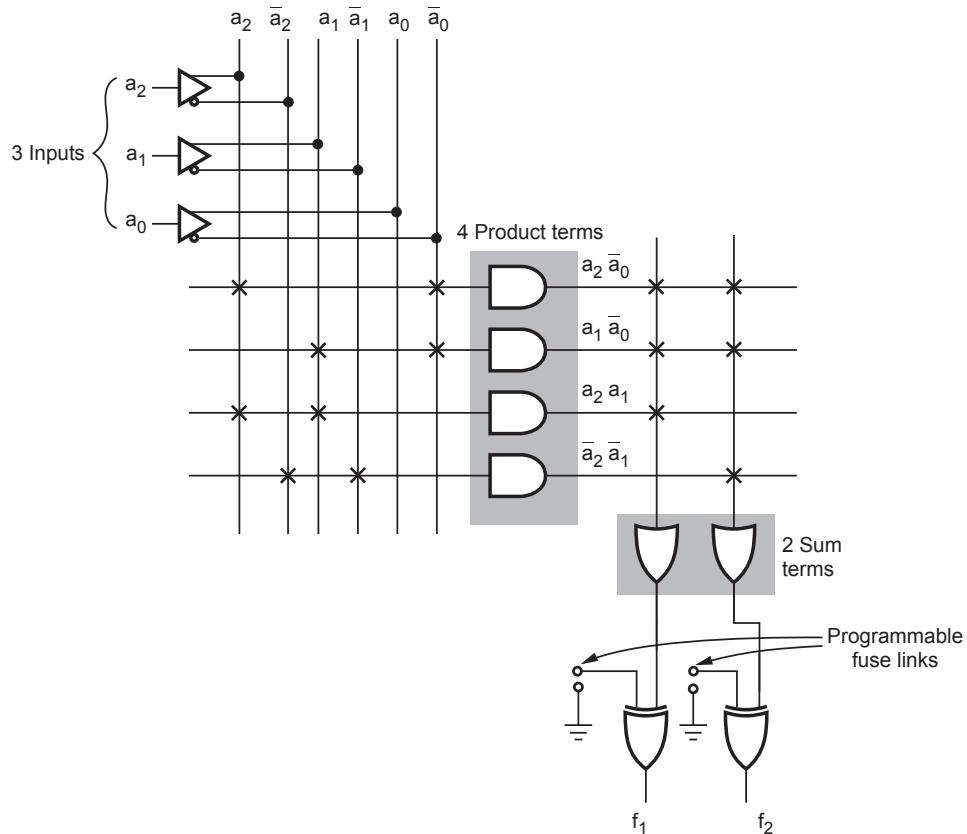


Fig. 9.3.10 Logic diagram

Looking at function outputs we can realize that product terms $a_2 \bar{a}_0$ and $a_1 \bar{a}_0$ are common in both functions. Therefore, we need only 4 product terms and functions can be implemented using a $3 \times 4 \times 2$ PLA as shown in Table 9.3.2 and Fig. 9.3.10.

PLA

Product terms	Inputs			Outputs	
	a_2	a_1	a_0	f_1	f_2
$a_2 \bar{a}_0$	1	—	0	1	1
$a_1 \bar{a}_0$	—	1	0	1	1
$a_2 a_1$	1	1	—	1	—
$\bar{a}_2 \bar{a}_1$	0	0	—	—	1
				C	C

Table 9.3.2

As shown in the Fig. 9.3.10 exclusive-OR gate is programmed to invert the function to get the desired function outputs.

Example 9.3.4 A combinational circuit is defined by the functions,

$$F_1 = \sum m(1, 3, 5) \quad F_2 = \sum m(5, 6, 7)$$

Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs.

Solution : K-map simplification

To implement functions F_1 and F_2 we require $3 \times 4 \times 2$ PLA and we have to implement them using $3 \times 3 \times 2$ PLA. There we have to examine product terms by grouping 0s instead of 1. That is product terms for complement of a function.

Looking at function outputs, functions \bar{F}_1 and F_2 have one common product term. Thus they have total 3 product terms and can be implemented using $3 \times 3 \times 2$ PLA.

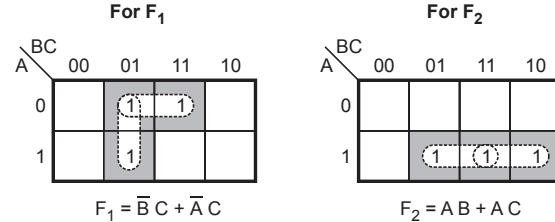


Fig. 9.3.11

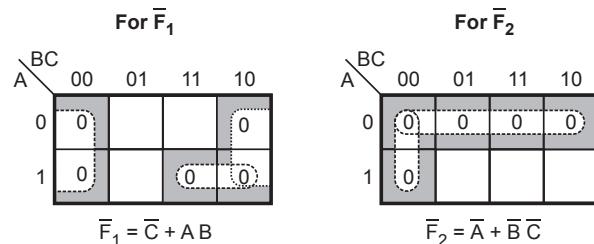


Fig. 9.3.12

PLA program table

Product terms	Inputs			Outputs	
	A	B	C	F_1	F_2
\bar{C}	-	-	0	1	-
AB	1	1	-	1	1
AC	1	-	1	-	1
				C	T

Table 9.3.3

Implementation : Refer Fig. 9.3.13 on next page.

Example 9.3.5 Design a BCD to Excess-3 code converter and implement using suitable PLA.

SPPU : May-18, Marks 6

Solution : Step 1 : Derive the truth table of BCD to Excess-3 converter

Decimal	BCD code				Excess-3 code			
	B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0

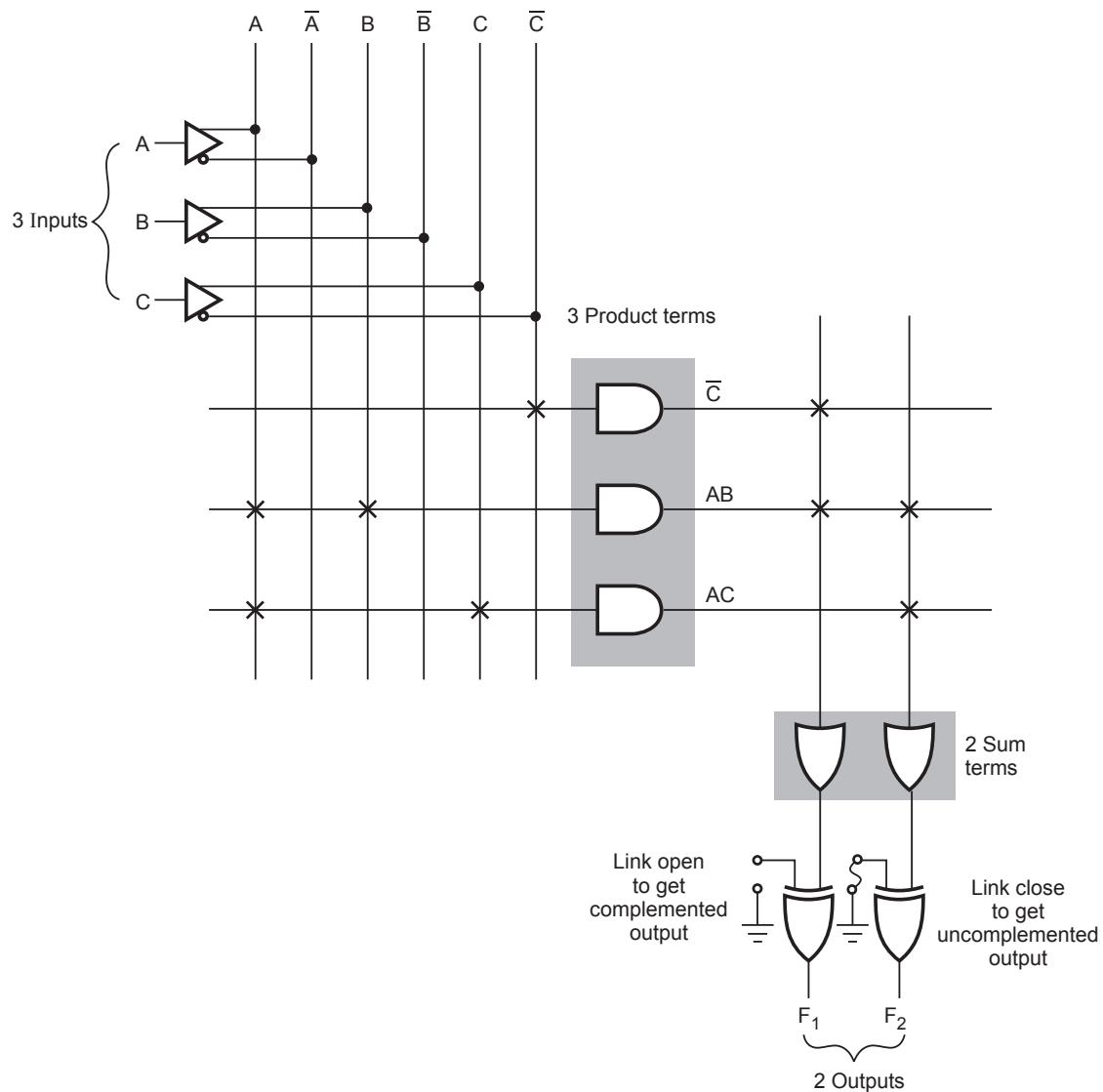


Fig. 9.3.13

2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Table 9.3.4 Truth table for BCD to Excess-3 code converter

Step 2 : Simplify the Boolean functions for Excess-3 code

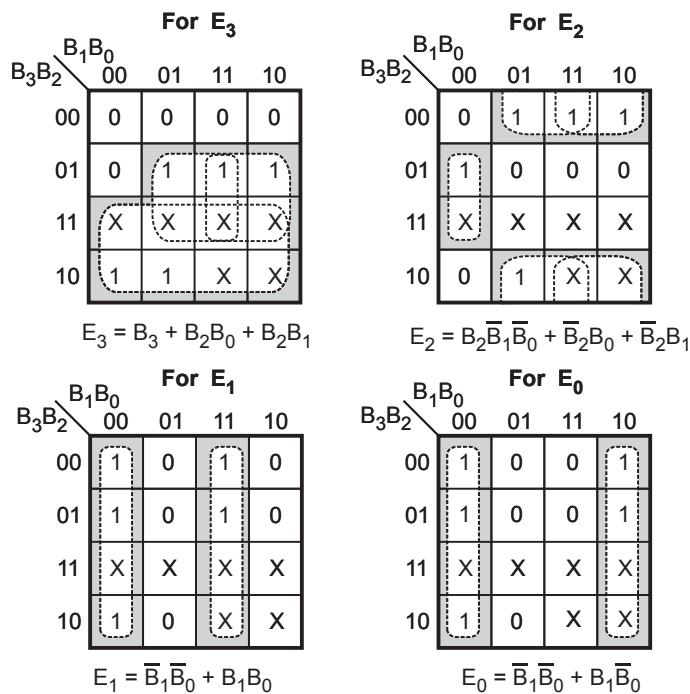
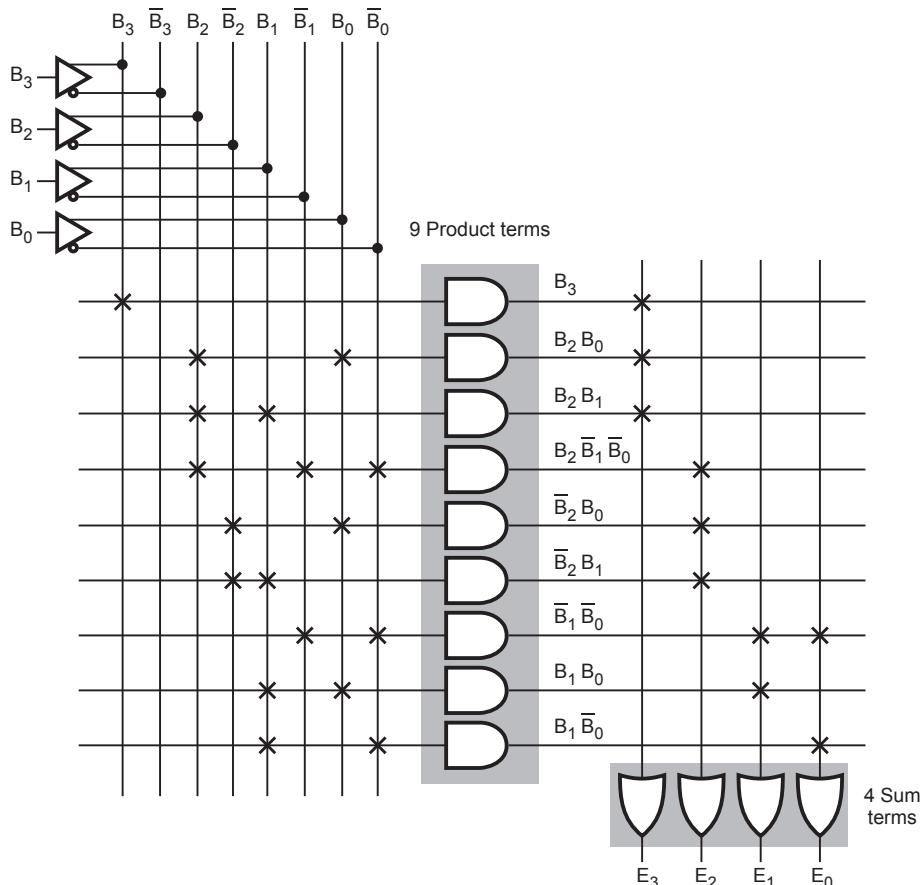


Fig. 9.3.14

Step 3 : Write PLA program table

Product terms	Inputs				Outputs			
	B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
B_3	1	1	—	—	—	1	—	—
$B_2 B_0$	2	—	1	—	1	1	—	—
$B_2 B_1$	3	—	1	1	—	1	—	—
$B_2 \bar{B}_1 \bar{B}_0$	4	—	1	0	0	—	1	—
$\bar{B}_2 B_0$	5	—	0	—	1	—	1	—
$\bar{B}_2 B_1$	6	—	0	1	—	—	1	—
$\bar{B}_1 B_0$	7	—	—	0	0	—	—	1
$B_1 B_0$	8	—	—	1	1	—	—	1
$B_1 \bar{B}_0$	9	—	—	1	0	—	—	1
					T	T	T	T/C

Table 9.3.5 PLA program table

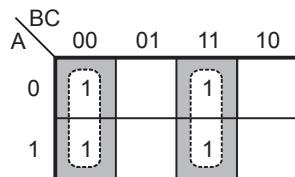
Step 4 : Implementation**Fig. 9.3.15**

Example 9.3.6 Implement the following function using PLA :

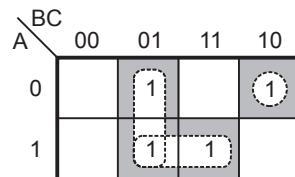
$$f_1 = \sum m(0, 3, 4, 7)$$

$$f_2 = \sum m(1, 2, 5, 7)$$

SPPU : Dec.-08, 14, Marks 8

Solution : K-map simplification

$$f_1 = \overline{B} \overline{C} + B C$$



$$f_2 = \overline{B} C + A C + \overline{A} B \overline{C}$$

Fig. 9.3.16

Refere Fig. 9.3.17.

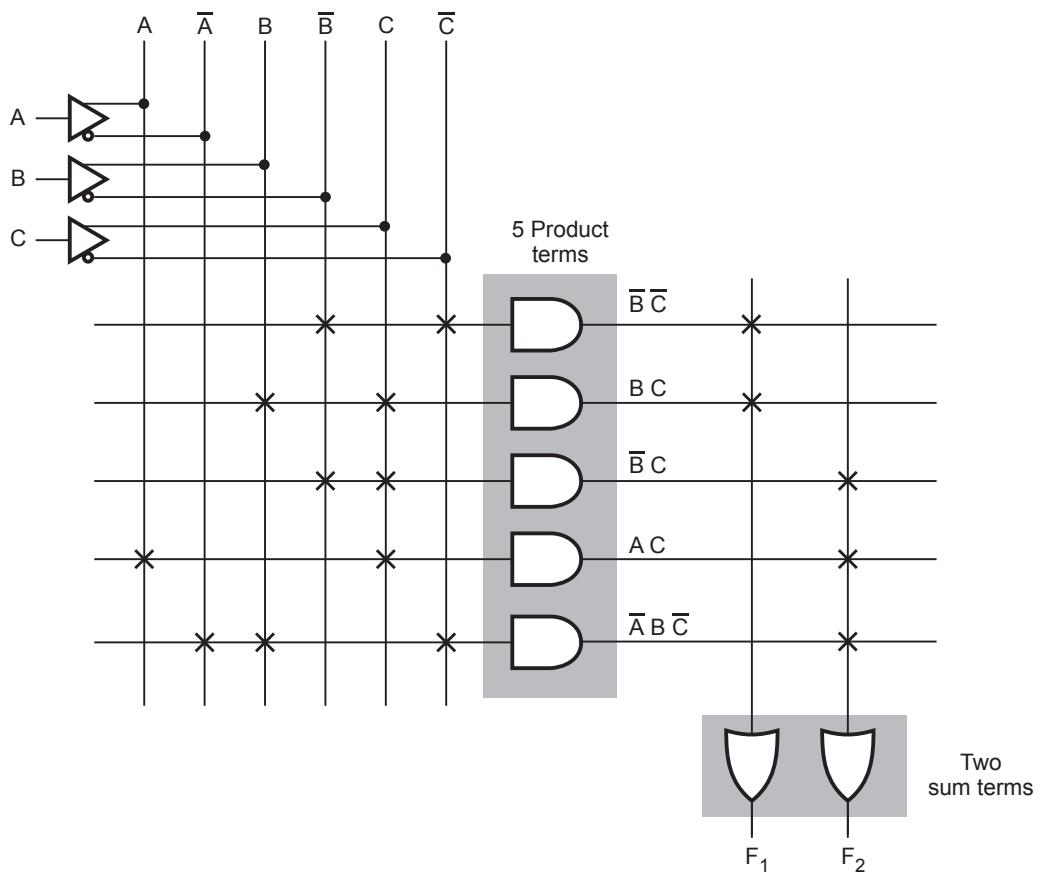


Fig. 9.3.17

Example 9.3.7 Design using PLD a 3 : 8 decoder.

SPPU : May-10, Marks 8; Dec.-13, May-16 Marks 4

Solution : The Fig. 9.3.18 shows 3 : 8 decoder using PLD.

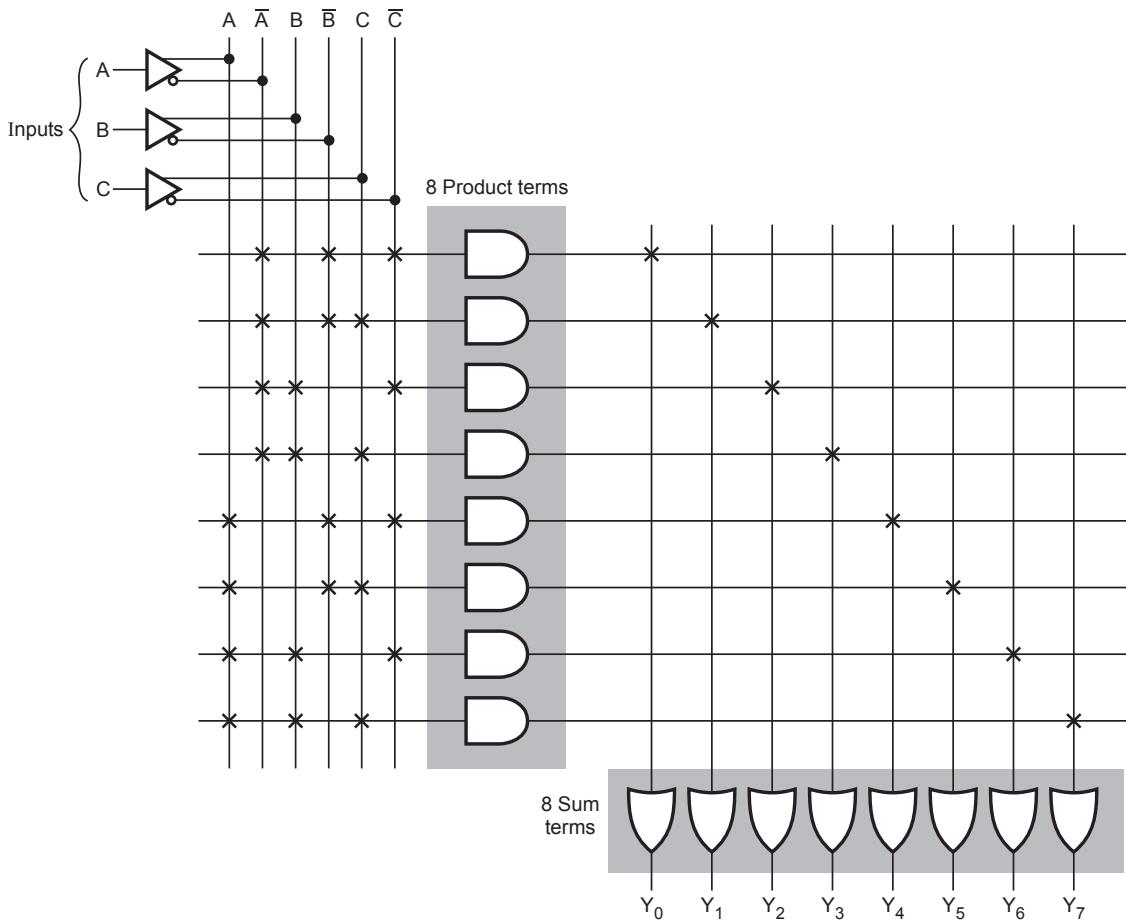


Fig. 9.3.18

Example 9.3.8 A combinational circuit is defined by the function

$$F_1(A, B, C) = \sum m(0, 1, 2, 4)$$

$$F_2(A, B, C) = \sum m(1, 3, 5, 6)$$

Implement this circuit with PLA.

SPPU : Dec.-13, Marks 7

Solution : K-map simplifications

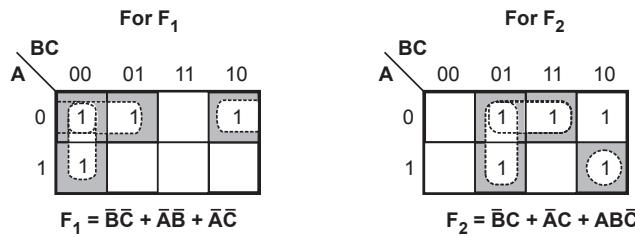


Fig. 9.3.19

Implementation : Refer Fig. 9.3.20.

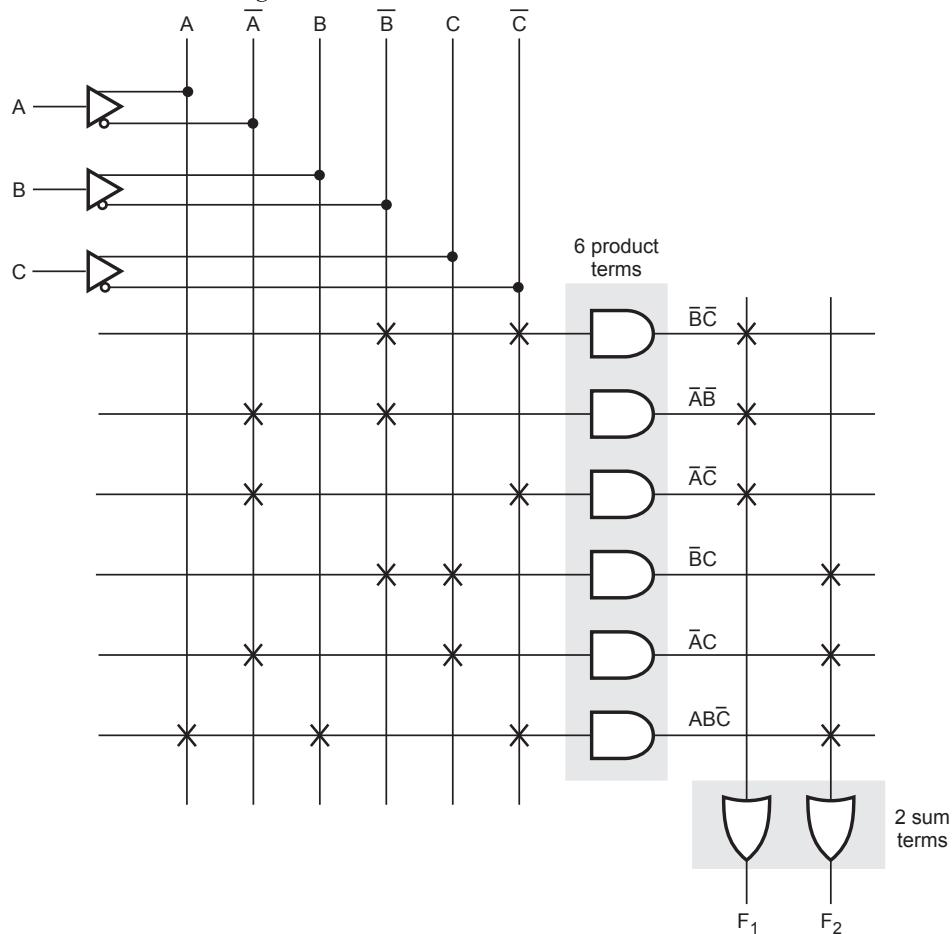


Fig. 9.3.20

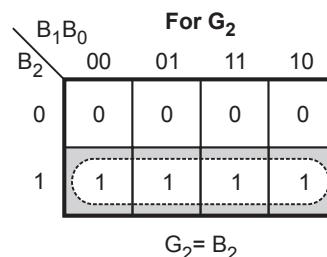
Example 9.3.9 Implement 3 bit binary to gray code converter using PLA.

SPPU : Dec.-16, May-18,19, Marks 6

Solution :

Binary code			Gray code		
B ₂	B ₁	B ₀	G ₂	G ₁	G ₀
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

K-map Simplification



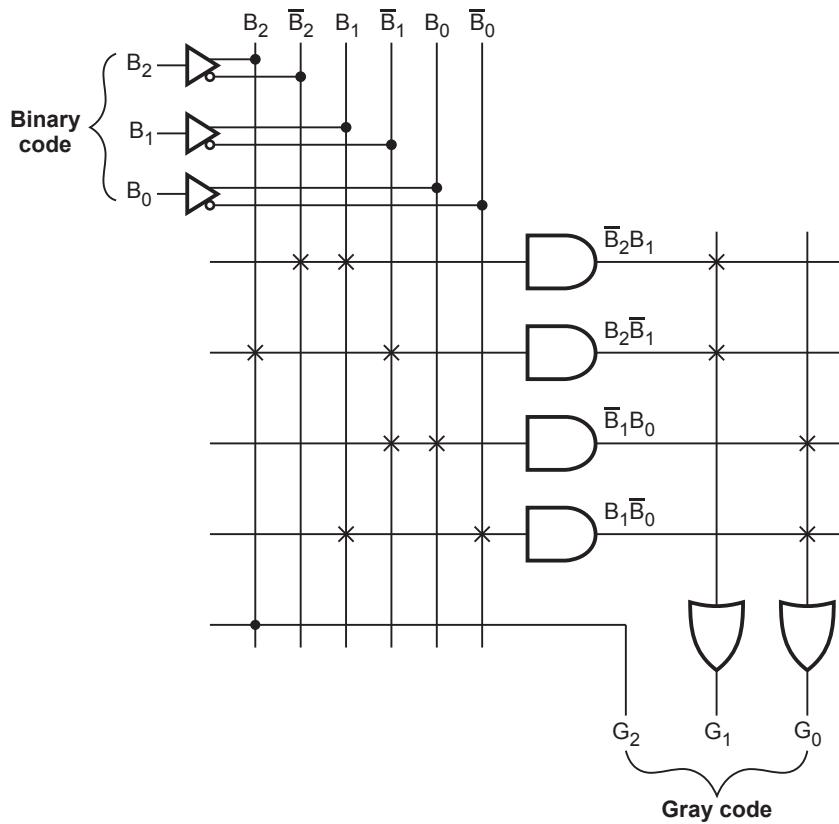
		For G_1				
		B ₁ B ₀	00	01	11	10
B ₂	0	0	0	1	1	
	1	1	1	0	0	

$$G_1 = \overline{B}_2 B_1 + B_2 \overline{B}_1$$

		For G_0				
		B ₁ B ₀	00	01	11	10
B ₂	0	0	1	0	1	
	1	0	1	0	1	

$$G_0 = \overline{B}_1 B_0 + B_1 \overline{B}_0$$

Implementation using PLA :



Example 9.3.10 Design 4 input and 6 output combinational circuit using PLA. The input variables are A, B, C and D :

$$Y_1 = \Sigma m (0, 3, 5, 6, 9, 10, 12, 15) \quad Y_2 = \Sigma m (0, 1, 2, 3, 11, 12, 14, 15)$$

$$Y_3 = \Sigma m (0, 4, 8, 12) \quad Y_4 = \Sigma m (0, 2, 3, 5, 7, 8, 12, 13)$$

$$Y_5 = \Sigma m (0, 1, 3, 4, 5, 6, 11, 13, 14, 15)$$

$$Y_6 = \Sigma m (1, 2, 6, 8, 15)$$

SPPU : May-17, Marks 6

Solution :

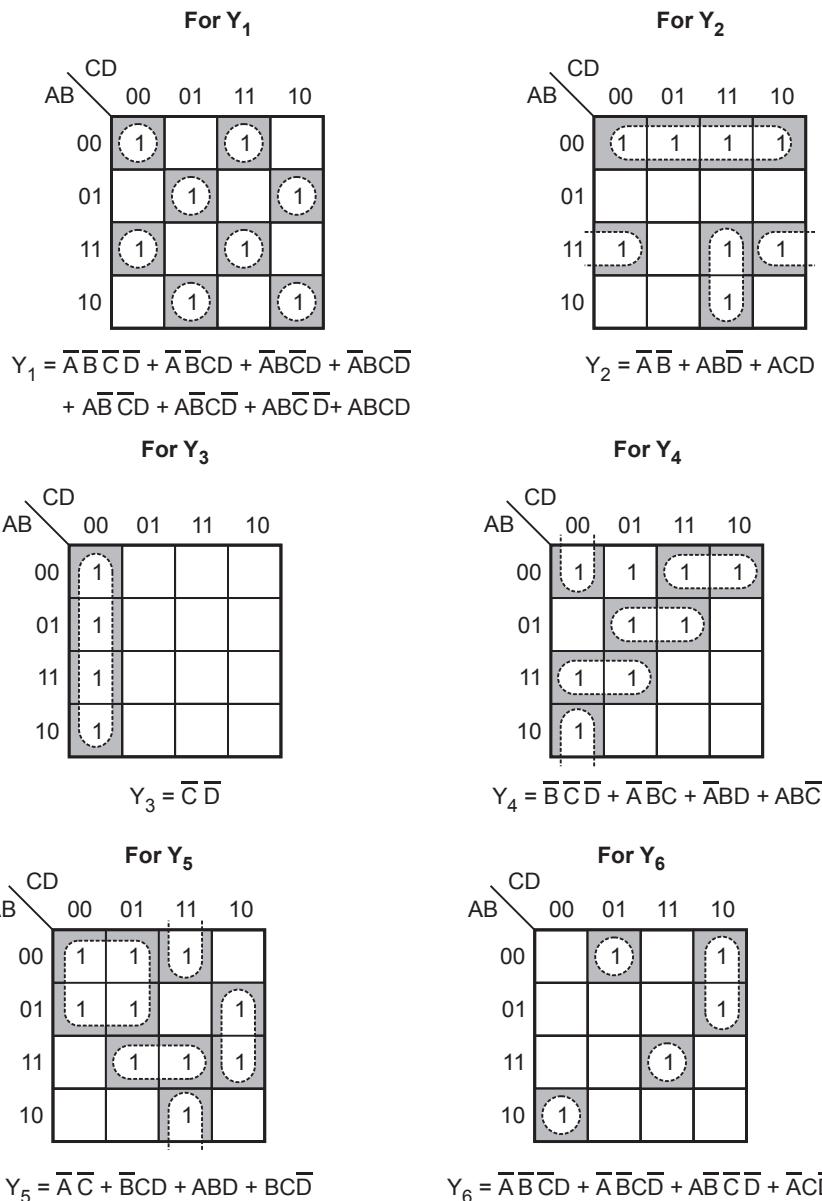


Fig. 9.3.21

After simplification for output functions we have realized that there are 23 product terms which are greater than possible 16 minterms.

To get minimal combinational circuit it is better to implement all 16 possible minterms as product terms as shown in the Fig. 9.3.22.

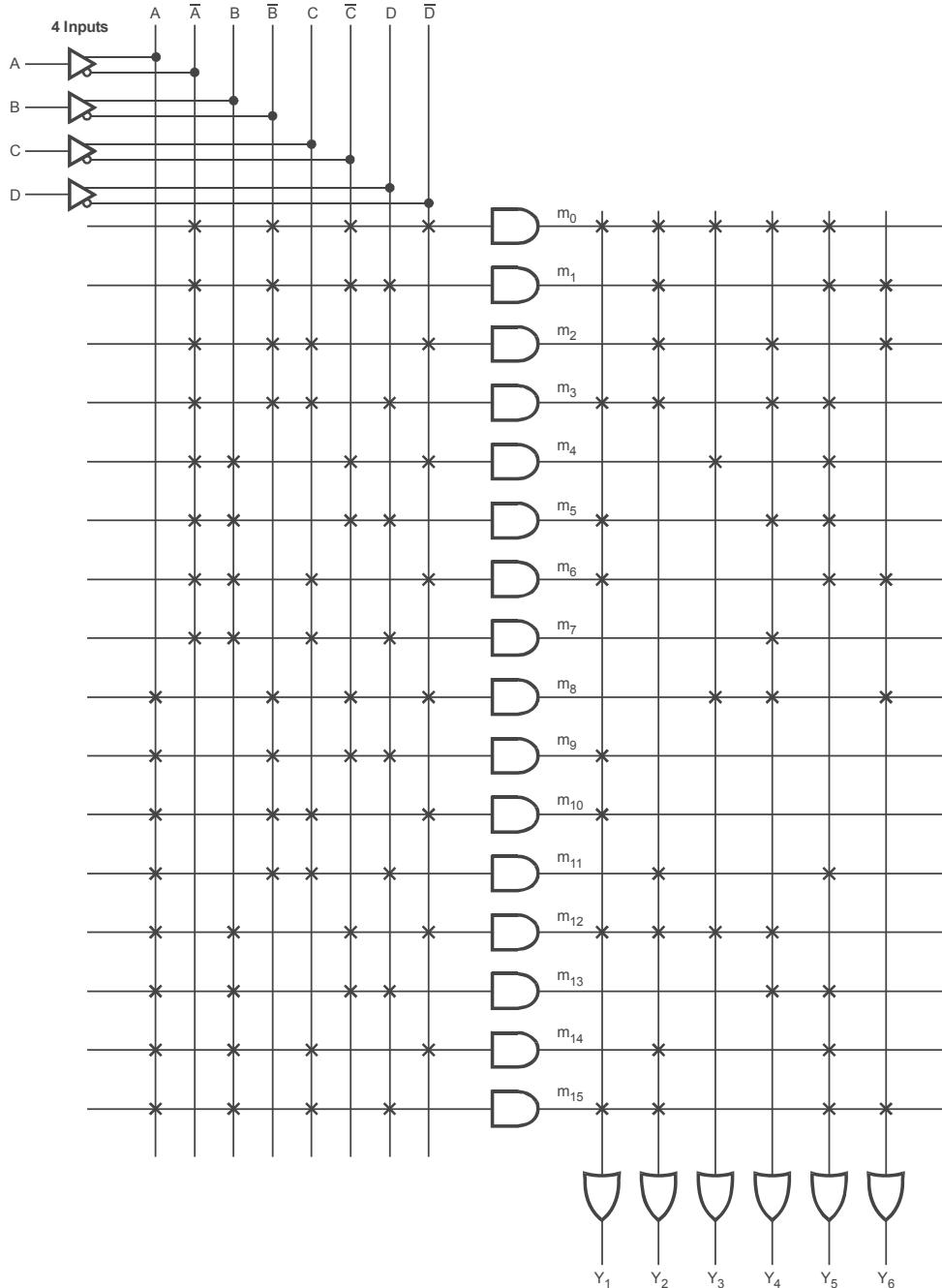


Fig. 9.3.22

Example 9.3.11 Implement the following functions using PLA :

$$F_1(A, B, C) = \sum m(1, 2, 4, 6)$$

$$F_2(A, B, C) = \sum m(0, 1, 6, 7)$$

SPPU : Dec.-19, Marks 6

Solution :

K-map simplification :

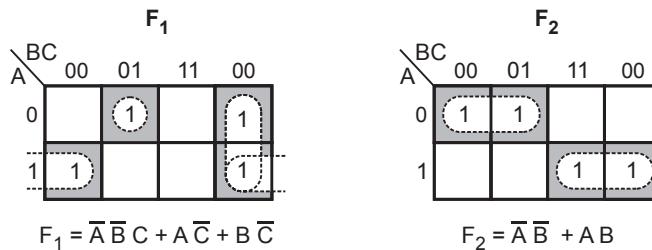


Fig. 9.3.23

Implementation :

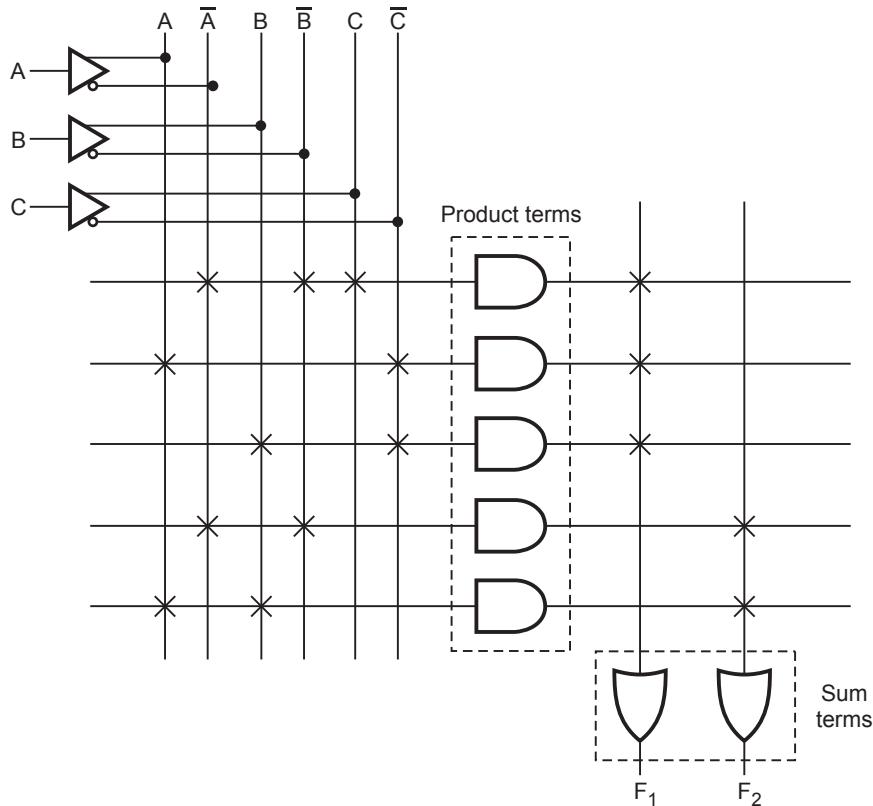


Fig. 9.3.24

Review Questions

1. Explain in brief the internal architecture of a PLA.

SPPU : Dec.-05, May-17, Marks 4

2. Explain PLA.

SPPU : Dec.-08, Marks 2

3. Explain in brief design model of PLA for any code conversion example.

SPPU : Dec.-10, Marks 8

4. Implement the following functions using PLA :

$$F_1(A,B,C) = \Sigma m(1, 2, 4, 6)$$

$$F_2(A,B,C) = \Sigma m(0, 1, 6, 7)$$

SPPU : May-13, Marks 8

5. Design 3 : 8 decoder using PLD.

SPPU : Dec.-13, Marks 4

6. What is PLA ? Explain the input buffer AND and OR matrix in PLA.

SPPU : May-14, Marks 6

7. A combinational circuit is defined by the function :

$$F1 = \Sigma m(3, 5, 7)$$

$$F2 = \Sigma m(4, 5, 7)$$

Implement the circuit with PLA having 3 input and 3 product term with 2 output.

SPPU : May-14, Marks 6

8. A combinational circuit is defined by following functions :

$$F1(A,B,C) = \sum m(0, 2, 4, 5), \quad F2(A,B,C) = \sum m(1, 3, 6, 7)$$

Implement this circuit using PLA.

SPPU : May-19, Marks 6

9.4 PAL (Programmable Array Logic)

SPPU : May-05, 11, 14, Dec.-08, 12, 13, 14, 18

We have seen that PLA is a device with a programmable AND array and programmable OR array. However, PAL programmable array logic is a programmable logic device with a fixed OR array and a programmable AND array. Because only AND gates are programmable, the PAL is easier to program, but is not as flexible as the PLA. Fig. 9.4.1 shows the array logic of a typical PAL. It has four inputs and four outputs. Each input has buffer and an inverter gate. It is important to note that two gates are shown with one composite graphic symbol with normal and complement outputs. There are four sections. Each section has three programmable AND gates and one fixed OR gate. The output of section 1 is connected to a buffer-inverter gate and then fed back into the inputs of the AND gates, through fuses. This allows the logic designer to feed an output function back as an input variable to create a new function. Such PALs are referred to as **Programmable I/O PALs**.

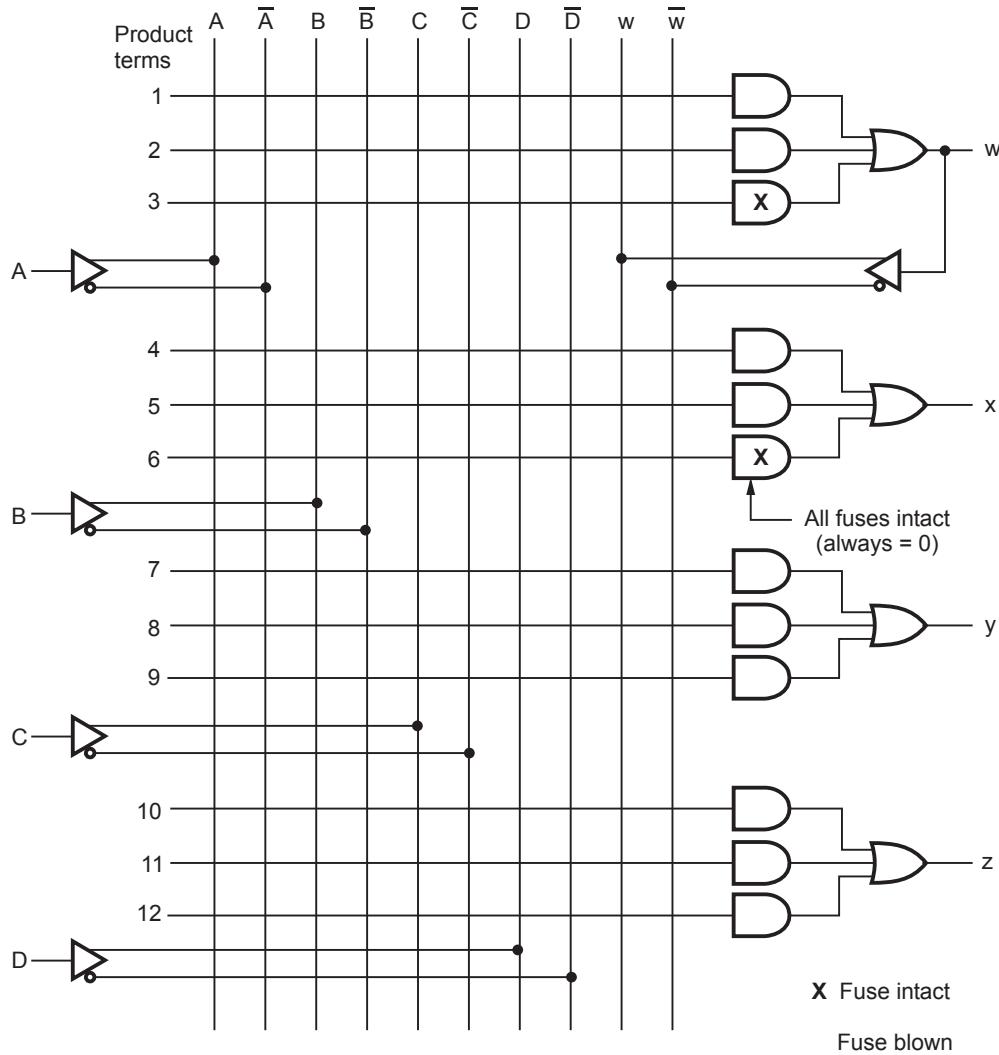


Fig. 9.4.1 Array logic for typical PAL

The commercial PAL devices have more gates than the one shown in Fig. 9.4.1. A typical PAL integrated circuit may have eight inputs, eight outputs, and eight sections, each consisting of an eight wide AND-OR array.

9.4.1 Implementation of Combinational Logic Circuit using PAL

Let us see the implementation of a combinational circuit using PAL with the help of examples.

Illustrative Examples

Example 9.4.1 Implement the following Boolean functions using PAL.

$$w(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13)$$

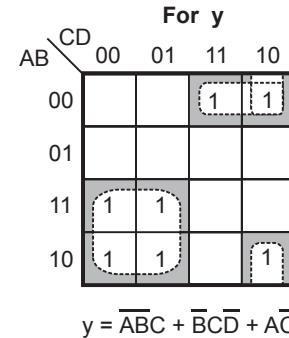
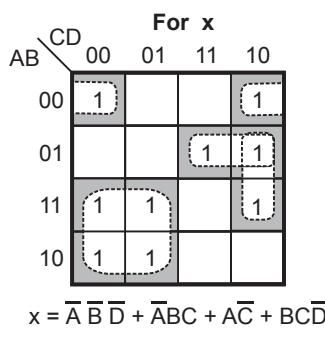
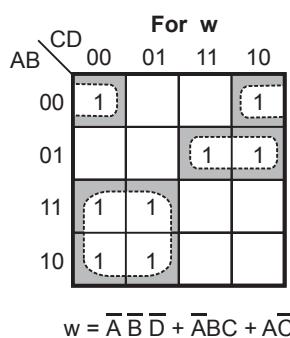
$$x(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13, 14)$$

$$y(A, B, C, D) = \sum m(2, 3, 8, 9, 10, 12, 13)$$

$$z(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 12, 14)$$

SPPU : May-14, Marks 7

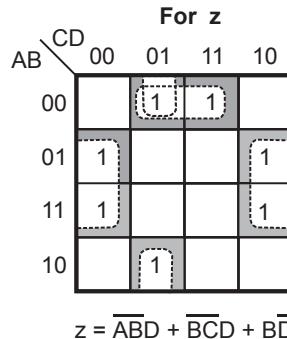
Solution : Step 1 : Simplify the four functions



$$w = \overline{A} \overline{B} \overline{D} + \overline{A} \overline{B} C + A \overline{C}$$

$$x = \overline{A} \overline{B} \overline{D} + \overline{A} \overline{B} C + A \overline{C} + B \overline{C} \overline{D}$$

$$y = \overline{A} \overline{B} C + \overline{B} \overline{C} \overline{D} + A \overline{C}$$



$$z = \overline{A} \overline{B} D + \overline{B} \overline{C} \overline{D} + B \overline{D}$$

Fig. 9.4.2 K-map simplification

Note that function x has four product terms. Three of them are equal to w. Therefore we can write $x = w + B \overline{C} \overline{D}$.

Step 2 : Implementation

In the last section we have seen the PLA program table. The program table for PAL is similar to PLA program table. Table 9.4.1 shows PAL program table with product terms, AND inputs and outputs.

Product term	AND Inputs					Outputs
	A	B	C	D	w	
1	0	0	—	0	—	$w = \overline{A} \overline{B} \overline{D} + \overline{A} BC + A \overline{C}$
2	0	1	1	—	—	
3	1	—	0	—	—	
4	—	—	—	—	1	$x = w + BCD$
5	—	1	1	0	—	
6	—	—	—	—	—	
7	0	0	1	—	—	$y = \overline{A} \overline{B} C + \overline{B} C \overline{D} + A \overline{C}$
8	—	0	1	0	—	
9	1	—	0	—	—	
10	0	0	—	1	—	$z = \overline{A} \overline{B} D + \overline{B} \overline{C} D + B \overline{D}$
11	—	0	0	1	—	
12	—	1	—	0	—	

Table 9.4.1 PAL program table

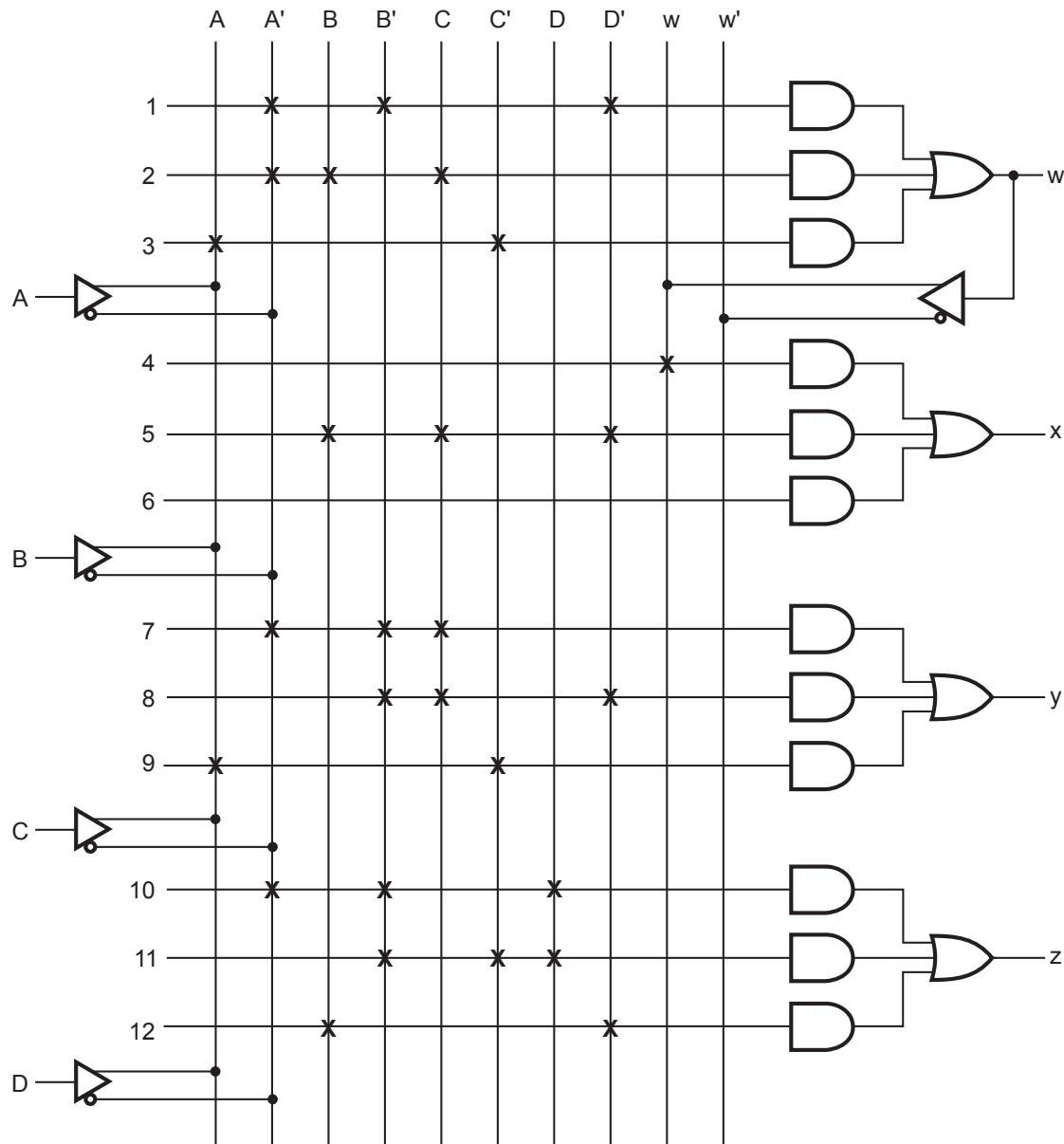


Fig. 9.4.3 Logic diagram

Example 9.4.2 Design BCD to Excess-3 converter using PAL.

Solution :

Step 1 : Derive the truth table of BCD to Excess-3 converter

Decimal	BCD code				Excess-3 code			
	B ₃	B ₂	B ₁	B ₀	E ₃	E ₂	E ₁	E ₀
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Table 9.4.2 Truth table for BCD to Excess-3 code converter

Step 2 : Simplify the Boolean functions for Excess-3 code outputs.

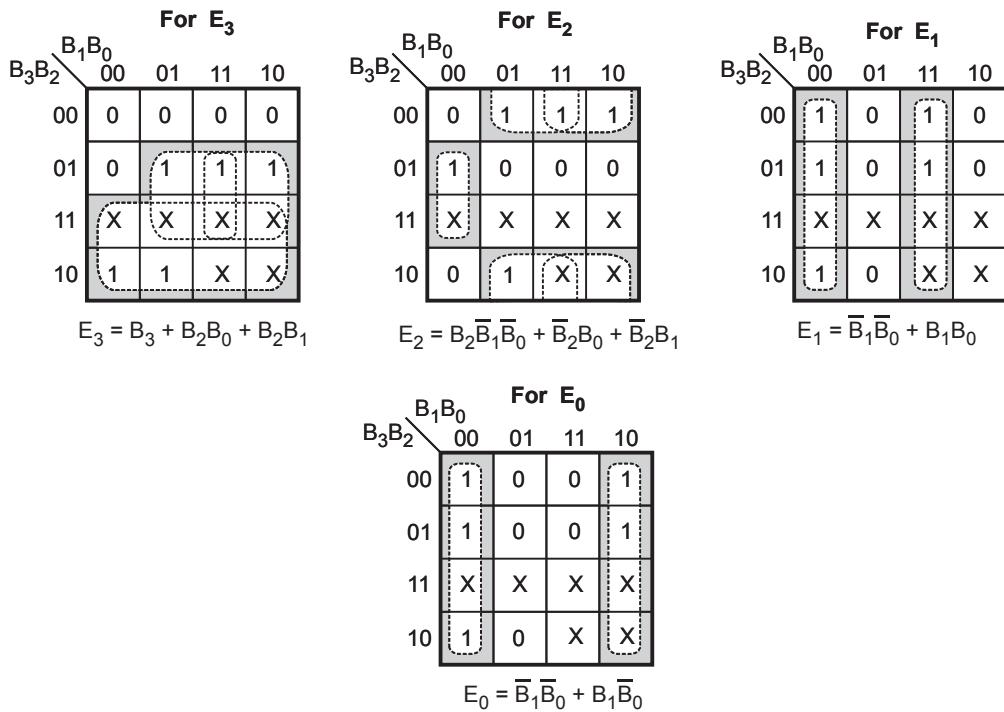
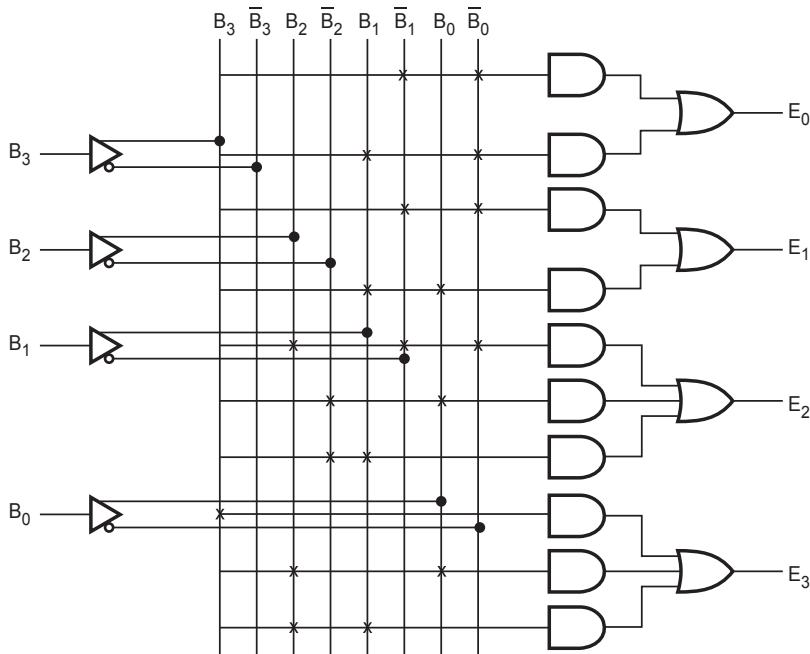


Fig. 9.4.4 K-map simplification

Step 3 : Implementation

Product terms	Inputs				Outputs			
	B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
B_3	1	1	—	—	—	1	—	—
$B_2 B_0$	2	—	1	—	1	1	—	—
$B_2 B_1$	3	—	1	1	—	1	—	—
$B_2 \bar{B}_1 \bar{B}_0$	4	—	1	0	0	—	1	—
$\bar{B}_2 B_0$	5	—	0	—	1	—	1	—
$\bar{B}_2 B_1$	6	—	0	1	—	—	1	—
$\bar{B}_1 \bar{B}_0$	7	—	—	0	0	—	—	1
$B_1 B_0$	8	—	—	1	1	—	—	1
$B_1 \bar{B}_0$	9	—	—	1	0	—	—	1
						T	T	T
								T/C

Table 9.4.3 PAL program table**Fig. 9.4.5 Logic diagram**

Example 9.4.3 Generate the following Boolean functions with a PAL with 4 inputs and 4 outputs.

$$Y_3 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}D, \quad Y_2 = \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + ABCD$$

$$Y_1 = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC\bar{D}, \quad Y_0 = ABCD$$

Solution : Step 1 : Simplify the Boolean functions

$$\begin{aligned} Y_3 &= \overline{A} B \overline{C} D + \overline{A} B C \overline{D} + A B \overline{C} D = (\overline{A} + A) B \overline{C} D + \overline{A} B C \overline{D} \\ &= B \overline{C} D + \overline{A} B C \overline{D} \end{aligned}$$

$$\begin{aligned} Y_2 &= \overline{A} B C \overline{D} + \overline{A} B C D + A B C D = \overline{A} B C (\overline{D} + D) + (\overline{A} + A) (B C D) \\ &= \overline{A} B C + B C D \end{aligned}$$

$$\begin{aligned} Y_1 &= \overline{A} B \overline{C} + \overline{A} B C + A \overline{B} C + A B \overline{C} \\ &= \overline{A} B (\overline{C} + C) + A \overline{B} C + (\overline{A} + A) B \overline{C} = \overline{A} B + A \overline{B} C + B \overline{C} \end{aligned}$$

$$Y_0 = A B C D$$

Step 2 : Implementation

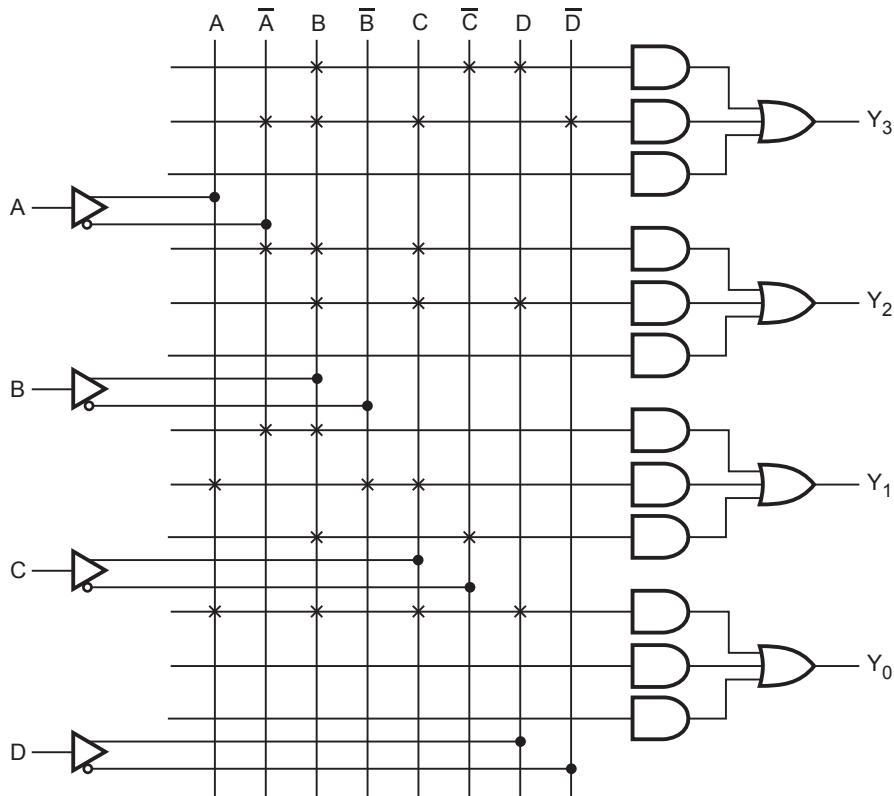


Fig. 9.4.6 Logic diagram

Example 9.4.4 Implement 4 : 1 multiplexer using PAL.

SPPU : Dec.-12,14, Marks 8

Solution : The Boolean function for 4 : 1 multiplexer is

$$Y = E \overline{S}_1 \overline{S}_0 D_0 + E \overline{S}_1 S_0 D_1 + E S_1 \overline{S}_0 D_2 + E S_1 S_0 D_3$$

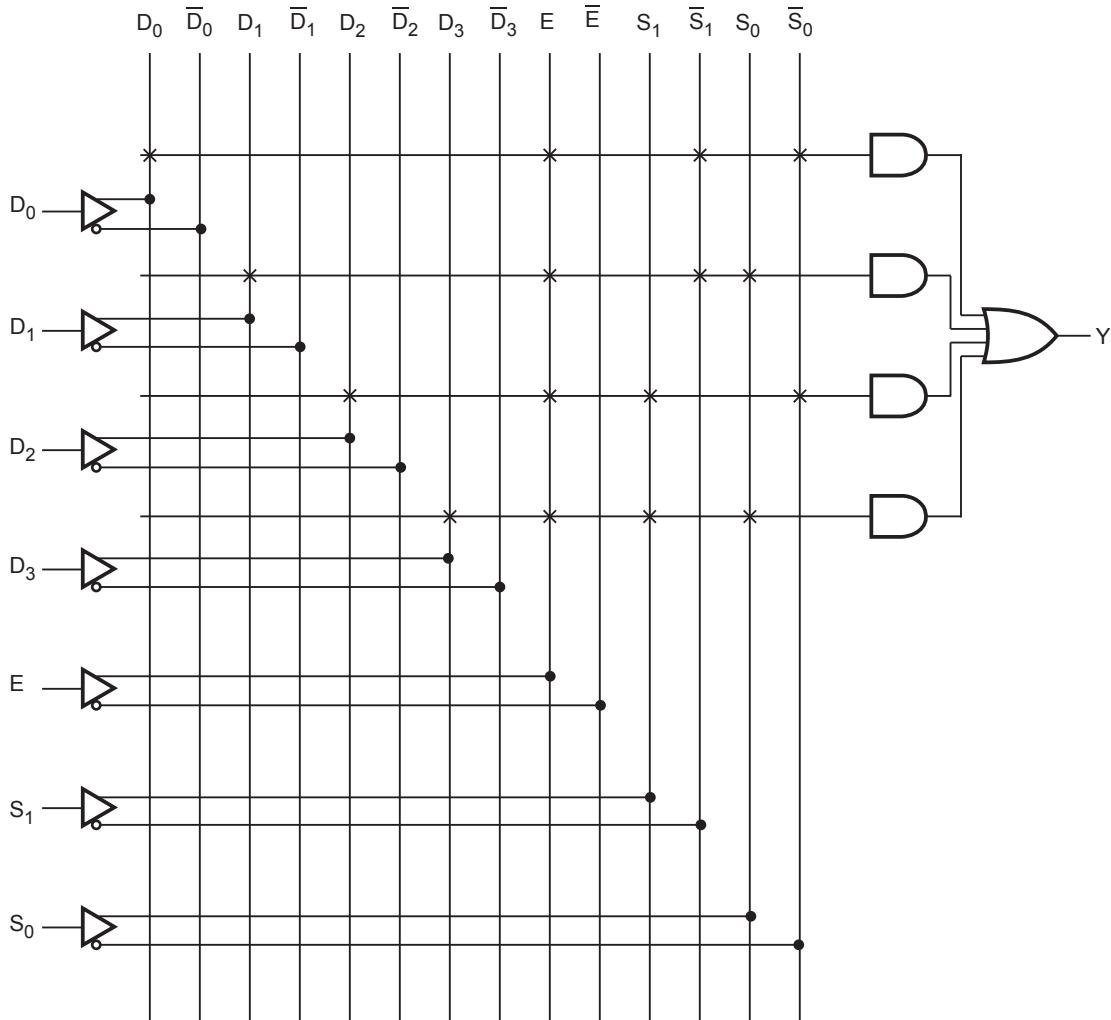


Fig. 9.4.7

Example 9.4.5 A combinational circuit is defined by the function

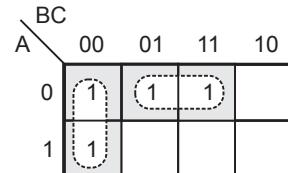
$$F_1(A, B, C) = \sum m(0, 1, 3, 4)$$

Implement this circuit with PAL.

SPPU : Dec.-13, Marks 8

Solution : K-map simplification

$$\therefore F_1 = \overline{B} \overline{C} + \overline{A} C$$



Implementation

Product term	AND inputs			Outputs
	A	B	C	
1	-	0	0	
2	0	-	1	

Table PAL program table

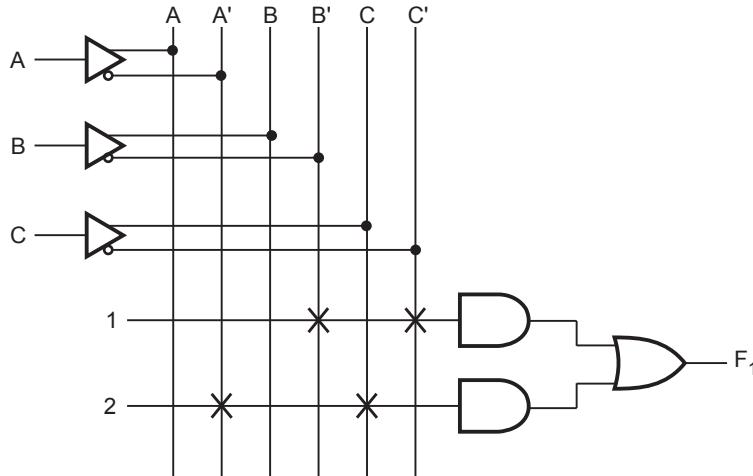


Fig. 9.4.8 Logic diagram

Example 9.4.6 Implement the following function using PAL :

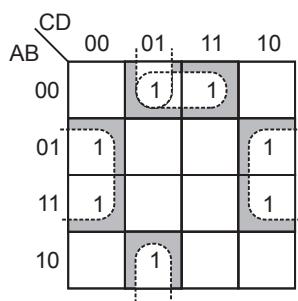
$$F1(A, B, C, D) = \sum m (1, 3, 4, 6, 9, 12, 14)$$

$$F2(A, B, C, D) = \sum m (1, 2, 3, 7, 12, 15).$$

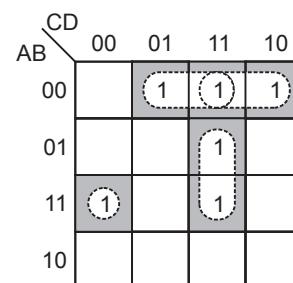
SPPU : Dec.-18, Marks 4

Solution :

Step 1 : K-map simplification



$$F1 = B D' + A' B' D + B' C' D$$



$$F2 = A B C' D' + A' B' D + A' B C + B C D$$

Fig. 9.4.9

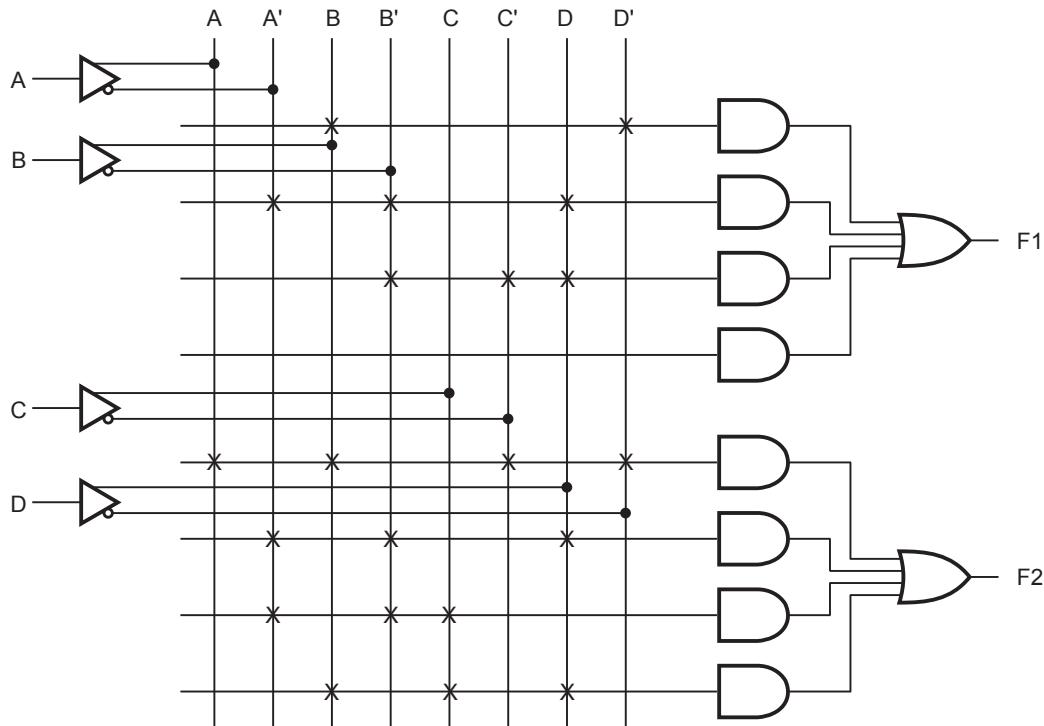


Fig. 9.4.9 (a)

Example for Practice

Example 9.4.6 : A combinational logic circuit is defined by the following function.
 $f_1(a, b, c) = \Sigma (0, 1, 6, 7)$, $f_2(a, b, c) = \Sigma (2, 3, 5, 7)$. Implement the circuit with a PAL having three inputs, three product terms and two outputs.

Review Questions

1. What is PAL ?
2. Explain PAL. SPPU : Dec.-08, Marks 2
3. Give the array logic symbol for eight input AND gate.
4. With the help of suitable example explain the basic fixed OR and programmable AND logic of PAL. SPPU : May-05, Marks 4
5. Explain the design model of PAL. SPPU : May-11, Marks 8
6. Implement the following Boolean function using PAL :
 $W(A, B, C, D) = \Sigma m(0, 2, 6, 7, 8, 9, 12, 13)$
 $x(A, B, C, D) = \Sigma m(0, 2, 6, 7, 8, 9, 12, 13, 14)$
 $y(A, B, C, D) = \Sigma m(2, 3, 8, 9, 10, 12, 13)$
 $z(A, B, C, D) = \Sigma m(1, 3, 4, 6, 9, 12, 14)$ SPPU : May-14, Marks 7

9.5 Comparison between PROM, PLA and PAL

SPPU : Dec.-05,06,07, May-06,07,08,15,16

Sr. No.	PROM	PLA	PAL
1.	AND array is fixed and OR array is programmable.	Both AND and OR arrays are programmable.	OR array is fixed and AND array is programmable.
2.	Cheaper and simple to use.	Costliest and complex than PAL and PROMs.	Cheaper and simpler.
3.	All minterms are decoded.	AND array can be programmed to get desired minterms.	AND array can be programmed to get desired minterms.
4.	Only Boolean functions in standard SOP form can be implemented using PROM.	Any Boolean functions in SOP form can be implemented using PLA.	Any Boolean functions in SOP form can be implemented using PLA.

Review Question

- What is the difference between PLA, PAL and PROM ?

SPPU : Dec.-05,06,07, May-06,07,08,15,16, Marks 4



Notes

UNIT - V

10

Logic Families

Syllabus

Classification of logic families : Unipolar and Bipolar Logic Families, Characteristics of Digital ICs : Fan-in, Fan-out, Current and voltage parameters, Noise immunity, Propagation Delay, Power Dissipation, Figure of Merits, Operating Temperature Range, power supply requirements.

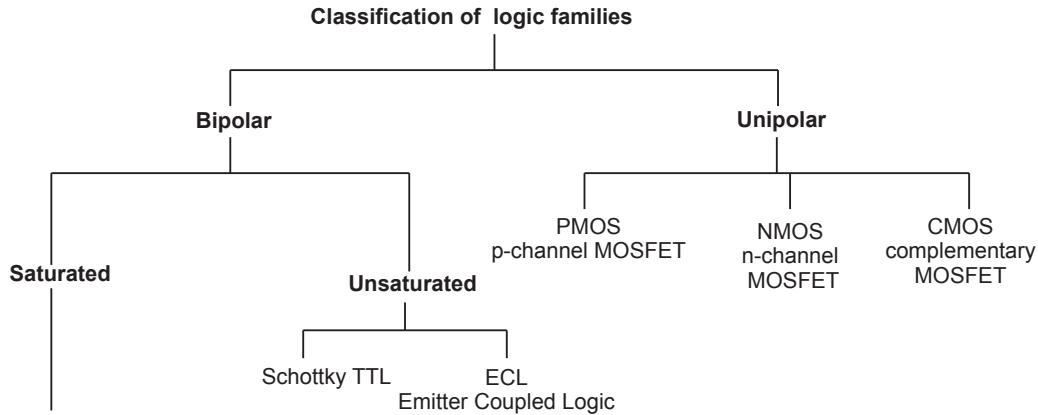
Transistor-Transistor Logic : Operation of TTL NAND Gate (Two input), TTL with active pull up, TTL with open collector output, Wired AND Connection, Tristate TTL Devices, TTL characteristics. **CMOS :** CMOS Inverter, CMOS characteristics, CMOS configurations- Wired Logic, Open drain outputs.

Contents

10.1	Classification of Logic Families	Dec.-08,14,16,17, May-10,14,18,	Marks 4
10.2	Characteristics of Digital ICs	Dec.-08,18, May-17	Marks 4
10.3	Transistor-Transistor Logic (TTL)	May-05,06,07,08,10,12,13,14,15, 16,17,18,19, Dec.-04,05,06,07,08,10, 12,13,15,17,18,19 Marks 8
10.4	Complementary MOS (CMOS)	May-05,06,07,08,11,12,13,14,15, 16,17,18, Dec.-04,05,06,07,08,10,11, Dec.-12,14,17,18,19 Marks 10
10.5	Interfacing TTL and CMOS Families	Dec.-18, Marks 8
10.6	Comparison between TTL and CMOS Families May-15,16,19, Dec.-13,19 Marks 6

10.1 Classification of Logic Families SPPU : Dec.-08,14,16,17, May-10,14,18

A digital logic family is a group of compatible devices with the same logic levels and supply voltages. According to components used in the logic family, digital logic families are classified as shown in the Fig. 10.1.1.



- **RTL** : Register Transistor Logic
- **DTL** : Diode Transistor Logic
- **DCTL** : Direct Coupled Transistor Logic
- **I²L** : Integrated Injection Logic
- **HTL** : High Threshold Logic
- **TTL** : Transistor Transistor Logic

Fig. 10.1.1 Classification of logic families

- Logic families are basically classified into two categories. They are
 1. Bipolar logic families
 2. Unipolar logic families
- **Bipolar logic families** : The main elements of a bipolar logic families are diodes and transistors. These are further divided into two types based on BJT operating mode. They are :
 1. Saturated
 2. Non-saturated
- In saturated logic, the transistors are driven to saturation mode, the saturated bipolar logic families are :

1. Resistor-Transistor Logic (RTL)	2. Diode Transistor Logic (DTL)
3. Direct Coupled Transistor Logic (DCTL)	4. Integrated Injection Logic (IIL)
5. High Threshold Logic (HTL)	6. Transistor Transistor Logic (TTL)
- The non saturated bipolar logic families are :
 1. Schottky TTL
 2. Emitter Coupled Logic (ECL)
- **Unipolar logic families** : MOS devices are unipolar devices and only MOSFETs are employed in these MOS logic circuits. The MOS logic families are :
 1. PMOS
 2. NMOS
 3. CMOS

Review Question

1. What is logic family ? Give the classification of logic families.

SPPU : May-10,14,18, Dec.-08,14,16,17, Marks 4

10.2 Characteristics of Digital ICs

SPPU : Dec.-08,18, May-17

Propagation Delay : The propagation delay of a gate is basically the time interval between the application of an input pulse and the occurrence of the resulting output pulse. The propagation delay is a very important characteristic of logic circuits because it limits the speed at which they can operate. The shorter the propagation delay, the higher the speed of the circuit and vice-versa.

Power Dissipation : The amount of power that an IC dissipates is determined by the average supply current, I_{CC} , that it draws from the V_{CC} supply. It is the product of I_{CC} and V_{CC} .

Current and Voltage Parameter

$V_{IH(min)}$ - High-Level Input Voltage : It is the minimum voltage level required for a logical 1 at an input. Any voltage below this level will not be accepted as a HIGH by the logic circuit.

$V_{IL(max)}$ - Low-Level Input Voltage : It is the maximum voltage level required for a logic 0 at an input. Any voltage above this level will not be accepted as a LOW by the logic circuit.

$V_{OH(min)}$ - High-Level Output Voltage : It is the minimum voltage level at a logic circuit output in the logical 1 state under defined load conditions.

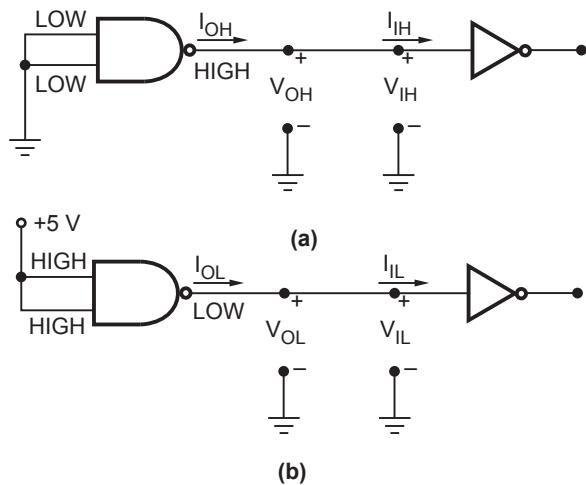


Fig. 10.2.1 Currents and voltages in the two logic states

$V_{OL(max)}$ - Low-Level Output Voltage : It is the maximum voltage level at a logic circuit output in the logical 0 state under defined load conditions.

I_{IH} - High-Level Input Current : It is the current that flows into an input when a specified high-level voltage is applied to that input.

I_{IL} - Low-Level Input Current : It is the current that flows into an input when a specified low-level voltage is applied to that input.

I_{OH} - High-Level Output Current : It is the current that flows from an output in the logical 1 state under specified load conditions.

I_{OL} - Low-Level Output Current : It is the current that flows from an output in the logical 0 state under specified load conditions.

Noise Margin : The **noise immunity** of a logic circuit refers to the circuit's ability to tolerate the noise without causing spurious changes in the output voltage. To avoid this problem due to noise, voltage level $V_{IH(min)}$ is kept at a few fraction of volts below $V_{OH(min)}$ and voltage level $V_{IL(max)}$ is kept above $V_{OL(max)}$, at the design time.

V_{NH} is the difference between the lowest possible HIGH output, $V_{OH(min)}$ and the minimum voltage, $V_{IH(min)}$ required for a HIGH input. This voltage difference, V_{NH} is called high-state noise margin. Similarly, we have low-state noise margin. It is the voltage difference between the largest possible low output, $V_{OL(max)}$ and the maximum voltage, $V_{IL(max)}$ required for a LOW input.

In short we can write as,

$$V_{NH} = V_{OH(min)} - V_{IH(min)} \quad \text{and}$$

$$V_{NL} = V_{IL(max)} - V_{OL(max)}$$

Fan-in and Fan-out : The maximum number of inputs of several gates that can be driven by the output of a logic gate is decided by the parameter called **fan-out**. In general, the fan-out is defined as the maximum number of inputs of the same IC family that the gate can drive maintaining its output levels within the specified limits.

The **fan-in** of a digital logic gate refers to the number of inputs.

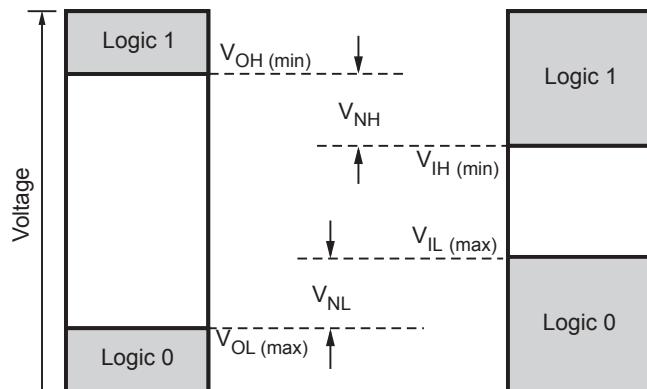


Fig. 10.2.2 Noise margins

Speed Power Product (Figure of Merit)

- In general, for any digital IC, it is desirable to have shorter propagation delays (higher speed) and lower values of power dissipation. There is usually a trade-off between switching speed and power dissipation in the design of a logic circuit i.e. speed is gained at the expense of increased power dissipation. Therefore, a common means for measuring and comparing the overall performance of an IC family is the **Speed-Power Product (SPP)**. It is also called **Figure of Merit**.

Current Sinking

- A device output is said to **sink current** when current flows from the power supply, through the load and through the device output to ground. This is illustrated in Fig. 10.2.3 (a).

Current Sourcing

- A device output is said to **source current** when current flows from the power supply, out of the device output and through the load to ground. This is illustrated in Fig. 10.2.3 (b).

Operating Temperature Range

- It is the temperature range specified by the logic family within which devices are guaranteed to work reliably.

Power Supply Requirements

- Power supply requirements differ from logic family to family. For example, it is 5V for TTL family and 3-15 volts for CMOS family. Further more, power supply tolerance also depends on logic family. For example, for 74 series TTL family it is ± 0.25 V and for 54 series TTL family it is ± 0.5 V.

Review Questions

- State and explain any four characteristics of digital ICs. **SPPU : May-17, Dec.-08,18, Marks 4**
- Define 1) V_{OH} , V_{IL} 2) V_{OL} , V_{IL} 3) Noise margin.
- Define fan-out.
- Define fan-in.
- What is propagation delay ?
- What is noise margin ?
- Define current sinking and current sourcing.
- What is speed power product ?

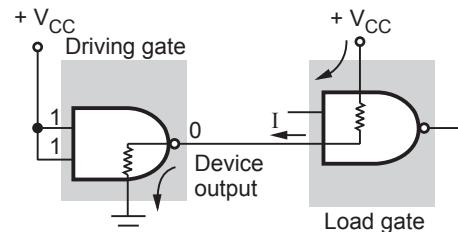


Fig. 10.2.3 (a) Current sinking

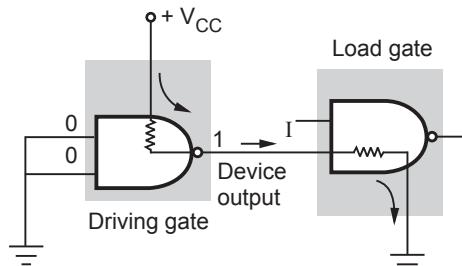


Fig. 10.2.3 (b) Current sourcing

10.3 Transistor-Transistor Logic (TTL)

**SPPU : May-05,06,07,08,10,12,13,14,15,16,17,18,19,
Dec.-04,05,06,07,08,10,12,13,15,17,18,19**

- Transistor-transistor logic, TTL, is named for its dependence on transistors alone to perform basic logic operations. The first version, which is now known as standard TTL, was developed in 1965 and is rarely used in today's systems. Through the years, the basic design has been modified to improve its performance in several respects and as a consequence, a number of subfamilies have evolved. In this section we are going to study the basic transistor configurations in TTL and its subfamily circuits along with their characteristics.

10.3.1 2-Input TTL NAND Gates

- The Fig. 10.3.1 (a) shows the circuit diagram of 2-input NAND gate. Its input structure consists of multiple-emitter transistor and output structure consists of totem-pole output. Here, Q_1 is an NPN transistor having two emitters, one for each input to the gate. Although this circuit looks complex, we can simplify its analysis by using the diode equivalent of the multiple-emitter transistor Q_1 , as shown in Fig. 10.3.1 (b). Diodes D_2 and D_3 represent the two E-B junctions of Q_1 and D_4 is the collector-base (C-B) junction.

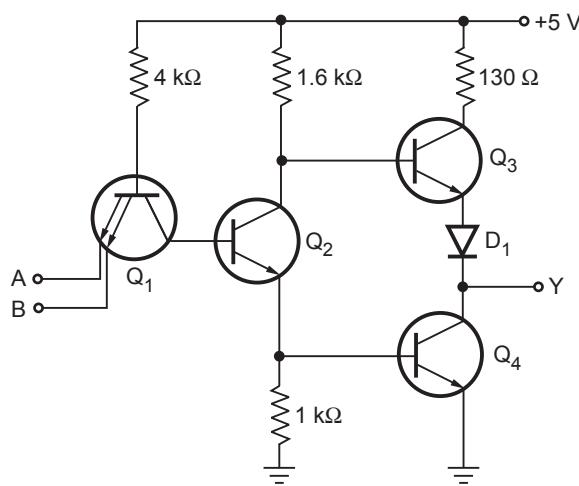


Fig. 10.3.1 (a) Two input TTL NAND gate

- The input voltages A and B are either LOW (ideally grounded) or HIGH (ideally + 5 volts). If either A or B or both are low, the corresponding diode conducts and the base of Q_1 is pulled down to approximately 0.7 V. This reduces the base voltage of Q_2 to almost zero. Therefore, Q_2 cuts off. With Q_2 open, Q_4 goes into cut-off and the Q_3 base is pulled HIGH. Since Q_3 acts as an emitter follower, the Y output is pulled up to a HIGH voltage. On the other hand, when A and B both are HIGH, the emitter diode of Q_1 are reversed biased making them off. This causes the collector diode D_4 to go into forward conduction. This forces Q_2 base to go HIGH. In turn, Q_4 goes into saturation, producing a low output. Table 10.3.1 summarizes all input and output conditions.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

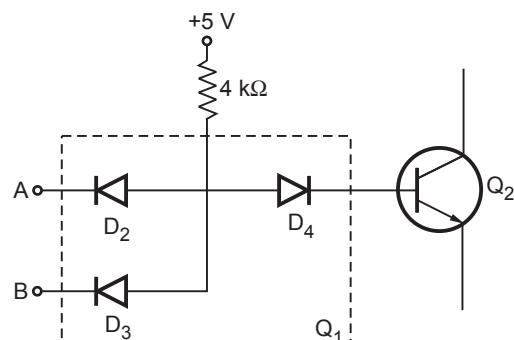


Fig. 10.3.1 (b) Diode equivalent for Q1

Table 10.3.1 Truth table for 2-input NAND gate

- Without diode D₁ in the circuit, Q₃ will conduct slightly when the output is low. To prevent this, the diode is inserted; its voltage drop keeps the base-emitter diode of Q₃ reverse-biased. In this way, only Q₄ conducts when the output is low.

10.3.2 Totem-Pole Output / Active Pull-Up

- Fig. 10.3.2 shows an highlighted output configuration. Transistor Q₃ and Q₄ form a totem-pole. Such a configuration is known as **active pull-up** or **totem pole** output.

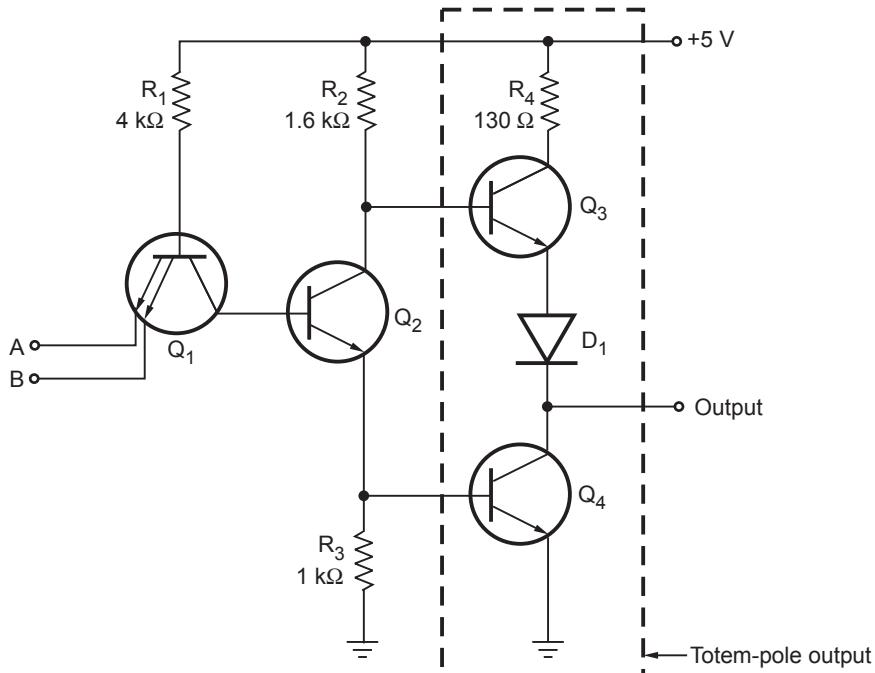


Fig. 10.3.2 Two input NAND gate with totem-pole output

- The active pull-up formed by Q_3 and Q_4 has specific advantage. Totem-pole transistors are used because they produce a LOW output impedance.
- Either Q_3 acts as an emitter follower (HIGH output), or Q_4 is saturated (LOW output).
- When Q_3 is conducting, the output impedance is approximately $70\ \Omega$; when Q_4 is saturated, the output impedance is only $12\ \Omega$. Either way, the output impedance is low. This means that the output voltage can change quickly from one state to the other because any stray output capacitance is rapidly charged or discharged through the low output impedance. Thus the propagation delay is low in totem-pole TTL logic.

10.3.3 Wired Logic - Open Collector Output

- One problem with totem pole output is that two outputs cannot be tied together. See Fig. 10.3.3, where the totem pole outputs of two separate gates are connected together at point X.
- Suppose that the output of gate A is high (Q_{3A} ON and Q_{4A} OFF) and the output of gate B is low (Q_{3B} OFF and Q_{4B} ON). In this situation transistor Q_{4B} acts as a load for Q_{3A} . Since Q_{4B} is a low resistance load, it draws high current around $55\ \text{mA}$. This current might not damage Q_{3A} or Q_{4B} immediately, but over a period of time can cause overheating and deterioration in performance and eventual device failure.

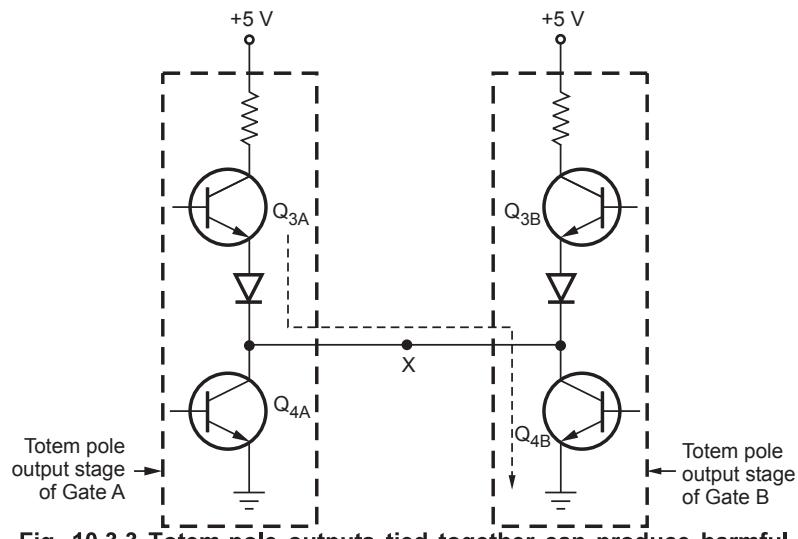


Fig. 10.3.3 Totem-pole outputs tied together can produce harmful current

- Some TTL devices provide another type of output called **open collector output**. The outputs of two different gates with open collector output can be tied together. This is known as **wired logic**.

- Fig. 10.3.4 shows a 2-input NAND gate with an open-collector output which eliminates the pull-up transistor Q_3 , D_1 and R_4 . The output is taken from the open collector terminal of transistor Q_4 .
- Because the collector of Q_4 is open, a gate like this will not work properly until you connect an external pull-up resistor, as shown in Fig. 10.3.5.

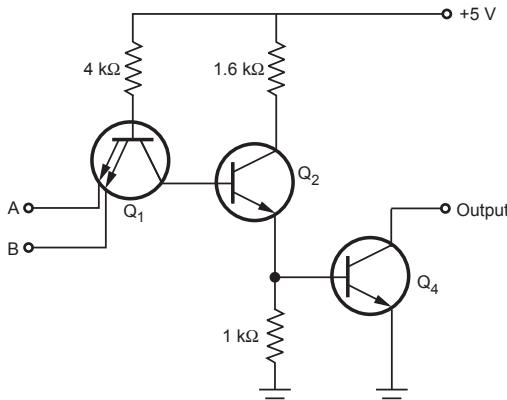


Fig. 10.3.4 Open collector 2-input TTL NAND gate

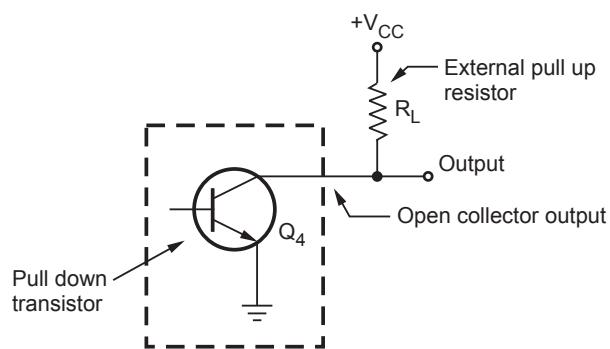
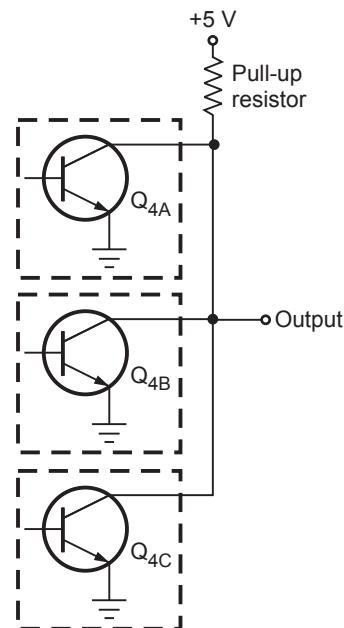
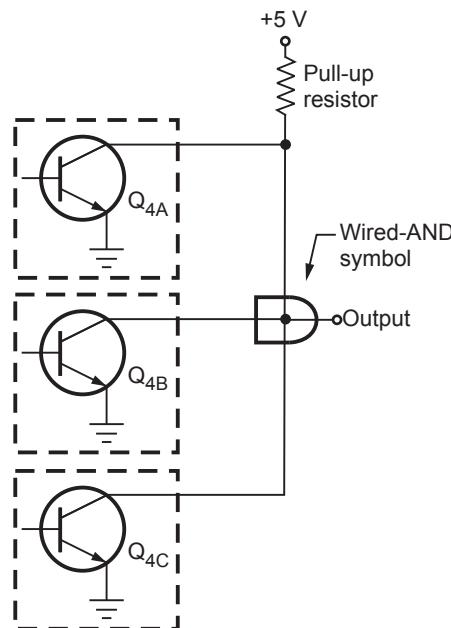


Fig. 10.3.5 Open collector output with pull-up resistor

- When Q_4 is ON, output is low and when Q_4 is OFF output is tied to V_{CC} through an external pull up resistor.



(a) Open collector outputs connected together



(b) Wired-AND output with special AND gate symbol

Fig. 10.3.6

- As mentioned earlier, the open collector outputs of two or more gates can be connected together, as shown in the Fig. 10.3.6 (a). The connection is called a **wired-AND** and represented schematically by the special AND gate symbol as shown in Fig. 10.3.6 (b).

10.3.4 Comparison between Totem-Pole and Open-Collector Outputs

Table 10.3.2 summarizes the difference between totem-pole and open collector outputs.

Sr. No.	Totem-pole	Open collector
1.	Output stage consists of pull-up transistor (Q_3), diode resistor and pull-down transistor (Q_4).	Output stage consists of only pull-down transistor.
2.	External pull-up resistor is not required.	External pull-up resistor is required for proper operation of gate.
3.	Output of two gates cannot be tied together.	Output of two gates can be tied together using wired AND technique.
4.	Operating speed is high.	Operating speed is low.

Table 10.3.2 Comparison of totem-pole and open collector output

10.3.5 Tri-state TTL Inverter

- The tristate configuration is a third type of TTL output configuration. It utilizes the high-speed operation of the totem-pole arrangement while permitting outputs to be wired-ANDED (connected together). It is called tristate TTL because it allows three possible output stages : **HIGH**, **LOW** and **high-impedance**.
- We know that transistor Q_3 is ON when output is HIGH and Q_4 is ON when output is LOW. In the high impedance state both transistors, transistors Q_3 and Q_4 in the totem-pole arrangement are turned OFF. As a result, the output is open or floating, it is neither LOW nor HIGH.
- Fig. 10.3.7 shows the simplified circuit for tristate inverter. It has two inputs A and E.
- A is the normal logic input whereas E is an ENABLE input. When ENABLE input is HIGH, the circuit works as a normal inverter. Because when E is HIGH, the state of the transistor Q_1 (either ON or OFF) depends on the logic input A, and the additional component diode is open circuited as its cathode is at logic HIGH.

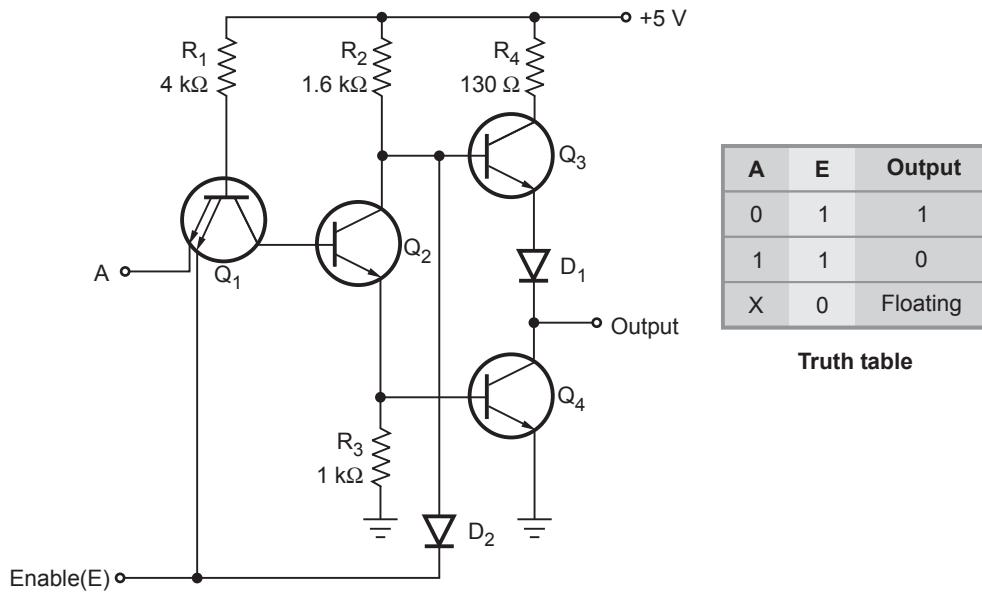
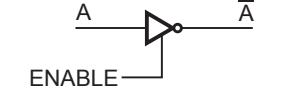
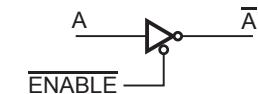


Fig. 10.3.7 Tristate TTL inverter

- When ENABLE input is LOW, regardless of the state of logic input A, the base-emitter junction of Q₁ is forward biased and as a result it turns ON. This shunts the current through R₁ away from Q₂ making it OFF.
- As Q₂ is OFF, there is no sufficient drive for Q₄ to conduct and hence Q₄ turns OFF.
- The LOW at ENABLE input also forward-biases diode D₂, which shunt the current away from the base of Q₃, making it OFF. In this way, when ENABLE input is LOW, both transistors are OFF and output is at high impedance state.
- Fig. 10.3.8 shows the logic symbols for tristate inverter. In above case circuit operation is enabled when ENABLE input is HIGH. Therefore, ENABLE input is active high. The logic symbol for active high enable input is shown in Fig. 10.3.8 (a). In some circuits ENABLE input can be active LOW, i.e. circuit operates when ENABLE input is LOW. The logic symbol for active low ENABLE input is shown in the Fig. 10.3.8 (b).



(a) Logic symbol for active high enable input



(b) Logic symbol for active low enable input

Fig. 10.3.8

10.3.6 Tri-state TTL NAND Gate

- Fig. 10.3.9 shows the tri-state 2-input TTL NAND gate. As shown in Fig. 10.3.9, the Q_1 has three inputs. Two of them are the inputs of NAND gate and the remaining input is an enable input (E).

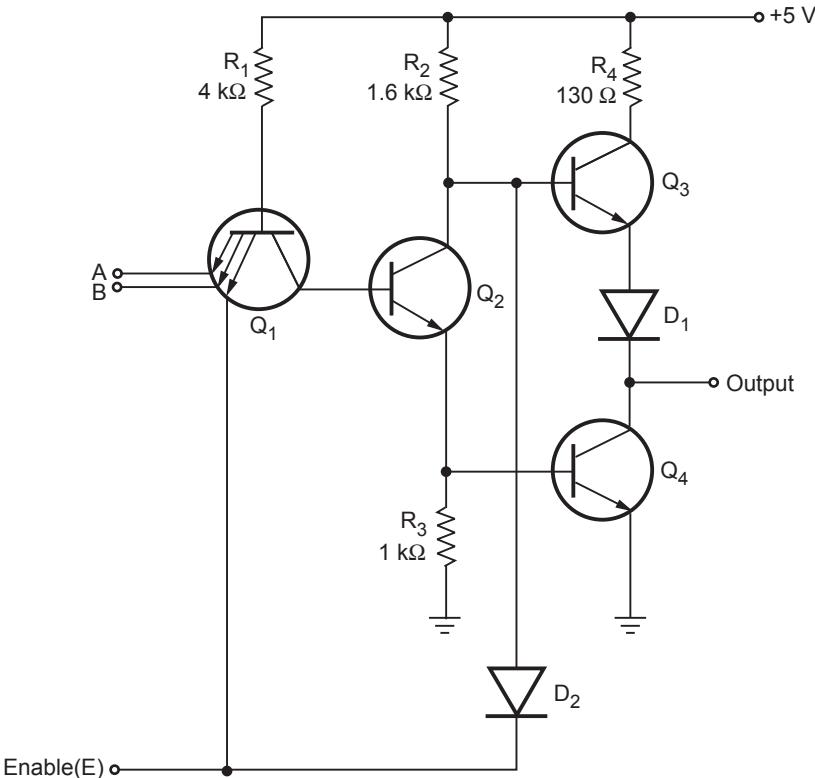


Fig. 10.3.9 Tri-state 2-input TTL NAND gate

- The function of enable input E and diode D_2 is same as that of tri-state inverter.
- When E input is HIGH, the state of transistor Q_1 (either ON or OFF) depends on the two inputs of NAND gate and the circuit will operate as a two-input NAND gate.
- When E input is low, regardless of the state of logic inputs A and B. The base-emitter junction of Q_1 is forward biased and as a result it turns ON. This shunts the current through R_1 away from Q_2 making it OFF. As Q_2 is OFF, there is no sufficient drive for Q_4 to conduct and hence Q_4 turns off. The LOW at ENABLE input also forward-biases diode D_2 , which shunt the current away from

the base of Q_3 , making it OFF. In this way, when ENABLE input is LOW, both transistors are OFF and output is at high impedance state.

10.3.7 Standard TTL Characteristics

- In 1964 Texas Instruments Corporation introduced the standard TTL ICs, 54/74 series. There are several series/ subfamilies in the TTL family of logic devices. Let us see the characteristics of standard TTL family.

Supply voltage and temperature range

- Both the 74 series and 54 series operate on supply voltage of 5 V. The 74 series works reliably over the range 4.75 V to 5.25 V, while the 54 series can tolerate a supply variation of 4.5 to 5.5 V.
- The 74 series devices are guaranteed to work reliably over a temperature range of 0 to $^{\circ}\text{C}$ whereas 54 series devices can handle temperature variations from -55 to $^{\circ}\text{C}$.

Voltage levels and noise margin

- Table 10.3.3 shows the input and output logic voltage levels for the standard 74 series.
- Looking at Table 10.3.3 we can say that, in the worst case, there is a difference of 0.4 V between the driver output voltages and the required load input voltages. For instance, the worst-case low values are

$$V_{OL(max)} = 0.4 \text{ V driver output}$$

$$V_{IL(max)} = 0.8 \text{ V load input}$$

Similarly, the worst-case high values are

$$V_{OH(min)} = 2.4 \text{ V driver output}$$

$$V_{IH(min)} = 2 \text{ V load input}$$

- In either case, the difference is 0.4 V. This difference is called *noise margin*. For TTL, Low state noise margin, V_{NL} and high state noise margin, V_{NH} both are equal and 0.4 V. This is illustrated in Fig. 10.3.10.

Voltages	Minimum	Typical	Maximum
V_{OL}	—	0.2	0.4
V_{OH}	2.4	3.4	—
V_{IL}	—	—	0.8
V_{IH}	2.0	—	—

Table 10.3.3 Voltage levels

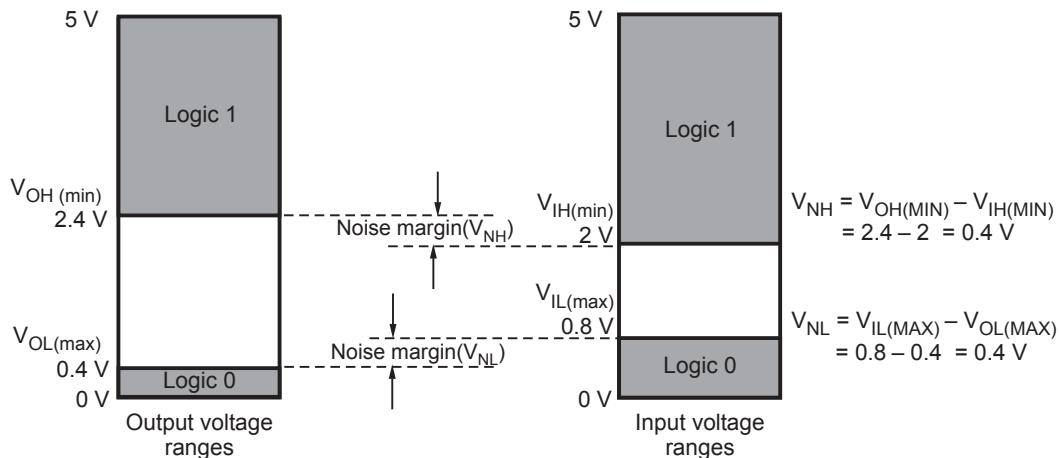


Fig. 10.3.10 TTL logic levels and noise margin

Power dissipation and propagation delay

- A standard TTL gate has an average power dissipation of about 10 mW.
- The propagation delay time of a TTL gate is approximately 10 nanoseconds.

Fan-out

- A standard TTL output can typically drive 10 standard TTL inputs. Therefore, standard TTL has fan-out 10.
- Table 10.3.4 summarizes the characteristics of standard TTL.

Characteristics	Values
Supply voltage	For 74 series - (4.75 to 5.25) units For 54 series - (4.5 to 5.5) units
Temperature range	For 74 series - (0 °C to 70 °C) For 54 series - (- 55 °C to 125 °C)
Voltage levels	$V_{OL(MAX)} - 0.4 \text{ V}$ $V_{OH(MIN)} - 2.4 \text{ V}$ $V_{IL(MAX)} - 0.8 \text{ V}$ $V_{IH(MIN)} - 2.0 \text{ V}$
Noise margin	0.4 V
Power dissipation	10 mW per gate
Propagation delay	Typically 10 ns
Fan-out	10

Table 10.3.4 Standard TTL characteristics

10.3.8 Advantages and Disadvantages of TTL Family

Advantages of TTL

1. High speed operation. Fastest among the saturated logic families. The propagation delay time is about 10 ns.

2. Moderate power dissipation.
3. Available in commercial and military versions.
4. Available for wide range of functions.
5. Low cost.
6. Moderate packaging density.

Disadvantages of TTL

1. Higher power dissipation than CMOS.
2. Lower noise immunity than CMOS.
3. Less fan-out than CMOS.

Review Questions

1. With neat circuit diagram explain the operation of two-input TTL NAND gates.

SPPU : May-06,10,13,17, Dec.-07,17, Marks 8

OR

Draw 2-input standard TTL NAND gate with totem pole. Explain operation of transistor (ON/OFF) with suitable input conditions and truth table.

SPPU : May-10,19, Dec.-12

OR

Explain the working of two input TTL NAND gate with active pull up. Consider various input, output states for explanation.

SPPU : May-12, Marks 8

2. What is totem-pole output ? Explain with the help of circuit diagram.

SPPU : Dec.-05, 06, May-05,08, Marks 6

- 3 Explain the wired logic output of TTL with neat diagram.

SPPU : Dec.-05,06,07, May-14, Marks 3

4. Draw and explain wired AND gate in detail.

SPPU : Dec.-18, Marks 6

5. Compare different types of output configurations in case of TTL family.

SPPU : Dec.-05, May-07, Marks 4

6. Give the advantages and disadvantages of totem-pole output stage arrangement.

SPPU : May-05, Dec.-07, Marks 4

7. Explain TTL open collector logic.

SPPU : May-18, Marks 5

8. Explain the advantages of open collector output.

SPPU : Dec.-06,15,17, May-08, Marks 4

9. What is tri-state ? What is the use of tri-state buffers ? Explain with suitable circuit diagram.

SPPU : May-07, Marks 4

10. Draw and explain tri-state TTL inverter.

SPPU : Dec.-05, 07, May-17,19, Marks 8

11. What do you mean by tri-state buffer ?

SPPU : May-05, 07, May-19, Marks 4

12. Explain the following characteristics of TTL logic families :

- i) Power dissipation ii) Noise margin iii) Propagation delay iv) Fan out.

OR

Explain standard TTL characteristics in detail.

SPPU : Dec.-08,10,12,13,17,19, May-10,13,15,16,19, Marks 8

10.4 Complementary MOS (CMOS)

SPPU : May-05,06,07,08,11,12,13,14,15,16,17,18, Dec.-04,05,06,07,08,10,11,12,14,17,18,19

10.4.1 CMOS Inverter

- Fig. 10.4.1 shows the basic CMOS inverter circuit. It consists of two MOSFETs in series in such a way that the P-channel device has its source connected to $+V_{DD}$ (a positive voltage) and the N-channel device has its source connected to ground. The gates of the two devices are connected together as the common input and the drains are connected together as the common output.

1. When input is HIGH, the gate of Q_1 (P-channel) is at 0 V relative to the source of Q_1 i.e. $V_{gs1} = 0$ V. Thus, Q_1 is OFF. On the other hand, the gate of Q_2 (N-channel) is at $+V_{DD}$ relative to its source i.e. $V_{gs2} = +V_{DD}$. Thus, Q_2 is ON. This will produce $V_{OUT} \approx 0$ V, as shown in the Fig. 10.4.2 (a).

2. When input is LOW, the gate of Q_1 (P-channel) is at a negative potential relative to its source while Q_2 has $V_{gs} = 0$ V. Thus, Q_1 is ON and Q_2 is OFF. This produces output voltage approximately $+V_{DD}$, as shown in the Fig. 10.4.2 (b).

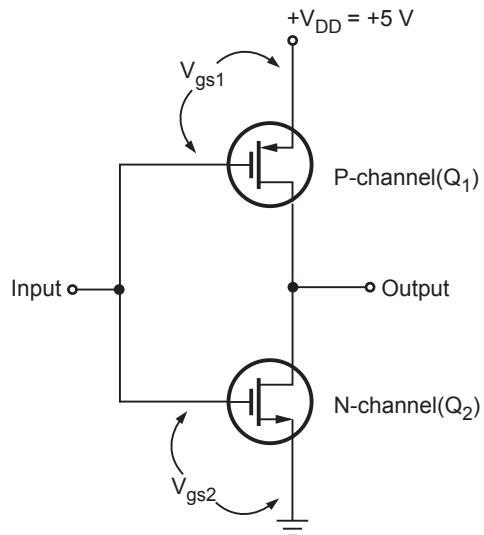


Fig. 10.4.1 CMOS inverter circuit

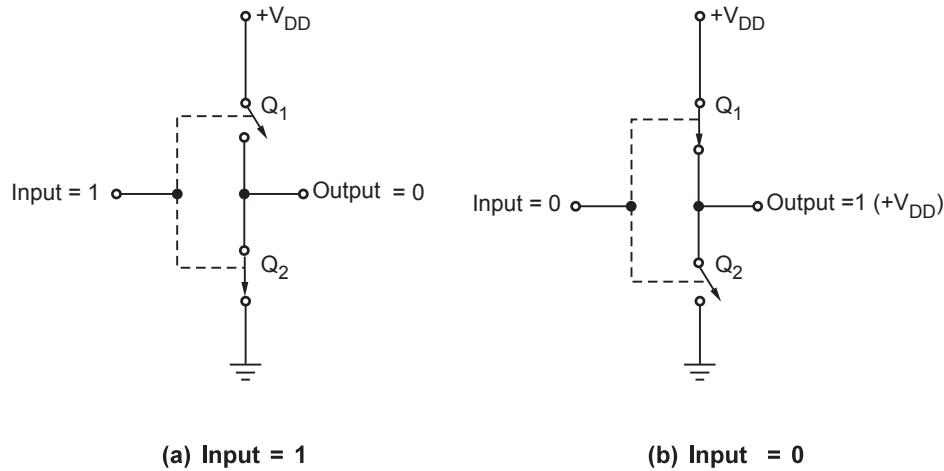


Fig. 10.4.2 Operation of CMOS inverter for both input conditions

- Table 10.4.1 summarizes the operation of CMOS inverter circuit

A	Q ₁	Q ₂	Output
0	ON	OFF	1
1	OFF	ON	0

Table 10.4.1 Truth table of inverter

- Fig. 10.4.3 shows, different symbols used for the p-channel and n-channel transistors to reflect their logical behaviour. The n-channel transistor (Q₂) is switched 'ON' when a HIGH voltage is applied at the input. The p-channel transistor (Q₁) has the opposite behaviour, it is switched ON when a LOW voltage is applied at the input. It is indicated by placing bubble in the symbol.

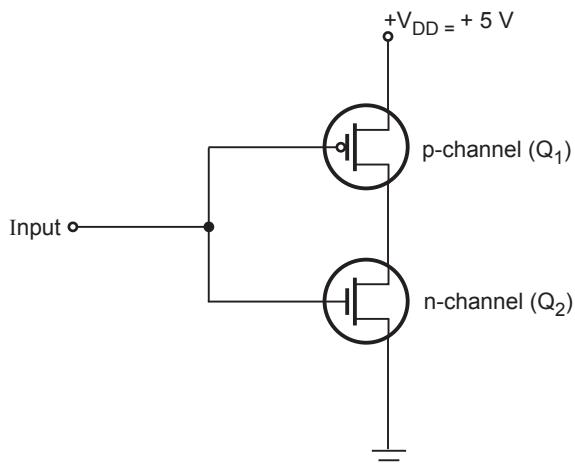


Fig. 10.4.3 The CMOS inverter

10.4.2 CMOS NAND Gate

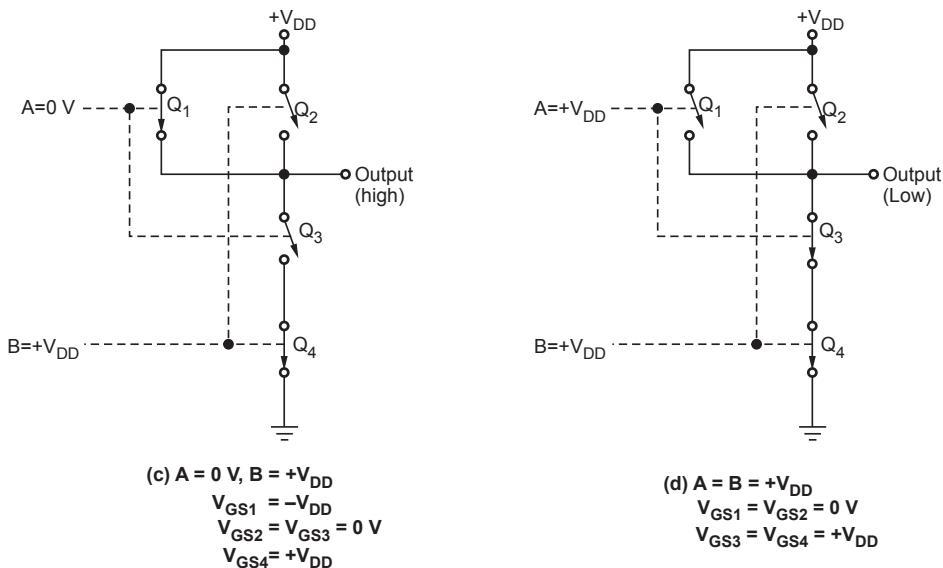
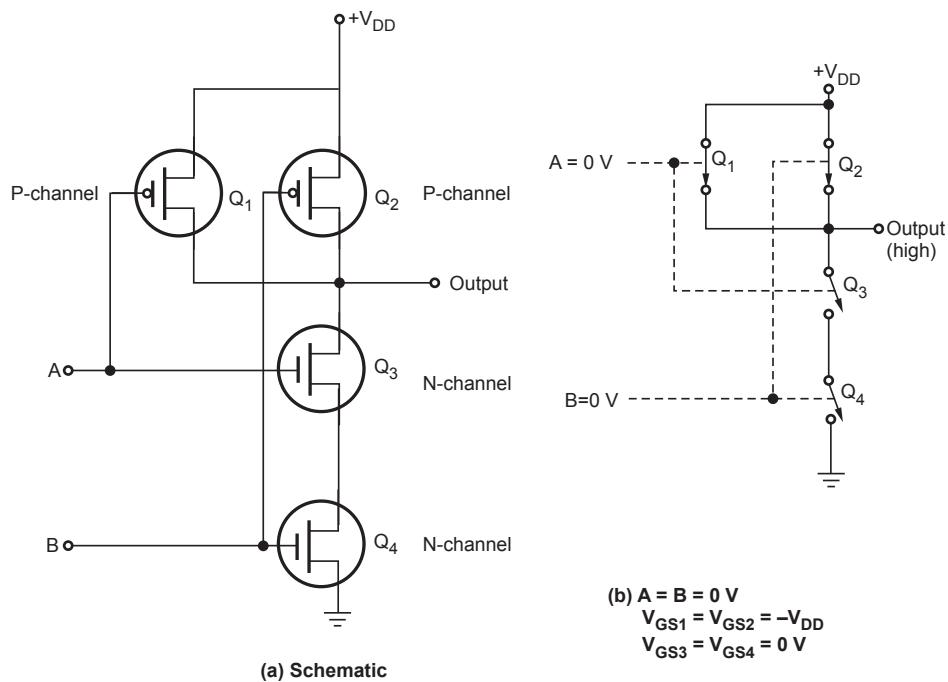


Fig. 10.4.4 CMOS NAND gate

P-channel MOSFET is ON when its gate voltage is negative with respect to its source whereas N-channel MOSFET is ON when its gate voltage is positive with respect to its source

- Fig. 10.4.4 shows CMOS 2-input NAND gate. It consists of two P-channel MOSFETs, Q_1 and Q_2 , connected in parallel and two N-channel MOSFETs, Q_3 and Q_4 connected in series.
- Fig. 10.4.4 (a) shows the equivalent switching circuit when both inputs are low. Here, the gates of both P-channel MOSFETs are negative with respect to their sources, since the sources are connected to $+V_{DD}$. Thus, Q_1 and Q_2 are both ON. Since the gate - to - source voltages of Q_3 and Q_4 (N-channel MOSFETs) are both 0 V, those MOSFETs are OFF. The output is therefore connected to $+V_{DD}$ (HIGH) through Q_1 and Q_2 and is disconnected from ground, as shown in the Fig. 10.4.4 (b).
- Fig. 10.4.4 (c) shows the equivalent switching circuit when $A = 0$ and $B = +V_{DD}$. In this case, Q_1 is on because $V_{GS1} = -V_{DD}$ and Q_4 is ON because $V_{GS4} = +V_{DD}$. MOSFETs Q_2 and Q_3 are off because their gate-to-source voltages are 0 V. Since Q_1 is ON and Q_3 is OFF, the output is connected to $+V_{DD}$ and it is disconnected from ground. When $A = +V_{DD}$ and $B = 0$ V, the situation is similar (not shown); the output is connected to $+V_{DD}$ through Q_2 and it is disconnected from ground because Q_4 is OFF.
- Finally, when both inputs are high ($A = B = +V_{DD}$), MOSFETs Q_1 and Q_2 are both OFF and Q_3 and Q_4 are both ON. Thus, the output is connected to the ground through Q_3 and Q_4 and it is disconnected from $+V_{DD}$.
- Table 10.4.2 summarizes the operation of 2-input CMOS NAND gate.

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Table 10.4.2 Truth table of NAND gate

- Fig. 10.4.5 shows the circuit diagram, function table and logic symbol of CMOS 3-input NAND gate.

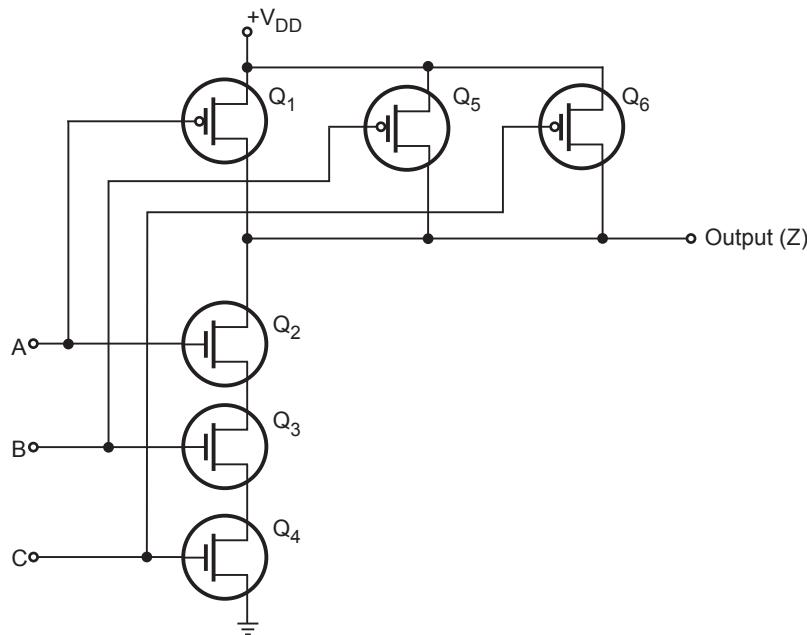


Fig. 10.4.5 (a) Circuit diagram for 3 input NAND gate

A	B	C	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Z
0	0	0	ON	OFF	OFF	OFF	ON	ON	1
0	0	1	ON	OFF	OFF	ON	ON	OFF	1
0	1	0	ON	OFF	ON	OFF	OFF	ON	1
0	1	1	ON	OFF	ON	ON	OFF	OFF	1
1	0	0	OFF	ON	OFF	OFF	ON	ON	1
1	0	1	OFF	ON	OFF	ON	ON	OFF	1
1	1	0	OFF	ON	ON	OFF	OFF	ON	1
1	1	1	OFF	ON	ON	ON	OFF	OFF	0

Fig. 10.4.5 (b) Function table

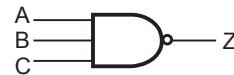
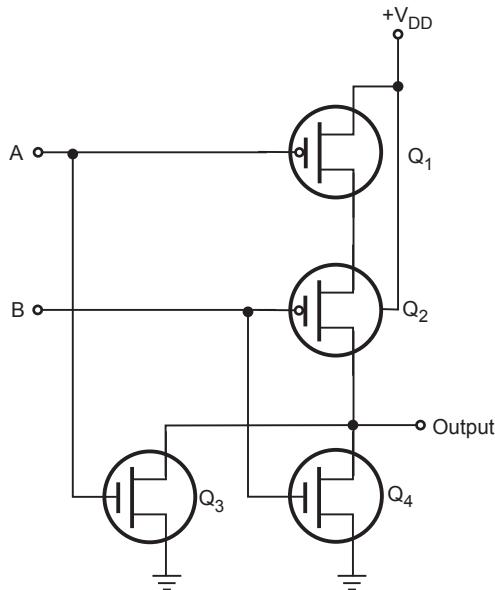


Fig. 10.4.5 (c) Logic symbol

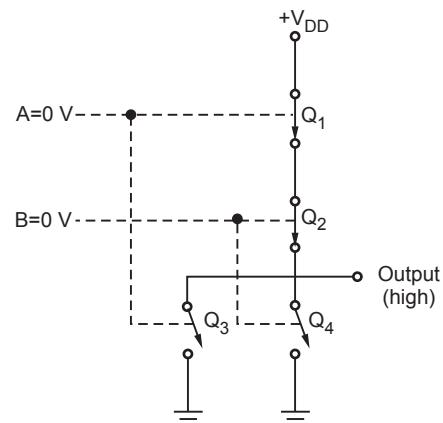
10.4.3 CMOS NOR Gate

- Fig. 10.4.6 (a) shows 2-input CMOS NOR gate. Here, P-channel MOSFETs Q₁ and Q₂ are connected in series and N-channel MOSFETs Q₃ and Q₄ are connected in parallel.

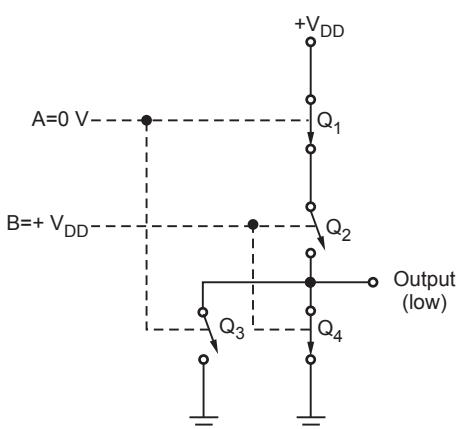
- Like NAND circuit, this circuit can be analyzed by realizing that a LOW at any input turns ON its corresponding P-channel MOSFET and turns OFF its corresponding N-channel MOSFET, and vice versa for a HIGH input. This is illustrated in Fig. 10.4.6. Table 10.4.3 summarizes the operation of 2-input NOR gate.



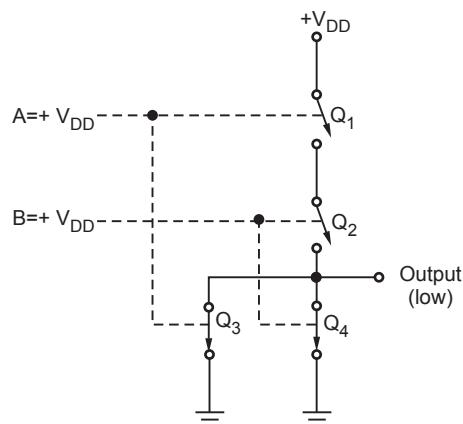
(a) Schematic



(b) $A = B = 0 \text{ V}$
 $V_{GS1} = V_{GS2} = -V_{DD}$
 $V_{GS3} = V_{GS4} = 0 \text{ V}$



(c) $A = 0 \text{ V}, B = +V_{DD}$
 $V_{GS1} = -V_{DD}$
 $V_{GS2} = V_{GS3} = 0 \text{ V}$
 $V_{GS4} = +V_{DD}$



(d) $A = B = +V_{DD}$
 $V_{GS1} = V_{GS2} = 0 \text{ V}$
 $V_{GS3} = V_{GS4} = +V_{DD}$

Fig. 10.4.6 CMOS NOR gate

A	B	Q ₁	Q ₂	Q ₃	Q ₄	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

Table 10.4.3 Truth table for NOR gate

10.4.4 CMOS Characteristics

- Operating Speed :** Slower than TTL series. Approximately 25 to 100 ns depending on the subfamily of CMOS. It also depends on the power supply voltage.
- Voltage Levels and Noise Margins :** The voltage levels for CMOS varies according to their subfamilies. These are listed in Table 10.4.4.

Parameter	CMOS series				
	4000 B	74 HC	74 HCT	74 AC	74 ACT
V _{IH(min)}	3.5	3.5	2.0	3.5	2.0
V _{IL(max)}	1.5	1.0	0.8	1.5	0.8
V _{OH(min)}	4.95	4.9	4.9	4.9	4.9
V _{OL(max)}	0.05	0.1	0.1	0.1	0.1
V _{NH}	1.45	1.4	2.9	1.4	2.9
V _{NL}	1.45	0.9	0.7	1.4	0.7

Table 10.4.4

- Noise margins in table are calculated as follows.
 $V_{NH} = V_{OH(min)} - V_{IH(min)}$
 $V_{NL} = V_{IL(max)} - V_{OL(max)}$
- Fan-out :** Typically, each CMOS load increases the driving circuit's propagation delay by 3 ns. Thus, fan-out for CMOS depends on the permissible maximum propagation delay.
- Typically, CMOS outputs are limited to a fan-out of 50.
- Power Dissipation (P_D) :** The power dissipation of a CMOS IC is very low as long as it is in a d.c. condition. Unfortunately, power dissipation of CMOS IC increases in proportion to the frequency at which the circuits are switching states. For example, a CMOS NAND gate that has P_D = 10 nW under d.c. conditions will have P_D = 0.1 mW at a frequency of 100 kHz and 1 mW at 1 MHz.

Propagation Delay : The propagation delay in CMOS is the sum of delay due to internal capacitance and due to load capacitance. The delay due to internal capacitance is called the **intrinsic propagation delay**. Typically, the propagation delay of CMOS is 70 ns.

Unused Inputs : CMOS inputs should never be left disconnected. All CMOS inputs have to be tied either to a fixed voltage level (0 V or V_{DD}) or to another input. An unused CMOS input is susceptible to noise and static charges.

10.4.5 | Wired Logic

Fig. 10.4.7 shows two CMOS inverters with their outputs connected together. This circuit does not work properly when B input is logic 0 and A input is logic 1. In this situation, Q_3 and Q_2 are ON and large current flows through Q_3 and Q_2 damaging these transistors. Therefore, wired-logic must not be used for CMOS logic circuits.

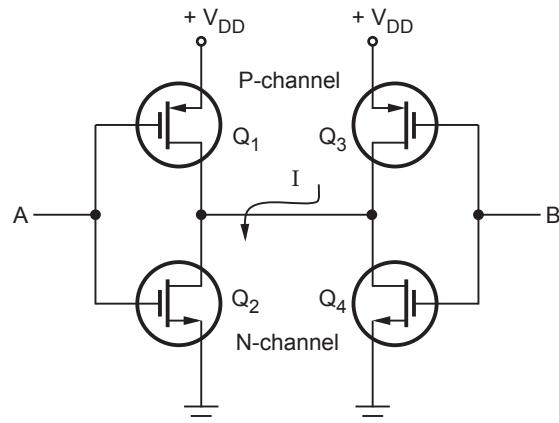


Fig. 10.4.7

10.4.6 | Open Drain Outputs

CMOS gates are available with open drain outputs, as shown in Fig. 10.4.8. In open drain outputs, PMOS transistor is replaced by a diode D_1 which provides protection from electrostatic discharge. Open drain gates can be used with external pull-up resistors to perform wired-AND operation, as discussed in TTL logic.

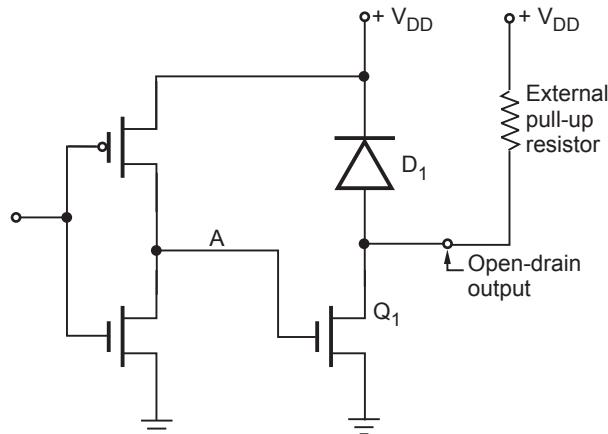


Fig. 10.4.8

10.4.7 | Advantages and Disadvantages of CMOS Family

Advantages

1. Consumes less power.
2. Can be operated at high voltages, resulting in improved noise immunity.
3. Fan-out is more.
4. Better noise margin.

Disadvantages

1. Susceptible to static charge.
2. Switching speed low.
3. Greater propagation delay.

Review Questions

1. Draw the structure of CMOS inverter gate. Explain its working.

SPPU : Dec.-07,17,19, Marks 3; May-12,17,18 Marks 4

2. Explain with neat diagram two input CMOS NAND gate.

SPPU : Dec.-12,14, May-14, Marks 8

3. Explain with neat diagram two input CMOS NOR gate.

SPPU : Dec.-10,18, May-13, Marks 4

4. Define the following parameters and give typical values of these parameters w.r.t. CMOS logic family : i) Speed of operation ii) Power dissipation

iii) Sourcing current iv) Fan out v) Sinking current.

SPPU : May-06, Marks 10

5. Explain, why wired-logic is not used for CMOS logic circuits.

SPPU : May-17, Marks 4

6. What do you mean by open drain output ? Where is it used ?

7. List differences between open drain and wired logic CMOS.

SPPU : May-12, Marks 4

8. State merits and demerits of CMOS logic family.

SPPU : Dec.-07, Marks 3

9. Explain with a neat diagram interfacing of TTL gate driving CMOS gates and vice-versa.

SPPU : May-05,07,13, Dec.-05, Marks 6; Dec.-08,11, Marks 8

10. Which parameters are significant while interfacing TTL and CMOS ? Draw and explain TTL driving CMOS gate.

SPPU : May-12, Marks 8

11. Compare TTL and CMOS logic families w.r.t. :

i) Power dissipation per gate ii) Propagation delay iii) Figure of merit iv) Fan-out.

SPPU : Dec.-04,05,06,12, May-08, Marks 6

12. List differences between CMOS and TTL.

SPPU : Dec.-11, May-15,16, Marks 4

13. Explain OR gate using CMOS logic.

SPPU : May-11, Marks 6

[Hints : Connect CMOS inverter at the output of CMOS NOR gate]

14. Why is it necessary to interface between TTL and CMOS ?

SPPU : May-13, Marks 2

10.5 Interfacing TTL and CMOS Families

SPPU : Dec.-18

- Interfacing means connecting the output(s) of one circuit or system to the input(s) of another circuit or system that may have different electrical characteristics. When two circuits have different electrical characteristics direct connection cannot be made. In such cases driver and load circuits are connected through interface

circuit. Its function is to take the driver output signal and condition it so that it is compatible with requirements of the load.

- One must consider following important points while interfacing two circuits or systems.
- The driver output must satisfy the voltage and current requirements of the load circuit.
- The driver and load circuit may require different power supplies. In such cases the output of both circuit must swing between its specified voltage ranges.

10.5.1 TTL Driving CMOS

- Here, TTL is a driver circuit and CMOS is a load circuit. The two circuits are from different families with different electrical characteristics. Therefore, we must check that the driving device can meet the current and voltage requirements of the load device.

	CMOS		TTL		
	4000B	74HC/HCT	74	74LS	74AS
I _{IH} (max)	1 μ A	1 μ A	40 μ A	20 μ A	200 μ A
I _{IL} (max)	1 μ A	1 μ A	1.6 mA	0.4 mA	2 mA
I _{OH} (max)	0.4 mA	4 mA	0.4 mA	0.4 mA	2 mA
I _{OL} (max)	0.4 mA	4 mA	16 mA	8 mA	20 mA

Table 10.5.1. Input/output currents for standard devices with supply voltage of 5 V

- Table 10.5.1 indicates that the input current values for CMOS are extremely low compared with the output current capabilities of any TTL series. Thus, TTL has no problem meeting the CMOS input current requirements.
- But when we compare the TTL output voltages with the CMOS input voltage requirements we find that :
- $V_{OH}(\min)$ for TTL $\ll V_{IH}(\min)$ for CMOS for these situations TTL output must be raised to an acceptable level for CMOS. This can be done by connecting pull-up resistor at the output of TTL, as shown in the Fig. 10.5.1. The pull-up resistor causes the TTL output to rise to approximately 5 V in the HIGH state, thereby providing an adequate CMOS input voltage level.

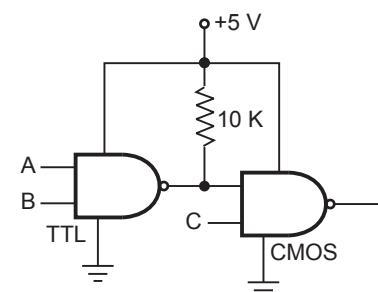


Fig. 10.5.1 TTL driving CMOS using external pull-up resistor

- **TTL Driving HIGH Voltage CMOS :** When output CMOS circuit is operating with V_{DD} greater than 5 V, the situation becomes more difficult. The outputs of many TTL devices cannot be operated at more than 5 V. In such cases some alternative arrangements are made. Two of them are discussed below :
 1. When the TTL output cannot be pulled up to V_{DD} , one can use open collector buffer as an interface between totem-pole TTL output and CMOS operating at $V_{DD} > 5$ V, as shown in the Fig. 10.5.2.

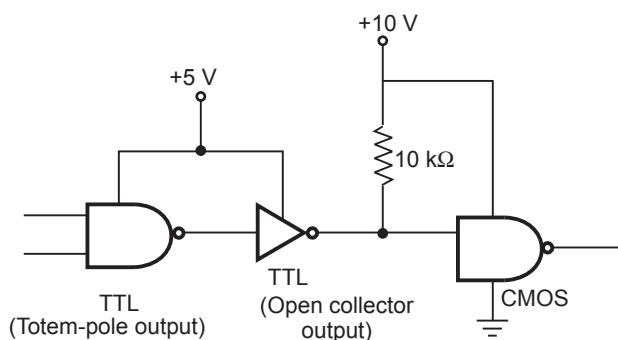


Fig. 10.5.2 Open collector buffer used as interface circuit

2. The second alternative is to use **level translator** circuit, such as the 40104. This is a CMOS chip that is designed to take a low-voltage input (e.g. from TTL) and translate it to high voltage output for CMOS. Fig. 10.5.3 shows the circuit arrangement.

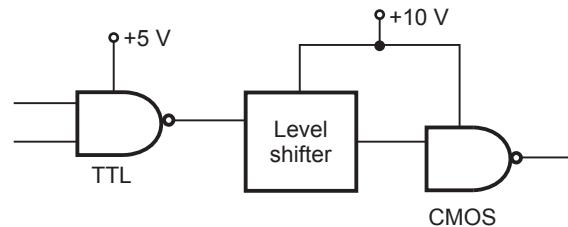


Fig. 10.5.3 Level shifter used as interface circuit

10.5.2 CMOS Driving TTL

- Before we consider the problem of interfacing CMOS outputs to TTL inputs, it will be helpful to review the CMOS output and TTL input characteristics for the two logic states.
- **CMOS Driving TTL in the HIGH state :** Above voltage parameters show that CMOS outputs can easily supply enough voltage (V_{OH}) to satisfy the TTL input requirement in the HIGH state (V_{IH}). The parameters also show that CMOS outputs can supply more than enough current (I_{OH}) to meet the TTL input current requirements (I_{IH}). Thus no special consideration is required for CMOS driving TTL in the HIGH state.
- **CMOS Driving TTL in the LOW state :** The parameters in the Table 10.5.2 show that CMOS output voltage (V_{OL}) satisfies TTL input requirement in the LOW state (V_{IL}). However, the current requirements in the LOW state are not satisfied. The TTL input has a relatively high input current in the LOW state (1.6 mA) and CMOS output current at LOW state (I_{OL}) is not sufficient to drive even one input

of the TTL. In such situations some type of interface circuit is needed between the CMOS and TTL devices. Fig. 10.5.4 shows the possible interface circuit.

- In Fig. 10.5.4 the CMOS 4050B, non-inverting buffer is used as an interfacing circuit. It has an output current rating of $I_{OL(\max)} = 3 \text{ mA}$ which satisfies the TTL input current requirement.
- **HIGH Voltage CMOS Driving TTL :** Some IC manufacturers have provided several 74LS TTL devices that can withstand input voltages as high as 15 V. These devices can be driven directly from CMOS outputs operating at $V_{DD} = 15 \text{ V}$. However, most TTL inputs cannot handle more than 7 V and so interface is necessary if they are to be driven from high-voltage CMOS. In such situations **voltage level translators** are used. They convert the high-voltage input to a 5 V output that can be connected to TTL.
- Fig. 10.5.5 shows how the 4050B can be used to perform this level translation between 15 V and 5 V.

For CMOS (4000B)	For TTL
$V_{OH(\min)} : 4.95 \text{ V}$	$V_{IH(\min)} : 2.0 \text{ V}$
$V_{OL(\max)} : 0.05 \text{ V}$	$V_{IL(\max)} : 0.8 \text{ V}$
$I_{OH(\max)} : 0.4 \text{ mA}$	$I_{IH(\max)} : 40 \mu\text{A}$
$I_{OL(\max)} : 0.4 \text{ mA}$	$I_{IL(\max)} : 1.6 \text{ mA}$

Table 10.5.2

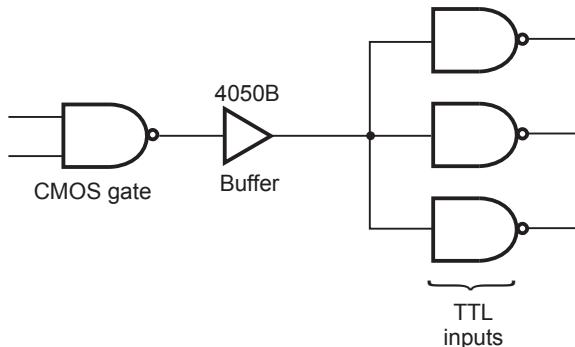


Fig. 10.5.4 CMOS driving TTL in LOW state using buffer

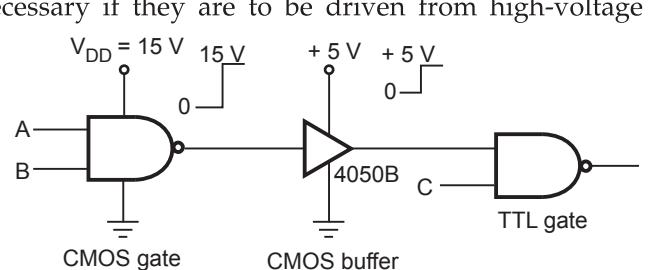


Fig. 10.5.5 Level translation using CMOS buffer

Review Questions

1. Explain the interfacing of TTL and CMOS :
 - i) CMOS driving TTL
 - ii) TTL driving CMOS

SPPU : Dec.-18, Marks 8

10.6 Comparison between TTL and CMOS Families

SPPU : May-15,16,19, Dec.-13,19

Sr. No.	Parameter	CMOS	TTL
1.	Device used	n-channel and p-channel MOSFET	Bipolar junction transistor
2.	$V_{IH(min)}$	3.5 V	2 V
3.	$V_{IL(max)}$	1.5 V	0.8 V
4.	$V_{OH(min)}$	4.95 V	2.7 V
5.	$V_{OL(max)}$	0.005 V	0.4 V
6.	High level noise margin	$V_{NH} = 1.45$ V	0.4 V
7.	Low level noise margin	$V_{NL} = 1.45$ V	0.4 V
8.	Noise immunity	Better than TTL	Less than CMOS
9.	Propagation delay	70 ns	10 ns
10.	Switching speed	Less than TTL	Faster than CMOS
11.	Power dissipation per gate	0.1 mW	10 mW
12.	Speed power product	0.7 pJ	100 pJ
13.	Fan-out	50	10
14.	Power supply voltage	3 - 15 V	Fixed 5 V
15.	Power dissipation	Increase with frequency	Increase with frequency
16.	Application	Portable instrument where battery supply is used.	Laboratory instruments.

Table 10.6.1 Comparison between TTL and CMOS families

Review Questions

1. Differentiate between standard TTL and CMOS logic circuit w.r.t.

i) Propagation delay ii) FANOUT iii) Figure of merit

SPPU : Dec.-13, Marks 6

2. List the differences between CMOS and TTL.

SPPU : May-15,16,19, Dec.-19, Marks 6



UNIT - VI

11

Introduction to Computer Architecture

Syllabus

Introduction to Ideal Microprocessor - Data Bus, Address Bus, Control Bus. Microprocessor based Systems - Basic Operation, Microprocessor operation, Block Diagram of Microprocessor.

Functional Units of Microprocessor - ALU using IC 74181, Basic Arithmetic operations using ALU IC 74181, 4-bit Multiplier circuit using ALU and shift registers. Memory Organization and Operations, digital circuit using decoder and registers for memory operations.

Contents

- 11.1 *Introduction to Ideal Microprocessor*
- 11.2 *Data Bus, Address Bus and Control Bus*
- 11.3 *Microprocessor Based Systems - Basic Operation*
- 11.4 *Microprocessor Operation*
- 11.5 *Block Diagram of Microprocessor with its Functional Units*
- 11.6 *ALU using IC 74181 - Basic Arithmetic operations*
- 11.7 *The 4-bit Multiplier Circuit using ALU and Shift Registers*
- 11.8 *Memory Organization*
- 11.9 *Memory Operation*

11.1 Introduction to Ideal Microprocessor

- A microprocessor is an important part of a computer architecture without which you will not be able to perform anything on your computer.
- It is a programmable device that takes in input, performs some arithmetic and logical operations over it and produces desired output.
- In simple words, a microprocessor is a digital device on a chip which can fetch instructions from memory, decode and execute them and give results.
- There is nothing like an ideal microprocessor. However, to understand the function of the microprocessor we have introduced this hypothetical device.
- Fig. 11.1.1 shows an ideal microprocessor with **n** inputs and **m** outputs.
- Input signals are applied from input devices. The input devices may include keyboard, mouse, sensors, switches, etc. These signals are in the binary form and are applied at the input terminals of the microprocessor.
- Microprocessor processes these input signals according to the sequence of operations stored in the memory. The sequence of operations referred to as program is in the binary form.
- The processed output in the binary form is fed to the output device. The output device may include indicators, displays, alarms, actuators etc.
- Microprocessor also called **Central Processing Unit (CPU)** consists of an ALU, control unit and register array.
 - The **ALU** performs arithmetic and logical operations on the data received from an input device or memory.
 - **Control unit** controls the instructions and flow of data within the computer.

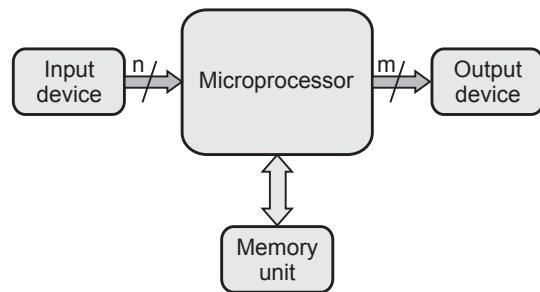


Fig. 11.1.1 An ideal microprocessor

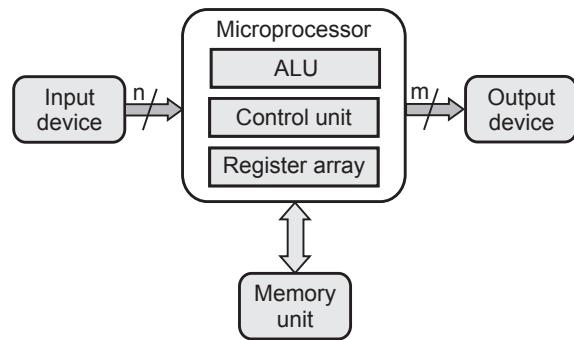


Fig. 11.1.2 Ideal microprocessor with ALU, Control unit and Register array

- **Register array** consists of registers identified by letters like B, C, D, E, H, L, and accumulator.
- Principal components of a CPU include the Arithmetic Logic Unit (ALU) that performs arithmetic and logic operations, processor registers that supply operands to the ALU and store the results of ALU operations, and a control unit that orchestrates the fetching (from memory) and execution of instructions by directing the coordinated operations of the ALU, registers and other components.

Review Questions

1. *What is microprocessor ?*
2. *Write a note on ideal microprocessor.*

11.2 Data Bus, Address Bus and Control Bus

- The central processing unit, memory unit and I/O unit are the hardware components/modules of microprocessor based systems. They work together with communicating each other and have paths for connecting the modules together. The collection of paths connecting the various modules is called the **interconnection structure**.
- The design of this interconnection structure will depend on the exchanges that must be made between modules.
- A group of wires, called **bus** is used to provide necessary signals for communication between modules.
- A bus that connects major microprocessor based system components/modules (CPU, memory, I/O) is called a **system bus**. The system bus is a set of conductors that connects the CPU, memory and I/O modules. Usually, the system bus is separated into three functional groups :
 - Address bus
 - Data bus
 - Control bus

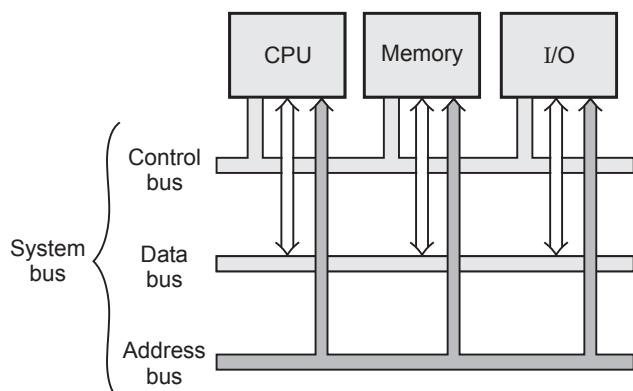


Fig. 11.2.1 Interconnection structure

11.2.1 Address Bus

- The memory which is external to the microprocessor consists of many millions of storage cells. Each cell is capable of storing 1-bit information having value 0 or 1. A single bit represents a very small amount of information. For this reason, the memory is organized so that a group of n -bits can be stored or retrieved in a single, basic operation. Each group of n bits is referred to as a **word** of information, and n is called the **word length**.

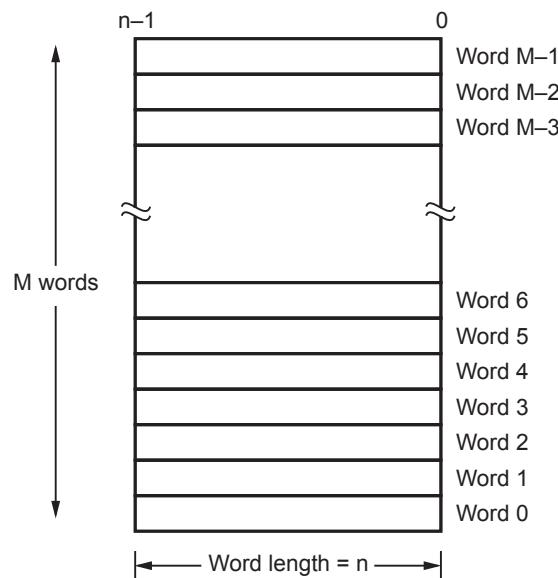


Fig. 11.2.2 Memory organization

- Fig. 11.2.2 shows the computer memory in the form of collection of words. In most of the memories word length is 8-bit, i.e., **byte**. Looking at the figure, we can say that memory is a array of M number of n -bit words.
- Each word of memory has an unique address. The address is used to identify a particular word in the memory or **memory location**. Thus the number and address lines provided by the processor decides the addressing capability of the microprocessor.
- For example, if the microprocessor has 16 address lines it can address up to 2^{16} (65536) memory locations. Table 2.3.1 shows the relation between memory capacity and the address lines.

Memory capacity	Address lines required
1 K = 1024 memory locations	10
2 K = 2048 memory locations	11
4K = 4096 memory locations	12
8K = 8192 memory locations	13
16K = 16384 memory locations	14
32K = 32768 memory locations	15
64K = 65536 memory locations	16

Table 11.2.1

- Usually the address bus of microprocessor consists of 16, 20, 24 or more parallel signal lines. On these lines the CPU sends out the address of the memory location or I/O port that is to be written to or read from.
- Here, the communication is one way, the address is send from CPU to memory and I/O port and hence these lines are **unidirectional**.

11.2.2 Data Bus

- The data bus consists of 8, 16, 32 or more parallel signal lines. These lines are used to send data to memory and output ports, and to receive data from memory and input port. Therefore, data bus lines are **bi-directional**.
- This means that CPU can read data on these lines from memory or from a port, as well as send data out on these lines to a memory location or to a port.
- The data bus is connected in parallel to all peripherals. The communication between peripheral and CPU is activated by giving output enable pulse to the peripheral. Outputs of peripherals are floated when they are not in use.
- The data transfer between the memory and microprocessor takes place through the use of two internal registers, usually called **MAR** (Memory Address Register) or simply **AR** (Address Register) and **MDR** (Memory Data Register) or simply **DR** (Data Register). This is illustrated in Fig. 11.2.3. If MAR is k -bit long and MDR is n bit long, it is possible to access up to 2^k memory locations, and during one memory cycle it is possible to transfer n -bit data.

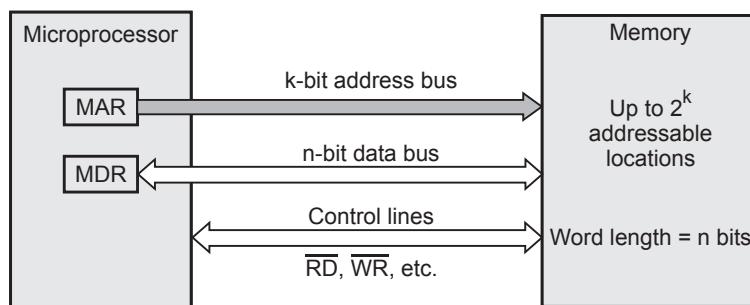


Fig. 11.2.3 Connection between memory and microprocessor

11.2.3 Control Bus

- The control lines from the microprocessor decide the memory operation. In case of read operation (\overline{RD}) signal is activated. It is used to enable the active low output enable signal of the memory. In case of write operation (\overline{WR}) signal is activated to indicate the write operation.

- The control lines regulate the activity on the bus. The CPU sends signals on the control bus to enable the outputs of addressed memory devices or I/O devices.
- At a time, microprocessor can communicate either with memory or I/O device. To choose between them microprocessor provides control signal called IO/M . When this signal is 1, the address meant for I/O devices. On the other hand, when this signal is 0, the address is for memory.

11.2.4 Multiplexed Address and Data Bus

- The main reason of multiplexing address and data bus is to reduce the number of pins for address and data and dedicate those pins for other several functions of microprocessor.
- These multiplexed set of lines used to carry the address as well as data at different time frames.
- In such cases, the external hardware called **latch** is used to de-multiplex address and data lines. This is illustrated in Fig. 11.2.4
- The input is transferred to the output only when clock is high. This clock signal is driven by **Address Latch Enable** (ALE) signal from microprocessor.
- During the first phase of machine cycle, address is put on the multiplexed address and data bus and the ALE signal is activated. This latches the address sent by microprocessor at the output of latch.
- In the remaining part of the machine cycle, ALE signal is disabled so output of the latch remains unchanged. During this time multiplexed address and data bus is used as a data bus.

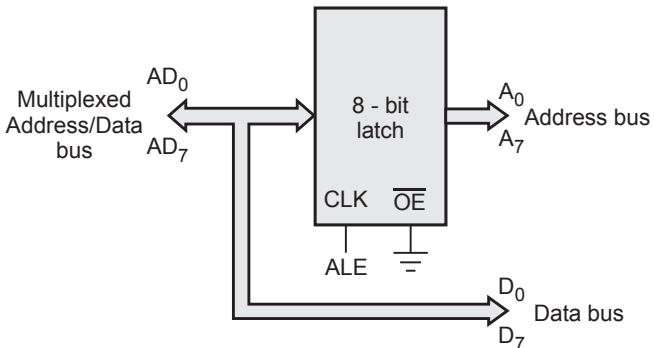


Fig. 11.2.4 De-multiplexing of address and data bus

11.2.5 Address Bus and Data Bus Drivers

- Bus drivers, buffers are used to increase the driving capacity of the microprocessor buses.

- **Unidirectional buffers** : As we know, the address bus is unidirectional, unidirectional buffer, is used to buffer address bus. Fig. 11.2.5 shows the logic diagram of 8-bit unidirectional buffer. It consists of eight non-inverting buffers with tri-state outputs. The enabling and disabling of these groups are controlled by (**Enable**) Signal.

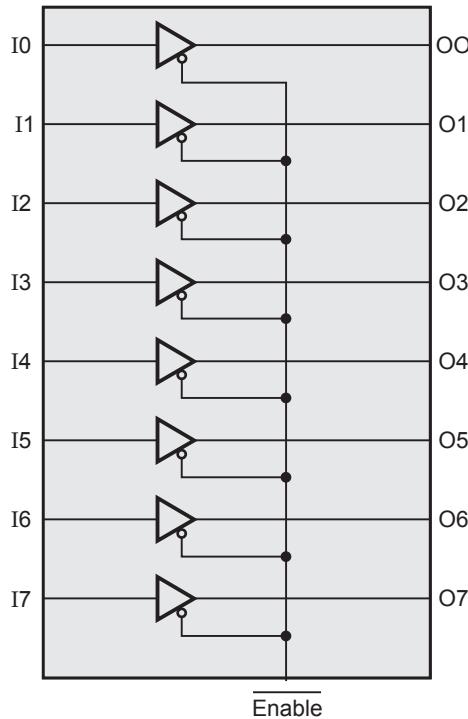


Fig. 11.2.5 8-bit unidirectional buffer

- To increase the driving capacity of data bus, bi-directional buffer is used. Fig. 11.2.6 shows the logic diagram of the 8-bit bi-directional buffer, also called an **octal bus transceivers**.
- It consists of sixteen non-inverting buffers, eight for each direction, with tri-state output. The direction of data flow is controlled by the pin DIR. When DIR is high, data flows from the A bus to the B bus; when it is low, data flows from B to A.
- For microprocessor, the number of address lines and data lines are in multiples of 8 (8, 16, 24, ...). In such case multiple number of buffer ICs are used to drive address bus and data bus.

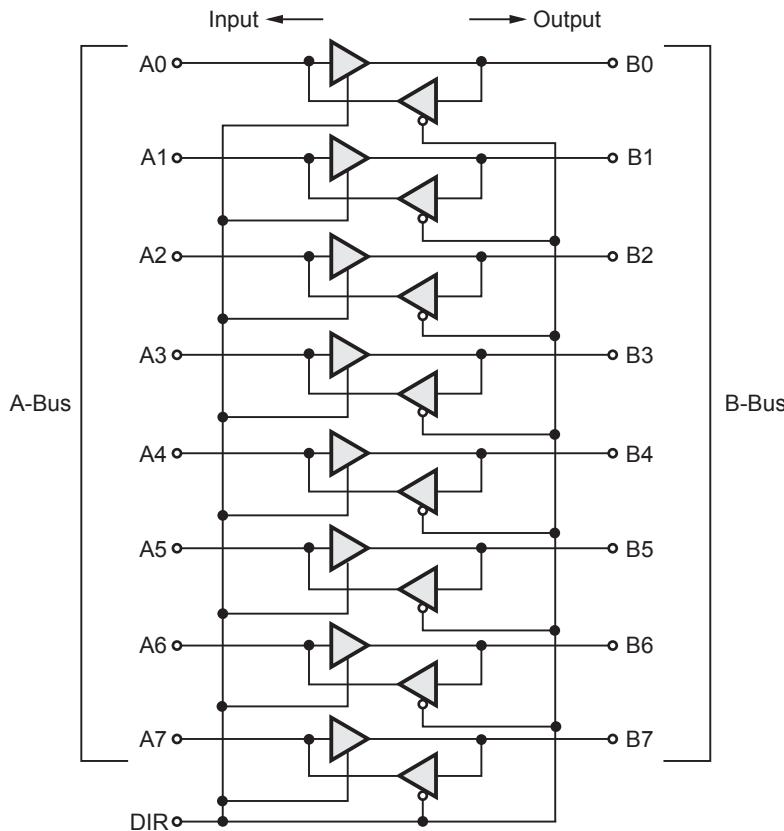


Fig. 11.2.6 8-bit bi-directional buffer

11.2.6 Sharing of Address, Data and Control Bus with DMA

- To increase the speed of data transfer between memory and I/O, the **hardware controlled I/O** is used. It is commonly referred to as Direct Memory Access (DMA). The hardware which controls this data transfer is commonly known as **DMA controller**.
- The DMA controller sends a **HOLD** signal to the microprocessor to initiate data transfer. In response to HOLD signal, microprocessor sends **HLDA** signal as an acknowledgement and releases its data, address and control buses to the DMA controller.
- Then the data transfer is controlled at high speed by the DMA controller without the intervention of the microprocessor. After data transfer, DMA controller sends low on the HOLD pin, which gives the control of data, address and control buses back to the microprocessor. This type of data transfer is used for large data transfers.

11.2.7 Control Signals to Provide Facility of Interrupt Driven I/O

- The interrupt driven I/O approach, provides the facility of interrupting the execution of the normal sequence of the program. To provide this facility, there is control input called **INTR** (Interrupt Request). When a peripheral wants to interrupt the microprocessor for some reason, it sends logic 1 on INTR control line. In response, microprocessor completes execution of the current instruction and sends out logic 0 on the **(INTA)** (Interrupt Acknowledge), output control line, acknowledging the request of the interrupting device. It then services the interrupt by transferring the program control to an interrupt service routine. This interrupt service routine performs the desire task and after completion of the task, it returns control to the main program at the point it was interrupted.

Review Questions

1. *What is bus ?*
2. *What do you mean by system bus ?*
3. *Draw the interconnection structure to connect memory and I/O devices with microprocessor.*
4. *Draw and explain the connections between memory and microprocessor.*
5. *What is the role of address bus ?*
6. *Write a short note on address bus.*
7. *Why is data bus bidirectional ?*
8. *What is the role of data bus ?*
9. *What is multiplexed address and data bus ?*
10. *How is address and data bus de-multiplexed ?*
11. *How are address and data lines de-multiplexed ?*
12. *Write a short note on address and data bus drivers.*
13. *What is DMA ?*
14. *What are the functions of HOLD and HLDA signals ?*
15. *State the control lines required to support interrupt driven I/O.*
16. *What is an interrupt driven I/O ?*

11.3 Microprocessor Based Systems - Basic Operation

- A microprocessor based system has two principle components : **hardware** and **software**. The hardware is the circuitry and physical devices, and the software is the collection of programs which controls and operates the hardware to get the desired output.
- The electronic components used in the microprocessor based system, as a whole, are referred to as **hardware**.

- The block diagram of a simple microprocessor based will give general layout of the hardware. Fig. 11.3.1 shows the block diagram of a simple microprocessor based. The major components of microprocessor based are Central Processing Unit (CPU), memory and input and output circuitry or I/O ports.
- These components of microprocessor based are connected using three sets of parallel lines called buses. The three buses are **address bus**, **data bus** and **control bus**.

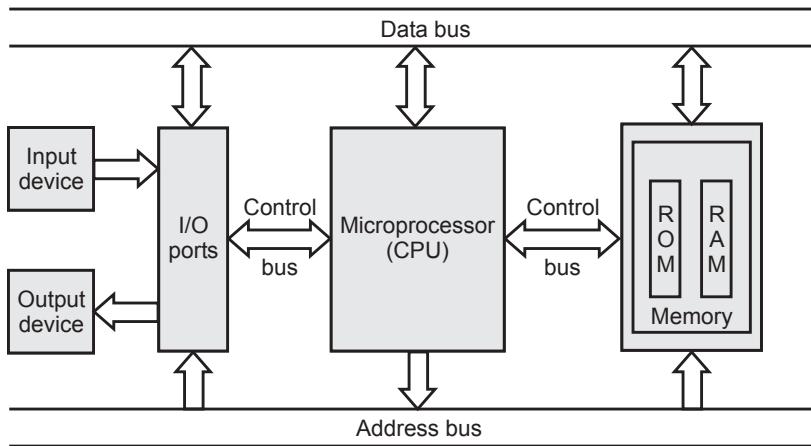


Fig. 11.3.1 Block diagram of microprocessor based system

- **Central Processing Unit (CPU)** : Central Processing Unit is a microprocessor and is often referred as Microprocessor Unit (MPU). Its purpose is to fetch binary coded instructions from memory, decode the fetched instructions and generate the control signals required to execute the instructions. The CPU contains an Arithmetic Logic Unit (ALU), which can perform add, subtract, OR, AND, invert and exclusive - OR operations on binary words. The CPU also contains a program counter register which is used to hold the address of the next instruction or data to be fetched from memory, general - purpose registers which are used for temporary storage of binary data, and circuitry which generates the control signals.
- **Input / Output Module** : Input/Output system consists of a variety of devices for communicating with the external world. It consists of input devices, output devices and control circuitry. Each port has a unique address. Microprocessor can read data from input device like keyboard, analog to digital converter, card readers and paper tape readers through the input port. Output ports are used to send data to output devices such as printer, video display, digital to analog converter, plotter and card punches. Physically the port is often just a set of parallel D flip flops which usually act as a buffer for input and as a latch for output.

- **Memory Module :** The memory module is used to store the binary codes for the sequences of instructions we want the microprocessor to carry out. This sequence of instructions or program is stored as binary numbers in successive memory locations. It is also used to store the binary coded data.
- Typically, memory is implemented with both, ROM (Read Only Memory) and RAM ICs. RAM and ROM memories consist of an array of registers, in which each register has unique address.
- **ROM :** It is a read only memory. We can't write data in this memory. It is a non volatile memory i.e. it can hold data even if power is turned off. Generally, ROM is used to store the binary codes for the sequence of instructions you want the microprocessor to carry out and data such as lookup tables. This is because this type of information does not change.
- **RAM :** Unlike ROM, we can read from or write into the RAM, so it is often called read/write memory. The numerical and character data that are to be processed by the microprocessor change frequently. These data must be stored in type of memory from which they can be read by the microprocessor, modified through processing, and written back for storage. For this reason, they are stored in RAM instead of ROM.
- Program is a series of instructions that can be executed in order to perform a **specified** task.
- Let us consider a simple task to understand the functioning of the components of a microprocessor. The task involves following three operations :
 1. Read a value from a keyboard connected to the port at address 01H.
 2. Add 30H to the value read from keyboard.
 3. Send the result to a display connected to the port at address 02H.

Table 11.3.1 shows a program to accomplish the given task. It consists of three instructions.

Memory Address		Contents (binary)										Contents (Hex)	Operation	
0	0	0	0	H	1	1	0	1	1	0	1	1	DB	Input from port 01H
0	0	0	1	H	0	0	0	0	0	0	0	1	01	
0	0	0	2	H	1	1	0	0	0	1	1	0	C6	Add immediate data 30h
0	0	0	3	H	0	0	1	1	0	0	0	0	30H	
0	0	0	4	H	1	1	0	1	0	0	1	1	D3	Output to port 02H
0	0	0	5	H	0	0	0	0	0	0	1	0	02	

Table 11.3.1 Memory addresses and memory contents for a three instruction program

- We assume that the microprocessor fetches instructions and data from memory 1 byte at a time.
- An **opcode** is the first byte of an instruction in machine language which tells the hardware what operation needs to be performed with this instruction. Every microprocessor has its own set of opcodes (operational codes) defined in its architecture.
- We also assume that the instructions are in sequential memory locations starting at address 0000H as shown in Table 11.3.1.
- Fig. 11.3.2 shows the hardware components and Table 11.3.2 shows the sequence of actions that the microprocessor will perform to execute these three instructions.

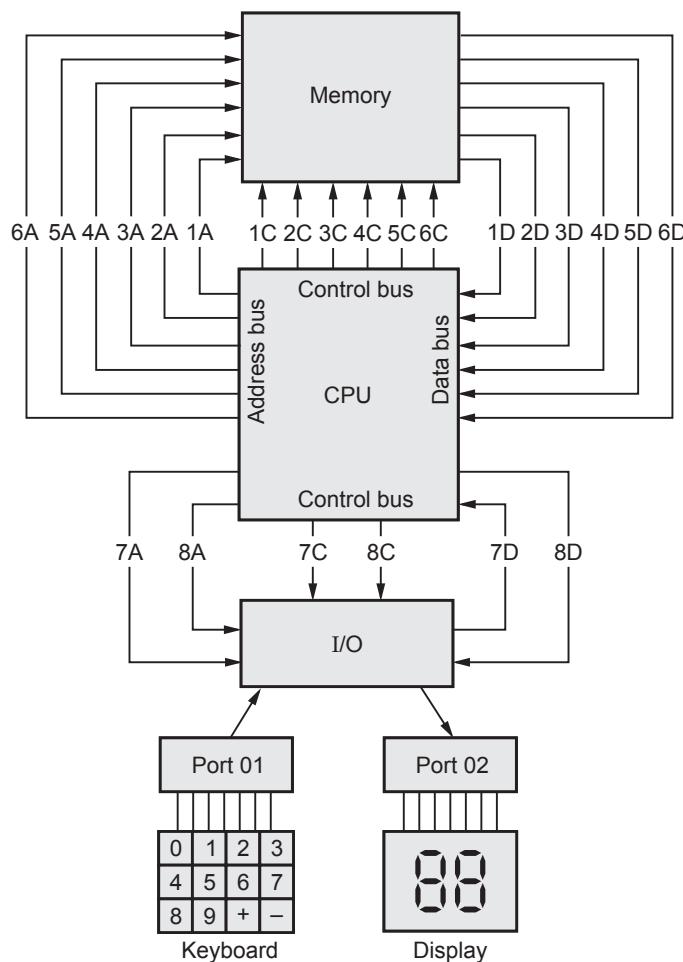


Fig. 11.3.2 Hardware components for execution of three-instruction program

Instruction		Action
1	1A	Microprocessor sends the address of the first instruction to the memory. Address Bus : 0000H
	1C	Microprocessor sends memory read control signal to enable memory.
	1D	Microprocessor reads first instruction byte (DBH) sent from memory on data bus and decodes it. By decoding it determines that the code read represents the INPUT instruction and it needs more information to carry out the instruction.
	2A	Microprocessor sends the address of the next memory location to get the remaining instruction. Address Bus : 0001H
	2C	Microprocessor sends memory read control signal to enable memory.
	2D	Microprocessor reads port address byte (01H) sent from memory on data bus
	7A	To execute instruction Microprocessor sends the port address (01H) on the address bus.
	7C	Microprocessor sends I/O read control signal to enable the addressed input port.
	7D	Input device puts a byte data on the data bus. Microprocessor reads the data byte from the data bus and stores it in the internal register. This completes execution of the first instruction.
2	3A	Microprocessor sends the address of the next (second) instruction (0002H) on the address bus.
	3C	Microprocessor sends memory read control signal to enable memory.
	3D	Microprocessor reads instruction byte (C6H) sent from memory on data bus and decodes it. By decoding it determines that it supposed to add some number to the number stored in the internal register. It also determines that it must get next byte of instruction from memory.
	4A	Microprocessor sends next sequential address (0003H) on the address bus.
	4C	Microprocessor sends memory read control signal to enable memory.
	4D	Microprocessor reads the data byte (30H) from the data bus and adds it to the contents of internal register. This completes execution of the second instruction.

3.	5A	Microprocessor sends the address of the next (third) instruction (00004H) on the address bus.
	5C	Microprocessor sends memory read control signal to enable memory.
	5D	Microprocessor reads instruction byte (D3H) sent from memory on data bus and decodes it. By decoding it determines that it is supposed to perform output operation. It also determines that it must get address of the output port from memory.
	6A	Microprocessor sends next sequential address (0005H) on the address bus.
	6C	Microprocessor sends memory read control signal to enable memory.
	6D	Microprocessor reads output port address byte (02H) sent from memory on data bus.
	8A	Microprocessor sends the output port address (02H) on the address bus.
	8D	Microprocessor sends the data byte from the internal register on the data bus.
	8C	Microprocessor sends I/O write signal on the control bus to enable the addressed output port so that the data from the data bus can pass through it to LED displays. This completes the execution of the third instruction.

Table 11.3.2 Sequence of actions during execution of three instruction program

Review Questions

1. Draw and explain the block diagram of microprocessor based system.
2. Write a note on memory module of a microprocessor based system.
3. Explain the execution of three-instruction program.

11.4 Microprocessor Operation

- The primary function of a microprocessor is to execute sequence of instructions stored in a memory, which is external to the microprocessor. The sequence of operations involved in processing an instruction constitutes an instruction cycle.
- From the above discussion it is cleared that, the complete instruction cycle involves three operations : **fetch, decode and execution.**
(See Fig. 11.4.1 on next page)
- **Fetch :**
 - Microprocessor sends the address of the instruction to the memory.
 - Microprocessor also sends memory read control signal to enable memory.
 - Microprocessor reads instruction byte (opcode) sent from memory on data bus and places it in the Instruction Register (IR) in the microprocessor.

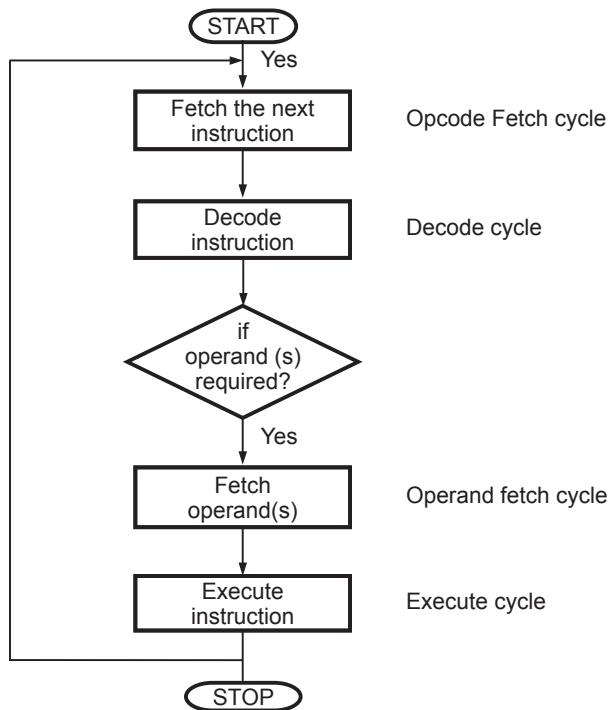


Fig. 11.4.1 Basic instruction cycle

- When the fetch cycle is used to read instruction it is known as **instruction fetch cycle**. On the other hand, when the fetch cycle is used to read operand it is known as **operand fetch cycle**.
- **Decode :**
 - Microprocessor decodes the opcode of the instruction stored in the instruction register to determine which operation is to be performed.
- **Execution :**
 - Microprocessor performs the specified operation. This often involves performing an arithmetic or logical operation and storing the result in the destination location.

Review Questions

1. Write a note on microprocessor operations
2. Explain the phases in the instruction cycle.

11.5 Block Diagram of Microprocessor with its Functional Units

- Fig. 11.5.1 shows the simplified block diagram of microprocessor. As shown in Fig. 11.5.1 includes three major logic devices
 - ALU
 - Several registers
 - Control unit
- The internal data bus is used to transmit data between these logic devices.

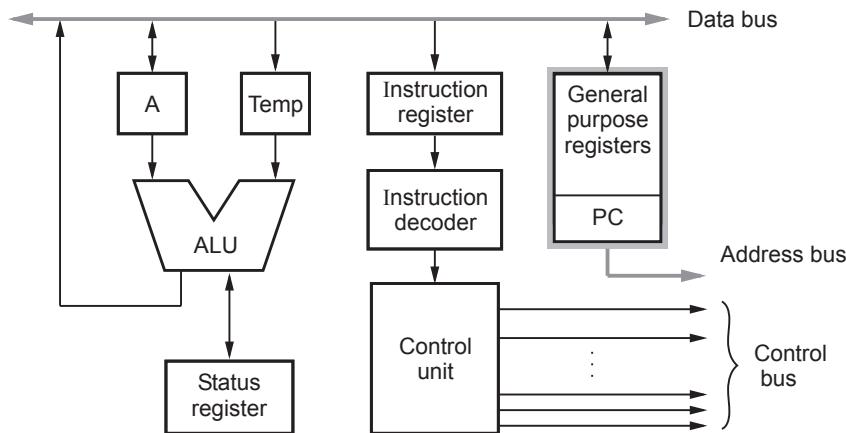


Fig. 11.5.1 Simplified block diagram of a microprocessor

11.5.1 Arithmetic and Logic Unit (ALU)

- One of the microprocessor's major logic devices is the arithmetic logic unit (ALU). It contains the microprocessor's data processing logic. It has two inputs and an output.
- The internal data bus of microprocessor is connected to the two inputs of ALU through the temporary register and the accumulator.
- The ALU's single output is connected to the internal data bus so that can be sent to any device connected to the bus. In most of the microprocessors **register A** gives data for the ALU and after performing the operation, the resulting data word is sent to the register A and stored there. This special register, where the result is accumulated is commonly known as **accumulator**.
- The ALU works on either one or two data words, depending on the kind of operation. The ALU uses input ports as necessary. For example, addition operation uses both ALU inputs while complementing data operation uses only one input.

To complement the data word, all the bits of the word's that are logic 1 are set to logic 0, and all the bits of the word at logic 0 are set to logic 1.

Table 11.5.1 lists some of the functions performed by the ALU in most of the microprocessors.

Add	Subtract	AND	OR	Exclusive OR
Complement	Shift right	Shift left	Increment	Decrement

Table 11.5.1 Functions performed by ALU

11.5.2 Registers

- Registers are a prominent part of the block diagram and the programming model of any microprocessor. The basic registers found in most of the microprocessors are :
 - Accumulator
 - Program Counter (PC)
 - Status Register (Flag Register)
 - General purpose registers
 - Memory address register
 - Instruction register and
 - Temporary data registers.
 - Stack Pointer (SP)

Accumulator

- The accumulator is the major working register of microprocessor. Most of the time it is used to hold the data for manipulation.
- Whenever the operation processes two words, whether arithmetically or logically, the accumulator contains one of the words. The other word may be present in another register or in a memory location.
- Most of the times the result of an arithmetic or logical operation is placed in the accumulator. In such cases, after execution of instruction original contents of accumulator are lost because they are overwritten.
- The accumulator is also used for data transfer between an I/O port and a memory location, or between one memory location and another.

Program Counter (PC)

- The Program Counter is one of the most important registers in the microprocessor. As mentioned earlier, a program is a series of instructions stored in the memory. These instructions tell the microprocessor exactly how to solve a problem. It is

important that these instructions must be executed in a proper order to get the correct result. This sequence of instruction execution is monitored by the program counter. It keeps track of which instruction is being used and what the next instruction will be.

- The program counter gives the address of memory location from where the next instruction is to be fetched. Due to this the length of the program counter decides the maximum program length in bytes. For example, microprocessor that has 16 bit program counter, can address bytes (64 K) of memory.
- Before the microprocessor can start executing a program, the program counter has to be loaded with valid memory address. This memory location must contain the opcode of first instruction in the program. In most of the microprocessors this location is fixed. For example, memory address (0000H) for 16 bit program counter. The fixed address is loaded into the program counter by resetting the microprocessor.

Status Register

- The status register is used to store the results of certain condition when certain operations are performed during execution of the program.
- The status register is also referred to as **flag register**. ALU operations and certain register operations may set or reset one or more bits in the status register.
- Status bits lead to a new set of microprocessor instructions. These instructions permit the execution of a program to change flow on the basis of the condition of bits in the status register. So the condition bits in the status register can be used to take logical decisions within the program. Some of the common status register bits are :
- **Carry/Borrow** : The carry bit is set when the summation of two 8 bit numbers is greater than 1111 1111 (FFH). A borrow is generated when a large number is subtracted from a smaller number.
- **Zero** : The zero bit is set when the contents of register are zero after any operation. This happens not only when you decrement the register, but also when any arithmetic or logical operation causes the contents of register to be zero.
- **Negative or sign** : In 2's complement arithmetic, the most significant bit is a sign bit. If this bit is logic 1, the number is negative number, otherwise a positive number. The negative bit or sign bit is set when any arithmetic or logical operation gives a negative result.
- **Auxiliary Carry** : The auxiliary carry bit of status register is set when an addition in the first 4 bits causes a carry into the fifth bit. This is often referred as half carry or intermediate carry. This is used in the BCD arithmetic.

- **Overflow Flag** : In 2's complement arithmetic, most significant bit is used to represent sign and remaining bits are used to represent magnitude of a number. This flag is set if the result of a signed operation is too large to fit in the number of bits available (7-bits for 8-bit number) to represent it.
- For example, if you add the 8-bit signed number 01110110 (+118 decimal) and the 8-bit signed number 00110110 (+ 54 decimal). The result will be 10101100 (+ 172 decimal), which is the correct binary result, but in this case it is too large to fit in the 7-bits allowed for the magnitude in an 8-bit signed number. The overflow flag will be set after this operation to indicate that the result of the addition has overflowed into the sign bit.
- **Parity** : When the result of an operation leave the indicated register with an even number of 1s, parity bit is set.

General Purpose Registers

- In addition to the basic registers, most microprocessors have other registers called **general purpose registers**.
- The general purpose registers are used as simple storage area, mainly these are used to store intermediate results of the operation. Getting the operand from the general purpose registers is more faster than from memory so it is better to have sufficient number of general purpose register in the microprocessor.
- The microprocessor used in this chapter has six general purpose registers (Refer Fig. 11.5.1) called the B, C, D, E, H, and L registers. These registers individually can operate as 8 bit registers. Together, the BC, DE, and HL registers can operate as 16 bit register pairs.

Memory Address Register

- The memory address register gives the address of memory location that the microprocessor wants to use. That is, memory address register holds 16-bit binary number. The output of the memory address register drives the 16-bit address bus. This output is used to select a memory location.

Instruction Register (IR)

- The instruction register holds the operation code (opcode) of the instruction the microprocessor is currently executing. The instruction register is loaded during the opcode fetch cycle. The contents of the instruction register are used to drive the part of the control logic known as the **instruction decoder**.

Temporary Data Register

- The need for the temporary data registers arises because the ALU has no storage of its own. The ALU has two inputs. One input is supplied by accumulator and

other from temporary data register. The programmer cannot access this temporary data register and, therefore it is not a part of programming model.

Stack Pointer

- The **stack** is a LIFO (last in, first out) data structure implemented in the RAM area and is used to store addresses and data. The Stack Pointer register holds the address of the top location of the stack.

11.5.3 Instruction Decoder

- It decodes the opcode from instruction register and generates the decoded output. This decoded output is used by control logic to generate control signals.

11.5.4 Control Logic

- The control logic is a important block in the microprocessor. The control logic is responsible for working of all other parts of the microprocessor together.
- It maintains the synchronization in operation of different parts in the microprocessor. The synchronization is achieved with the help of one of the control logic's major external inputs, microprocessor's clock. The clock is a signal which is the basis of all the timings inside the microprocessor.
- The control logic receives the signal from instruction decoder and generates the control signals necessary to execute the instruction.
- The control logic does a few other special functions. It looks after the microprocessor power-up sequence. It also processes interrupts.

11.5.5 Internal Data Bus

- The internal data bus connects the different parts of microprocessor together and it enables the communication between these parts. The data transfer through this internal data bus is controlled by control logic.
- Microprocessor's internal data bus usually connected to an external data bus. Due to this microprocessor can communicate with external memory or I/O devices. Usually the internal data bus is connected to the external data bus by logic called a **bi-directional bus** (transceiver).

11.5.6 Subroutine, Stack and Stack Pointer

- As said earlier, the instructions must be executed in a proper order to get the correct result. This does not mean that every instruction must follow the last instruction in the memory. But it must follow the logical sequence of the instructions.

- In some situations, it is better to execute part of a program that is not in sequence (don't confuse with logical sequence) with the main program.
- For example, there may be a part of a program that must be repeated many times during the execution of the entire program. Rather than writing repeated part of the program again and again, the programmer can write that part only once. This part is written separately. The part of the program which is written separately is called **subroutine**.
- Fig. 11.5.2 shows how the main and subroutine programs are executed.
- The program counter does the major role in subroutine execution as it can be loaded with required memory address.
- With the help of instruction it is possible to load any memory address in the program counter. When subroutine is to be executed, the program counter is loaded with the memory address of the first instruction in the subroutine.
- After execution of the subroutine, the program counter is loaded with the memory address of the next instruction from where the program control was transferred to the subroutine program.
- During subroutine operation, before transferring the program control to the subroutine the return address is kept in a special memory area called the **stack**.
- After the execution of subroutine the return address is popped off from the stack and loaded into the program counter.
- The memory address of the stack area is given by a special register called the **stack pointer**.
- Like the Program Counter, the Stack Pointer automatically points to the next available location in the memory. In most microprocessors, the stack pointer decrements (points to the next lower memory address) when data is pushed on the stack. This allows the programmer to build the stack down in memory as shown in the Fig. 11.5.3.

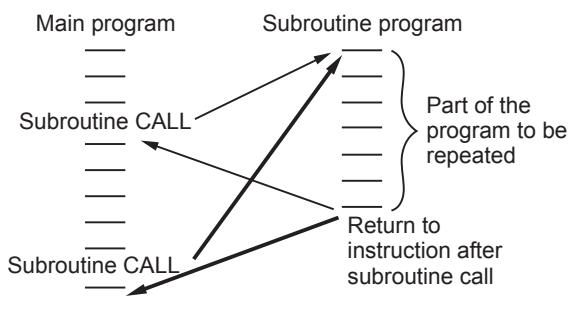


Fig. 11.5.2 Execution of subroutine programs

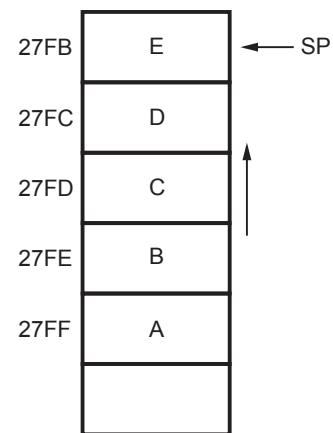


Fig. 11.5.3 Stack operation

- It is important to note that as you go on storing (pushing) data on the stack, the stack pointer always points the last data placed on the stack and when you try to remove (pop) data you always get the last data placed on the stack. This kind of stack operation is called **LIFO (Last In First Out) operation**.

Review Questions

- Draw and explain the block diagram of microprocessor.
- Explain various functions of ALU.
- What is accumulator ?
- What is program counter ?
- What do you mean by general purpose registers ?
- List various flags in the status register.
- What is status register ? Explain its use
- State the functions of instruction register and instruction decoder.
- What is subroutine ?
- Explain the execution of subroutine program.
- What is stack and stack pointer ?
- Explain the operation of stack.

11.6 ALU using IC 74181 - Basic Arithmetic operations

- In this section we study the very popular ALU IC, IC 74LS181. It is a 4-bit Arithmetic Logic Unit (ALU). Its features are as given below :
- Features :**
 - Provides 16 arithmetic operations : add, subtract, compare, double, plus twelve other arithmetic operations.
 - Provides all 16 logic operations of two variables : exclusive-OR, compare, AND, NAND, OR, NOR, plus ten other logic operations.
 - Full lookahead for high speed arithmetic operation on long words.
- Fig. 11.6.1 and Fig. 11.6.2 show the block diagram and connection diagram for IC74LS181.
- As shown in the Fig. 11.6.1, 74LS181 has two four bit operands ($A_0 - A_3$ and $B_0 - B_3$). Its mode select input selects one of the two modes : arithmetic or logic, and four function select inputs select a particular function from the selected mode.

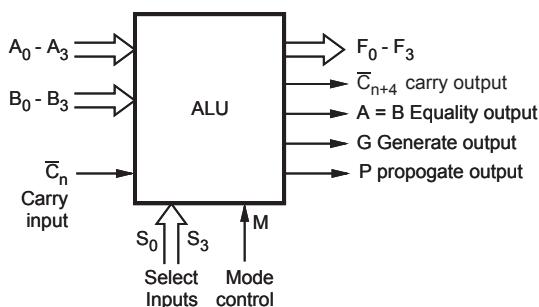


Fig. 11.6.1 Block diagram

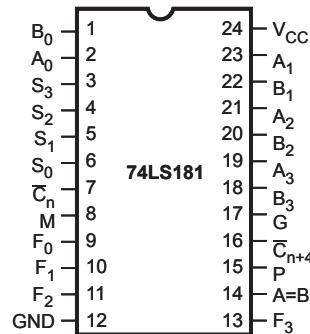


Fig. 11.6.2 Connection diagram

- Table 11.6.1 gives the pin description for IC 74LS181 and Table 11.6.2 gives the function table for IC 74LS181.

Pin Names	Description
A ₀ - A ₃	Operand Inputs
B ₀ - B ₃	Operand Inputs
S ₀ - S ₃	Function Select Inputs
M	Mode Control Input
C _n	Carry Input (Active LOW)
F ₀ - F ₃	Function Outputs
A = B	Comparator Output
G	Carry Generate Output
P	Carry Propagate Output
C _{n+4}	Carry Output (Active LOW)

Table 11.6.1 Pin description of IC 74LS181

Mode Select Inputs				Active HIGH Operands and F _n Outputs	
S ₃	S ₂	S ₁	S ₀	Logic (M = 1)	Arithmetic (Note 2) (M = 0) (C _n = 1)
0	0	0	0	F = \bar{A}	F = A
0	0	0	1	F = $\bar{A} + \bar{B}$	F = A + B
0	0	1	0	F = $\bar{A}B$	F = A + B

0	0	1	1	$F = \text{Logic 0}$	$F = \text{minus 1}$
0	1	0	0	$F = \overline{AB}$	$F = A \text{ plus } \overline{AB}$
0	1	0	1	$F = \overline{B}$	$F = (A + B) \text{ plus } \overline{AB}$
0	1	1	0	$F = A \oplus B$	$F = A \text{ minus } B \text{ minus 1}$
0	1	1	1	$F = A\overline{B}$	$F = AB \text{ minus 1}$
1	0	0	0	$F = \overline{A} + B$	$F = A \text{ plus } AB$
1	0	0	1	$F = \overline{A} \oplus \overline{B}$	$F = A \text{ plus } B$
1	0	1	0	$F = B$	$F = (A + \overline{B}) \text{ plus } AB$
1	0	1	1	$F = AB$	$F = AB \text{ minus 1}$
1	1	0	0	$F = \text{Logic 1}$	$F = A \text{ plus } A \text{ (Note 1)}$
1	1	0	1	$F = A + \overline{B}$	$F = (A + B) \text{ plus } A$
1	1	1	0	$F = A + B$	$F = (A + \overline{B}) \text{ plus } A$
1	1	1	1	$F = A$	$F = A \text{ minus 1}$

Table 11.6.2 (a) Function table for IC 74LS181

Note 1 : Each bit is shifted to the next most significant position.

Note 2 : Arithmetic operations expressed in 2's complement notation.

Mode Select Inputs				Active LOW Operands and F_n Outputs	
				Logic ($M = 1$)	Arithmetic (Note 2) ($M = 0$) ($\overline{C}_n = 0$)
S_3	S_2	S_1	S_0		
0	0	0	0	$F = \overline{A}$	$F = A \text{ minus 1}$
0	0	0	1	$F = \overline{AB}$	$F = AB \text{ minus 1}$
0	0	1	0	$F = \overline{A} + \overline{B}$	$F = A\overline{B} \text{ minus 1}$
0	0	1	1	$F = \text{Logic 1}$	$F = \text{minus 1}$
0	1	0	0	$F = \overline{A} + \overline{B}$	$F = A \text{ plus } (A + \overline{B})$
0	1	0	1	$F = \overline{B}$	$F = AB \text{ plus } (A + \overline{B})$
0	1	1	0	$F = \overline{A} \oplus \overline{B}$	$F = A \text{ minus } B \text{ minus 1}$
0	1	1	1	$F = A + \overline{B}$	$F = A + \overline{B}$
1	0	0	0	$F = \overline{A} B$	$F = A \text{ plus } (A + B)$
1	0	0	1	$F = A \oplus B$	$F = A \text{ plus } B$

1	0	1	0	$F = B$	$F = \bar{AB}$ plus $(A + B)$
1	0	1	1	$F = A + B$	$F = A + B$
1	1	0	0	$F = \text{Logic 0}$	$F = A$ plus A (Note 1)
1	1	0	1	$F = \bar{AB}$	$F = AB$ plus A
1	1	1	0	$F = AB$	$F = \bar{AB}$ minus A
1	1	1	1	$F = A$	$F = A$

Table 11.6.2 (b) Function table for IC 74LS181

Note 1 : Each bit is shifted to the next most significant position.

Note 2 : Arithmetic operations expressed in 2's complement notation.

Functional Description

- The 74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU), controlled by the four Function Select inputs (S_0 - S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands.
- When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed.
- When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words.
- The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the $\bar{C}_n + 4$ output, or for carry lookahead between packages using the signals P (Carry Propagate) and G (Carry Generate).
- In the ADD mode, P indicates that F is 15 or more, while G indicates that F is 16 or more.
- In the SUBTRACT mode, P indicates that F is zero or less, while G indicates that F is less than zero. P and G are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output ($\bar{C}_n + 4$) signal to the Carry input (C_n) of the next unit.
- The $A = B$ output from the device goes HIGH when all four F outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The $A = B$ output is open-collector and can be wired - AND with other $A = B$ out puts to give a comparison for more than four bits. The $A = B$ signal can also be used with the $\bar{C}_n + 4$ signal to indicate $A > B$ and $A < B$.
- The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds one to each operation. Thus, select code 0110

generates A minus B minus 1 (2's complement notation) without a carry in and generates A minus B when a carry is applied.

- Because subtraction is actually performed by complementary addition (1's complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.
- As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Example 11.6.1 Design 8 bit ALU circuit using two 74LS181 ICs.

Solution : Fig. 11.6.3 shows the cascaded connection of two 74LS181 ICs.

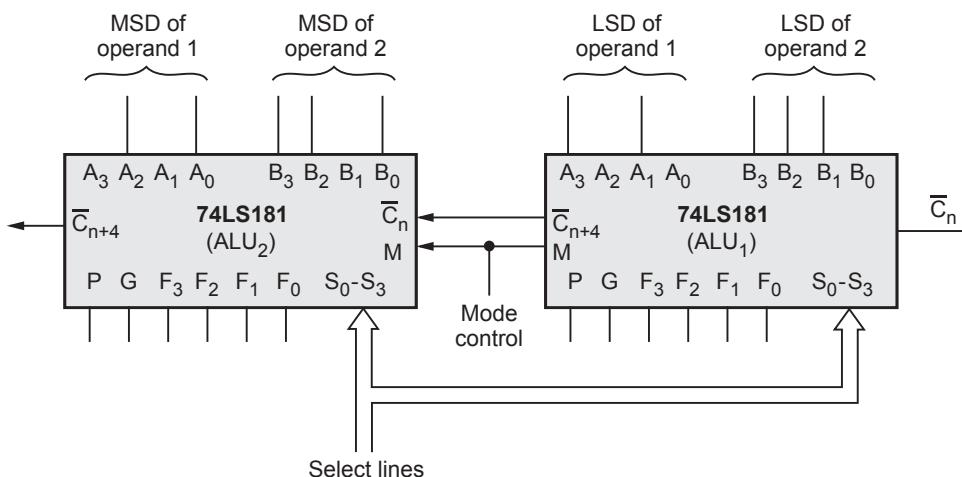


Fig. 11.6.3 8-bit ALU using two 74LS181 ICs

- As shown in the Fig. 11.6.3 mode and select inputs for both ICs are connected in parallel so that they operate in same mode and perform the same function. For ALU₁, carry out (C_{out}) is connected to C_n input of the ALU₂, i.e. carry of one stage is propagated to next stage. The C_{n+4} output of ALU₂ gives the final carry.

Example 11.6.2 Show how the circuit designed in the previous example works for following operations.

1. A - B
 2. A + B
 3. A XOR B
 4. A AND B
- Assume : A = 56₁₀ = 0011 1000₂ and B = 45₁₀ = 0010 1100₂

Solution : A = 56₁₀ = 0011 1000₂ and B = 45₁₀ = 0010 1100₂

Subtraction

0	0	1	0	1	1	0	0
1	1	0	1	0	0	1	1
+							1
1	1	0	1	0	1	0	0

B**1's complement of B****Add 1****2's complement of B****Addition**

	1	1	1				
0	0	1	1	1	0	0	0
0	0	1	0	1	1	0	0

Carry**A****B****Result**

1	1	1					
0	0	1	1	1	0	0	0
+	1	1	0	1	0	1	0

Carry**A****2's complement of B**

Ignore carry **Result**

0	0	0	0	1	1	0	0
---	---	---	---	---	---	---	---

Operation	Mode Control	Select Inputs	Most Significant ALU (ALU ₂)				Least Significant ALU (ALU ₁)				Output			
			Inputs		Outputs		Inputs		Outputs					
	M	S ₃ S ₂ S ₁ S ₀	A	B	\bar{C}_n	S	\bar{C}_{n+4}	A	B	\bar{C}_n	S	\bar{C}_{n+4}	Binary	Decimal
1. A - B	0	0 1 1 0	0011	0010	1	0000	0	1000	1100	0	1100	1	0000 1100	12
2. A + B	0	1 0 0 1	0011	0010	0	0110	1	1000	1100	1	0100	0	0110 0100	100

XOR operation

XOR	0	0	1	1	1	0	0	0
	0	0	1	0	1	1	0	0
	0	0	0	1	0	1	0	0

A
B
Result

AND operation

AND	0	0	1	1	1	0	0	0
	0	0	1	0	1	1	0	0
	0	0	1	0	1	0	0	0

A
B
Result

Operation	Mode Control	Select Inputs	Most Significant ALU (ALU ₂)				Least Significant ALU (ALU ₁)				Output	
			Inputs		Outputs		Inputs		Outputs			
	M	S ₃ S ₂ S ₁ S ₀	A	B	S	A	B	S	Binary	Decimal		
3. A XOR B	1	0 1 1 0	0011	0010	0001	1000	1100	0100	0001 0100	10		
4. A AND B	0	1 0 1 1	0011	0010	0010	1000	1100	1000	0010 1000	100		

Review Questions

1. Draw the block diagram of ALU IC 74181 and explain the function of all important pins.
2. Write a short note on IC 74181.
3. Explain any four arithmetic and four logic functions of ALU IC 74181.
4. Implement an 8-bit ALU using two 74181 ICs.

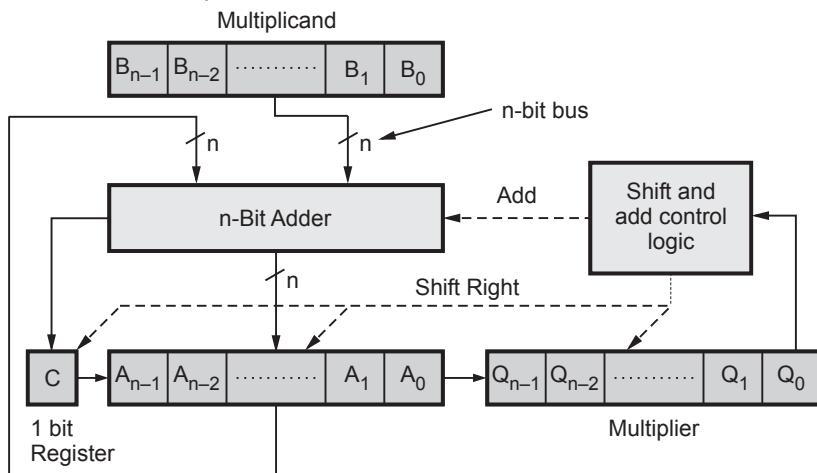
11.7 The 4-bit Multiplier Circuit using ALU and Shift Registers

- The multiplication is a complex operation than addition and subtraction. It can be performed in **hardware** or **software**.
- Fig. 11.7.1 shows the usual algorithm for multiplying positive numbers by hand.
- Looking at this algorithms we can note following points :
 - Multiplication process involves generation of partial products, one for each digit in the multiplier. These partial products are then summed to produce the final product.
 - In the binary system the partial products are easily defined. When the multiplier bit is 0, the partial product is 0, and when the multiplier is 1, the partial product is the multiplicand.
 - The final product is produced by summing the partial products. Before summing operation each successive partial product is shifted one position to the left relative to the preceding partial product, as shown in the Fig. 11.7.1.
 - The product of two n-digit numbers can be accommodated in $2n$ digits, so the product of the two 4-bit numbers in fits into 8-bits.
- Fig. 11.7.2 shows the implementation of manual multiplication approach. It consists of n-bit binary adder, shift and add control logic and four registers, A, B, C.

$$\begin{array}{r}
 1101 \quad (13) \quad \text{Multiplicand} \\
 \times 1001 \quad (9) \quad \text{Multiplier} \\
 \hline
 1101 \\
 0000 \\
 0000 \\
 1101 \\
 \hline
 1110101 \quad \text{Final product (117)}
 \end{array}$$

} Partial products

Fig. 11.7.1 Manual multiplication algorithm



Note : Dotted lines indicate control signals

Fig. 11.7.2 Hardware implementation of unsigned binary multiplication

C and Q. As shown in the Fig. 11.7.2 multiplier and multiplicand are loaded into register Q and register B, respectively, and C are initially set to 0.

Multiplication Operation Steps

1. Bit 0 of multiplier operand (Q_0 of Q register) is checked.
 2. If bit 0 (Q_0) is one then multiplicand and partial product are added and all bits of C, A and Q registers are shifted to the right one bit, so that the C bit goes into A_{n-1} , A_0 goes into Q_{n-1} , and Q_0 is lost. If bit 0 (Q_0) is 0, then no addition is performed, only shift operation is carried out.
 3. Steps 1 and 2 are repeated n times to get the desired result in the A and Q registers.
- A flowchart for multiplication operation is shown in Fig. 11.7.3.

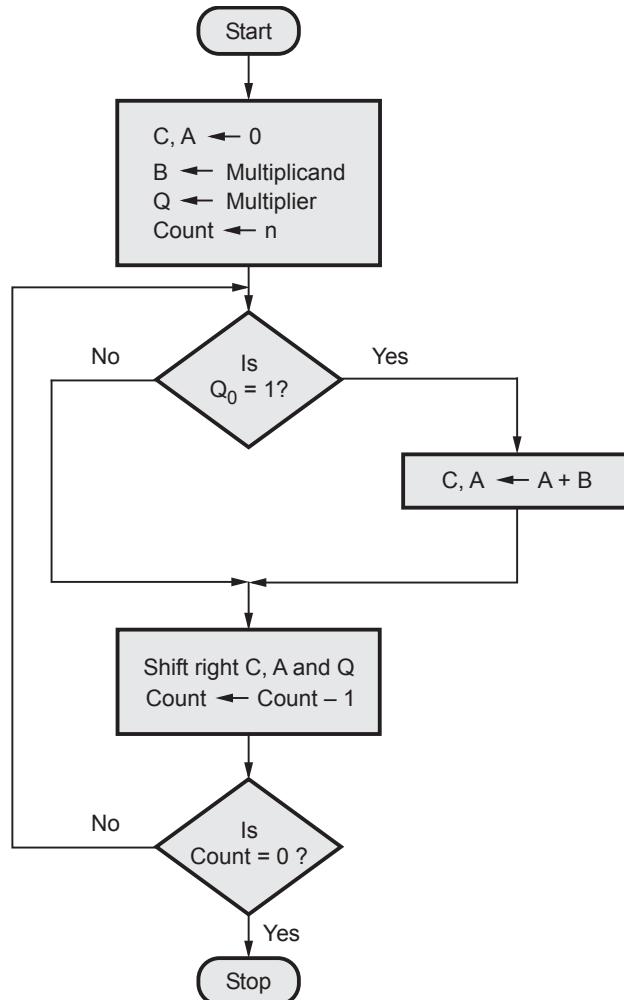


Fig. 11.7.3 Flowchart for multiplication operation

- Let us see one example.

Consider 4-bit multiplier and multiplicand :

Multiplicand = 1 1 0 1 and Multiplier = 1 0 1 1

Fig. 11.7.4 shows operations involved and their results in the multiplication process.

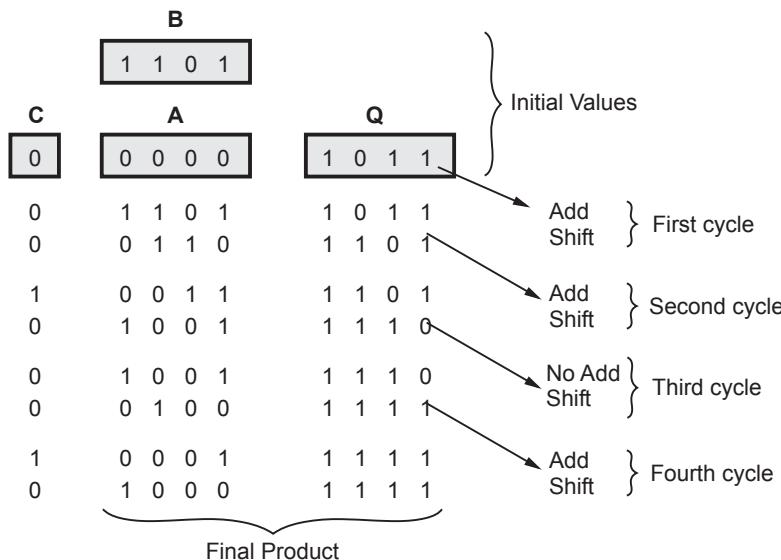


Fig. 11.7.4 Multiplication process

Review Questions

- Explain an algorithm to multiply two positive numbers. Also discuss the realization of a multiplier to implement the same.
- Design a multiplier that multiplies two 4-bit numbers.
- Explain the operation of sequential circuit binary multiplier with
Multiplicand 1101
Multiplier 1011.
- Draw flowchart hardware multiplication algorithm and explain it.

11.8 Memory Organization

- Memories are made up of registers. Each register in the memory is one storage location. Each location is identified by an **address** called **memory address**. The number of storage locations can vary from a few in some memories to hundreds of thousand in others.

- Each location can accommodate one or more bits. Generally, the total number of bits that a memory can store is its capacity. Most of the types the capacity is specified in terms of bytes (group of eight-bits).
- Each register consists of storage elements (flip-flops or capacitors in semiconductor memories and magnetic domain in magnetic storage), each of which stores one-bit of data. A storage element is called a **cell**.
- The data stored in a memory by a process called **writing** and are retrieved from the memory by a process called **reading**. Fig. 11.8.1 illustrates in a very simplified way the concept of write, read, address and storage capacity for a generalized memory.

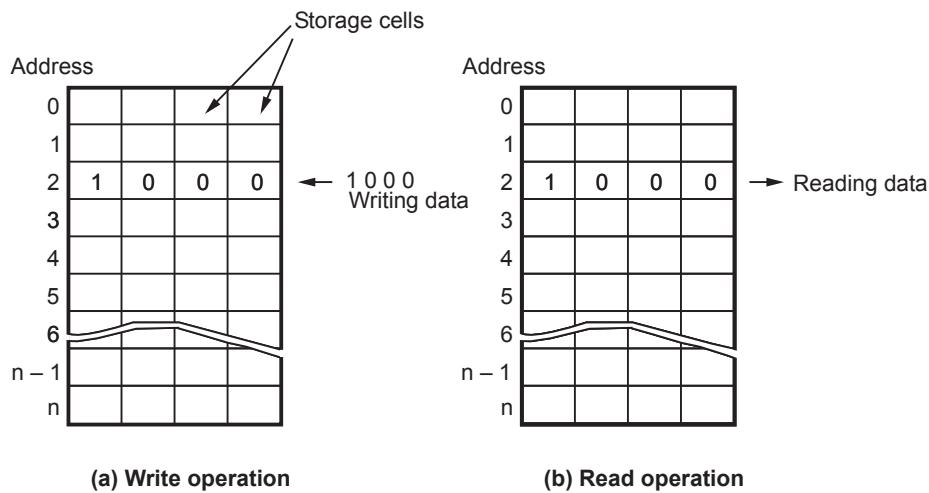


Fig. 11.8.1

- As shown in the Fig. 11.8.1, a memory unit stores binary information in groups of bits called **words**. A word in memory is an entity of bits that moves in and out of storage as a unit. A word having group of 8-bits is called a **byte**. Most computer memories use words that are multiples of eight-bits in length. Thus, a 16-bit word contains two bytes, and a 32-bit word is made of 4 bytes.
- The communication between a memory and its environment is achieved through data lines, address selection lines and control lines that specify the direction of transfer.

11.8.1 Block Diagram of Memory Unit

- Fig. 11.8.2 shows the block diagram of memory unit. The n data lines provide the information to be stored in memory and the k address lines specify the particular word chosen among the many available. The control input R/W (read and write) specify the direction transfer.

- When R/\bar{W} signal is HIGH, read operation is activated and data bus will act as input for memory.
- When R/\bar{W} signal is LOW, write operation is activated and data bus will act as output for memory.
- Another control signal, chip select (CS) or Chip Enable (CE) is used to enable the memory chip for read/write operation. The CS input selects the specified memory chip in a multichip memory system.

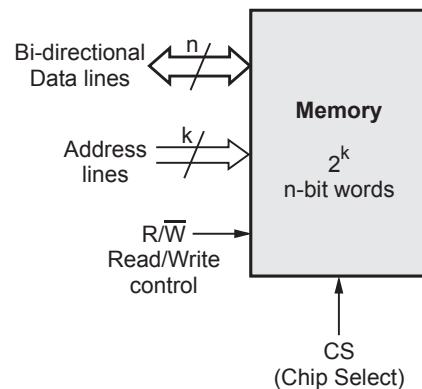


Fig. 11.8.2 Block diagram of memory unit

11.8.2 Digital Circuit using Decoder and Registers for Memory Operations

- Fig. 11.8.3 shows the internal organization of 16 X 4 memory chip. Here, the organization is shown with detail connections of address lines, data lines and control lines.

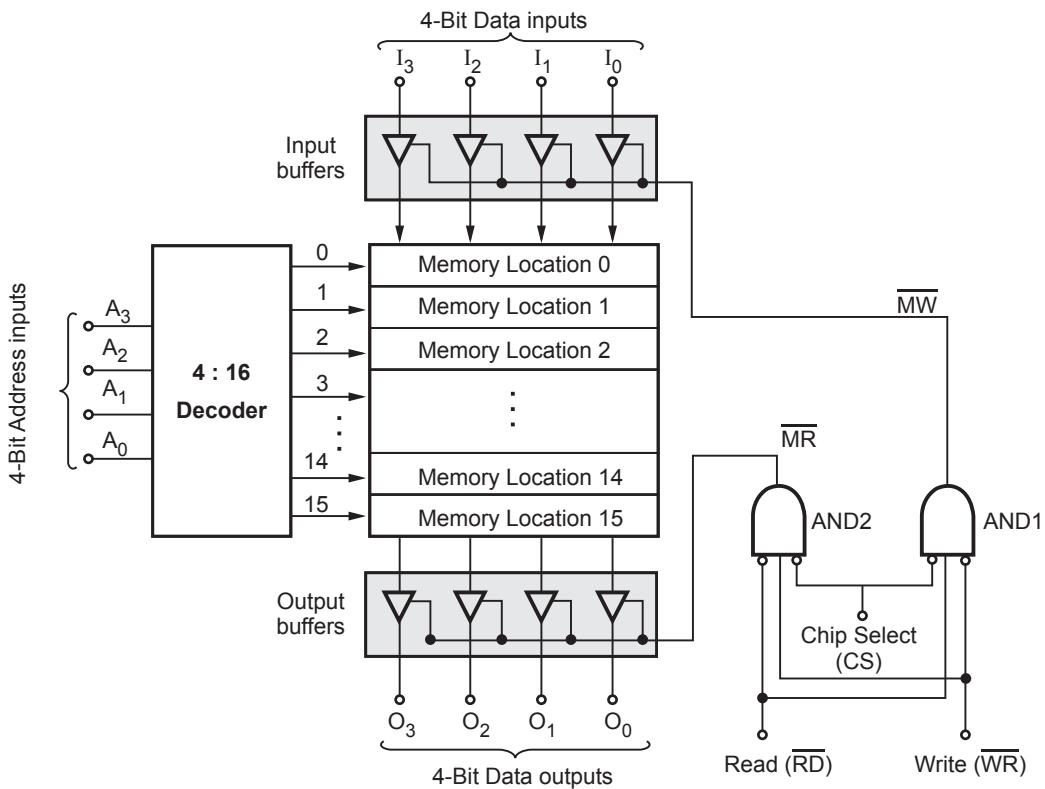


Fig. 11.8.3 Internal organization of 16 X 4 memory chip

- The 4 : 16 decoder is used to decode the contents on address lines and select one of the sixteen possible memory locations.
- Two AND gates circuitry controlled by (\overline{RD}) , (\overline{WR}) and (\overline{CS}) control signals is used to active read/write operation. Note that, here (\overline{RD}) and (\overline{WR}) are the two separate signals.
- Input and output buffers are enabled according to the operation to be performed. For memory write input buffers are enabled and for memory read output buffers are enabled.

Review Questions

1. Write a note on memory organization.
2. Draw and explain the block diagram of memory unit.
3. Draw and explain the internal organization of 16 X 4 memory chip.

11.9 Memory Operation

- The memory unit supports two basic operations : **read** and **write**. The read operation reads previously stored data and the write operation stores a new value in memory.
- Both of these operations require a memory address. In addition, the write operation requires specification of the data to be written.
- Two metrics are used to characterize memory :
- **Access time** refers to the amount of time required by the memory to retrieve the data at the addressed location.
- The other metric is the **memory cycle time**, which refers to the minimum time between successive memory operations.
- The **read operation is non-destructive** in the sense that one can read a location of the memory as many times as one wishes without destroying the contents of that location. The write operation, however, is destructive, as writing a value into a location destroys the old contents of that memory location.

11.9.1 Read Operation

Steps to perform memory read operation are as follows :

1. Place the address of the location to be read on the address bus.
2. Activate the memory read control signal on the control bus.
3. Read the data from the data bus.
4. De-activate the memory read control signal to terminate the read cycle

- Fig. 11.9.1 shows the timing diagram for read cycle.

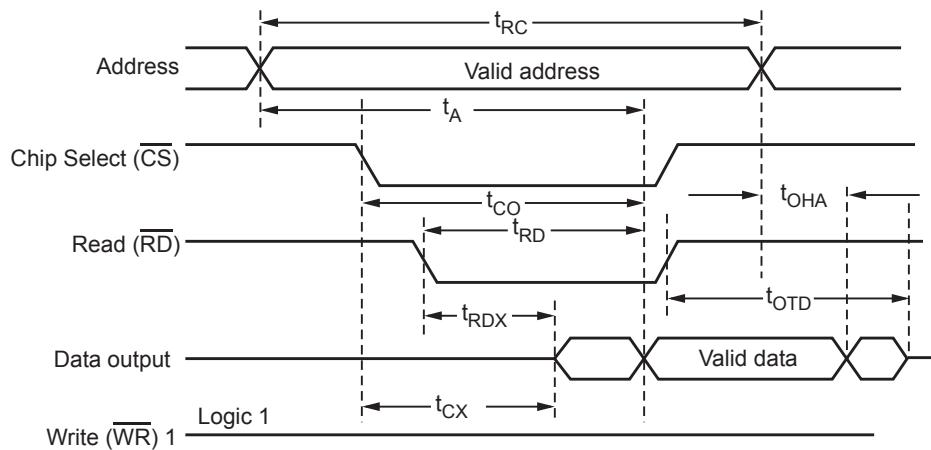


Fig. 11.9.1 Read cycle timing waveform

- The timing diagram is drawn on the basis of different timing parameters. These are as follows :

 - t_{RC} : Read Cycle Time :** It is the minimum time for which an address must be held stable on the address bus, in read cycle.
 - t_A : Address Access Time :** It is the maximum specified time within which a valid new data is available on the data bus after an address is applied.
 - t_{RD} : Read to Output Valid Time :** It is the maximum time delay after (\overline{RD}) goes LOW (beginning of read pulse) and the availability of valid data on the data bus. Using this timing parameter we can specify the maximum rate at which data can be read. It is given as

$$\text{The maximum rate at which data can be read} = \frac{1}{t_{RD}}$$

- For example, if $t_{RD} = 100$ ns,

$$\text{The maximum rate at which data can be read} = \frac{1}{100 \times 10^{-9}} = 10 \times 10^6 \text{ words/s}$$

- t_{RDX} : Read to Output Active Time :** It is the minimum time delay after (\overline{RD}) goes LOW (beginning of read pulse) and the output buffers coming to active state.
- t_{CO} : Chip Select to Output Valid Time :** It is the maximum time delay after (\overline{CS}) goes LOW (beginning of chip select pulse) and the availability of valid data on the data bus.

6. t_{CX} : Chip Select to Output Active Time : It is the minimum delay after (\overline{CS}) goes LOW (beginning of chip select pulse) and the output buffers coming to active state.
7. t_{OTD} : Output tri-state from Read : It is the maximum time delay after (\overline{RD}) goes HIGH (end of read pulse) and the output buffers going to high impedance state.
8. t_{OHA} : Data Hold Time : It is the minimum time for which the valid data is available on the data output after the address ends.

11.9.2 Write Operation

Steps to perform memory write operation are as follows :

1. Place the address of the location to be written on the address bus.
 2. Place the data to be written on the data bus.
 3. Activate the memory write control signal on the control bus.
 4. De-activate the memory write control signal to terminate the write cycle
- Fig. 11.9.2 shows the write cycle for memory.

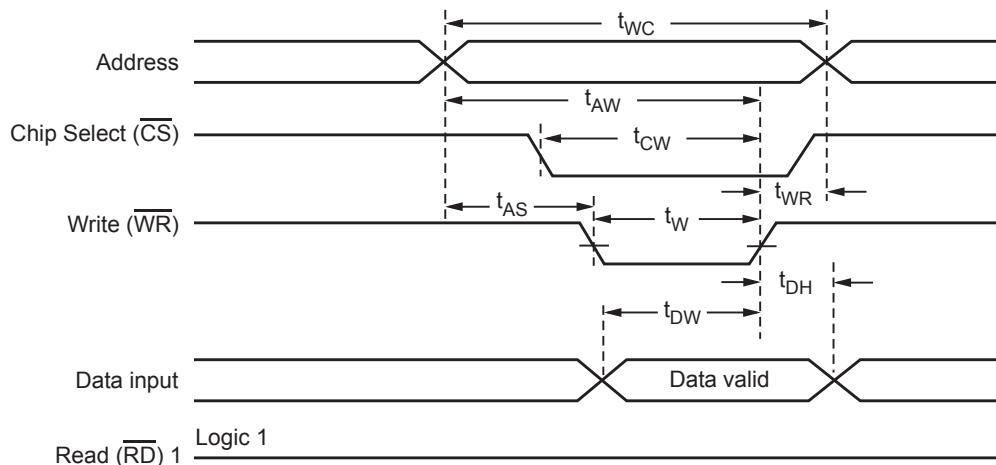


Fig. 11.9.2 Write cycle timing waveform

- The timing diagram is drawn on the basis of different timing parameters. These are as follows :
1. **t_{WC} : Write Cycle Time :** It is the minimum time for which an address must be held stable on the address bus, in write cycle. Using this timing parameter we can specify the maximum rate at which data can be stored. It is given as

$$\text{The maximum rate at which data can be stored} = \frac{1}{t_{WC}}$$

For example if $t_{WC} = 200$ ns,

- The maximum rate at which data can be stored = $\frac{1}{200 \times 10^{-9}} = 5 \times 10^6$ words/s
- 2. **t_{AW} : Address Valid to End of Write** : It is the time at which address must be applied on the address bus before WR goes high.
- 3. **t_{WR} : Write Recovery Time** : It is the time for which address will remain on address bus after WR goes high.
- 4. **t_{AS} : Address Setup Time** : When address is applied, it is the time after which WR can be made low.
- 5. **t_{CW} : Chip Selection to the End of Write** : It is the time at which the CS must be made low to select the device before WR goes high.
- 6. **t_W : Write Pulse Width** : It is the time for which WR goes low.
- 7. **t_{DW} : Data Valid to the End of Write** : It is the minimum time for which data must be valid on the data bus before WR goes high.
- 8. **t_{DH} : Data Hold Time** : It is the time for which data must be held valid after WR goes high.

Review Questions

1. Write a note on memory read operation.
2. Write a note on memory write operation.
3. Explain the read cycle waveform for memory.
4. Explain the write cycle waveform for memory.
5. Define timing parameters : t_{WR} , t_{WC} , t_{CO} , t_{RD} , t_{RC} .



Notes

Notes