



<b>Course Name:</b>	<b>Microprocessors and Peripherals (2UXC404)</b>	<b>Semester:</b>	<b>IV</b>
<b>Date of Performance:</b>	20/1/2021	<b>Batch No:</b>	B2
<b>Faculty Name:</b>	KCS	<b>Roll No:</b>	1912052
<b>Faculty Sign &amp; Date:</b>		<b>Grade/Marks:</b>	___/25

### **Experiment No: 1**

**Title:** Addition and Subtraction of two 8-bit and two 16-bit numbers

#### **Aim and Objective of the Experiment:**

**Aim:** Write an 8085 based ALP to

- Add two 8 bit numbers
- Add two 16 bit numbers with carry.
- Subtract two 8 bit numbers with a display of borrow.
- Subtract two 16 bit numbers with a display of borrow

#### **Objectives:**

To study basic instructions and addressing modes of 8085.

This experiment covers following instructions groups.

- Data transfer
- Arithmetic
- Logical
- Branch

#### **COs to be achieved:**

**CO 1.** Describe basic operation of 8085 microprocessor system and explain its timing diagrams.

#### **Useful links**

Virtual Lab:

[http://vlabs.iitb.ac.in/vlabs-dev/labs\\_local/microprocessor/labs/explist.php](http://vlabs.iitb.ac.in/vlabs-dev/labs_local/microprocessor/labs/explist.php)

Simulator:

<https://www.sim8085.com/>

#### **Work to be done**

- Upload codes for addition of 8 bit and 16 bit addition and 8-bit and 16 bit subtraction and screenshots of virtual lab implementation.
- Upload scanned image of handwritten algorithm/flowchart and code and results for post lab questions.

Sim8085

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Registers

A/PSW 0x 2A 02

BC 0x 00 00

DE 0x 00 00

HL 0x 75 03

SP 0x FF FF

PC 0x 08 09

Flags

Z ☐

S ☐

P ☐

C ☐

AC ☐

main.asm

```
1 LXI H,7501H
2 MOV A,M
3 INX H
4 ADD M
5 INX H
6 MOV M,A
7 HLT
```

Load at 0x0800

Memory View

0x 7501

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
750	00	19	11	2A	00	00	00	00	00	00	00	00	00	00	00	00
751	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
752	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
753	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
754	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
755	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
756	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
757	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
758	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
759	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
75A	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
75B	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
75C	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
75D	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
75E	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
75F	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

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Registers

A/PSW 0x 00 02

BC 0x 00 00

DE 0x 04 05

HL 0x 06 08

SP 0x FF FF

PC 0x 08 15

Flags

Z ☐

S ☐

P ☐

C ☐

main.asm

```
1 LHLD 7601H
2 XCHG
3 LHLD 7603H
4 MVI C,00H
5 DAD D
6 JNC down
7 INR C
8 MOV A,C
9 STA 7613H
10 down: SHLD 7611H
11 HLT
```

Load at 0x0800

Memory View

0x 7600

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
760	00	05	04	03	02	00	00	00	00	00	00	00	00	00	00	00
761	00	08	06	00	00	00	00	00	00	00	00	00	00	00	00	00
762	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
763	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
764	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
765	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
766	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
767	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
768	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
769	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
76A	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
76B	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
76C	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
76D	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
76E	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

four\_bit\_adder\_na...vhd

four\_bit\_adder\_na...vhd

Show all

Sim8085 - A 8085 microprocesso x (31) WhatsApp Virtual Labs

sim8085.com

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**Registers**

A/PSW	0x F0 87
BC	0x 00 00
DE	0x 04 05
HL	0x 76 03
SP	0x FF FF
PC	0x 08 08

**Flags**

Z	<input type="checkbox"/>
S	<input checked="" type="checkbox"/>
P	<input checked="" type="checkbox"/>
C	<input checked="" type="checkbox"/>

**main.asm**

```

1
2 LXI H, 7601H
3 MOV A, M
4 INX H
5 SBB M
6 INX H
7 MOV M, A
8 HLT
9

```

**Memory View** 0x 7600

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
760	00	25	35	F0	00	00	00	00	00	00	00	00	00	00	00	00
761	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
762	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
763	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
764	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
765	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
766	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
767	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
768	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
769	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
76A	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
76B	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
76C	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
76D	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
76E	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

four\_bit\_adder\_na....vhd

Sim8085 - A 8085 microprocesso x (32) WhatsApp Virtual Labs

sim8085.com

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**Registers**

A/PSW	0x FF 97
BC	0x 00 00
DE	0x 00 11
HL	0x FF E0
SP	0x FF FF
PC	0x 08 10

**Flags**

Z	<input type="checkbox"/>
S	<input checked="" type="checkbox"/>
P	<input checked="" type="checkbox"/>
C	<input checked="" type="checkbox"/>

**main.asm**

```

1 LHLD 7501H
2 XCHG
3 LHLD 7503H
4 MOV A,E
5 SUB L
6 MOV L,A
7 MOV A,D
8 SBB H
9 MOV H,A
10 SHLD 7505H
11 HLT

```

**Memory View** 0x 7500

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
750	00	11	00	31	00	E0	FF	00	00	00	00	00	00	00	00	00
751	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
752	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
753	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
754	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
755	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
756	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
757	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
758	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
759	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
75A	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
75B	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
75C	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
75D	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
75E	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

MAP\_exp 1.1912....docx four\_bit\_adder\_na....vhd four\_bit\_adder\_na....vhd

### Post Lab Subjective/Objective type Questions:

Q1. Write an 8085 based ALP to find 16 bit sum for an array of numbers. Assume length of the array in memory location C020H and array actually starts from C021H. Store the 16-bit sum in memory locations C030H and C031H

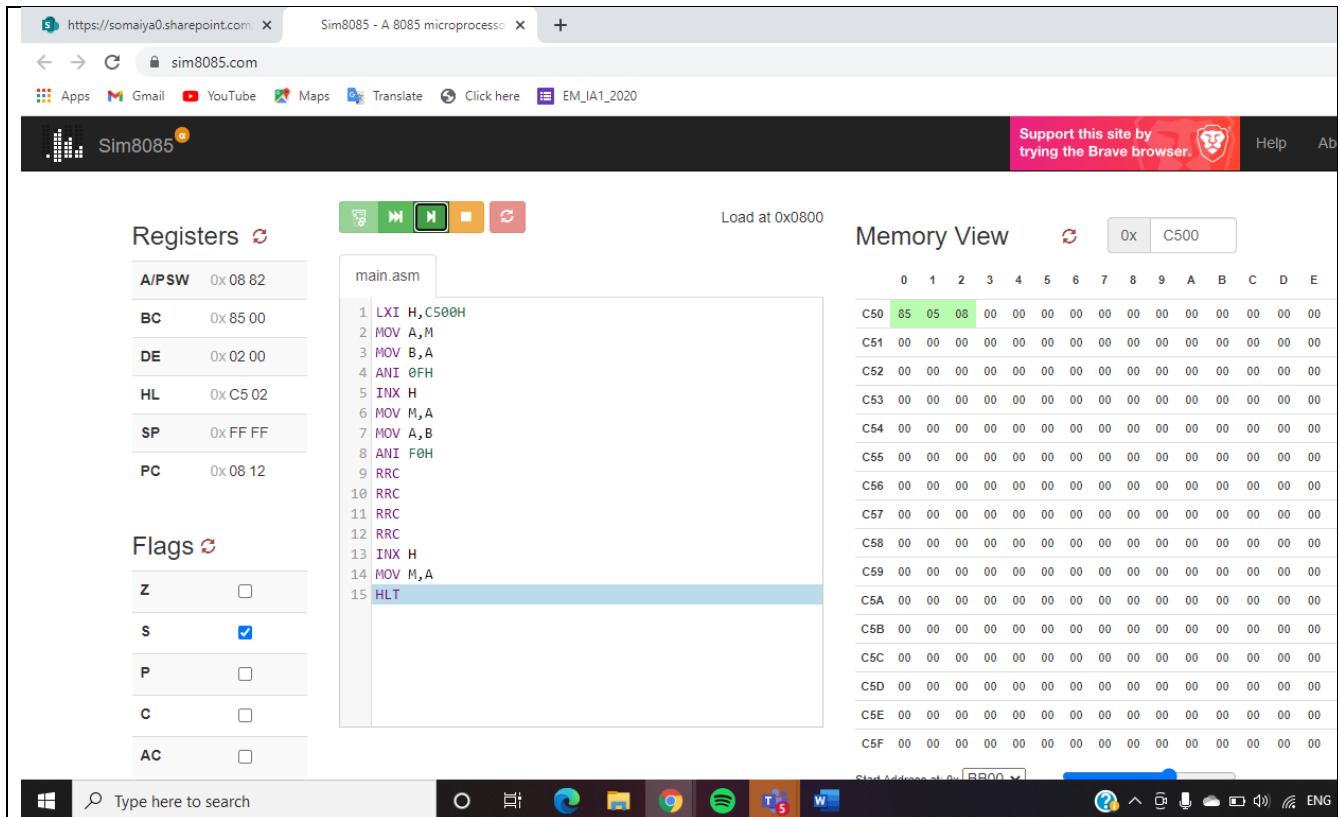
			1912052
0800	3A	LDA C020H	Load content of C020H into accumulator.
0801	20		
0802	00		
0803	4F	MOV C,A	content of accumulator into C register.
0804	21	LXI H,C021H	Load immediate content of C021H into HL pair.
0805	21		
0806	00		
0807	AF	XRA A	XOR acc. w/ itself.
0808	16	MVI D,00	move immediate 00 into D register.
0809	00		
080A	86	UPADD N	ADD HL with accumulator.
080B	2C	INRL	Increment L register.
080C	D2	JNC NXT	jump if no carry to NXT.

1912052

080D	10		
080E	08		
080F	14	INR D	increment D register.
0810	DD	NXT DCRC	Decrement C register.
0811	C2	JNX UP	Jump if not zero to UP.
0812	08		
0813	0A		
0814	32	STA C030H	store content of accm into C030H.
0815	30		
0816	C0		
0817	7A	MOV A, D	move D to accm
0818	32	STA C031H	store content of accm into C031H
0819	31		
081A	C0		
081B	76	HLT	halt

Q2. Write an 8085 based ALP to unpack a packed BCD number. Assume a packed BCD number in memory C500H. Disassemble the word into two nibbles. Store the lower unpacked BCD digit into the LSB position of C501H and the upper nibble (BCD digit) in the LSB position of C502H





Q3. What are the different addressing modes of 8085?

- **Immediate addressing mode:**  
In this mode, the source operand is always a data. Like LXI, MVI etc
- **Register addressing mode:**  
The data that is to be operated is available in the register and the operand is also a register. For eg. MOV A,B: moves data stored in register B to register A
- **Register Indirect addressing mode:**  
The data to be operated is available inside a memory location and that memory location is indirectly specified by a register pair. For eg. LDAX B: moves contents of B-C register to the accumulator
- **Direct addressing mode:**  
The data to be operated is available inside a memory location and that memory location is directly specified as an operand. The operand is directly available in the instruction itself.

For eg. LHLD addr: loads the data from memory location to HL pair

**Table to be used for Writing the code for Postlab Questions**



Address	Opcode	Label	Mnemonics	Comments

Format for writing result for postlab questions				
	Memory Location	Contents	Memory Location	Contents
	Before execution		After execution	

**Conclusion:**

We achieved Addition and Subtraction of two 8-bit and two 16-bit numbers using simulator 8085.

**Signature of faculty in-charge with Date:**