AUDIT COURSE ELECTRONIC CIRCUITS 1:
SIMULATION BASED STUDY

LAB 15

Kindly update your name and roll no, once this document is shared with you
Time slot to complete your work is **40 MINUTES**
Date: 28/9/2020
Kindly upload your schematic & waveform images here, every 10 minutes, indicating your progress and intention to completion of WORK within time slot allotted

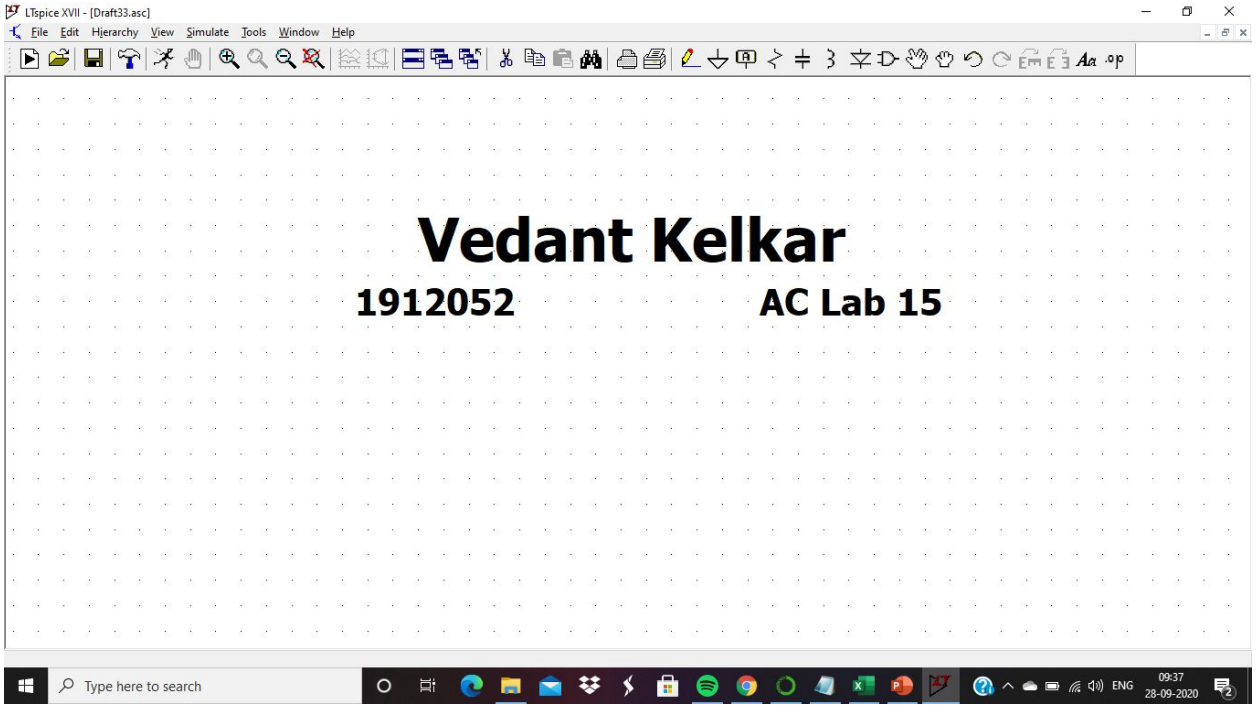
Time slot allotted to you all for the completion of WEEK 8 DAY 1 is 40 MINUTES

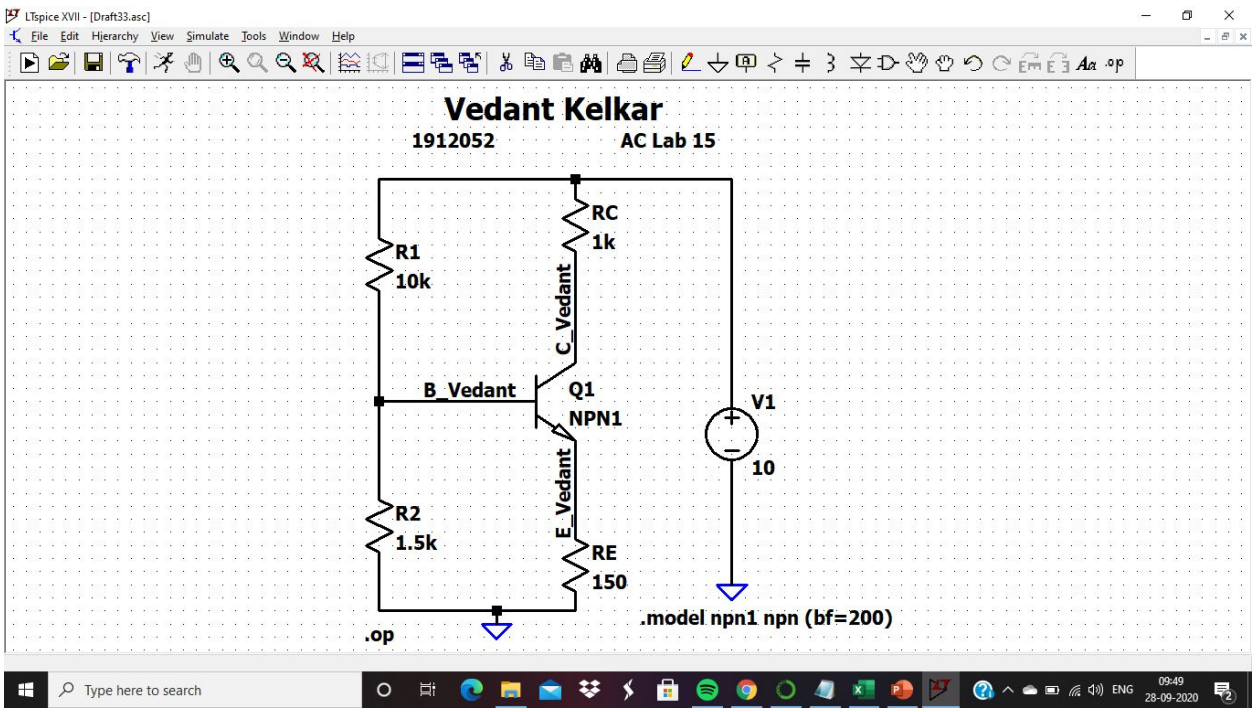
Kindly upload your work (only circuit schematic & waveform in LTSpice) in the shared google doc between this time slot only.

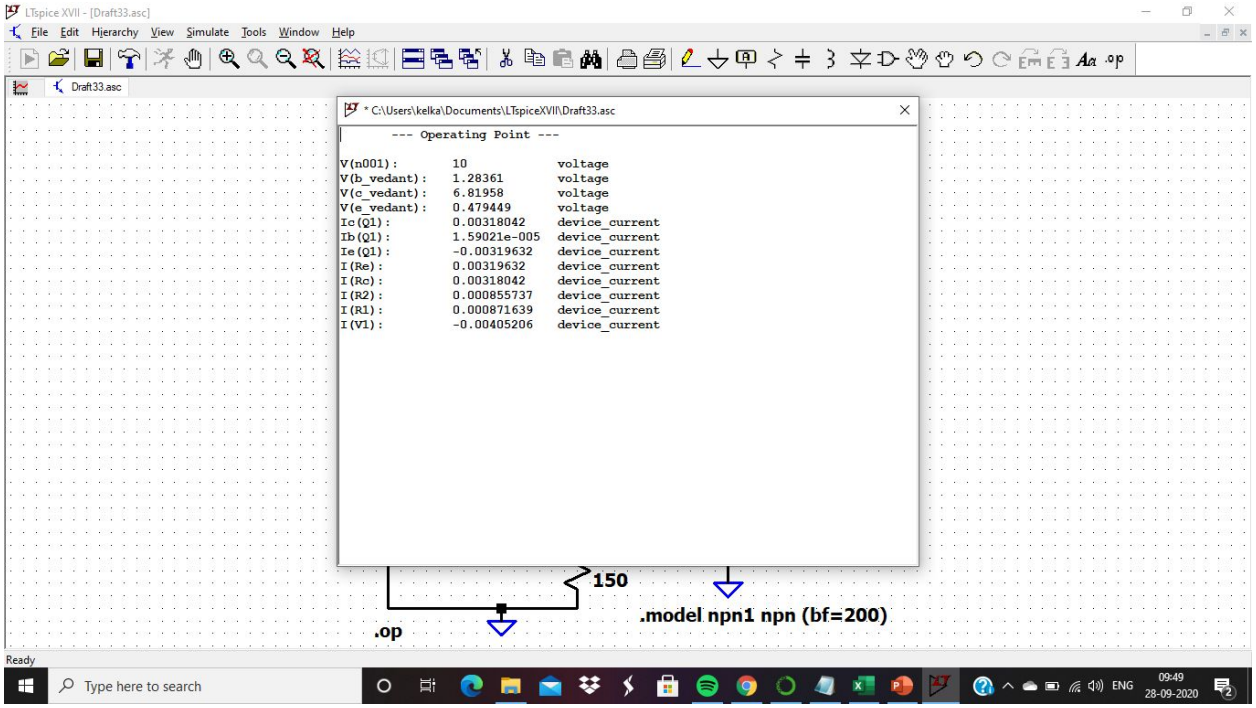
Follow these instruction strictly:
1, Start sharp ON TIME, by posting your name and roll no and **screenshot of your LT spice work screen (time and date MUST BE VISIBLE)**
2. Upload your work every 10 minutes, i.e LT spice work screen
3. This means you will upload LT spice work screen 4 times during this time slot.
4. Point 3 indicates your readiness and presences for completion of WEEK 8 DAY 1

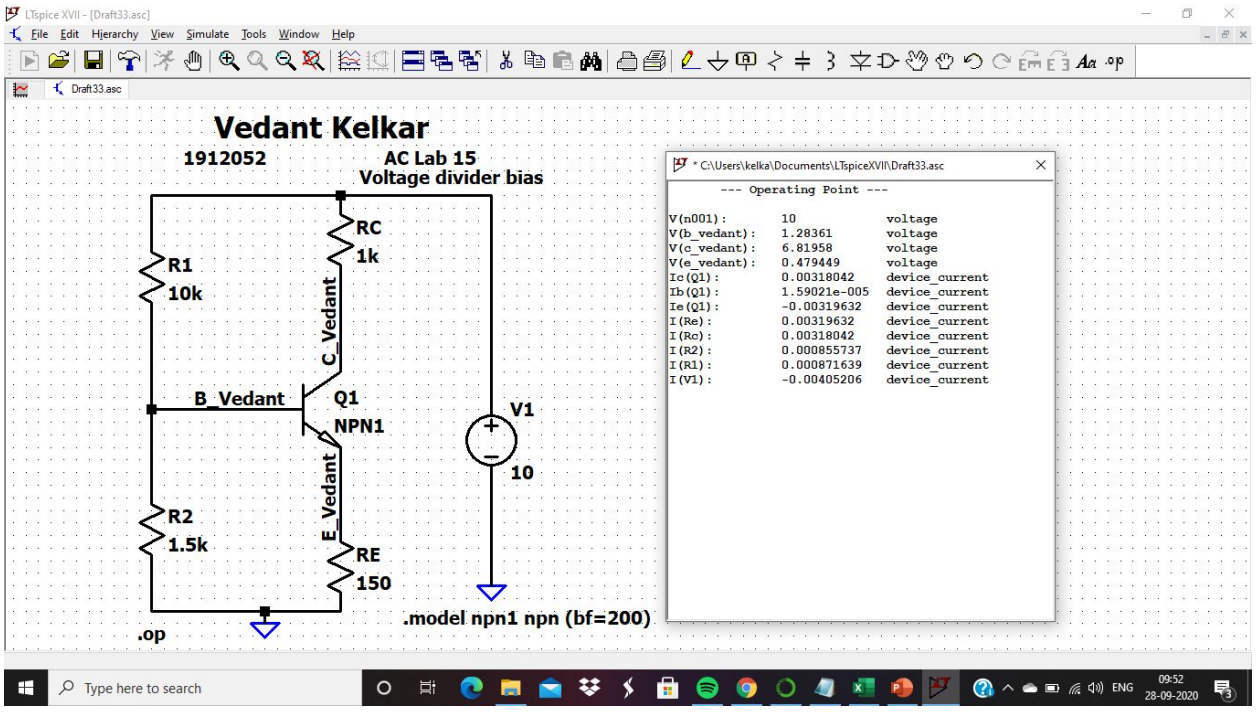
You are entitled for 1 CREDIT per Lab only if you follow above instruction to the details

STUDENTS WORK AREA STARTS HERE


LTspice XVII - [Draft33.asc]
File Edit Hierarchy View Simulate Tools Window Help
Vedant Kelkar
1912052
AC Lab 15
Type here to search
ENG
09:37
28-09-2020

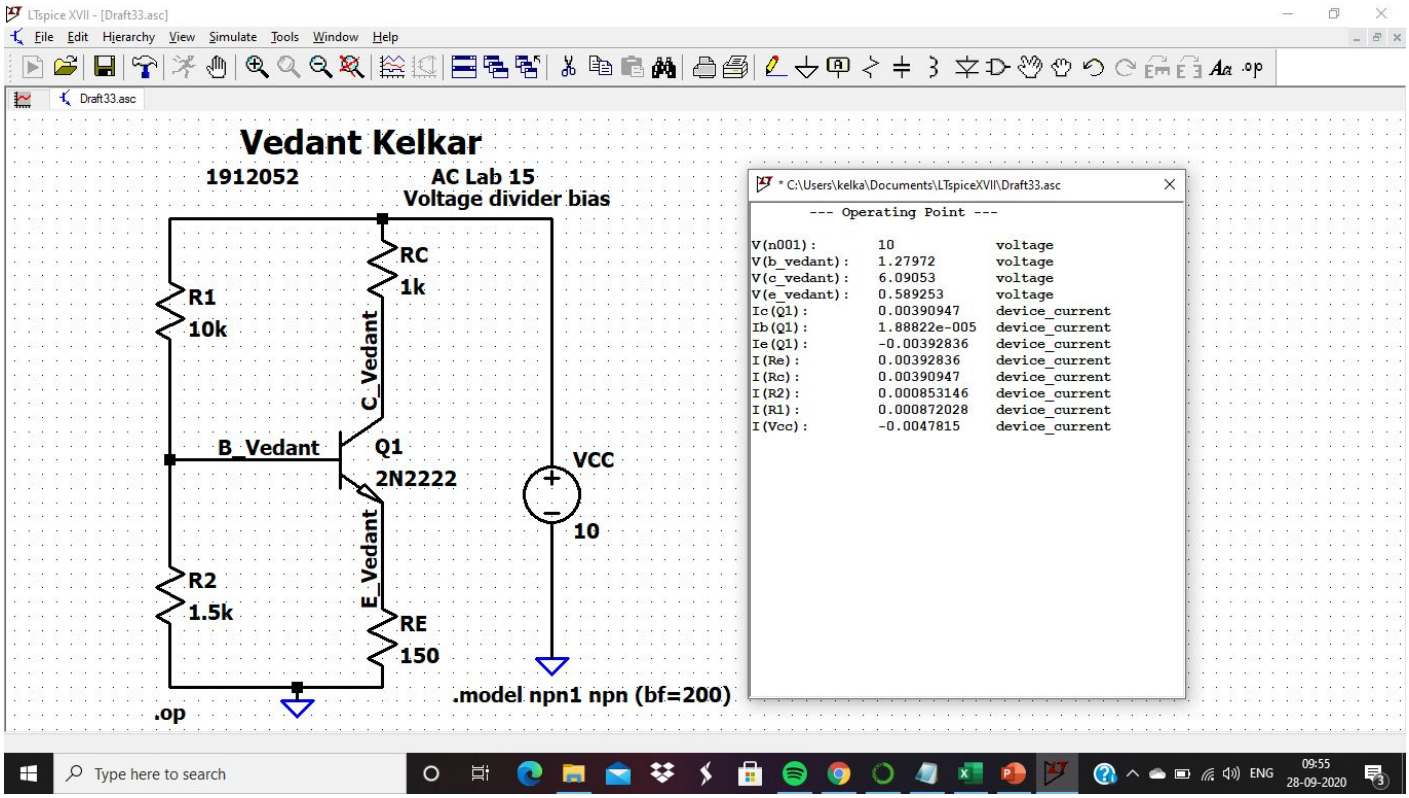

LTspice XVII - [Draft33.asc]
File Edit Hierarchy View Simulate Tools Window Help
Vedant Kelkar
1912052
AC Lab 15
RC
1k
R1
10k
C_Vedant
B_Vedant
Q1
NPN1
V1
10
E_Vedant
R2
1.5k
RE
150
.op
.model npn1 npn (bf=200)
Type here to search
ENG
09:49
28-09-2020





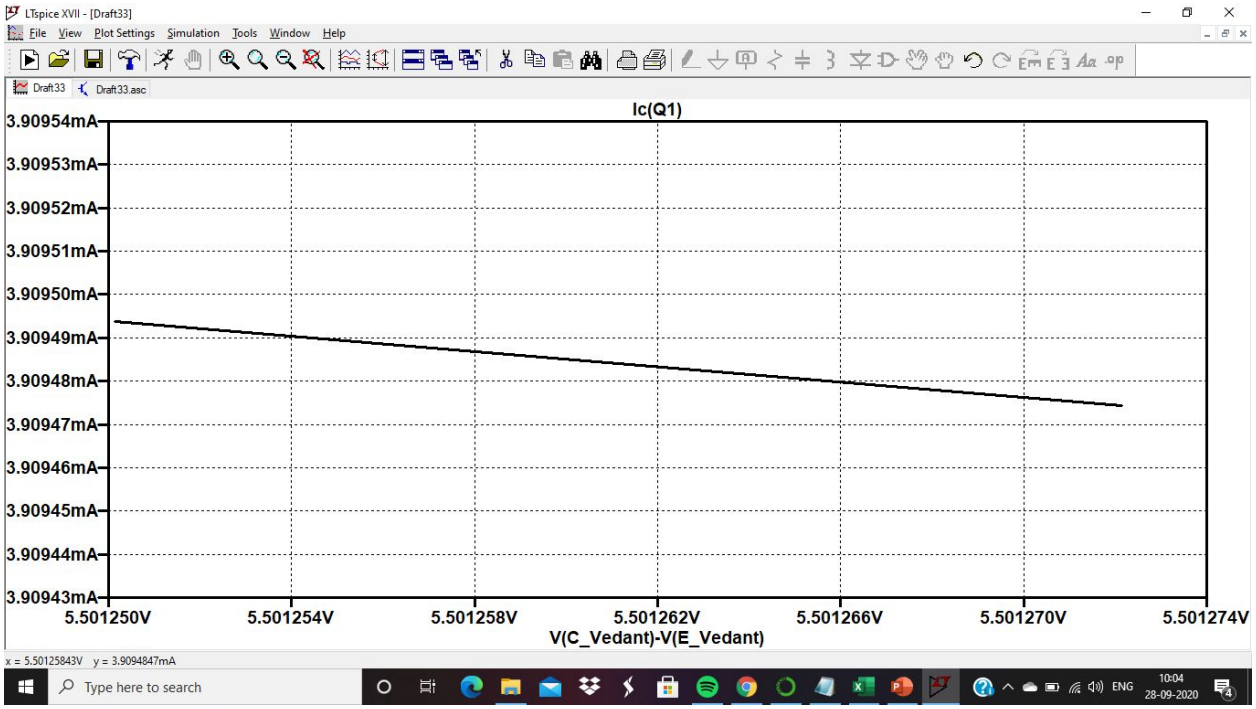
2N222 TRANSISTER

B=200



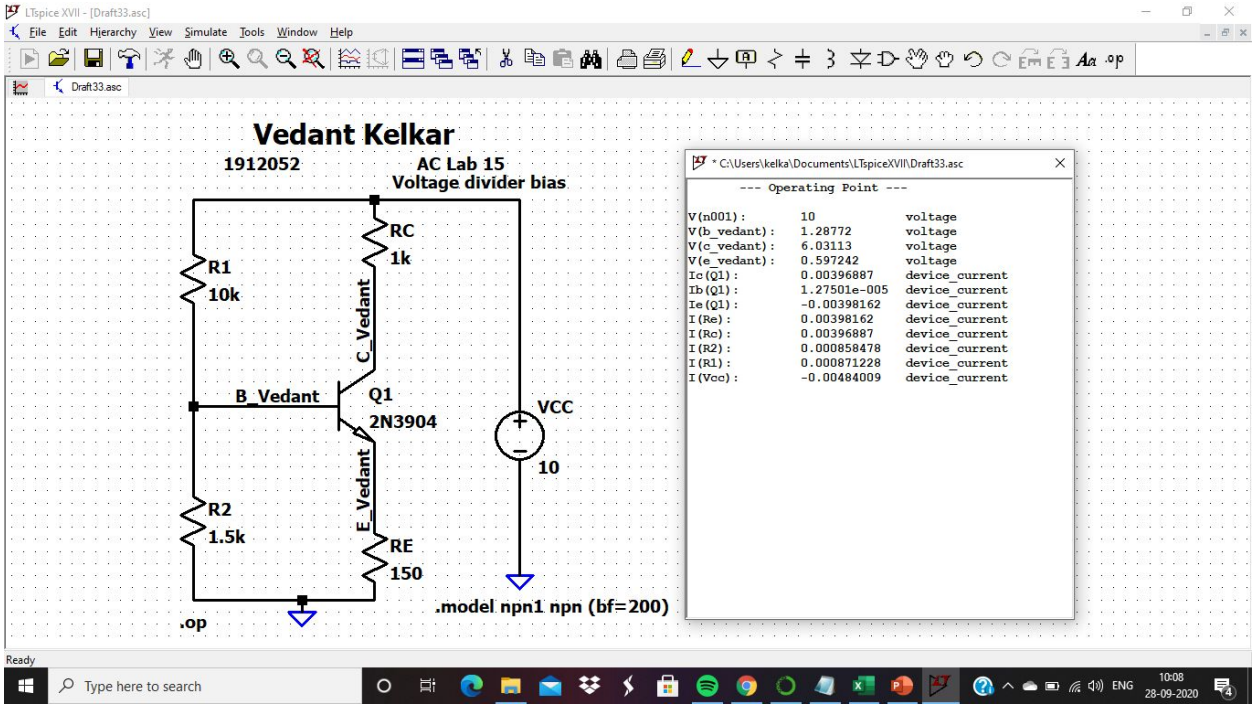
V(n001): 10 voltage
V(b_vedant): 1.27972 voltage
V(c_vedant): 6.09053 voltage
V(e_vedant): 0.589253 voltage
Ic(Q1): 0.00390947 device_current
Ib(Q1): 1.88822e-005 device_current
Ie(Q1): -0.00392836 device_current
I(Re): 0.00392836 device_current
I(Rc): 0.00390947 device_current
I(R2): 0.000853146 device_current
I(R1): 0.000872028 device_current
I(Vcc): -0.0047815 device_current

IBQ Simulted	IBQ Calculated	ICQ Simulted	ICQ Calculated	VCEQ Simulted	VCEQ Calculated
18.88uA	19.2uA	3.909uA	3.84uA	5.501V	5.584V



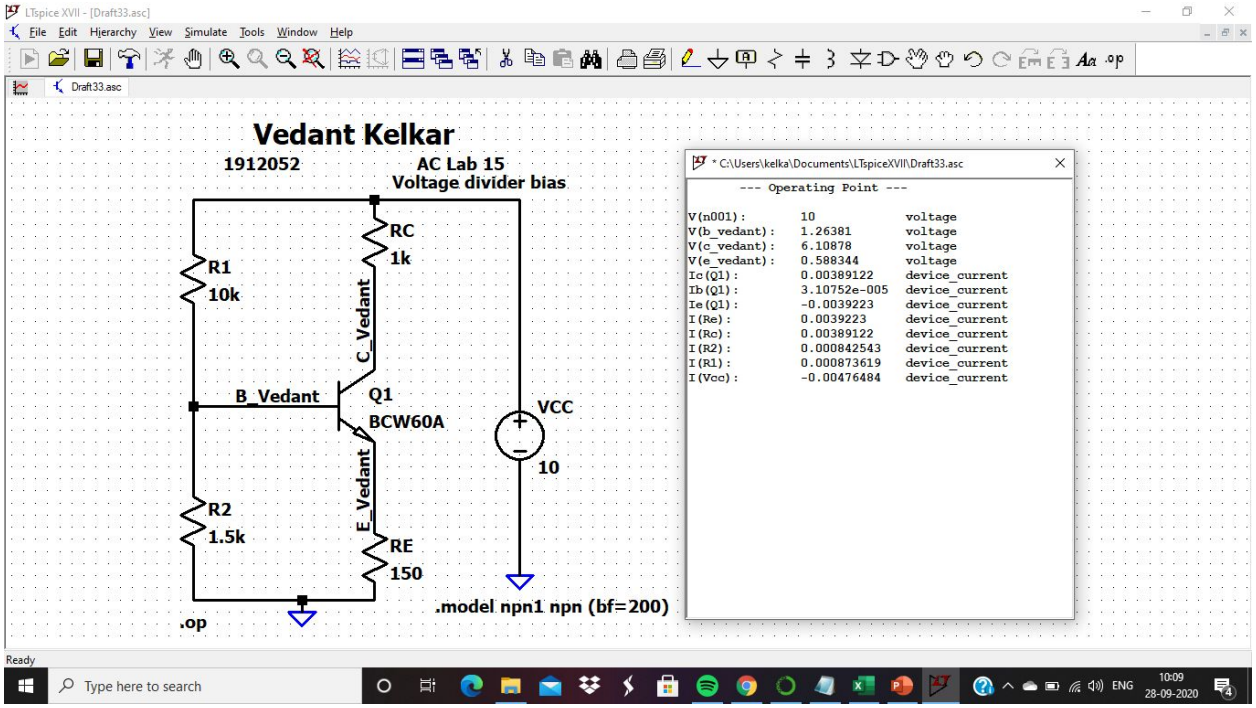
2N3904 TRANSISTER

B=300



V(n001): 10 voltage
V(b_vedant): 1.28772 voltage
V(c_vedant): 6.03113 voltage
V(e_vedant): 0.597242 voltage
Ic(Q1): 0.00396887 device_current
Ib(Q1): 1.27501e-005 device_current
Ie(Q1): -0.00398162 device_current
I(Re): 0.00398162 device_current
I(Rc): 0.00396887 device_current
I(R2): 0.000858478 device_current
I(R1): 0.000871228 device_current
I(Vcc): -0.00484009 device_current

BVW60A TRANSISTER
B=120



V(n001): 10 voltage
V(b_vedant): 1.26381 voltage
V(c_vedant): 6.10878 voltage
V(e_vedant): 0.588344 voltage
Ic(Q1): 0.00389122 device_current
Ib(Q1): 3.10752e-005 device_current
Ie(Q1): -0.0039223 device_current
I(Re): 0.0039223 device_current
I(Rc): 0.00389122 device_current
I(R2): 0.000842543 device_current
I(R1): 0.000873619 device_current
I(Vcc): -0.00476484 device_current

B	ICQ	VCQ
120	3.8912mA	5.521V
200	3.909mA	5.5008V
300	3.968mA	5.4338V

Day

Date

syng

Thevinin at B

1912052

$R_{th} = R_1 \| R_2$

$R_{TH} = \frac{10\times10^3 \times 1.5\times10^3}{10\times10^3 + 1.5\times10^3}$

$= 1.304 k\Omega$

$V_{th} = \frac{R_2}{R_1+R_2} \times V_{CC} = \frac{1.5}{1.5+10} \times 100 = 1.304V.$

KVL at BE.

$V_{TH} - I_B R_{th} - V_{BE} - I_E R_E = 0$

$V_{th} - I_B R_{th} - V_{BE} - (1+\beta) I_B R_E = 0$

$I_{BQ} = 19.202 \mu A$

$I_{CQ} = R I_{bQ} = 200 \times 19.202 \times 10^{-6}$

$I_{CQ} = 3.84 mA$

AC LAB 15 is approved: Inderjit Singh Dhanjal