Audit Course Session 14

AUDIT COURSE
ELECTRONIC CIRCUITS 2: SIMULATION BASED STUDY

Kindly update your name and roll no, once this document is shared with you
Time slot to complete your work is **40 MINUTES**
Date: 16/3/2021
Kindly upload your schematic & waveform images here, every 10 minutes, indicating your progress and intention to completion of WORK within time slot allotted

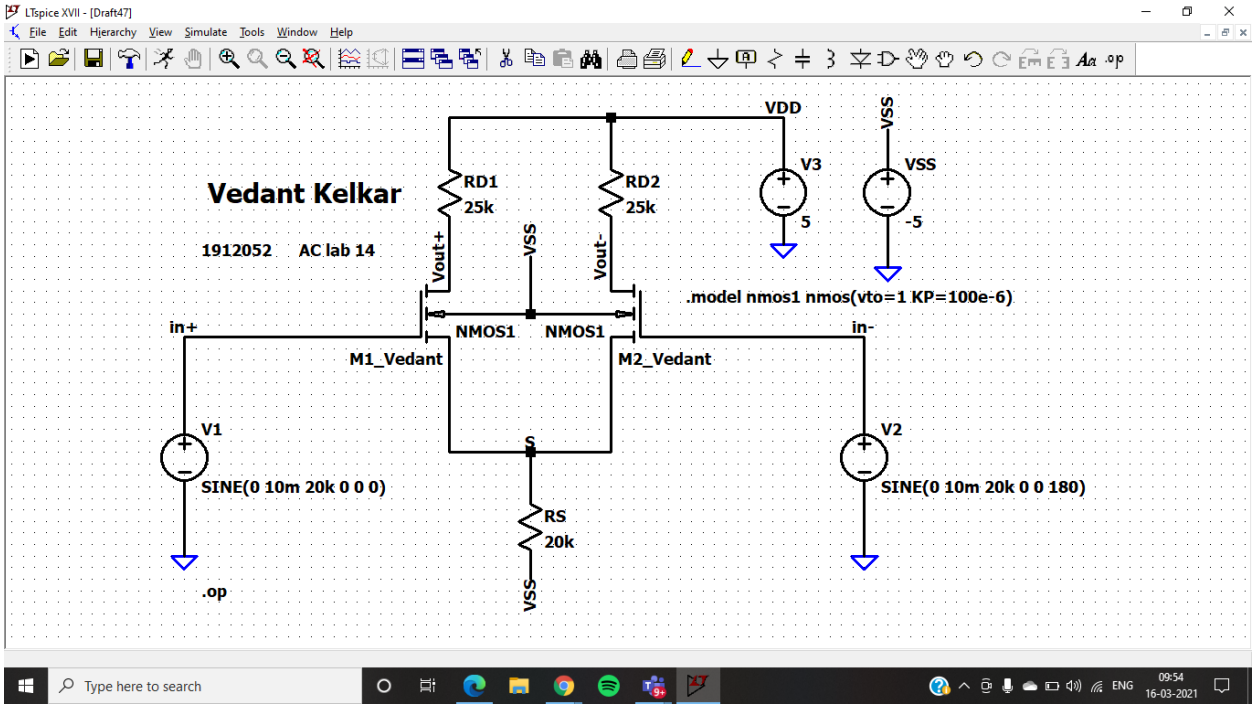
Time slot allotted to you all for the completion of Session 14 is 40 MINUTES

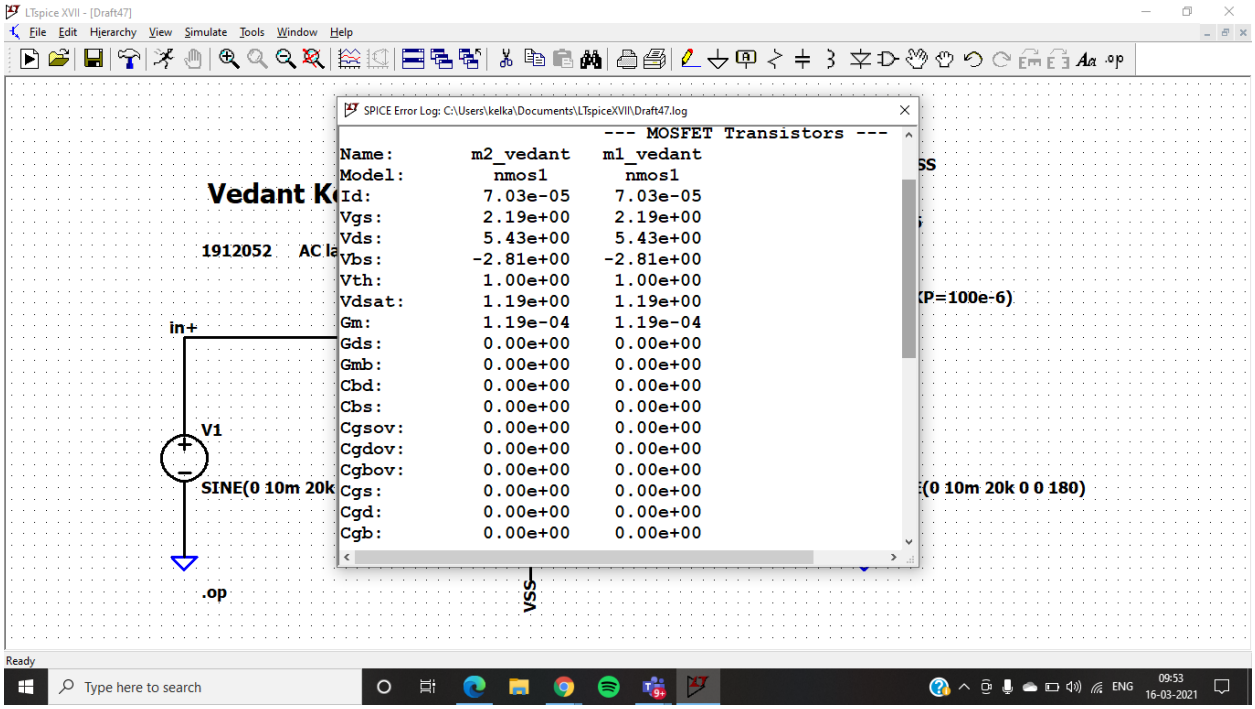
Kindly upload your work (only circuit schematic & waveform in LTspice) in the shared google doc between this time slot only.

Follow these instruction strictly:
1, Start sharp ON TIME, by posting your name and roll no and **screenshot of your LT spice work screen (time and date MUST BE VISIBLE)**
2. Upload your work every 10 minutes, i.e LT spice work screen
3. This means you will upload LT spice work screen 4 times during this time slot.
4. Point 3 indicates your readiness and presences for completion of Session 14

You are entitled for 10 points per session only if you follow above instruction to the details

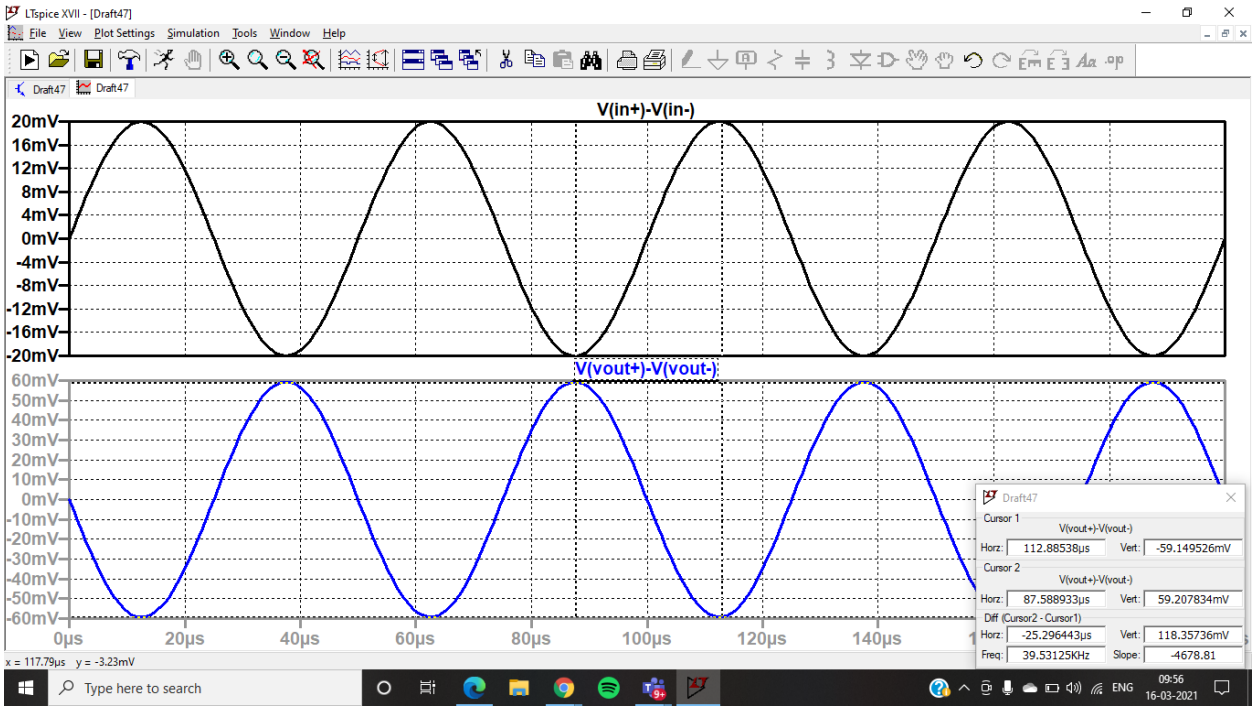
STUDENTS WORK AREA STARTS HERE

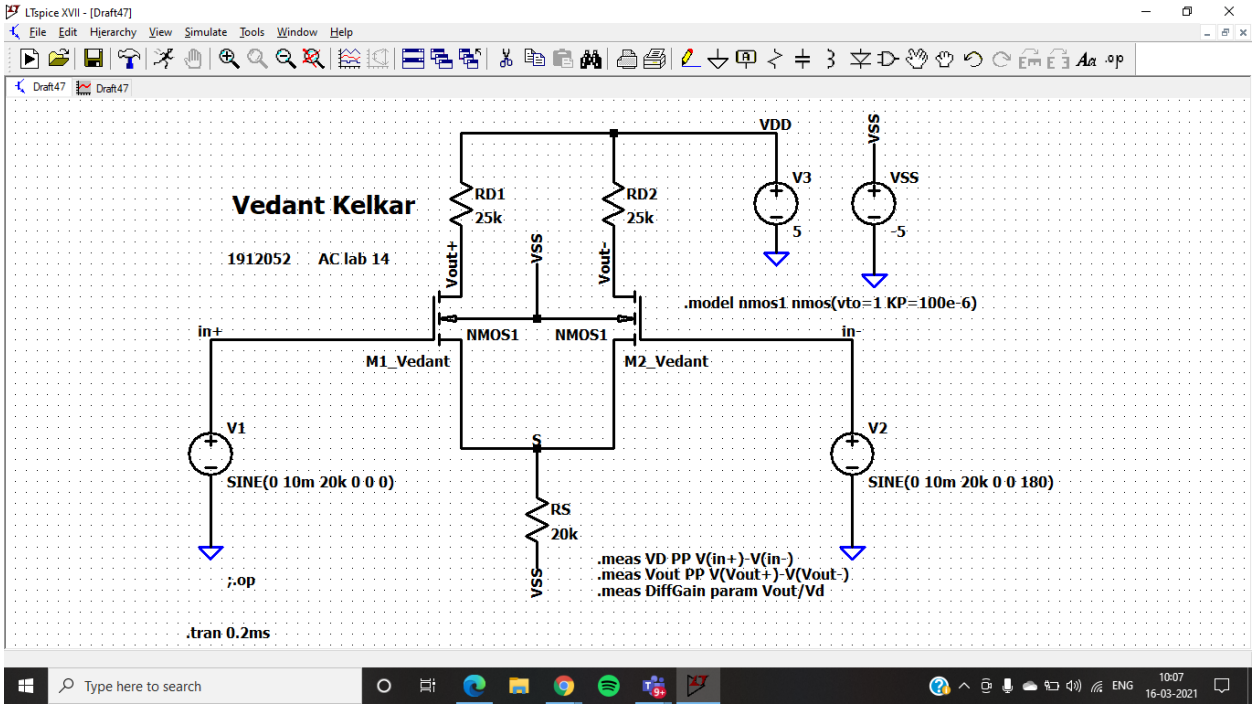




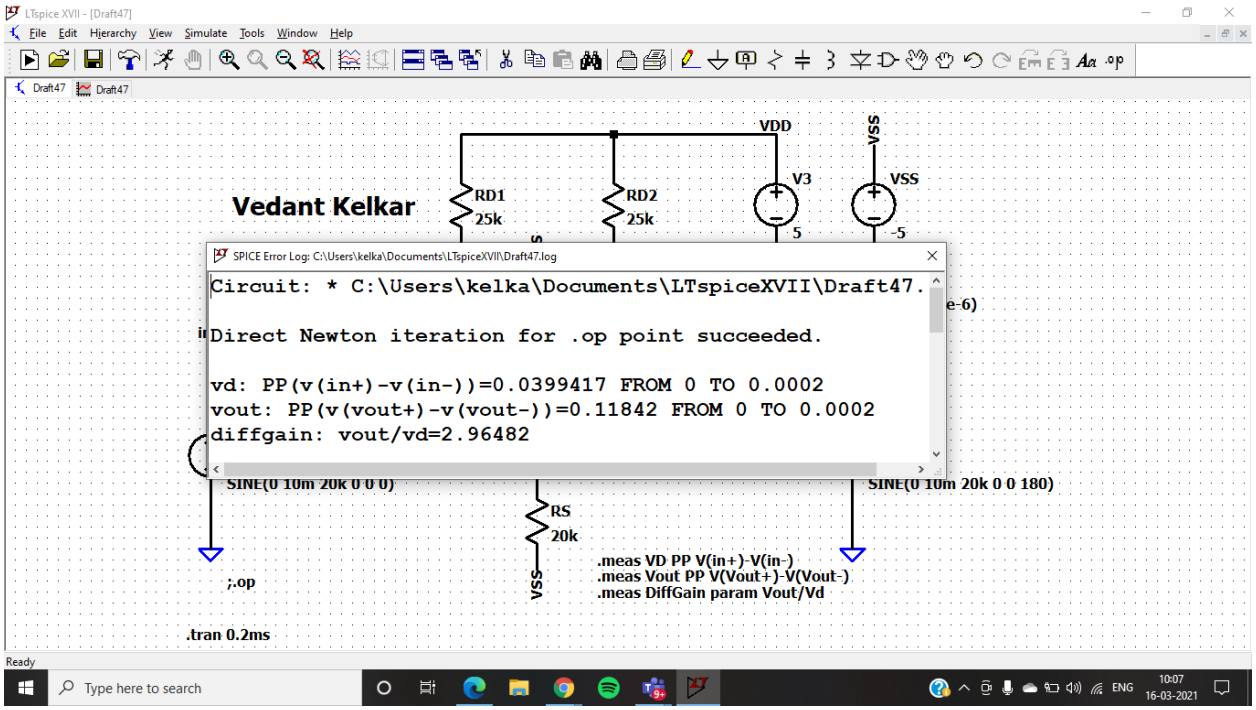
Model: nmos1 nmos1
Id: 7.03e-05 7.03e-05
Vgs: 2.19e+00 2.19e+00
Vds: 5.43e+00 5.43e+00
Vbs: -2.81e+00 -2.81e+00
Vth: 1.00e+00 1.00e+00
Vdsat: 1.19e+00 1.19e+00

Gm:	**1.19e-04**	**1.19e-04**
Gds:	**0.00e+00**	**0.00e+00**
Gmb:	**0.00e+00**	**0.00e+00**
Cbd:	**0.00e+00**	**0.00e+00**
Cbs:	**0.00e+00**	**0.00e+00**
Cgsov:	**0.00e+00**	**0.00e+00**
Cgdov:	**0.00e+00**	**0.00e+00**
Cgbov:	**0.00e+00**	**0.00e+00**
Cgs:	**0.00e+00**	**0.00e+00**
Cgd:	**0.00e+00**	**0.00e+00**
Cgb:	**0.00e+00**	**0.00e+00**



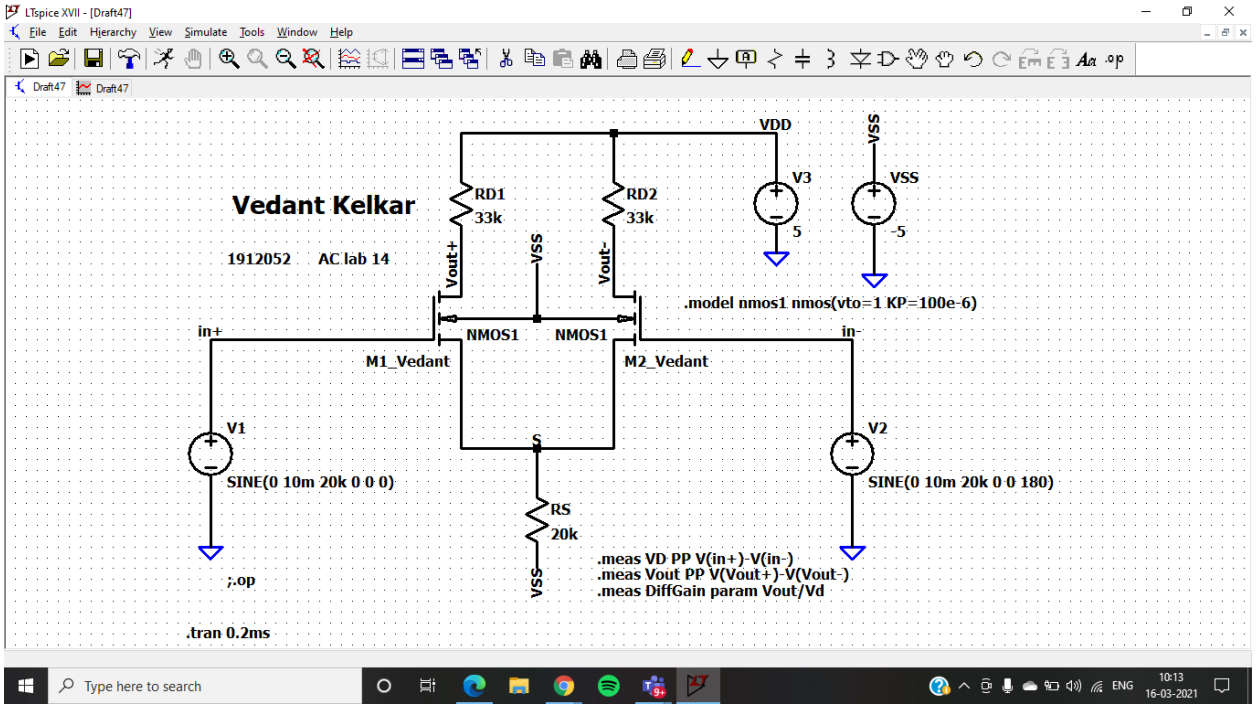


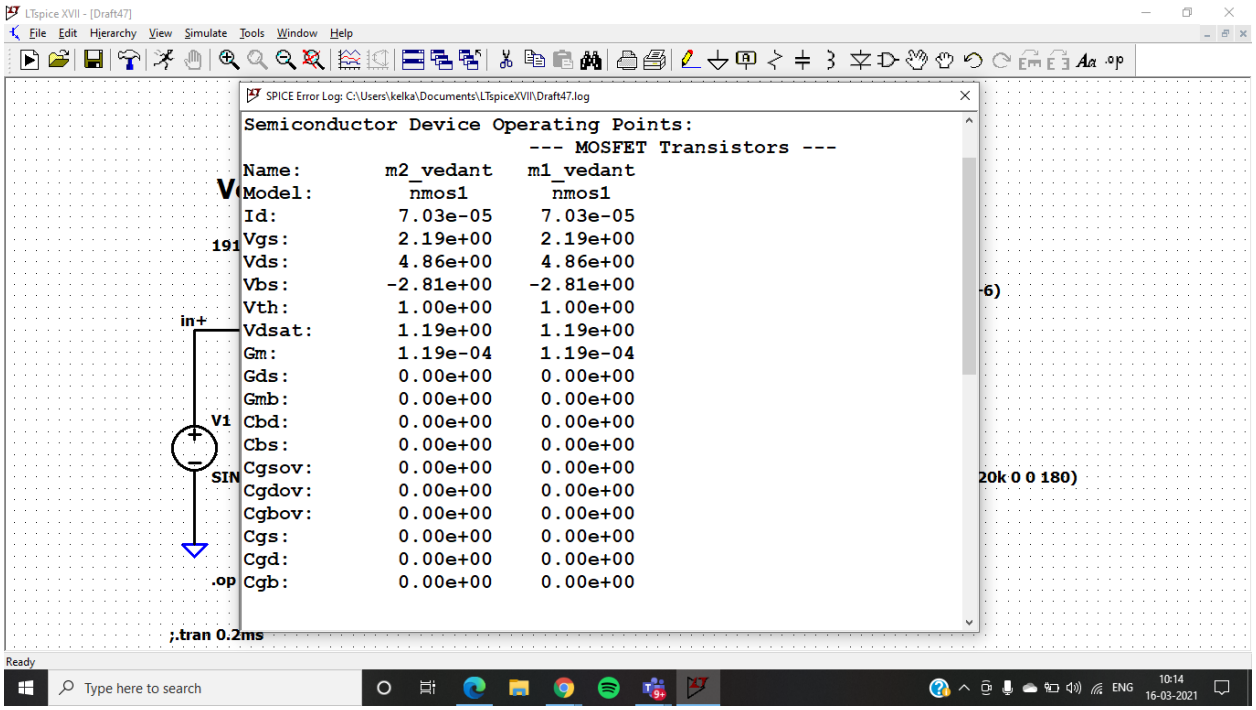
vd: PP(v(in+)-v(in-))=0.0399417 FROM 0 TO 0.0002
vout: PP(v(vout+)-v(vout-))=0.11842 FROM 0 TO 0.0002
diffgain: vout/vd=2.96482



Parameters	Calculated	Simulated
VGSQ1	2.186 V	2.19 V
IDQ1	70.33 uA	70.3 uA
gm1	0.1186 mA/V	0.119 mA/V
VGSQ2	2.186 V	2.19 V
IDQ2	70.33 uA	70.3 uA
gm2	0.1186 mA/V	0.119 mA/V
Ad	2.965	2.96482

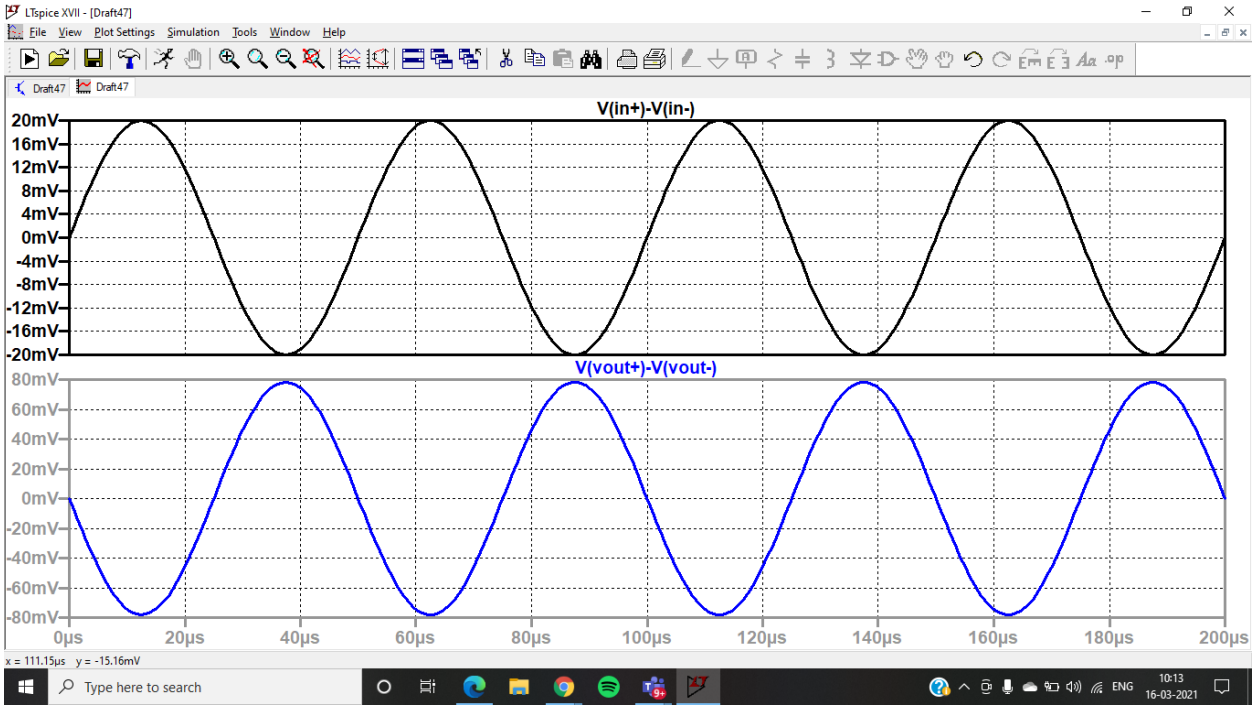
EX-1
RD1=RD2=33k

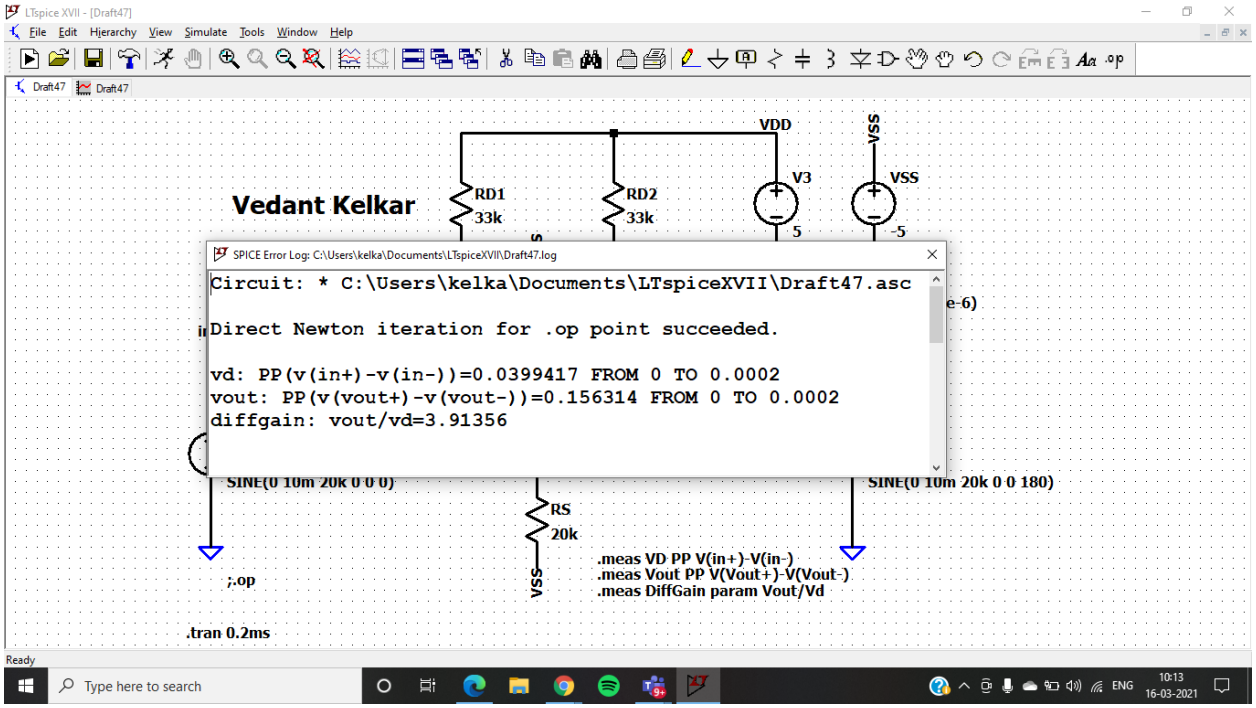




Name: m2_vedant m1_vedant
Model: nmos1 nmos1
Id: 7.03e-05 7.03e-05
Vgs: 2.19e+00 2.19e+00
Vds: 4.86e+00 4.86e+00
Vbs: -2.81e+00 -2.81e+00
Vth: 1.00e+00 1.00e+00

Vdsat:	1.19e+00	1.19e+00
Gm:	1.19e-04	1.19e-04
Gds:	0.00e+00	0.00e+00
Gmb:	0.00e+00	0.00e+00
Cbd:	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00
Cgsov:	0.00e+00	0.00e+00
Cgdov:	0.00e+00	0.00e+00
Cgbov:	0.00e+00	0.00e+00
Cgs:	0.00e+00	0.00e+00
Cgd:	0.00e+00	0.00e+00
Cgb:	0.00e+00	0.00e+00





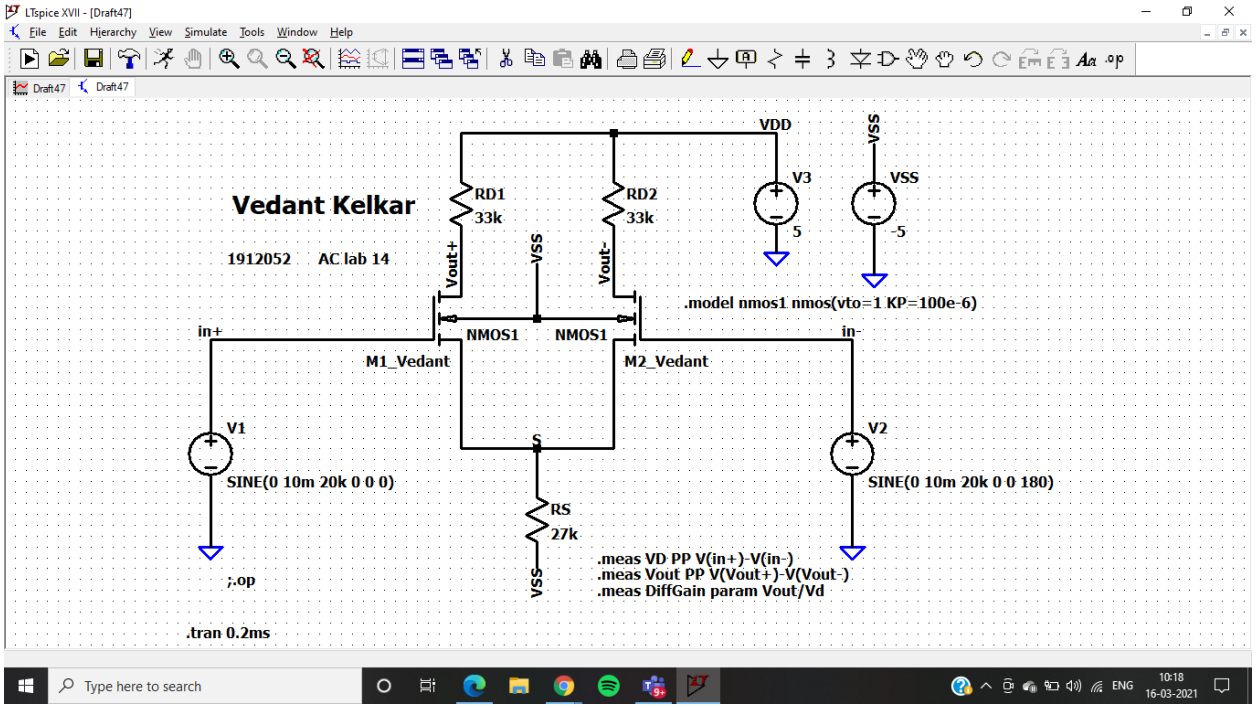
vd: PP(v(in+)-v(in-))=0.0399417 FROM 0 TO 0.0002
vout: PP(v(vout+)-v(vout-))=0.156314 FROM 0 TO 0.0002
diffgain: vout/vd=3.91356

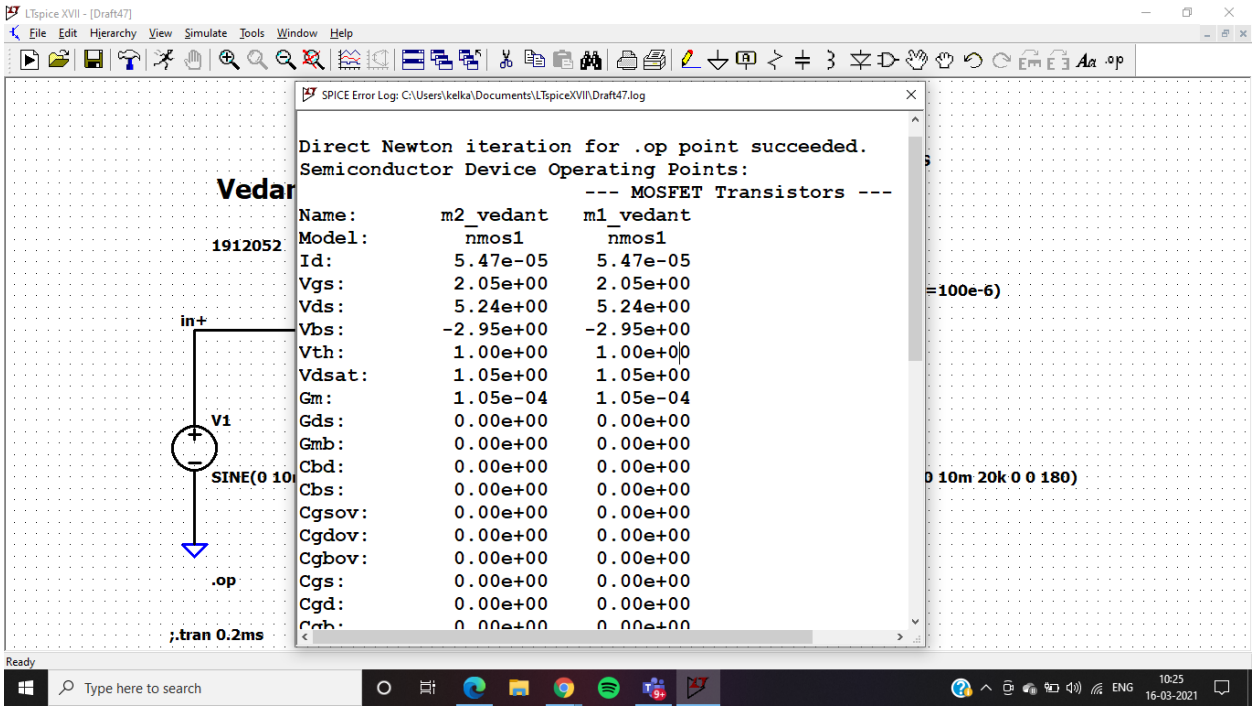
Parameters that changed:

Parameter	Rd1= Rd2 = 25k ohm	Rd1 = Rd2 = 33k ohm
Ad	2.96482	3.91356

Since value of RD increases, the gain of the amplifier also increases.

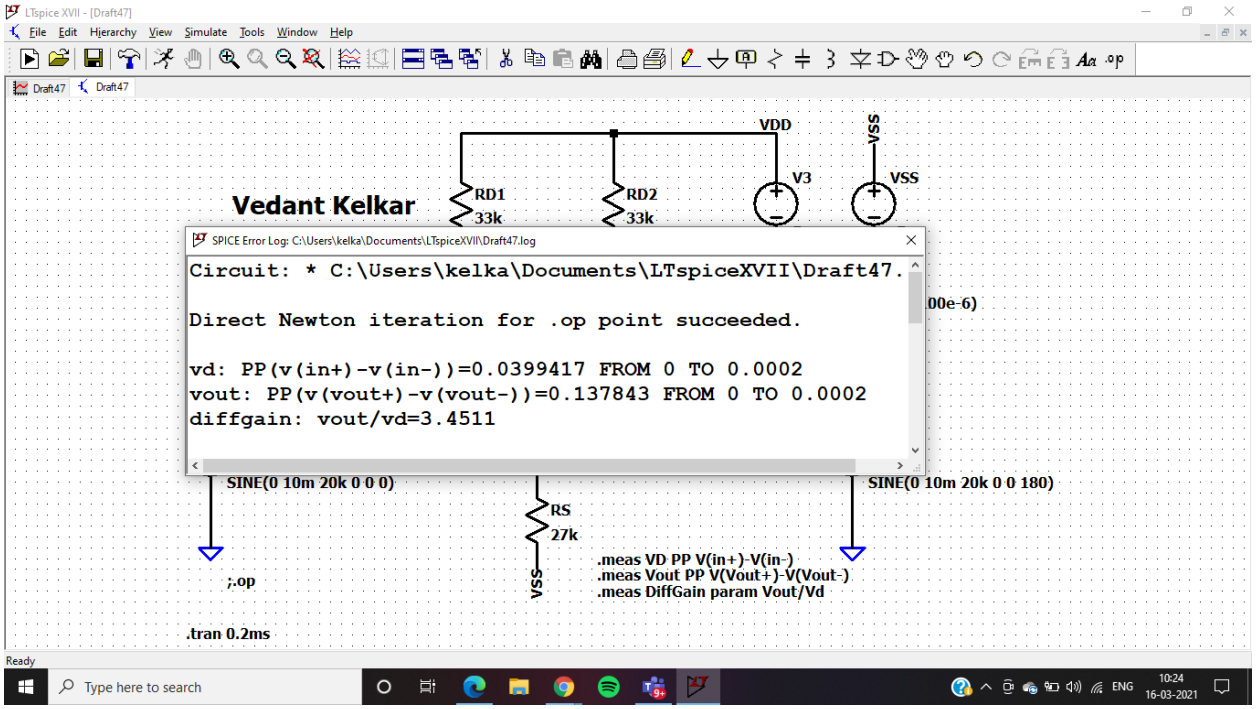
EX2
RS=27k



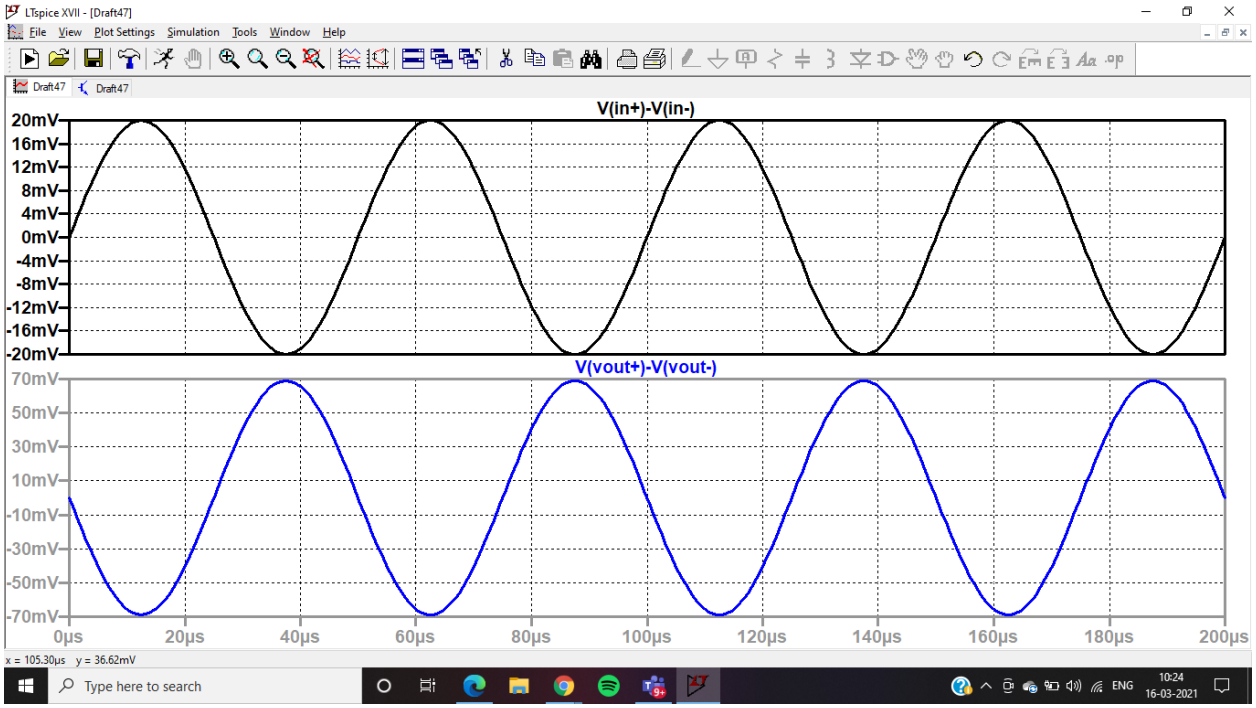


Model:	nmos1	nmos1
Id:	5.47e-05	5.47e-05
Vgs:	2.05e+00	2.05e+00
Vds:	5.24e+00	5.24e+00
Vbs:	-2.95e+00	-2.95e+00
Vth:	1.00e+00	1.00e+00
Vdsat:	1.05e+00	1.05e+00

Gm:	1.05e-04	1.05e-04
Gds:	0.00e+00	0.00e+00
Gmb:	0.00e+00	0.00e+00
Cbd:	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00
Cgsov:	0.00e+00	0.00e+00
Cgdov:	0.00e+00	0.00e+00
Cgbov:	0.00e+00	0.00e+00
Cgs:	0.00e+00	0.00e+00
Cgd:	0.00e+00	0.00e+00
Cgb:	0.00e+00	0.00e+00



vd: PP(v(in+)-v(in-))=0.0399417 FROM 0 TO 0.0002
vout: PP(v(vout+)-v(vout-))=0.137843 FROM 0 TO 0.0002
diffgain: vout/vd=3.4511



Parameters	RS1 = 25K ohm	RS1 = 20K ohm
VGSQ1	2.19 V	2.05 V
IDQ1	70.3 uA	54.7 uA
gm1	0.119 mA/V	0.105 mA/V
VGSQ2	2.19 V	2.05 V
IDQ2	70.3 uA	54.7 uA
gm2	0.119 mA/V	0.105 mA/V

Ad	2.96482	3.4511

All the DC parameters are decreased when the source resistor is decreased and the gain is increased.

Suggestions: Add inference and table
AC LAB 14 is approved with suggestions: Inderjit Singh Dhanjal