AUDIT COURSE ELECTRONIC CIRCUITS 1:
SIMULATION BASED STUDY

LAB 11

Kindly update your name and roll no, once this document is shared with you
Time slot to complete your work is **40 MINUTES**
Date: 7/9/2020
Kindly upload your schematic & waveform images here, every 10 minutes, indicating your progress and intention to completion of WORK within time slot allotted

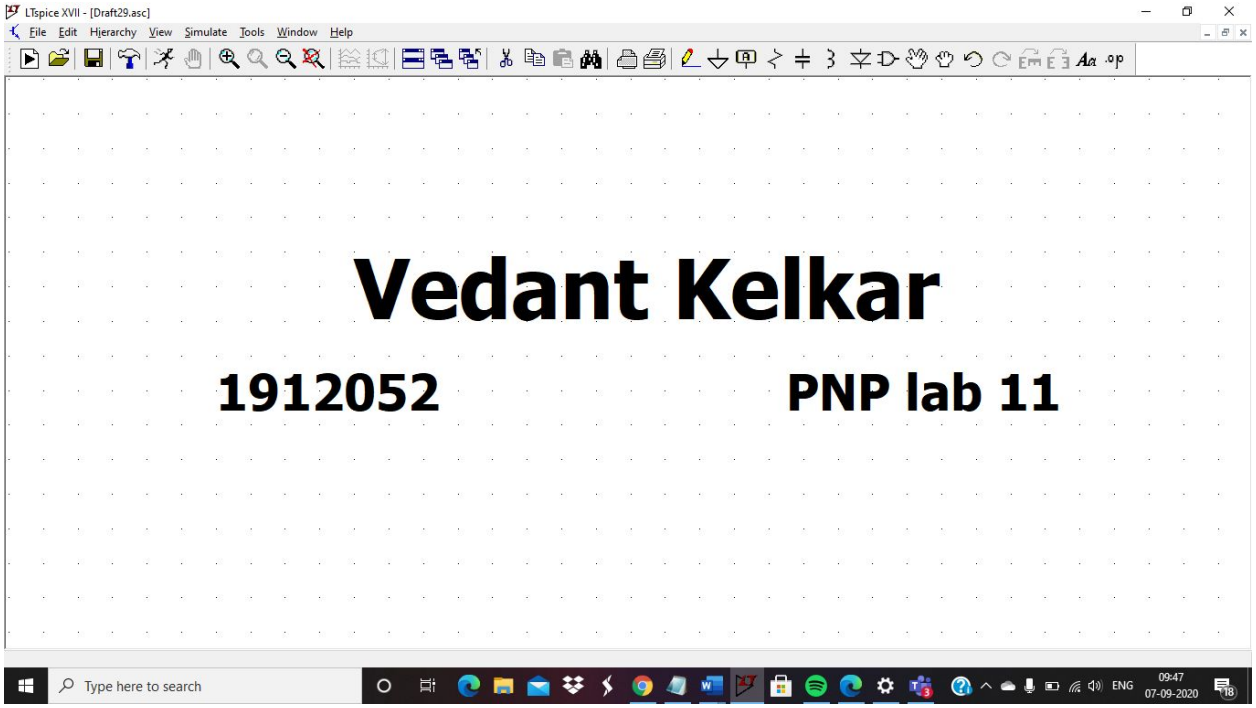
Time slot allotted to you all for the completion of WEEK 6 DAY 1 is 40 MINUTES

Kindly upload your work (only circuit schematic & waveform in LTSpice) in the shared google doc between this time slot only.

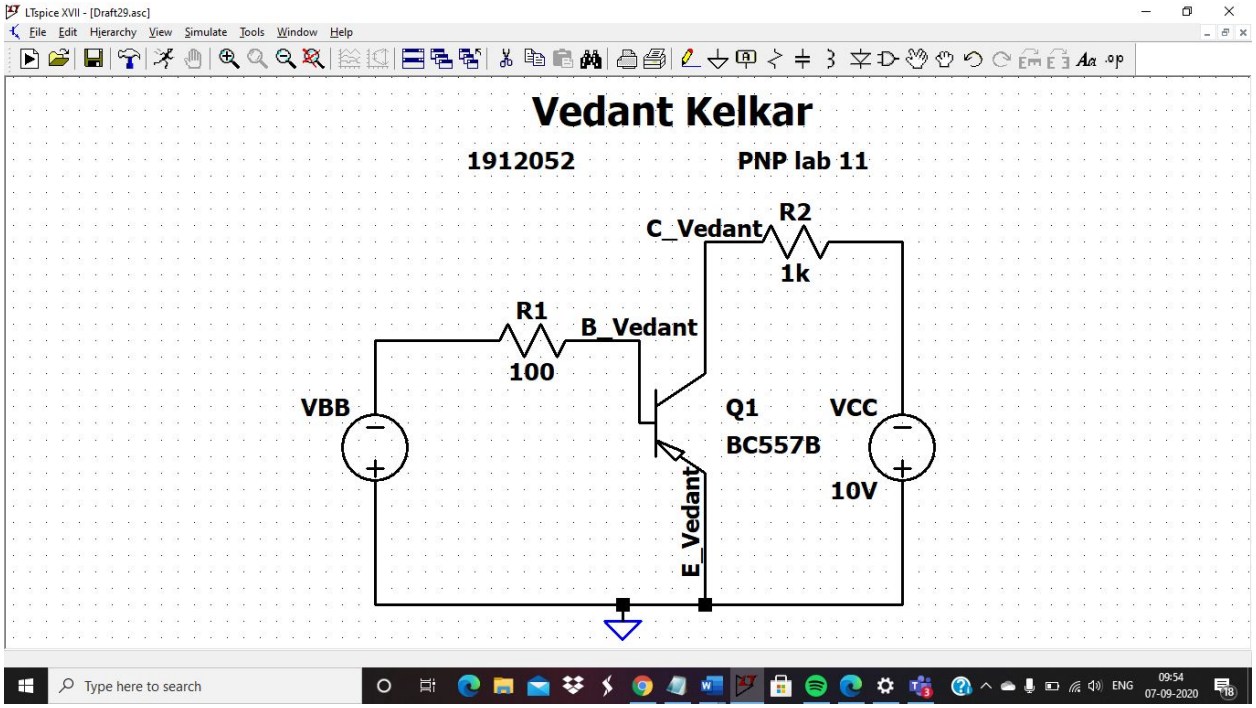
Follow these instruction strictly:
1, Start sharp ON TIME, by posting your name and roll no and **screenshot of your LT spice work screen (time and date MUST BE VISIBLE)**
2. Upload your work every 10 minutes, i.e LT spice work screen
3. This means you will upload LT spice work screen 4 times during this time slot.
4. Point 3 indicates your readiness and presences for completion of WEEK 6 DAY 1

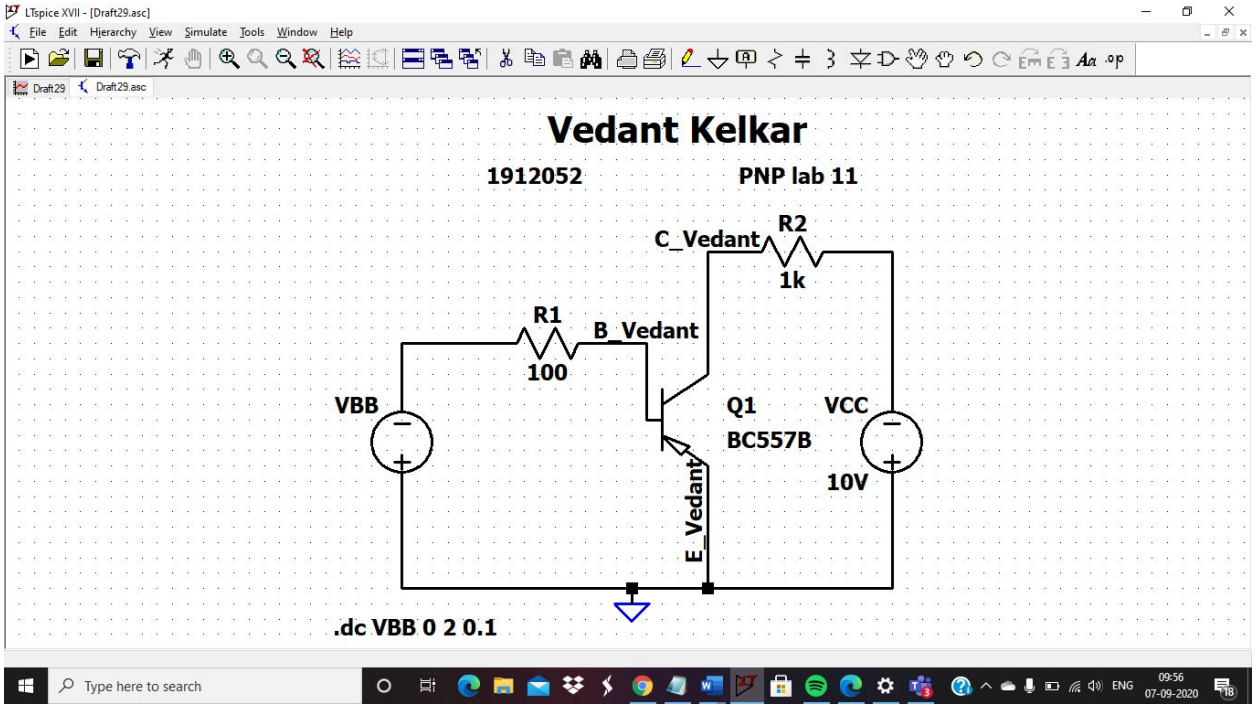
You are entitled for 1 CREDIT per Lab only if you follow above instruction to the details

STUDENTS WORK AREA STARTS HERE

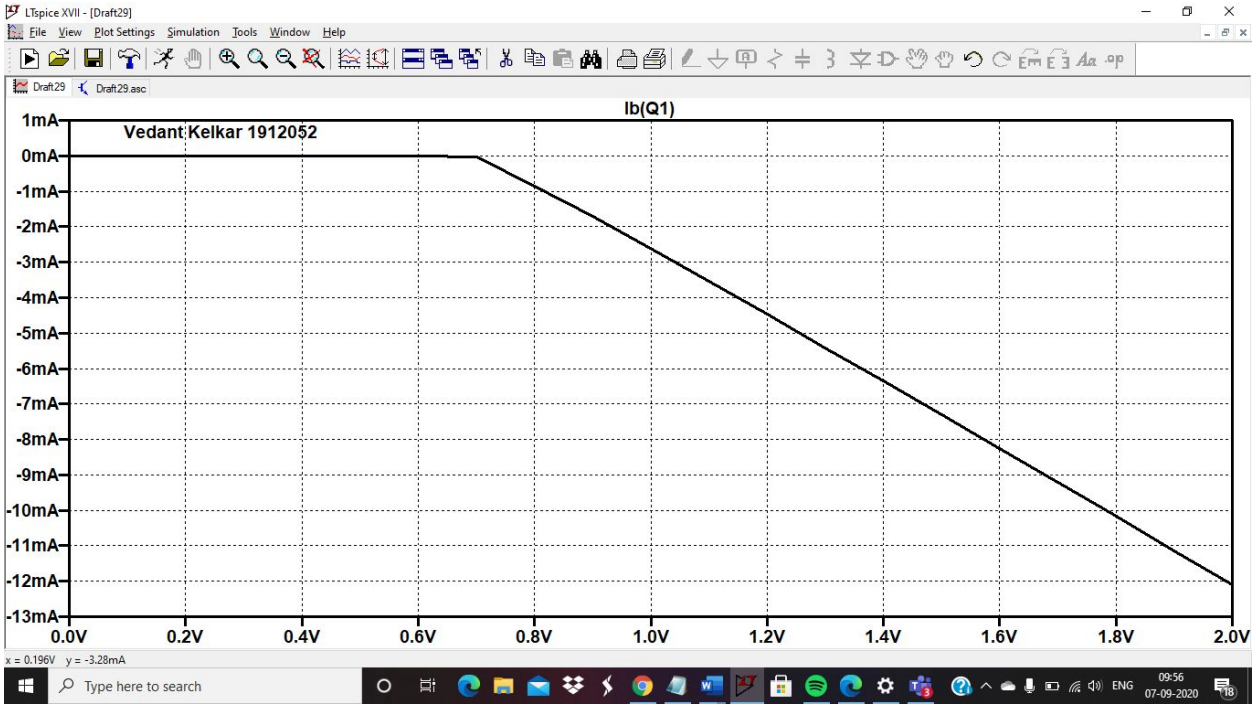


PNP INPUT CHARACTERISTICS common emitter

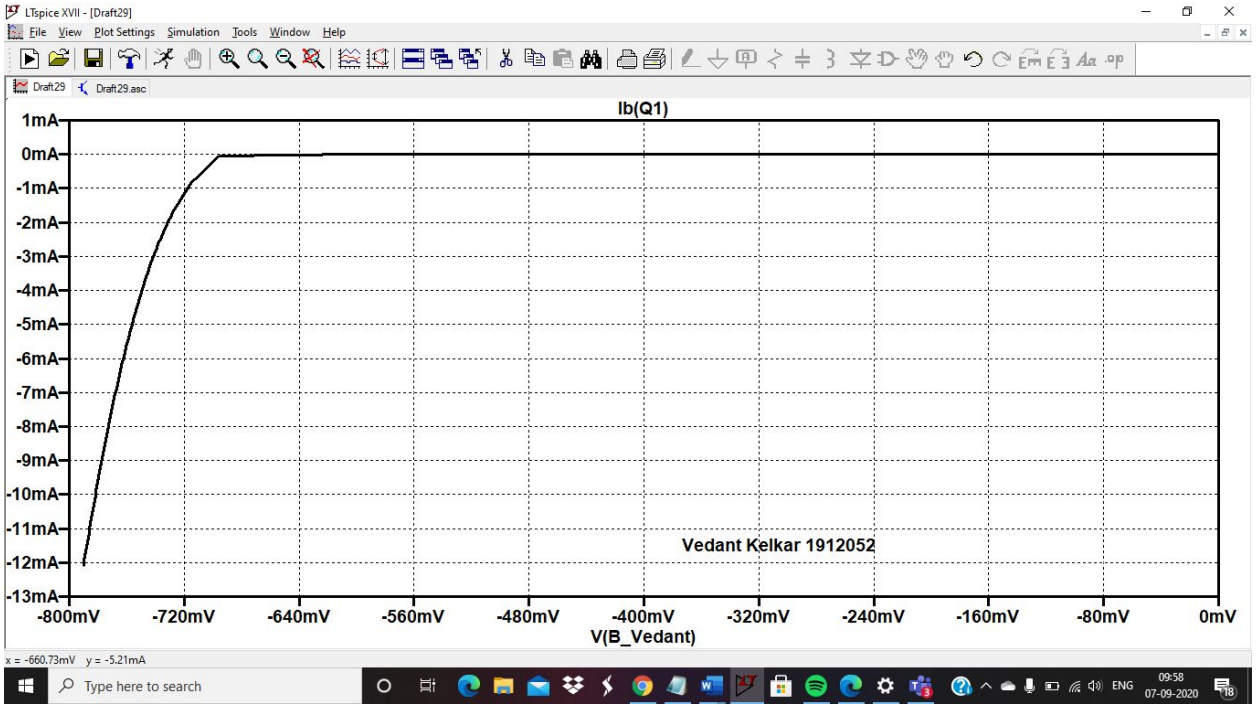



LTspice XVII - [Draft29.asc]
File Edit Hierarchy View Simulate Tools Window Help
Draft29 Draft29.asc
Vedant Kelkar
1912052
PNP lab 11
C_Vedant
R2
1k
R1
100
B_Vedant
VBB
Q1
BC557B
VCC
10V
E_Vedant
.dc VBB 0 2 0.1
Type here to search
ENG
09:56
07-09-2020

VBB vs Ib

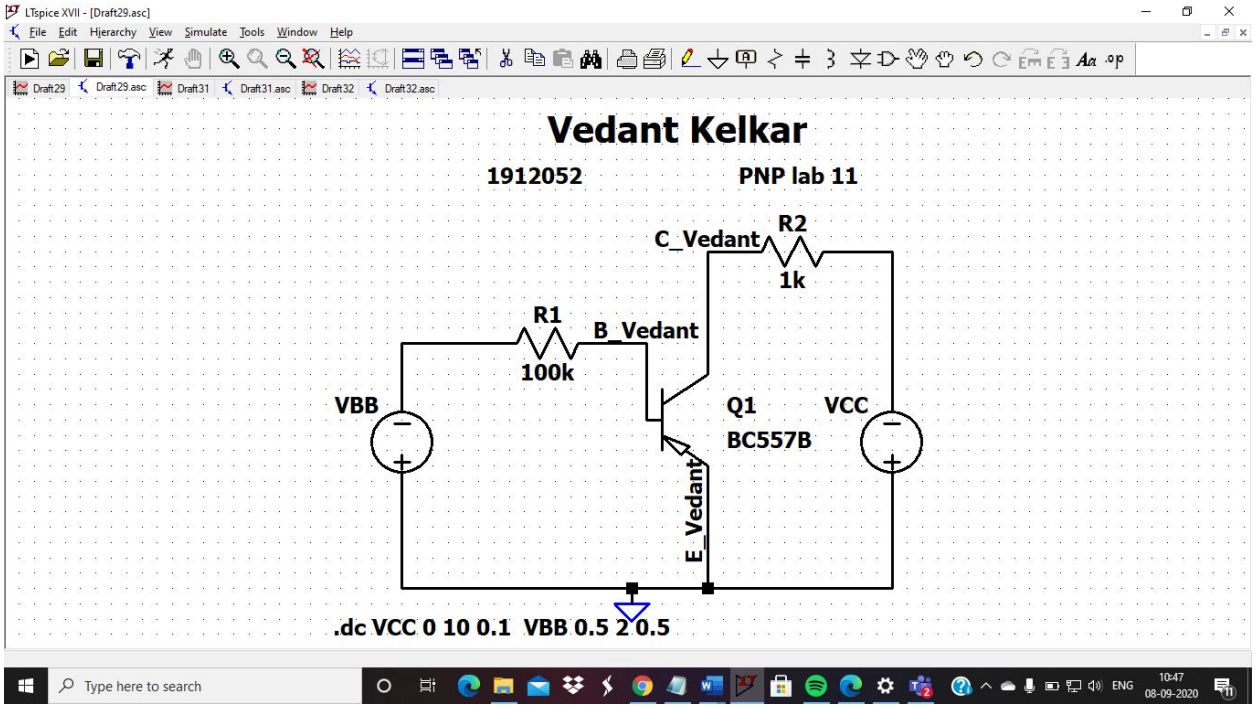

LTspice XVII - [Draft29]
File View Plot Settings Simulation Tools Window Help
Draft29 Draft29.asc
Ib(Q1)
Vedant Kelkar 1912052
1mA
0mA
-1mA
-2mA
-3mA
-4mA
-5mA
-6mA
-7mA
-8mA
-9mA
-10mA
-11mA
-12mA
-13mA
0.0V
0.2V
0.4V
0.6V
0.8V
1.0V
1.2V
1.4V
1.6V
1.8V
2.0V
x = 0.196V y = -3.28mA
Type here to search
ENG
09:56
07-09-2020

VB vs Ib

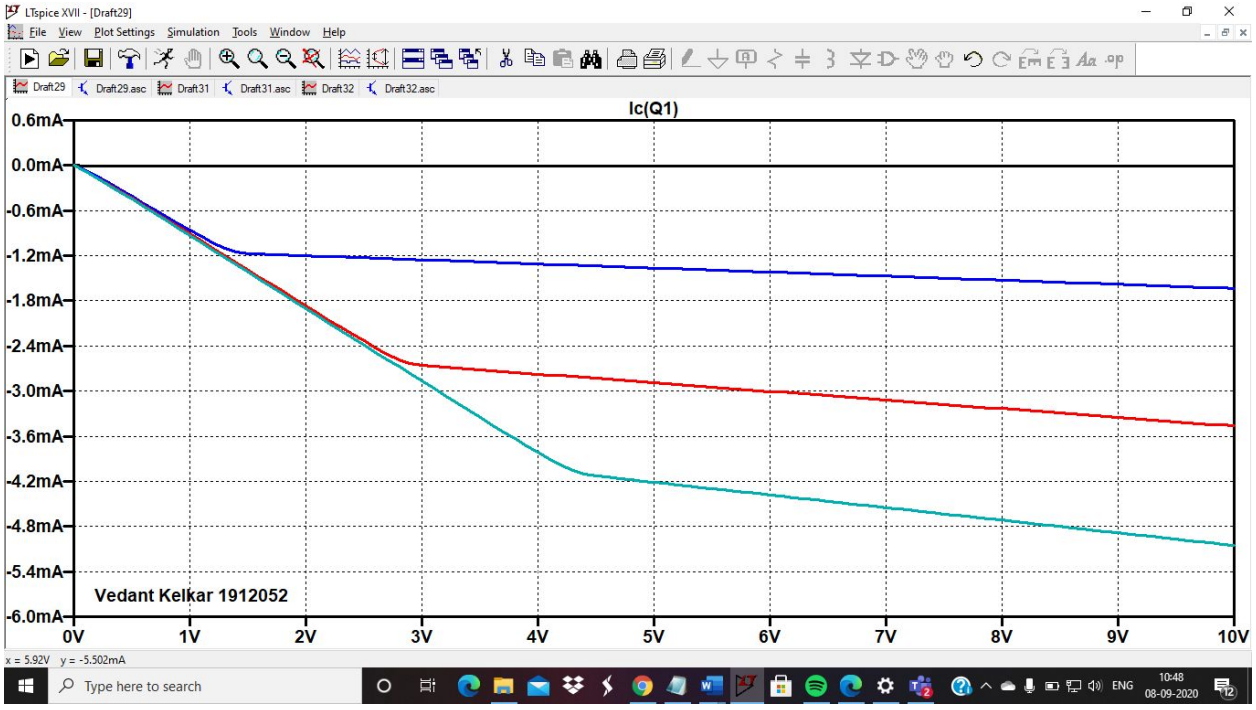


VB	IB
0	0
200mV	7.6202 pA
400mV	-878.312 pA
500mV	-37.31 nA
580mV	634.77 nA
600mV	-1.223 uA
620mV	2.488 uA
640mV	-5.401 uA

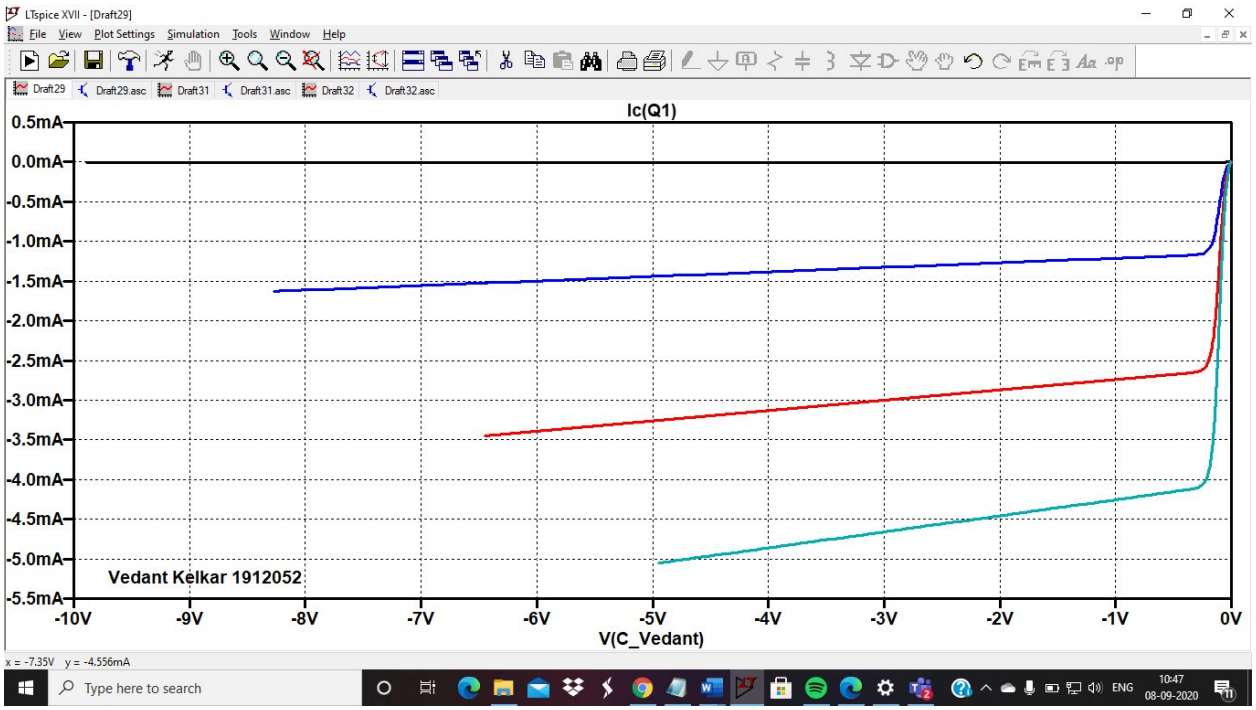
PNP OUTPUT CHARACTERISTICS common emitter


LTspice XVII - [Draft29.asc]
File Edit Hierarchy View Simulate Tools Window Help
Draft29 Draft29.asc Draft31 Draft31.asc Draft32 Draft32.asc
Vedant Kelkar
1912052
PNP lab 11
C_Vedant
R2
1k
R1
100k
B_Vedant
VBB
Q1
BC557B
VCC
E_Vedant
.dc VCC 0 10 0.1 VBB 0.5 2 0.5
Type here to search
ENG
10:47
08-09-2020

VCC vs Ic


LTspice XVII - [Draft29]
File View Plot Settings Simulation Tools Window Help
Draft29 Draft29.asc Draft31 Draft31.asc Draft32 Draft32.asc
Ic(Q1)
0.6mA
0.0mA
-0.6mA
-1.2mA
-1.8mA
-2.4mA
-3.0mA
-3.6mA
-4.2mA
-4.8mA
-5.4mA
-6.0mA
Vedant Kelkar 1912052
0V
1V
2V
3V
4V
5V
6V
7V
8V
9V
10V
x = 5.92V y = -5.502mA
Type here to search
ENG
10:48
08-09-2020

VEC vs Ic



Vec	Ic
0	0
100mV	-0.518mA
200mV	-1.122mA
300mV	-1.157mA
500mV	-1.179mA
1V	-1.224mA
3V	-1.313mA
5V	-1,452mA
8V	-1.617mA

I HAVE MADE THE SUGGESTED CHANGES

Suggestions: Mention which characteristics and which configurations for above printscreens:

AC LAB 11 is approved with suggestions: Inderjit SIngh Dhanjal