## AUDIT COURSE ELECTRONIC CIRCUITS 1: SIMULATION BASED STUDY

## **LAB 16**

Kindly update your name and roll no, once this document is shared with you Time slot to complete your work is **40 MINUTES** 

Date: 29/9/2020

Kindly upload your schematic & waveform images here, every 10 minutes, indicating your progress and intention to completion of WORK within time slot allotted

Time slot allotted to you all for the completion of WEEK 8 DAY 2 is 40 MINUTES

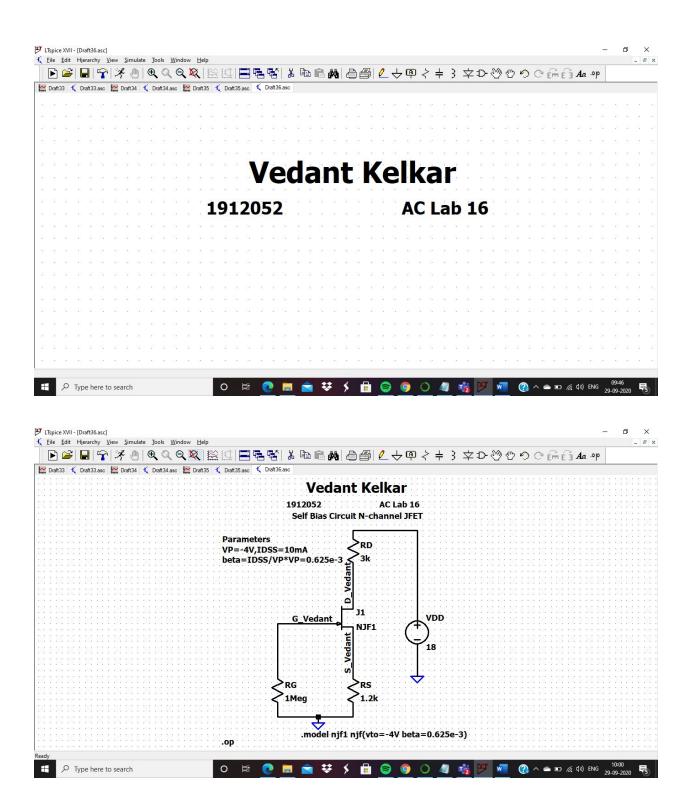
Kindly upload your work (only circuit schematic & waveform in LTSpice) in the shared google doc between this time slot only.

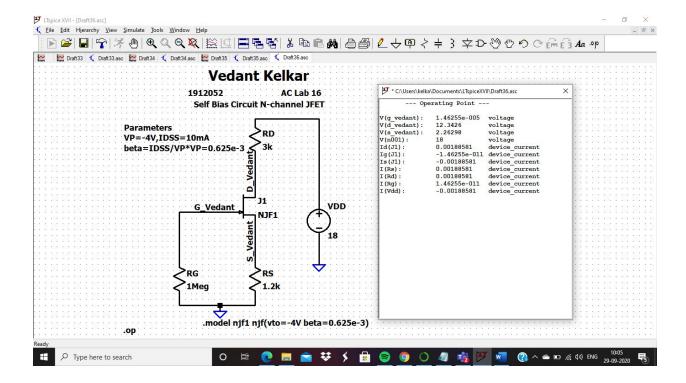
## Follow these instruction strictly:

- 1, Start sharp ON TIME, by posting your name and roll no and screenshot of your LT spice work screen (time and date MUST BE VISIBLE)
- 2. Upload your work every 10 minutes, i.e LT spice work screen
- 3. This means you will upload LT spice work screen 4 times during this time slot.
- 4. Point 3 indicates your readiness and presences for completion of WEEK 8 DAY 2

You are entitled for 1 CREDIT per Lab only if you follow above instruction to the details

STUDENTS WORK AREA STARTS HERE





V(g\_vedant): 1.46255e-005 voltage V(d\_vedant): 12.3426 voltage V(s\_vedant): 2.26298 voltage

**V(n001):** 18 voltage

Id(J1): 0.00188581 device current

**Ig(J1):** -1.46255e-011 device current

Is(J1): -0.00188581 device\_current I(Rs): 0.00188581 device\_current I(Rd): 0.00188581 device\_current I(Rg): 1.46255e-011 device current

I(Vdd): -0.00188581 device current

TFET Biasing.

Vedant Kelkar. 1912052 B2

VG=IGRG

Va=0 :: Ia=0.

due to Reverse bias.

VS= IO. RS (IO~IS)

Vs= To (1200)

Vas = Va-Vs

= -Ip(1200) (D)

Drain corrent ID

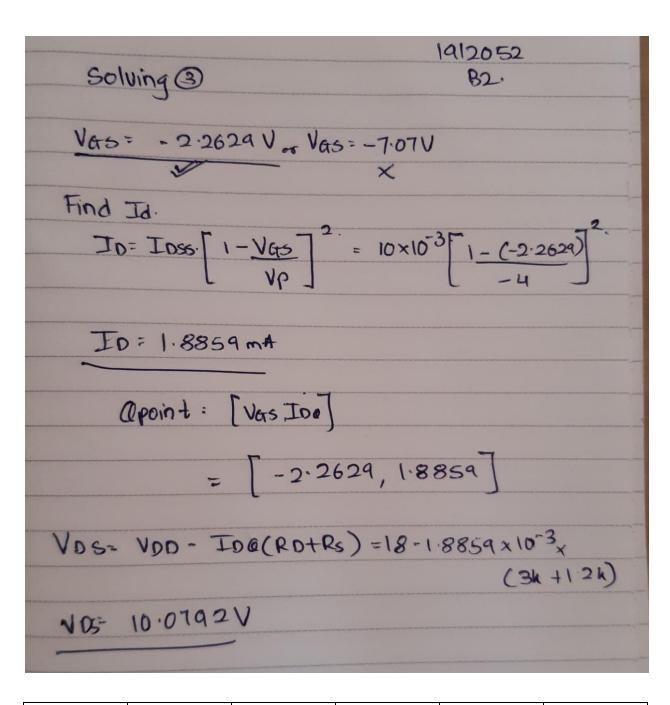
ID: IOSS 1- Vas = 10×10 3x 1× Vas 2 -0

from O & @

Vas = -1200 × 10 × 10-3 [ 1+ Vas + Vas2 2 16 -

Vas = -12 [1+0.5 Vas + 0.0625 Vas2]

VGS= -12-6VGS-0.75 VGS2 0.75 VG52 + 7VG5 +12=0 (3)



IDQ calc	IDQ sim	VGSQ calc	VGSQ sim	VDSQ calc	VDSQ sim
0.0018859A	0.00188581A	- 2.2629V	- 2.26298V	10.0792V	10.0797V