Audit Course Session 12

AUDIT COURSE
ELECTRONIC CIRCUITS 2: SIMULATION BASED STUDY

Kindly update your name and roll no, once this document is shared with you
Time slot to complete your work is **40 MINUTES**
Date: 1/3/2021
Kindly upload your schematic & waveform images here, every 10 minutes, indicating your progress and intention to completion of WORK within time slot allotted

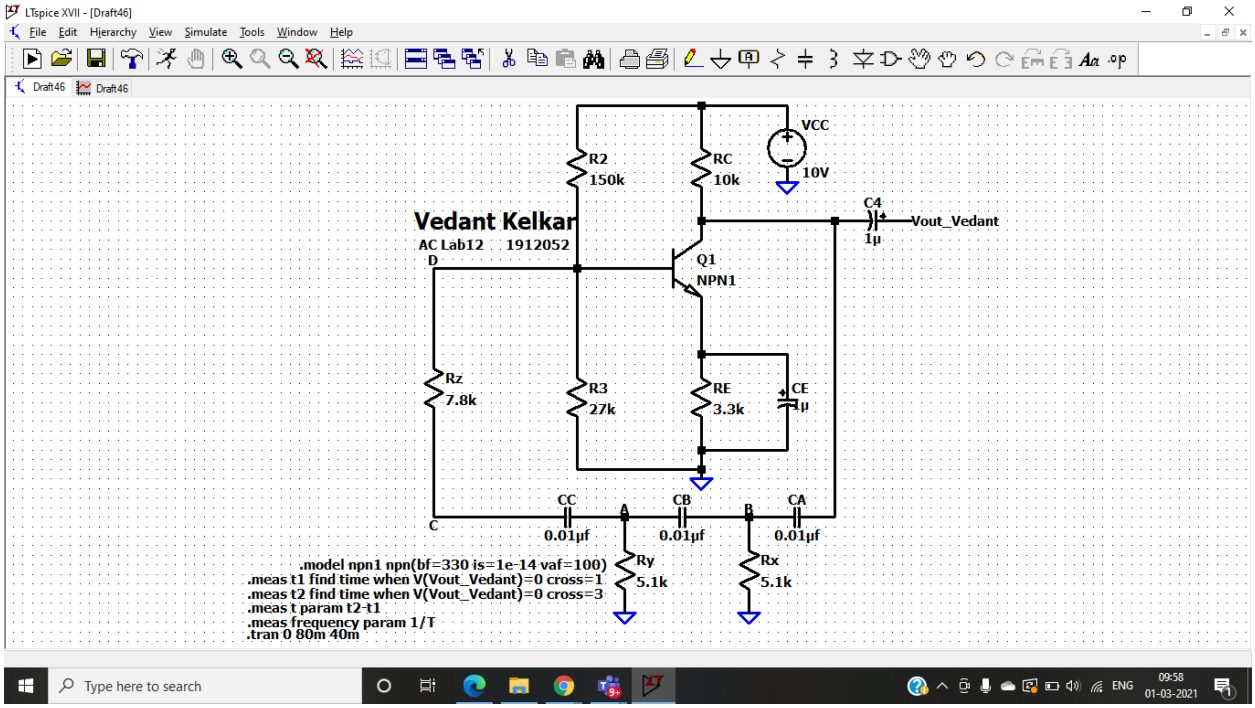
Time slot allotted to you all for the completion of Session 12 is 40 MINUTES

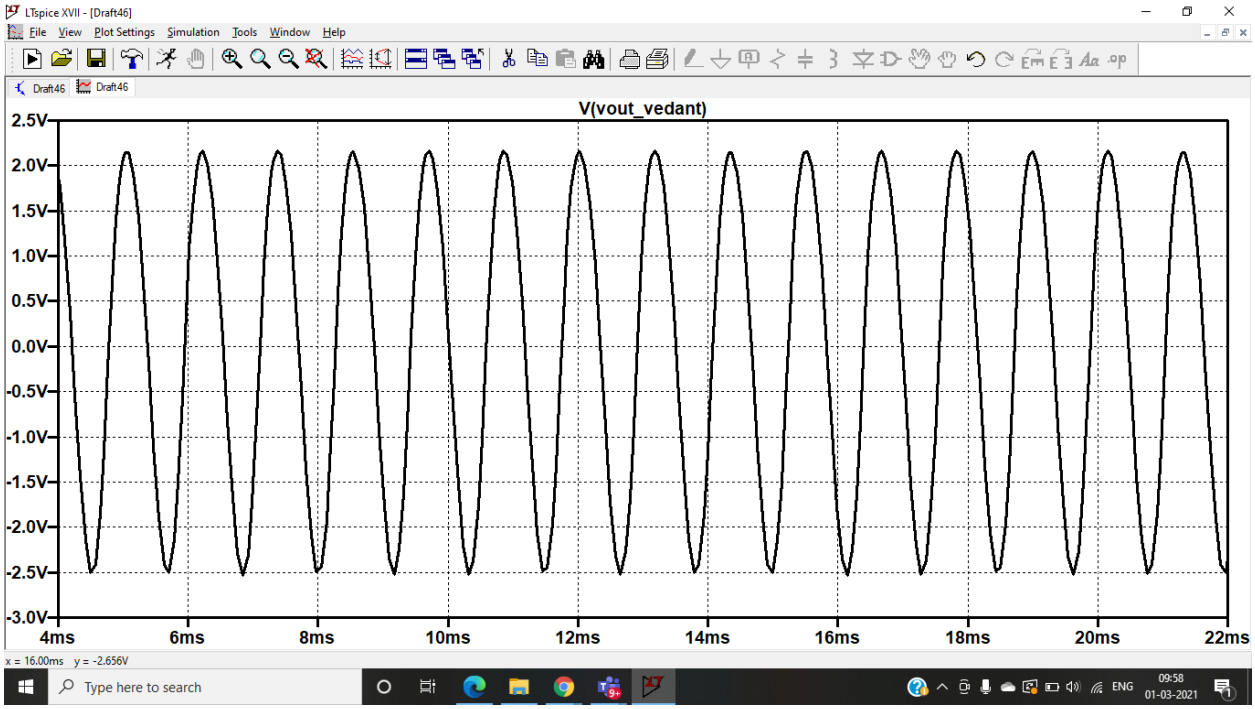
Kindly upload your work (only circuit schematic & waveform in LTSpice) in the shared google doc between this time slot only.

Follow these instruction strictly:
1, Start sharp ON TIME, by posting your name and roll no and **screenshot of your LT spice work screen (time and date MUST BE VISIBLE)**
2. Upload your work every 10 minutes, i.e LT spice work screen
3. This means you will upload LT spice work screen 4 times during this time slot.
4. Point 3 indicates your readiness and presences for completion of Session 12

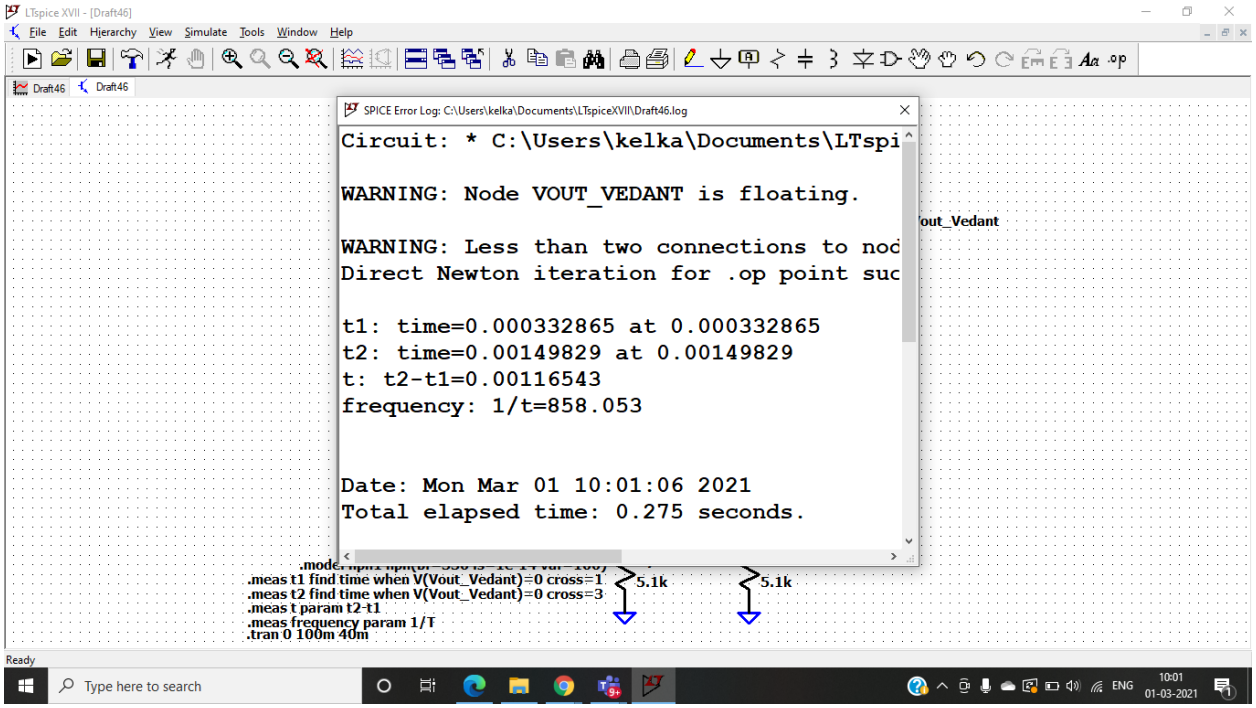
You are entitled for 10 points per session only if you follow above instruction to the details

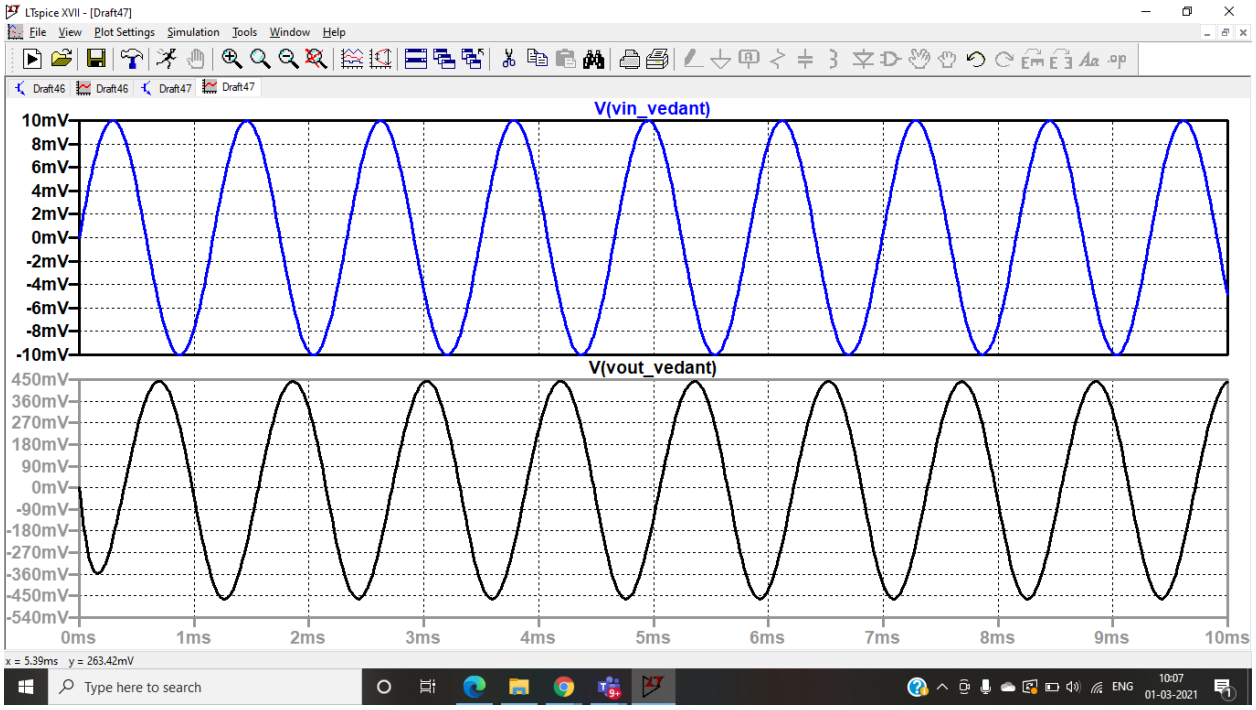
STUDENTS WORK AREA STARTS HERE


LTspice XVII - [Draft46]
File Edit Hierarchy View Simulate Tools Window Help
Draft46 Draft46
VCC
10V
R2
150k
RC
10k
C4
1µ
Vout_Vedant
Vedant Kelkar
AC Lab12 1912052
D
Q1
NPN1
Rz
7.8k
R3
27k
RE
3.3k
CE
1µ
CC
0.01µf
CB
0.01µf
CA
0.01µf
C
A
B
Ry
5.1k
Rx
5.1k
.model npn1 npn(bf=330 is=1e-14 vaf=100)
.meas t1 find time when V(Vout_Vedant)=0 cross=1
.meas t2 find time when V(Vout_Vedant)=0 cross=3
.meas t param t2-t1
.meas frequency param 1/T
.tran 0 80m 40m
Type here to search
ENG
09:58
01-03-2021


LTspice XVII - [Draft46]
File View Plot Settings Simulation Tools Window Help
Draft46 Draft46
V(vout_vedant)
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
-0.5V
-1.0V
-1.5V
-2.0V
-2.5V
-3.0V
4ms
6ms
8ms
10ms
12ms
14ms
16ms
18ms
20ms
22ms
x = 16.00ms y = -2.656V
Type here to search
ENG
09:58
01-03-2021

100m

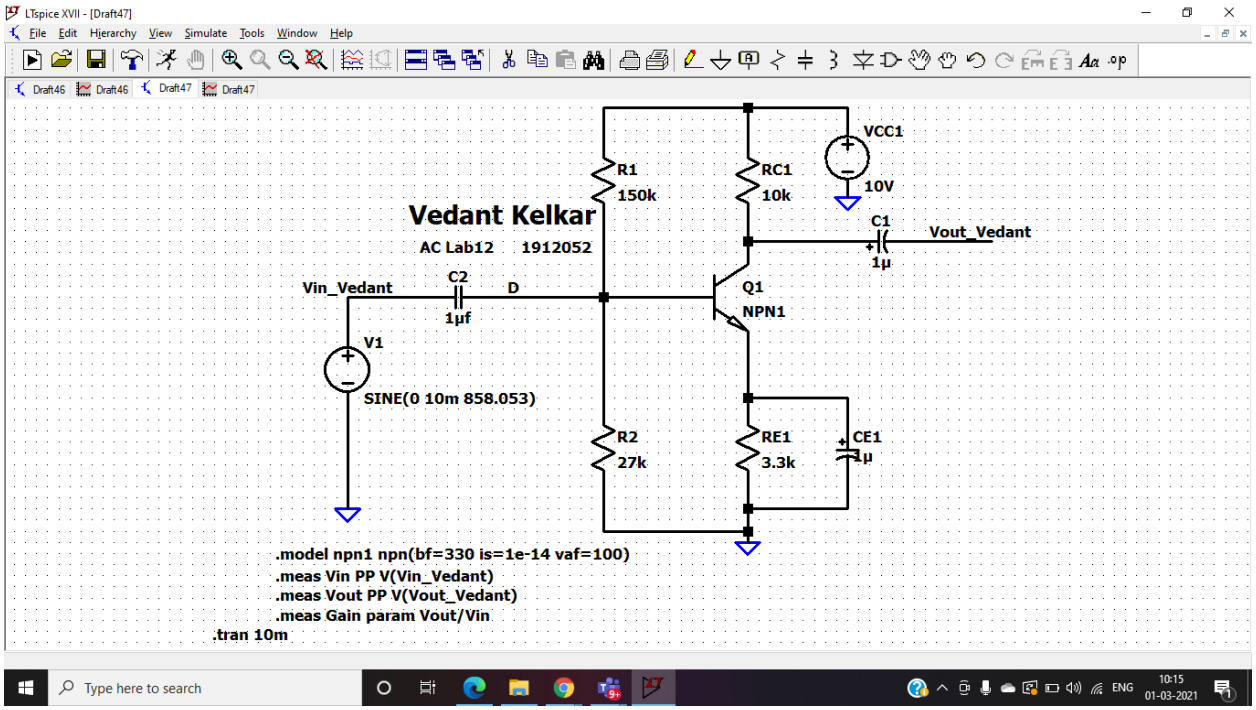


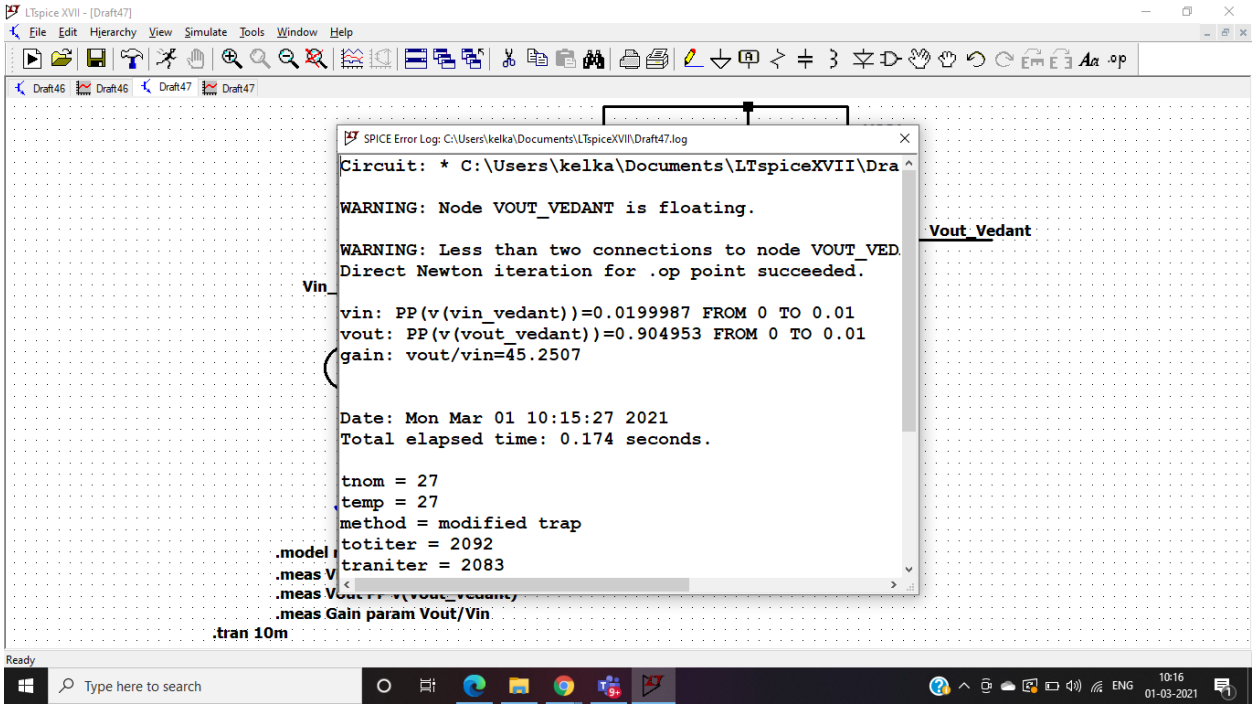


Parameters	Calculated	Simulated

fo	838.748 Hz	858.053Hz
A.K	Less than 1 (at the start)	44.4867 * 0.0675263 = 3

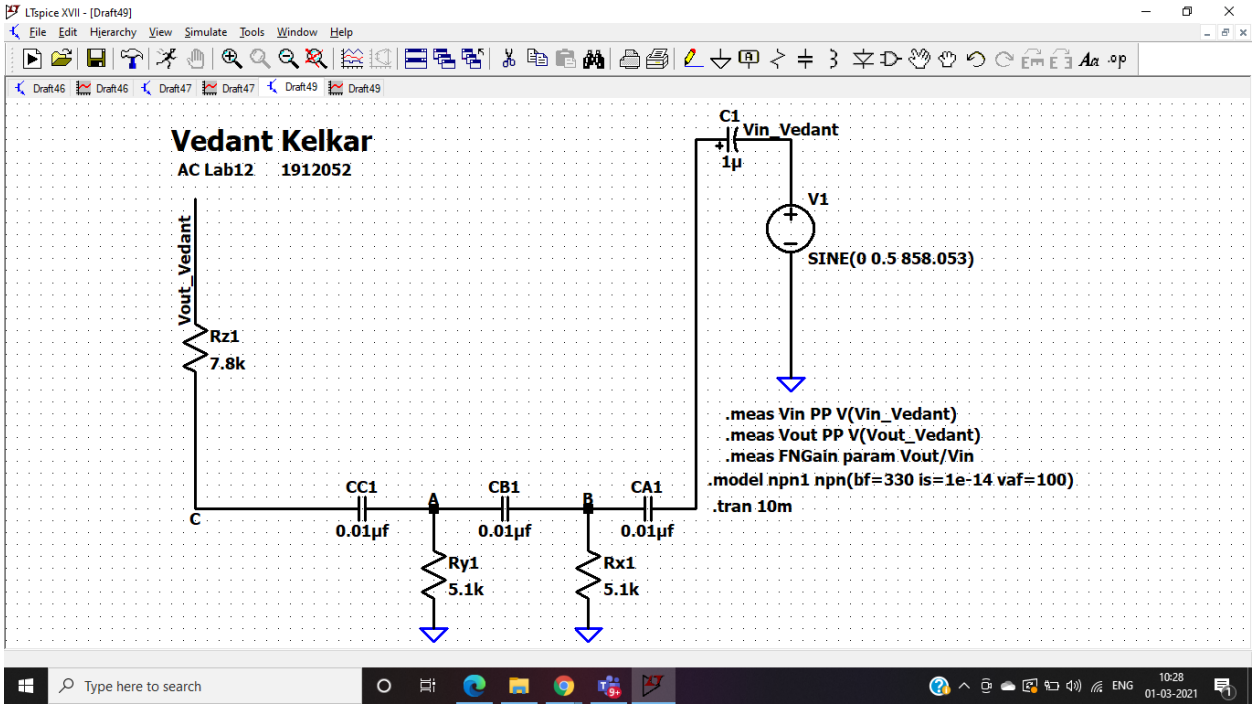
Amplifier Gain

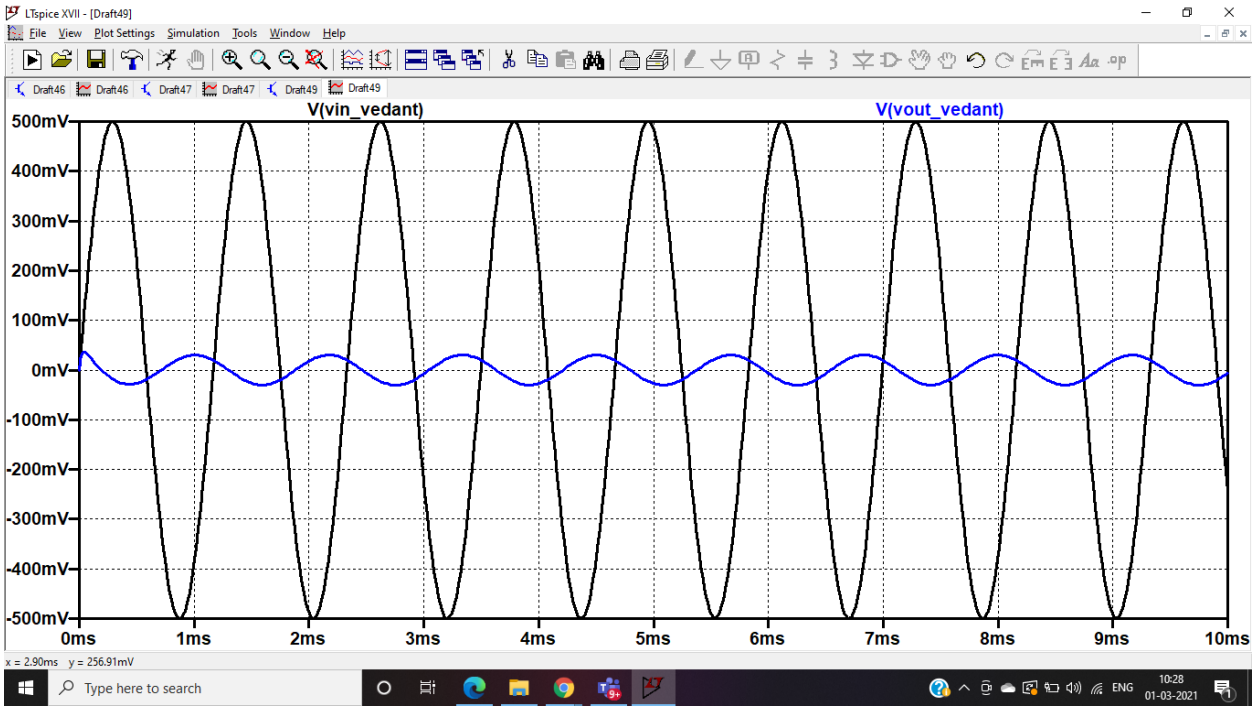


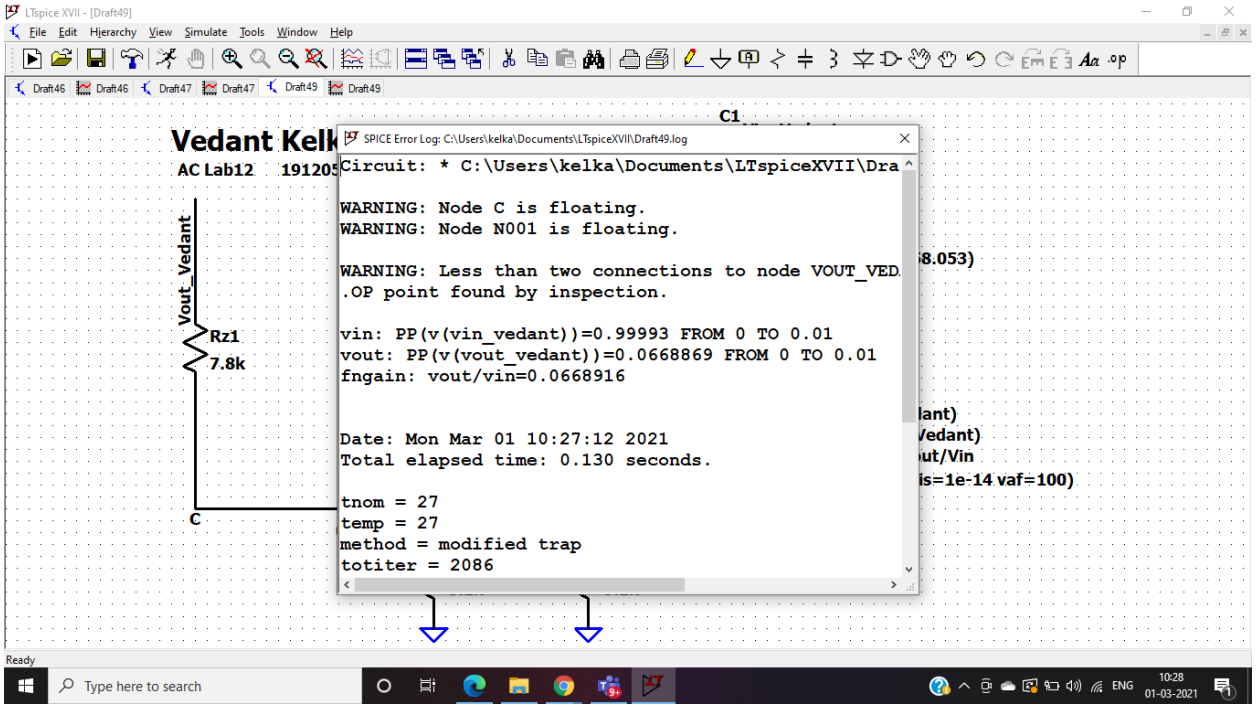


Parameter	Simulated
A (amplifier gain)	45.2507

Feedback

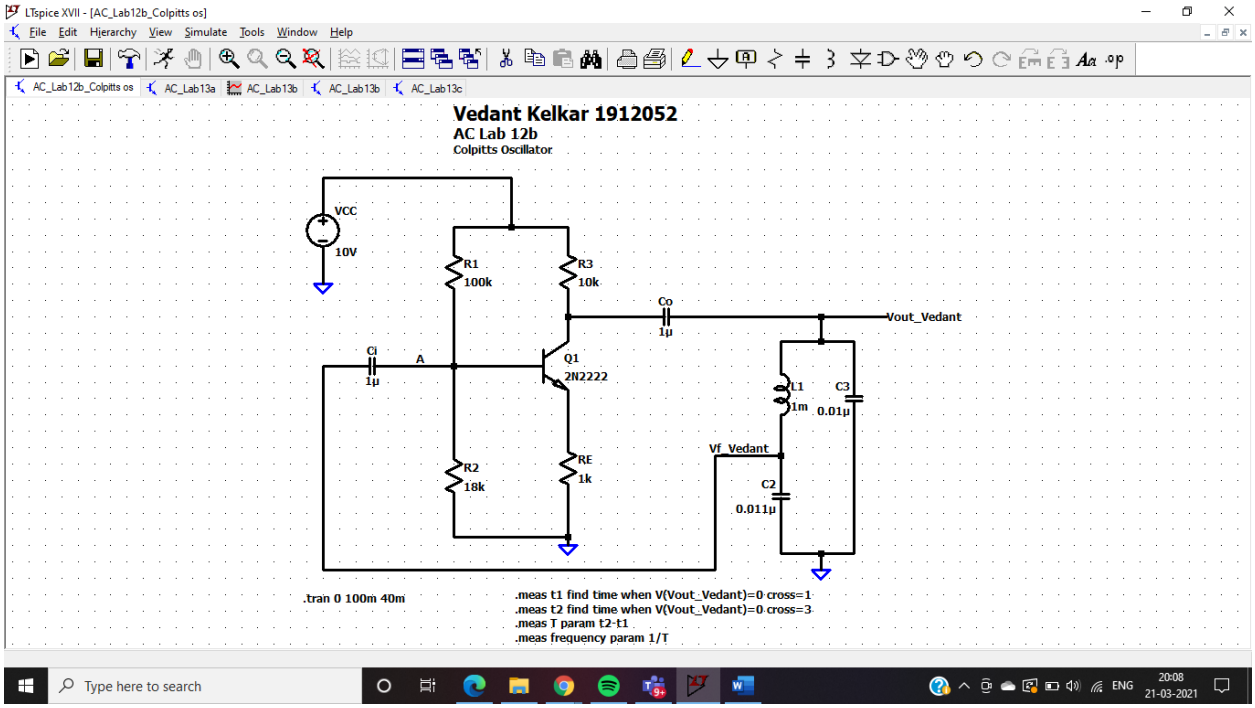

LTspice XVII - [Draft49]
File Edit Hierarchy View Simulate Tools Window Help
Draft46 Draft46 Draft47 Draft47 Draft49 Draft49
Vedant Kelkar
AC Lab12 1912052
C1
Vin_Vedant
1µ
V1
SINE(0 0.5 858.053)
Vout_Vedant
Rz1
7.8k
.meas Vin PP V(Vin_Vedant)
.meas Vout PP V(Vout_Vedant)
.meas FNGain param Vout/Vin
.model npn1 npn(bf=330 is=1e-14 vaf=100)
.tran 10m
CC1
0.01µf
CB1
0.01µf
CA1
0.01µf
A
B
C
Ry1
5.1k
Rx1
5.1k
Type here to search
ENG
10:28
01-03-2021

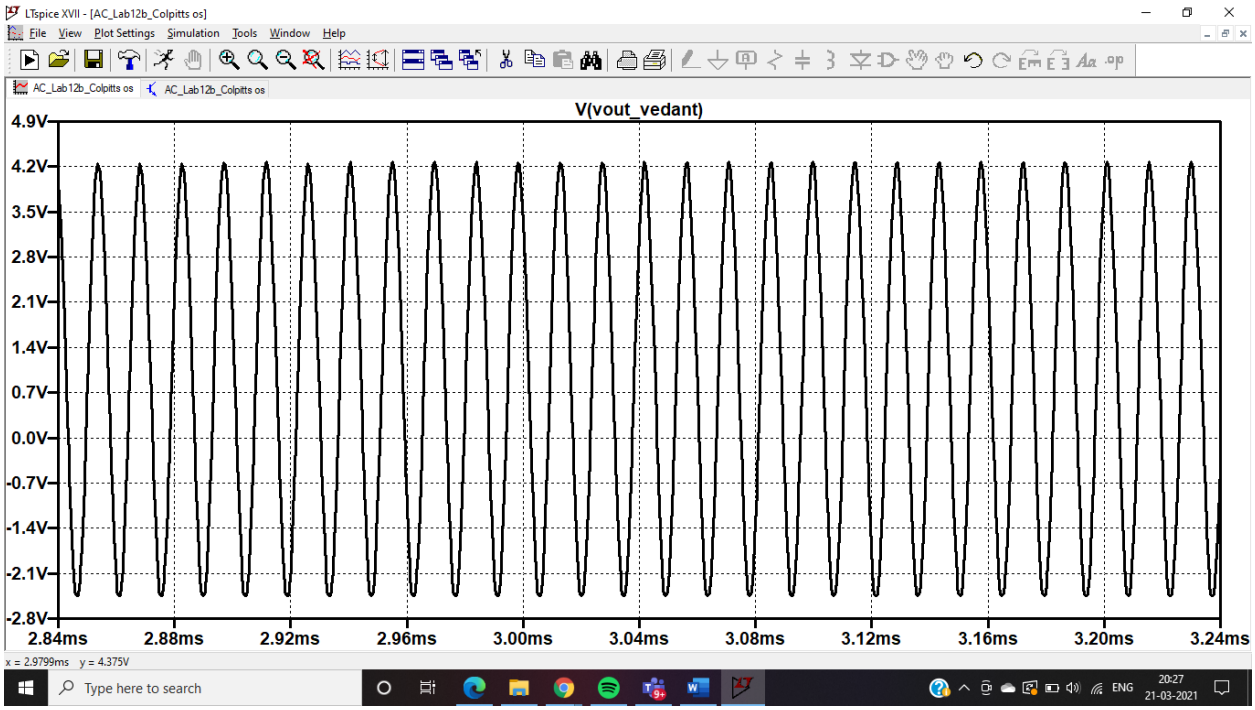

LTspice XVII - [Draft49]
File View Plot Settings Simulation Tools Window Help
Draft46 Draft46 Draft47 Draft47 Draft49 Draft49
V(vin_vedant)
V(vout_vedant)
500mV
400mV
300mV
200mV
100mV
0mV
-100mV
-200mV
-300mV
-400mV
-500mV
0ms
1ms
2ms
3ms
4ms
5ms
6ms
7ms
8ms
9ms
10ms
x = 2.90ms y = 256.91mV
Type here to search
ENG
10:28
01-03-2021



Parameter	Simulated
K (feedback factor)	0.668916

12 B)
Colpitts Oscillator


LTspice XVII - [AC_Lab12b_Colpitts os]
File Edit Hierarchy View Simulate Tools Window Help
AC_Lab12b_Colpitts os
AC_Lab13a
AC_Lab13b
AC_Lab13b
AC_Lab13c
Vedant Kelkar 1912052
AC Lab 12b
Colpitts Oscillator
VCC
10V
R1
100k
R3
10k
Co
1µ
Vout_Vedant
Ci
1µ
A
Q1
2N2222
L1
1m
C3
0.01µ
Vf_Vedant
R2
18k
RE
1k
C2
0.011µ
.tran 0 100m 40m
.meas t1 find time when V(Vout_Vedant)=0 cross=1
.meas t2 find time when V(Vout_Vedant)=0 cross=3
.meas T param t2-t1
.meas frequency param 1/T
Type here to search
ENG
20:08
21-03-2021


LTspice XVII - [AC_Lab12b_Colpitts os]
File View Plot Settings Simulation Tools Window Help
AC_Lab12b_Colpitts os
AC_Lab12b_Colpitts os
V(vout_vedant)
4.9V
4.2V
3.5V
2.8V
2.1V
1.4V
0.7V
0.0V
-0.7V
-1.4V
-2.1V
-2.8V
2.84ms
2.88ms
2.92ms
2.96ms
3.00ms
3.04ms
3.08ms
3.12ms
3.16ms
3.20ms
3.24ms
x = 2.9799ms y = 4.375V
Type here to search
ENG
20:27
21-03-2021

```
Direct Newton iteration for .op point succeeded

t1: time=6.96968e-006 at 6.96968e-006
t2: time=2.14429e-005 at 2.14429e-005
t: t2-t1=1.44733e-005
frequency: 1/t=69092.9
```

Parameter	Calculated	Simulated
fo	69.54 KHz	69.0929 KHz

AC LAB 12 is approved: Inderjit Singh Dhanjal