Audit Course Session 13

AUDIT COURSE
ELECTRONIC CIRCUITS 2: SIMULATION BASED STUDY

Kindly update your name and roll no, once this document is shared with you
Time slot to complete your work is **40 MINUTES**
Date: 2/3/2021
Kindly upload your schematic & waveform images here, every 10 minutes, indicating your progress and intention to completion of WORK within time slot allotted

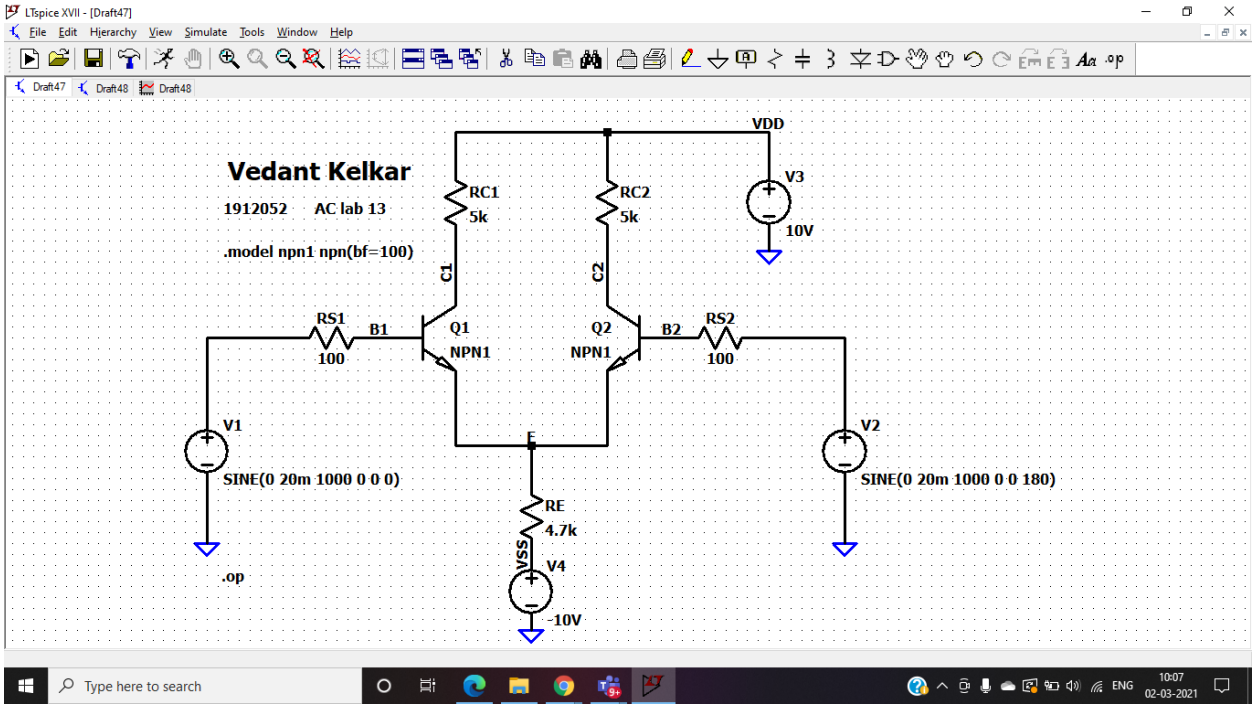
Time slot allotted to you all for the completion of Session 13 is 40 MINUTES

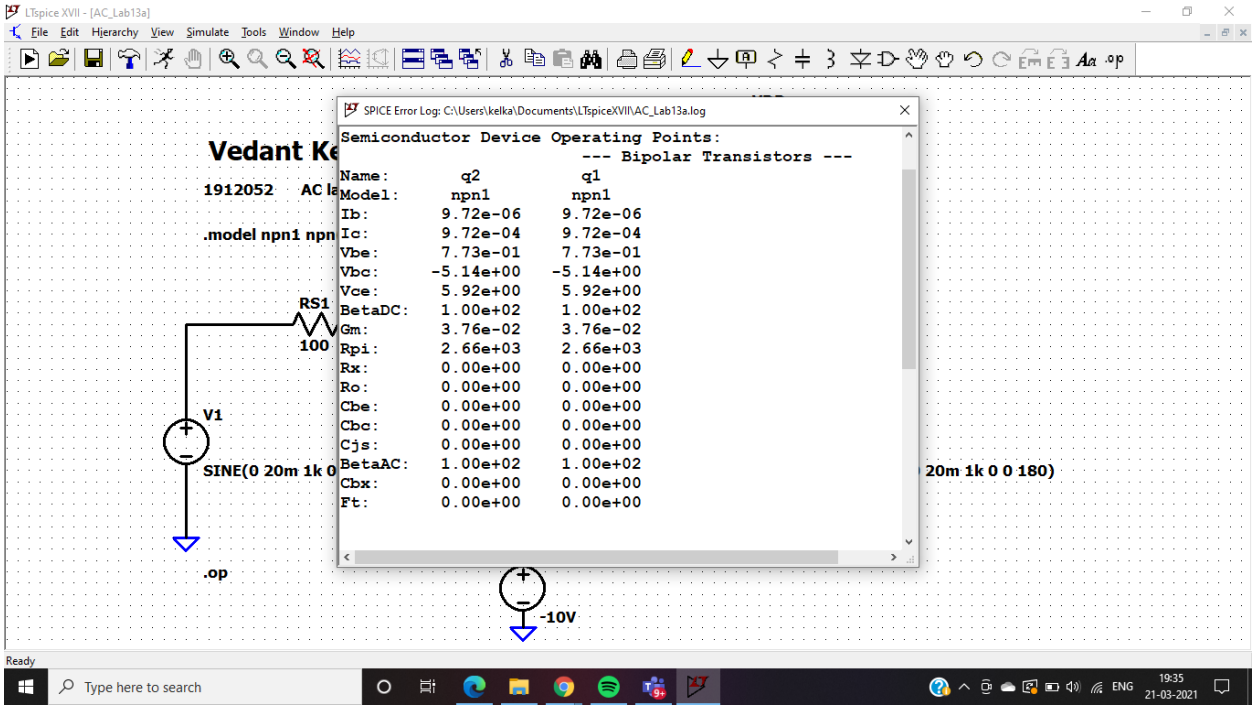
Kindly upload your work (only circuit schematic & waveform in LTspice) in the shared google doc between this time slot only.

Follow these instruction strictly:
1, Start sharp ON TIME, by posting your name and roll no and **screenshot of your LT spice work screen (time and date MUST BE VISIBLE)**
2. Upload your work every 10 minutes, i.e LT spice work screen
3. This means you will upload LT spice work screen 4 times during this time slot.
4. Point 3 indicates your readiness and presences for completion of Session 13

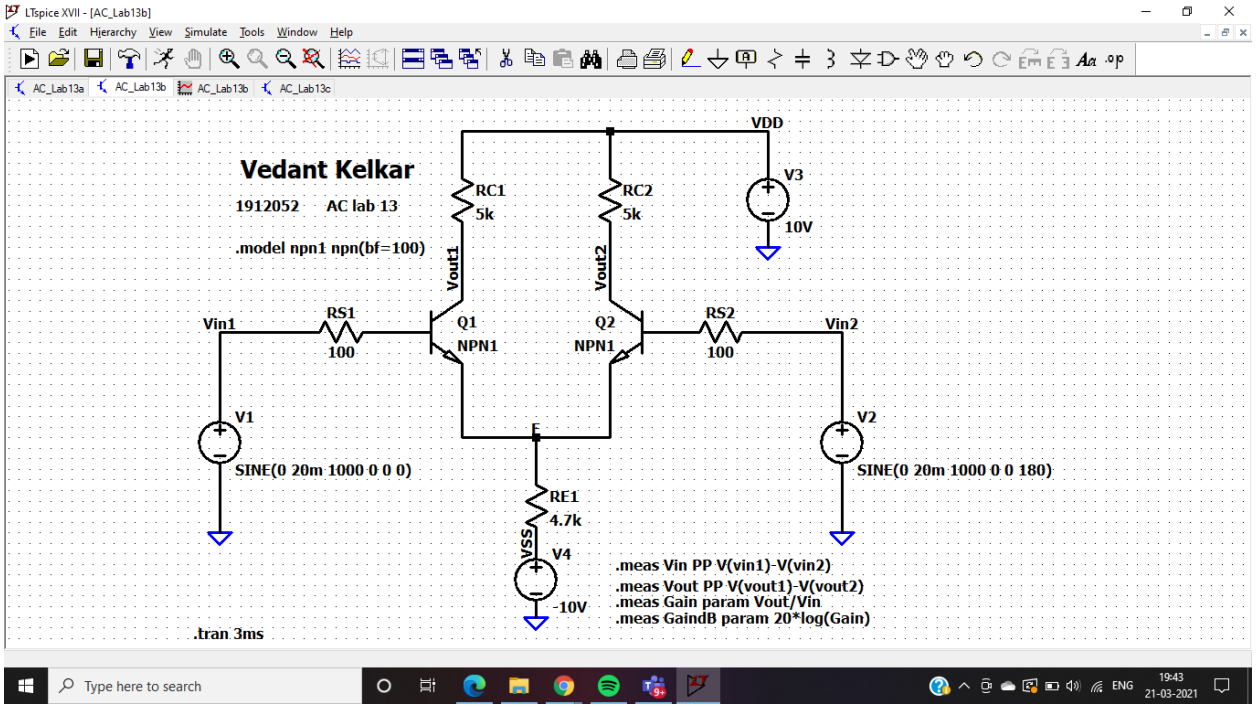
You are entitled for 10 points per session only if you follow above instruction to the details

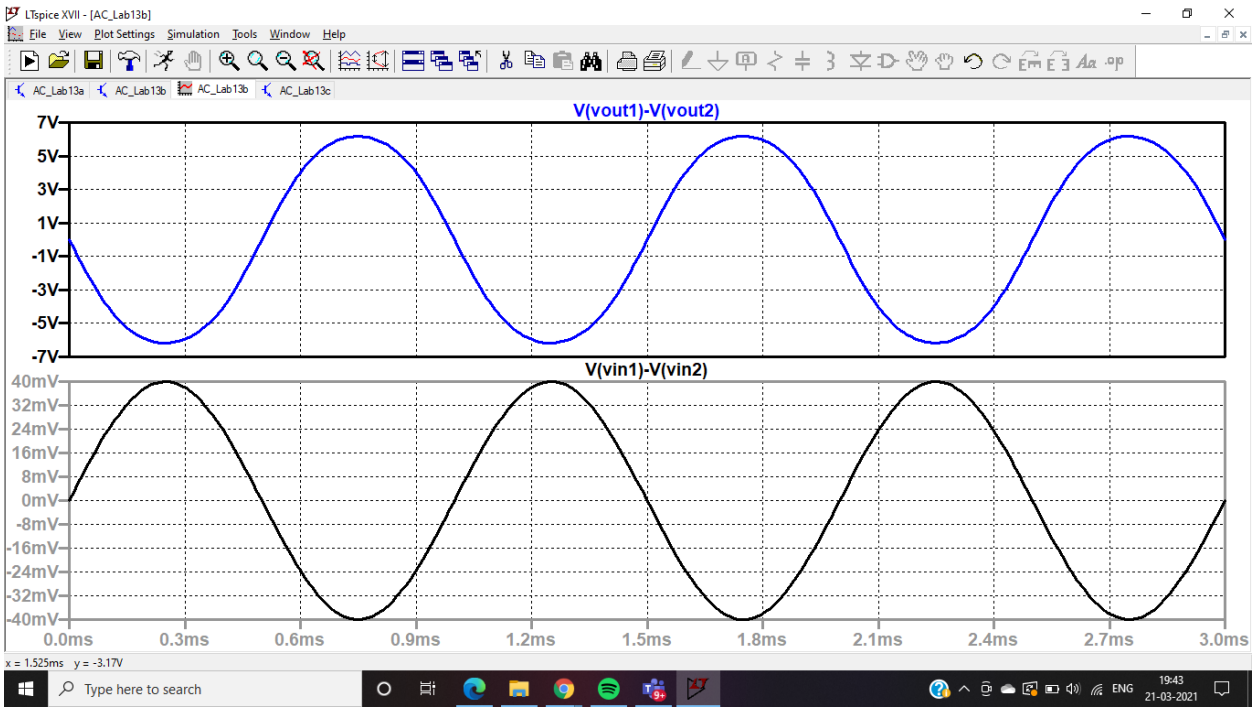
STUDENTS WORK AREA STARTS HERE

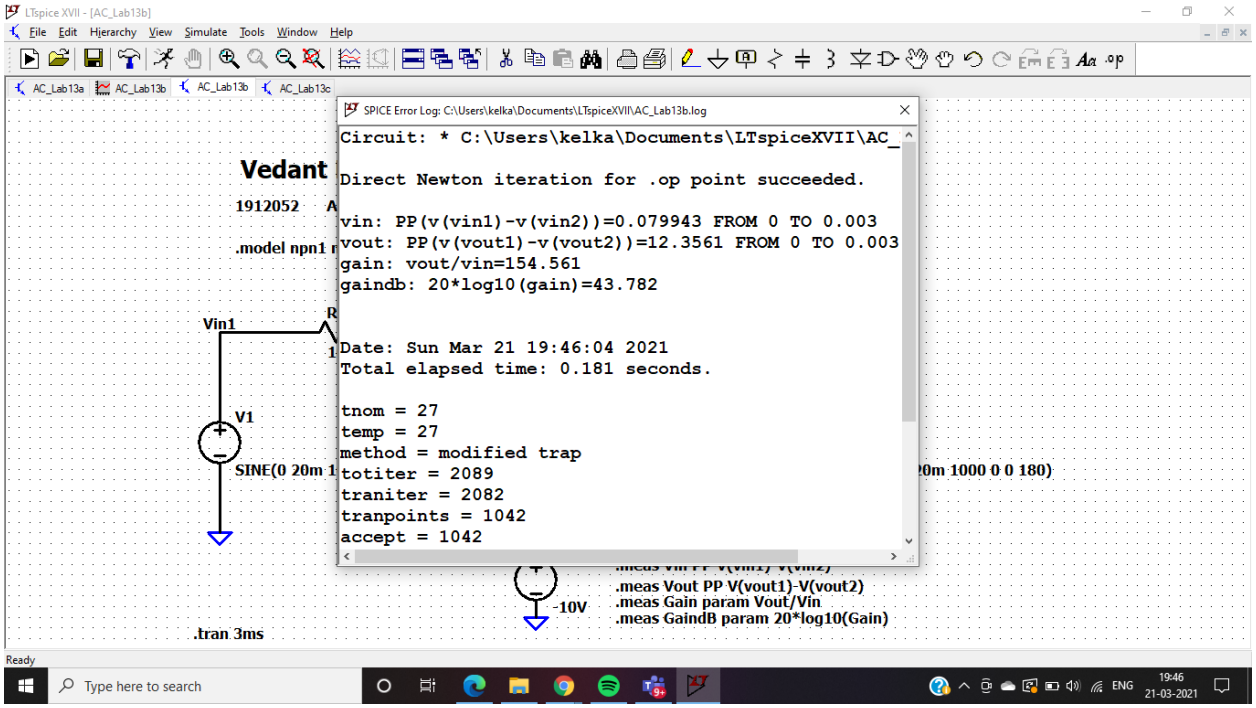

LTspice XVII - [Draft47]
File Edit Hierarchy View Simulate Tools Window Help
Draft47 Draft48 Draft48
Vedant Kelkar
1912052 AC lab 13
.model npn1 npn(bf=100)
VDD
V3
10V
RC1
5k
RC2
5k
C1
C2
RS1
100
B1
Q1
NPN1
Q2
NPN1
B2
RS2
100
V1
SINE(0 20m 1000 0 0 0)
V2
SINE(0 20m 1000 0 0 180)
RE
4.7k
VSS
V4
-10V
.op
Type here to search
ENG
10:07
02-03-2021


LTspice XVII - [AC_Lab13a]
File Edit Hierarchy View Simulate Tools Window Help
SPICE Error Log: C:\Users\kelka\Documents\LTspiceXVII\AC_Lab13a.log
Semiconductor Device Operating Points:
--- Bipolar Transistors ---
Name: q2 q1
Model: npn1 npn1
Ib: 9.72e-06 9.72e-06
Ic: 9.72e-04 9.72e-04
Vbe: 7.73e-01 7.73e-01
Vbc: -5.14e+00 -5.14e+00
Vce: 5.92e+00 5.92e+00
BetaDC: 1.00e+02 1.00e+02
Gm: 3.76e-02 3.76e-02
Rpi: 2.66e+03 2.66e+03
Rx: 0.00e+00 0.00e+00
Ro: 0.00e+00 0.00e+00
Cbe: 0.00e+00 0.00e+00
Cbc: 0.00e+00 0.00e+00
Cjs: 0.00e+00 0.00e+00
BetaAC: 1.00e+02 1.00e+02
Cbx: 0.00e+00 0.00e+00
Ft: 0.00e+00 0.00e+00
RS1
100
V1
.op
-10V
Ready
Type here to search
ENG
19:35
21-03-2021

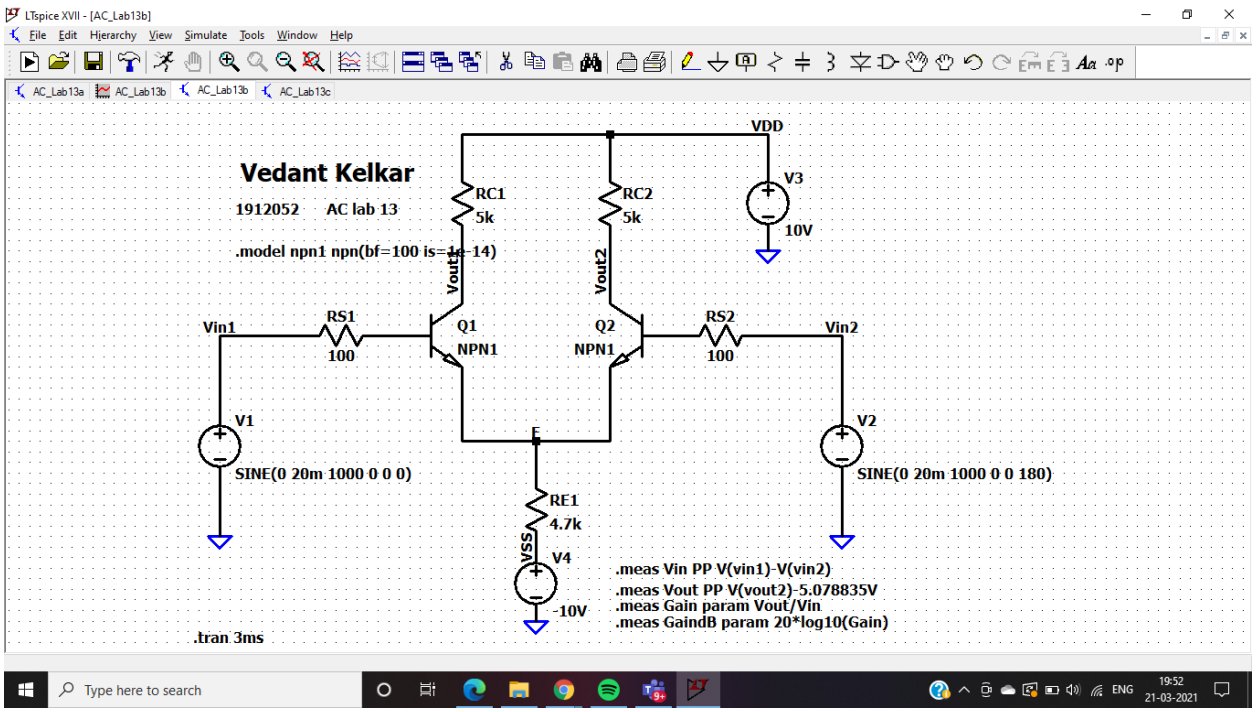
AC

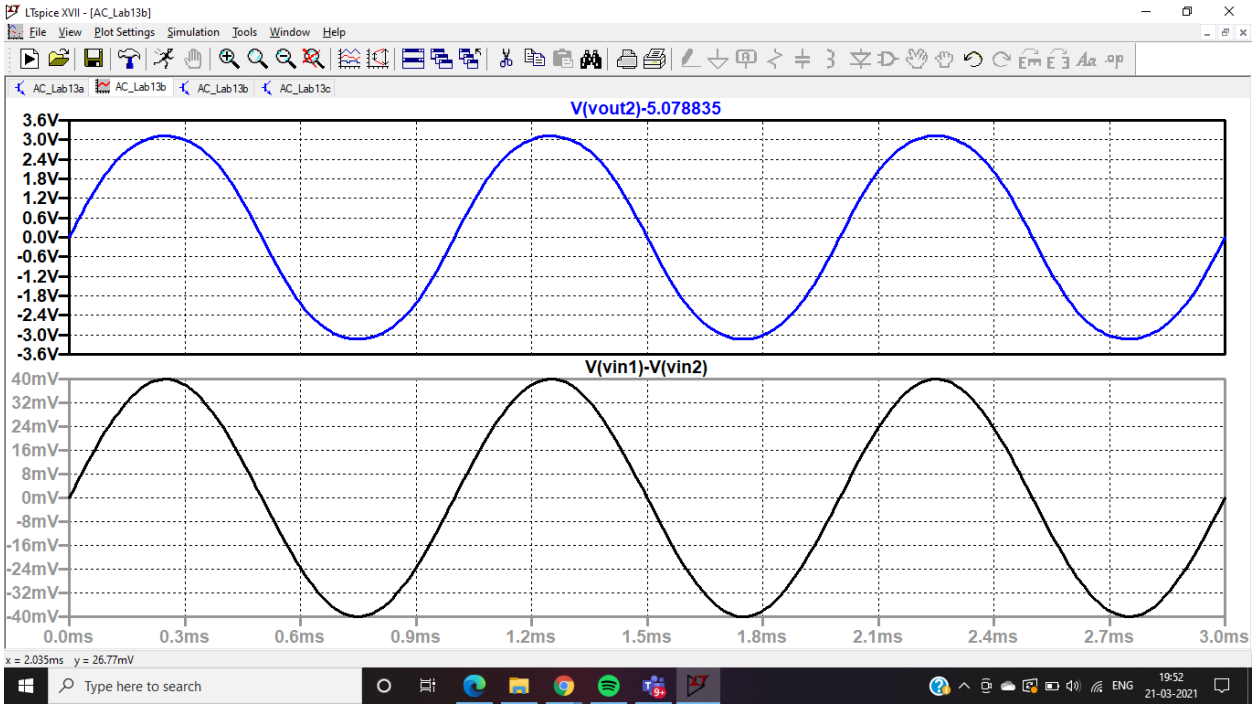

LTspice XVII - [AC_Lab13b]
File Edit Hierarchy View Simulate Tools Window Help
AC_Lab13a AC_Lab13b AC_Lab13b AC_Lab13c
Vedant Kelkar
1912052 AC lab 13
.model npn1 npn(bf=100)
VDD
V3
10V
RC1
5k
RC2
5k
Vout1
Vout2
Vin1
RS1
100
Q1
NPN1
Q2
NPN1
RS2
100
Vin2
V1
SINE(0 20m 1000 0 0 0)
V2
SINE(0 20m 1000 0 0 180)
RE1
4.7k
VSS
V4
-10V
.meas Vin PP V(vin1)-V(vin2)
.meas Vout PP V(vout1)-V(vout2)
.meas Gain param Vout/Vin
.meas GaindB param 20*log(Gain)
.tran 3ms
Type here to search
ENG
19:43
21-03-2021

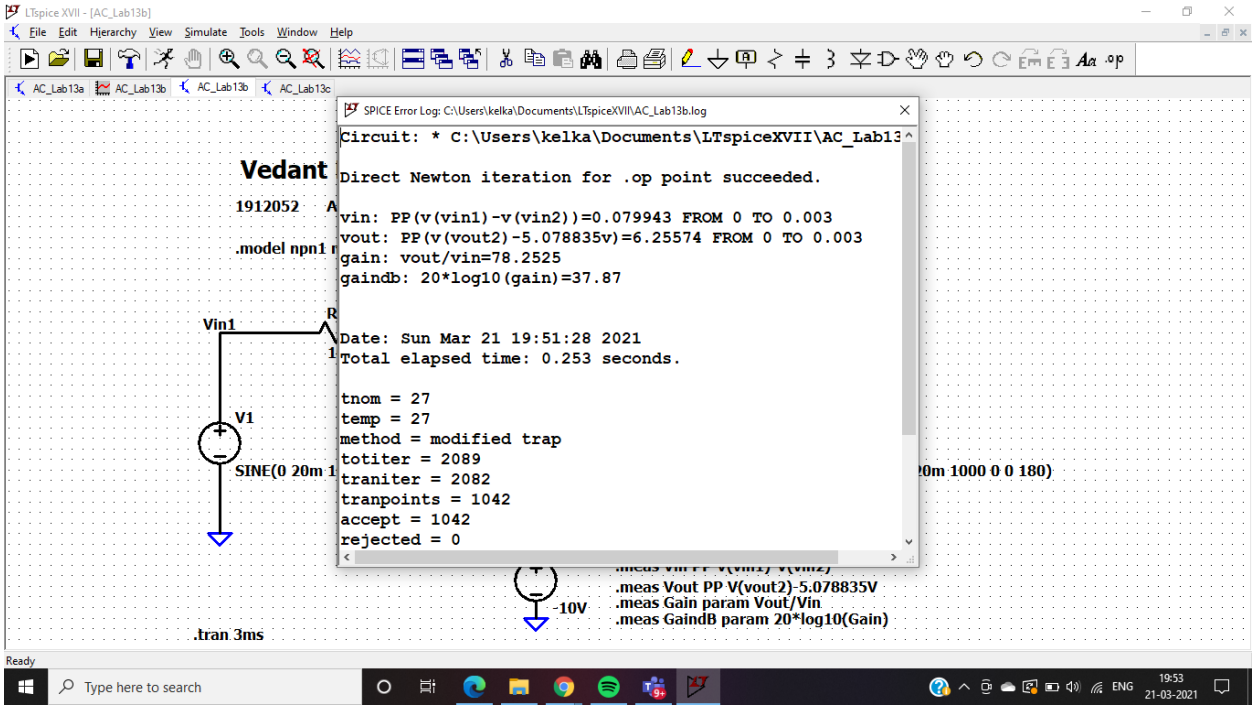

LTspice XVII - [AC_Lab13b]
File View Plot Settings Simulation Tools Window Help
AC_Lab13a AC_Lab13b AC_Lab13b AC_Lab13c
V(vout1)-V(vout2)
7V
5V
3V
1V
-1V
-3V
-5V
-7V
V(vin1)-V(vin2)
40mV
32mV
24mV
16mV
8mV
0mV
-8mV
-16mV
-24mV
-32mV
-40mV
0.0ms
0.3ms
0.6ms
0.9ms
1.2ms
1.5ms
1.8ms
2.1ms
2.4ms
2.7ms
3.0ms
x = 1.525ms y = -3.17V
Type here to search
ENG
19:43
21-03-2021


LTspice XVII - [AC_Lab13b]
File Edit Hierarchy View Simulate Tools Window Help
AC_Lab13a AC_Lab13b AC_Lab13b AC_Lab13c
SPICE Error Log: C:\Users\kelka\Documents\LTspiceXVII\AC_Lab13b.log
Circuit: * C:\Users\kelka\Documents\LTspiceXVII\AC_
Direct Newton iteration for .op point succeeded.
vin: PP(v(vin1)-v(vin2))=0.079943 FROM 0 TO 0.003
vout: PP(v(vout1)-v(vout2))=12.3561 FROM 0 TO 0.003
gain: vout/vin=154.561
gaindb: 20*log10(gain)=43.782
Date: Sun Mar 21 19:46:04 2021
Total elapsed time: 0.181 seconds.
tnom = 27
temp = 27
method = modified trap
totiter = 2089
traniter = 2082
tranpoints = 1042
accept = 1042
Vedant
1912052
.model npn1
Vin1
V1
SINE(0 20m 1
-10V
.meas Vout PP V(vout1)-V(vout2)
.meas Gain param Vout/Vin
.meas GaindB param 20*log10(Gain)
.tran 3ms
Ready
Type here to search
ENG
19:46
21-03-2021

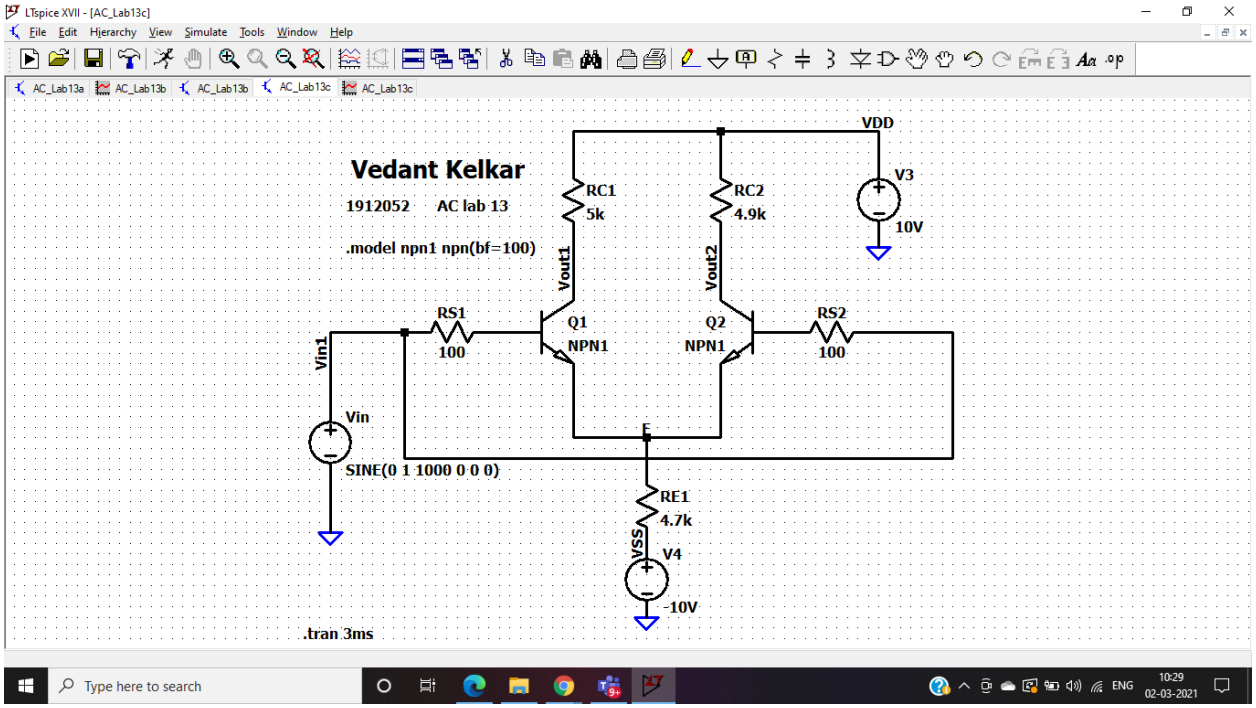
For DIUO

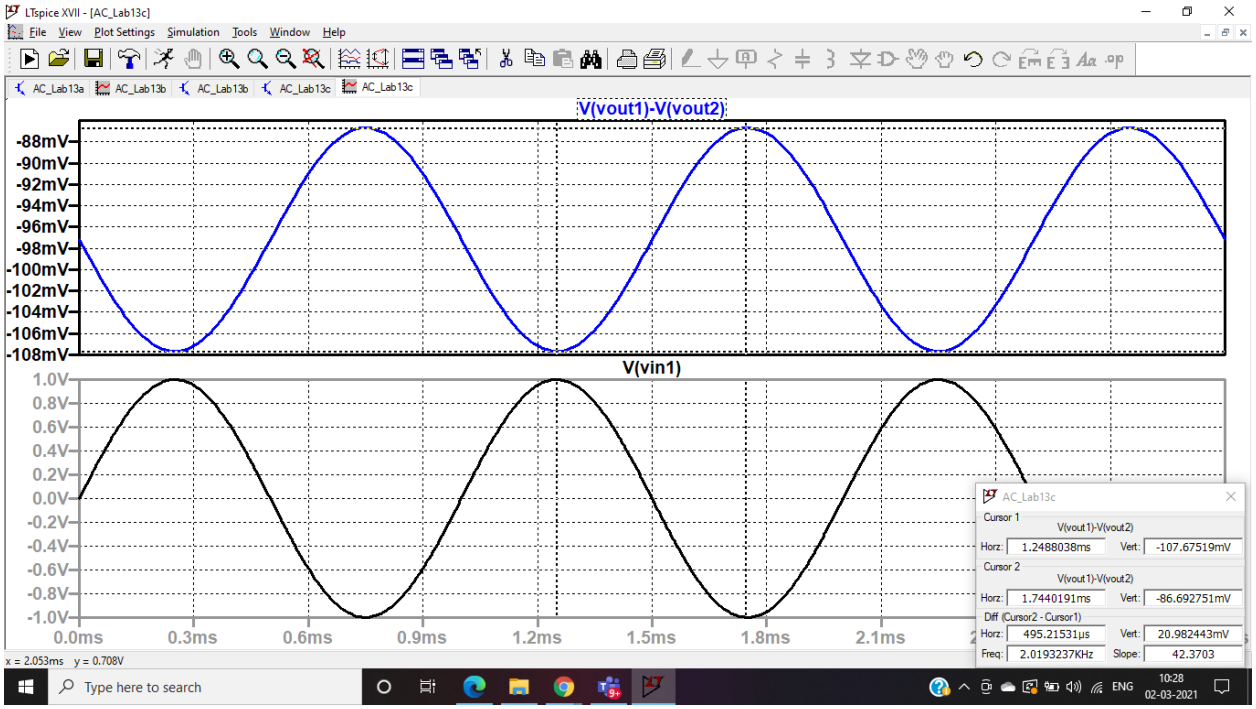

LTspice XVII - [AC_Lab13b]
File Edit Hierarchy View Simulate Tools Window Help
AC_Lab13a AC_Lab13b AC_Lab13b AC_Lab13c
Vedant Kelkar
1912052 AC lab 13
.model npn1 npn(bf=100 is=1e-14)
VDD
V3
10V
RC1
5k
RC2
5k
Vout1
Vout2
Vin1
RS1
100
Q1
NPN1
Q2
NPN1
RS2
100
Vin2
V1
SINE(0 20m 1000 0 0 0)
V2
SINE(0 20m 1000 0 0 180)
E
RE1
4.7k
VSS
V4
-10V
.meas Vin PP V(vin1)-V(vin2)
.meas Vout PP V(vout2)-5.078835V
.meas Gain param Vout/Vin
.meas GaindB param 20*log10(Gain)
.tran 3ms
Type here to search
ENG
19:52
21-03-2021





o/p-6.1732197V
ip=80mv
AD=77.125 DIBO





o/p=194.367mV
i/p=2V
Acm=0.0972 DIBO

AC LAB 13 is approved: Inderjit Singh Dhanjal