K. J. Somaiya College of Engineering, Mumbai-77
(A Constituent College of Somaiya Vidyavihar University)
Department of Electronics Engineering

LINEAR INTEGRATED CIRCUIT AND DESIGN

IA2 Simulation based Assignment
Sem-Vth (2021-22)
Total marks-50

Instructions:

- **Attempt All questions**
- **Even roll number students and Odd roll number students are required to solve the respective numerical mentioned.**
-

Note:

- In simulation, you are required to put **Roll_no_Name** on schematic .
- Also write **DOP and IA1** on top right side of simulation
- In waveform, Vin(name of student) and Vo(name of student) should be written

ETRX B1

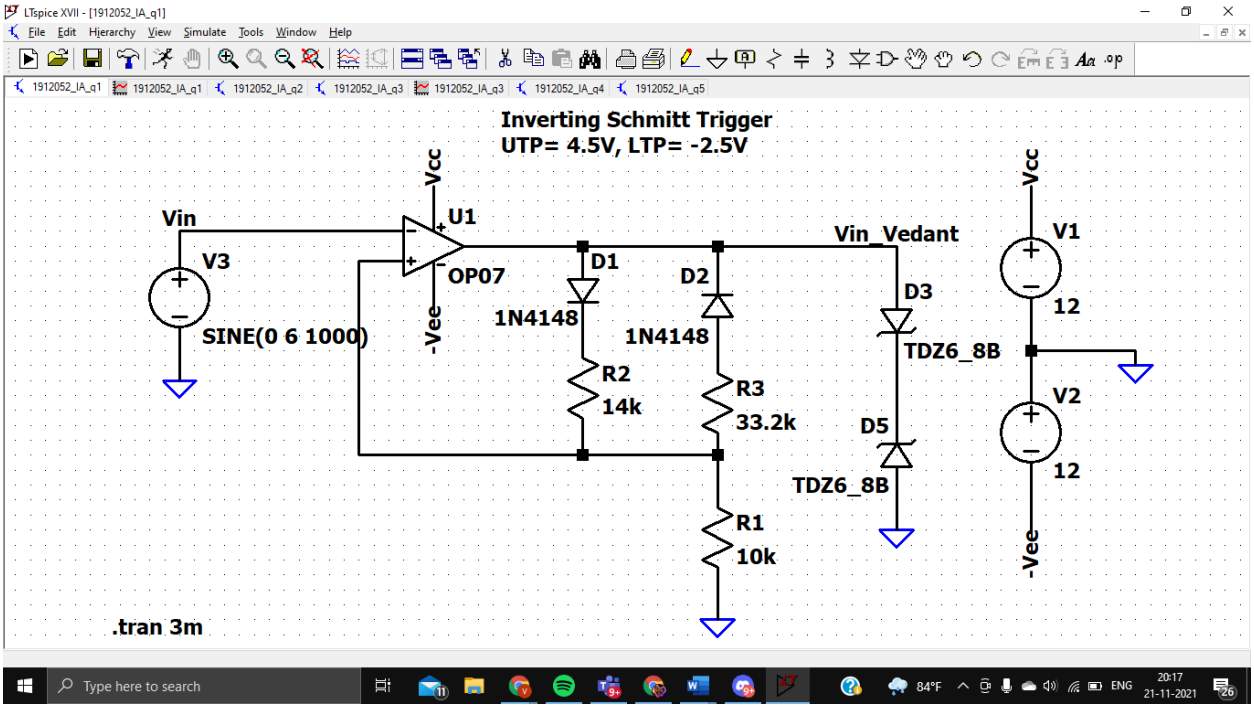
Name: Vedant Kelkar

Roll No: 1912052
Marks:

Q1. Design an Inverting Schmitt Trigger with upper threshold point as + 4.5V and lower threshold point as - 2.5V (Even roll no: Solve this)

Design an Inverting Schmitt Trigger with upper threshold point as + 4V and lower threshold point as - 6V (Odd roll no: Solve this)

Hint: Use Asymmetric design technique with diodes.
Build your designed circuit in LTspice and verify/validate your design values with at least three set of reading's for the suitable inputs (include one where hysteresis curve disappears) (Attach handwritten solution of design, and printscreen images of schematic & results. Also, prepare observation table for three set of readings)


LTspice XVII - [1912052_IA_q1]
File Edit Hierarchy View Simulate Tools Window Help
1912052_IA_q1 1912052_IA_q1 1912052_IA_q2 1912052_IA_q3 1912052_IA_q3 1912052_IA_q4 1912052_IA_q5
Inverting Schmitt Trigger
UTP= 4.5V, LTP= -2.5V
Vcc
Vin
U1
V3
OP07
SINE(0 6 1000)
-Vee
D1
1N4148
D2
1N4148
Vin_Vedant
D3
TDZ6_8B
V1
12
R2
14k
R3
33.2k
D5
TDZ6_8B
V2
12
R1
10k
-Vee
.tran 3m
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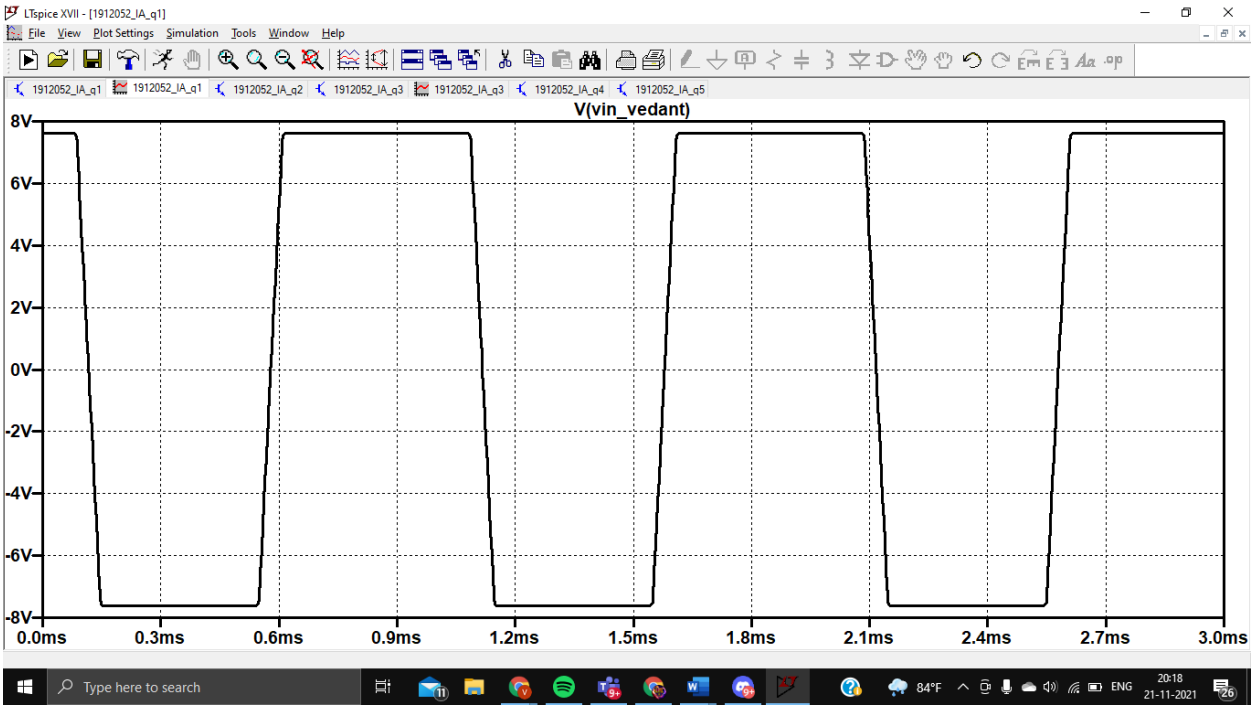
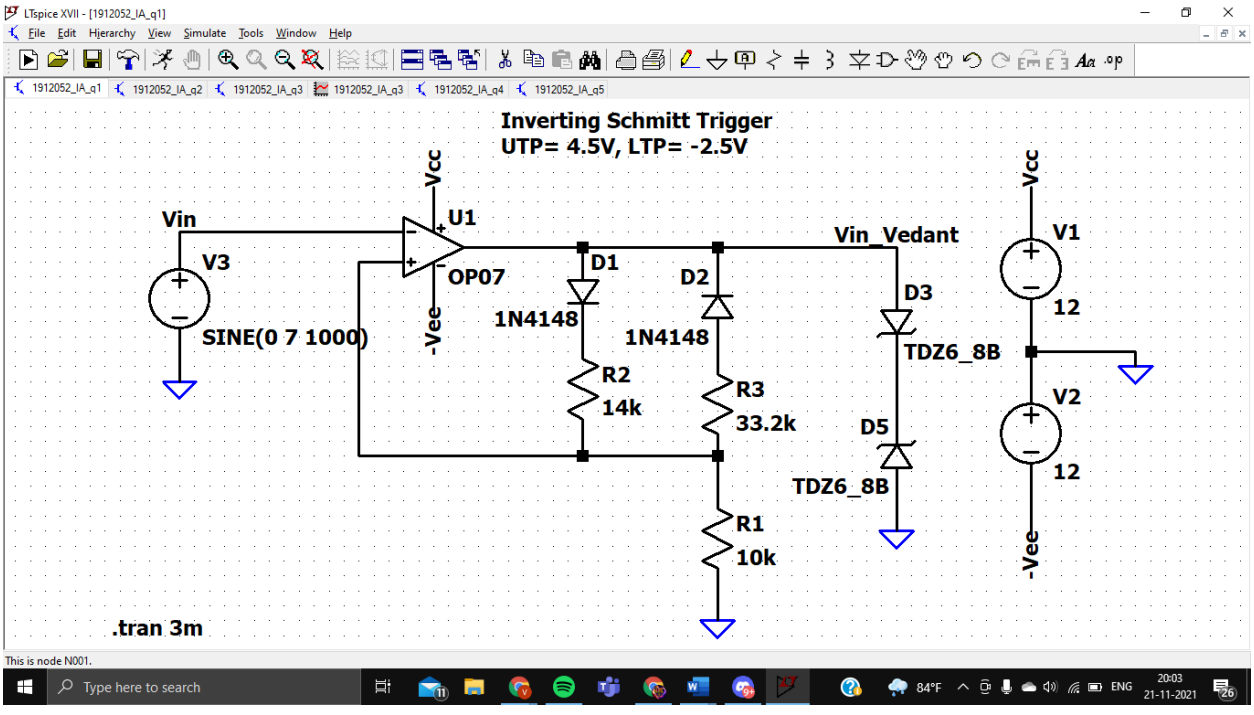
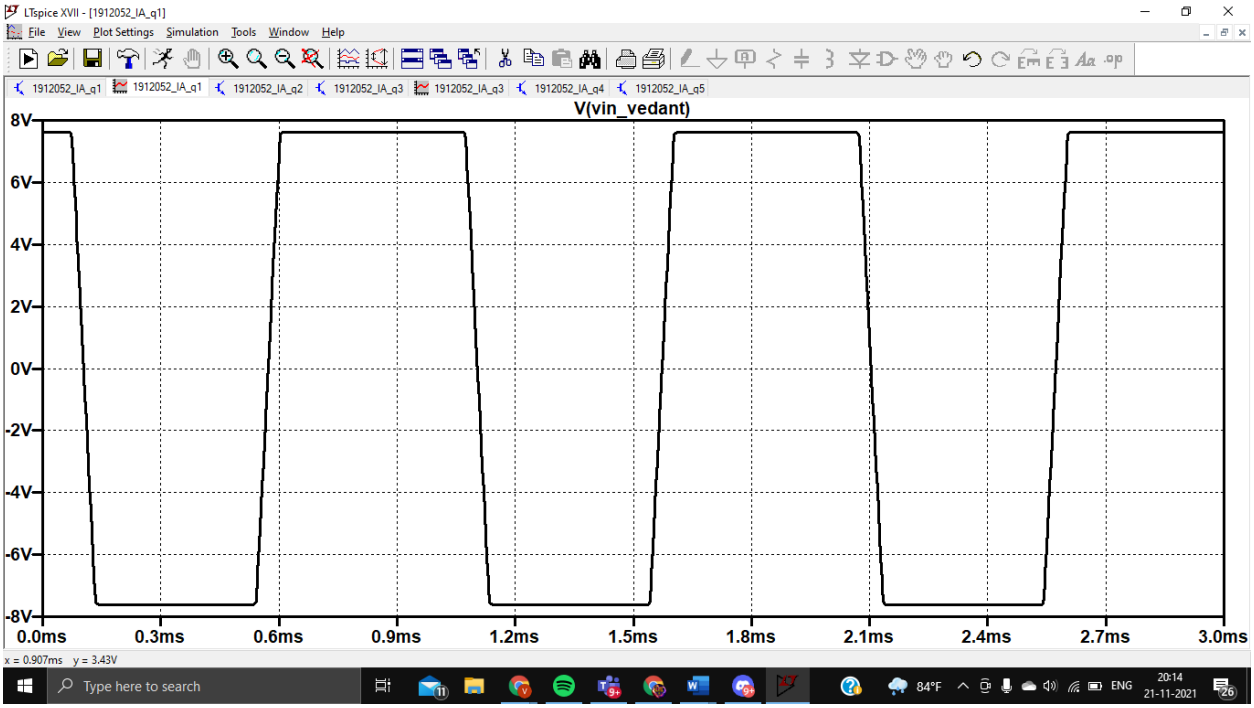
84°F
ENG
20:17
21-11-2021


LTspice XVII - [1912052_IA_q1]
File View Plot Settings Simulation Tools Window Help
V(vin_vedant)
8V
6V
4V
2V
0V
-2V
-4V
-6V
-8V
0.0ms
0.3ms
0.6ms
0.9ms
1.2ms
1.5ms
1.8ms
2.1ms
2.4ms
2.7ms
3.0ms


LTspice XVII - [1912052_IA_q1]
File Edit Hierarchy View Simulate Tools Window Help
Inverting Schmitt Trigger
UTP= 4.5V, LTP= -2.5V
Vin
V3
SINE(0 7 1000)
U1
OP07
Vcc
-Vee
D1
1N4148
D2
1N4148
R2
14k
R3
33.2k
R1
10k
Vin_Vedant
D3
TDZ6_8B
D5
TDZ6_8B
V1
12
V2
12
.tran 3m
This is node N001.


LTspice XVII - [1912052_IA_q1]
File View Plot Settings Simulation Tools Window Help
1912052_IA_q1 1912052_IA_q1 1912052_IA_q2 1912052_IA_q3 1912052_IA_q3 1912052_IA_q4 1912052_IA_q5
V(vin_vedant)
8V
6V
4V
2V
0V
-2V
-4V
-6V
-8V
0.0ms 0.3ms 0.6ms 0.9ms 1.2ms 1.5ms 1.8ms 2.1ms 2.4ms 2.7ms 3.0ms
x = 0.907ms y = 3.43V
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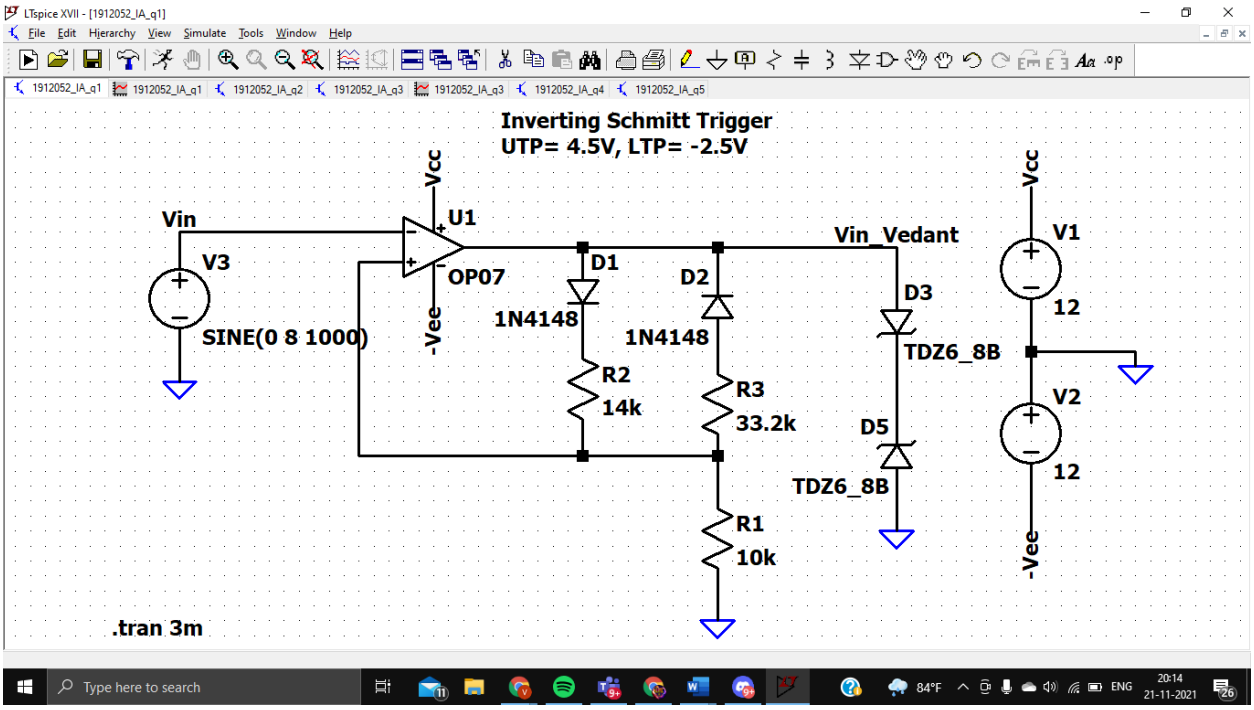
84°F
ENG
20:14
21-11-2021


LTspice XVII - [1912052_IA_q1]
File Edit Hierarchy View Simulate Tools Window Help
1912052_IA_q1 1912052_IA_q1 1912052_IA_q2 1912052_IA_q3 1912052_IA_q3 1912052_IA_q4 1912052_IA_q5
Inverting Schmitt Trigger
UTP= 4.5V, LTP= -2.5V
Vcc
U1
Vin
V3
OP07
SINE(0 8 1000)
-Vee
D1
1N4148
D2
1N4148
Vin_Vedant
D3
TDZ6_8B
V1
12
R2
14k
R3
33.2k
D5
TDZ6_8B
V2
12
R1
10k
-Vee
.tran 3m
Type here to search
84°F
ENG
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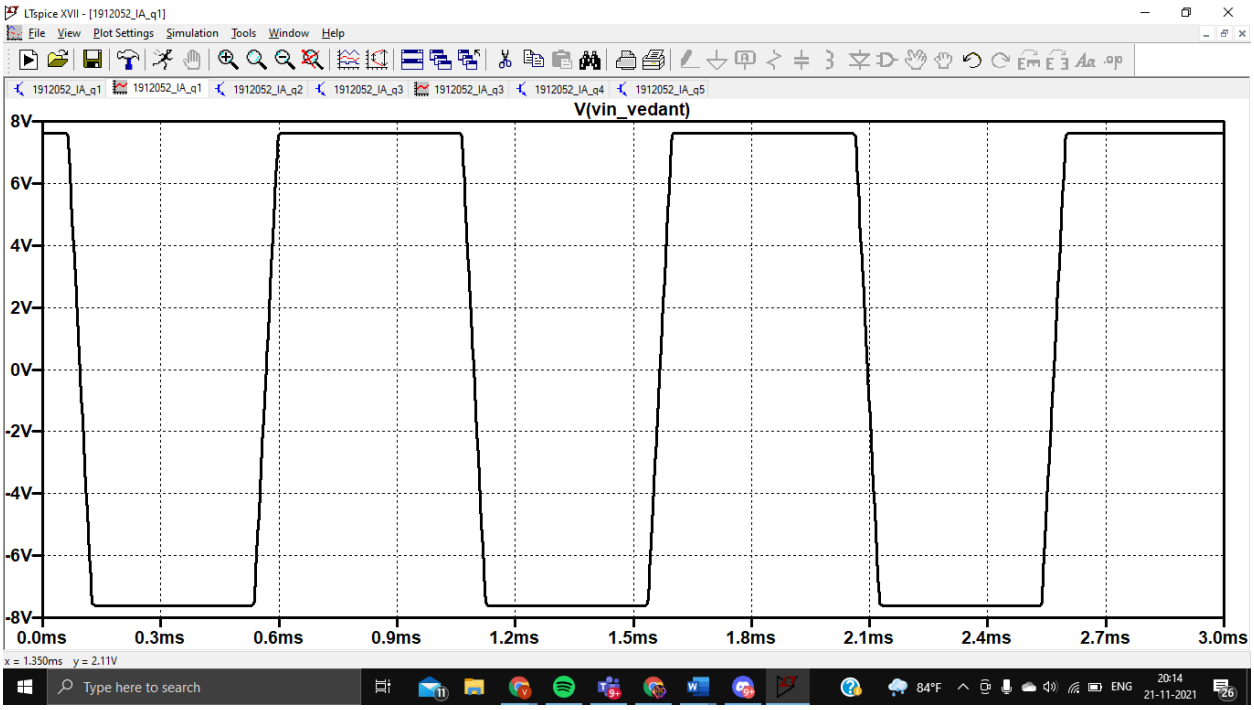
21-11-2021



Vin	Vutp	Vltp
6V	4.3V	-2.48V
7V	3.8V	-2.25V
8V	4V	-2.5V

Somaiya Vidyavihar University

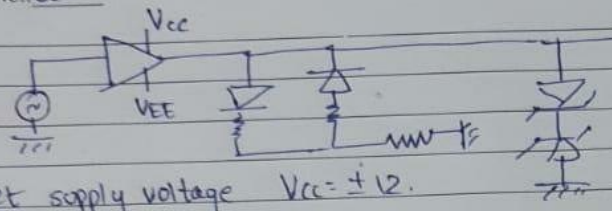
Answer Sheet: Online Examination

Roll No.:	1912052
Page No.	

Date : 21/11/2021

Name of the student:	Signature of the student:
Vedant Kelkar.	Kelkar

Q. No.: Q1



let supply voltage $V_{cc} = \pm 12$.

$V_{sat} = 0.9 \times \pm 12 = \pm 10.8\ V$

for positive V_{sat} voltage diode D_1

$V_{UT} = +4.5$

$V^+ = 4.5$

$V^+ = 4.5 = \frac{R_1}{R_1 + R_2} \times V_{sat}$

Let $R_1 = 10k\Omega$

$4.5 = \frac{10k}{10k + R_2} \times 10.8$

$R_2 = 14k\Omega$.

$-V_{sat}$ voltage D_2 is ON

$V_{LTP} = -2.5V$

$R_1 = 10k\Omega$

$V^+ = \frac{R_1}{R_1 + R_3} \times V_{sat}$

$-2.5 = \frac{10k}{10k + R_3} \times (-10.8)$

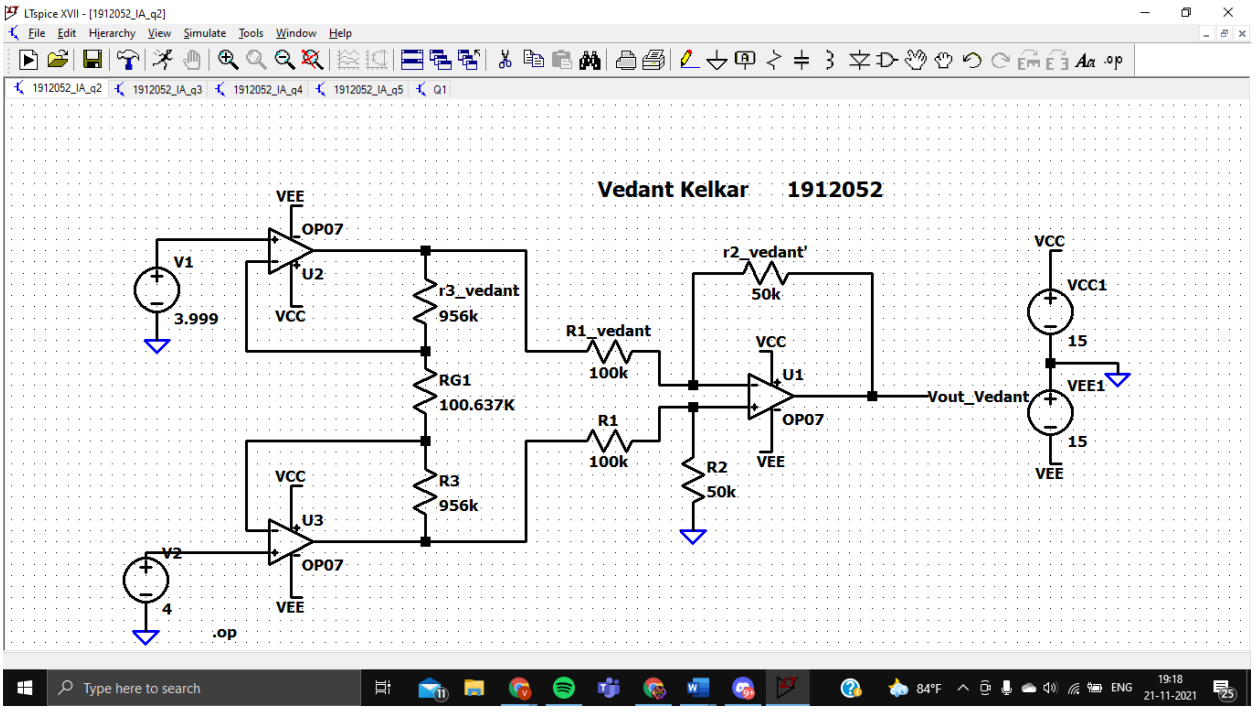
$R_3 = \frac{10k(-10.8)}{-2.5} - 10k = 33.2k\Omega$

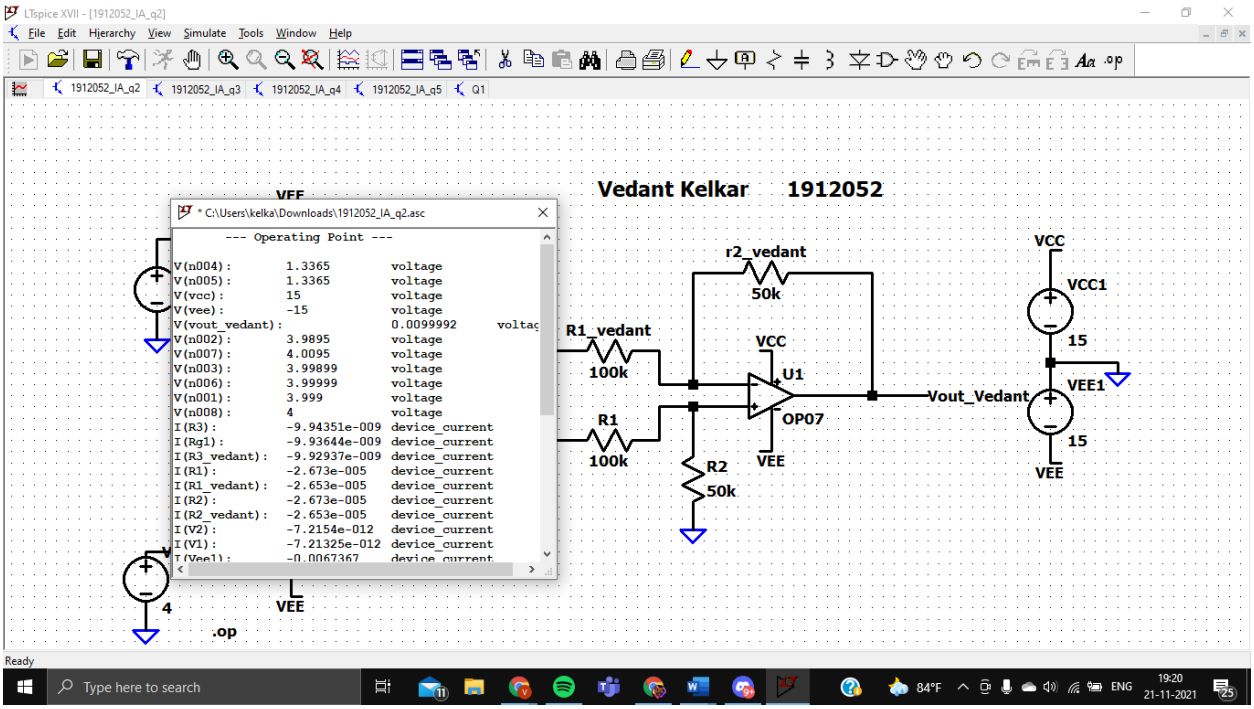
Q1 is for 10 marks, Select suitable Supply voltage to power up the Opamp OP-07

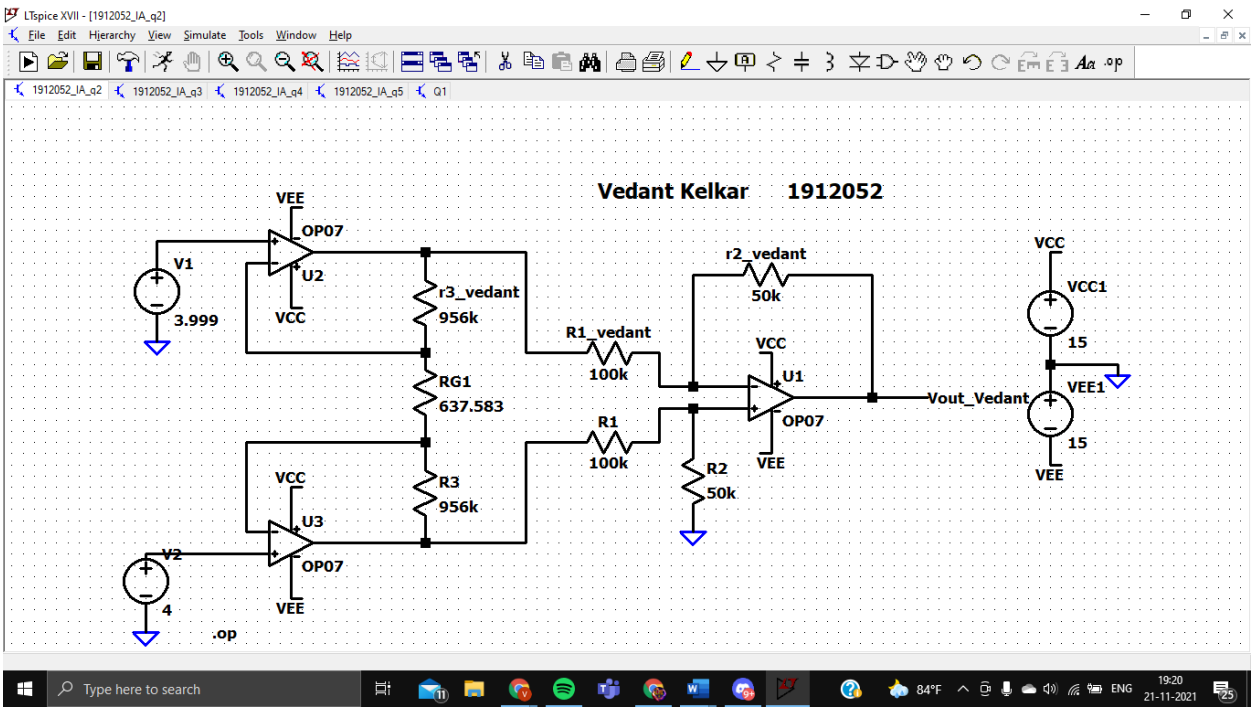
Q2. Design an instrumentation amplifier whose gain can be varied in the range of 2 to 2500. **(Odd roll no: Solve this)**

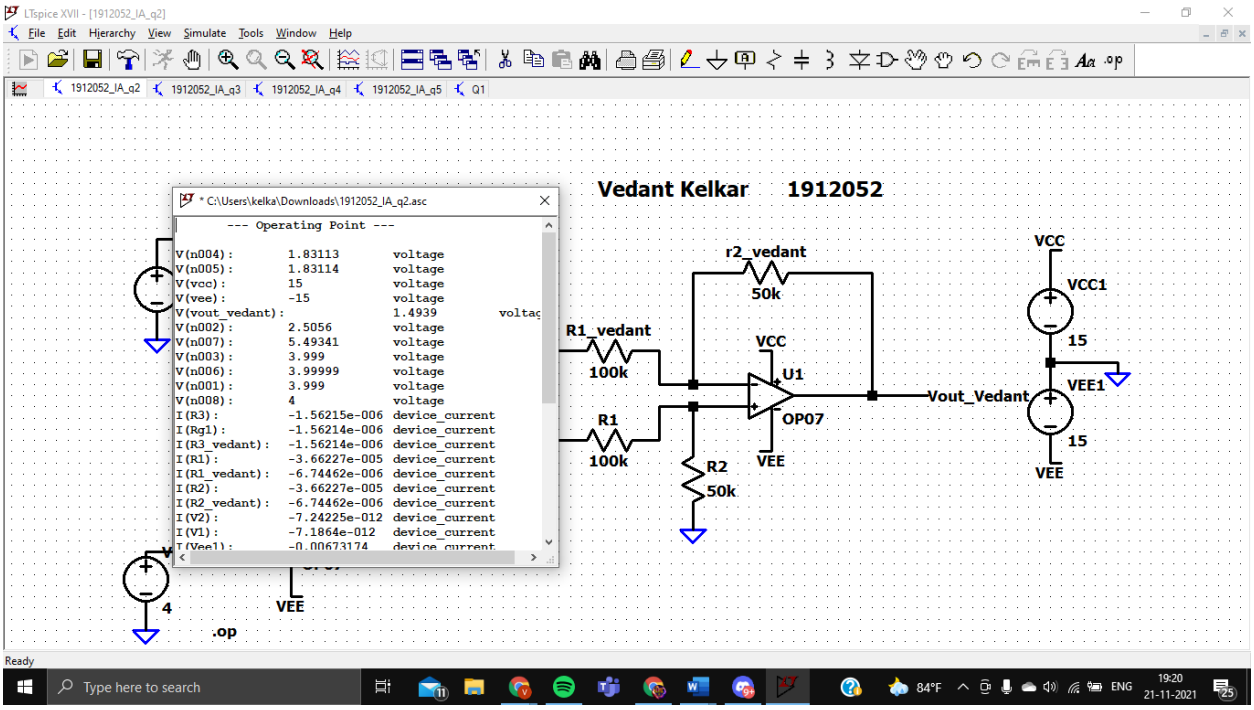
Design an instrumentation amplifier whose gain can be varied in the range of 10 to 1500. **(EVEN roll no: Solve this)**

Hint: Start with 2nd stage design first.
Build your designed circuit in LTspice and verify/validate your design values with at least three set of reading's for the **suitable** inputs. (Attach handwritten solution of design, and printscreen images of schematic & results. Also, prepare observation table for three set of readings)




LTspice XVII - [1912052_IA_q2]
File Edit Hierarchy View Simulate Tools Window Help
1912052_IA_q2 1912052_IA_q3 1912052_IA_q4 1912052_IA_q5 Q1
Vedant Kelkar 1912052
C:\Users\kelka\Downloads\1912052_IA_q2.asc
--- Operating Point ---
V(n004): 1.3365 voltage
V(n005): 1.3365 voltage
V(vcc): 15 voltage
V(vee): -15 voltage
V(vout_vedant): 0.0099992 voltag
V(n002): 3.9895 voltage
V(n007): 4.0095 voltage
V(n003): 3.99899 voltage
V(n006): 3.99999 voltage
V(n001): 3.999 voltage
V(n008): 4 voltage
I(R3): -9.94351e-009 device_current
I(Rg1): -9.93644e-009 device_current
I(R3_vedant): -9.92937e-009 device_current
I(R1): -2.673e-005 device_current
I(R1_vedant): -2.653e-005 device_current
I(R2): -2.673e-005 device_current
I(R2_vedant): -2.653e-005 device_current
I(V2): -7.2154e-012 device_current
I(V1): -7.21325e-012 device_current
VEE
r2_vedant
50k
R1_vedant
100k
VCC
U1
OP07
R1
100k
R2
50k
VEE
Vout_Vedant
VCC
VCC1
15
VEE1
15
VEE
4
.op
Ready
Type here to search
84°F
ENG
19:20
21-11-2021


LTspice XVII - [1912052_IA_q2]
File Edit Hierarchy View Simulate Tools Window Help
1912052_IA_q2 1912052_IA_q3 1912052_IA_q4 1912052_IA_q5 Q1
Vedant Kelkar 1912052
VEE
OP07
V1
3.999
U2
VCC
r3_vedant
956k
RG1
637.583
R3
956k
VCC
U3
V2
4
OP07
VEE
.op
r2_vedant
50k
R1_vedant
100k
VCC
U1
OP07
R1
100k
R2
50k
VEE
Vout_Vedant
VCC
VCC1
15
VEE1
15
VEE
Type here to search
84°F
ENG
19:20
21-11-2021


LTspice XVII - [1912052_IA_q2]
File Edit Hierarchy View Simulate Tools Window Help
1912052_IA_q2 1912052_IA_q3 1912052_IA_q4 1912052_IA_q5 Q1
* C:\Users\kelka\Downloads\1912052_IA_q2.asc
--- Operating Point ---
V(n004): 1.83113 voltage
V(n005): 1.83114 voltage
V(vcc): 15 voltage
V(vee): -15 voltage
V(vout_vedant): 1.4939 voltag
V(n002): 2.5056 voltage
V(n007): 5.49341 voltage
V(n003): 3.999 voltage
V(n006): 3.99999 voltage
V(n001): 3.999 voltage
V(n008): 4 voltage
I(R3): -1.56215e-006 device_current
I(Rg1): -1.56214e-006 device_current
I(R3_vedant): -1.56214e-006 device_current
I(R1): -3.66227e-005 device_current
I(R1_vedant): -6.74462e-006 device_current
I(R2): -3.66227e-005 device_current
I(R2_vedant): -6.74462e-006 device_current
I(V2): -7.24225e-012 device_current
I(V1): -7.1864e-012 device_current
Vedant Kelkar 1912052
r2_vedant
50k
R1_vedant
100k
R1
100k
R2
50k
VCC
U1
OP07
VEE
Vout_Vedant
VCC
VCC1
15
VEE1
15
VEE
4
VEE
.op
Ready
Type here to search
84°F
ENG
19:20
21-11-2021

Somaiya Vidyavihar University

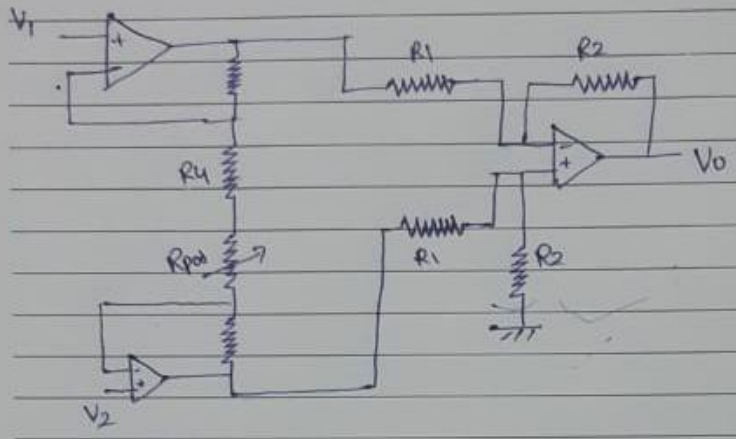
Answer Sheet: Online Examination

Roll No.:	
Page No.	

Date : 21/11/2021

Name of the student:	Signature of the student:
Vedant Kelkar	Kelkar

Q. No.: Q2



Gain from 2nd stage = 0.5

Gain 2 = $\frac{R_2}{R_1}$ = 0.5.

R_1 = 100kΩ R_2 = 50kΩ

A $\frac{R_2}{R_1}\left[1 + \frac{2R_3}{R_a}\right]$ $R_a = R_4 + R_{pot}$

when gain is min(1) R_a is max
when gain is max(1500) $R_a = R_4$

$$100 = 0.5\left[1 + \frac{2R_3}{R_4 + R_{pot}}\right]$$

$$20 = 1 + \frac{2R_3}{R_4 + R_{pot}} \qquad 19 = \frac{2R_3}{R_4 + R_{pot}}$$

Let R_{pot} = 100kΩ.

Somaiya Vidyavihar University

Answer Sheet: Online Examination

Roll No.:	1912052
Page No.	

Date :

Name of the student:	Signature of the student:
Vedant kelkar	

Q. No.: Q2.

$19(R_4+100k) = 2R_3$ -①

now, for maximum gain

$$1500 = \frac{R_2}{R_1}\left[1+\frac{2R_3}{R_4}\right] = 0.5\left[1+\frac{2R_3}{R_4}\right]$$

$$3000 = 1+\frac{2R_3}{R_4}$$

$2999 \cdot R_4 = 2R_3$ -②

$2999\,R_4 = 19(R_4+100k)$

$2980R_4 = 1900k$

$R_4 = 637.583\,\Omega$

from ①

$2R_3 = 19(R_4+100k)$

$R_3 = 956.057\,k\Omega$.

$R_1 = 100k\Omega$ $R_4 = 637.583\Omega$

$R_2 = 50k\Omega$ $R_{pot} = 100k\Omega$

$R_3 = 956.057k\Omega$

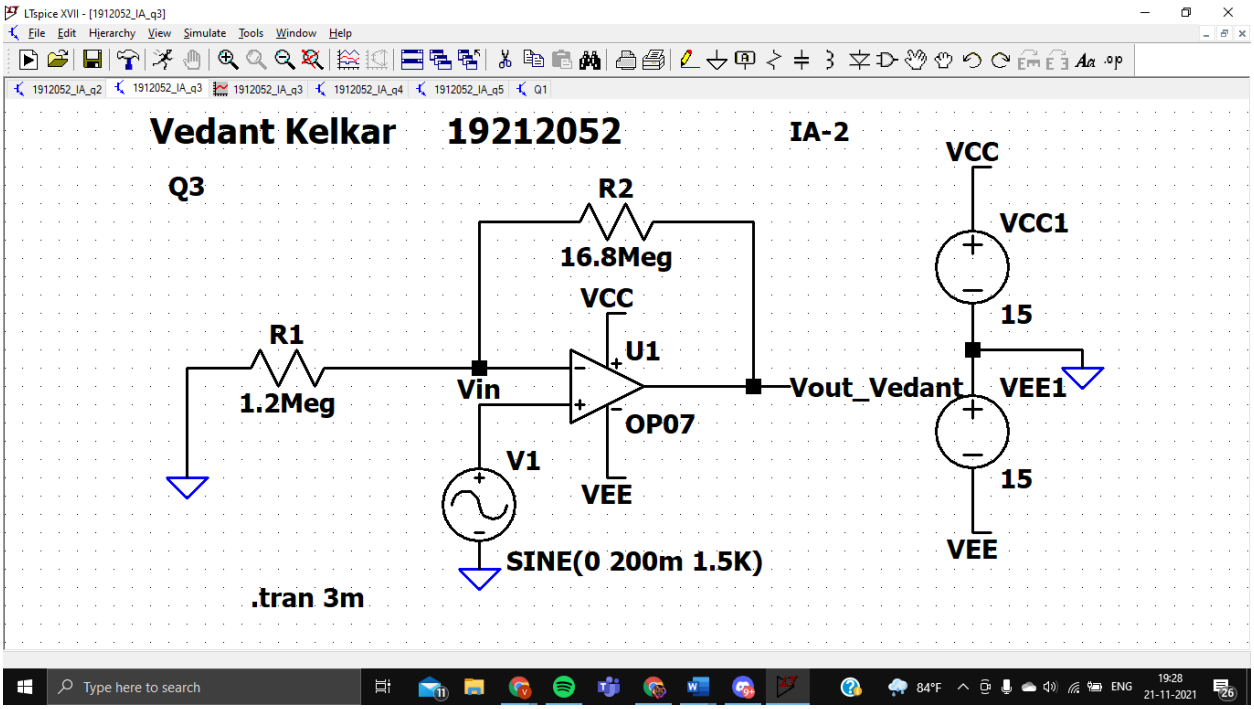
Q2 is for 10 marks, Supply voltage can be ±15 V to power up the Opamp OP-07

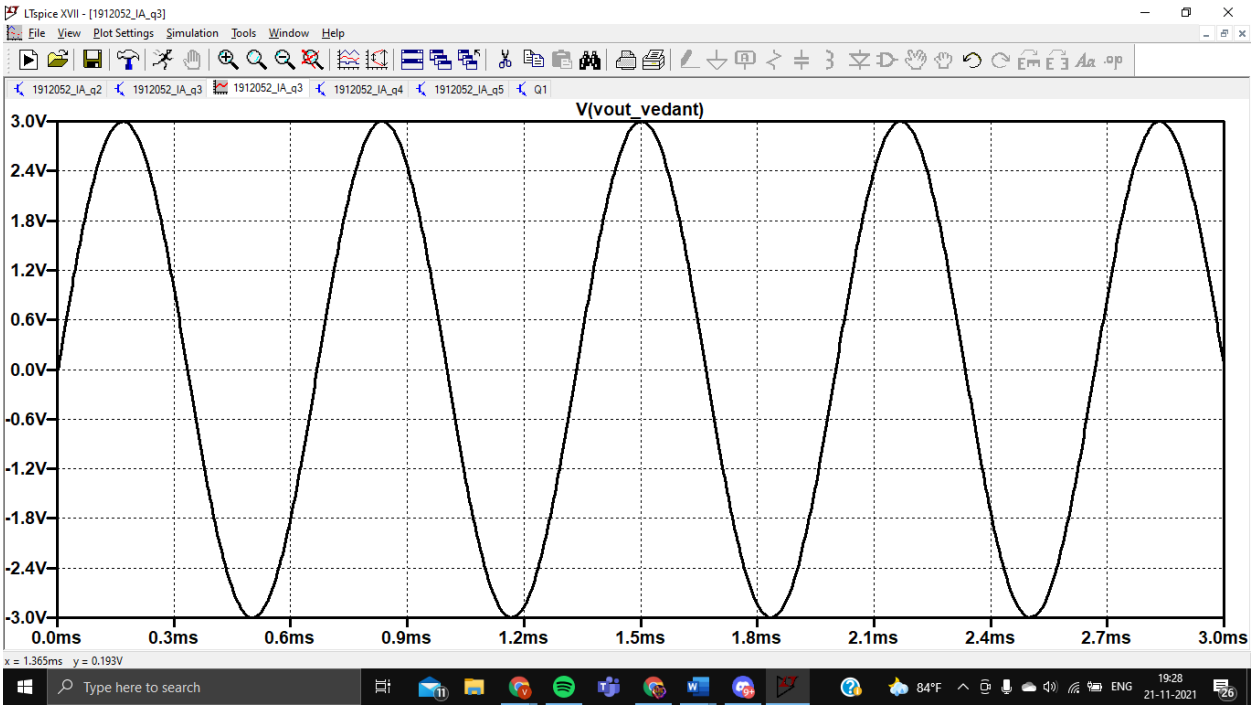
Q3. .Design an non-inverting amplifier for a gain of 15, and with an input impedance of 1.2MΩ **(For Even Roll Numbers)**
1.Design an inverting amplifier for a gain of -9, and with an input impedance of 15kΩ **(For ODD Roll Numbers)**

a to d part remains same for the above question:

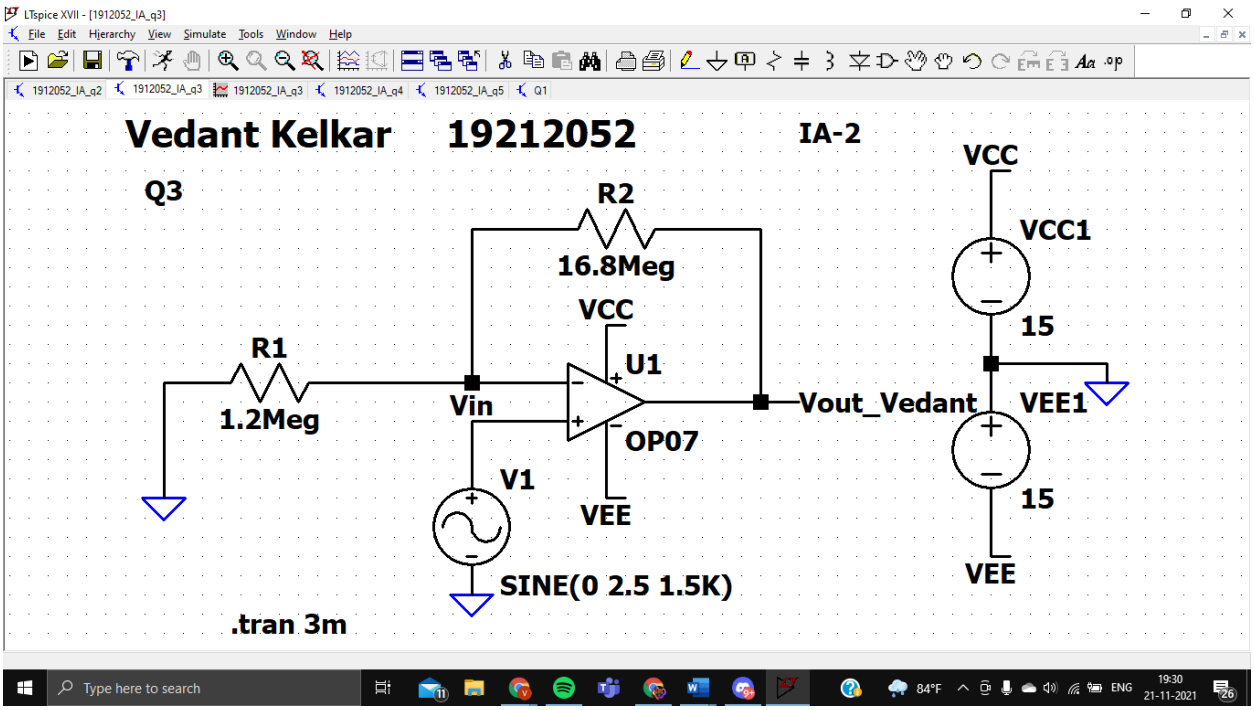
a. Build your designed circuit in LTspice and verify your design values. (One can max Vin = 200mV peak sine wave, f = 1500 Hz
b. Increase Vin to 2.5V peak, keeping frequency same and observe the output waveforms. Record the peak values of output waveforms. Comment on the output obtained.
c. Increase f to 30 KHz , keeping Vin = 200mV peak and observe the output waveforms. Record the peak values of output waveforms. Comment on the output obtained.
d. In a), perform parametric sweep on any one external resistor and obtain 5 simultaneous outputs visible at the same time.

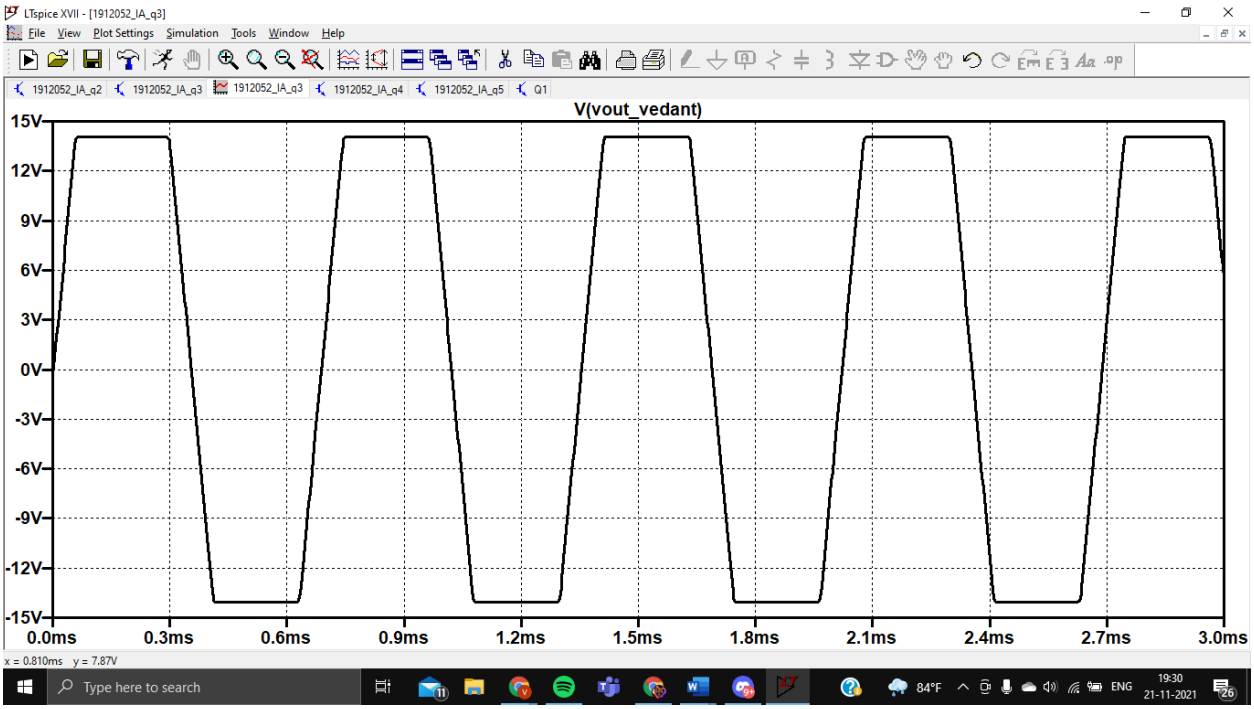
A


LTspice XVII - [1912052_IA_q3]
File Edit Hierarchy View Simulate Tools Window Help
1912052_IA_q2 1912052_IA_q3 1912052_IA_q3 1912052_IA_q4 1912052_IA_q5 Q1
Vedant Kelkar 19212052
IA-2
Q3
R2
16.8Meg
VCC
VCC1
15
R1
1.2Meg
U1
Vin
Vout_Vedant
VEE1
OP07
V1
VEE
15
VEE
SINE(0 200m 1.5K)
.tran 3m
Type here to search
84°F
ENG
19:28
21-11-2021


LTspice XVII - [1912052_IA_q3]
File View Plot Settings Simulation Tools Window Help
1912052_IA_q2 1912052_IA_q3 1912052_IA_q3 1912052_IA_q4 1912052_IA_q5 Q1
V(vout_vedant)
3.0V
2.4V
1.8V
1.2V
0.6V
0.0V
-0.6V
-1.2V
-1.8V
-2.4V
-3.0V
0.0ms
0.3ms
0.6ms
0.9ms
1.2ms
1.5ms
1.8ms
2.1ms
2.4ms
2.7ms
3.0ms
x = 1.365ms y = 0.193V
Type here to search
84°F
ENG
19:28
21-11-2021

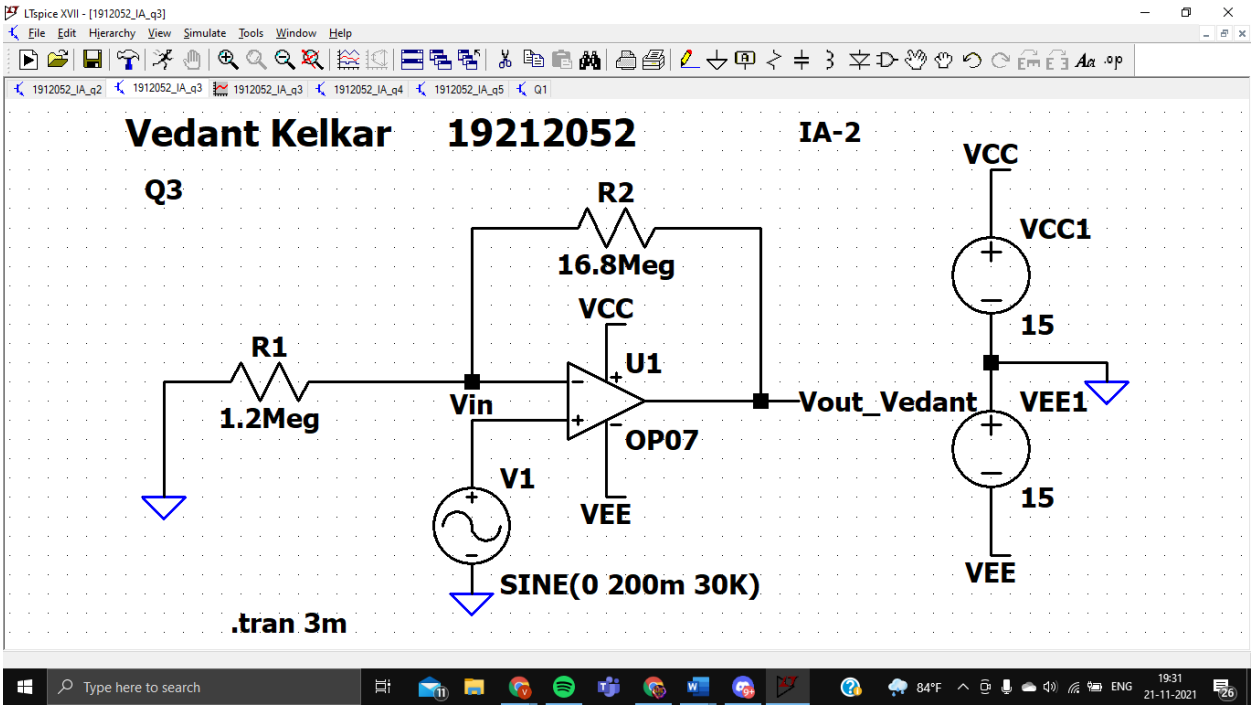
B

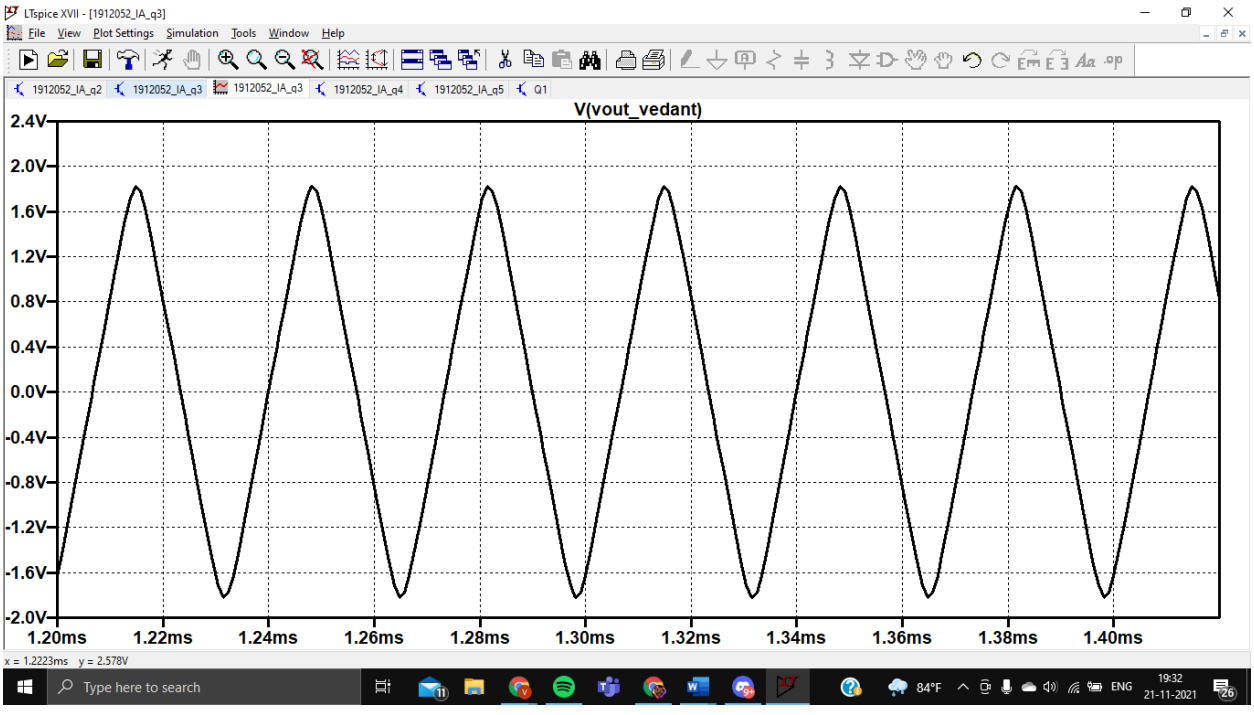

LTspice XVII - [1912052_IA_q3]
File Edit Hierarchy View Simulate Tools Window Help
1912052_IA_q2 1912052_IA_q3 1912052_IA_q3 1912052_IA_q4 1912052_IA_q5 Q1
Vedant Kelkar 19212052
IA-2
Q3
R2
16.8Meg
VCC
VCC1
15
R1
1.2Meg
U1
Vin
Vout_Vedant
VEE1
OP07
V1
VEE
15
VEE
SINE(0 2.5 1.5K)
.tran 3m
Type here to search
84°F
ENG
19:30
21-11-2021



As we can see the output, the waveform of the out gets cut at around +/-14V which is nothing but the Saturation voltage of the Op-Amp.

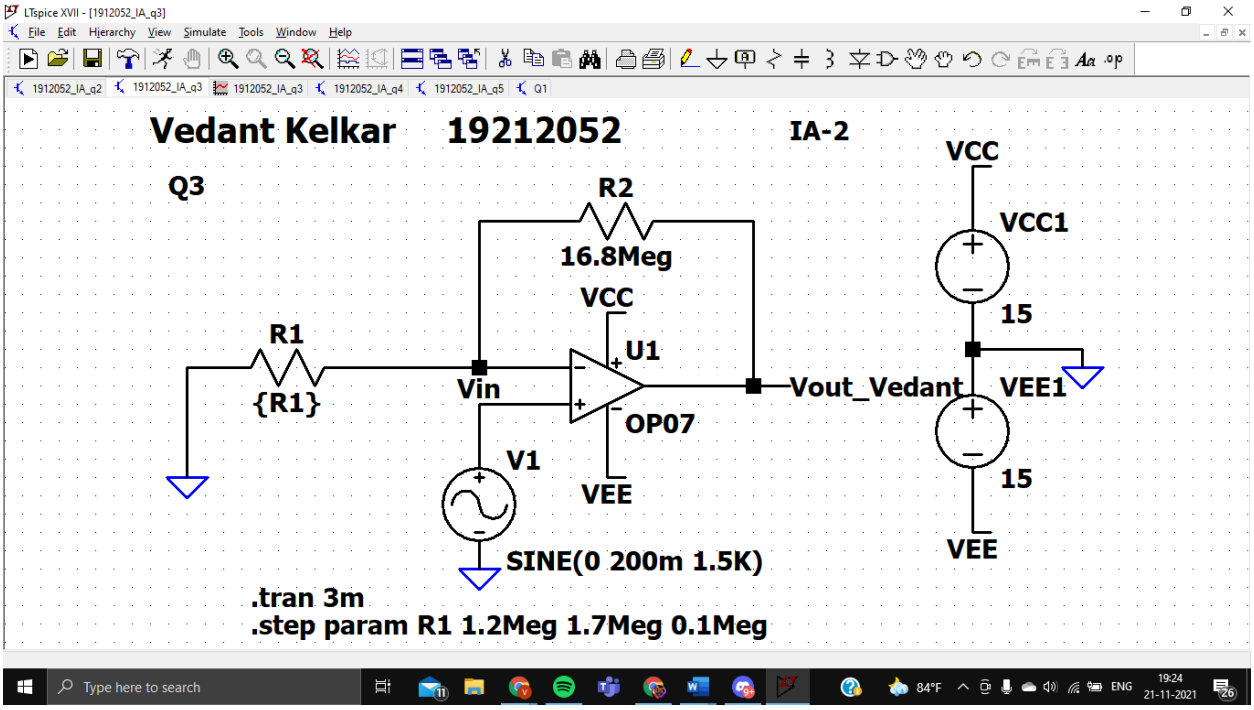
C

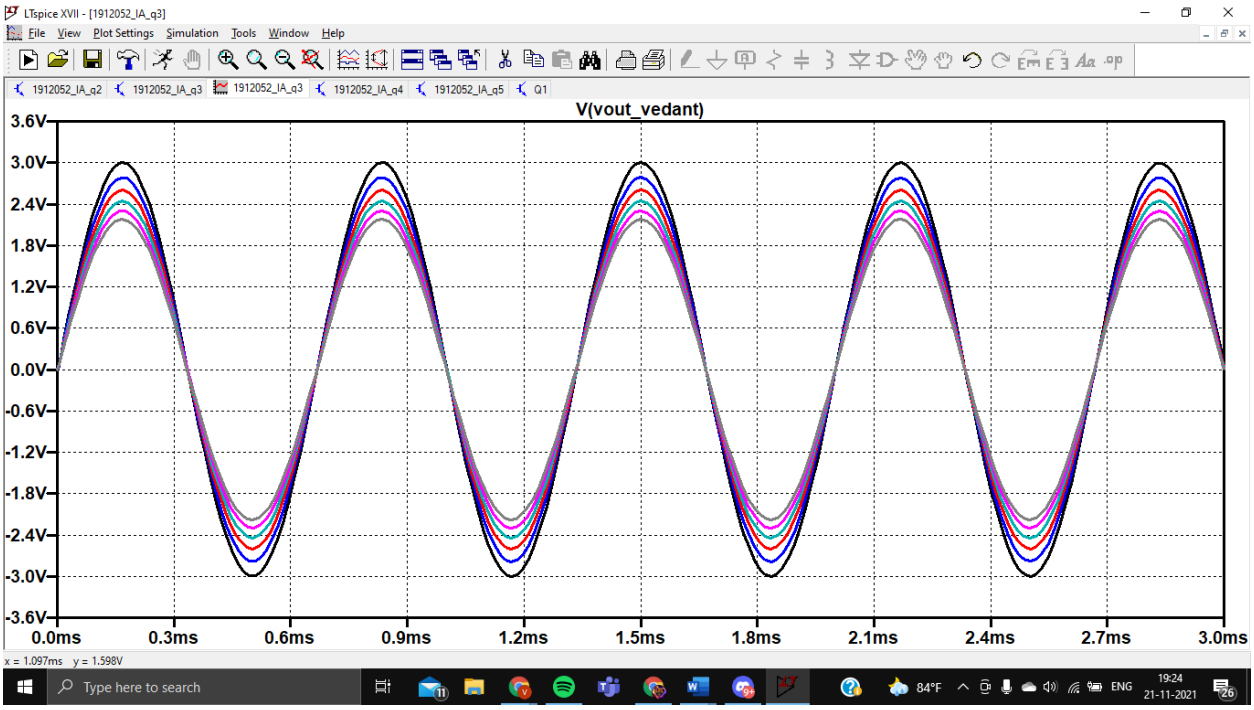

LTspice XVII - [1912052_IA_q3]
File Edit Hierarchy View Simulate Tools Window Help
1912052_IA_q2 1912052_IA_q3 1912052_IA_q3 1912052_IA_q4 1912052_IA_q5 Q1
Vedant Kelkar 19212052
IA-2
Q3
R2
16.8Meg
VCC
R1
1.2Meg
U1
Vin
OP07
Vout_Vedant
VCC
VCC1
15
VEE1
15
VEE
V1
VEE
SINE(0 200m 30K)
.tran 3m
Type here to search
84°F
ENG
19:31
21-11-2021


LTspice XVII - [1912052_IA_q3]
File View Plot Settings Simulation Tools Window Help
1912052_IA_q2 1912052_IA_q3 1912052_IA_q3 1912052_IA_q4 1912052_IA_q5 Q1
V(vout_vedant)
2.4V
2.0V
1.6V
1.2V
0.8V
0.4V
0.0V
-0.4V
-0.8V
-1.2V
-1.6V
-2.0V
1.20ms
1.22ms
1.24ms
1.26ms
1.28ms
1.30ms
1.32ms
1.34ms
1.36ms
1.38ms
1.40ms
x = 1.2223ms y = 2.578V
Type here to search
84°F
ENG
19:32
21-11-2021

As we can see the output, the number of peaks per unit time increases as we increase the frequency

D




LTspice XVII - [1912052_IA_q3]
File View Plot Settings Simulation Tools Window Help
1912052_IA_q2 1912052_IA_q3 1912052_IA_q3 1912052_IA_q4 1912052_IA_q5 Q1
V(vout_vedant)
3.6V
3.0V
2.4V
1.8V
1.2V
0.6V
0.0V
-0.6V
-1.2V
-1.8V
-2.4V
-3.0V
-3.6V
0.0ms 0.3ms 0.6ms 0.9ms 1.2ms 1.5ms 1.8ms 2.1ms 2.4ms 2.7ms 3.0ms
x = 1.097ms y = 1.598V
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84°F
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Name of the student:	Signature of the student:
Vedant kelkar	Vkelkar

Q. No.: Q3

Given gain=15

Input impedence = 1·2M

Gain of non-inverting amplifier

$$\text{Gain} = \frac{1+R_2}{R_1}$$

$$15 = \frac{1+R_2}{R_1}$$

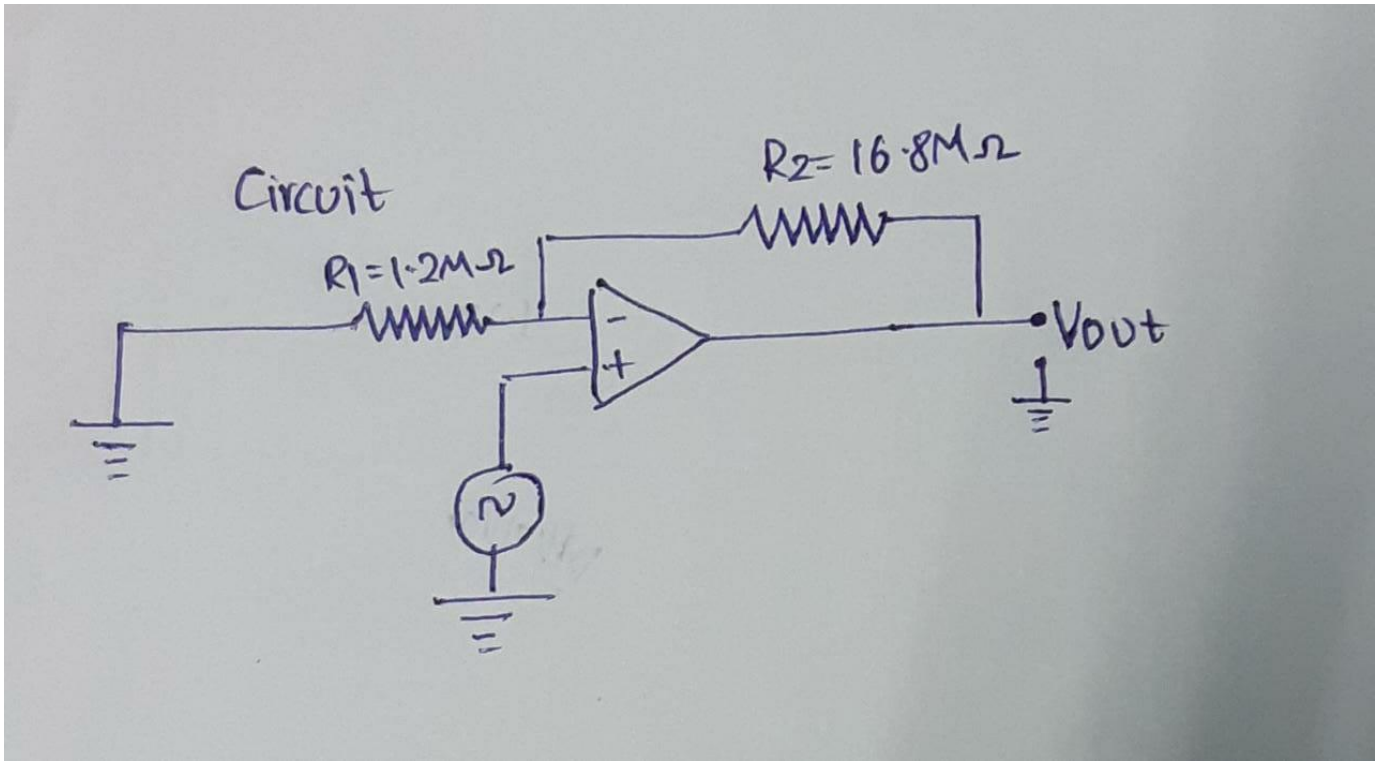
$$14 = \frac{R_2}{R_1}$$

$$R_2 = 14 \cdot R_1$$

$$R_2 = 14(1.2)$$

$$\therefore R_2 = 16.8\ M\Omega$$

∴ Input impedence & Resistive feedback are 1·2MHz & 16·8MΩ.

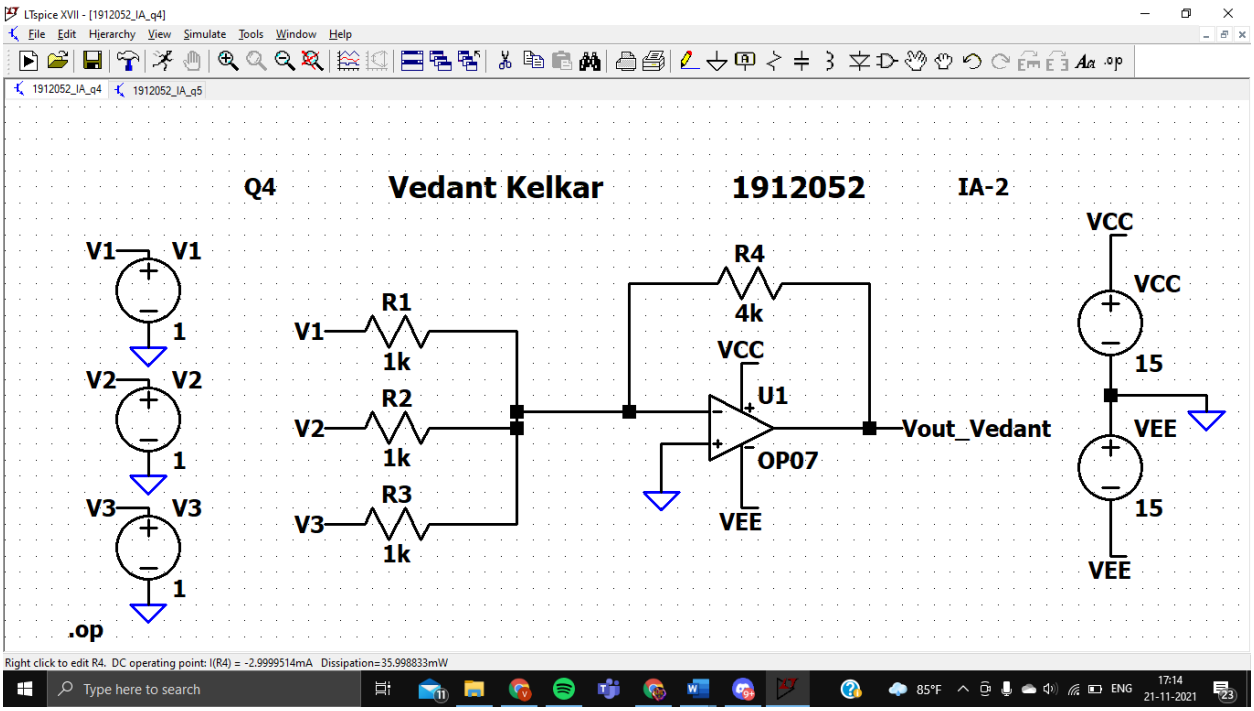

Circuit
R2= 16·8MΩ
R1=1·2MΩ
Vout

Q3 is for 10 marks, Supply voltage can be ±15 V to power up the Opamp OP-07

Q4. Design a summing amplifier to add three input voltages. The output of this circuit must be equal to 4 times the negative sum of the inputs.

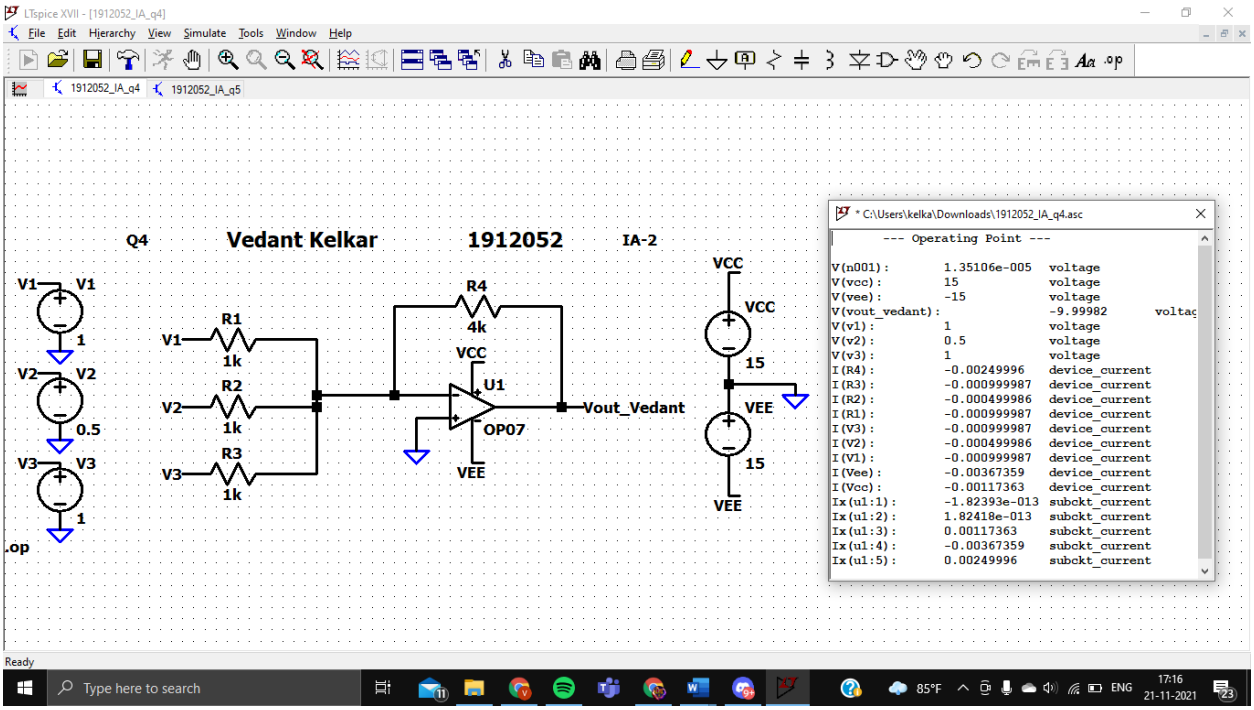
Build your designed circuit in LTspice and verify/validate your design values with at least three set of reading for the inputs. (Attach handwritten solution of design, and printscreen images of schematic & results. Also, prepare observation table for three set of readings)

Q4 is for 10 marks, Supply voltage can be ±15 V to power up the Opamp OP-07
(For all students)



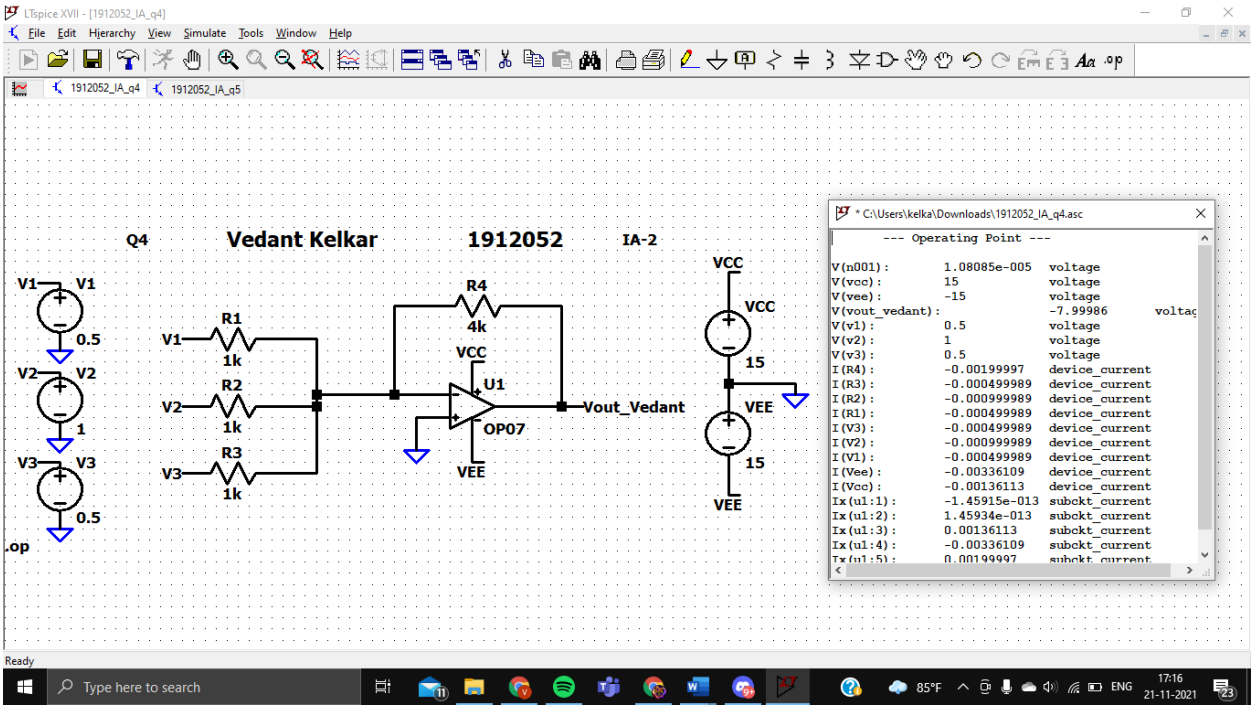
1st reading

Vout=-9.99982V



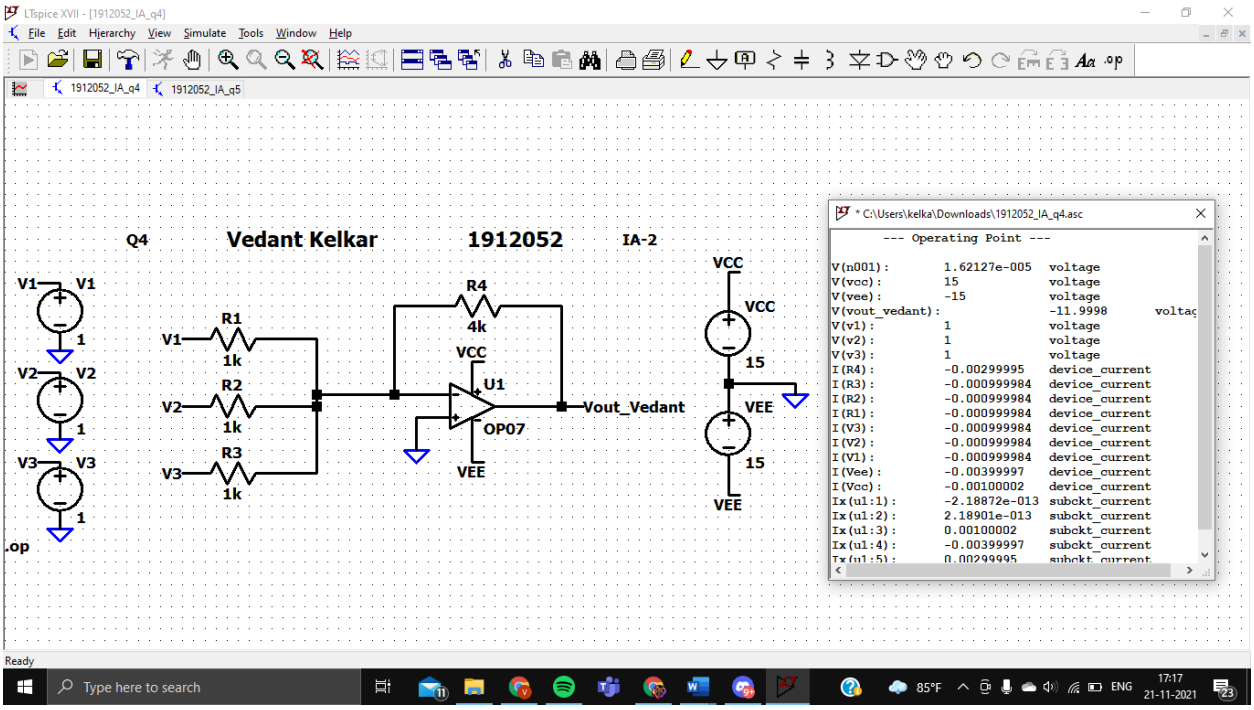
2nd reading

Vout=-7.99986V



3rd reading

Vout= -11.9998V


LTspice XVII - [1912052_IA_q4]
File Edit Hierarchy View Simulate Tools Window Help
1912052_IA_q4
1912052_IA_q5
Q4
Vedant Kelkar
1912052
IA-2
V1
V2
V3
R1
R2
R3
1k
R4
4k
U1
OP07
VCC
VEE
Vout_Vedant
15
.op
C:\Users\kelka\Downloads\1912052_IA_q4.asc
--- Operating Point ---
V(n001): 1.62127e-005 voltage
V(vcc): 15 voltage
V(vee): -15 voltage
V(vout_vedant): -11.9998 voltag
V(v1): 1 voltage
V(v2): 1 voltage
V(v3): 1 voltage
I(R4): -0.00299995 device_current
I(R3): -0.000999984 device_current
I(R2): -0.000999984 device_current
I(R1): -0.000999984 device_current
I(V3): -0.000999984 device_current
I(V2): -0.000999984 device_current
I(V1): -0.000999984 device_current
I(Vee): -0.00399997 device_current
I(Vcc): -0.00100002 device_current
Ix(u1:1): -2.18872e-013 subckt_current
Ix(u1:2): 2.18901e-013 subckt_current
Ix(u1:3): 0.00100002 subckt_current
Ix(u1:4): -0.00399997 subckt_current
Ready
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85°F
ENG
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Vedant kelkar	vkelkar

Q. No.: Q4

Vout expression for summing amplifier:-

$V_{out} = -4[V_1+V_2+V_3]$ ... (1)

where, V_1, V_2 & V_3 are inputs.

$V_{out} = \frac{-R_f}{R}[V_1+V_2+V_3]$ ... (standard Vout for summing amplifier) (2)

where $R = R_1 = R_2 = R_3$

∴ from (1) & (2)

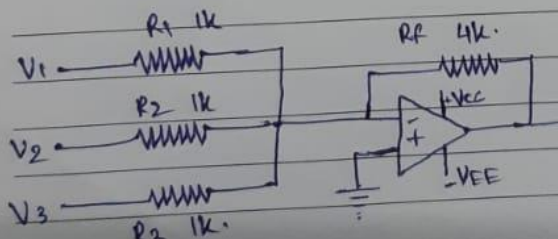
$\frac{-R_f}{R} = -4$ ∴ $\frac{R_f}{R} = 4$

Consider $R = 1k\Omega$

∴ $R_f = 4R$

$R_f = 4k\Omega$

So $V_{out} = -4[V_1+V_2+V_3]$



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Vedant kelkar	Vkelkar

Q. No.:_____

Calculations

→ $V_1 = 1V$, $V_2 = 0.5V$, $V_3 = 1V$

$V_{out} = -4(1+0.5+1) = -10V$

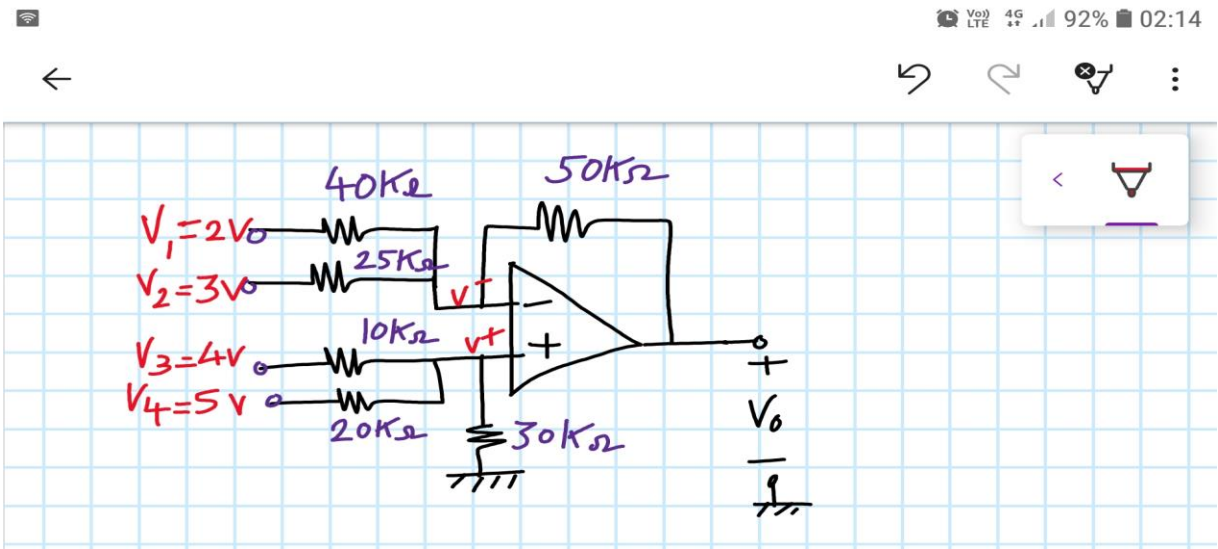
→ $V_1 = 0.5V$, $V_2 = 1V$, $V_3 = 0.5V$

$V_{out} = -4(0.5+1+0.5) = -8V$

→ $V_1 = 1V$, $V_2 = 1V$, $V_3 = 1V$

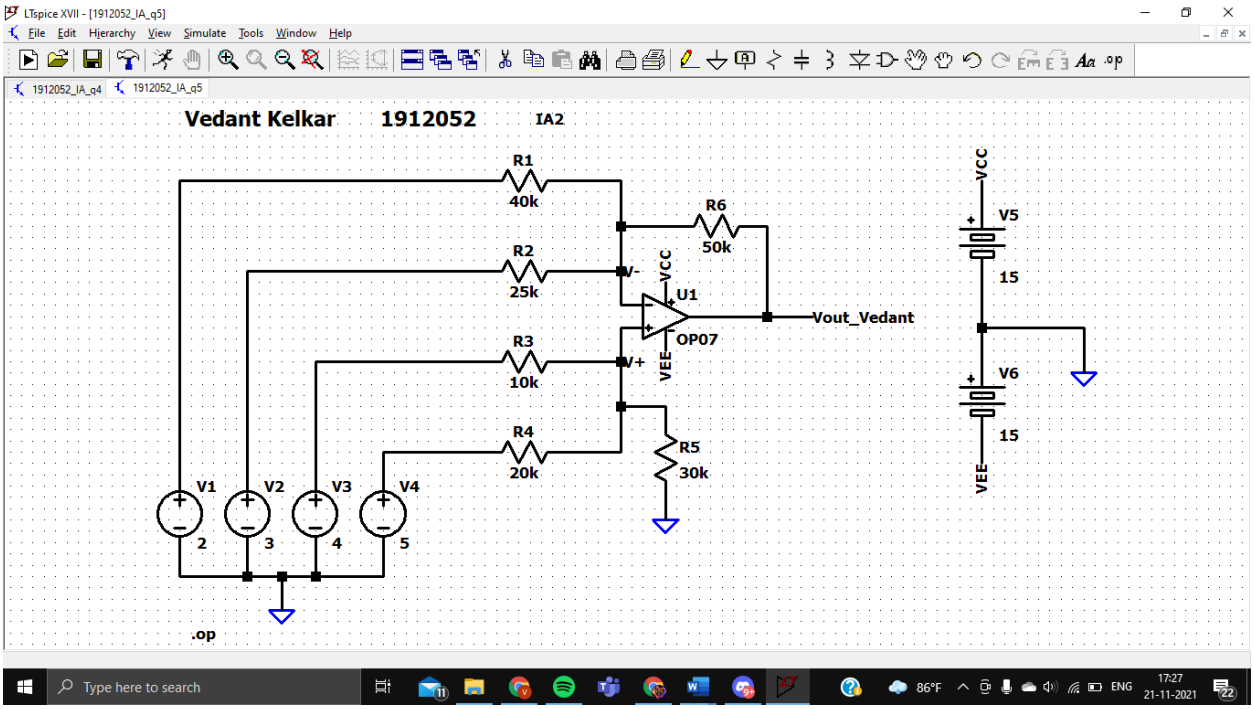
$V_{out} = -4(1+1+1) = -12V$

Q5. Find V_0 for the adder-subtractor circuit shown . **(For all students)**



Build your designed circuit in LTspice and verify/validate your design values. (Attach handwritten solution of design, and printscreen images of schematic & results)

Q5 is for 10 points, Supply voltage can be ±15 V to power up the Opamp OP-07


LTspice XVII - [1912052_IA_q5]
File Edit Hierarchy View Simulate Tools Window Help
1912052_IA_q4
1912052_IA_q5
Vedant Kelkar
1912052
IA2
R1
40k
R2
25k
R3
10k
R4
20k
R5
30k
R6
50k
V1
V2
V3
V4
2
3
4
5
V-
V+
VCC
VEE
U1
OP07
Vout_Vedant
V5
15
V6
15
.op
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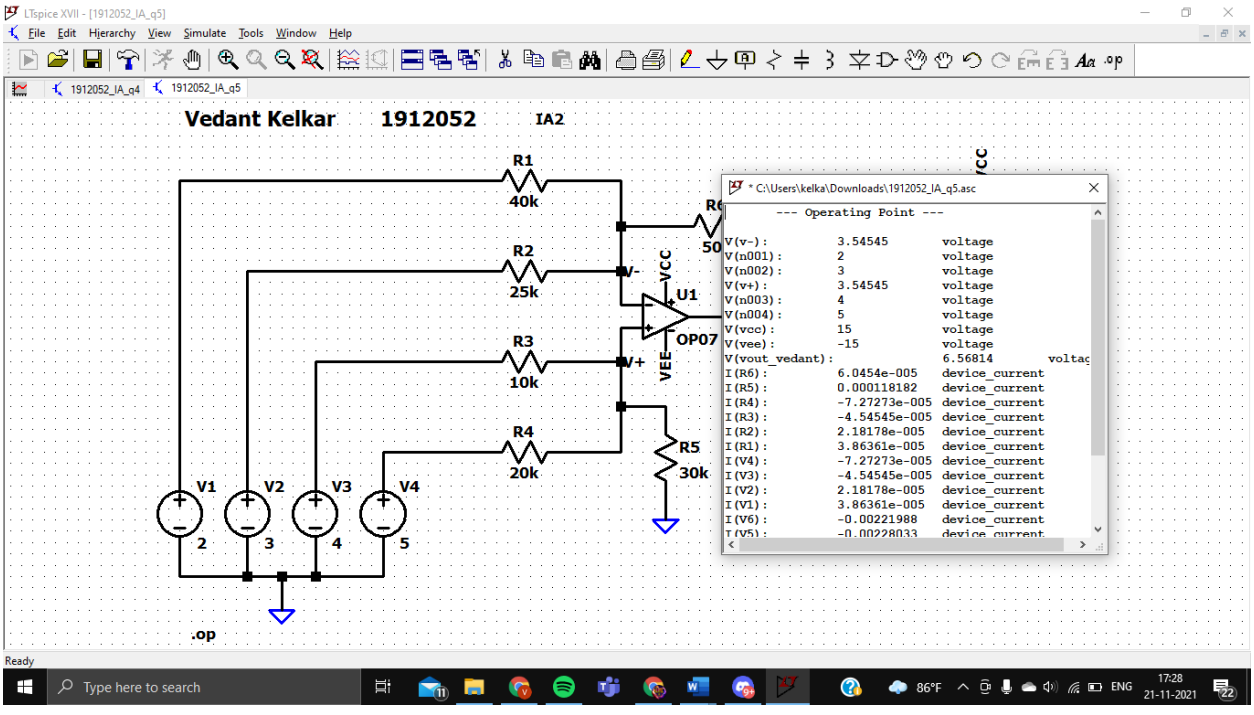
LTspice XVII - [1912052_IA_q5]
File Edit Hierarchy View Simulate Tools Window Help
1912052_IA_q4
1912052_IA_q5
Vedant Kelkar
1912052
IA2
R1
40k
R2
25k
R3
10k
R4
20k
R5
30k
V1
V2
V3
V4
2
3
4
5
V-
V+
VCC
VEE
U1
OP07
.op
C:\Users\kelka\Downloads\1912052_IA_q5.asc
--- Operating Point ---
V(v-): 3.54545 voltage
V(n001): 2 voltage
V(n002): 3 voltage
V(v+): 3.54545 voltage
V(n003): 4 voltage
V(n004): 5 voltage
V(vcc): 15 voltage
V(vee): -15 voltage
V(vout_vedant): 6.56814 voltage
I(R6): 6.0454e-005 device_current
I(R5): 0.000118182 device_current
I(R4): -7.27273e-005 device_current
I(R3): -4.54545e-005 device_current
I(R2): 2.18178e-005 device_current
I(R1): 3.86361e-005 device_current
I(V4): -7.27273e-005 device_current
I(V3): -4.54545e-005 device_current
I(V2): 2.18178e-005 device_current
I(V1): 3.86361e-005 device_current
I(V6): -0.00221988 device_current
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ENG
17:28
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Vout= `6.56814` **V (simulated)**

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Name of the student: Vedant Kelkar

Signature of the student: Vkelkar

Q. No.: Q5.

at V^- (KCL) at inverting terminal

$$\frac{V^- - 2}{40} + \frac{V^- - 3}{25} + \frac{V^- - V_{out}}{50} = 0$$

$$V^-\left[\frac{1}{40} + \frac{1}{25} + \frac{1}{50}\right] - \frac{2}{40} - \frac{3}{25} - \frac{V_{out}}{50} = 0$$

$$V^-\left[\frac{17}{200}\right] - \frac{V_{out}}{15} = \frac{17}{100} \quad \text{①}$$

now at V^+ (KCL) at non-inverting terminal.

$$\frac{V^+ - 4}{10} + \frac{V^+ - 5}{20} + \frac{V^+ - 0}{30} = 0$$

$$\therefore V^+\left[\frac{1}{10} + \frac{1}{20} + \frac{1}{30}\right] - \frac{4}{10} - \frac{5}{20} = 0 \qquad \therefore V^+\left(\frac{11}{60}\right) = \frac{13}{20}$$

$$V^+ = \left[\frac{39}{11}\right] \quad \ldots \text{(According to virtual-short, voltage at the inverting terminal is equal to the Vat the non-inverting terminal)}$$

$$\therefore V^- = V^+ = \frac{39}{11} V$$

$$\frac{39}{11}\left[\frac{17}{200}\right] - \frac{V_{out}}{50} = \frac{17}{100}$$

$$\frac{289}{2200} = \frac{V_{out}}{50}$$

$$V_{out} = 6.56$$