Design Style #2 Moore

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```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
-------------------------------------------------------
ENTITY <ent_name> IS
   PORT (input: IN <data_type>;
         reset, clock: IN STD_LOGIC;
         output: OUT <data_type>);
END <ent_name>;
-------------------------------------------------------
ARCHITECTURE <arch_name> OF <ent_name> IS
   TYPE states IS (state0, state1, state2, state3, ...);
   SIGNAL pr_state, nx_state: states;
   SIGNAL temp: <data_type>;
BEGIN
   ---------- Lower section: --------------------------
   PROCESS (reset, clock)
   BEGIN
      IF (reset='1') THEN
         pr_state <= state0;
      ELSIF (clock'EVENT AND clock='1') THEN
         output <= temp;
         pr_state <= nx_state;
      END IF;
   END PROCESS;

    ---------- Upper section: --------------------------
    PROCESS (pr_state)
   BEGIN
      CASE pr_state IS
         WHEN state0 =>
            temp <= <value>;
            IF (condition) THEN nx_state <= state1;
            ...
            END IF;
         WHEN state1 =>
            temp <= <value>;
            IF (condition) THEN nx_state <= state2;
            ...
            END IF;
         WHEN state2 =>
            temp <= <value>;
            IF (condition) THEN nx_state <= state3;
            ...
            END IF;
         ...
      END CASE;
   END PROCESS;
END <arch_name>;
```

o/p is before the if statement
i.e. after the state statement