Helium v1.1
User manual

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For any queries or support, contact the CPLD team at
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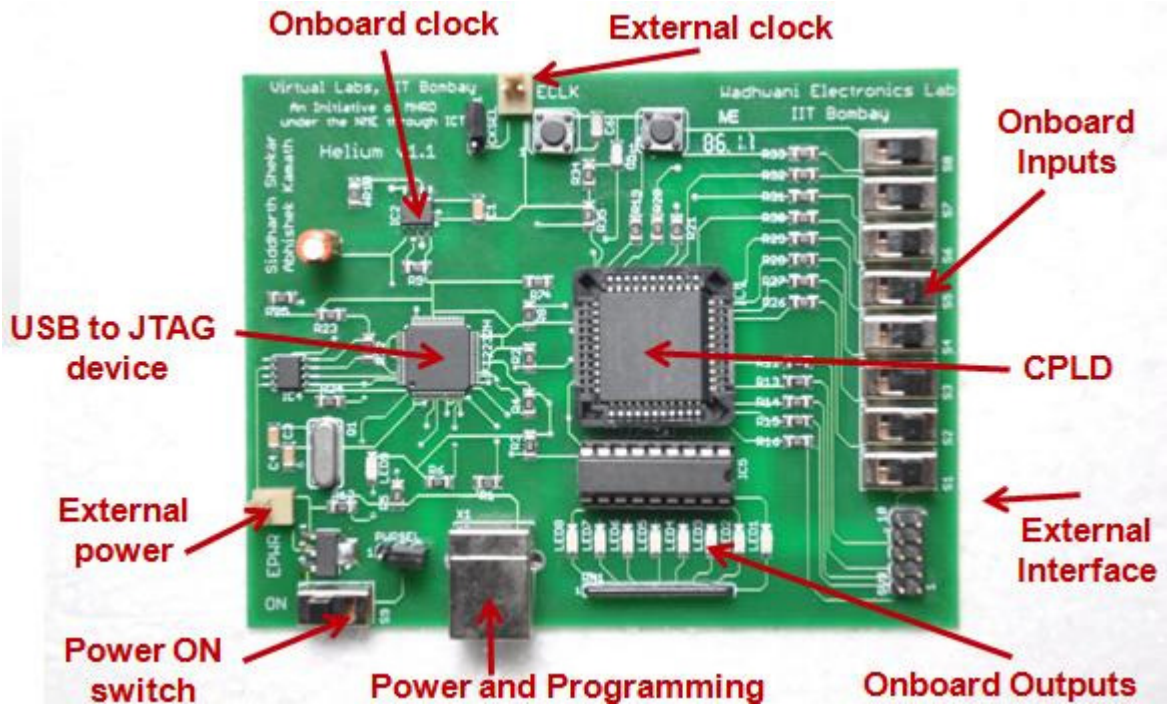
Board Details:



Features:

- Based on Altera MAX 3000 architecture.
- Device used on board: EPM3064A (1250 usable gates).
- **Powered and Programmed through USB.**
- 8 inputs and 8 outputs onboard.
- 8 user configurable I/O pins for interfacing to external circuitry.
- Onboard clock of 1Hz.

Note:

- *Do not touch any IC with your hands as they may be damaged due to electrostatic discharge.*
- *When using an external supply to power the board, use only a single regulated +5V DC supply.*

Initial Board Settings:

Two jumpers need to be set on the board prior to setup.

1. **PWRSEL:** The power select jumper. It is located close to the USB connector on the board.

Pins	Mode
Pins 1 & 2	Externally powered
Pins 2 & 3	USB powered

The connector for the **external supply** can be found close to the to the PWRSEL jumper with the power polarities indicated. Use only +5V DC supply for external supply.

2. **CKSEL:** The clock select jumper. It is located close to the CPLD.

Pins	Mode
Pins 1 & 2	Onboard clock
Pins 2 & 3	External clock

The connector for the external clock (ECLK) can be found close to the to the CKSEL jumper.

Installing the Drivers:

1. Plug in the USB connector to both the board and the PC. The board would be powered ON and the power LED should glow.
2. The **"Found new hardware"** wizard will open, which prompts a dialog-box.
3. Select **"No, not this time"** and click **"Next".**
4. Select **"Install from a specific location"**, and click next.
5. Navigate to the folder containing the CDM drivers. The drivers are provided on the CD and are also available on FTDI's website.
6. The drivers will be installed.
7. This process will run four times- one each for Serial Converter A, B, and twice for the two serial ports.

It is recommended that you keep a copy of the drivers in your computer. You may be prompted for the drivers again if a different board is connected.

Using Altera Quartus:

1. Create a new project from File » New Project Wizard.
2. The project name and the top level design entity should have the same name.
3. Follow the onscreen instructions to create a new project. An existing VHDL/ Verilog file can be added to the project if a program file has been already written or else, it may be left blank if you wish to create a new VHDL/ Verilog file in the current project directory.
4. Select the programmable device family as MAX3000A, and EPM3064ALC44-10N from the device list that shows up.
5. Open a new VHDL/ Verilog file and write the program, in case a new file is to be complied.
6. Compile the design and rectify errors, if any.
7. Once the design is compiled, you can choose what pins to assign as input/output from "Pin Planner" under the Assignments tab in the Menu bar. Refer to the last section for the I/O pin configuration.
8. Re-run the compiler and make sure that there are no errors.
9. To generate the '.svf' file, select 'Programmer' under the Tools tab in the Menu bar. Check if the device EPM3064ALC44-10N is recognized in the programmer window.
10. Select the file type as '.svf' and click 'Generate'.

The entire process described above has been demonstrated in the video tutorial which can be found on the CD accompanying the board.
For more information on VHDL/Verilog and using Quartus, refer to the Virtual Lab website.

Programming the CPLD:

1. Open the JTAG shell in the UrJTAG folder. In case the JTAG shell doesn't start and reports an error saying the "libusb.dll" missing, copy the file from the CD and past it in the system32 folder in the Windows directory. This should solve the error.
2. At the command prompt, type **"cable ft2232"**.
3. You will get a message saying **"connected to libd2xx"**.
4. The **"detect"** command should identify the CPLD device and display its signature.
5. In case you have other devices connected to the JTAG chain, you can choose the appropriate device by specifying the corresponding part number. This is **optional** in this case, as only one device is present in the JTAG chain. Since the CPLD is the only device in the JTAG chain, you can select it by typing the **"part 0"** command.
6. Type **"svf <svf file location>"** on the command prompt. The file will now be loaded, and the output of the VHDL/ Verilog program may be observed on the board.

I/O configuration:

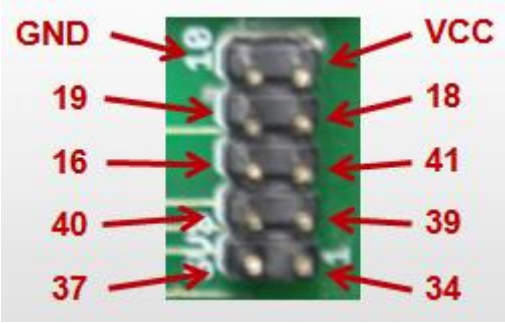
The pins which have been configured as input and output on the board are as follows:

Inputs	Pin No.
SW1	4
SW2	5
SW3	6
SW4	8
SW5	9
SW6	11
SW7	12
SW8	14

Outputs	Pin No.
LED1	24
LED 2	25
LED 3	26
LED 4	27
LED 5	28
LED 6	29
LED 7	31
LED 8	33

External I/O:

The following pins are available for interfacing the board with external hardware.
PIN 16, 18, 19, 34, 37, 39, 40 and 41.



It is recommended to use external power supply of +5V when interfacing external hardware to the board.

Clock:

For using the onboard clock, map your clock input to pin 43 of the CPLD which is the Global Clock of the CPLD.

Links for downloading software:

1. http://www.altera.com/download/software/quartus-ii-we (Download the Web Edition v10.1 or later. You may be required to register on the website.)
2. http://urjtag.org (It is available free!! No registration required.)