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| **Course Name:** | **Hardware Description Language Lab (2UXL401)** | **Semester:** | **IV** |
| **Date of Performance:** | **07 / 05 / 2021** | **Batch No:** | **B2** |
| **Faculty Name:** | **Prof. Bhargavi Kaslikar** | **Roll No:** | **1912060** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** |  |

**Experiment No: 10**

**Title:** Mini Project

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| **Aim and Objective of the Experiment:** |
| Write your problem statement for Mini Project:   * Design a Vending Machine using FSM in VHDL to dispense the item bought(y) and the change(x).   Explain Objective of the Project   * Applying the knowledge of finite state machines to build a application based project in VHDL. |

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| **COs to be achieved:** |
| **CO 1**: Use basic Concurrent and Sequential statements in VHDL and write codes for simple applications  **CO 2**: Test a VHDL code and verify the circuit model.  **CO 3:** Synthesize and Implement the designed circuits on CPLD/ FPGA. |

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| **Work to be done** |
| Upload VHDL codes. Also upload test bench and simulation for the project. Write comments at appropriate places in your code. |
| Main Code: |
| -- MINI PROJECT  -- ROLL NUMBER - 1912052 - VEDANT KELKAR  -- 1912060 - NACHIKET NAIK  library ieee;  use ieee.std\_logic\_1164.all;  entity miniPro is  port(  i,j,Clk : in std\_logic;  x,y : out std\_logic  );  end miniPro;  architecture miniPro\_arch of miniPro is  type state\_type is (a,b,c);  signal next\_s : state\_type;  begin process(Clk)  begin  if(rising\_edge(Clk)) then  case next\_s is  when a =>  if(i='0' and j='0') then  x <= '0';  y <= '0';  next\_s <= a;  elsif(i='1' and j='0') then  x <= '0';  y <= '0';  next\_s <= b;  elsif(i='1' and j='1') then  x <= '0';  y <= '0';  next\_s <= c;  end if;  when b =>  if(i='0' and j='0') then  x <= '0';  y <= '0';  next\_s <= b;  elsif(i='1' and j='0') then  x <= '0';  y <= '0';  next\_s <= c;  elsif(i='1' and j='1') then  x <= '1';  y <= '0';  next\_s <= a;  end if;  when c =>  if(i='0' and j='0') then  x <= '0';  y <= '0';  next\_s <= c;  elsif(i='1' and j='0') then  x <= '1';  y <= '0';  next\_s <= a;  elsif(i='1' and j='1') then  x <= '1';  y <= '1';  next\_s <= a;  end if;  end case;  end if;  end process;  end miniPro\_arch; |
| Testbench: |
| -- MINI PROJECT  -- ROLL NUMBER - 1912052 - VEDANT KELKAR  -- 1912060 - NACHIKET NAIK  library ieee;  use ieee.std\_logic\_1164.all;  entity miniPro\_tb is  end miniPro\_tb;  architecture miniPro\_tb\_arch of miniPro\_tb is    component miniPro  port(  i,j,Clk : in std\_logic;  x,y : out std\_logic  );  end component;    signal Clk,x,y,i,j : std\_logic := '0';    begin  uut: miniPro port map (i,j,Clk);    process  begin  Clk <= '0';  wait for 5 ns;  Clk <= '1';  wait for 5 ns;  end process;    process  begin  wait for 20 ns;  i <= '0';j <= '0'; wait for 20 ns;  i <= '0';j <= '1'; wait for 10 ns;  i <= '1';j <= '0'; wait for 10 ns;  i <= '1';j <= '1'; wait for 10 ns;  i <= '0';j <= '0'; wait for 10 ns;  i <= '0';j <= '1'; wait for 20 ns;  i <= '1';j <= '1'; wait for 10 ns;  i <= '1';j <= '0'; wait for 10 ns;  i <= '0';j <= '0'; wait for 10 ns;  i <= '0';j <= '1'; wait for 10 ns;  i <= '1';j <= '1'; wait for 10 ns;  i <= '1';j <= '1'; wait for 10 ns;  i <= '1';j <= '0'; wait for 20 ns;  i <= '1';j <= '1'; wait for 10 ns;  wait;  end process;  end miniPro\_tb\_arch; |
| Output Waveform: |
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| RTL Viewer: |
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| State Machine viewer: |
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| **Conclusion:** |
| **Thus, we have simulated a vending machine using FSM and VHDL. We have used a Mealy machine for the state machine.** |

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| **Signature of faculty in-charge with Date:** |