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2022VST9504

50 point FFT (mix radix 2 and radix 5) - with precision of [sign + 15bits] {Sign + 2(integer) +13(fractional)}

1. Introduction

In the realm of signal processing and data analysis, the Fast Fourier Transform (FFT) stands as a cornerstone technique, allowing us to delve into the frequency components of discrete data. The FFT is vital in a myriad of applications, ranging from audio signal processing to image analysis and beyond. This project centers on the development and implementation of a 50-point FFT, characterized by a unique combination of radix-2 and radix-5 algorithms, all while adhering to a specific precision format of [sign + 15 bits] {Sign + 2 (integer) + 13 (fractional)}.

The Fast Fourier Transform, or FFT, is a computationally efficient algorithm used to transform time-domain data into the frequency domain. This transformation is instrumental in uncovering the underlying patterns and spectral information within the data. The significance of the FFT cannot be overstated, as it underpins numerous applications, from audio compression to seismic data analysis, and is pivotal in modern technologies like digital signal processing and telecommunications.

The primary objectives of this project include:

1. Implementing a 50-point FFT algorithm.
2. Combining radix-2 and radix-5 algorithms to optimize computational efficiency.
3. Ensuring that the computed FFT results conform to the specified precision format of [sign + 15 bits] {Sign + 2 (integer) + 13 (fractional)}.
4. ASIC Synthesis.
5. Testability analysis.

1.1 Referenced documents

- *R. Singleton, ”An algorithm for computing the mixed radix fast Fourier transform,” in IEEE Transactions on Audio and Electroacoustics, vol. 17, no. 2, pp. 93-103, June 1969.*
- *G. L. DeMuth, ”Algorithms for defining mixed radix FFT flow graphs,” in IEEE Transactions on Acoustics, Speech, and Signal Processing, vol. 37, no. 9, pp. 1349-1358, Sept. 1989,*
- *"Verilog HDL: A Guide to Digital Design and Synthesis" by Samir Palnitkar.*
- *The Fast Fourier Transform And Its Applications by* E. Oran Brigham

1.2 Design library name

UMC65

2. Function

The 50-point FFT serves as the key computational component, responsible for transforming time-domain data into the frequency domain. Its primary functions and importance can be summarized as follows:

1. Frequency Domain Analysis: The central function of the 50-point FFT is to provide insights into the frequency components of a discrete data sequence. By computing the FFT, we can extract information about the amplitudes and phases of sinusoidal components at various frequencies present in the input data.

2. Signal Decomposition: The 50-point FFT algorithm dissects the input data into its constituent sinusoidal components. This decomposition is particularly valuable in applications where understanding the spectral content of signals is crucial. For instance, in audio processing, it enables us to separate individual audio frequencies from complex sound waves.

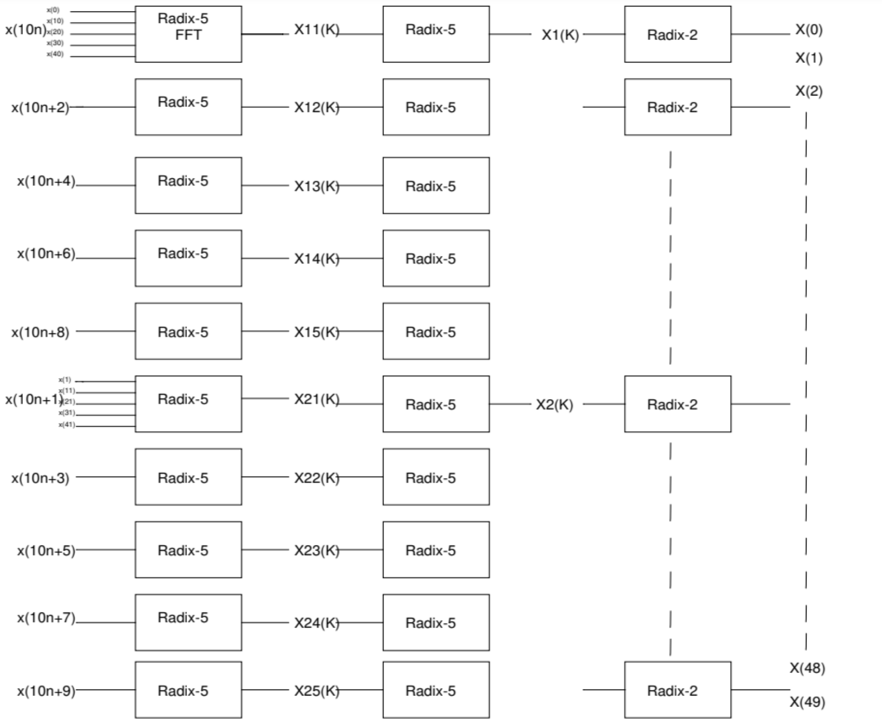
3. Precision: The 50-point FFT, in this project, is designed to adhere to a specific precision format of [sign + 15 bits] {Sign + 2 (integer) + 13 (fractional)}. This precision is critical in ensuring the accuracy of the computed frequency domain information, particularly in applications where fine-grained spectral analysis is required.

4. Integration into Larger Framework: The 50-point FFT acts as a fundamental building block within this project. It is the bridge that connects the raw input data with the frequency domain analysis. Its precision and efficiency attributes make it suitable for real-world applications that demand accurate signal analysis.

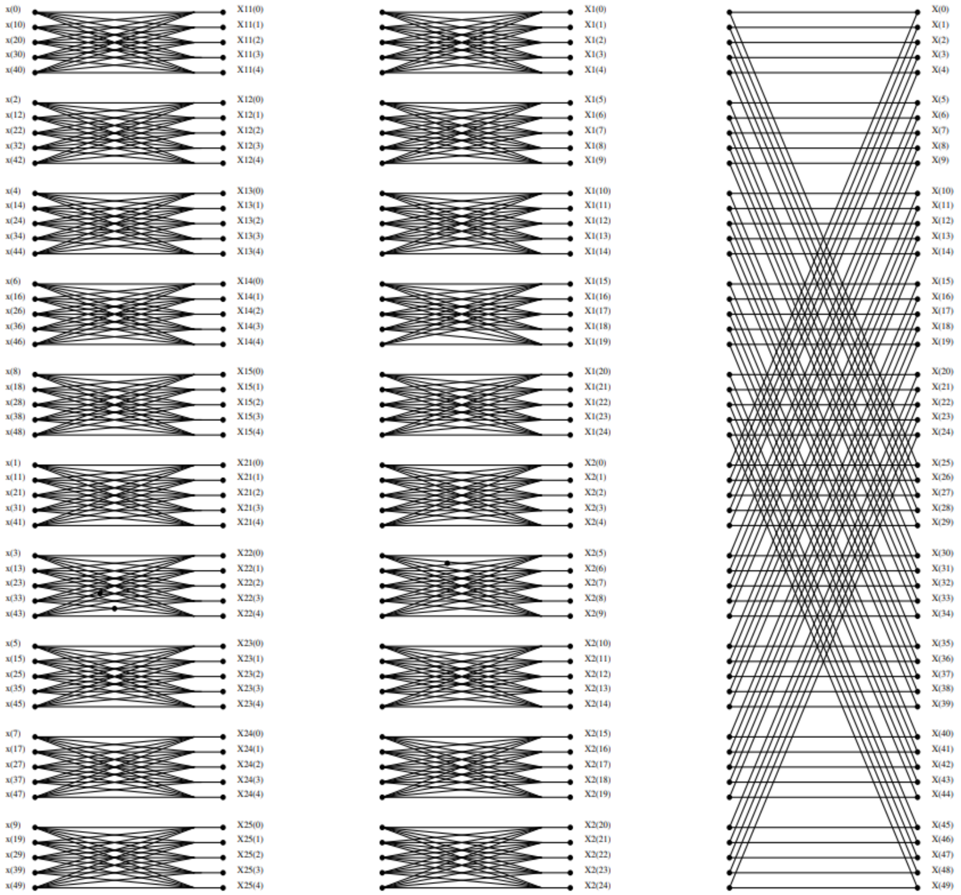
2.1 Architecture

The architecture section offers a comprehensive view of the design and structure of the 50-point FFT (Fast Fourier Transform) implementation, incorporating a mix of radix-2 and radix-5 algorithms. Radix-2 and Radix-5: The architectural foundation of this project is the amalgamation of the radix-2 and radix-5 algorithms. Radix-2 is utilized for its computational efficiency when dealing with power-of-two-sized transforms. Radix-5 is selectively integrated to optimize the efficiency of the 50-point transform.

50 point FFT using radix-2 and radix-5

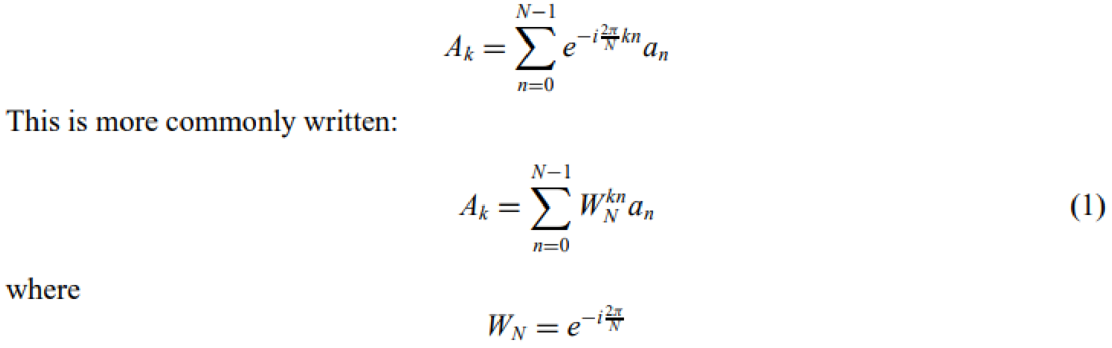


Butterfly Diagram for 50 point FFT using radix-2 and radix-5



2.2 Principle of DFT(Discrete Fourier Transform) and FFT

When a signal is discrete and periodic, we don’t need the continuous Fourier transform. Instead we use the discrete Fourier transform, or DFT. Suppose our signal is an for n = 0 ... N − 1, and an = an+ jN for all n and j. The discrete Fourier transform of a, also known as the spectrum of a, is:



$$A_k = \sum_{n=0}^{N-1} e^{-i\frac{2\pi}{N}kn} a_n$$

This is more commonly written:

$$A_k = \sum_{n=0}^{N-1} W_N^{kn} a_n \tag{1}$$

where

$$W_N = e^{-i\frac{2\pi}{N}}$$

and Wk N for k = 0 ... N − 1 are called the Nth roots of unity. The FFT is a fast algorithm for computing the DFT. If we take the 2-point DFT and 4-point DFT and generalize them to 8-point, 16-point, ..., 2r -point, we get the FFT algorithm. To compute the DFT of an N-point sequence using equation (1) would take O(N2) multiplies and adds. The FFT algorithm computes the DFT using O(N log N) multiplies and adds.

2.3 Detailed functional description

Functional Checklists and Description:

- **Input Data Handling**:

The 50-point FFT begins with the input data, a sequence of 50 discrete points in the time domain, typically represented as a one-dimensional array.
The input data may undergo pre-processing steps as needed, such as windowing functions to reduce spectral leakage.

- **Radix-2 and Radix-5 Algorithms:**

The architecture employs a combination of radix-2 and radix-5 algorithms, each with distinct roles:

Radix-2 Algorithm*:* Used for efficiently handling transforms of sizes that are powers of two, including intermediate stages of the 50-point FFT.

Radix-5 Algorithm: Selectively integrated to handle composite-sized FFTs, such as the 50-point FFT, optimizing computational efficiency.

- **Data Decomposition:**

Within the 50-point FFT, the input data is decomposed into its constituent frequency components. This decomposition is achieved through a recursive process of dividing the input data into smaller segments, allowing for efficient computation.

- **Twiddle Factor Computation:**

The FFT involves complex exponentials known as twiddle factors. These factors are pre-computed and stored for various stages of the FFT, reducing redundant calculations and enhancing performance.

- **Butterfly Operations:**

The core operation of the FFT is the butterfly operation. This operation combines pairs of data points, applying twiddle factors to calculate the complex spectral components. The butterfly operation is performed iteratively, merging data points in a "butterfly" pattern.

- **Output Generation:**

The output of the 50-point FFT consists of a frequency domain representation of the input data. It provides information about the amplitude and phase of sinusoidal components at different frequencies.
In the specified precision format of [sign + 15 bits] {Sign + 2 (integer) + 13 (fractional)}, the output values are stored as fixed-point numbers with 15 bits, comprising 2 integer bits and 13 fractional bits.

- **Complexity and Computational Efficiency:**

The choice of a mixed radix-2 and radix-5 approach allows for optimized computational efficiency. The radix-2 algorithm is leveraged for its simplicity and speed in handling power-of-two transforms, while radix-5 components are applied to efficiently manage composite-sized FFTs like the 50-point FFT.

- **Precision Maintenance:**

Throughout the computation, the architecture maintains the precision format of [sign + 15 bits] {Sign + 2 (integer) + 13 (fractional)}. This precision ensures that the computed results meet the specified accuracy requirements, making it suitable for applications where precise spectral analysis is crucial.

3. Design parameters

3.1 Performance Requirements:Clock Frequency150MHz

3.2 Clock Distribution

N/A

3.3 Reset

N/A

3.4 Timing Description

N/A

4. Verification Strategy:-

4.1 Functional Verification:

Theoretical Analysis:

Conducted a thorough review of the underlying mathematical foundations of the radix-2 and radix-5 algorithms employed in the 50-point FFT. Confirmed the precision maintenance throughout the algorithm, ensuring that the output adheres to the specified [sign + 15 bits] {Sign + 2 (integer) + 13 (fractional)} format.

Simulation: Implemented a suite of test cases covering diverse input scenarios, including edge cases, to simulate the performance of the 50-point FFT.

Numerical Validation:

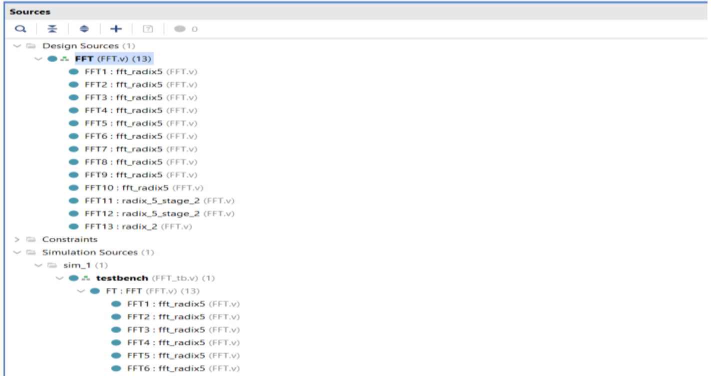
Employ numerical validation techniques to compare the output of the 50-point FFT against known results for specific test cases using online calculator.
https://engineering.icalculator.com/discrete-fourier-transform-calculator.html

4.2 Tools and Version

ModelSim,Vivado,Cadence.

4.3 Checking mechanisms

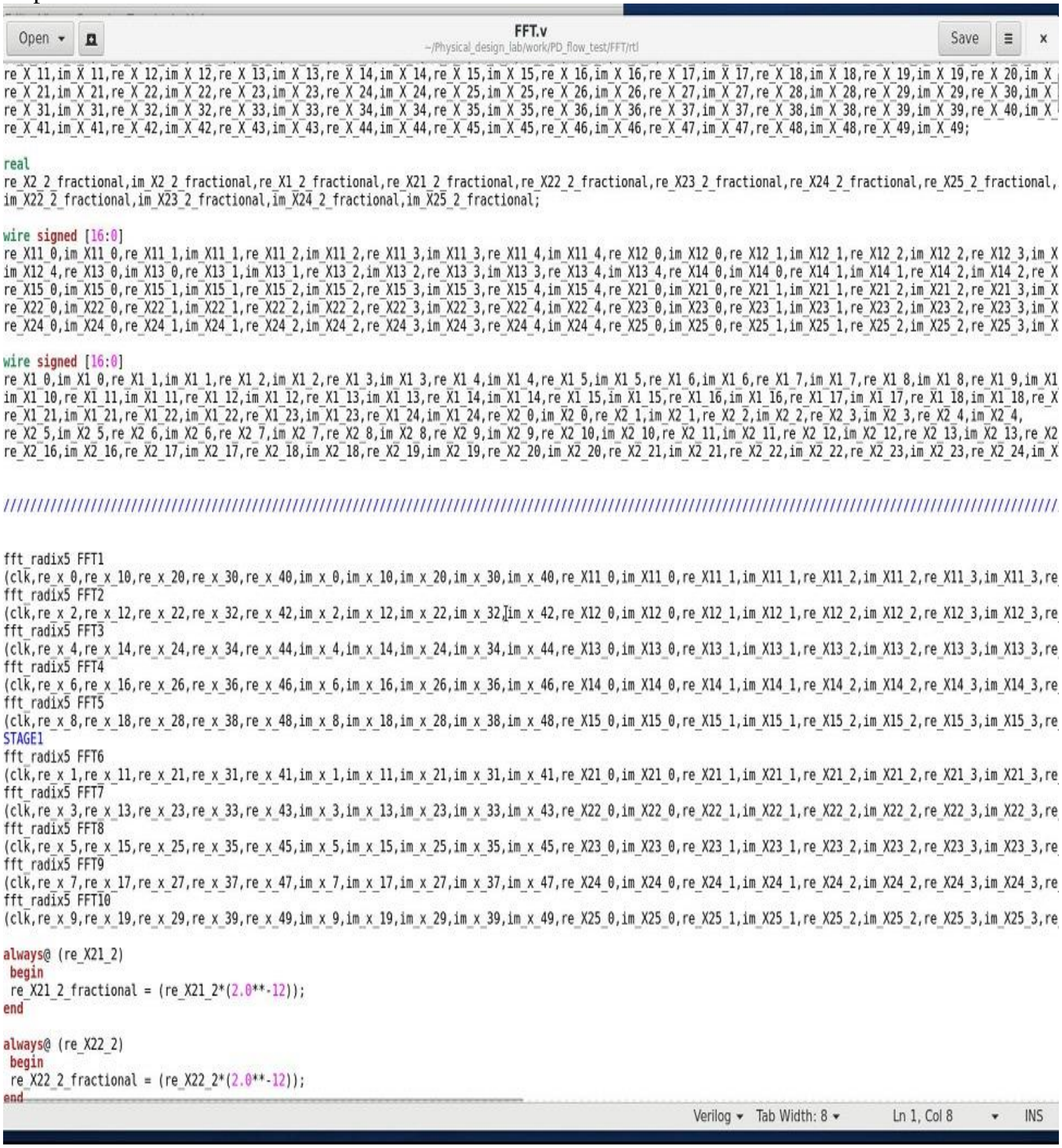
- **Testbench**: Developed a comprehensive testbench with test vectors that cover various input scenarios.
- **Timing Verification:** Static timing analysis to ensure that the design meets timing constraints and that all paths meet setup and hold time requirements.
- **Verilog Code:** Attached code and testbench with assignment.



```
Sources
Design Sources (1)
  FFT (FFT.v) (13)
    FFT1 : fft_radix5 (FFT.v)
    FFT2 : fft_radix5 (FFT.v)
    FFT3 : fft_radix5 (FFT.v)
    FFT4 : fft_radix5 (FFT.v)
    FFT5 : fft_radix5 (FFT.v)
    FFT6 : fft_radix5 (FFT.v)
    FFT7 : fft_radix5 (FFT.v)
    FFT8 : fft_radix5 (FFT.v)
    FFT9 : fft_radix5 (FFT.v)
    FFT10 : fft_radix5 (FFT.v)
    FFT11 : radix_5_stage_2 (FFT.v)
    FFT12 : radix_5_stage_2 (FFT.v)
    FFT13 : radix_2 (FFT.v)
Constraints
Simulation Sources (1)
  sim_1 (1)
    testbench (FFT_tb.v) (1)
      FT : FFT (FFT.v) (13)
        FFT1 : fft_radix5 (FFT.v)
        FFT2 : fft_radix5 (FFT.v)
        FFT3 : fft_radix5 (FFT.v)
        FFT4 : fft_radix5 (FFT.v)
        FFT5 : fft_radix5 (FFT.v)
        FFT6 : fft_radix5 (FFT.v)
```

4.4 ASIC Synthesis and verification

1. Design Entry: Utilized Verilog to describe the FFT algorithm for ASIC implementation.



```
re_X_11,im_X_11,re_X_12,im_X_12,re_X_13,im_X_13,re_X_14,im_X_14,re_X_15,im_X_15,re_X_16,im_X_16,re_X_17,im_X_17,re_X_18,im_X_18,re_X_19,im_X_19,re_X_20,im_X_
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re_X_31,im_X_31,re_X_32,im_X_32,re_X_33,im_X_33,re_X_34,im_X_34,re_X_35,im_X_35,re_X_36,im_X_36,re_X_37,im_X_37,re_X_38,im_X_38,re_X_39,im_X_39,re_X_40,im_X_
re_X_41,im_X_41,re_X_42,im_X_42,re_X_43,im_X_43,re_X_44,im_X_44,re_X_45,im_X_45,re_X_46,im_X_46,re_X_47,im_X_47,re_X_48,im_X_48,re_X_49,im_X_49;

real
re_X2_2_fractional,im_X2_2_fractional,re_X1_2_fractional,re_X21_2_fractional,re_X22_2_fractional,re_X23_2_fractional,re_X24_2_fractional,re_X25_2_fractional,
im_X22_2_fractional,im_X23_2_fractional,im_X24_2_fractional,im_X25_2_fractional;

wire signed [16:0]
re_X11_0,im_X11_0,re_X11_1,im_X11_1,re_X11_2,im_X11_2,re_X11_3,im_X11_3,re_X11_4,im_X11_4,re_X12_0,im_X12_0,re_X12_1,im_X12_1,re_X12_2,im_X12_2,re_X12_3,im_X
im_X12_4,re_X13_0,im_X13_0,re_X13_1,im_X13_1,re_X13_2,im_X13_2,re_X13_3,im_X13_3,re_X13_4,im_X13_4,re_X14_0,im_X14_0,re_X14_1,im_X14_1,re_X14_2,im_X14_2,re_X
re_X15_0,im_X15_0,re_X15_1,im_X15_1,re_X15_2,im_X15_2,re_X15_3,im_X15_3,re_X15_4,im_X15_4,re_X21_0,im_X21_0,re_X21_1,im_X21_1,re_X21_2,im_X21_2,re_X21_3,im_X
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wire signed [16:0]
re_X1_0,im_X1_0,re_X1_1,im_X1_1,re_X1_2,im_X1_2,re_X1_3,im_X1_3,re_X1_4,im_X1_4,re_X1_5,im_X1_5,re_X1_6,im_X1_6,re_X1_7,im_X1_7,re_X1_8,im_X1_8,re_X1_9,im_X1
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re_X2_5,im_X2_5,re_X2_6,im_X2_6,re_X2_7,im_X2_7,re_X2_8,im_X2_8,re_X2_9,im_X2_9,re_X2_10,im_X2_10,re_X2_11,im_X2_11,re_X2_12,im_X2_12,re_X2_13,im_X2_13,re_X2
re_X2_16,im_X2_16,re_X2_17,im_X2_17,re_X2_18,im_X2_18,re_X2_19,im_X2_19,re_X2_20,im_X2_20,re_X2_21,im_X2_21,re_X2_22,im_X2_22,re_X2_23,im_X2_23,re_X2_24,im_X


/////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////


fft_radix5 FFT1
(clk,re_x_0,re_x_10,re_x_20,re_x_30,re_x_40,im_x_0,im_x_10,im_x_20,im_x_30,im_x_40,re_X11_0,im_X11_0,re_X11_1,im_X11_1,re_X11_2,im_X11_2,re_X11_3,im_X11_3,re
fft_radix5 FFT2
(clk,re_x_2,re_x_12,re_x_22,re_x_32,re_x_42,im_x_2,im_x_12,im_x_22,im_x_32,im_x_42,re_X12_0,im_X12_0,re_X12_1,im_X12_1,re_X12_2,im_X12_2,re_X12_3,im_X12_3,re
fft_radix5 FFT3
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fft_radix5 FFT5
(clk,re_x_8,re_x_18,re_x_28,re_x_38,re_x_48,im_x_8,im_x_18,im_x_28,im_x_38,im_x_48,re_X15_0,im_X15_0,re_X15_1,im_X15_1,re_X15_2,im_X15_2,re_X15_3,im_X15_3,re
STAGE1
fft_radix5 FFT6
(clk,re_x_1,re_x_11,re_x_21,re_x_31,re_x_41,im_x_1,im_x_11,im_x_21,im_x_31,im_x_41,re_X21_0,im_X21_0,re_X21_1,im_X21_1,re_X21_2,im_X21_2,re_X21_3,im_X21_3,re
fft_radix5 FFT7
(clk,re_x_3,re_x_13,re_x_23,re_x_33,re_x_43,im_x_3,im_x_13,im_x_23,im_x_33,im_x_43,re_X22_0,im_X22_0,re_X22_1,im_X22_1,re_X22_2,im_X22_2,re_X22_3,im_X22_3,re
fft_radix5 FFT8
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fft_radix5 FFT9
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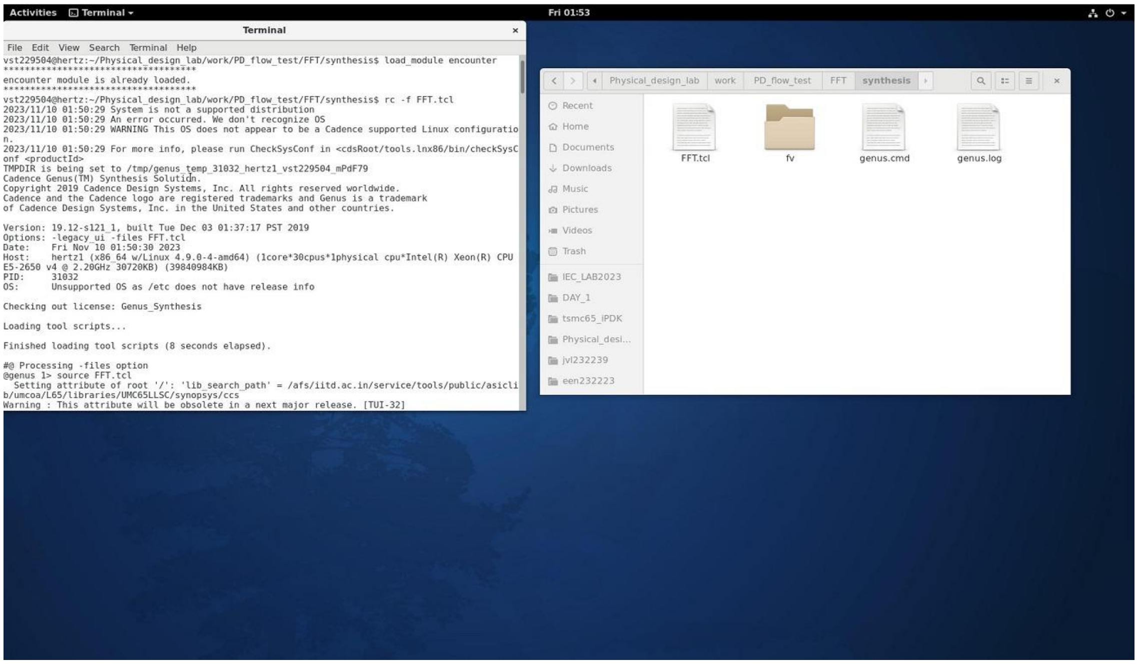
fft_radix5 FFT10
(clk,re_x_9,re_x_19,re_x_29,re_x_39,re_x_49,im_x_9,im_x_19,im_x_29,im_x_39,im_x_49,re_X25_0,im_X25_0,re_X25_1,im_X25_1,re_X25_2,im_X25_2,re_X25_3,im_X25_3,re

always@ (re_X21_2)
 begin
 re_X21_2_fractional = (re_X21_2*(2.0**-12));
end

always@ (re_X22_2)
 begin
 re_X22_2_fractional = (re_X22_2*(2.0**-12));
end
```

Verilog file for FFT

2. RTL Synthesis: Employed the genus tool for Register-Transfer Level (RTL) synthesis to convert verilog code into a gate-level netlist.



```
vst229504@hertz:~/Physical_design_lab/work/PD_flow_test/FFT/synthesis$ load_module encounter
***********************************
encounter module is already loaded.
***********************************
vst229504@hertz:~/Physical_design_lab/work/PD_flow_test/FFT/synthesis$ rc -f FFT.tcl
2023/11/10 01:50:29 System is not a supported distribution
2023/11/10 01:50:29 An error occurred. We don't recognize OS
2023/11/10 01:50:29 WARNING This OS does not appear to be a Cadence supported Linux configuratio
n.
2023/11/10 01:50:29 For more info, please run CheckSysConf in <cdsRoot/tools.lnx86/bin/checkSysC
onf <productId>
TMPDIR is being set to /tmp/genus_temp_31032_hertz1_vst229504_mPdF79
Cadence Genus(TM) Synthesis Solution.
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of Cadence Design Systems, Inc. in the United States and other countries.

Version: 19.12-s121_1, built Tue Dec 03 01:37:17 PST 2019
Options: -legacy_ui -files FFT.tcl
Date:    Fri Nov 10 01:50:30 2023
Host:    hertz1 (x86_64 w/Linux 4.9.0-4-amd64) (1core*30cpus*1physical cpu*Intel(R) Xeon(R) CPU
E5-2650 v4 @ 2.20GHz 30720KB) (39840984KB)
PID:     31032
OS:      Unsupported OS as /etc does not have release info

Checking out license: Genus_Synthesis

Loading tool scripts...

Finished loading tool scripts (8 seconds elapsed).

#@ Processing -files option
@genus 1> source FFT.tcl
  Setting attribute of root '/': 'lib_search_path' = /afs/iitd.ac.in/service/tools/public/asicli
b/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs
Warning : This attribute will be obsolete in a next major release. [TUI-32]
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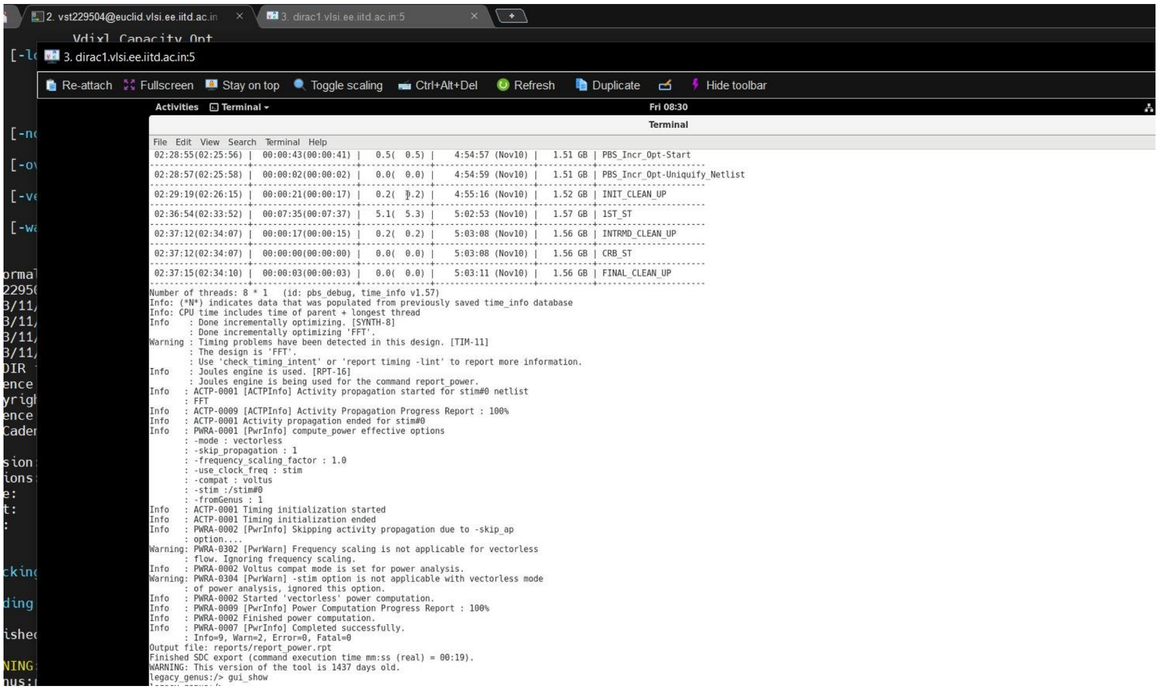
2. vst229504@euclid.vlsi.ee.iitd.ac.in
3. dirac1.vlsi.ee.iitd.ac.in:5
3. dirac1.vlsi.ee.iitd.ac.in:5
Re-attach
Fullscreen
Stay on top
Toggle scaling
Ctrl+Alt+Del
Refresh
Duplicate
Hide toolbar
Activities
Terminal
Fri 08:30
Terminal
File Edit View Search Terminal Help

```
02:28:55(02:25:56) |  00:00:43(00:00:41) |   0.5(  0.5) |    4:54:57 (Nov10) |   1.51 GB | PBS_Incr_Opt-Start
--------------------+---------------------+--------------+--------------------+-----------+--------------------
02:28:57(02:25:58) |  00:00:02(00:00:02) |   0.0(  0.0) |    4:54:59 (Nov10) |   1.51 GB | PBS_Incr_Opt-Uniquify_Netlist
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02:29:19(02:26:15) |  00:00:21(00:00:17) |   0.2(  0.2) |    4:55:16 (Nov10) |   1.52 GB | INIT_CLEAN_UP
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02:36:54(02:33:52) |  00:07:35(00:07:37) |   5.1(  5.3) |    5:02:53 (Nov10) |   1.57 GB | 1ST_ST
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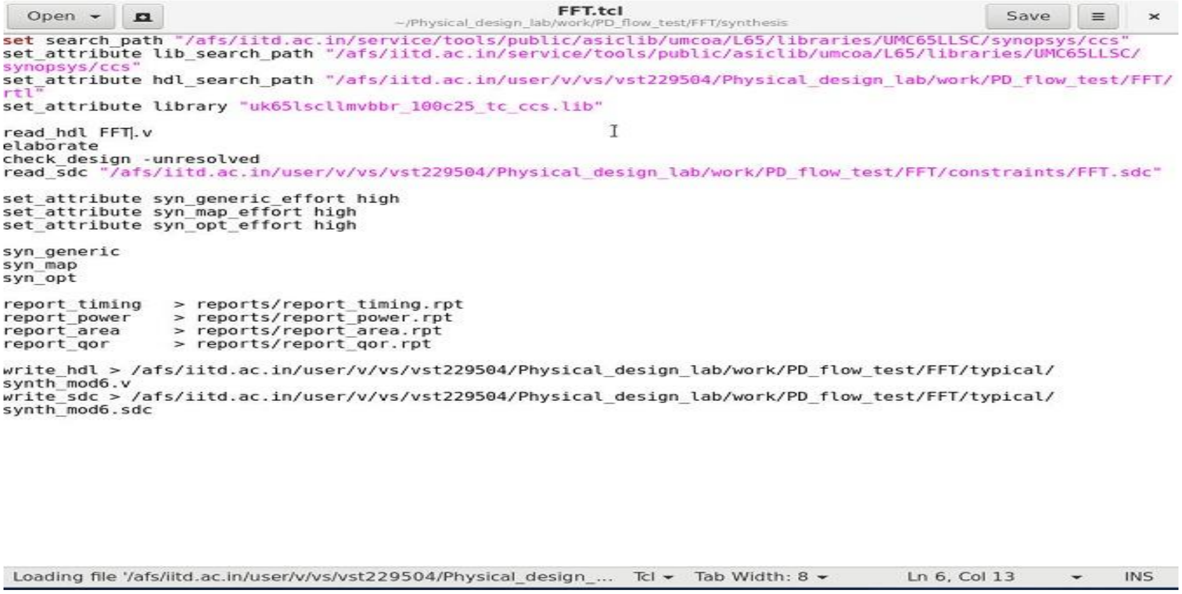
02:37:15(02:34:10) |  00:00:03(00:00:03) |   0.0(  0.0) |    5:03:11 (Nov10) |   1.56 GB | FINAL_CLEAN_UP
--------------------+---------------------+--------------+--------------------+-----------+--------------------
Number of threads: 8 * 1   (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
Info    : Done incrementally optimizing. [SYNTH-8]
        : Done incrementally optimizing 'FFT'.
Warning : Timing problems have been detected in this design. [TIM-11]
        : The design is 'FFT'.
        : Use 'check_timing_intent' or 'report timing -lint' to report more information.
Info    : Joules engine is used. [RPT-16]
        : Joules engine is being used for the command report_power.
Info   : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0 netlist
       : FFT
Info   : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%
Info   : ACTP-0001 Activity propagation ended for stim#0
Info   : PWRA-0001 [PwrInfo] compute_power effective options
       : -mode : vectorless
       : -skip_propagation : 1
       : -frequency_scaling_factor : 1.0
       : -use_clock_freq : stim
       : -compat : voltus
       : -stim :/stim#0
       : -fromGenus : 1
Info   : ACTP-0001 Timing initialization started
Info   : ACTP-0001 Timing initialization ended
Info   : PWRA-0002 [PwrInfo] Skipping activity propagation due to -skip_ap
       : option....
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for vectorless
       : flow. Ignoring frequency scaling.
Info   : PWRA-0002 Voltus compat mode is set for power analysis.
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with vectorless mode
       : of power analysis, ignored this option.
Info   : PWRA-0002 Started 'vectorless' power computation.
Info   : PWRA-0009 [PwrInfo] Power Computation Progress Report : 100%
Info   : PWRA-0002 Finished power computation.
Info   : PWRA-0007 [PwrInfo] Completed successfully.
       : Info=9, Warn=2, Error=0, Fatal=0
Output file: reports/report_power.rpt
Finished SDC export (command execution time mm:ss (real) = 00:19).
WARNING: This version of the tool is 1437 days old.
legacy_genus:/> gui_show
```

3. Technology Mapping: Mapped generic gates to the UMC65 technology library, ensuring compatibility and optimization for the specific ASIC technology.



```
set search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"
set_attribute lib_search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/
synopsys/ccs"
set_attribute hdl_search_path "/afs/iitd.ac.in/user/v/vs/vst229504/Physical_design_lab/work/PD_flow_test/FFT/
rtl"
set_attribute library "uk65lscllmvbbr_100c25_tc_ccs.lib"

read_hdl FFT.v
elaborate
check_design -unresolved
read_sdc "/afs/iitd.ac.in/user/v/vs/vst229504/Physical_design_lab/work/PD_flow_test/FFT/constraints/FFT.sdc"

set_attribute syn_generic_effort high
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

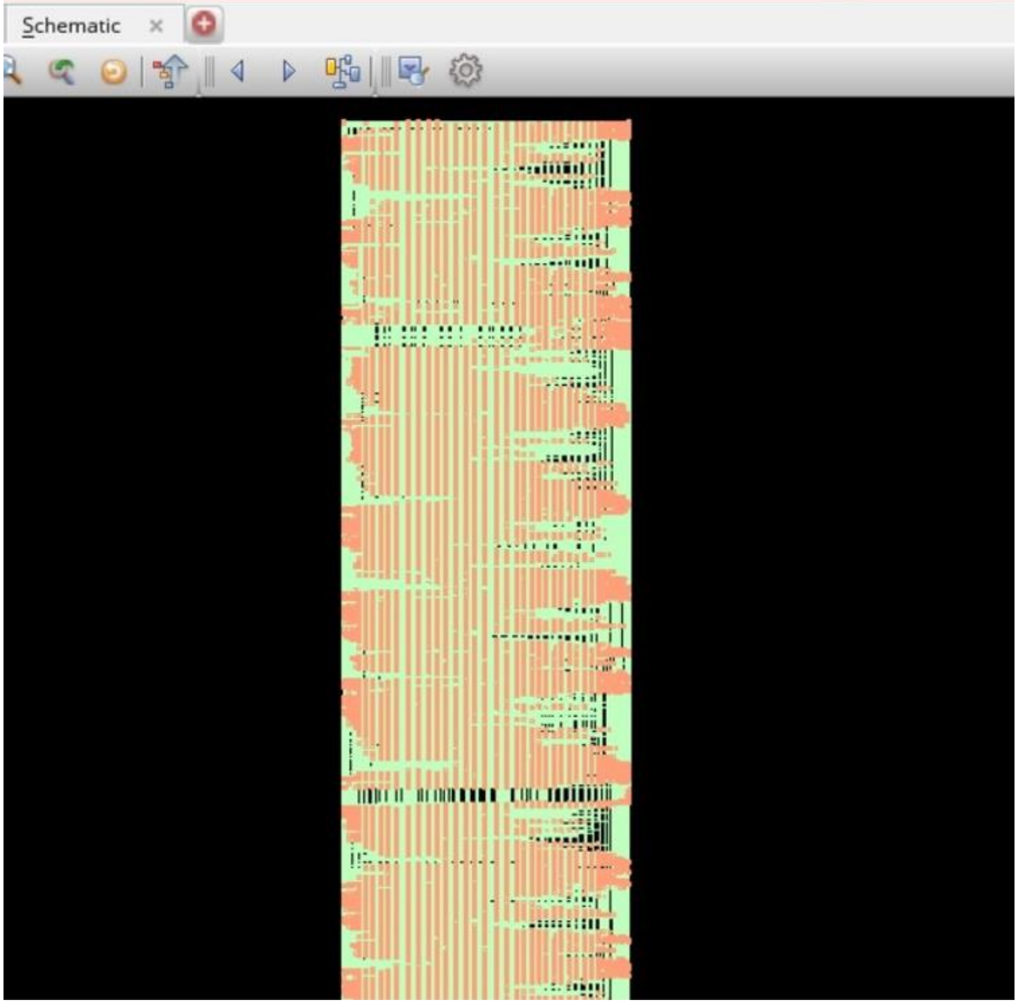
syn_generic
syn_map
syn_opt

report_timing   > reports/report_timing.rpt
report_power    > reports/report_power.rpt
report_area     > reports/report_area.rpt
report_qor      > reports/report_qor.rpt

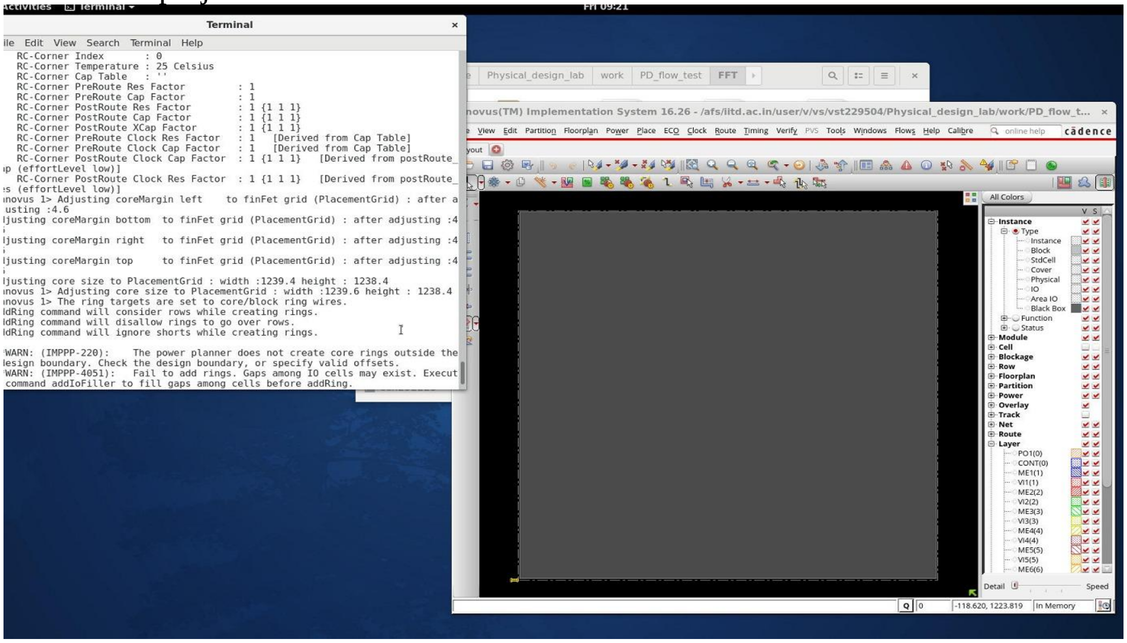
write_hdl > /afs/iitd.ac.in/user/v/vs/vst229504/Physical_design_lab/work/PD_flow_test/FFT/typical/
synth_mod6.v
write_sdc > /afs/iitd.ac.in/user/v/vs/vst229504/Physical_design_lab/work/PD_flow_test/FFT/typical/
synth_mod6.sdc
```

```
Loading file '/afs/iitd.ac.in/user/v/vs/vst229504/Physical_design_...   Tcl   Tab Width: 8   Ln 6, Col 13   INS
```

4. Netlist Output: Obtained a finalized gate-level netlist as the output, ready for subsequent stages of the ASIC design flow.



5. Physical Design: Executed physical design steps, including placement and routing, considering the UMC65 technology constraints to optimize chip area and performance for the FFT project.



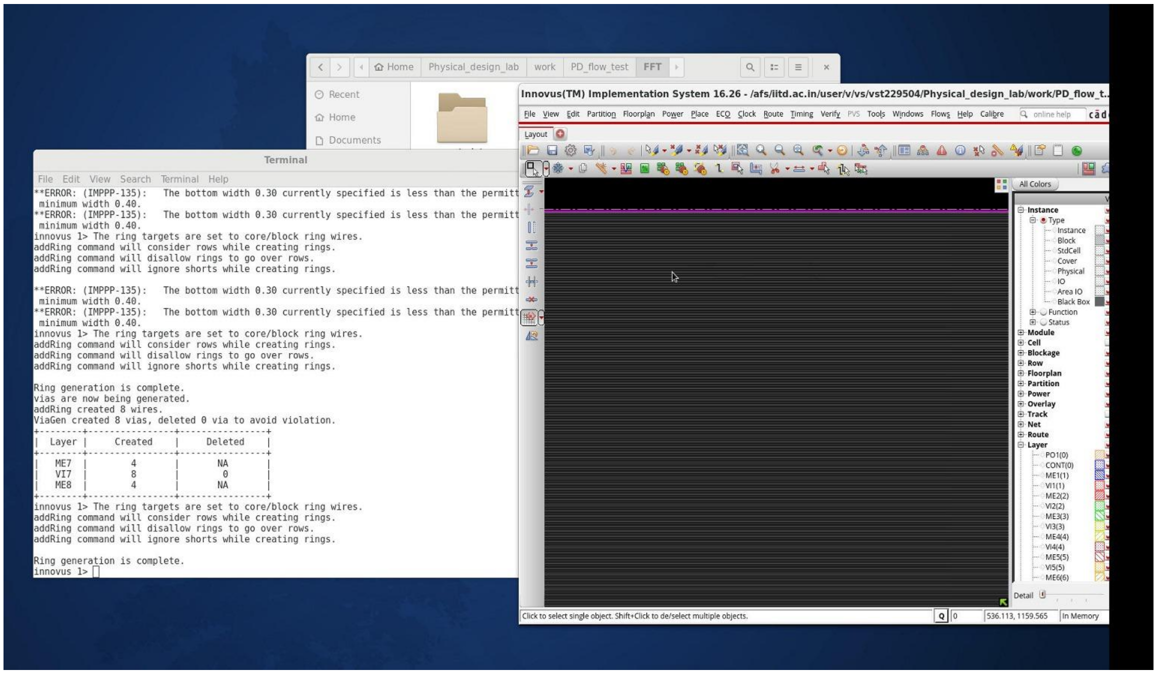
```
  RC-Corner Index       : 0
  RC-Corner Temperature : 25 Celsius
  RC-Corner Cap Table   : ''
  RC-Corner PreRoute Res Factor         : 1
  RC-Corner PreRoute Cap Factor         : 1
  RC-Corner PostRoute Res Factor        : 1 {1 1 1}
  RC-Corner PostRoute Cap Factor        : 1 {1 1 1}
  RC-Corner PostRoute XCap Factor       : 1 {1 1 1}
  RC-Corner PreRoute Clock Res Factor   : 1   [Derived from Cap Table]
  RC-Corner PreRoute Clock Cap Factor   : 1   [Derived from Cap Table]
  RC-Corner PostRoute Clock Cap Factor  : 1 {1 1 1}   [Derived from postRoute_
ip (effortLevel low)]
  RC-Corner PostRoute Clock Res Factor  : 1 {1 1 1}   [Derived from postRoute_
es (effortLevel low)]
inovus 1> Adjusting coreMargin left    to finFet grid (PlacementGrid) : after a
usting :4.6
ljusting coreMargin bottom  to finFet grid (PlacementGrid) : after adjusting :4

ljusting coreMargin right   to finFet grid (PlacementGrid) : after adjusting :4

ljusting coreMargin top     to finFet grid (PlacementGrid) : after adjusting :4

ljusting core size to PlacementGrid : width :1239.4 height : 1238.4
inovus 1> Adjusting core size to PlacementGrid : width :1239.6 height : 1238.4
inovus 1> The ring targets are set to core/block ring wires.
ldRing command will consider rows while creating rings.
ldRing command will disallow rings to go over rows.
ldRing command will ignore shorts while creating rings.

WARN: (IMPPP-220):    The power planner does not create core rings outside the
lesign boundary. Check the design boundary, or specify valid offsets.
WARN: (IMPPP-4051):   Fail to add rings. Gaps among IO cells may exist. Execut
 command addIoFiller to fill gaps among cells before addRing.
```



Home
Physical_design_lab
work
PD_flow_test
FFT
Recent
Home
Documents
Terminal
File Edit View Search Terminal Help
Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/v/vs/vst229504/Physical_design_lab/work/PD_flow_t...
Layout
All Colors
Instance
Type
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
Detail
Click to select single object. Shift+Click to de/select multiple objects.
536.113, 1159.565
In Memory

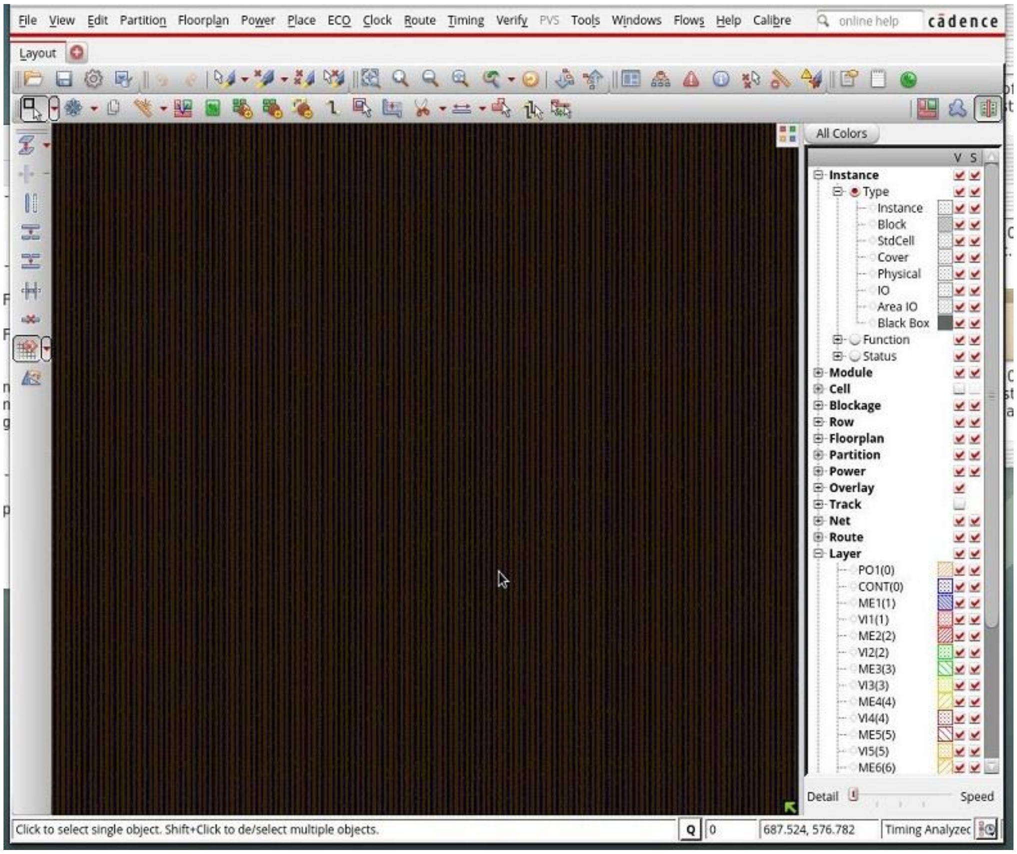
```
**ERROR: (IMPPP-135):   The bottom width 0.30 currently specified is less than the permitt
 minimum width 0.40.
**ERROR: (IMPPP-135):   The bottom width 0.30 currently specified is less than the permitt
 minimum width 0.40.
innovus 1> The ring targets are set to core/block ring wires.
addRing command will consider rows while creating rings.
addRing command will disallow rings to go over rows.
addRing command will ignore shorts while creating rings.

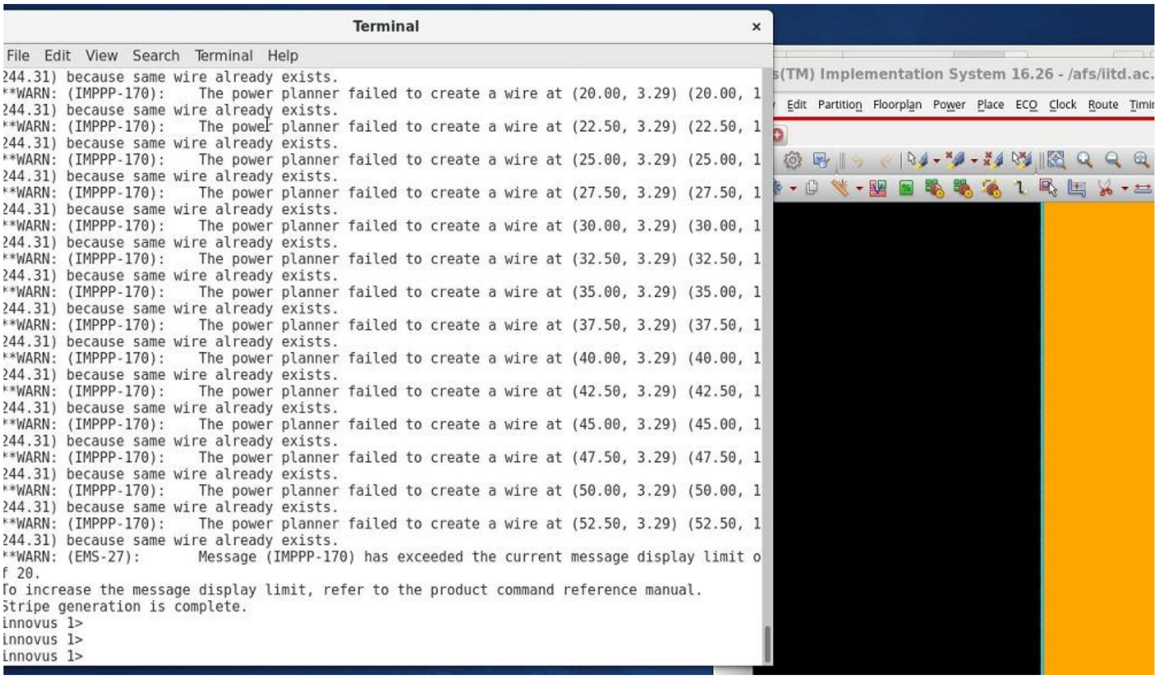
**ERROR: (IMPPP-135):   The bottom width 0.30 currently specified is less than the permitt
 minimum width 0.40.
**ERROR: (IMPPP-135):   The bottom width 0.30 currently specified is less than the permitt
 minimum width 0.40.
innovus 1> The ring targets are set to core/block ring wires.
addRing command will consider rows while creating rings.
addRing command will disallow rings to go over rows.
addRing command will ignore shorts while creating rings.

Ring generation is complete.
vias are now being generated.
addRing created 8 wires.
ViaGen created 8 vias, deleted 0 via to avoid violation.
+--------+----------------+----------------+
|  Layer |     Created    |     Deleted    |
+--------+----------------+----------------+
|   ME7  |        4       |        NA      |
|   VI7  |        8       |         0      |
|   ME8  |        4       |        NA      |
+--------+----------------+----------------+
innovus 1> The ring targets are set to core/block ring wires.
addRing command will consider rows while creating rings.
addRing command will disallow rings to go over rows.
addRing command will ignore shorts while creating rings.

Ring generation is complete.
innovus 1> 
```

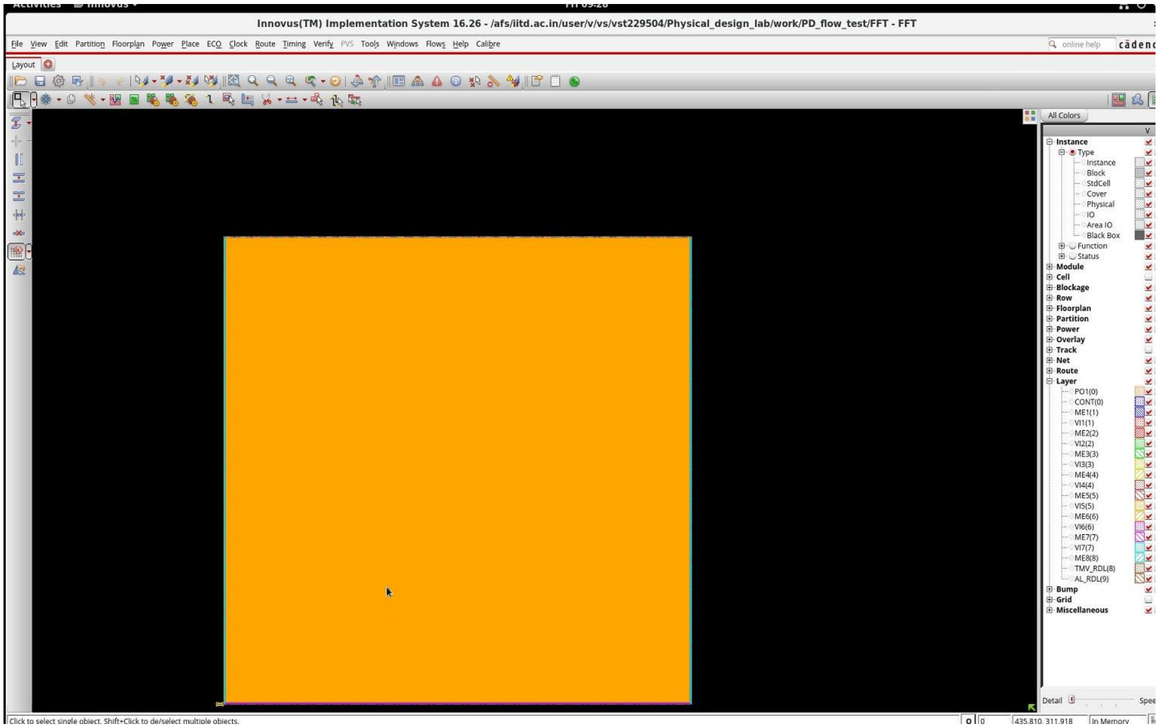
Ring generation




Terminal
File Edit View Search Terminal Help
s(TM) Implementation System 16.26 - /afs/iitd.ac.
Edit Partition Floorplan Power Place ECO Clock Route Timi

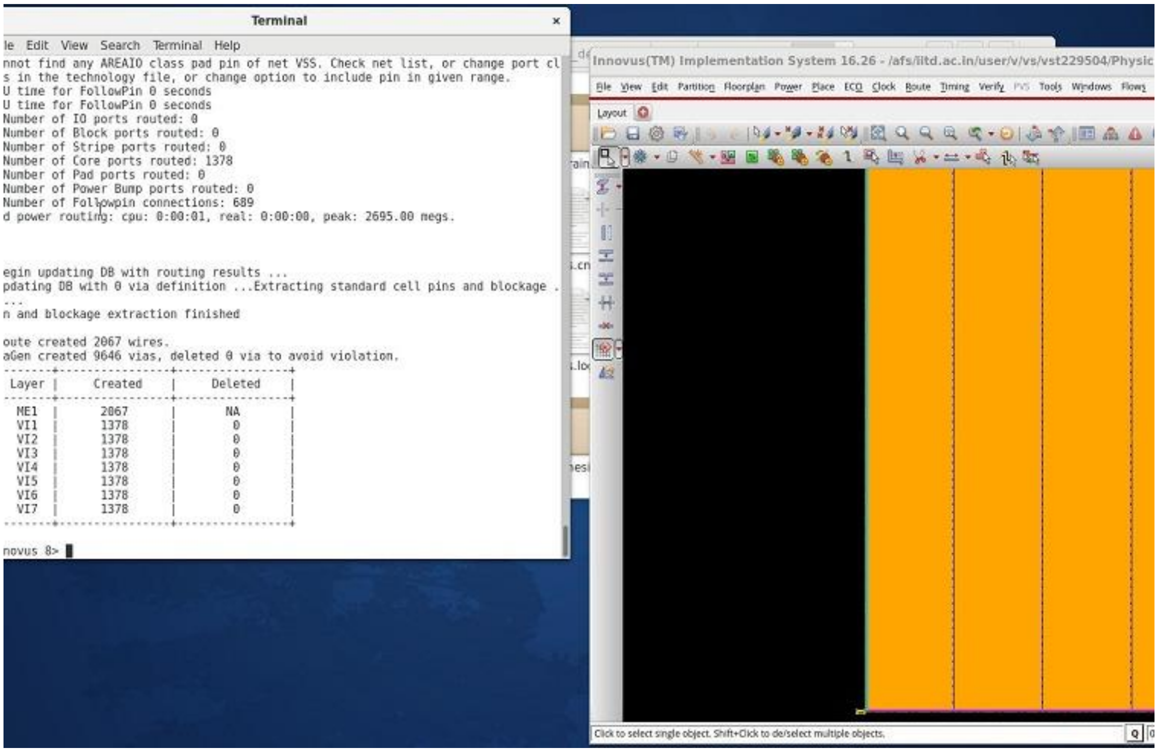
```
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (20.00, 3.29) (20.00, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (22.50, 3.29) (22.50, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (25.00, 3.29) (25.00, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (27.50, 3.29) (27.50, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (30.00, 3.29) (30.00, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (32.50, 3.29) (32.50, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (35.00, 3.29) (35.00, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (37.50, 3.29) (37.50, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (40.00, 3.29) (40.00, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (42.50, 3.29) (42.50, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (45.00, 3.29) (45.00, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (47.50, 3.29) (47.50, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (50.00, 3.29) (50.00, 1
244.31) because same wire already exists.
**WARN: (IMPPP-170):    The power planner failed to create a wire at (52.50, 3.29) (52.50, 1
244.31) because same wire already exists.
**WARN: (EMS-27):       Message (IMPPP-170) has exceeded the current message display limit o
f 20.
To increase the message display limit, refer to the product command reference manual.
Stripe generation is complete.
innovus 1>
innovus 1>
innovus 1>
```

Stripe generation



Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/v/vs/vst229504/Physical_design_lab/work/PD_flow_test/FFT - FFT

Click to select single object. Shift+Click to de/select multiple objects.



```
                              Terminal
le  Edit  View  Search  Terminal  Help
nnot find any AREAIO class pad pin of net VSS. Check net list, or change port cl
s in the technology file, or change option to include pin in given range.
U time for FollowPin 0 seconds
U time for FollowPin 0 seconds
Number of IO ports routed: 0
Number of Block ports routed: 0
Number of Stripe ports routed: 0
Number of Core ports routed: 1378
Number of Pad ports routed: 0
Number of Power Bump ports routed: 0
Number of Followpin connections: 689
d power routing: cpu: 0:00:01, real: 0:00:00, peak: 2695.00 megs.



egin updating DB with routing results ...
pdating DB with 0 via definition ...Extracting standard cell pins and blockage .
...
n and blockage extraction finished

oute created 2067 wires.
aGen created 9646 vias, deleted 0 via to avoid violation.
-------+----------------+----------------+
 Layer |     Created    |     Deleted    |
-------+----------------+----------------+
  ME1  |      2067      |       NA       |
  VI1  |      1378      |        0       |
  VI2  |      1378      |        0       |
  VI3  |      1378      |        0       |
  VI4  |      1378      |        0       |
  VI5  |      1378      |        0       |
  VI6  |      1378      |        0       |
  VI7  |      1378      |        0       |
-------+----------------+----------------+

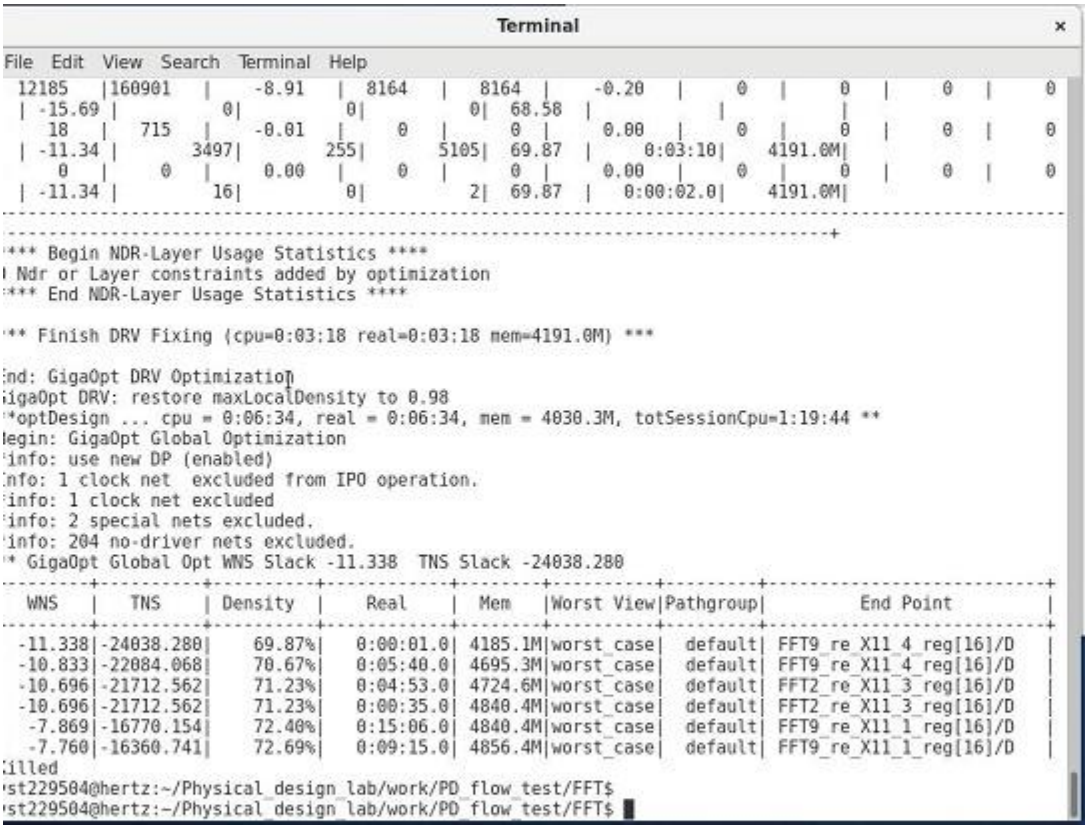
novus 8> 
```

Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/v/vs/vst229504/Physic

Click to select single object. Shift+Click to de/select multiple objects.

File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows
Layout

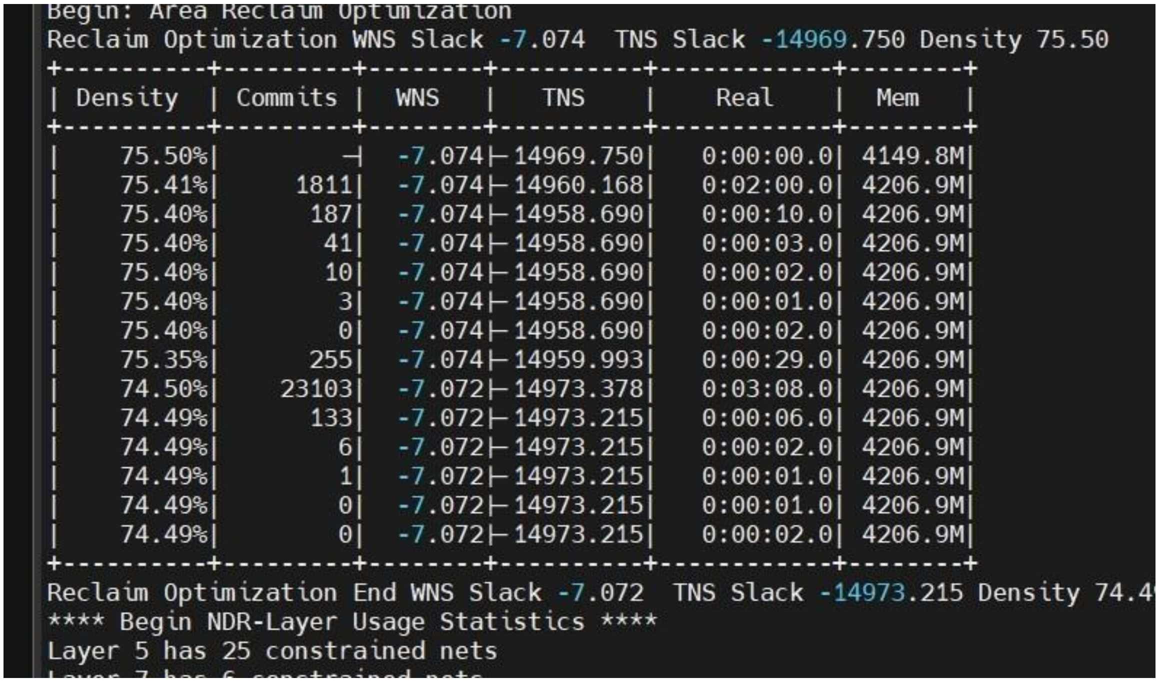
Srouting



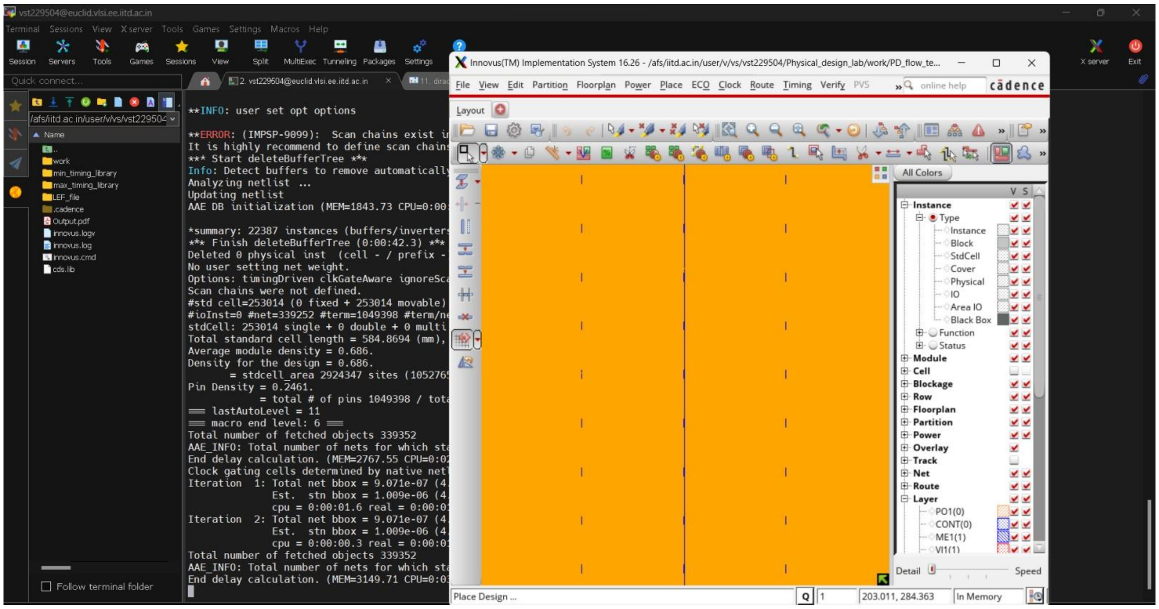
```
  12185   |160901   |    -8.91   |  8164   |   8164  |    -0.20   |     0   |     0   |     0   |     0
 | -15.69 |          0|          0|          0|  68.58  |            |          |
    18    |   715   |    -0.01   |     0   |     0   |   0.00   |     0   |     0   |     0   |     0
 | -11.34 |       3497|        255|       5105|  69.87  |    0:03:10|   4191.0M|
     0    |     0   |     0.00   |     0   |     0   |   0.00   |     0   |     0   |     0   |     0
 | -11.34 |         16|          0|          2|  69.87  |  0:00:02.0|   4191.0M|
--------------------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------+
*** Begin NDR-Layer Usage Statistics ****
 Ndr or Layer constraints added by optimization
*** End NDR-Layer Usage Statistics ****

** Finish DRV Fixing (cpu=0:03:18 real=0:03:18 mem=4191.0M) ***

nd: GigaOpt DRV Optimization
igaOpt DRV: restore maxLocalDensity to 0.98
*optDesign ... cpu = 0:06:34, real = 0:06:34, mem = 4030.3M, totSessionCpu=1:19:44 **
egin: GigaOpt Global Optimization
info: use new DP (enabled)
nfo: 1 clock net  excluded from IPO operation.
info: 1 clock net excluded
info: 2 special nets excluded.
info: 204 no-driver nets excluded.
* GigaOpt Global Opt WNS Slack -11.338  TNS Slack -24038.280
--------+----------+----------+------------+--------+----------+---------+--------------------------+
  WNS   |   TNS    | Density  |    Real    |  Mem   |Worst View|Pathgroup|        End Point         |
--------+----------+----------+------------+--------+----------+---------+--------------------------+
 -11.338|-24038.280|    69.87%|   0:00:01.0| 4185.1M|worst_case|  default| FFT9_re_X11_4_reg[16]/D  |
 -10.833|-22084.068|    70.67%|   0:05:40.0| 4695.3M|worst_case|  default| FFT9_re_X11_4_reg[16]/D  |
 -10.696|-21712.562|    71.23%|   0:04:53.0| 4724.6M|worst_case|  default| FFT2_re_X11_3_reg[16]/D  |
 -10.696|-21712.562|    71.23%|   0:00:35.0| 4840.4M|worst_case|  default| FFT2_re_X11_3_reg[16]/D  |
  -7.869|-16770.154|    72.40%|   0:15:06.0| 4840.4M|worst_case|  default| FFT9_re_X11_1_reg[16]/D  |
  -7.760|-16360.741|    72.69%|   0:09:15.0| 4856.4M|worst_case|  default| FFT9_re_X11_1_reg[16]/D  |
illed
st229504@hertz:~/Physical_design_lab/work/PD_flow_test/FFT$
st229504@hertz:~/Physical_design_lab/work/PD_flow_test/FFT$ 
```



```
Begin: Area Reclaim Optimization
Reclaim Optimization WNS Slack -7.074  TNS Slack -14969.750 Density 75.50
+----------+---------+--------+----------+------------+--------+
| Density  | Commits |  WNS   |   TNS    |    Real    |  Mem   |
+----------+---------+--------+----------+------------+--------+
|    75.50%|       -|  -7.074|-14969.750|   0:00:00.0| 4149.8M|
|    75.41%|     1811|  -7.074|-14960.168|   0:02:00.0| 4206.9M|
|    75.40%|      187|  -7.074|-14958.690|   0:00:10.0| 4206.9M|
|    75.40%|       41|  -7.074|-14958.690|   0:00:03.0| 4206.9M|
|    75.40%|       10|  -7.074|-14958.690|   0:00:02.0| 4206.9M|
|    75.40%|        3|  -7.074|-14958.690|   0:00:01.0| 4206.9M|
|    75.40%|        0|  -7.074|-14958.690|   0:00:02.0| 4206.9M|
|    75.35%|      255|  -7.074|-14959.993|   0:00:29.0| 4206.9M|
|    74.50%|    23103|  -7.072|-14973.378|   0:03:08.0| 4206.9M|
|    74.49%|      133|  -7.072|-14973.215|   0:00:06.0| 4206.9M|
|    74.49%|        6|  -7.072|-14973.215|   0:00:02.0| 4206.9M|
|    74.49%|        1|  -7.072|-14973.215|   0:00:01.0| 4206.9M|
|    74.49%|        0|  -7.072|-14973.215|   0:00:01.0| 4206.9M|
|    74.49%|        0|  -7.072|-14973.215|   0:00:02.0| 4206.9M|
+----------+---------+--------+----------+------------+--------+
Reclaim Optimization End WNS Slack -7.072  TNS Slack -14973.215 Density 74.4
**** Begin NDR-Layer Usage Statistics ****
Layer 5 has 25 constrained nets
Layer 7 has 6 constrained nets
```



vst229504@euclid.vlsi.ee.iitd.ac.in
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings
2. vst229504@euclid.vlsi.ee.iitd.ac.in
/afs/iitd.ac.in/user/v/vs/vst229504
work
min_timing_library
max_timing_library
LEF_file
.cadence
Output.pdf
innovus.logv
innovus.log
innovus.cmd
cds.lib
Follow terminal folder
Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/v/vs/vst229504/Physical_design_lab/work/PD_flow_te...
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS
cādence
Layout
All Colors
Instance
Type
Instance
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
PO1(0)
CONT(0)
ME1(1)
VI1(1)
Detail
Speed
Place Design ...
203.011, 284.363
In Memory
X server Exit

```
**INFO: user set opt options

**ERROR: (IMPSP-9099):  Scan chains exist i
It is highly recommend to define scan chains
*** Start deleteBufferTree ***
Info: Detect buffers to remove automatically
Analyzing netlist ...
Updating netlist
AAE DB initialization (MEM=1843.73 CPU=0:00

*summary: 22387 instances (buffers/inverters
*** Finish deleteBufferTree (0:00:42.3) ***
Deleted 0 physical inst  (cell - / prefix -
No user setting net weight.
Options: timingDriven clkGateAware ignoreSca
Scan chains were not defined.
#std cell=253014 (0 fixed + 253014 movable)
#ioInst=0 #net=339252 #term=1049398 #term/ne
stdCell: 253014 single + 0 double + 0 multi
Total standard cell length = 584.8694 (mm),
Average module density = 0.686.
Density for the design = 0.686.
       = stdcell_area 2924347 sites (105276
Pin Density = 0.2461.
            = total # of pins 1049398 / tota
=== lastAutoLevel = 11
=== macro end level: 6 ===
Total number of fetched objects 339352
AAE_INFO: Total number of nets for which sta
End delay calculation. (MEM=2767.55 CPU=0:0
Clock gating cells determined by native net
Iteration  1: Total net bbox = 9.071e-07 (4
              Est.  stn bbox = 1.009e-06 (4
              cpu = 0:00:01.6 real = 0:00:0
Iteration  2: Total net bbox = 9.071e-07 (4
              Est.  stn bbox = 1.009e-06 (4
              cpu = 0:00:00.3 real = 0:00:0
Total number of fetched objects 339352
AAE_INFO: Total number of nets for which sta
End delay calculation. (MEM=3149.71 CPU=0:0
```

During placement of design command

6. Results

6.1 Area

6.2 DRC rule Violations

6.3 Timing(Clock Tree Synthesis (CTS):

5.Testbench(Attached with assignment)

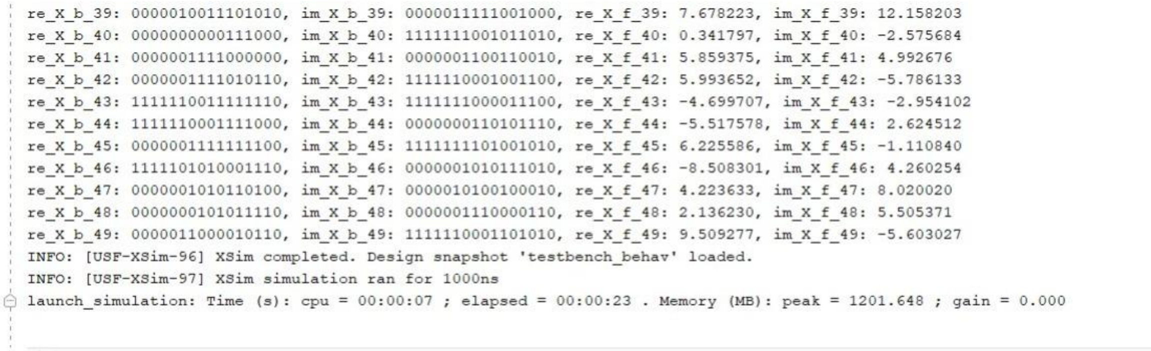
5.1 Input Generation: An FFT module (FT) is instantiated with the declared input and output signals. The module has a set of reg and wire declarations, representing real and imaginary parts of input (re_x_i and im_x_i) and output (re_X_i and im_X_i) data.The code calculates fractional parts (_fractional) of the real and imaginary inputs.

5.2 Fractional Part Calculation: Calculates the fractional part for both input and output real and imaginary parts.

5.3 Precision Testing: For each re_x_i, we convert the value to a fractional representation (re_x_i_fractional) with higher precision. This is achieved by scaling down the original value (re_x_i) through multiplication by 2.0**-13. In binary terms, this operation is equivalent to right-shifting the binary representation of the original value by 13 bits, effectively dividing it by 2^13.

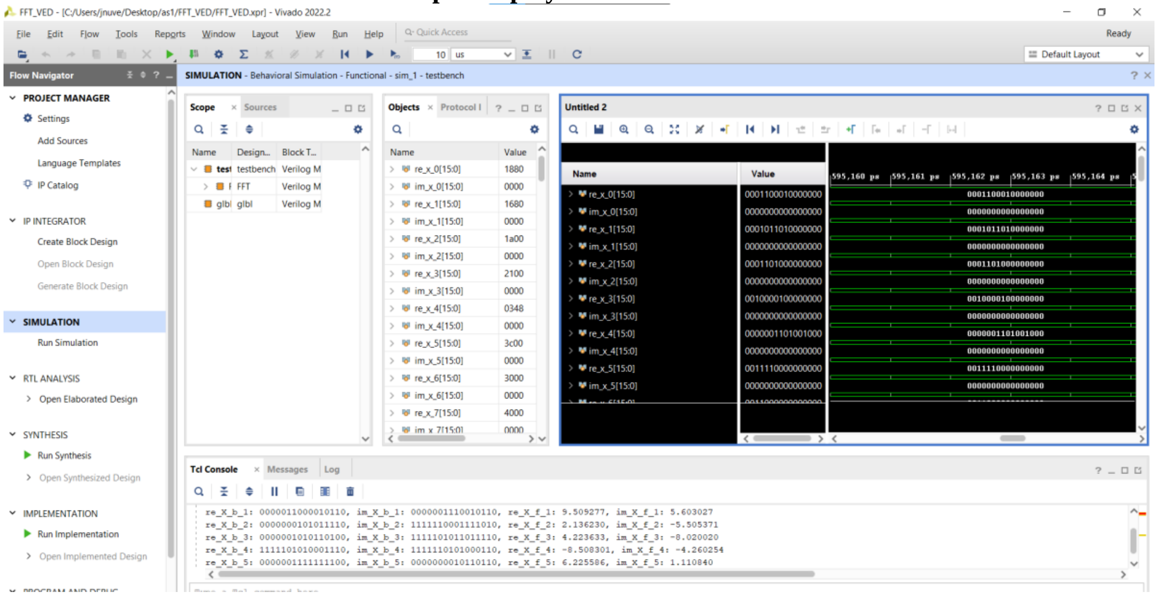
5.4 Clock and Clock Generation: A clock (clk) is declared, and a clock generation process is defined to toggle the clock every 5 time units. Toggles the clock signal every 5 time units.

5.5 Simulation and Results:



```
re_X_b_39: 0000010011101010, im_X_b_39: 0000011111001000, re_X_f_39: 7.678223, im_X_f_39: 12.158203
re_X_b_40: 0000000000111000, im_X_b_40: 1111111001011010, re_X_f_40: 0.341797, im_X_f_40: -2.575684
re_X_b_41: 0000001111000000, im_X_b_41: 0000001100110010, re_X_f_41: 5.859375, im_X_f_41: 4.992676
re_X_b_42: 0000001111010110, im_X_b_42: 1111110001001100, re_X_f_42: 5.993652, im_X_f_42: -5.786133
re_X_b_43: 1111110011111110, im_X_b_43: 1111111000011100, re_X_f_43: -4.699707, im_X_f_43: -2.954102
re_X_b_44: 1111110001111000, im_X_b_44: 0000000110101110, re_X_f_44: -5.517578, im_X_f_44: 2.624512
re_X_b_45: 0000001111111100, im_X_b_45: 1111111101001010, re_X_f_45: 6.225586, im_X_f_45: -1.110840
re_X_b_46: 1111101010001110, im_X_b_46: 0000001010111010, re_X_f_46: -8.508301, im_X_f_46: 4.260254
re_X_b_47: 0000001010110100, im_X_b_47: 0000010100100010, re_X_f_47: 4.223633, im_X_f_47: 8.020020
re_X_b_48: 0000000101011110, im_X_b_48: 0000001110000110, re_X_f_48: 2.136230, im_X_f_48: 5.505371
re_X_b_49: 0000011000010110, im_X_b_49: 1111110001101010, re_X_f_49: 9.509277, im_X_f_49: -5.603027
INFO: [USF-XSim-96] XSim completed. Design snapshot 'testbench_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:23 . Memory (MB): peak = 1201.648 ; gain = 0.000
```

Output displayed in console

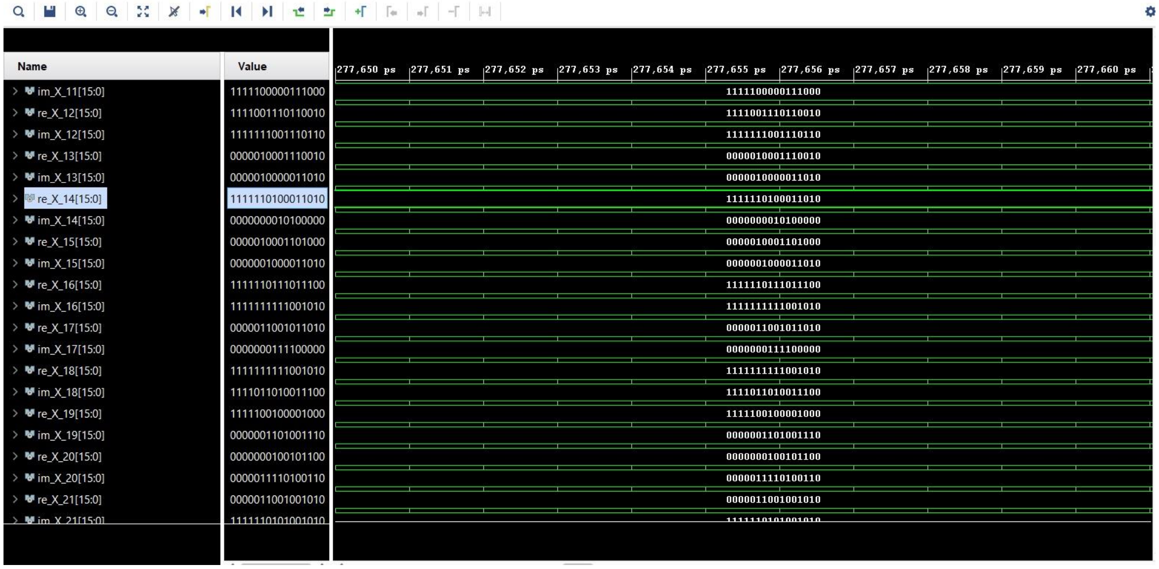


Name	Design...	Block T...
testbench	testbench	Verilog M
FFT		Verilog M
glbl	glbl	Verilog M

Name	Value
re_x_0[15:0]	1880
im_x_0[15:0]	0000
re_x_1[15:0]	1680
im_x_1[15:0]	0000
re_x_2[15:0]	1a00
im_x_2[15:0]	0000
re_x_3[15:0]	2100
im_x_3[15:0]	0000
re_x_4[15:0]	0348
im_x_4[15:0]	0000
re_x_5[15:0]	3c00
im_x_5[15:0]	0000
re_x_6[15:0]	3000
im_x_6[15:0]	0000
re_x_7[15:0]	4000
im_x_7[15:0]	0000

Name	Value
re_x_0[15:0]	0001100010000000
im_x_0[15:0]	0000000000000000
re_x_1[15:0]	0001011010000000
im_x_1[15:0]	0000000000000000
re_x_2[15:0]	0001101000000000
im_x_2[15:0]	0000000000000000
re_x_3[15:0]	0010000100000000
im_x_3[15:0]	0000000000000000
re_x_4[15:0]	0000001101001000
im_x_4[15:0]	0000000000000000
re_x_5[15:0]	0011110000000000
im_x_5[15:0]	0000000000000000

```
re_X_b_1: 0000011000010110, im_X_b_1: 0000001110010110, re_X_f_1: 9.509277, im_X_f_1: 5.603027
re_X_b_2: 0000000101011110, im_X_b_2: 1111110001111010, re_X_f_2: 2.136230, im_X_f_2: -5.505371
re_X_b_3: 0000001010110100, im_X_b_3: 1111101011011110, re_X_f_3: 4.223633, im_X_f_3: -8.020020
re_X_b_4: 1111101010001110, im_X_b_4: 1111110101000110, re_X_f_4: -8.508301, im_X_f_4: -4.260254
re_X_b_5: 0000001111111100, im_X_b_5: 0000000010110110, re_X_f_5: 6.225586, im_X_f_5: 1.110840
```



Name	Value
im_X_11[15:0]	1111100000111000
re_X_12[15:0]	1111001110110010
im_X_12[15:0]	1111111001110110
re_X_13[15:0]	0000010001110010
im_X_13[15:0]	0000010000011010
re_X_14[15:0]	1111110100011010
im_X_14[15:0]	0000000010100000
re_X_15[15:0]	0000010001101000
im_X_15[15:0]	0000001000011010
re_X_16[15:0]	1111110111011100
im_X_16[15:0]	1111111111001010
re_X_17[15:0]	0000011001011010
im_X_17[15:0]	0000000111100000
re_X_18[15:0]	1111111111001010
im_X_18[15:0]	1111011010011100
re_X_19[15:0]	1111100100001000
im_X_19[15:0]	0000001101001110
re_X_20[15:0]	0000000100101100
im_X_20[15:0]	0000011110100110
re_X_21[15:0]	0000011001001010
im_X_21[15:0]	1111110101001010

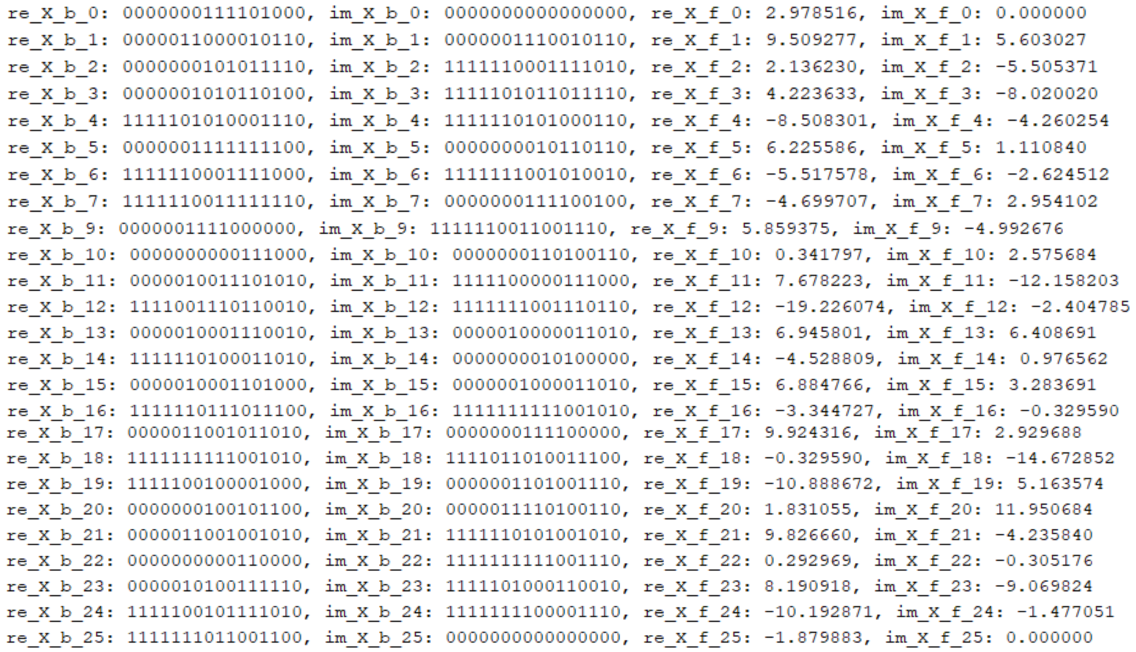
Graphical output of testbench

5. Tests Specification

1: Basic Functionality: This test is designed to verify the fundamental functionality of your FFT implementation. It typically involves providing known input signals to the FFT algorithm and checking if the output matches the expected results.

- **Sample results from 50 point FFT simulations and comparison**

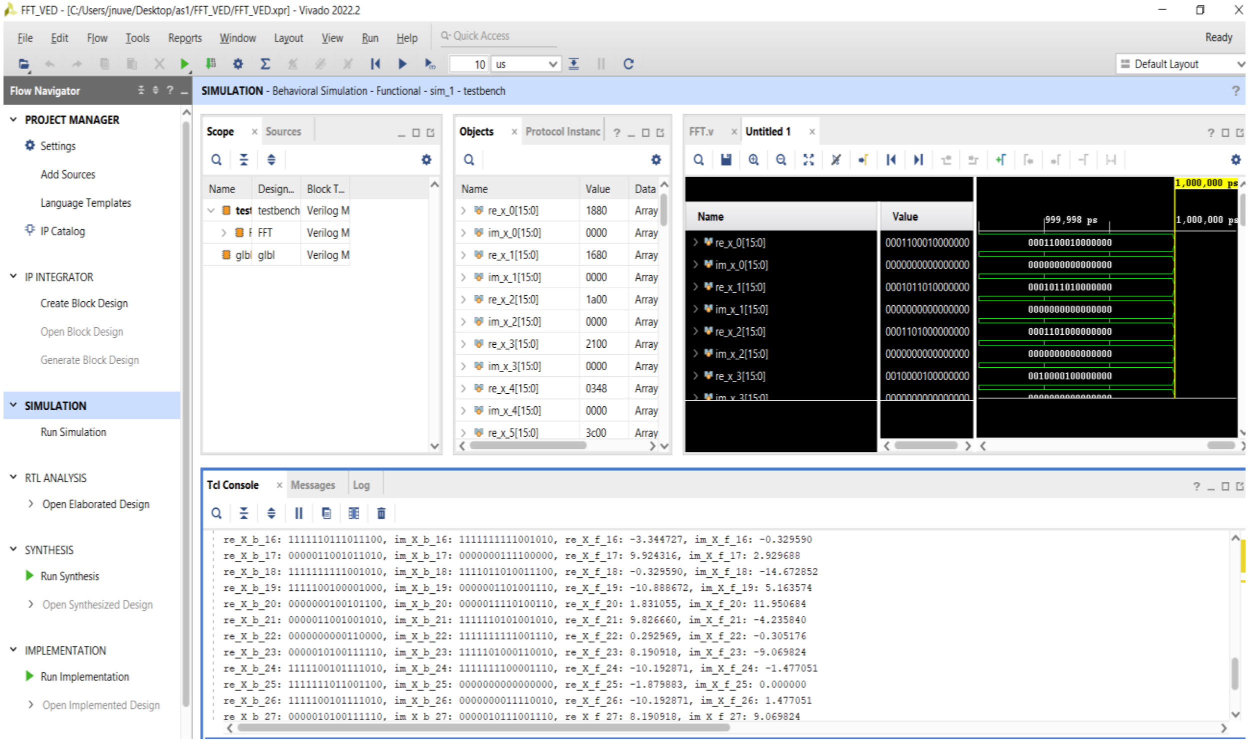
Input (x[n])	Simulation Results([X[n])	Online calculator results
0.7656	**2.978+0j**	**2.975+0j**
0.703	**9.509+5.603j**	**9.513+5.612j**
0.813	**2.136-5.505j**	**2.136-551j**
1.0313	**4.223-8.020j**	**4.227-8.023j**
0.1025	**-8.508-4.26j**	**-8.516-4.257j**
1.875	**6.225+1.110j**	**6.23+1.112j**
1.5	**-5.517-2.624j**	**-5.538-2.627j**
2.0	**-4.699+2.954**	**-4.697+2.962j**
-3.996	**6.013 + 5.79j**	**6 + 5.8j**
1	**5.859 -4.992j**	**5.869 -4.991j**
0.017	**0.342+2.575j**	**0.337 + 2.571j**
0.047	**7.678-12.175j**	**7.681 – 12.179j**
0.508	**-19.226 -2.404j**	**-19.248 – 2.411j**



```
re_X_b_0: 0000000111101000, im_X_b_0: 0000000000000000, re_X_f_0: 2.978516, im_X_f_0: 0.000000
re_X_b_1: 0000011000010110, im_X_b_1: 0000001110010110, re_X_f_1: 9.509277, im_X_f_1: 5.603027
re_X_b_2: 0000000101011110, im_X_b_2: 1111110001111010, re_X_f_2: 2.136230, im_X_f_2: -5.505371
re_X_b_3: 0000001010110100, im_X_b_3: 1111101011011110, re_X_f_3: 4.223633, im_X_f_3: -8.020020
re_X_b_4: 1111101010001110, im_X_b_4: 1111110101000110, re_X_f_4: -8.508301, im_X_f_4: -4.260254
re_X_b_5: 0000001111111100, im_X_b_5: 0000000010110110, re_X_f_5: 6.225586, im_X_f_5: 1.110840
re_X_b_6: 1111110001111000, im_X_b_6: 1111111001010010, re_X_f_6: -5.517578, im_X_f_6: -2.624512
re_X_b_7: 1111110011111110, im_X_b_7: 0000000111100100, re_X_f_7: -4.699707, im_X_f_7: 2.954102
re_X_b_9: 0000001111000000, im_X_b_9: 1111110011001110, re_X_f_9: 5.859375, im_X_f_9: -4.992676
re_X_b_10: 0000000000111000, im_X_b_10: 0000000110100110, re_X_f_10: 0.341797, im_X_f_10: 2.575684
re_X_b_11: 0000010011101010, im_X_b_11: 1111100000111000, re_X_f_11: 7.678223, im_X_f_11: -12.158203
re_X_b_12: 1111001110110010, im_X_b_12: 1111111001110110, re_X_f_12: -19.226074, im_X_f_12: -2.404785
re_X_b_13: 0000010001110010, im_X_b_13: 0000010000011010, re_X_f_13: 6.945801, im_X_f_13: 6.408691
re_X_b_14: 1111110100011010, im_X_b_14: 0000000010100000, re_X_f_14: -4.528809, im_X_f_14: 0.976562
re_X_b_15: 0000010001101000, im_X_b_15: 0000001000011010, re_X_f_15: 6.884766, im_X_f_15: 3.283691
re_X_b_16: 1111110111011100, im_X_b_16: 1111111111001010, re_X_f_16: -3.344727, im_X_f_16: -0.329590
re_X_b_17: 0000011001011010, im_X_b_17: 0000000111100000, re_X_f_17: 9.924316, im_X_f_17: 2.929688
re_X_b_18: 1111111111001010, im_X_b_18: 1111011010011100, re_X_f_18: -0.329590, im_X_f_18: -14.672852
re_X_b_19: 1111100100001000, im_X_b_19: 0000001101001110, re_X_f_19: -10.888672, im_X_f_19: 5.163574
re_X_b_20: 0000000100101100, im_X_b_20: 0000011110100110, re_X_f_20: 1.831055, im_X_f_20: 11.950684
re_X_b_21: 0000011001001010, im_X_b_21: 1111110101001010, re_X_f_21: 9.826660, im_X_f_21: -4.235840
re_X_b_22: 0000000000110000, im_X_b_22: 1111111111001110, re_X_f_22: 0.292969, im_X_f_22: -0.305176
re_X_b_23: 0000010100111110, im_X_b_23: 1111101000110010, re_X_f_23: 8.190918, im_X_f_23: -9.069824
re_X_b_24: 1111100101111010, im_X_b_24: 1111111100001110, re_X_f_24: -10.192871, im_X_f_24: -1.477051
re_X_b_25: 1111111011001100, im_X_b_25: 0000000000000000, re_X_f_25: -1.879883, im_X_f_25: 0.000000
```

```
re_X_b_26: 1111100101111010, im_X_b_26: 0000000011110010, re_X_f_26: -10.192871, im_X_f_26: 1.477051
re_X_b_27: 0000010100111110, im_X_b_27: 0000010111001110, re_X_f_27: 8.190918, im_X_f_27: 9.069824
re_X_b_28: 0000000000110000, im_X_b_28: 0000000000110010, re_X_f_28: 0.292969, im_X_f_28: 0.305176
re_X_b_29: 0000011001001010, im_X_b_29: 0000001010110110, re_X_f_29: 9.826660, im_X_f_29: 4.235840
re_X_b_30: 0000000100101100, im_X_b_30: 1111100001011010, re_X_f_30: 1.831055, im_X_f_30: -11.950684
re_X_b_31: 1111100100001000, im_X_b_31: 1111110010110010, re_X_f_31: -10.888672, im_X_f_31: -5.163574
re_X_b_32: 1111111111001010, im_X_b_32: 0000100101100100, re_X_f_32: -0.329590, im_X_f_32: 14.672852
re_X_b_33: 0000011001011010, im_X_b_33: 1111111000100000, re_X_f_33: 9.924316, im_X_f_33: -2.929688
re_X_b_34: 1111110111011100, im_X_b_34: 0000000000110110, re_X_f_34: -3.344727, im_X_f_34: 0.329590
re_X_b_35: 0000010001101000, im_X_b_35: 1111110111100110, re_X_f_35: 6.884766, im_X_f_35: -3.283691
re_X_b_36: 1111110100011010, im_X_b_36: 1111111101100000, re_X_f_36: -4.528809, im_X_f_36: -0.976562
re_X_b_37: 0000010001110010, im_X_b_37: 1111101111100110, re_X_f_37: 6.945801, im_X_f_37: -6.408691
re_X_b_38: 1111001110110010, im_X_b_38: 0000000110001010, re_X_f_38: -19.226074, im_X_f_38: 2.404785
re_X_b_39: 0000010011101010, im_X_b_39: 0000011111001000, re_X_f_39: 7.678223, im_X_f_39: 12.158203
re_X_b_40: 0000000000111000, im_X_b_40: 1111111001011010, re_X_f_40: 0.341797, im_X_f_40: -2.575684
re_X_b_41: 0000001111000000, im_X_b_41: 0000001100110010, re_X_f_41: 5.859375, im_X_f_41: 4.992676
re_X_b_42: 0000001111010110, im_X_b_42: 1111110001001100, re_X_f_42: 5.993652, im_X_f_42: -5.786133
re_X_b_43: 1111110011111110, im_X_b_43: 1111111000011100, re_X_f_43: -4.699707, im_X_f_43: -2.954102
re_X_b_44: 1111110001111000, im_X_b_44: 0000000110101110, re_X_f_44: -5.517578, im_X_f_44: 2.624512
re_X_b_45: 0000001111111100, im_X_b_45: 1111111101001010, re_X_f_45: 6.225586, im_X_f_45: -1.110840
re_X_b_46: 1111101010001110, im_X_b_46: 0000001010111010, re_X_f_46: -8.508301, im_X_f_46: 4.260254
re_X_b_47: 0000001010110100, im_X_b_47: 0000010100100010, re_X_f_47: 4.223633, im_X_f_47: 8.020020
re_X_b_48: 0000000101011110, im_X_b_48: 0000001110000110, re_X_f_48: 2.136230, im_X_f_48: 5.505371
re_X_b_49: 0000011000010110, im_X_b_49: 1111110001101010, re_X_f_49: 9.509277, im_X_f_49: -5.603027
```

Output displayed in console



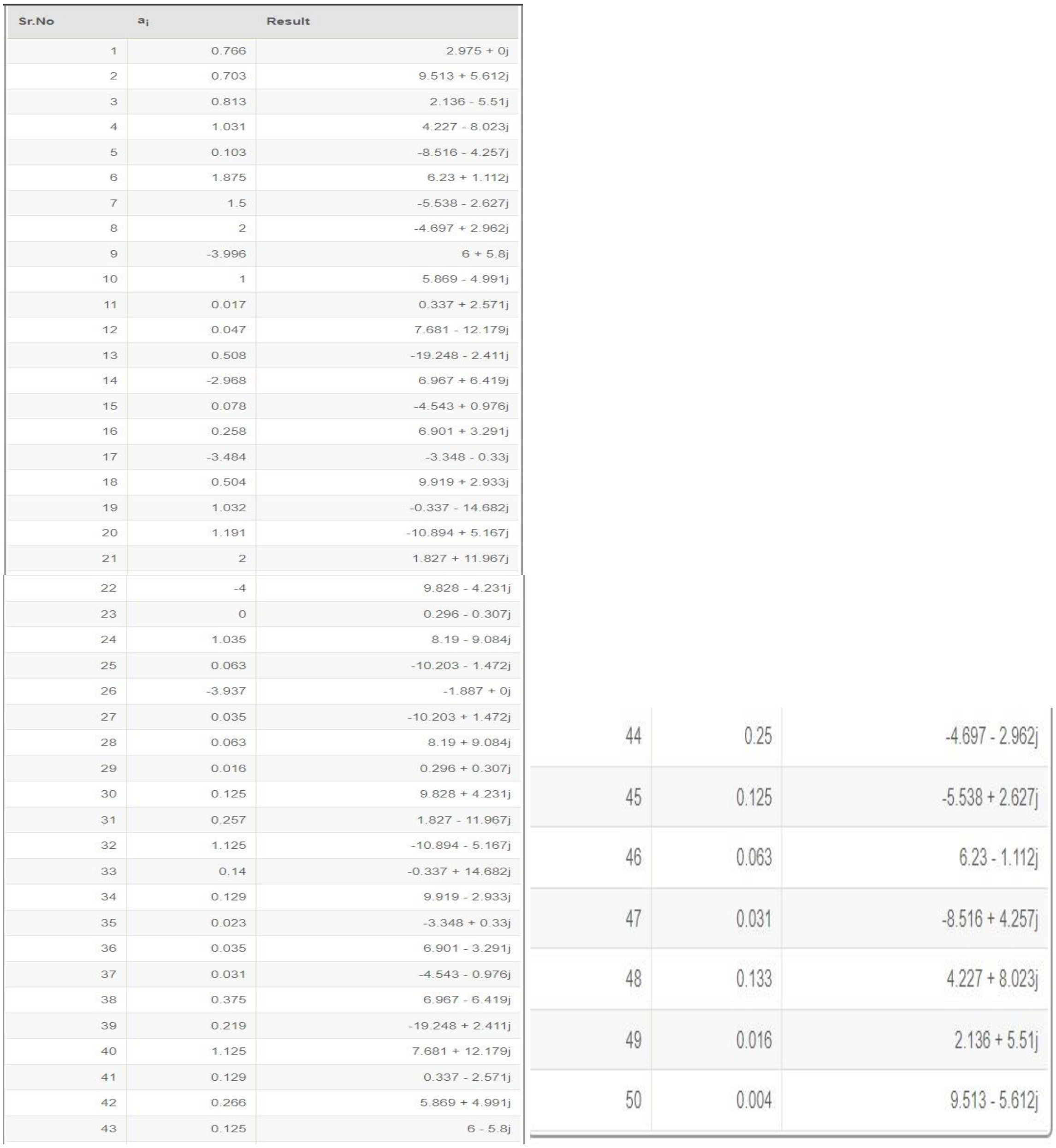
Name	Design...	Block T...
test	testbench	Verilog M
F	FFT	Verilog M
glbl	glbl	Verilog M

Name	Value	Data
re_x_0[15:0]	1880	Array
im_x_0[15:0]	0000	Array
re_x_1[15:0]	1680	Array
im_x_1[15:0]	0000	Array
re_x_2[15:0]	1a00	Array
im_x_2[15:0]	0000	Array
re_x_3[15:0]	2100	Array
im_x_3[15:0]	0000	Array
re_x_4[15:0]	0348	Array
im_x_4[15:0]	0000	Array
re_x_5[15:0]	3c00	Array

Name	Value	999,998 ps
re_x_0[15:0]	0001100010000000	0001100010000000
im_x_0[15:0]	0000000000000000	0000000000000000
re_x_1[15:0]	0001011010000000	0001011010000000
im_x_1[15:0]	0000000000000000	0000000000000000
re_x_2[15:0]	0001101000000000	0001101000000000
im_x_2[15:0]	0000000000000000	0000000000000000
re_x_3[15:0]	0010000100000000	0010000100000000
im_x_3[15:0]	0000000000000000	0000000000000000

1,000,000 ps

```
re_X_b_16: 1111110111011100, im_X_b_16: 1111111111001010, re_X_f_16: -3.344727, im_X_f_16: -0.329590
re_X_b_17: 0000011001011010, im_X_b_17: 0000000111100000, re_X_f_17: 9.924316, im_X_f_17: 2.929688
re_X_b_18: 1111111111001010, im_X_b_18: 1111011010011100, re_X_f_18: -0.329590, im_X_f_18: -14.672852
re_X_b_19: 1111100100001000, im_X_b_19: 0000001101001110, re_X_f_19: -10.888672, im_X_f_19: 5.163574
re_X_b_20: 0000000100101100, im_X_b_20: 0000011110100110, re_X_f_20: 1.831055, im_X_f_20: 11.950684
re_X_b_21: 0000011001001010, im_X_b_21: 1111110101001010, re_X_f_21: 9.826660, im_X_f_21: -4.235840
re_X_b_22: 0000000000110000, im_X_b_22: 1111111111001110, re_X_f_22: 0.292969, im_X_f_22: -0.305176
re_X_b_23: 0000010100111110, im_X_b_23: 1111101000110010, re_X_f_23: 8.190918, im_X_f_23: -9.069824
re_X_b_24: 1111100101111010, im_X_b_24: 1111111100001110, re_X_f_24: -10.192871, im_X_f_24: -1.477051
re_X_b_25: 1111111011001100, im_X_b_25: 0000000000000000, re_X_f_25: -1.879883, im_X_f_25: 0.000000
re_X_b_26: 1111100101111010, im_X_b_26: 0000000011110010, re_X_f_26: -10.192871, im_X_f_26: 1.477051
re X b 27: 0000010100111110, im X b 27: 0000010111001110, re X f 27: 8.190918, im X f 27: 9.069824
```

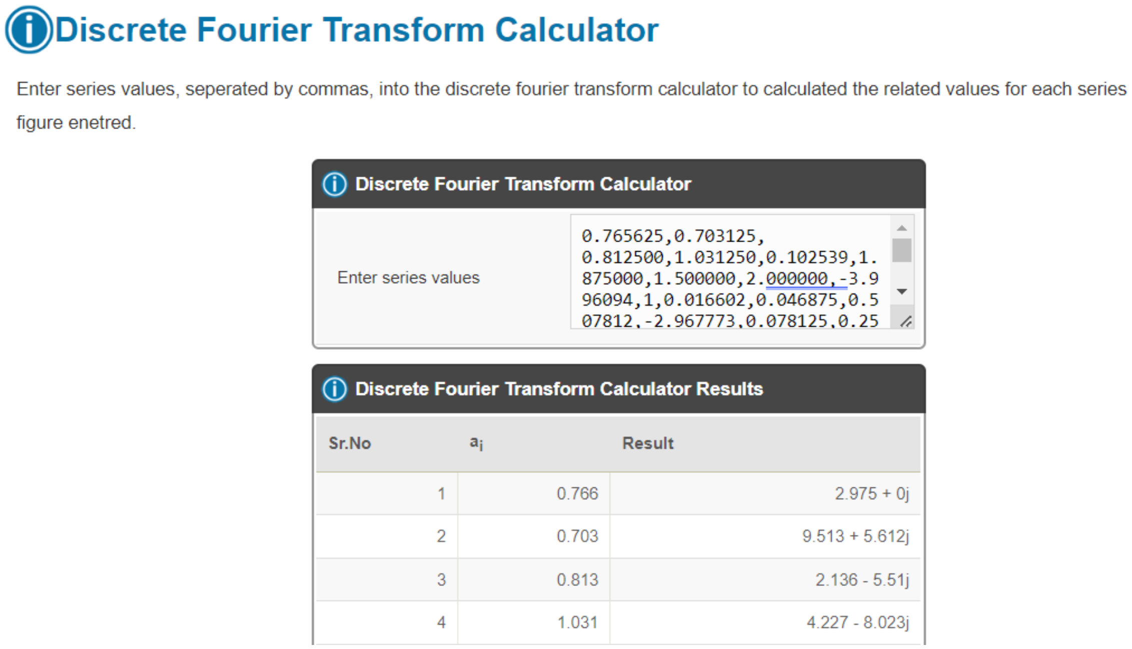


Sr.No	a_i	Result
1	0.766	2.975 + 0j
2	0.703	9.513 + 5.612j
3	0.813	2.136 - 5.51j
4	1.031	4.227 - 8.023j
5	0.103	-8.516 - 4.257j
6	1.875	6.23 + 1.112j
7	1.5	-5.538 - 2.627j
8	2	-4.697 + 2.962j
9	-3.996	6 + 5.8j
10	1	5.869 - 4.991j
11	0.017	0.337 + 2.571j
12	0.047	7.681 - 12.179j
13	0.508	-19.248 - 2.411j
14	-2.968	6.967 + 6.419j
15	0.078	-4.543 + 0.976j
16	0.258	6.901 + 3.291j
17	-3.484	-3.348 - 0.33j
18	0.504	9.919 + 2.933j
19	1.032	-0.337 - 14.682j
20	1.191	-10.894 + 5.167j
21	2	1.827 + 11.967j
22	-4	9.828 - 4.231j
23	0	0.296 - 0.307j
24	1.035	8.19 - 9.084j
25	0.063	-10.203 - 1.472j
26	-3.937	-1.887 + 0j
27	0.035	-10.203 + 1.472j
28	0.063	8.19 + 9.084j
29	0.016	0.296 + 0.307j
30	0.125	9.828 + 4.231j
31	0.257	1.827 - 11.967j
32	1.125	-10.894 - 5.167j
33	0.14	-0.337 + 14.682j
34	0.129	9.919 - 2.933j
35	0.023	-3.348 + 0.33j
36	0.035	6.901 - 3.291j
37	0.031	-4.543 - 0.976j
38	0.375	6.967 - 6.419j
39	0.219	-19.248 + 2.411j
40	1.125	7.681 + 12.179j
41	0.129	0.337 - 2.571j
42	0.266	5.869 + 4.991j
43	0.125	6 - 5.8j
44	0.25	-4.697 - 2.962j
45	0.125	-5.538 + 2.627j
46	0.063	6.23 - 1.112j
47	0.031	-8.516 + 4.257j
48	0.133	4.227 + 8.023j
49	0.016	2.136 + 5.51j
50	0.004	9.513 - 5.612j

Output from Online Calculator

2: Precision Handling: Throughout the computation, itmaintains the precision format of [sign + 15 bits] {Sign + 2 (integer) + 13 (fractional)} and scaled by using this **(re_x_i*(2.0**-13){i is 0 to 49}.**

3: Cross-Validation with Reference: The outputs match within acceptable tolerances with online FFT calculator.



Discrete Fourier Transform Calculator

Enter series values, seperated by commas, into the discrete fourier transform calculator to calculated the related values for each series figure enetred.

Discrete Fourier Transform Calculator

Enter series values

```
0.765625,0.703125,
0.812500,1.031250,0.102539,1.
875000,1.500000,2.000000,-3.9
96094,1,0.016602,0.046875,0.5
07812,-2.967773,0.078125,0.25
```

Discrete Fourier Transform Calculator Results

Sr.No	a_i	Result
1	0.766	2.975 + 0j
2	0.703	9.513 + 5.612j
3	0.813	2.136 - 5.51j
4	1.031	4.227 - 8.023j

7. Physical Hierarchy

7.1 Floorplanning

- Aspect Ratio=1
- Core utilization=0.7
- Core to die boundary =>
  - core to left =4.5
  - core to right =4.5
  - core to top =4.5
  - core to bottom =4.5

7.2 Layout Strategy

Core Margins all with width =4.5 from boundary

Ring Configuration Top Layer ME(8) width=0.4 spacing=0.985
Bottom Layer ME(8) width=0.4 spacing=0.985
Left Layer ME(7) width=0.4 spacing=0.985
Right Layer ME(7) width=0.4spacing=0.985

Stripes Layer -ME6(6) with Vertical Direction
Width=0.4 spacing =0.4
set to set distance =2.5

SRoute → Top Layer ME8(8) to Bottom Layer ME1(1)

10. Issues known at submission date

Server getting killed multiple times while doing placement of design so unable to do steps after that.