CLASS: S.E. COMP **SUBJECT :DEL**

EXPT. NO.: 06 **DATE:**

TITLE : Parity Generator and Checker

OBJECTIVE :

1. Design and Implement Parity Generator and checker using EX-OR.

APPARATUS :

Digital-Board, GP-4Patch-Cords, IC-74LS86 and Required Logic gates if any.

THEORY :

Parity Generator

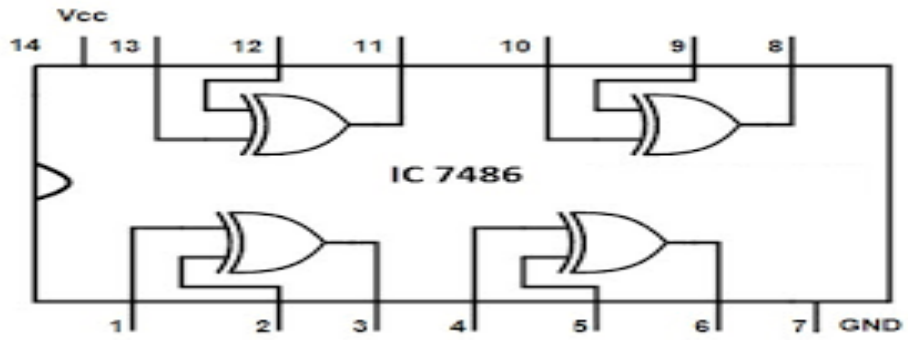
It is combinational circuit that accepts an n-1 bit stream data and generates the additional bit that is to be transmitted with the bit stream. This additional or extra bit is termed as a parity bit. In **even parity** bit scheme, the parity bit is '**0**' if there are **even number of 1s** in the data stream and the parity bit is '**1**' if there are **odd number of 1s** in the data stream. In **odd parity** bit scheme, the parity bit is '**1**' if there are **even number of 1**s in the data stream and the parity bit is '**0**' if there are **odd number of 1s** in the data stream. Let us discuss both even and odd parity generators.

Parity Checker

It is a logic circuit that checks for possible errors in the transmission. This circuit can be an even parity checker or odd parity checker depending on the type of parity generated at the transmission end. When this circuit is used as even parity checker, the number of input bits must always be even. When a parity error occurs, the 'sum even' output goes low and 'sum odd' output goes high. If this logic circuit is used as an odd parity checker,

the number of input bits should be odd, but if an error occurs the 'sum odd' output goes low and 'sum even' output goes high.

PIN DIAGRAM:



PROCEDURE :

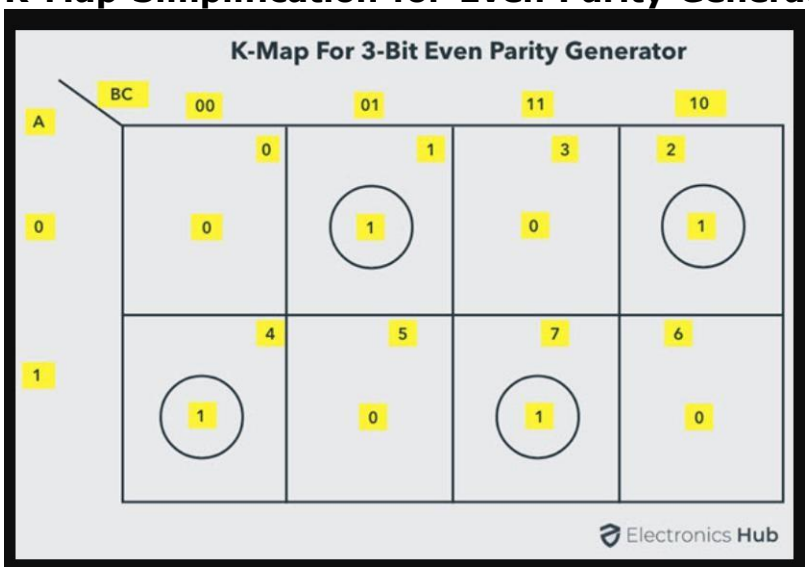
1. Make the connections as per the Logic circuit of Even Parity Generator circuit and Verify its Truth Table.
2. Make the connections as per the Logic circuit of Odd Parity Generator circuit and Verify its Truth Table.
3. Make the connections as per the Logic circuit of Even Parity Checker circuit and Verify its Truth Table.
4. Make the connections as per the Logic circuit of Odd Parity Generator circuit and Verify its Truth Table.

Design of Even Parity Generator:

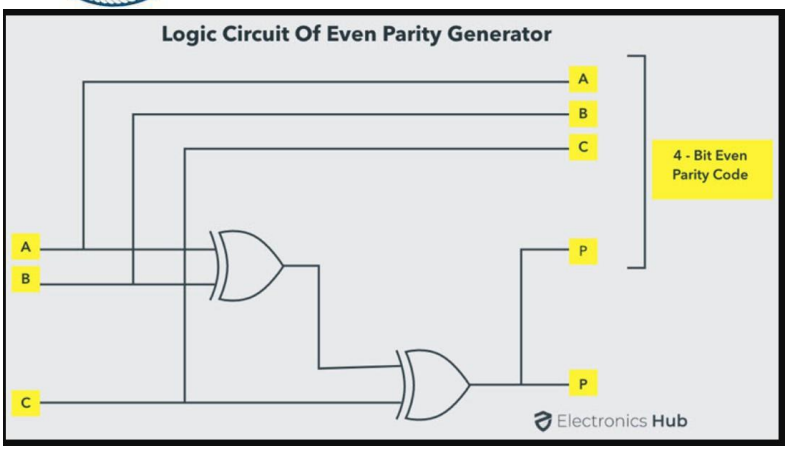
Truth Table:

3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

K-Map Simplification for Even Parity Generator



Logic Diagram:

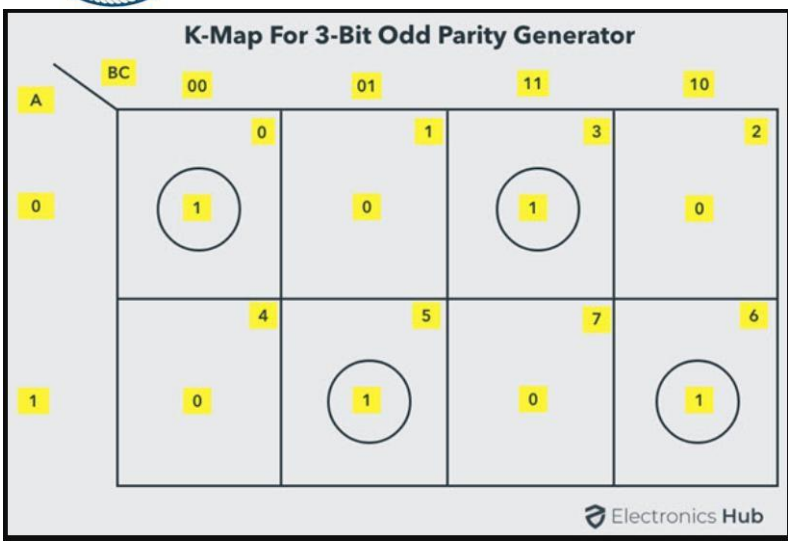


Design of odd Parity Generator:

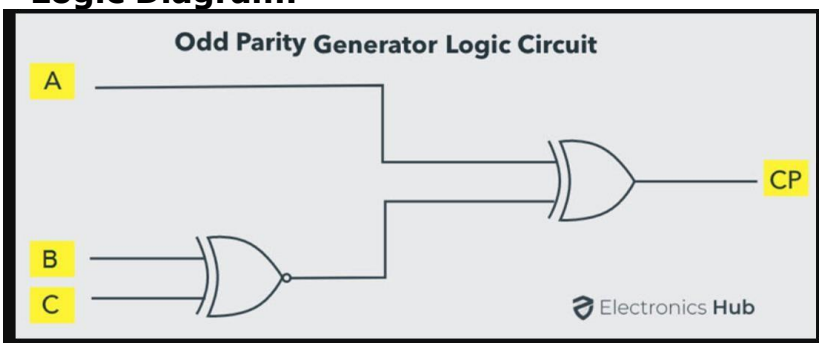
Truth Table:

3-bit message			Odd parity bit generator (P)
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

K-Map Simplification for Odd Parity Generator :



Logic Diagram:

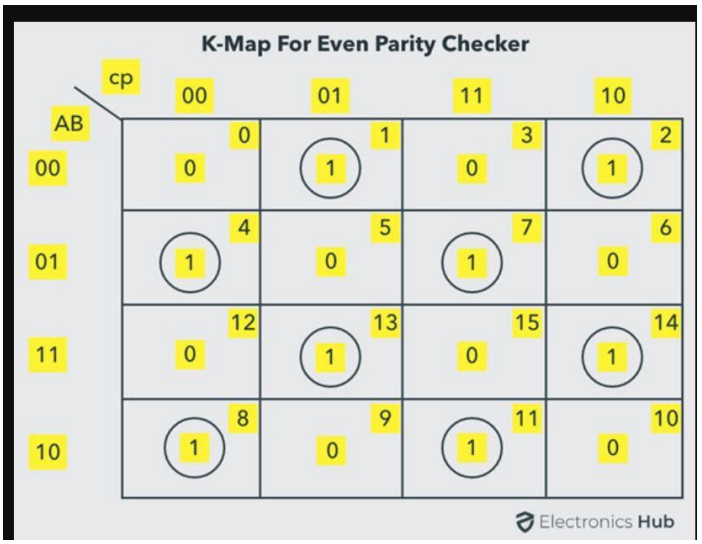


Design of Even Parity Checker:

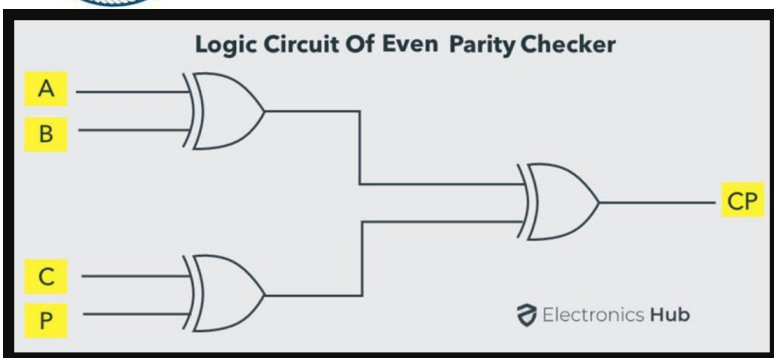
Truth Table:

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

K-Map Simplification for Even Parity Checker :



Logic Diagram:

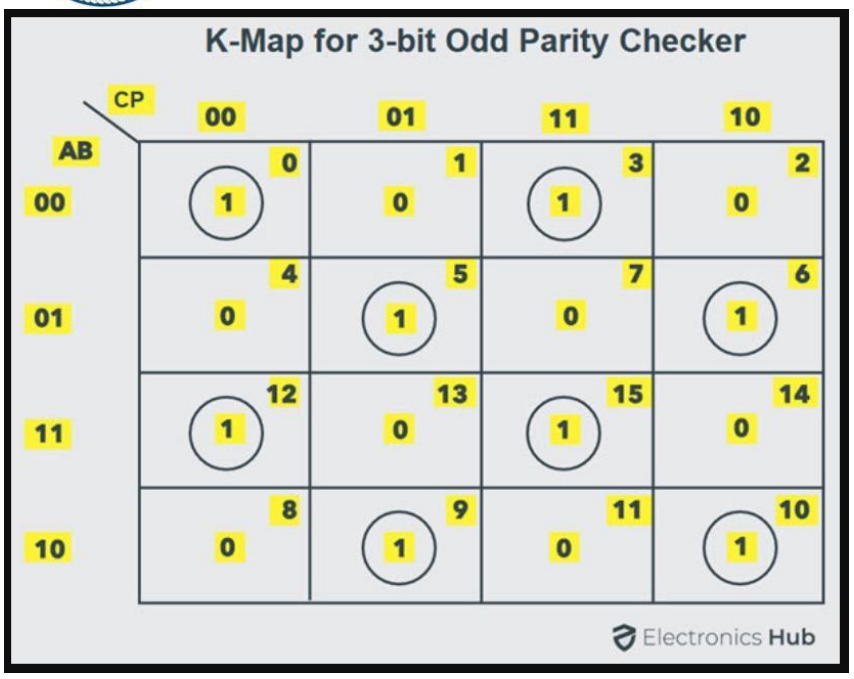


Design of odd Parity Checker:

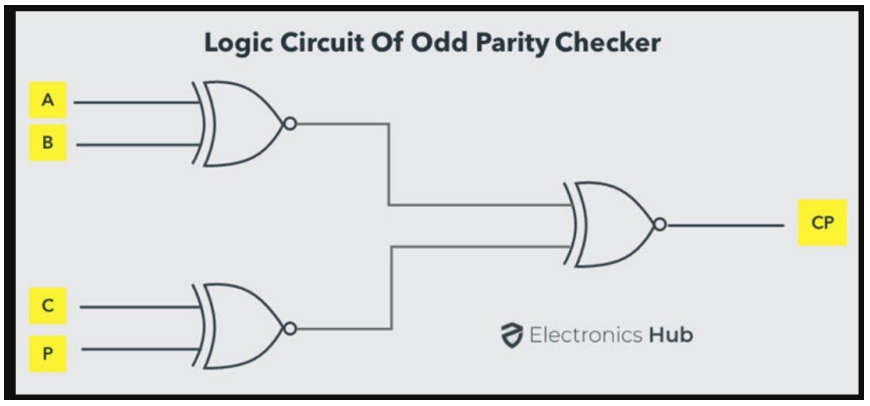
Truth Table:

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

K-Map Simplification for Odd Parity Checker :



Logic Diagram:



Logic Gates / MSI Device required for Implementation:

Sr.No.	Title	Name of the IC	Number of Gates required	IC Required
01	Even Parity Generator			
02	Odd Parity Generator			
03	Even Parity Checker			
04	Odd Parity Checker			

CONCLUSION:

After completion student will be able to understand working of parity checker and parity generator. The students are able to design and implement the circuit by choosing appropriate ICs

REFERENCE:

1. **R.P.Jain "Modern Digital Electronics" TMH 4th Edition**
2. **D.Leach,Malvino,Saha,"Digital Principles and Applications",TMH**

Subject teacher Sign with Date Remark