COMPUTER ORGANIZATION AND ARCHITECTURE

SYLLABUS and SCHEME

William Stallings Computer Organization and Architecture

Chapter 1
Introduction

Introduction to Computer System & its sub-modules

- Computer?
- Digital electronic device
- Binary number system
- The smallest unit of information that is represented in computer is known as **Bit** (Binary Digit), which is either 0 or 1.
- Four bits together is known as **Nibble**, and Eight bits together is known as **Byte**.

ARCHITECTURE & ORGANIZATION

- **Computer Architecture** is those **attributes visible to the programmer/direct impact on logical execution of a pgm**
  - *Instruction set, number of bits used for data representation, I/O mechanisms, addressing techniques, data types*

- **Computer Organization** refers **to operational units and their interconnections** that realize the architectural **specifications-how features are implemented**
  - *Control signals, interfaces, memory technology.*

COMPUTER ARCHITECTURE	COMPUTER ORGANIZATION
Way hardware components are connected together to form a computer system.	**Structure and behaviour** of a computer system as **seen by the user**.
It acts as the interface between hardware and software.	It deals with the components of a connection in a system.
Helps us to understand the **functionalities** of a system.	How exactly all the **units in the system are arranged and interconnected.**
A programmer can **view architecture** in terms of **instructions, addressing modes and registers**.	Whereas Organization expresses the **realization of architecture.**
While **designing** a computer system **architecture is considered first**.	An organization is done on the basis of architecture.
Computer Architecture deals with high-level design issues.	Computer Organization deals with low-level design issues.
Architecture involves **Logic** (Instruction sets, Addressing modes, Data types, Cache optimization)	Organization involves **Physical Components** (Circuit design, Adders, Signals, Peripherals)

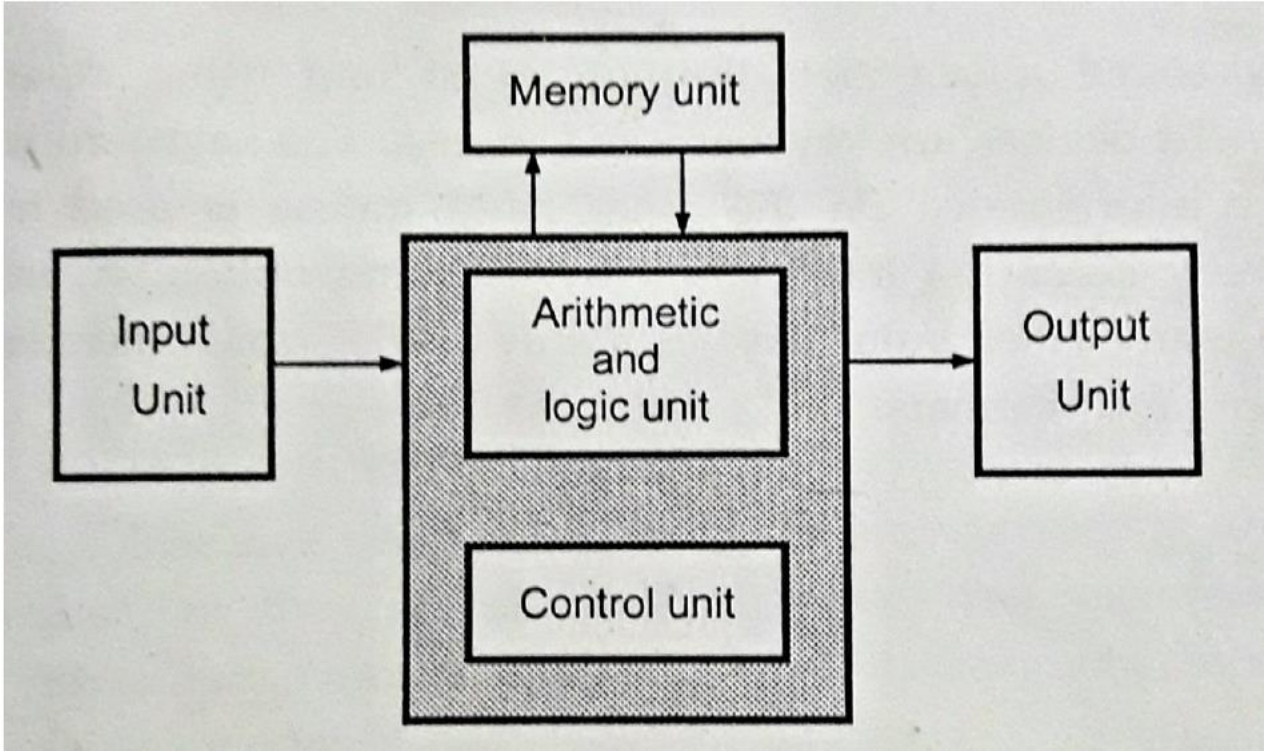
ARCHITECTURE & ORGANIZATION

- All **Intel x86** family share the same basic **architecture**
- The **IBM System/370** family share the same basic **architecture**
- This gives **code compatibility (**it can **run the same executable code**, typically machine code for a general-purpose computer CPU, that another computer system can run)
- **Organization** differs between different versions

- LATEST VERSION OF PROCESSOR IN PC??

S.NO	Processor	Clock Speed	Bus Width	MIPS	Power	Price
1	**Intel Pentium 111**	The clock speed of Intel Pentium 111 processor is 1GHz	The bus width of Intel Pentium 111 processor is 32	A million instructions per second of Intel Pentium 111 processor is ~900	The power of this processor is 97 W	$900
2	**IBM PowerPC 750X**	The clock speed of the IBM PowerPC 750X processor is 550 MHz	The bus width of the IBM PowerPC 750X processor is 32/64	A million instructions per second of IBM PowerPC 750X processor is ~1300	The power of this processor is 5 W	#900
3	MIPS R5000	The clock speed of the MIPS R5000 processor is 250 MHz	The bus width of the MIPS R5000 processor is 32/64	NA	NA	NA
4	StrongARM SA-110	The clock speed of StrongARM SA-110 processor is 233 MHz	The bus width of StrongARM SA-110processor is 32	The million instructions per second of StrongARM SA-110processor is 268	The power of this processor is 1 W	NA

Basic Organization of Computer



- **Input Unit**
- With the help of input unit **data from outside can be supplied to the computer**
- Keyboard, Mouse, Hard disk, Floppy disk, CD-ROM drive etc.

- **Memory Unit**
- The memory unit is used to **store programs and data**.
- 2 types-primary storage memory device and secondary storage memory device.
- Primary memory is also known as **Main memory or Internal memory**-storage of programs and active data – **semi-conductor memories**
  - Volatile Memory : RAM (Random Access Memory).
  - Non-Volatile Memory : ROM (Read only Memory), PROM (Programmable ROM)

- Secondary memory is also known as External memory or Auxiliary memory- **non volatile memory** and it is used for **permanent storage of data and program.**
- Examples: Hard Disk, Floppy Disk, Magnetic Tapes, etc

- **Arithmetic and Logic Unit**
- responsible for **performing arithmetic operations** such as add, subtract, division and multiplication, and **logical operations** (such as ANDing, ORing, Inverting etc)
- To perform these operations operands (object of mathematical operation) from the **main memory** are brought into high speed storage element called **registers** of the processor

- **Output Unit**
- The output unit **sends the processed results to the user using output devices** such as video monitor, printer, plotter, etc

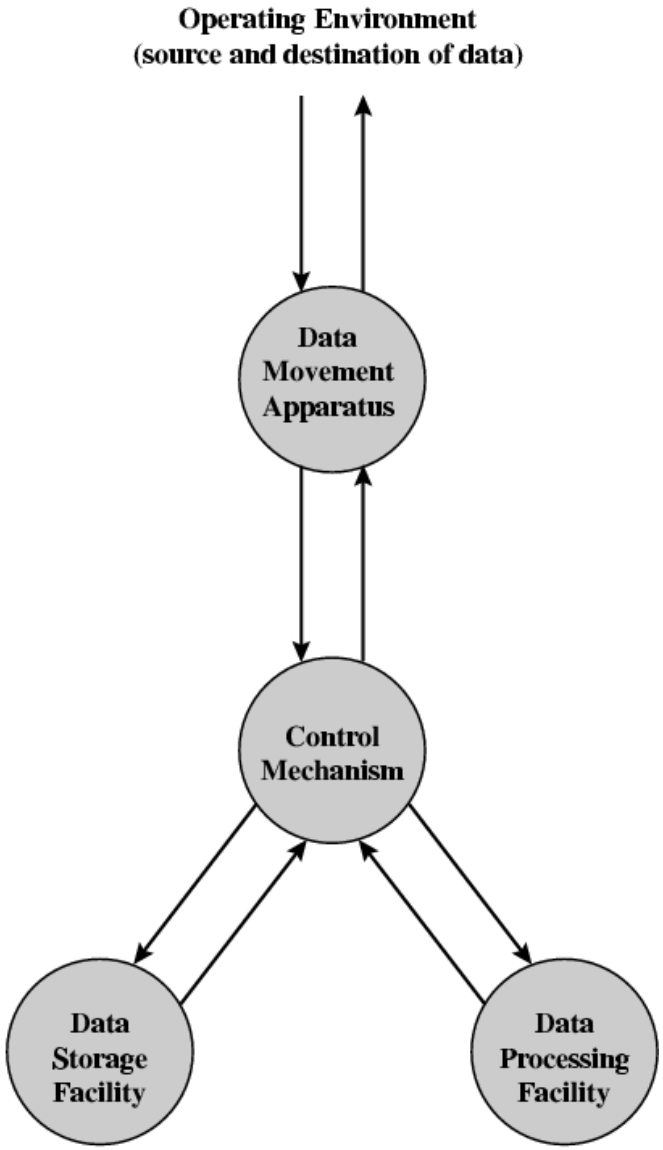
- **Control unit**
- co-ordinates and controls the activities amongst the functional units.
- fetch the instructions stored in the main memory, identify the operations and the devices involved in it, and accordingly generate control signals to execute the desired operations.
- Has a set of registers and control circuit to generate control signals.
- The arithmetic and logic unit in conjunction with control unit is commonly called Central Processing Unit (CPU).

- The input unit accepts the digital information from user with the help of input devices such as keyboard, mouse, microphone etc.
- The information received from the arithmetic and logic unit to perform the desired operation.
- The program stored in the memory decides the processing steps and the processed output is sent to the user with the help of output devices or it is stored in the memory for later reference.
- All the above mentioned activities are coordinated and controlled by the control unit.

Structure & Function

- **Structure** is the way in which **components relate** to each other
- **Function** is the **operation of individual components** as part of the structure

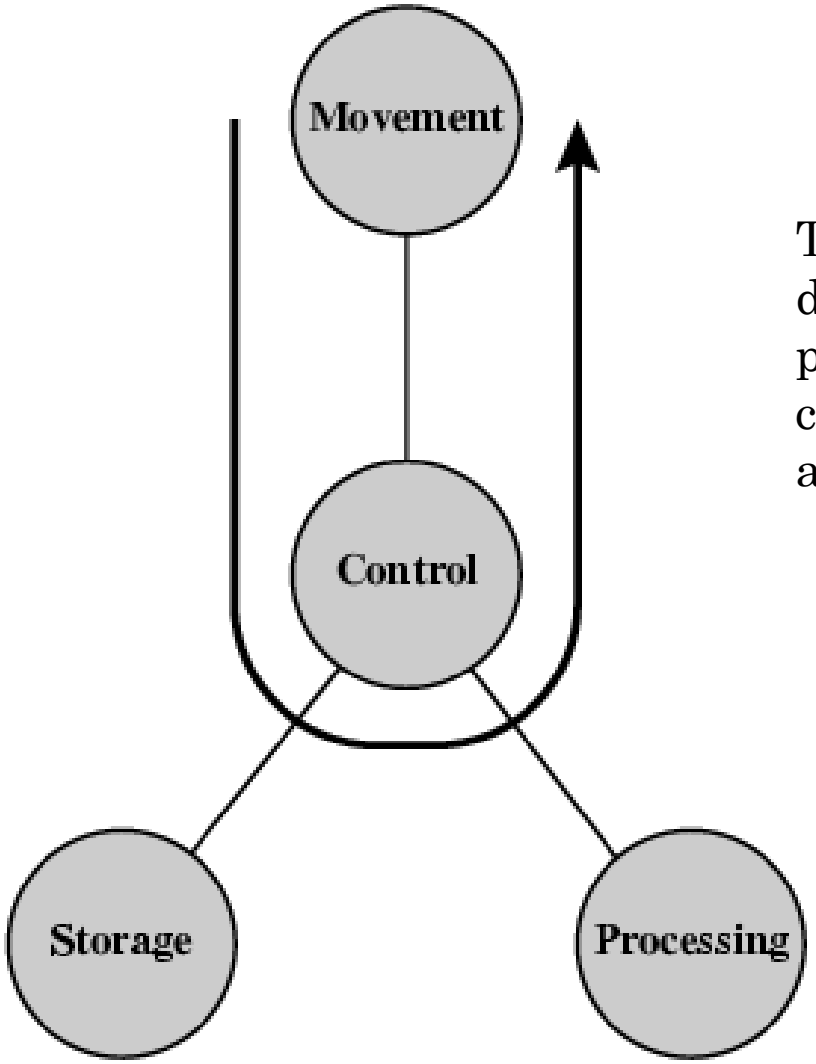
FUNCTIONAL VIEW



FUNCTION

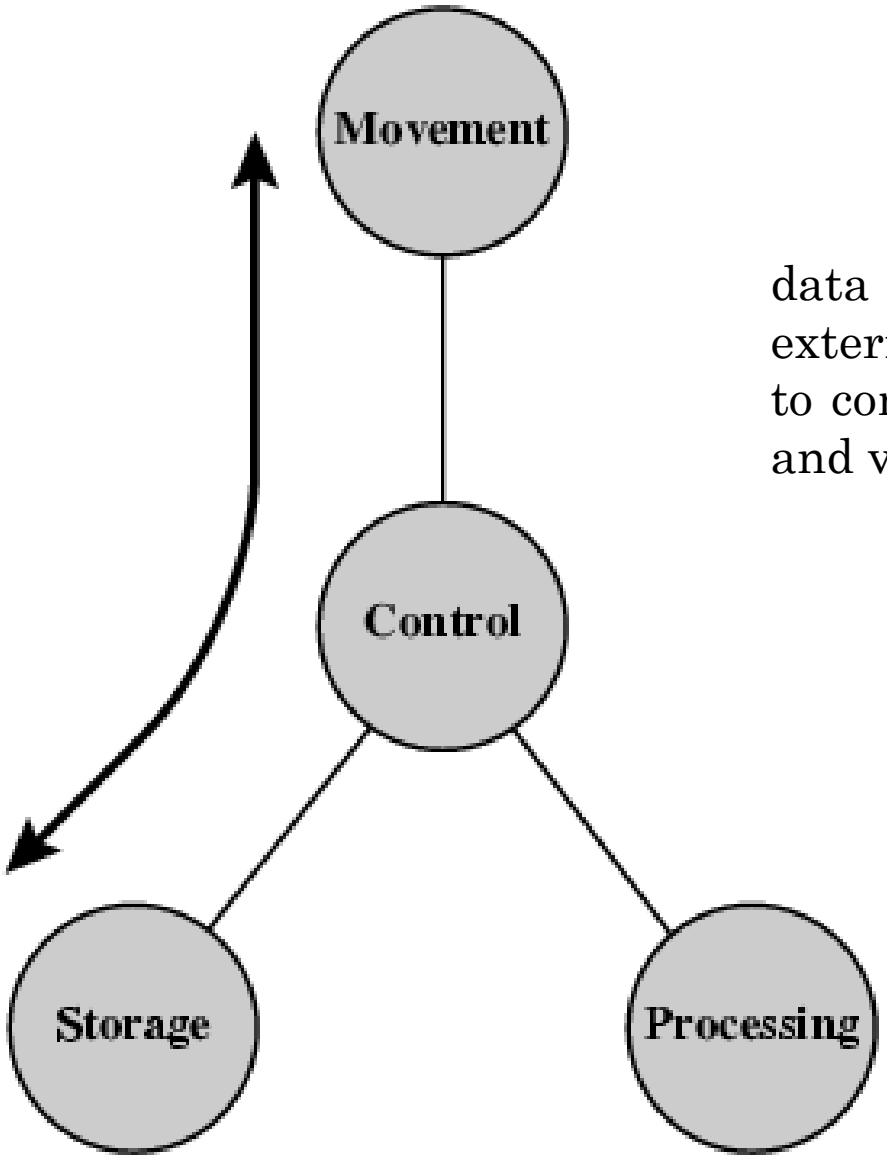
- All computer **functions** are:
- Data processing-wide variety of data and processing
- Data storage-Files of data are stored on the computer for subsequent retrieval and update
- Data movement- computer serve as sources or destinations of data-
  - When data are received from or delivered to a device that is directly connected to the computer, the process is known as **input–output (I/O), and the device is referred to as a peripheral.**
  - When data are moved over longer distances, to or from a remote device, the process is known as **data communications.**
- Control-control unit **manages** the computer's resources and orchestrates the performance of its functional parts in response to instructions.

Possible Computer Operations
Operations (a) Data movement



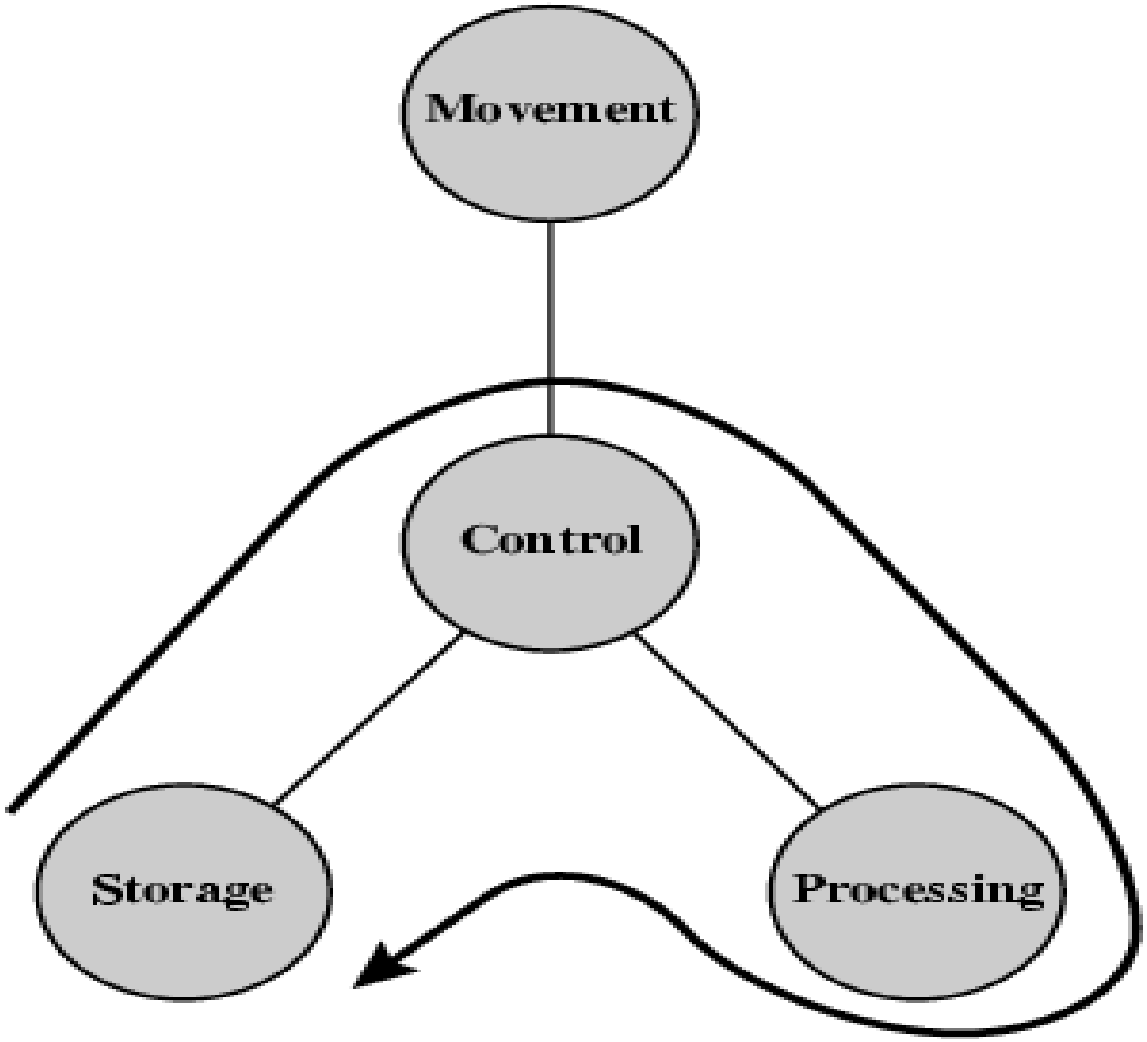
Transferring data from one peripheral or communications line to another

OPERATIONS (B) STORAGE

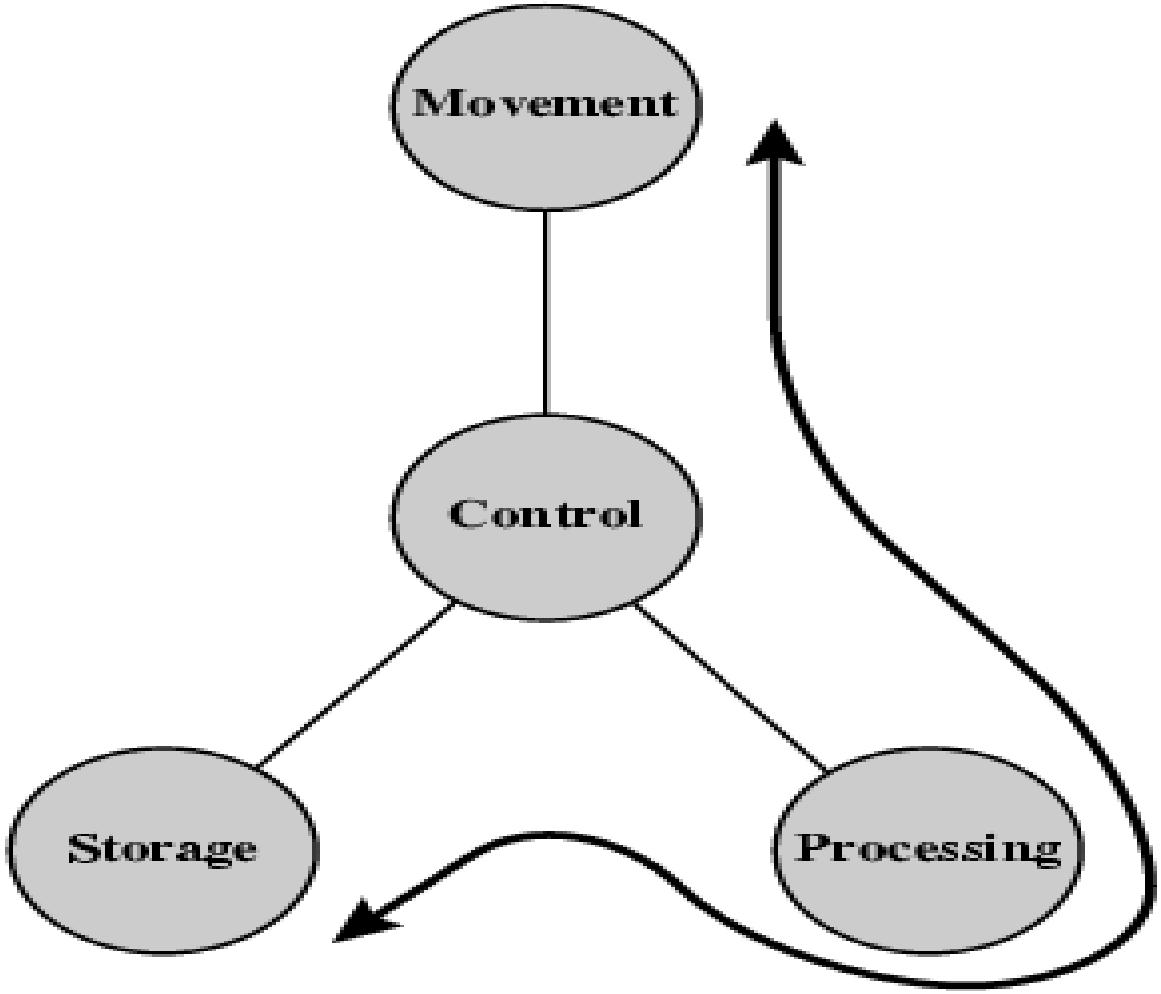


data transferred from the external environment to computer storage (read) and vice versa (write).

Operation (c) Processing from/to storage



Operation (d)
Processing from storage to I/O



COMPUTER TOP-LEVEL STRUCTURE

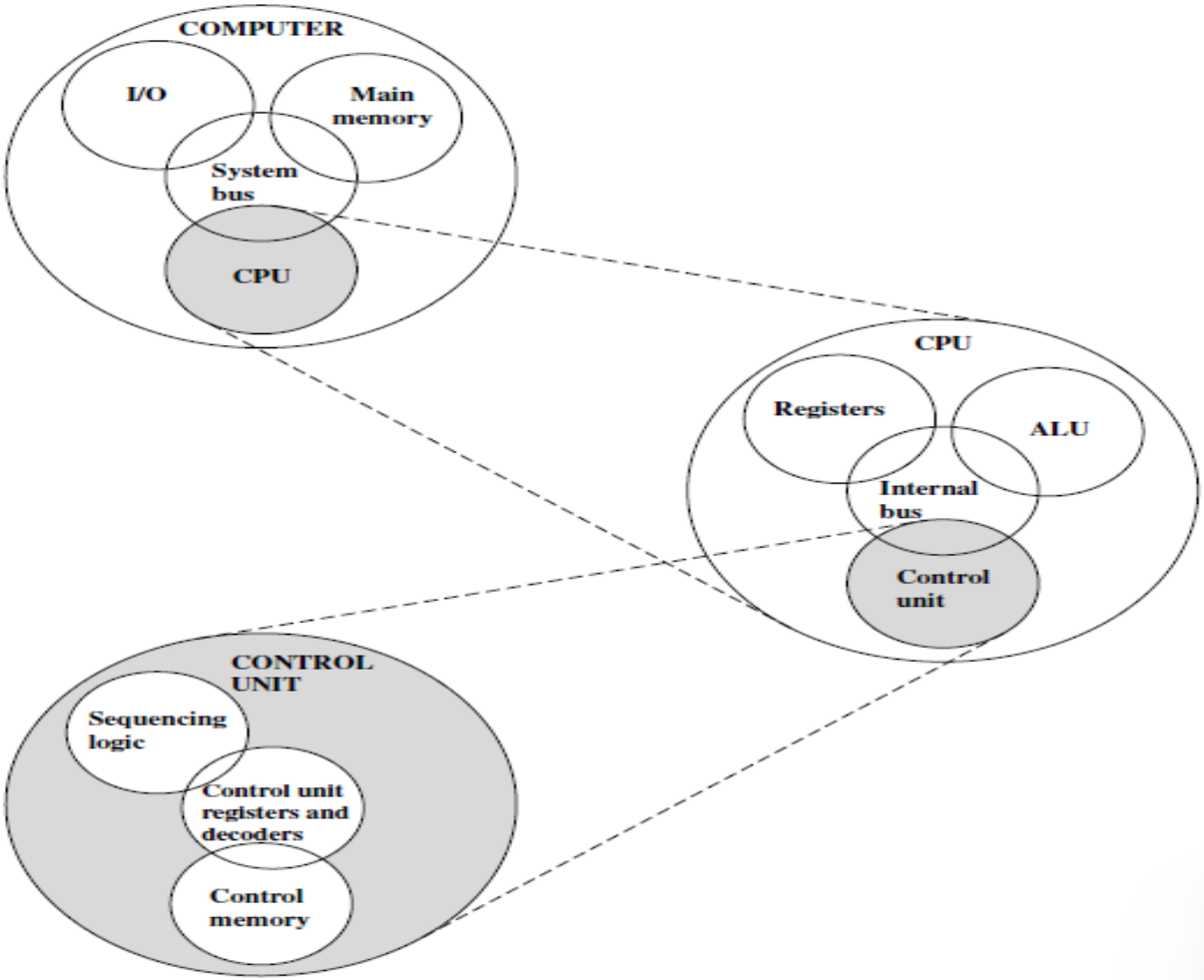
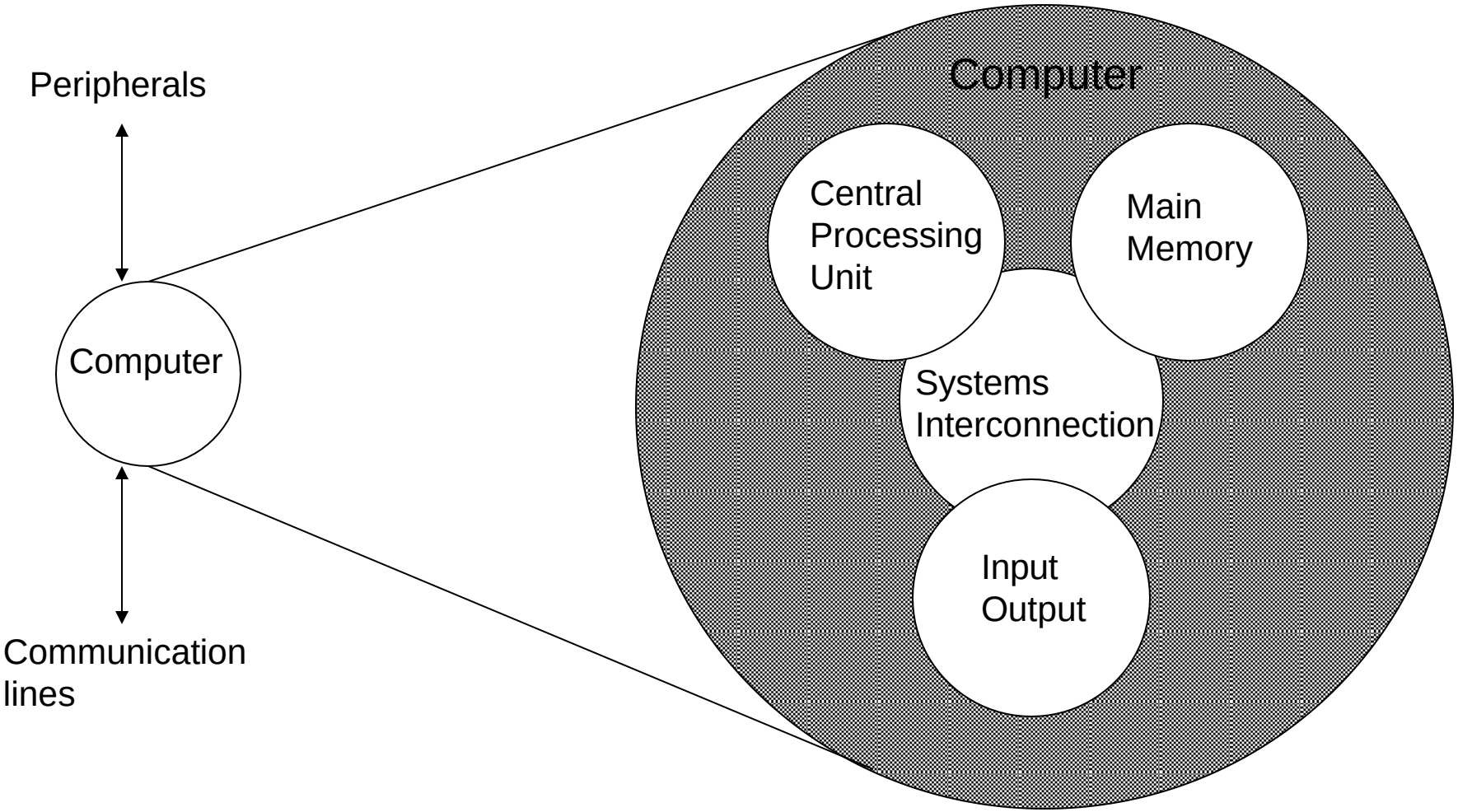


Figure 1.4 The Computer: Top-Level Structure

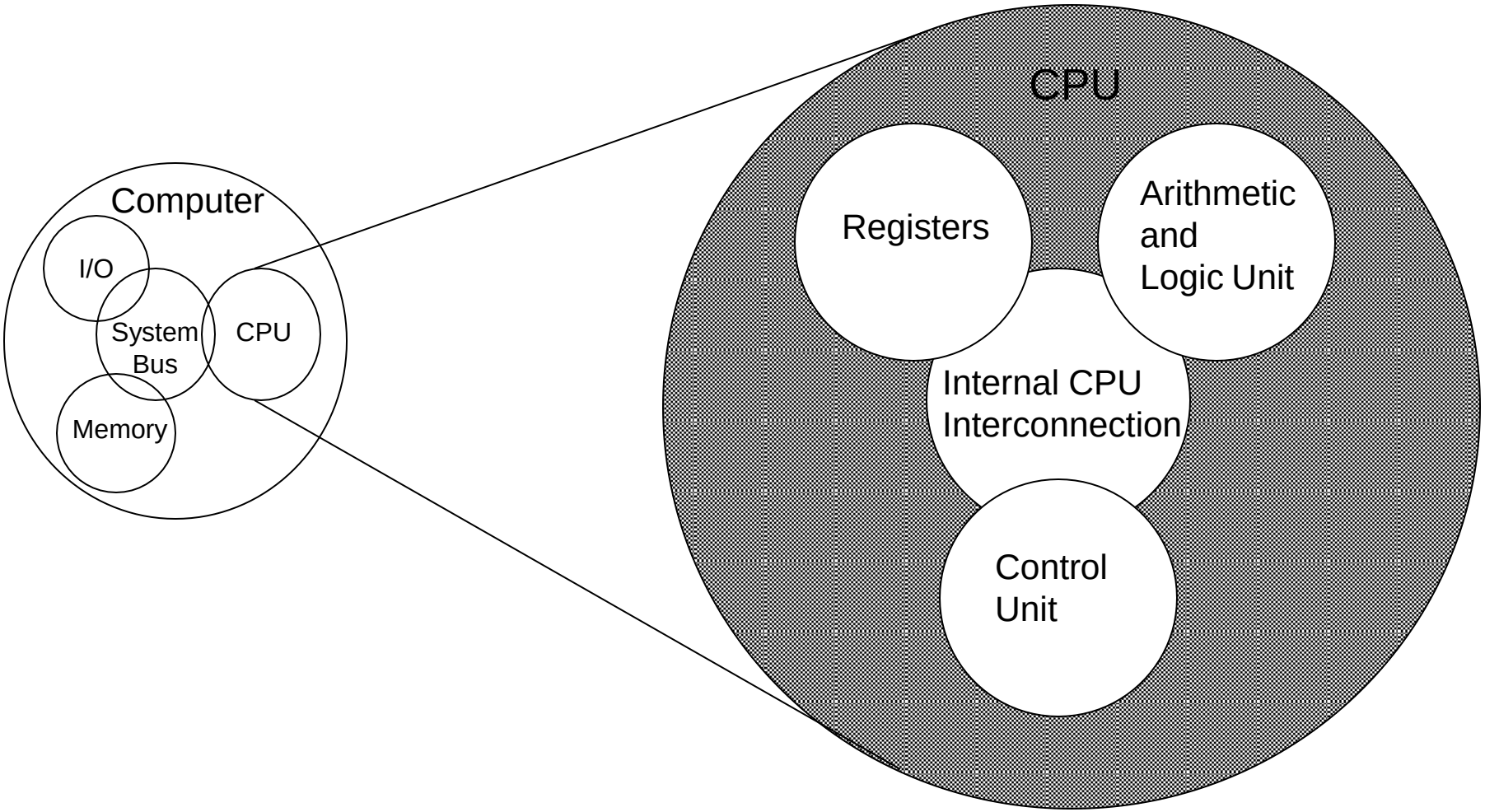
STRUCTURE - TOP LEVEL

SIMPLE SINGLE-PROCESSOR COMPUTER



- Top-down approach-beginning with a top view and decomposing the system into its subparts-effective
- ***Simple single-processor computer***
- **Central processing unit (CPU):** Controls the operation of the computer and performs its data processing functions-**processor**.
- **Main memory:** Stores data.
- **I/O:** Moves data between the computer and its external environment.
- **System interconnection:** Some mechanism that provides for communication among CPU, main memory, and I/O.
- A common example of system interconnection is by means of a **system bus**, consisting of a number of conducting wires to which all the other components attach.

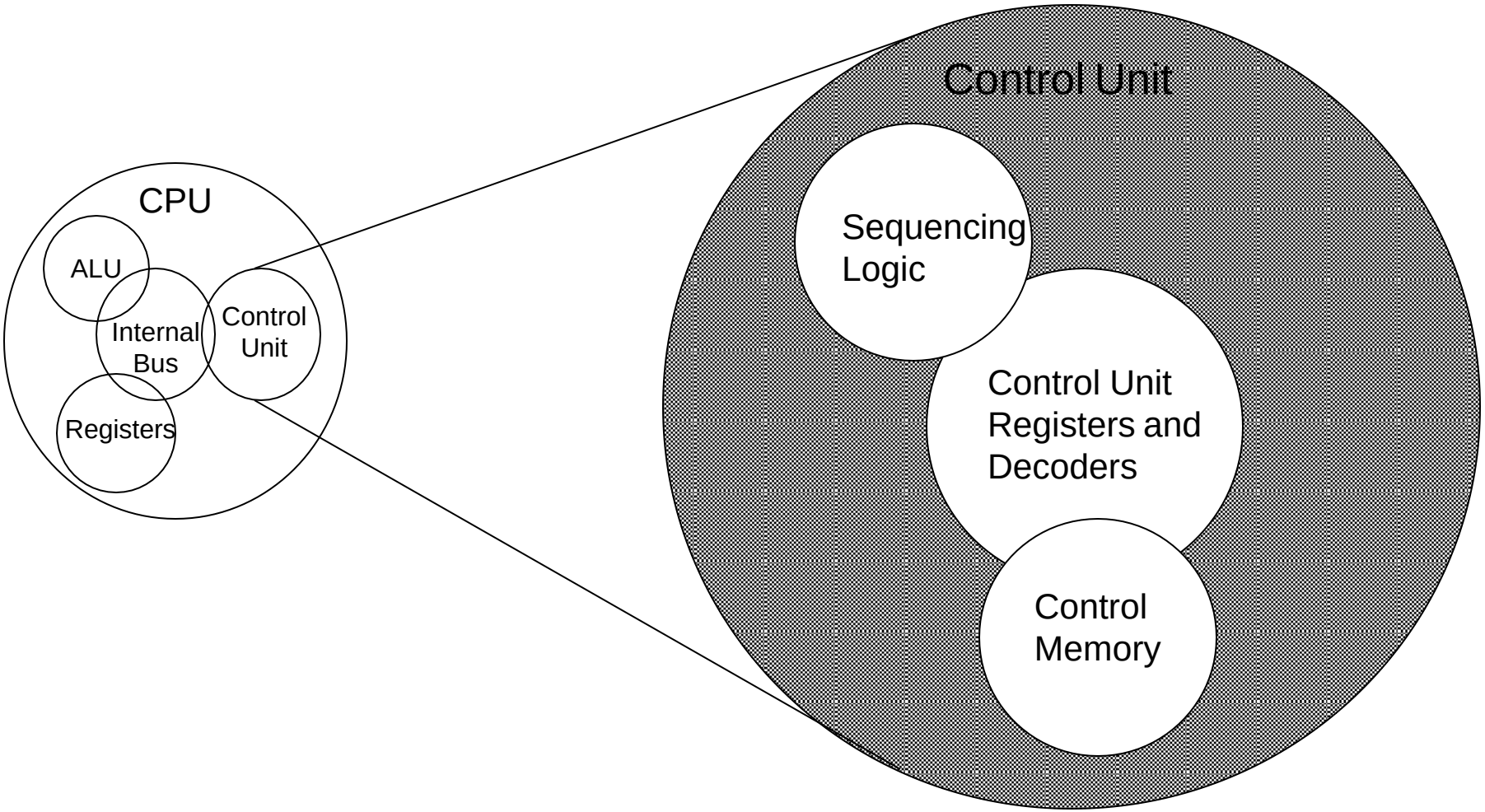
Structure - The CPU



- Major structural components of CPU are:
- **Control unit:** Controls the operation of the CPU
- **Arithmetic and logic unit (ALU):** Performs the computer's data processing functions.
- **Registers:** Provides storage internal to the CPU.
- **CPU interconnection:** Some mechanism that provides for communication among the control unit, ALU, and registers.

- Several approaches to the implementation of the control unit
- *Microprogrammed* implementation-A microprogrammed control unit operates by executing microinstructions that define the functionality of the control unit.

Structure - The Control Unit



MULTICORE COMPUTER STRUCTURE

- When these processors all reside on a single chip, the term *multicore computer* is used, and each processing unit (consisting of a control unit, ALU, registers, and perhaps cache) is called a *core*
- **Central processing unit (CPU):** That portion of a computer that fetches and executes instructions. It consists of an ALU, a control unit, and registers
- **Core:** An individual processing unit on a processor chip. A core may be equivalent in functionality to a CPU on a single- CPU system
- Processor-Theprocessor is the computer component that interprets and executes instructions. If a processor contains multiple cores, it is referred to as a **multicore processor**.

William Stallings Computer Organization and Architecture 8th Edition

Chapter 2 Computer Evolution and Performance

VON NEUMANN ARCHITECTURE

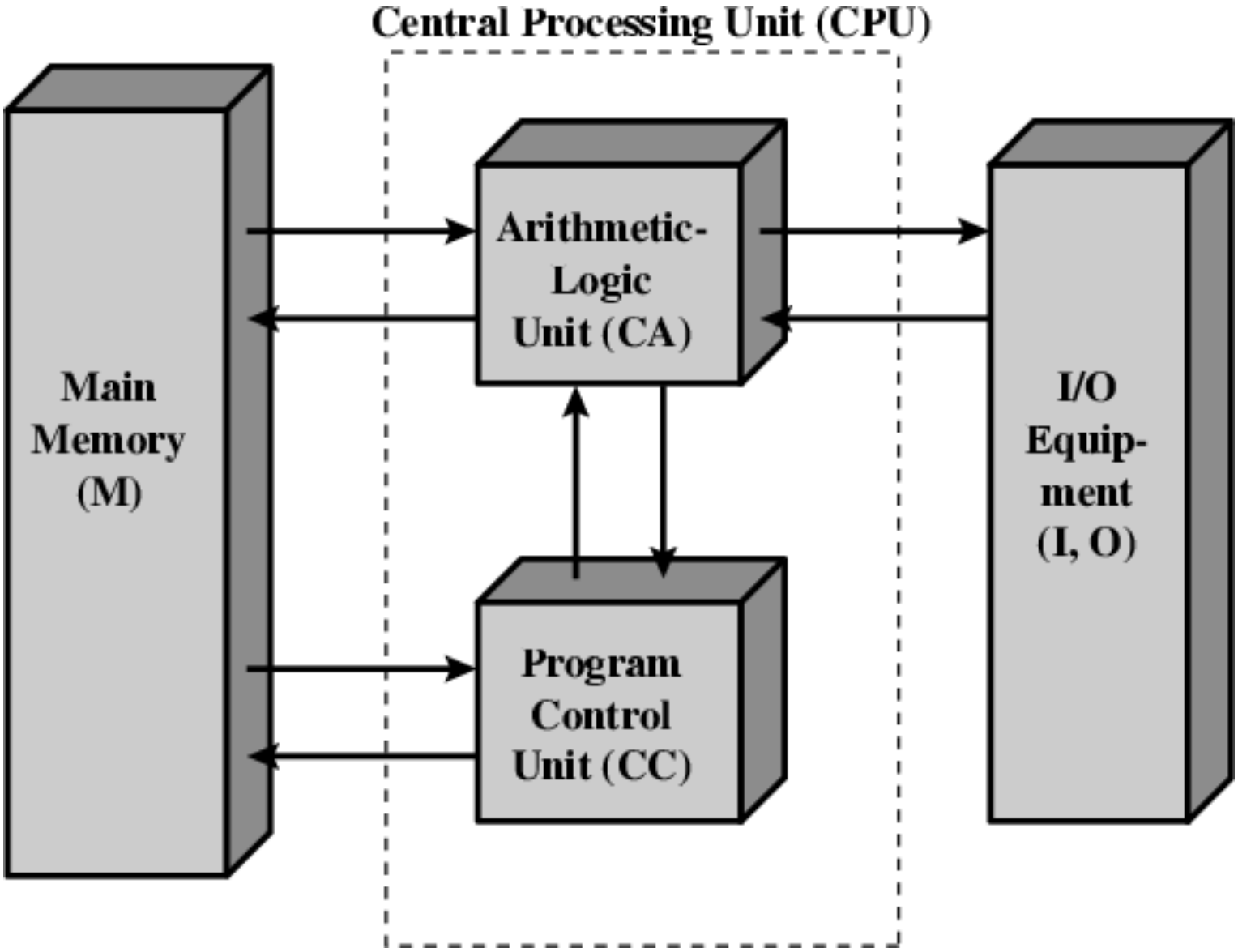
- **Fixed Program Computers –** Their function is very specific and they couldn't be reprogrammed, e.g. Calculators.
- **Computers based on Stored Program concept-**programs and data are stored in a separate storage unit called memories and are treated the same-easier to reprogram.
- Uses a single processor
- Uses one memory for both instructions and data.
- Executes programs following the fetch-decode-execute cycle

- Princeton Institute for Advanced Studies

– Design of new stored program computer, referred to as the IAS computer (Institute for Advanced Study)

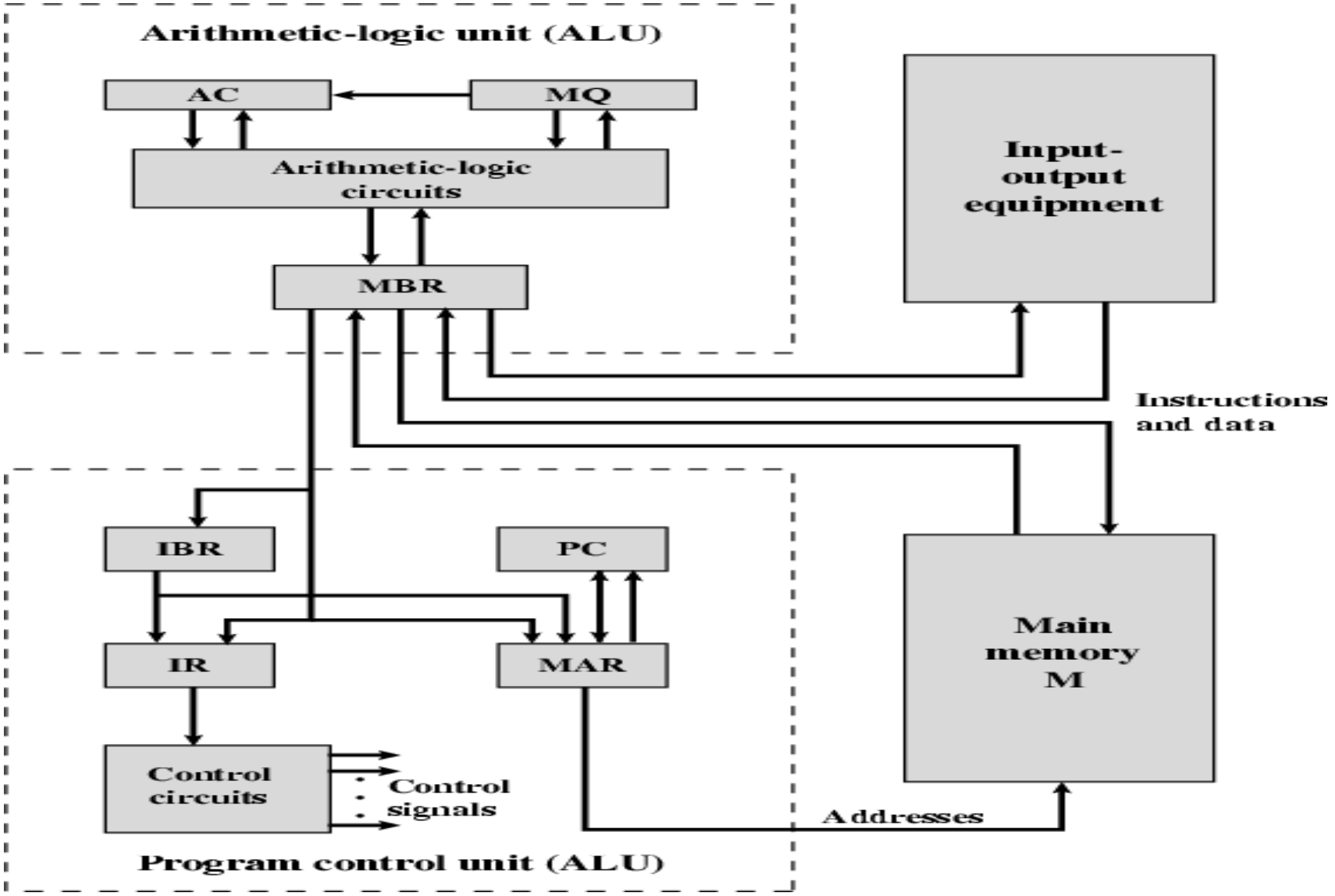
- Completed 1952
- It consists of
  - **Main memory** storing programs and data
  - **ALU** operating on binary data
  - **Control unit** interpreting instructions from memory and executing
  - **Input and output** equipment operated by control unit

Structure of Von Neumann machine



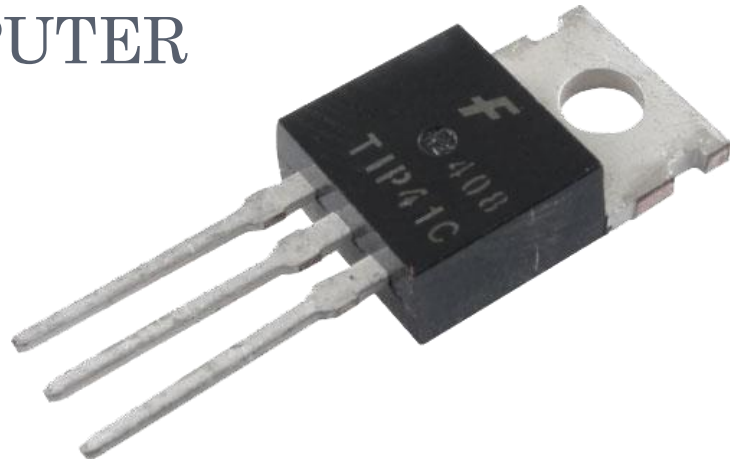
- CA-Central arithmetical part perform the elementary operations of **arithmetic** (Addition, Subtraction, Comparisons. It performs **Logical** Operations, Bit Shifting Operations, and Arithmetic operations.)
- CC- Central control-proper **sequencing of its operations/logical control of the device**
- M-Main memory-**collection of storage cells** together with associated circuits needed to transfer information in and out of the storage. The memory **stores binary information** in groups of bits called words.
- I,O-capable of **delivering data** (output) to and **receiving data** from a computer (input)

STRUCTURE OF IAS – DETAIL

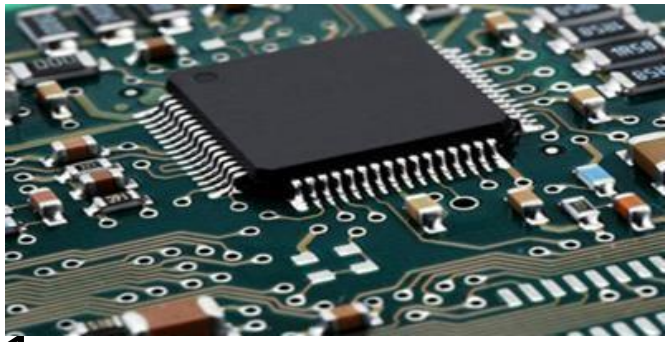


- Both the control unit and the ALU contain storage locations, called *registers*
- **Memory buffer register (MBR):** Contains a word to be stored in memory or sent to the I/O unit, or is used to receive a word from memory or from theI/O unit.
- **Memory address register (MAR):** Specifies the address in memory of the word to be written from or read into the MBR.
- **Instruction register (IR):** Contains the 8-bit opcode (identifies which basic computer operation in the instruction set is to be performed.) instruction being executed.
- **Instruction buffer register (IBR):** Employed to hold temporarily the right hand instruction from a word in memory.
- **Program counter (PC):** Contains the address of the next instruction-pair to be fetched from memory.
- **Accumulator (AC) and multiplier quotient (MQ):** Employed to hold temporarily operands and results of ALU operations

Generations of Computer



- Vacuum tube - 1946-1957
- Transistor - 1958-1964
- Small scale integration - 1965
  - Up to 100 devices on a chip
- Medium scale integration - to 1971
  - 100-3,000 devices on a chip
- Large scale integration - 1971-1977
  - 3,000 - 100,000 devices on a chip



- Very large scale integration - 1978 -1991
  - 100,000 - 100,000,000 devices on a chip
- Ultra large scale integration – 1991 -Over 100,000,000 devices on a chip

Table 2.2 Computer Generations

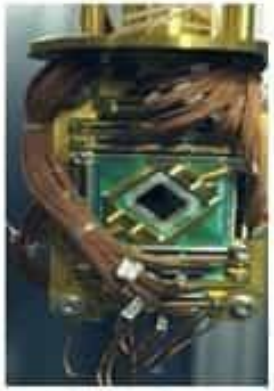
Generation	Approximate Dates	Technology	Typical Speed (operations per second)
1	1946–1957	Vacuum tube	40,000
2	1958–1964	Transistor	200,000
3	1965–1971	Small and medium scale integration	1,000,000
4	1972–1977	Large scale integration	10,000,000
5	1978–1991	Very large scale integration	100,000,000
6	1991–	Ultra large scale integration	1,000,000,000

Vacuum Tube

Transistors

Integrated Circuit

Microprocessor



Quantum Computer

1st Generation Computer

2nd Generation Computer

3rd Generation Computer

4th Generation Computer

5th Generation Computer

Subject	1st generation	2nd generation	3rd generation	4th generation	5th generation
Period	1940-1956	1956-1963	1964-1971	1971-present	present & beyond
Circuitry	Vacuum tube	Transistor	Integrated chips (IC)	Microprocessor (VLSI)	ULSI (Ultra Large Scale Integration) technology
Memory Capacity	20 KB	128KB	1MB	Magnetic core memory, LSI and VLSI. High Capacity	ULSI
Processing Speed	300 IPS instructions Per sec.	300 IPS	1MIPS (1 million inst. Per sec.)	Faster than 3rd generation	Very fast
Programming Language	Machine, Language	Assembly language & early high-level languages(FORTRAN, COBOL, ALGOL)	C,C++	Higher level languages,C,C++,Java	All the Higher level languages,,Neural networks,
Example of computers	UNIVAC, EDVAC	IBM 1401, IBM 7094, CDC 3600,D UNIVAC 1108	IBM 360 series, 1900 series	Pentium series,Multimedia,	Artificial Intelligence, Robotics

What is a Bus?

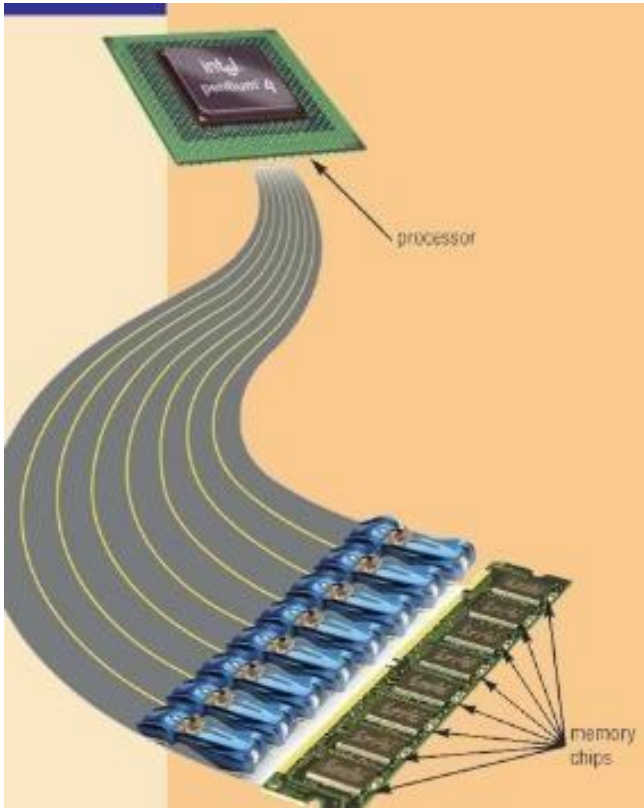
- A **communication pathway** connecting two or more devices
- **Data connection** between 2 or more devices connected to the computer
- Usually **broadcast** ,Often grouped
  - For Ex: A bus enables a computer processor to communicate with the memory or video card to communicate with the memory
  - several lines of a bus can be used to transmit binary digits simultaneously e.g. 32 bit data bus is 32 separate single bit channels
- Power lines may not be shown

- it is a **shared transmission medium-**Multiple devices connect to the bus, and a signal transmitted by any one device is available for reception by all other devices attached to the bus.
- If two devices transmit during the same time period, their signals will overlap and become garbled-Only one device at a time can successfully transmit.
- Bus consists of multiple communication pathways/ lines
- A bus that connects major computer components (processor, memory, I/O) is called a ***system bus***

BUSES

- There are a number of possible interconnection systems
- Single and multiple BUS structures are most common
- e.g. Control/Address/Data bus (PC)
- e.g. Unibus (DEC-PDP)

(Digital Equipment Corporation-Programmed Data Processor)



FUNCTIONS OF BUSES IN COMPUTERS

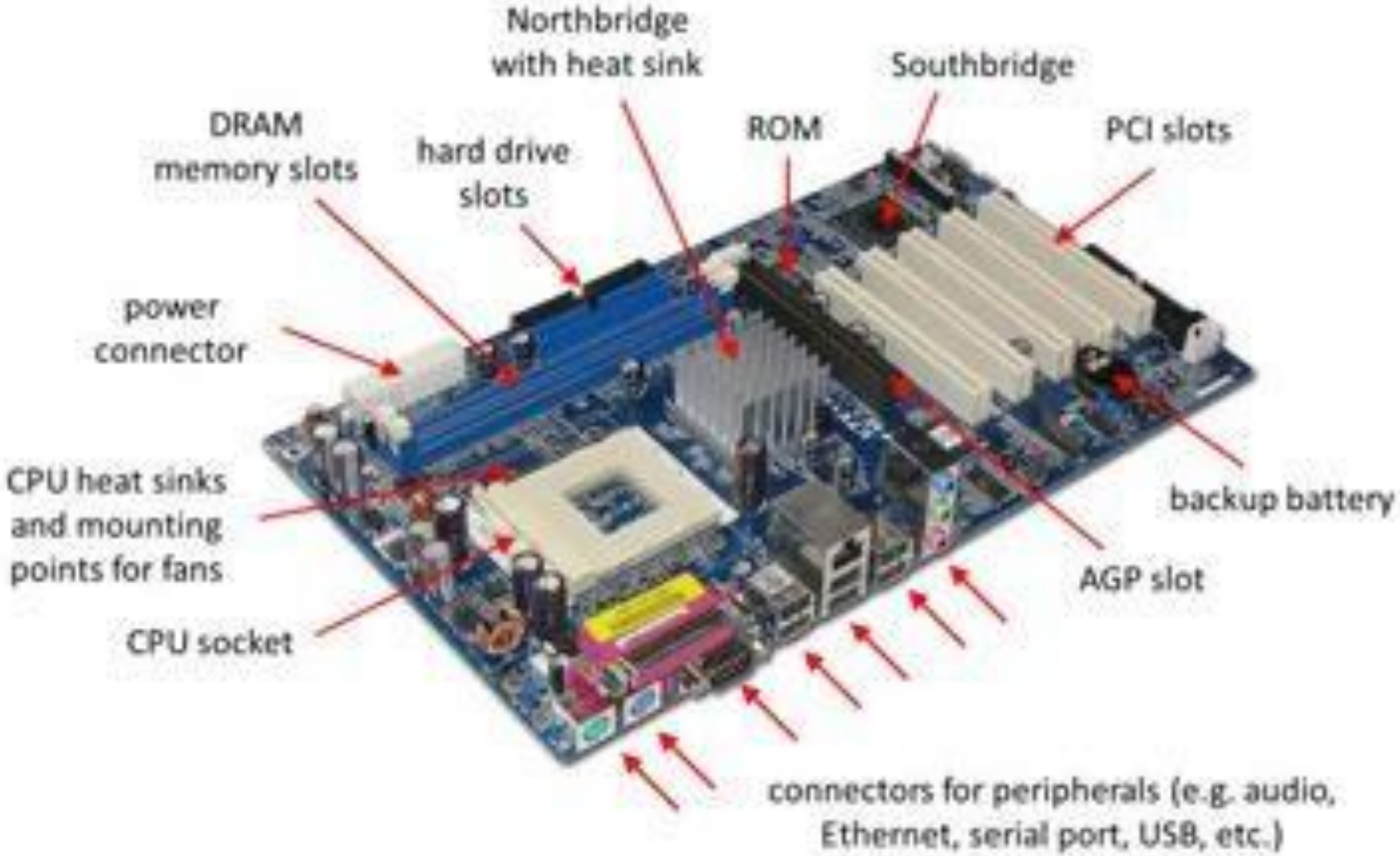
Data sharing - Serial/Parallel transmission, 8-bit, 16-bit, 32-bit or even 64-bit buses.

Addressing - A bus has address lines which allows **data to be sent to or from specific memory locations**.

Power - A bus **supplies power** to various peripherals connected to it.

Timing - System clock-synchronize the peripherals attached to it with the rest of the system.

Eg: The expansion bus facilitates easy connection of more or additional components and devices on a computer such as a TV card or sound card.

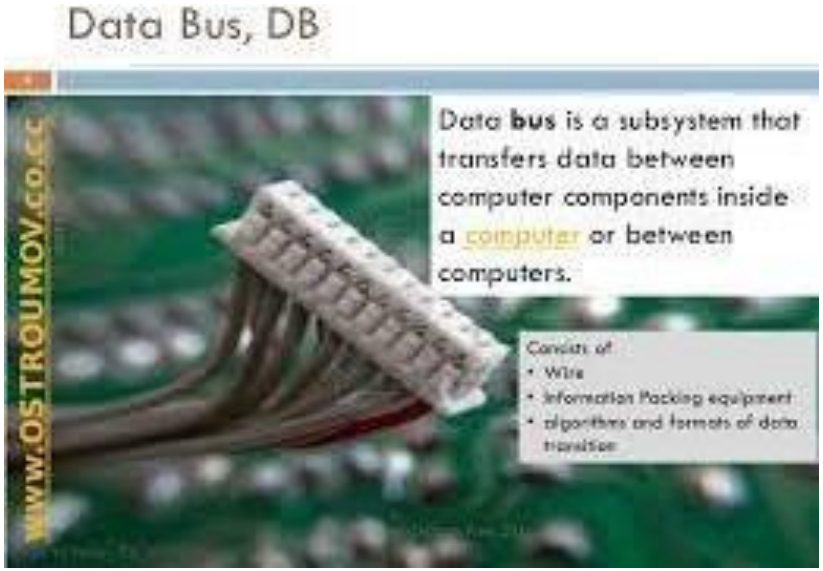

Northbridge
with heat sink
Southbridge
DRAM
memory slots
hard drive
slots
ROM
PCI slots
power
connector
CPU heat sinks
and mounting
points for fans
backup battery
AGP slot
CPU socket
connectors for peripherals (e.g. audio,
Ethernet, serial port, USB, etc.)

Bus Structure

- A system bus consists, typically, of from about 50 to hundreds of separate lines
- lines can be classified into three functional groups: **data, address, and control lines.**

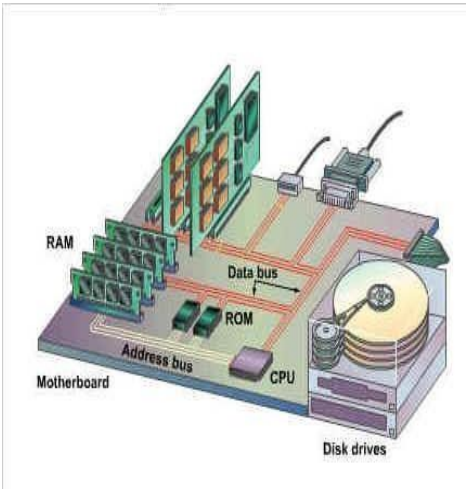
DATA BUS

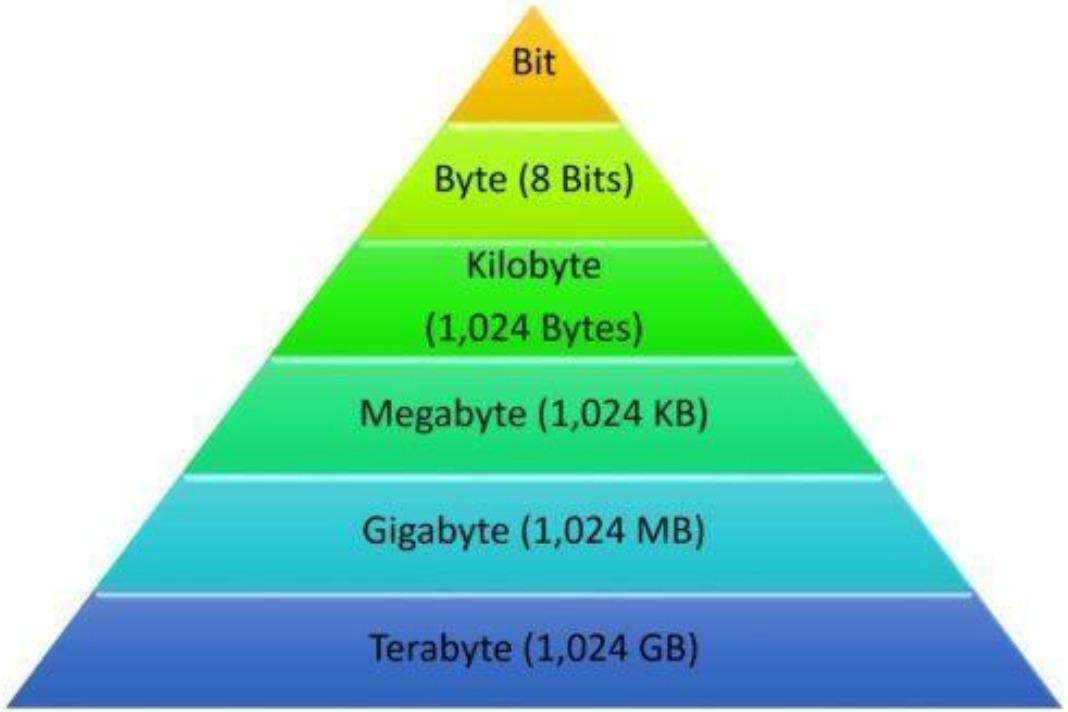
- **Data lines=Data bus**
- data bus may consist of 32, 64, 128, or even more separate lines
- number of lines being referred to as the *width* of the data bus.
- Carries **data**
  - Remember that there is no difference between "data" and "instruction" at this level
- **Width** is a key determinant of **performance-no: of lines determine amount of bits transferred**
  - 8, 16, 32, 64 bit

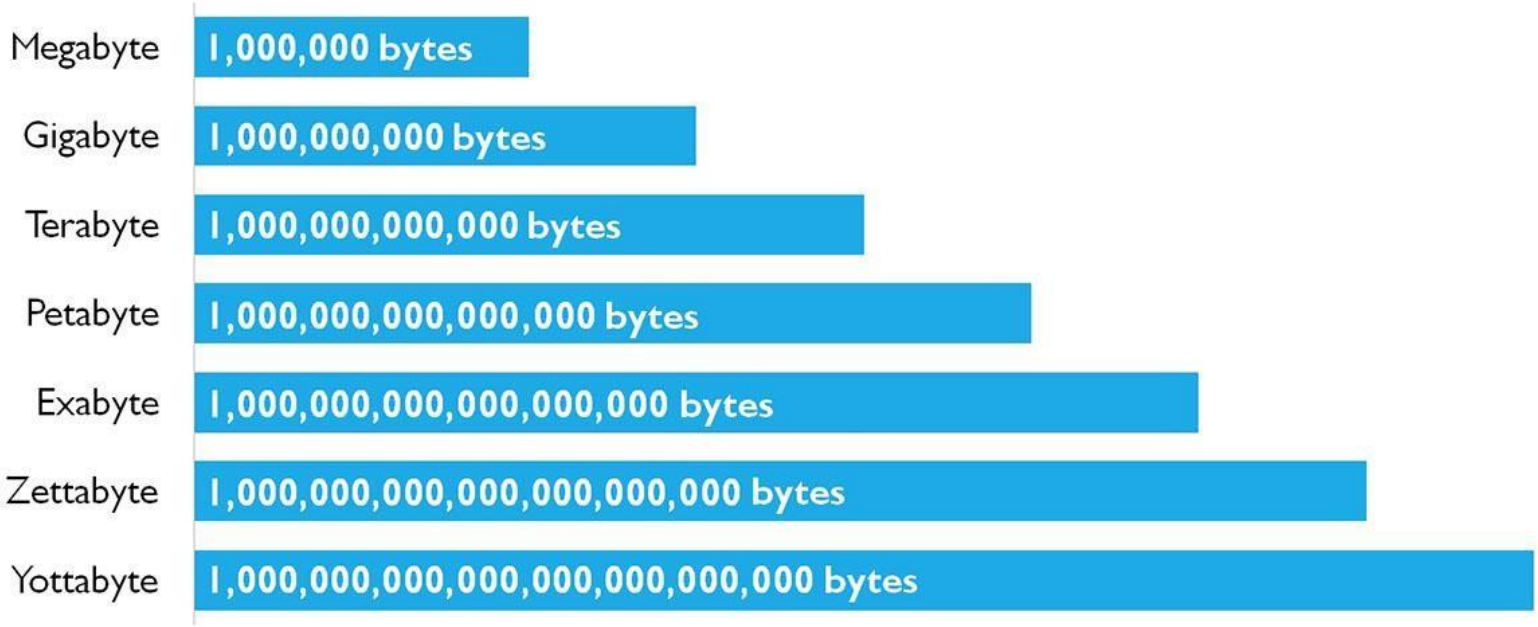


ADDRESS BUS

- Identify the source or destination of data-Eg 1000H,1200H
- e.g. CPU needs to read an instruction (data) from a given location in memory
- Bus width determines **maximum memory capacity** of system
- 2 ^nos of address lines=Memory Capacity
  - e.g. 8080 has 16 bit address bus giving 64k address space
  - 32 bit?64bit ? 2 ^
  - (16.777216 million terabyte)




Bit
Byte (8 Bits)
Kilobyte
(1,024 Bytes)
Megabyte (1,024 KB)
Gigabyte (1,024 MB)
Terabyte (1,024 GB)


Megabyte
1,000,000 bytes
Gigabyte
1,000,000,000 bytes
Terabyte
1,000,000,000,000 bytes
Petabyte
1,000,000,000,000,000 bytes
Exabyte
1,000,000,000,000,000,000 bytes
Zettabyte
1,000,000,000,000,000,000,000 bytes
Yottabyte
1,000,000,000,000,000,000,000,000 bytes

CONTROL BUS

- Controls activities of all units of a computer- control the **access to and the use of the data and address lines**

- Control signals transmit both **command** (specify operations to be performed) and **timing information** (validity of data and address information) among system modules.

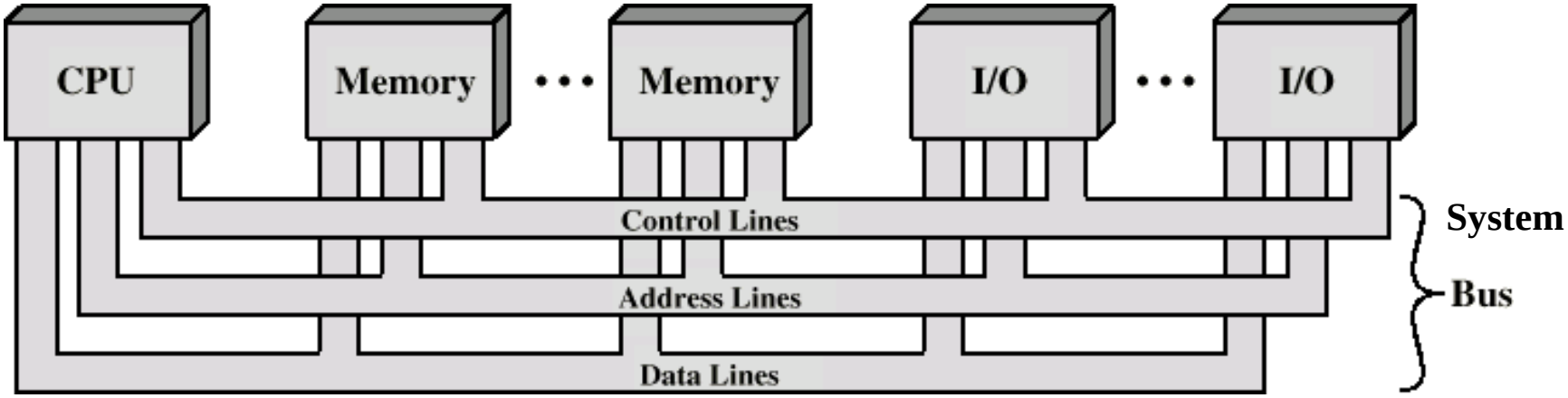
- Main Function is to carry **control signals** generated by control unit
  - Ex: One line of control bus is used to indicate whether the CPU is reading/writing to the main memory

- Control and timing information
  - Memory read/write signal
  - Interrupt request
  - Clock signals

Examples of control lines

- **Memory write:** Causes data on the bus to be written into the addressed location
- **Memory read:** Causes data from the addressed location to be placed on the bus
- **I/O write:** Causes data on the bus to be output to the addressed I/O port
- **I/O read:** Causes data from the addressed I/O port to be placed on the bus
- **Transfer ACK:** Indicates that data have been accepted from or placed on the bus
- **Bus request:** Indicates that a module needs to gain control of the bus
- **Bus grant:** Indicates that a requesting module has been granted control of the bus
- **Interrupt request:** Indicates that an interrupt is pending
- **Interrupt ACK:** Acknowledges that the pending interrupt has been recognized
- **Clock:** Is used to synchronize operations
- **Reset:** Initializes all modules

Bus Interconnection Scheme



- If one module wishes to *send data* to another,

(1) obtain the use of the bus, and

(2) transfer data via the bus.

- If one module wishes to *request data* from another module, it must

(1) obtain the use of the bus, and

(2) transfer a request to the other module over the appropriate control and address lines. It must then wait for that second module to send the data.

Single Bus Problems

- Lots of devices (greater the bus length) on one bus leads to:
  - Propagation delays
    - Long data paths mean that **co-ordination of bus use can adversely affect performance**
    - If aggregate data transfer approaches bus capacity
      - Remedy-by increasing the data rate that the bus can carry and by using wider buses
- Most systems use multiple buses to overcome these problems

Table 3.2 Elements of Bus Design

Type	**Bus Width**
Dedicated	Address
Multiplexed	Data
Method of Arbitration	**Data Transfer Type**
Centralized	Read
Distributed	Write
Timing	Read-modify-write
Synchronous	Read-after-write
Asynchronous	Block

BUS TYPES

- **Dedicated**
  - permanently assigned either to one function or to a physical subset of computer components
  - Eg: of functional dedication-Separate data & address lines
- **Multiplexed**

-Assigned too many functions based on some parameters-**Shared lines**

-Eg:- Address and data information may be transmitted over the same set of lines using an Address Valid control line.

At the beginning of the data transfer the **address is placed** on the bus and the address valid line is activated.

The address is then removed from the same bus line & is used for **data transfer**.

  - Address valid or data valid control line

- same lines for multiple purposes is known as *time multiplexing*.
- Advantage - fewer lines (space and cost are saved)
- Disadvantages
  - More complex control
  - Reduction in performance

- *Physical dedication* refers to the use of multiple buses, each of which connects only a subset of modules.
  - A typical example is the use of an I/O bus to interconnect all I/O modules
  - High throughput, because there is less bus contention (when two outputs drive the same signal at the same time).
  - A disadvantage is the increased size and cost of the system.

Bus Arbitration

- Only one module may control bus at one time-e.. CPU and DMA controller

- More than one module controlling the bus-data corruption and system instability
- **Bus arbitration** is the process of resolving conflicts that arise when multiple devices attempt to access the bus at the same time
- Ensure that only one device has access to the bus at any given time.
- Arbitration may be **centralised or distributed**

Centralised or Distributed Arbitration

- Centralised
  - Single hardware device controlling bus access-responsible for allocating time on the bus
    - Bus Controller
    - Arbiter
  - May be part of CPU or separate
- Distributed
  - Each module may claim the bus
  - No central controller
  - Control logic on all modules

- purpose is to designate one device, either the processor or an I/O module, as master-initiate a data transfer (e.g., read or write) with some other device, which acts as slave for this particular exchange.

INTRODUCTION TO PCI BUS

- Bus
  a) highways that take information and power from one place to another.
  b) channel or path between the components in a computer
  c) lets you connect components to the computer's processor
  d) hard disks, memory, sound systems, video systems , graphics card etc…
- PCI Bus
- Nowadays USB-
- Used as the standard in most computers' high-speed buses
- Firewire ?
- ISA Bus- Industry Standard Architecture
- IT PROVIDES DIRECT ACCESS TO SYSTEM MEMORY FOR CONNECTED DEVICES
- Intel created the PnP standard and incorporated it into the design for PCI.

PCI-PERIPHERAL COMPONENT INTERCONNECT (PCI)

- **high-bandwidth,processor-independent, low cost** bus that can function as a peripheral bus
- PCI delivers better system performance for **high-speed I/O** subsystems (*e.g., graphic display adapters, network interface controllers, disk controllers)*
- Current standard allows the use of up to **64 data lines at 66 MHz, for a raw transfer rate of 528 MByte/s, or 4.224 Gbps**
- Requires very few chips to implement and supports other buses attached to the PCI bus.
- PCI is designed to support a variety of microprocessor-based configurations, including both single- and multiple-processor systems
- It makes use of **synchronous timing and a centralized arbitration scheme.**

FEATURES

- Plug & Play capability
- Hot-plug ability
- Hot swappable
- High speed
- Backward compatibility-Older versions of independent bus can be connected to PCI slot
- Independent bus-Device operates independently without CPU intervention
- High operational frequency-upto 133 MHz
- Supports 3 independent address spaces-memory, (memory mapped i/o functions) i/o (used within the processor) & configuration (for PCI plug & play capability)

PCI Bus-Peripheral Component Interconnect

- Intel released to public domain-32 bit and 64 bit versions
- PCI bus connects the CPU and expansion boards
  - Examples of PCI devices
    - Modem
    - Network Card
    - Sound Card,Video Card,etc

- PCI may be configured as a 32- or 64-bit bus

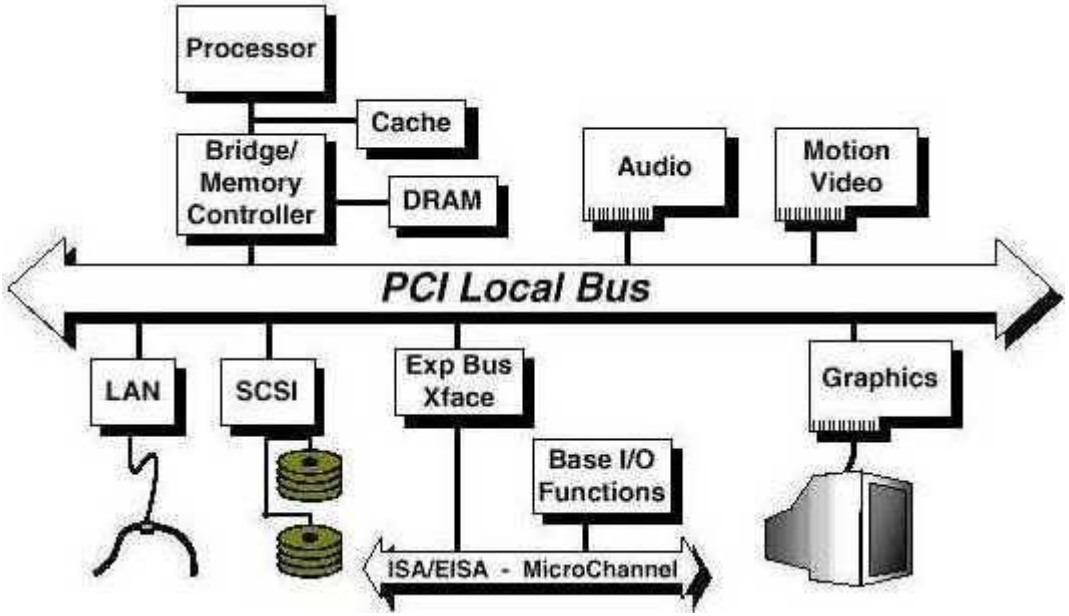
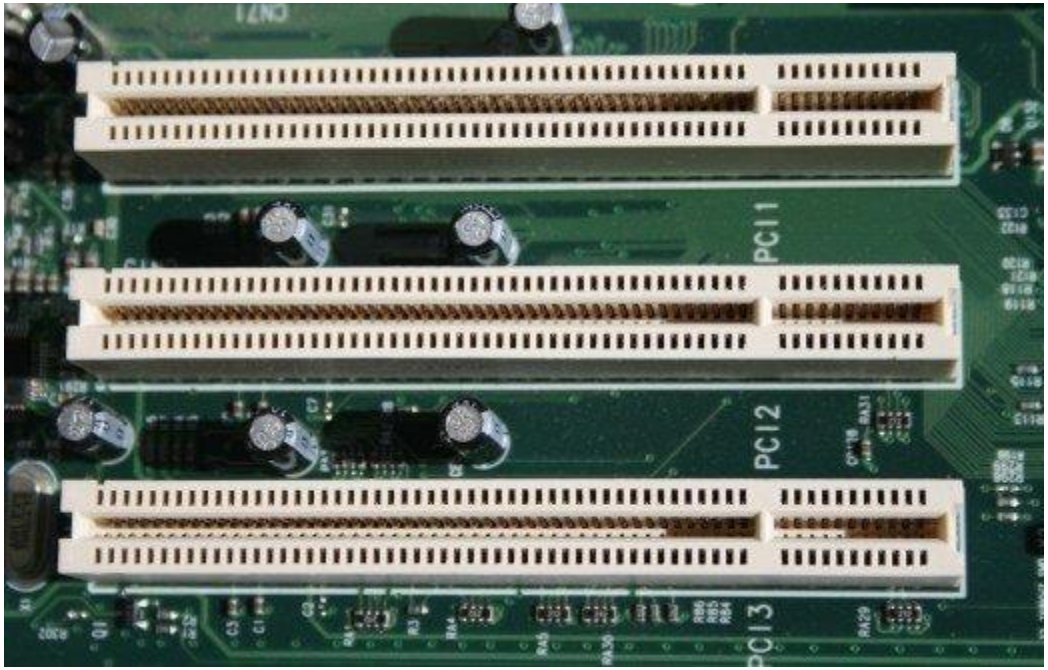


Table 3.3 Mandatory PCI Signal Lines & Optional Signal lines- Refer

PCI Bus Lines (required)

- **Systems lines**
  - Including clock and reset
- **Address & Data**
  - 32 time mux lines for address/data
  - Interrupt & validate lines (carry the addresses and data)
- **Interface Control** (Control the timing of transactions and provide coordination among initiators and targets.)
- **Arbitration**
  - Not shared
  - PCI master has its own pair of arbitration lines that connect it directly to the PCI bus arbiter.
  - **Error lines**

PCI Bus Lines (Optional)



PCI Bus Lines (Optional)

- **Interrupt lines**
  - Not shared
  - generate requests for service
- **Cache support- support a memory on PCI** that can be cached in the processor or another device
- **64-bit Bus Extension**
- Additional 32 lines time multiplexed for addresses and data and that are combined with the mandatory address/data lines to form a 64-bit address/data bus
- used to interpret and validate the signal lines that carry the addresses and data
  - 2 lines to enable devices to agree to use 64-bit transfer

- PCIe (PCI Express®) is the more recently introduced standard for connecting devices to computers.
- It's software-compatible with PCI but has higher potential bandwidth and greater flexibility than PCI

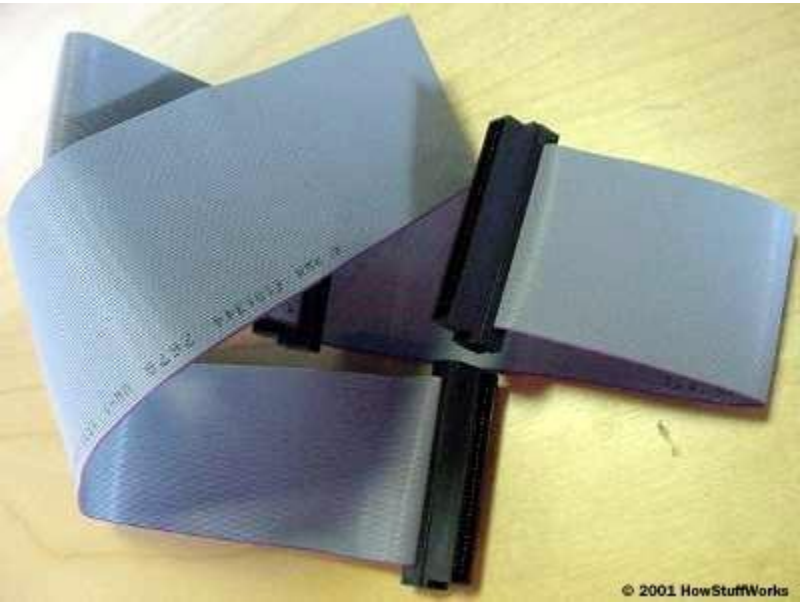
- **Let's say that you have just added a new PCI-based sound card to your Windows XP computer. Here's an example of how it would work**.
- You open up your computer's case and plug the sound card into an empty PCI slot on the motherboard
- You close the computer's case and power up the computer.
- The system BIOS initiates the PnP BIOS.
- The PnP BIOS scans the PCI bus for hardware. It does this by sending out a signal to any device connected to the bus, asking the device who it is.
- The sound card responds by identifying itself. The device ID is sent back across the bus to the BIOS.
- The PnP BIOS checks the ESCD to see if the configuration data for the sound card is already present. Since the sound card was just installed, there is no existing ESCD record for it.
- The PnP BIOS assigns IRQ, DMA, memory address and I/O settings to the sound card and saves the data in the ESCD.
- Windows XP boots up. It checks the ESCD and the PCI bus. The operating system detects that the sound card is a new device and displays a small window telling you that Windows has found new hardware and is determining what it is.
- In many cases, Windows XP will identify the device, find and load the necessary drivers, and you'll be ready to go. If not, the "Found New Hardware Wizard" will open up. This will direct you to install drivers off of the disc that came with the sound card.
- Once the driver is installed, the device should be ready for use. Some devices may require that you restart the computer before you can use them. In our example, the sound card is immediately ready for use.
- You want to capture some audio from an external tape deck that you have plugged into the sound card. You set up the recording software that came with the sound card and begin to record.
- The audio comes into the sound card via an external audio connector. The sound card converts the analog signal to a digital signal.
- The digital audio data from the sound card is carried across the PCI bus to the bus controller. The controller determines which device on the PCI device has priority to send data to the CPU. It also checks to see if data is going directly to the CPU or to system memory.
- Since the sound card is in record mode, the bus controller assigns a high priority to the data coming from it and sends the sound card's data over the bus bridge to the system bus.
- The system bus saves the data in system memory. Once the recording is complete, you can decide whether the data from the sound card is saved to a hard drive or retained in memory for additional processing.

INTRODUCTION TO SCSI BUS

- Pronounced "scuzzy"
- **Fast bus** that can connect lots of devices to a **COMPUTER** at the same time, including hard drives, scanners, CD-ROM/RW drives, printers and tape drives unlike USB connected for small devices.
- Helps to put **multiple items on one bus.**
- Also works with most computer systems.
- Prob---
  - Limited BIOS support as it has to be configured for each computer
  - No common SCSI software interface

  –All different types of SCSI have different speeds,bus widths,connectors Which can be confusing !

- Standard interface for connecting peripheral devices to PC(16 peripheral devices via a single bus and a host adapter)
- Deliver faster data transfer, increase performance etc
- It is less commonly used in desktop PCs
- Either embedded on motherboard or a host adapter is inserted into the expansion slot on motherboard



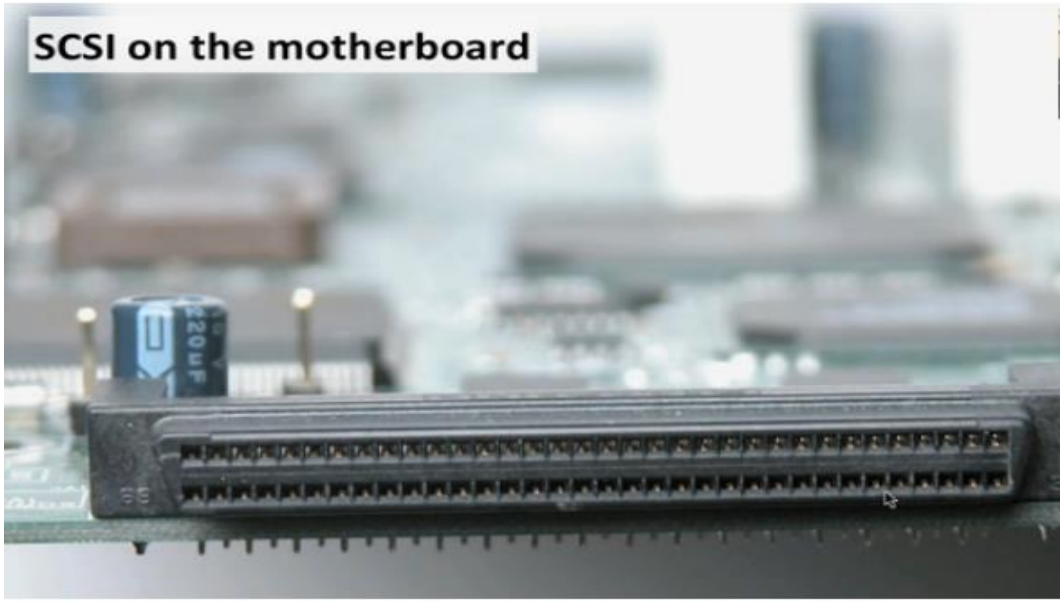
Internal SCSI devices connect to a ribbon cable.

External SCSI devices connect using thick, round cables

SCSI-Small Computer System Interface

- Set of standard electronic interfaces that allow personal computers **PC's to communicate with peripheral hardware** such as disk drives,tapes,CDs,Printers,scanners,etc
- Faster.
- SCSI standards are generally backward compatible
  - A parallel interface standard used by Apple Macintosh computers, PCs and Unix systems for attaching peripheral devices to a computer.

- SCSI interfaces used internally in computers to connect different types of hardware devices directly to a motherboard or storage controller card.
- When used internally, devices are attached through a ribbon cable.
- External connections are also common and typically connect via an external port on a storage controller card using a cable.
- Within the controller is a memory chip that holds the SCSI BIOS, which is a piece of integrated software that's used to control the connected devices.


SCSI on the motherboard

- There are several SCSI technologies that support different cable lengths, speeds, and a number of devices that can be attached to one cable

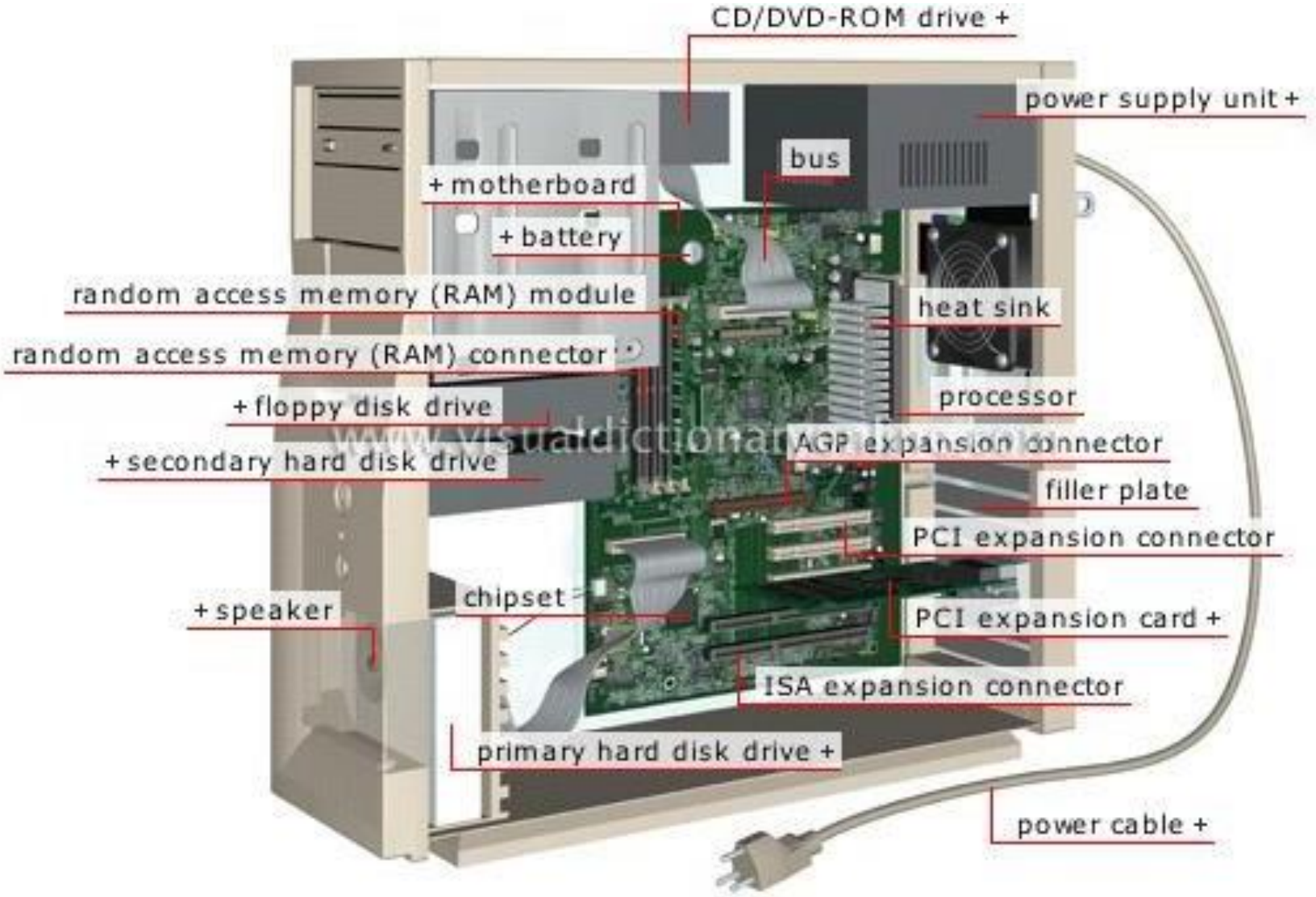
Here are some of the other SCSI interfaces that have existed:

- **Fast SCSI**: 10 MBps; connects eight devices
- **Fast Wide SCSI**: 20 MBps; connects 16 devices
- **Ultra Wide SCSI**: 40 MBps; connects 16 devices
- **Ultra2 Wide SCSI**: 80 MBps; connects 16 devices
- **Ultra3 SCSI**: 160 MBps; connects 16 devices
- **Ultra-320 SCSI**: 320 MBps; connects 16 devices
- **Ultra-640 SCSI**: 640 MBps; connects 16 devices

- A SCSI controller coordinates between all of the other devices on the SCSI bus and the computer. Also called a **host adapter**, the controller can be a card that you plug into an available slot or it can be built into the motherboard.
- Each SCSI device must have a unique **identifier** (ID) in order for it to work properly
- Internal devices connect to a SCSI controller with a ribbon cable.
- If the SCSI bus were left open, electrical signals sent down the bus could reflect back and interfere with communication between devices and the SCSI controller.
- The solution is to **terminate** the bus, closing each end with a **resistor circuit**. If the bus supports both internal and external devices, then the last device on each series must be terminated.

SCSI ADVANTAGES

- Not just for hard drives
  - Scanners, tape drives, CD-ROM drives
- Many devices on a single bus
  - 8 on narrow bus, 16 on wide bus
- Very intelligent interface functionality
  - Much of the difficult configuration work is done between the SCSI devices
- Industry longevity
  - Tends to be specialized these days
- SCSI is particular about termination
  - The recent SCSI standards automatically configure most drive settings


CD/DVD-ROM drive +
power supply unit +
bus
+ motherboard
+ battery
random access memory (RAM) module
heat sink
random access memory (RAM) connector
processor
+ floppy disk drive
AGP expansion connector
+ secondary hard disk drive
filler plate
PCI expansion connector
chipset
+ speaker
PCI expansion card +
ISA expansion connector
primary hard disk drive +
power cable +

SCSI DISADVANTAGES

- Refer
- Why it is not common nowadays?