**K. J. Somaiya College of Engineering, Mumbai-77**
**(Autonomous College Affiliated to University of Mumbai)**
Semester: **August – November 2020**
**In-Semester Examination**

**Class: SY B. Tech**
**Branch: Computer Engineering** **Semester : III**
**Full name of the course: Computer Organization & Architecture** **Course Code:2UCC303**
**Duration: 1hr.15 min (attempting questions) +15 min (uploading)** **Max. Marks: 30**

| Q. No | Questions | Marks |
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| **1** | Multiple Choice Questions(MCQ),<br>All Questions are compulsory | Total 10 MKS |
| **1.1** | The MDR and MAR registers are used to perform a write/read operation into a specified memory location. Arrange the steps required for the above in the correct order for write operation.<br><br>1. The address of the location into which the word is to be stored is loaded by the CPU into a MAR.<br>2. A write signal is issued by the CPU.<br>3. The word to be stored into the memory location is loaded by the CPU into MDR.<br><br>Choose the correct answer sequence.<br><br>A) 3, 1, 2<br>B) 1, 2, 3<br>C) 2, 1, 3<br>D) 2, 3, 1 | 1M |
| **1.2** | Separation of user logical memory and physical memory is _____<br>A) Memory control<br>B) Memory management<br>C) Memory sharing<br>D) Virtual memory | 1M |
| **1.3** | Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address. What is the maximum directly addressable memory capacity (in bytes)?<br>A) 4 MB<br>B) 16 MB<br>C) 32 MB<br>D) 64 MB | 1M |

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| **1.4** | While browsing at Tom Tim's computer store, you overhear a customer asking Tom Tim what is the fastest computer in the store that he can buy. Tom Tim replies, "You're looking at our Macintoshes. The fastest Mac we have runs at a clock speed of 1.2 GHz.If you really want the fastest machine, you should buy our 2.4-GHz Intel Pentium IV instead." What option would you say to help this customer?<br>A) Intel machine having a faster clock speed (2.4 GHz vs. 1.2 GHz), means the system will perform faster as different systems are comparable on clock speed.<br>B) Factors such as the system components (memory, buses, architecture) and the instruction sets should not be taken into account.<br>C) It is inaccurate measure is to run both systems on a benchmark such as running office applications, performing floating-point operations, graphics operations.<br>D) Systems cannot be compared to each other but few of them can be parameters like support on transferability speed, millions of transistors on a chip, software incompatilbilty, etc. | 1M |
| **1.5** | ____ is the raw material used as input and _____is the processed data obtained as output of data processing.<br>A) Data, Instructions<br>B) Instructions, Program<br>C) Data, Program<br>D) Program, Code | 1M |
| **1.6** | Direct Memory Access (DMA) is an I/O handling method with the following characteristics:<br>1. Data is transferred between the I/O device and memory with CPU intervention<br>2. The I/O module controls the data transfer leaving the CPU free to do other useful work<br>3. The I/O module doesn't notify the CPU with an interrupt when the transfer is complete<br>4. The transfer is still initiated by a program executing in the CPU<br>5. DMA is well suited for high-speed data transfer (e.g. disk transfer, video I/O device, etc.)<br>Which of the following options are correct?<br>A) 1 ,2 , 5<br>B) 4, 3 , 1<br>C) 2, 4 , 5<br>D) 3, 2 , 1 | 1M |

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| **1.7** | The major function or requirement for an I/O module is :<br>A) Control Unit Interrupt timing<br>B) Processor communication<br>C) Device management synchronization<br>D) Data buffering & Error correction | 1M |
| **1.8** | Flash memory –a form of semiconductor memory is intermediate between EPROM and EEPROM characterizes the following<br>a) Provides block electrical erasure but not byte level<br>b) High-density, only one transistor per bit<br>c)Fast read speeds, but not as good as SRAM<br>d) Flash memory is durable<br>e) Flash drivers have to manage bad blocks in a fashion similar to disk drivers<br>Which option suits best to Flash memory as described above.<br>OPTIONS<br>A) a, b , e<br>B) b, d, c<br>C) e ,a ,c<br>D) d, e ,c | 1M |
| **1.9** | The Interrupt service routine must have instructions to perform the following tasks:<br>1 .Restore contents of processor registers.<br>2. Turn the interrupt facility on.<br>3. Check which flag is set.<br>4. Save contents of processor registers.<br>5. Service the device whose flag is set.<br>6. Return to the running program.<br>Choose the correct order in the options given below<br>A) 4,3,5,1,2,6<br>B) 1,2,3,4,5,6<br>C) 3,2,4,2,6,1<br>D) 2,5,6,3,1,4 | 1M |

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| **1.10** | Consider 3-disks , 2 GB-per-disk RAID arrangement. What are the number of disks and the available data storage capacity combination for each of the RAID levels 0, 1, 3, 4, 5, and 6?(RL- Raid Level) –Eg RL0 is Raid level 0 and so on…<br>OPTIONS<br>A) RL 0-3 disks ,2 GB, RL 1- 3 disks,4 GB,RL 2-6 disks,12 GB,RL 3- 5 disks,10 GB,RL 4- 5 disks,10 GB, RL 5-5 disks, 10 GB,RL 6-5 disks, 10GB.<br>B) RL 0-3 disks ,6 GB, RL 1-5 disks, 10 GB,RL 2-4 disks,10GB,RL 3-5 disks,8GB,RL 4- 5 disks,8GB, RL 5-5 disks, 8 GB,RL 6-6 disks, 10GB.<br>C) RL 0-3 disks ,6 GB, RL 1-6 disks, 12 GB,RL 2-5 disks,10 GB,RL 3-4 disks,8 GB,RL 4- 4 disks,8 GB, RL 5-4 disks, 8 GB,RL 6-5 disks, 10 GB.<br>D) RL 0-3 disks ,3 GB, RL 1-6 disks, 12 GB,RL 2-5 disks,10GB,RL 3-4 disks,8GB,RL 4- 4 disks,8GB, RL 5-4 disks, 8 GB,RL 6-4 disks, 8 GB. | 1M |
| Q2 | What are the advantages of bit-pair recoding algorithm over Booth's algorithm? Implement multiplication of the following pair of signed 2's complement numbers using bit-pair recoding.<br>M=110101<br>Q=101100<br>**OR**<br>Draw the flowchart for non-restoring division algorithm for unsigned numbers and solve<br>M=18<br>Q=25 | 10 marks |
| Q3 | 3.1 What is the need for cache mapping? Explain the different mapping techniques of cache memory?<br>3.2 Explain how a memory address is mapped into a cache memory address using 2 way set associative mapped cache. The main memory is 64K words. The cache memory has 2048 words with block size of 128 words. | 5+5 marks |