K. J. Somaiya College of Engineering, Mumbai-77

Experiment / Assignment / Tutorial No. 4
Grade: AA / AB / BB / BC / CC / CD /DD
Signature of the Staff In-charge with date

Batch: D2	**Roll No.: 16010122323**	**Experiment / assignment / tutorial No.: 4**

Title: 4 bit Magnitude Comparator

Objective: Design a 2-bit comparator using logic gates and verify 4-bit magnitude comparator using IC 7485

Expected Outcome of Experiment:

CO2: Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

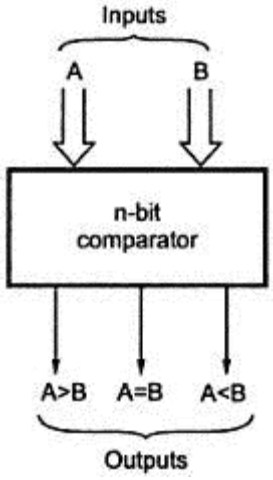
Books/ Journals/ Websites referred:

- VLab Link: http://vlabs.iitb.ac.in/vlabs-dev/labs/dldesignlab/experimentlist.html
- R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill
- M .Morris Mano, "Digital Logic & computer Design", PHI
- http://elnsite.teilam.gr/ebooks/digital_design/lab/dataSheets_page/7485.pdf

Pre Lab/ Prior Concepts:

The comparison of two numbers is an operator that determines one number is greater than, less

than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B, A=B (or) A<B.



Two Bit Magnitude Comparator Implementation Details:

Truth Table

A1	A0	B1	B0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

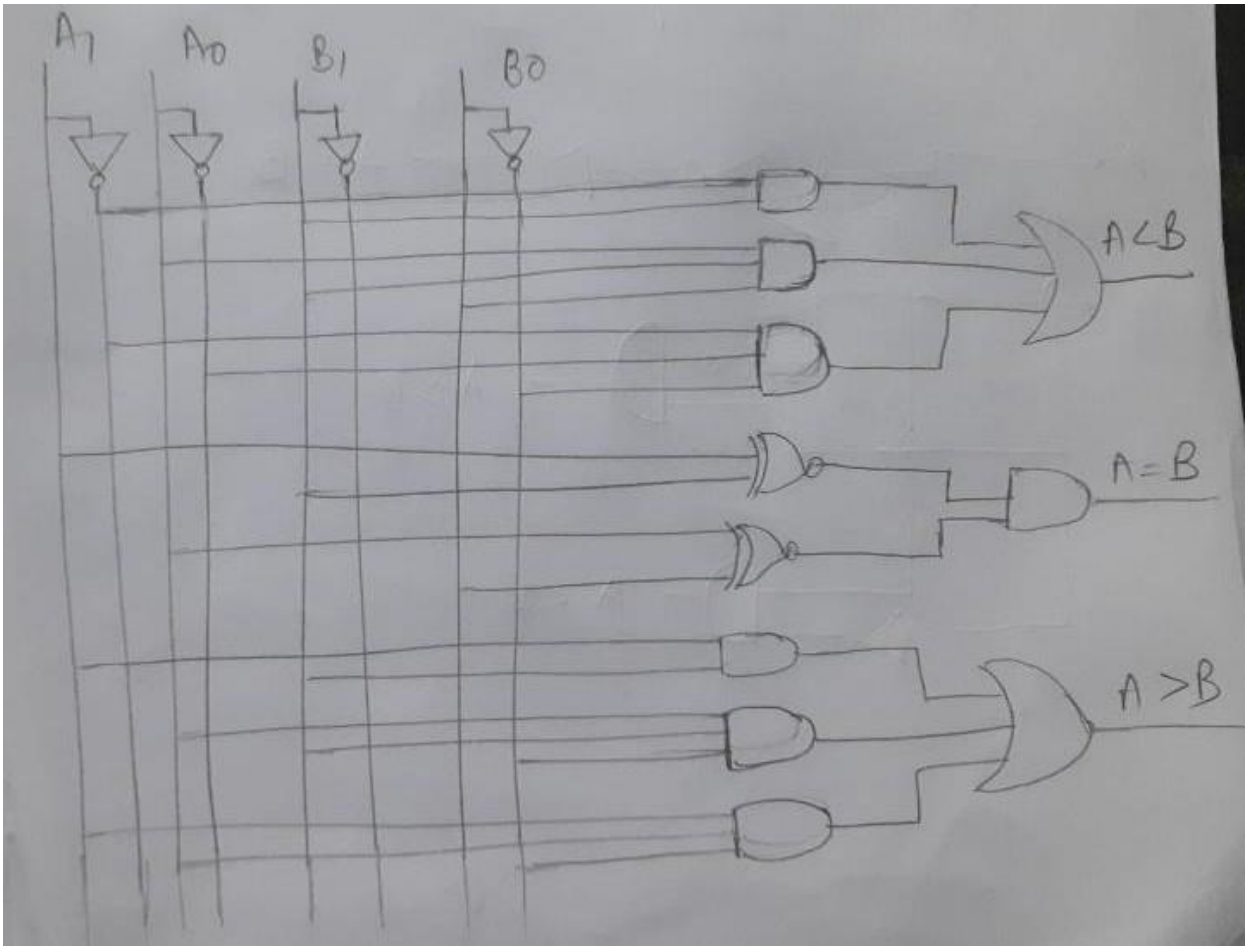
From the Truth Table:

(A<B)= A1'B1 + A0'B1B0 + A1'A0'B0

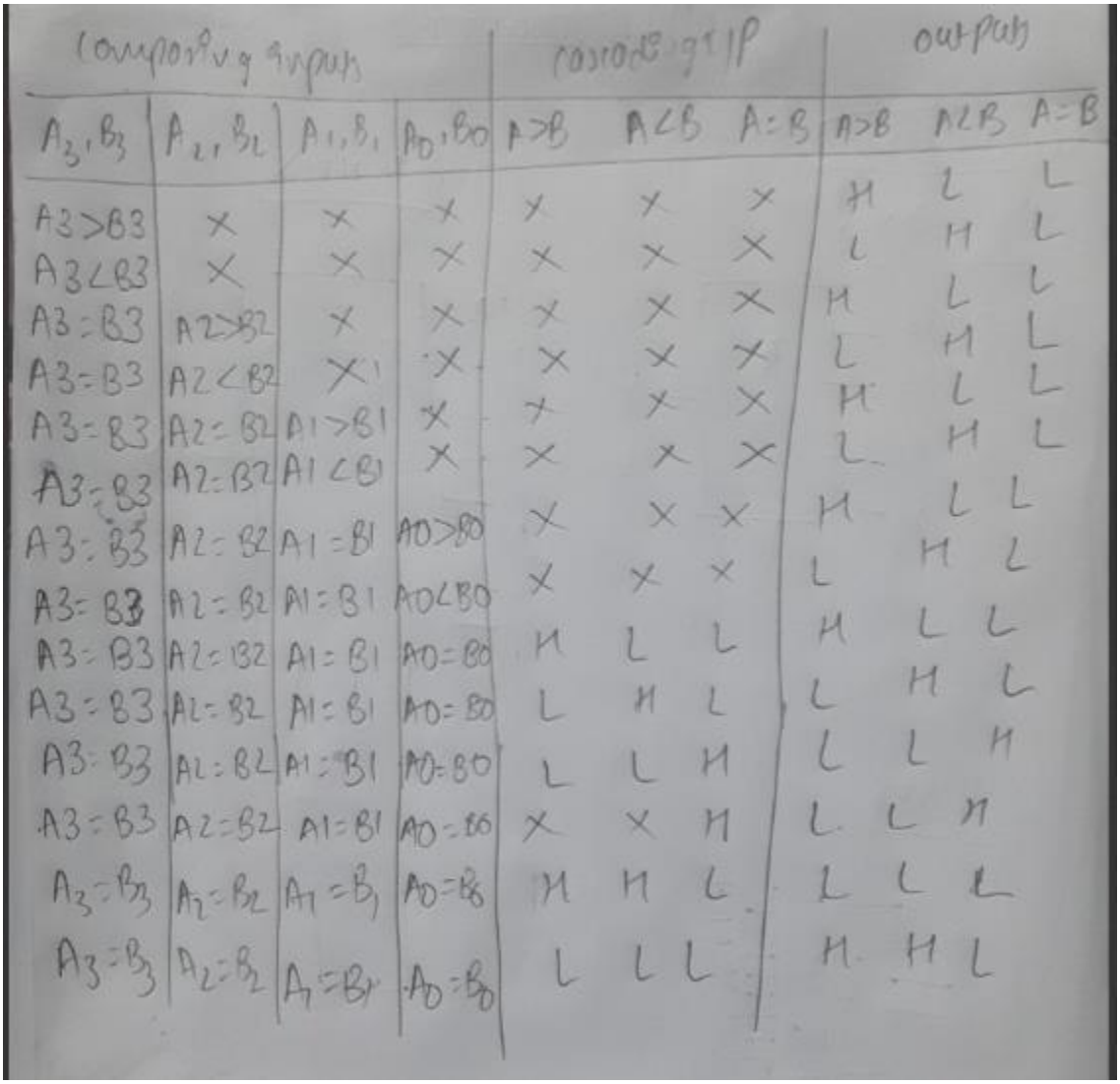
(A=B)= A1'A0'B1'B0' + A1'A0B1'B0 + A1A0B1B0 + A1A0'B1B0'

(A>B)= A1B1' + A0B1'B0' + A1A0B0'

Logic Diagram of 2 bit Comparator



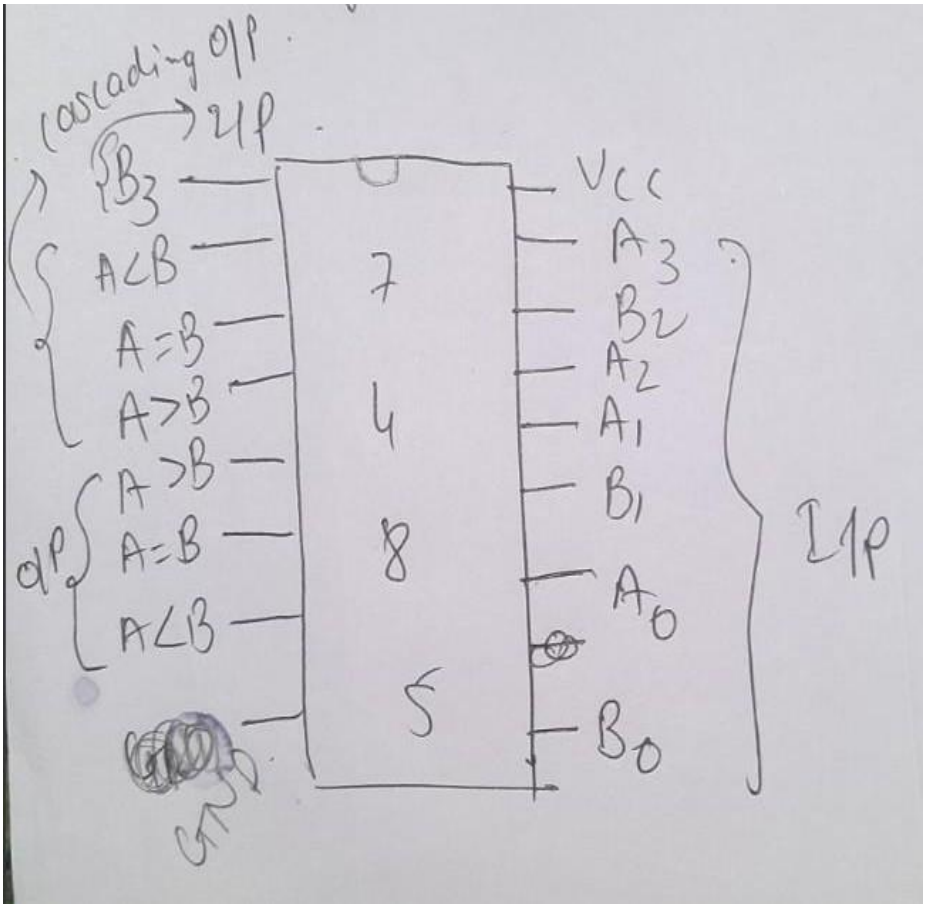
Comparing Table:



Comparing inputs				cascading i/p			outputs		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

Four Bit Magnitude Comparator Implementation Details

Pin Diagram of IC 7485



Conclusion: In this experiment, we learned to design a 2-bit comparator using logic gates and verify 4-bit magnitude comparator using IC 7485

Post-Lab Descriptive Questions

1. Design a 1-bit magnitude comparator using logic gates.