Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**09/ 10 /2023**	**Batch No:**	**D-2**
Faculty Name:	**Ruchira Jadhav**	**Roll No:**	**16010122323**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 7
Title: Asynchronous Counter

Aim and Objective of the Experiment:

To design and implement 3 bit Asynchronous up counter using JK Flip Flop

COs to be achieved:

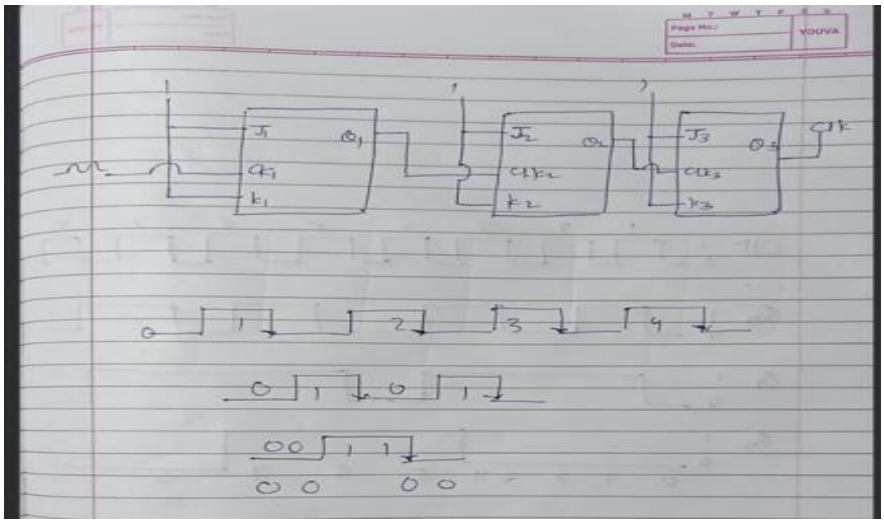
CO3: Design synchronous and asynchronous sequential circuits.

Tools used:

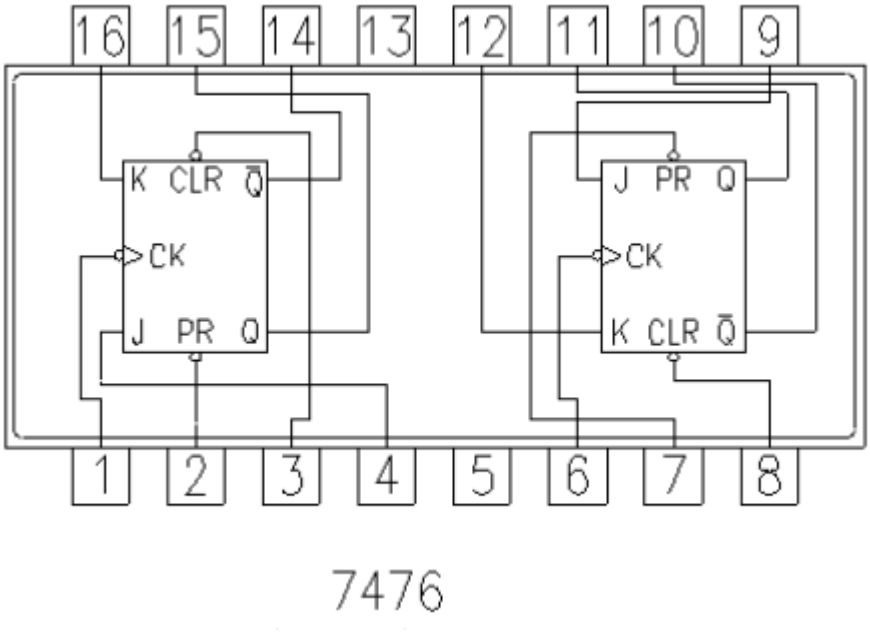
Trainer kits

Theory:

Circuit diagram of 3 bit Asynchronous Up counter using JK FF (IC 7476)



Pin diagram of JK FF (IC 7476)



7476

Implementation Details

Procedure

1) Locate IC 7476 JK FF on Digital trainer kit
2) Apply various inputs to appropriate pins as per the circuit diagram of the 3 bit Asynchronous up counter with reference to the pin configuration of the IC.
3) Make sure of Reset and Clear Pins connections with reference to data sheet information.
4) Connect a pulsar switch to the clock input.
5) Verify the working and prepare a truth table.

Post Lab Subjective/Objective type Questions:

1. How JK FF need to be configured to use for counter operation?

Ans)**Common types of counters include:**

Up Counters: These count upwards from a starting point to an ending point. JK Flip-Flops in this configuration should be connected to toggle when the count reaches a specific value.

Down Counters: These count downwards from a starting point to an ending point. JK Flip-Flops in this configuration should be connected to toggle when the count reaches a specific value.

Binary Counters: These use a series of JK Flip-Flops to count in binary. Each Flip-Flop represents a different bit in the binary number.

Ring Counters: In a ring counter, the output of one Flip-Flop is connected to the input of the next one, creating a "ring" of Flip-Flops that cycle through a specific sequence.

2. What changes are required to use the same counter as 3 bit asynchronous down counter?

Ans)**the steps to modify a counter into a 3-bit asynchronous down counter:**

Change the initial state: For an up counter, the initial state is typically 000. In a down counter, the initial state should be set to the highest count value, which is 111 for a 3-bit counter.

Change the count sequence: In an up counter, the Flip-Flops are usually configured to increment the count on clock pulses. In a down counter, they should decrement the count when a clock pulse is received.

Update the JK Flip-Flop configurations: To create a 3-bit asynchronous down counter, set up the JK Flip-Flops as follows:

For the first Flip-Flop (LSB), configure J=0 and K=1. This means it toggles (Q flips) on every clock pulse.

For the second Flip-Flop, connect its clock input to the output of the first Flip-Flop and configure J=0 and K=1. This Flip-Flop toggles on the falling edge of the clock signal,

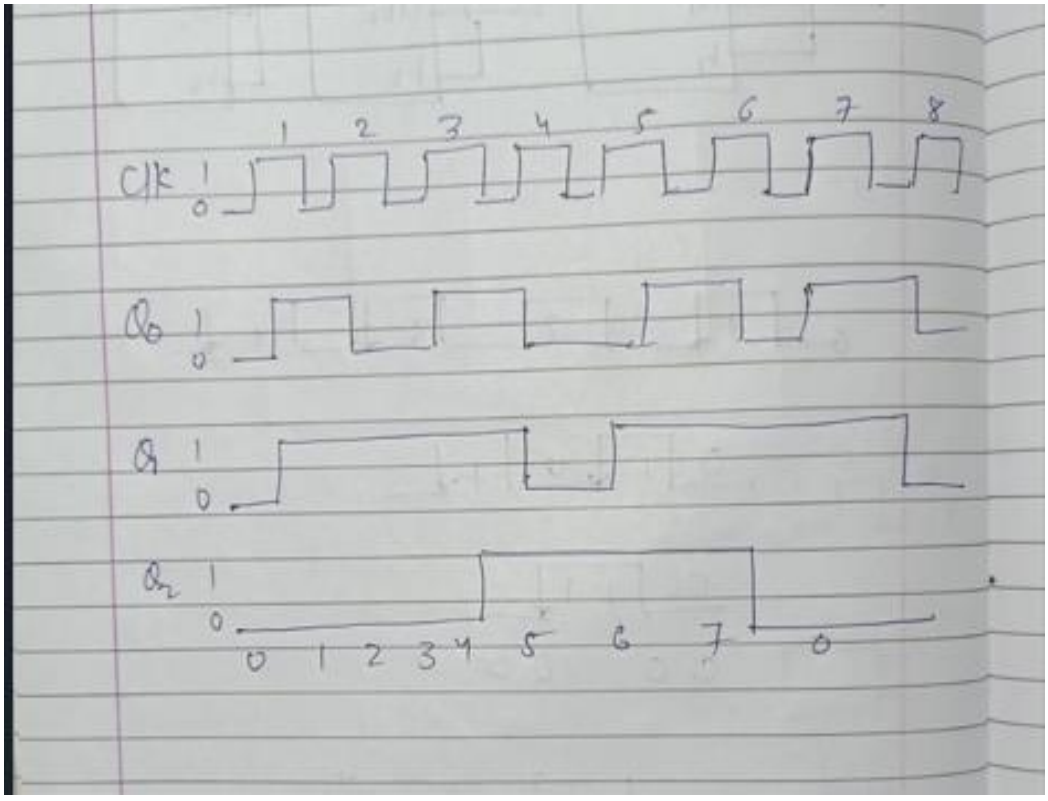
creating a binary "10" sequence.

For the third Flip-Flop (MSB), connect its clock input to the output of the second Flip-Flop and configure J=0 and K=1. This Flip-Flop toggles on the falling edge of the second Flip-Flop's output, creating a binary "100" sequence.

Clock signal: Ensure that the clock signal is provided appropriately to all Flip-Flops, and that it should trigger them on the falling edge (because you are counting down).

3. Draw the timing diagram of 3 bit Asynchronous up counter.

Ans)



4. What is mod n concept used in counters?

Ans)**The "mod n" concept in counters refers to the counting range or the maximum count value that a counter can reach before it resets back to zero (or another predefined starting value). It's a fundamental concept in digital electronics and is often used to design counters for specific applications.**
In the context of counters, "mod n" means that the counter will count from 0 to n-1 before resetting. Here's a breakdown of how it works:

Modulus (n): This represents the counting range of the counter. For example, if you have a "mod 10" counter, it means the counter will count from 0 to 9 before resetting. In binary, a "mod 10" counter counts from 0000 to 1001 (0 to 9 in decimal).

Reset to 0: When the counter reaches its maximum count value (n-1), it resets back to 0. This reset can be triggered by a clock signal or some other control signal.

5. For Mod-5 counter how many JK FFs are required?

Ans) **3**

Conclusion:

In this experiment, we learned to design and implement 3 bit Asynchronous up counter using JK Flip Flop

Signature of faculty in-charge with Date: