K. J. Somaiya College of Engineering, Mumbai-77

Experiment / Assignment / Tutorial No. 6
Grade: AA / AB / BB / BC / CC / CD /DD
Signature of the Staff In-charge with date

Batch: D2	**Roll No.: 16010122323**	**Experiment / assignment / tutorial No.: 6**

Title: Shift Register

Objective: To implement the SISO, SIPO, PISO, PIPO shift register using D flips flop

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Expected Outcome of Experiment:

CO2: Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

Books/ Journals/ Websites referred:

- VLab Link: http://vlabs.iitkgp.ernet.in/dec/#
- R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill
- M .Morris Mano, "Digital Logic & computer Design", PHI
- A.P.Godse, D.A.Godse, "Digital Logic Design"

Pre Lab/ Prior Concepts:

A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-Flip flop cascaded with output of one flip flop connected to input of next flip flop. All flip flops receive common clock pulses

which causes the shift in the output of the flip flop.The simplest possible shift register is one that uses only flip flop. The output of a given flip flop is connected to the input of next flip flop of the register. Each clock pulse shifts the content of register one bit position to right.

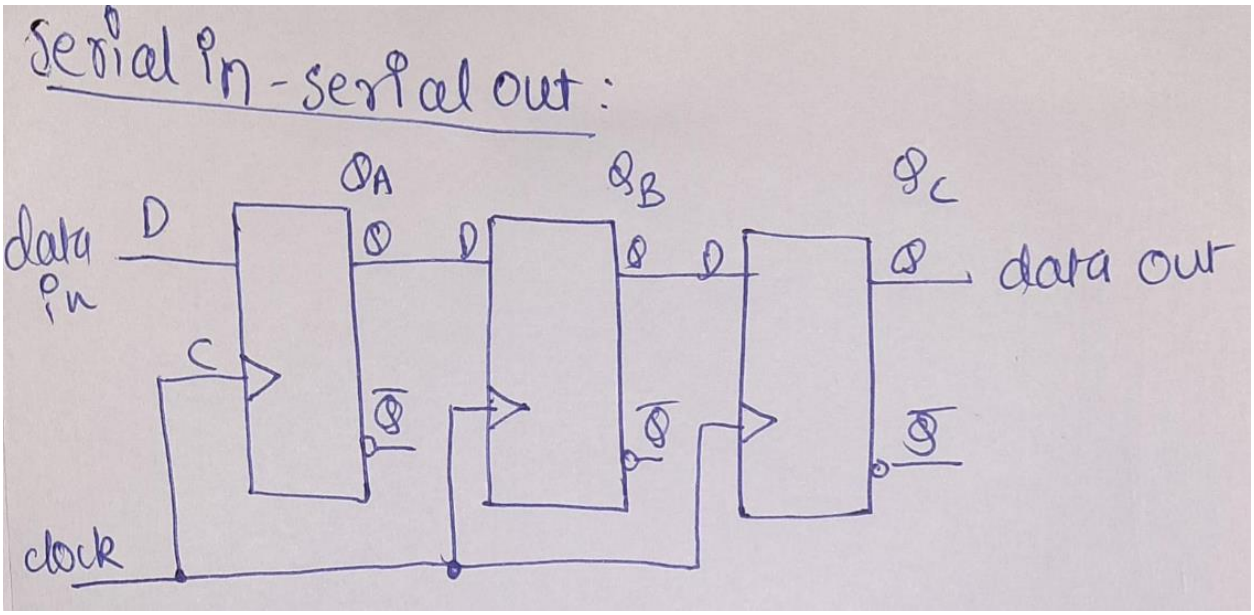
The basic types of shift registers are

- Serial In - Serial Out
- Serial In - Parallel Out
- Parallel In - Serial Out
- Parallel In - Parallel Out
- Bidirectional shift registers.

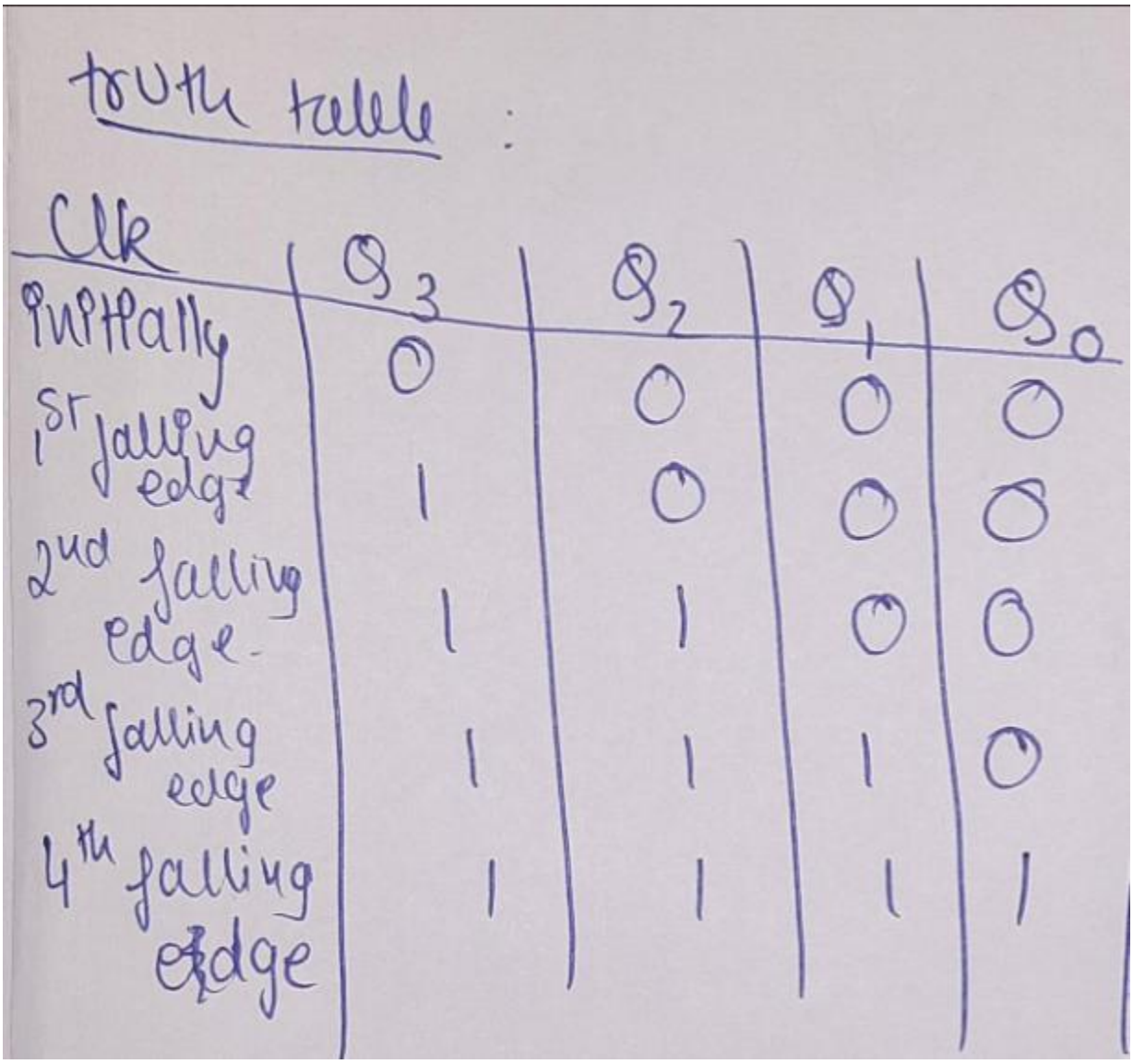
Implementation Details:

Logic Diagram

Serial in Serial Out



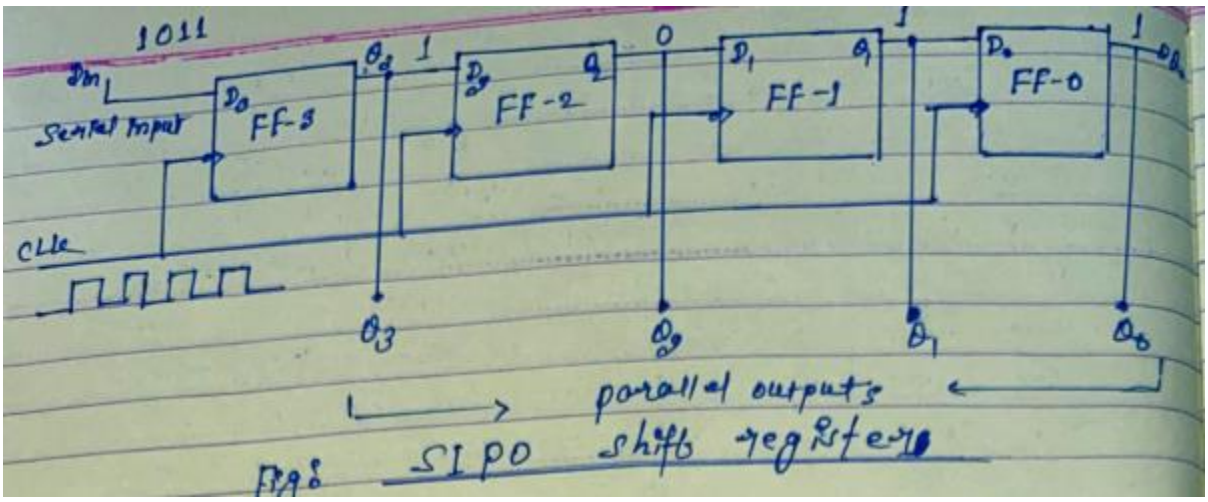
Truth table



truth table :

Clk	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1st falling edge	1	0	0	0
2nd falling edge	1	1	0	0
3rd falling edge	1	1	1	0
4th falling edge	1	1	1	1

Serial In - Parallel Out



Truth table

Truth table :

CLK pulse	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	0	1	0
4	1	1	0	1

Parallel In Serial Out

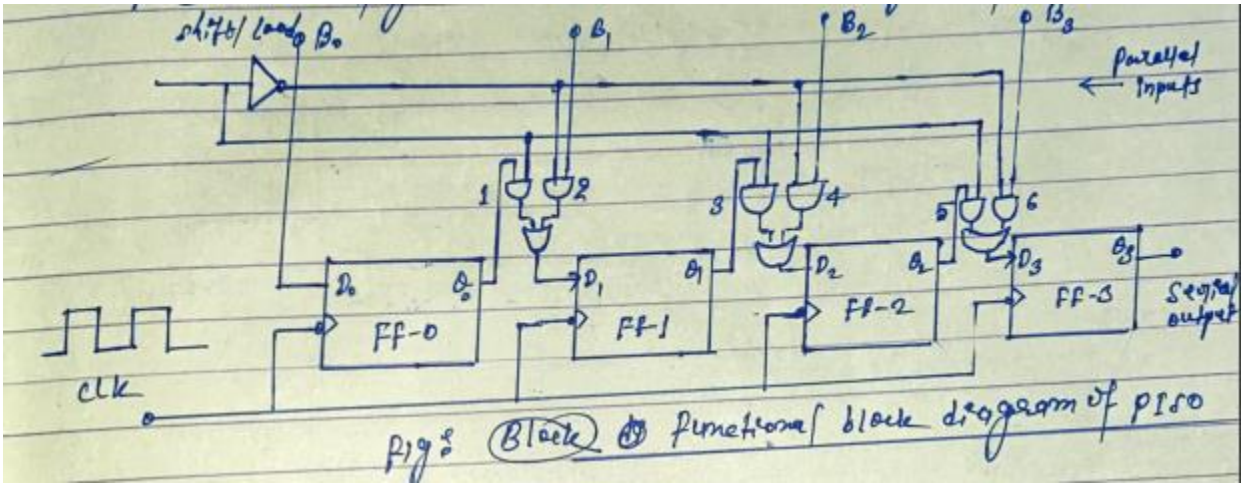
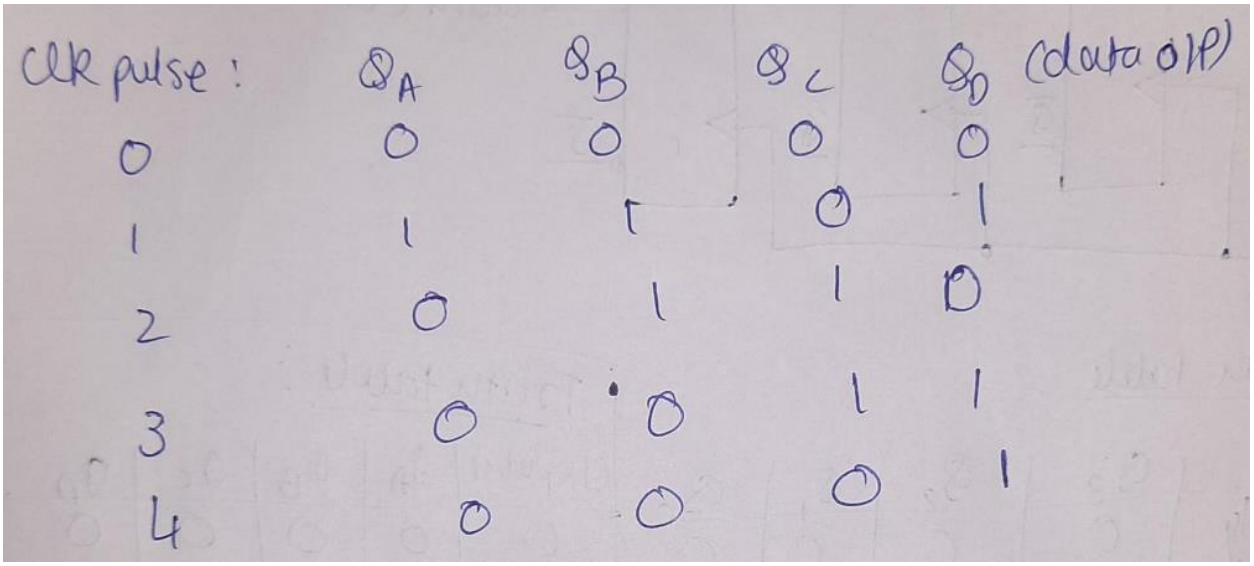
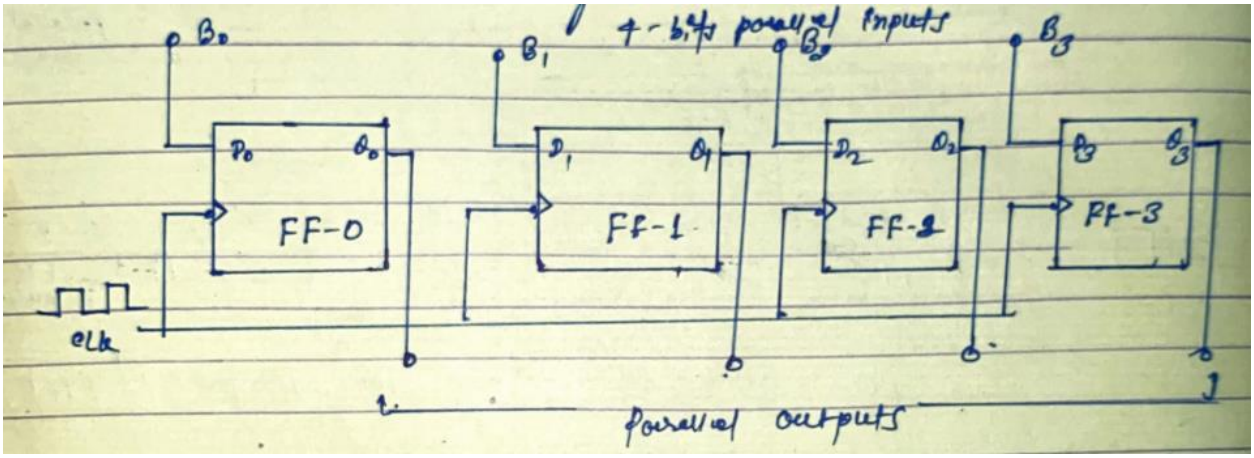


Fig: Block & functional block diagram of PISO

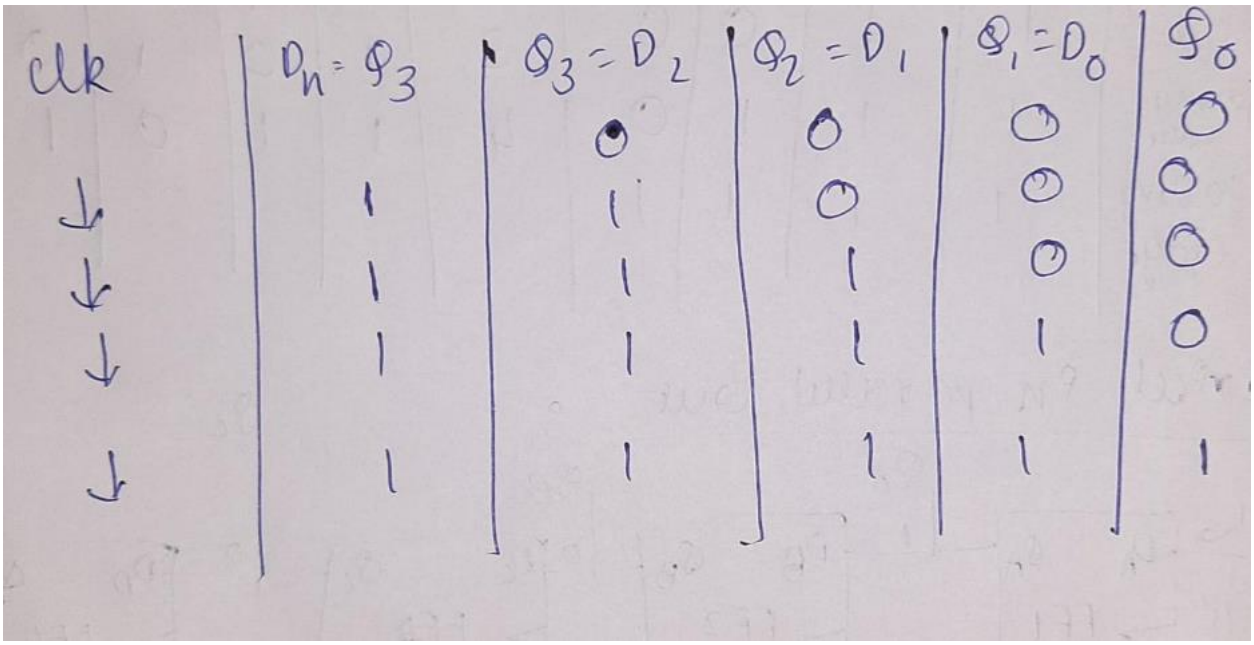
Truth table



Parallel In Parallel Out



Truth table



Conclusion: **In this experiment, we learned to implement the SISO, SIPO, PISO, PIPO shift register using D flips flop**

Post Lab Descriptive Questions

1. What is a universal shift register?Which MSI TTL IC is used as a Universal Shift Register?Attach its pin diagram and Truth table from the data sheet.

Ans) A universal shift register is a digital circuit that can perform both parallel and serial data transfer operations. It allows data to be shifted either left or right (serially) and can also load data in parallel. This versatility makes it a valuable component in digital systems where data needs to be shifted or transferred in different ways.

One of the commonly used MSI (Medium Scale Integration) TTL (Transistor-Transistor Logic) ICs that can be used as a universal shift register is the 74194. The 74194 is a 4-bit

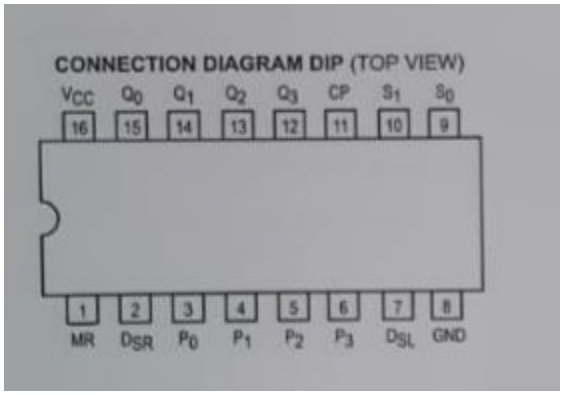
universal shift register with parallel load capabilities. It has four data inputs (D0, D1, D2, and D3), which can be used to load data in parallel. It also has control inputs for shifting left, shifting right, parallel loading, and clearing the register.

S0 and S1: These control inputs determine the shift operation. The following combinations are possible:

S0 = 0, S1 = 0: Parallel load (PL) mode.
S0 = 0, S1 = 1: Shift right (SR) mode.
S0 = 1, S1 = 0: Shift left (SL) mode.
S0 = 1, S1 = 1: Clear (CLR) mode.
CP: Clock input for clocking the data through the register.

MR (Master Reset): Resets the register when active.

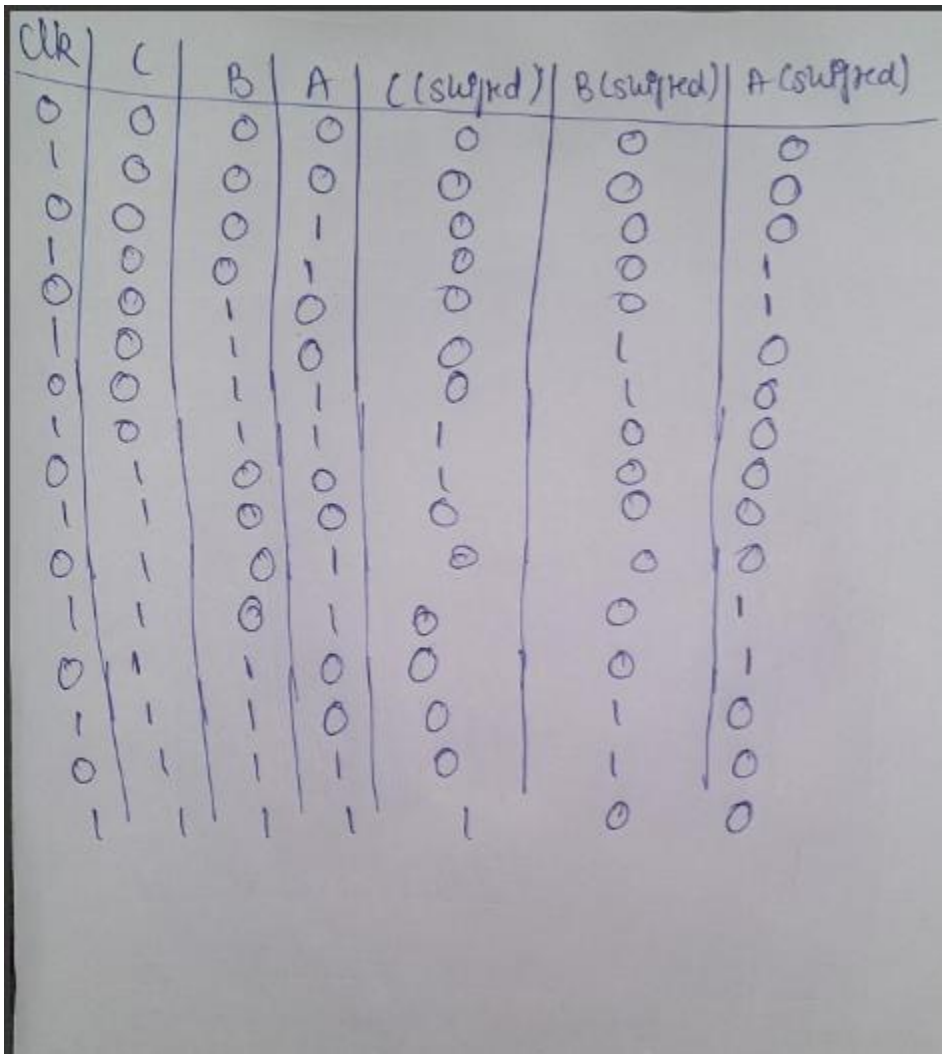
QA, QB, QC, QD: These are the four outputs of the shift register.



MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	MR	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H H	h h	l l	X X	l h	X X	q_1 q_1	q_2 q_2	q_3 q_3	L H
Shift Right	H H	l l	h h	l h	X X	X X	L H	q_0 q_0	q_1 q_1	q_2 q_2
Parallel Load	H	h	h	X	X	P_n	P_0	P_1	P_2	P_3

2. Prepare a truth table for 3 bit SISO left shift with data(- - -) along with clock pulse Ans)



3. Can a shift register be used as a counter? Give any one application.

Ans)Yes, a shift register can be used as a counter in certain applications

Ring Counter Application: Shift Register as a Frequency Divider

A common application of a shift register acting as a ring counter is as a frequency divider. In this application, the shift register divides an input clock signal by a fixed factor, effectively producing a lower-frequency output signal. The number of stages in the shift register determines the division factor.

For example, let's say you have a 4-stage ring counter (4-bit shift register). When you apply a clock signal to the first stage (Stage 1), the shift register will cycle through 4 states before repeating. Each state corresponds to a binary value (0001, 0010, 0100, 1000), effectively dividing the input clock frequency by 4. This can be useful in applications where you need to

generate lower-frequency clock signals for different parts of a digital system or for timing purposes.

Another application of ring counters is in creating sequence generators for controlling the operation of digital systems, such as controlling the lighting patterns in LED displays, generating control signals for state machines, or implementing various timing sequences in microcontrollers.

Keep in mind that the choice of the shift register's configuration (e.g., number of stages) will determine the specific counting sequence and division factor, so it can be tailored to suit the requirements of the application.

4. How many clock pulses are required to enter a byte of data serially into an 8-bit shift register?

Ans) To serially enter a byte of data into an 8-bit shift register, you would need one clock pulse per bit. Since there are 8 bits in a byte, you would require 8 clock pulses to completely load the byte of data into the 8-bit shift register.