Course Name:	Digital Design Laboratory	Semester:	III
Date of Performance:	__7_ / _8__ / __23____	Batch No:	D2
Faculty Name:		Roll No:	16010122323
Faculty Sign & Date:		Grade/Marks:	___/25

Experiment No: 3

Title: 4:1 Multiplexer and 3: 8 Decoder

Aim and Objective of the Experiment:
To design and implement a 4:1 multiplexer and 3: 8 Decoder

COs to be achieved:
CO2: Use different minimization technique and solve combinational circuits.

Tools used:
Trainer kits

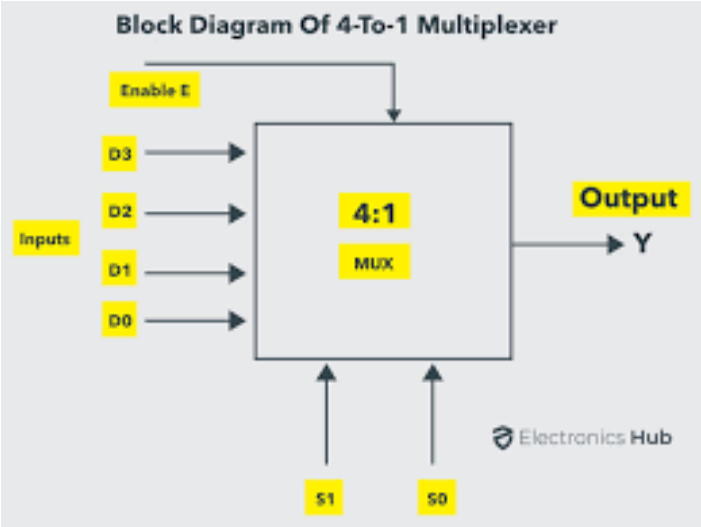
Theory:

Multiplexer: Multiplexer is a special type of combinational circuit. It is a digital circuit that selects one of the n data inputs and routes it to the output. The selection of one of the n inputs is done by the select lines. To select n inputs we require m select lines, such that 2^m=n. Depending on the digital code applied at the select inputs, one out of the n data sources is selected and transmitted to a single output.

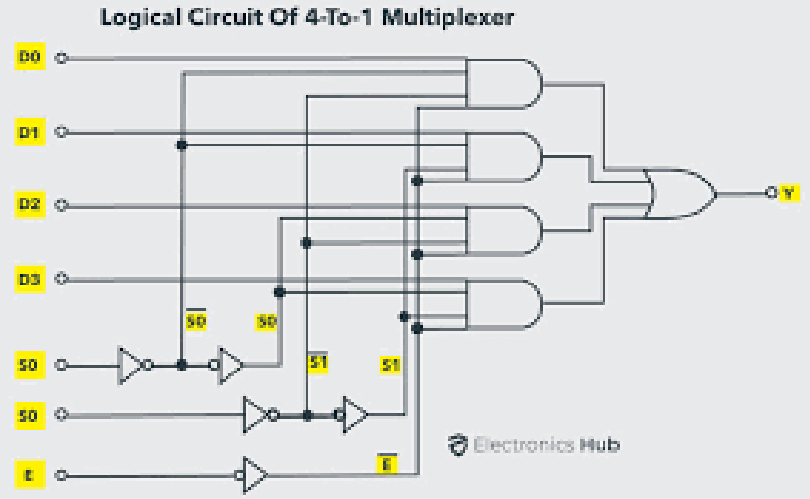
Decoder: A decoder is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. The input code generally has fewer bits than the output code, and there is a one-to-one mapping from input code words into output code words. The general structure of a decoder circuit is shown in the Figure below. The enable inputs, if present, must be asserted for the decoder to perform its normal mapping function. The most commonly used input code is an N-bit binary code, where an N-bit word represents one of 2^N different coded values. Normally, they range from 0 through $2^N - 1$. The input code lines select which output is active. The remaining output lines are disabled.

Implementation Details:

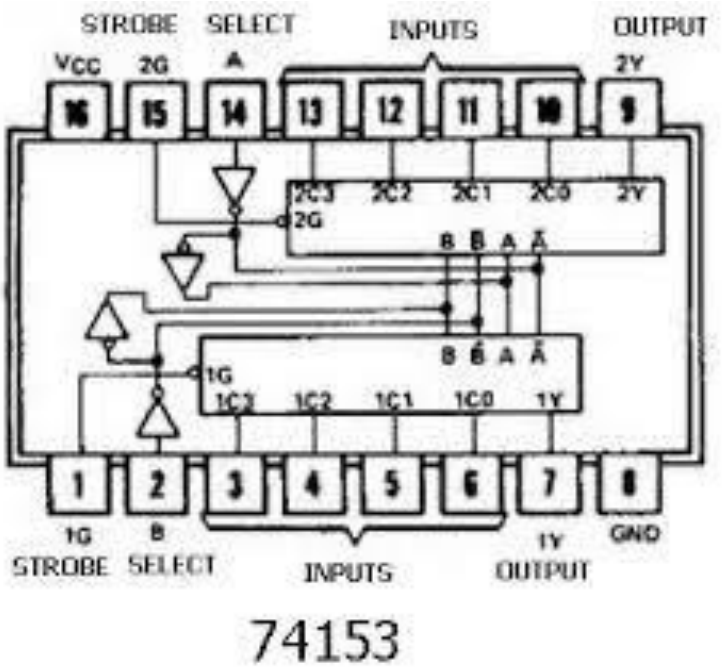
4:1 Multiplexer Block Diagram



4:1 Multiplexer Circuit



Pin Diagram IC74153

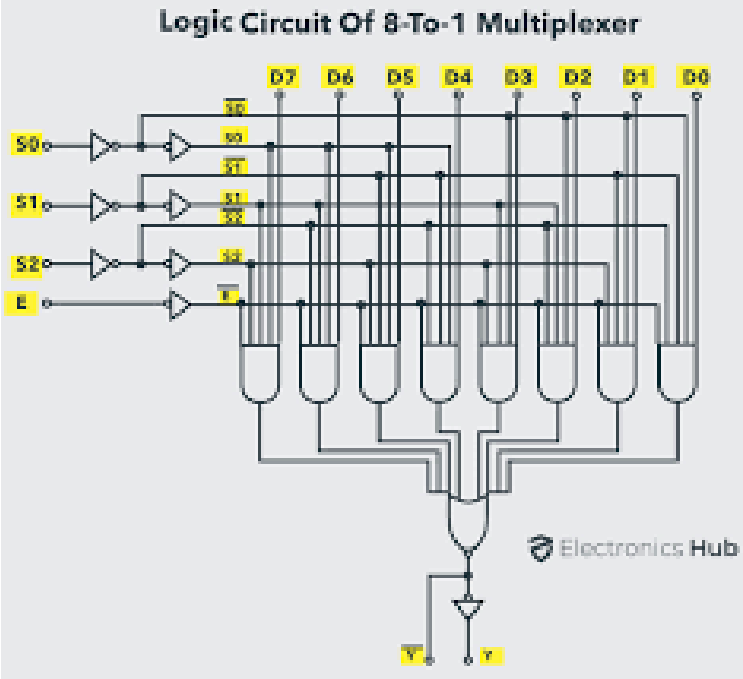


Implementation Details of 8:1 MUX

Larger Multiplexers can be constructed by using lower multiplexers by chaining them together. Here, an 8:1 multiplexer can be formed with two 4:1 and one 2:1 multiplexer.

Thus, we can use two 4x1 Multiplexers in first stage to get the 8 data inputs. And the yield of each multiplexer will feed into a 2x1 Multiplexer in successive stage by considering the yields of first stage as inputs and to produce the result Y.

Circuit Diagram of 8:1 MUX



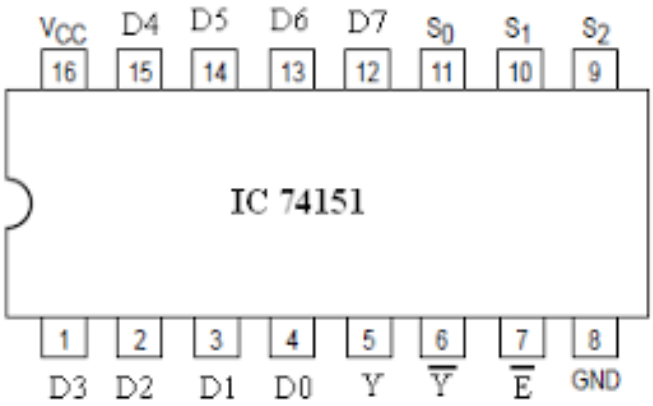
Truth Table for 8:1 Multiplexer

INPUTS			Output
S_2	S_1	S_0	Y
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

From Truth Table:

Y = S0'.S1'.S2'.A0+S0.S1'.S2'.A1+S0'.S1.S2'.A2+S0.S1.S2'.A3+S0'.S1'.S2 A4+S0.S1'.S2 A5+S0'.S1.S2 .A6+S0.S1.S3.A7

Pin diagram: IC 74151



Implementation Details

Procedure:

1) Locate the IC 74153 and place the IC on trainer kit.
2) Connect VCC and ground to respective pins of IC trainer kit.
3) Implement the circuit as shown in the circuit diagram.
4) Connect the inputs to the input switches provided in the trainer kit.
5) Connect the outputs to the switches of O/P LEDs
6) Apply various combinations of inputs according to the truth table and observe the condition of LEDs.
7) Note down the corresponding output readings for various combinations of inputs.

Post Lab Subjective/Objective type Questions:

1. Design and verify a 2:1 multiplexer using logic gates.

Apply these steps to design a 2:1 Mux using logic gates:

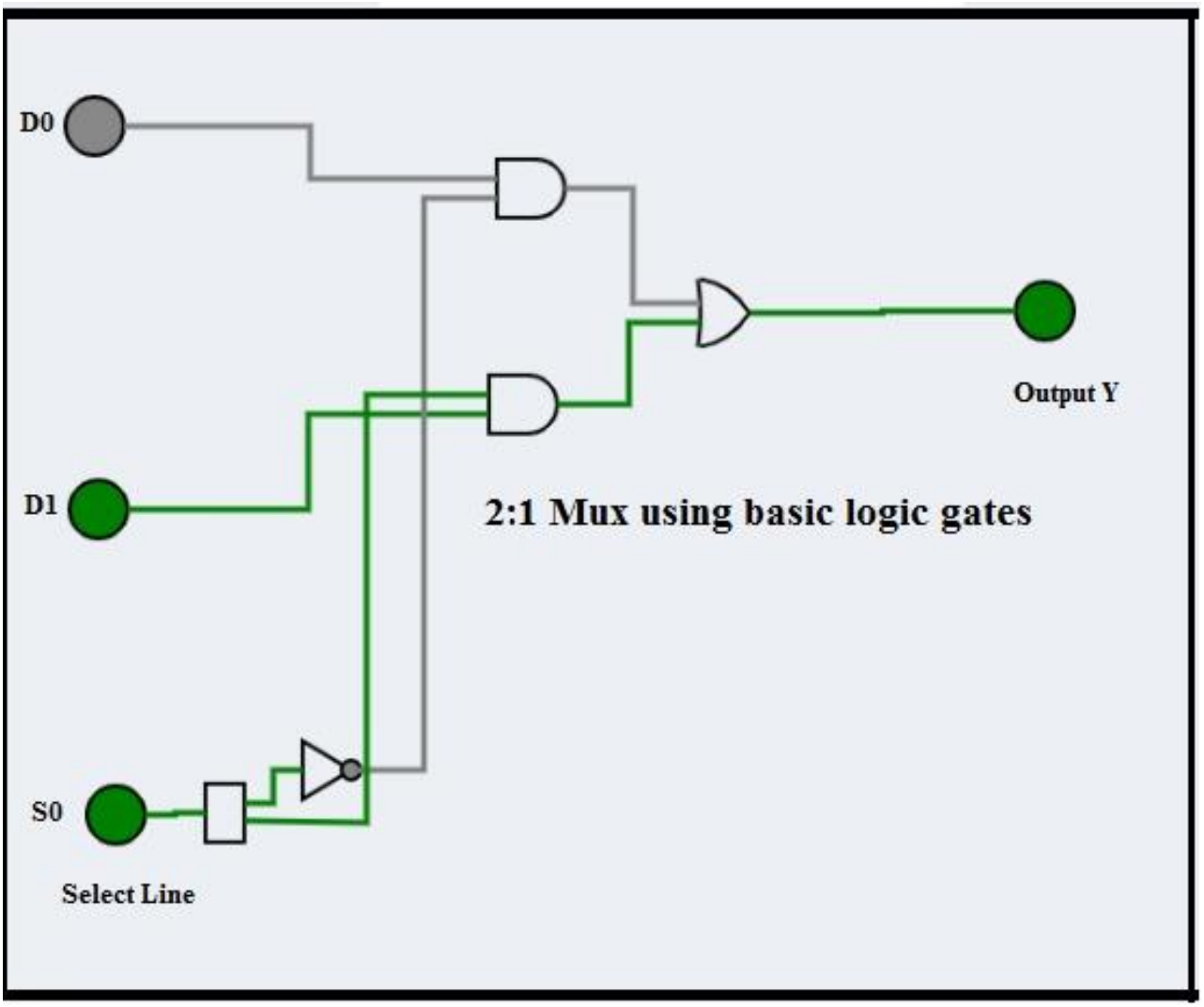
a. Prepare the function table of the 2:1 Mux:

Select I/p	Inputs		Fundamental Product FP	Output Y	Output Y (in terms of input)
S0	D1	D0			
0	X	0	S0'. D0'	0	Y = D0
0	X	1	S0'. D0	1	
1	0	X	S0 . D1'	0	Y = D1
1	1	X	S0 . D1	1	

b. Formulate the expression for output Y by considering only those FPs for which the output is 1. Y = S0'. D0 + S0 . D1 The simplified function can be tabulated as:

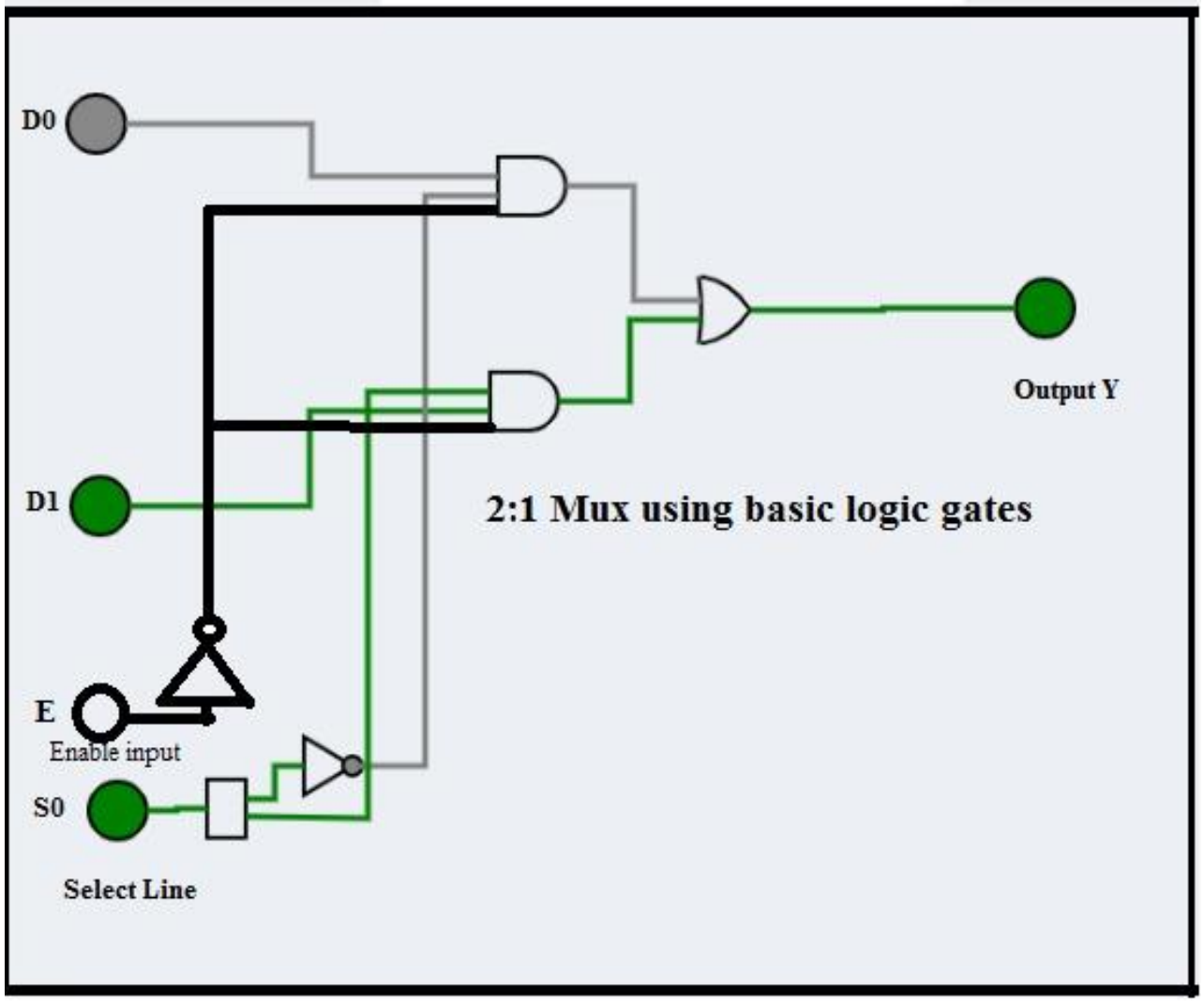
Select Input S0	Output Y
0	Y = D0
1	Y = D1

c. Draw the logic diagram for the expression:



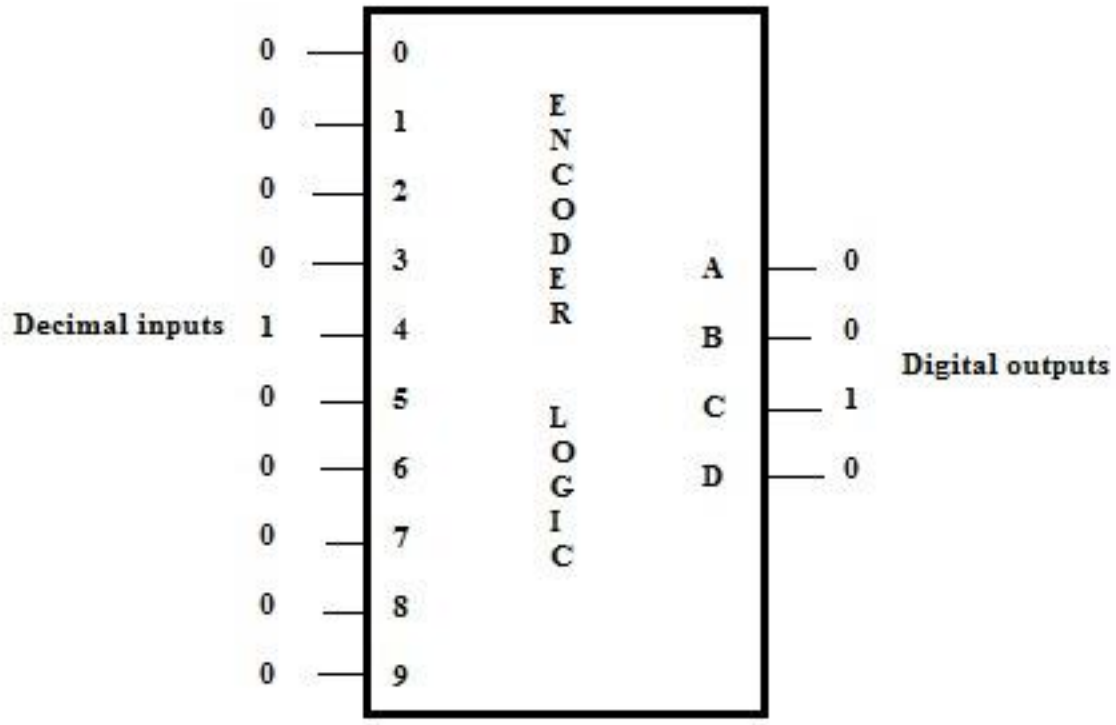
d. Using simulator construct the circuit and verify its operation.
e. The same circuit can also be designed by having an active low enable input as shown in image. The simplified function can be tabulated as:

Select Input S0	Enable Input E	Output Y
X	1	0
0	0	Y=D0
1	0	Y=D1

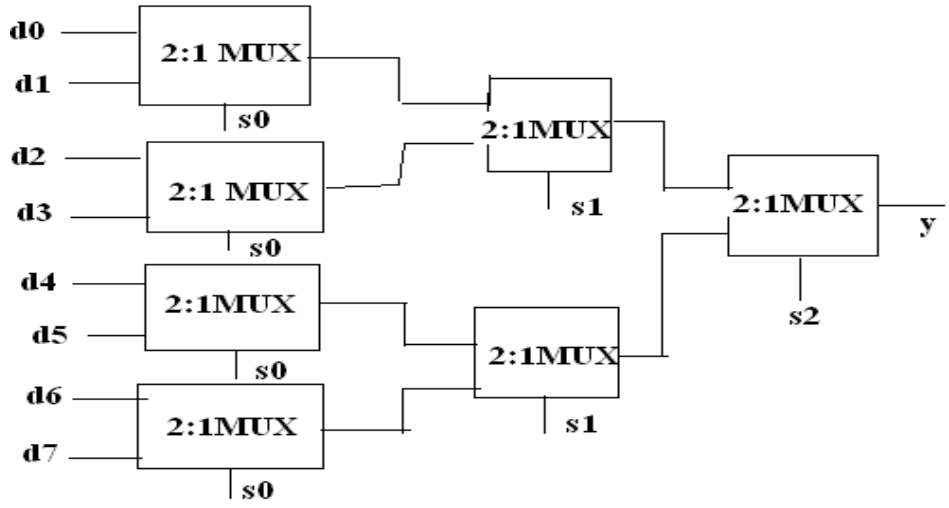


1.3. Encoder Logic The figure shows the concept of encoder wherein input line 4 is high and all other inputs are low. The output of the encoder is a decimal 4, whose equivalent binary is 0100.

The concept of decimal to binary(10 to 4 binary) encoder is shown in the figure given below. On similar lines an octal-binary encoder will have eight inputs and produce 3-bit binary output.



2. Build an 8:1 multiplexer using only 2:1 multiplexers.



Conclusion:
Thus we have learned about and implemented multiplexers.

Signature of faculty in-charge with Date: