Analog Multiplier Using Gilbert Cell

Vedhant abrol (2023PVL0098)

***Abstract*—This project report presents the development of an analog multiplier utilizing the Gilbert cell architecture in a 180nm technology node, implemented using SymicaDE software. The multiplier operates under a 5V power supply and performs multiplication of two input with multiplication factor $\alpha = 1.28$. Input signal is sine waveforms with frequencies of 1GHz and 0.5GHz, both with a 1V DC offset .**

I. Introduction

Fig. 1 is of basic Gilbert cell. Our study of differential pairs reveals two important aspects of their operation:
(1) the small-signal gain of the circuit is a function of the tail current, and
(2) the two transistors in a differential pair provide a simple means of steering the tail current to one of two destinations. By combining these two properties, we can develop a versatile building block.

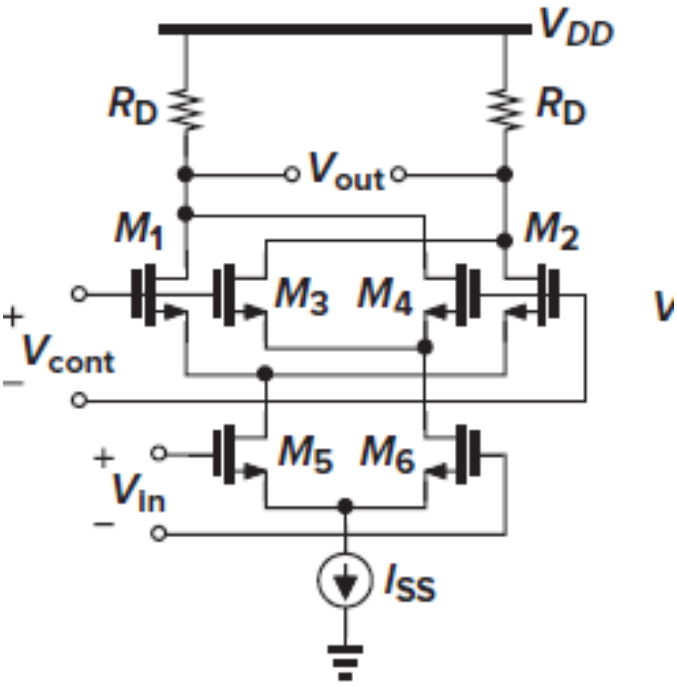

Fig. 1. Basic gilbert cell circuit .
Source :Fig.4.43(a) from " Razavi, B. (2005). Design of analog CMOS integrated circuits. "

Since the gain of the circuit is a function of V_{cont}= $V_{cont1}V_{cont2}$, we haveV_{out} = V_{in} · f (V_{cont}). Expanding f (V_{cont}) in a Taylor series and retaining only the first-order term,αV_{cont}, we have $V_{out} = \alpha V_{in} V_{cont}$. Thus, the circuit can multiply voltages. This property accompanies any voltage-controlled variable-gain amplifier. Fig . 1 shows a basic gilbert cell.

II. Design Procedure

A. Basic amplifier

To get a basic understanding of how amplifiers work and obtaining desired values of resistance, threshold voltage, bias voltage we use simulation of basic common source topology in symica. Schematic of Common source amplifier is shown in Fig. 2

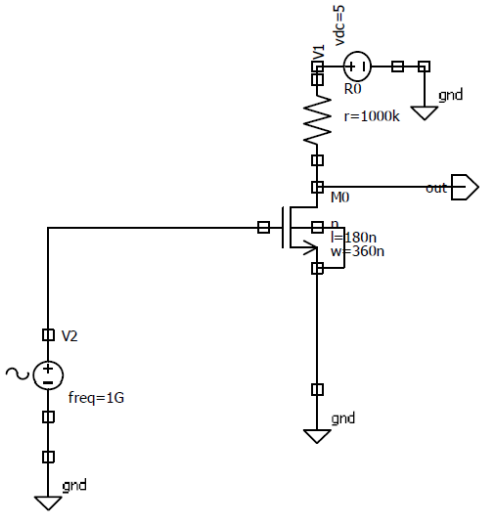

Fig. 2. CS topologySource:"SymicaDE snapshot of schematic"

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B. Differential pair

Now proceeding with the understanding of parameters and simulations of Current source topology, we can proceed building a differential pair and analyse its working which is basic building block of Gilbert cell. Schematic of Differential pair is shown in Fig. 3

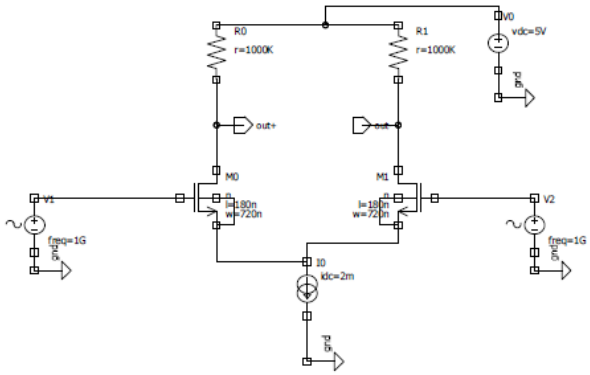

Fig. 3. MOS differential pairSource:"SymicaDE snapshot of schematic"

C. Gilbert multiplier using ideal current source

After getting basic understanding of Differential pair we will build a ideal gilbert cell using ideal current sources and do its anlysis so that we can proceed with our main Gilbert cell multiplier circuit. Schematica of Gilbert cell using ideal current sources is shown in fig. 4

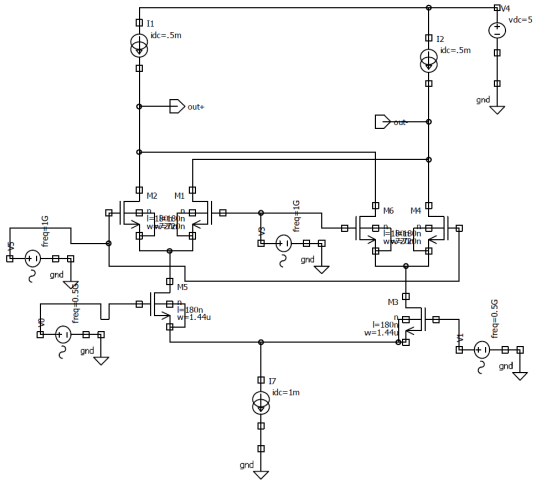

Fig. 4. Gilbert cell using ideal current .
Source:"SymicaDE snapshot of schematic"

Fig. 5 is the simulated result of Gilbert cell using ideal current sources.

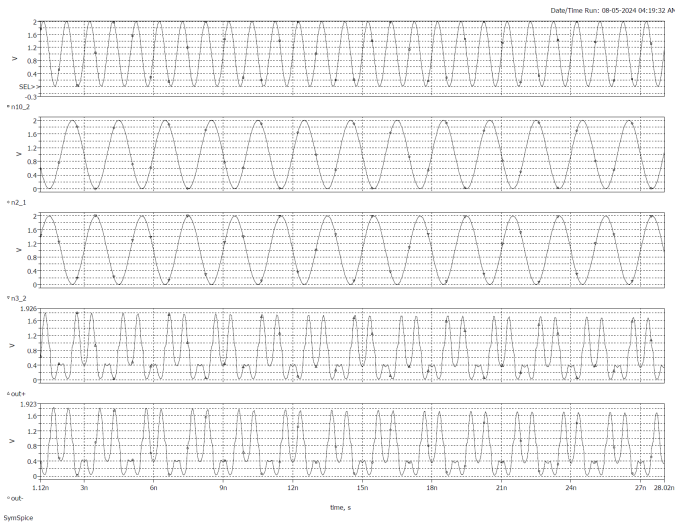

Fig. 5. Waveform of Fig. 4Source:"SymicaDE snapshot of simulation"

D. Gilbert cell multiplier circuit

Now keeping the observations of above circuits we can build a complete multiplier circuit shown in fig. 6

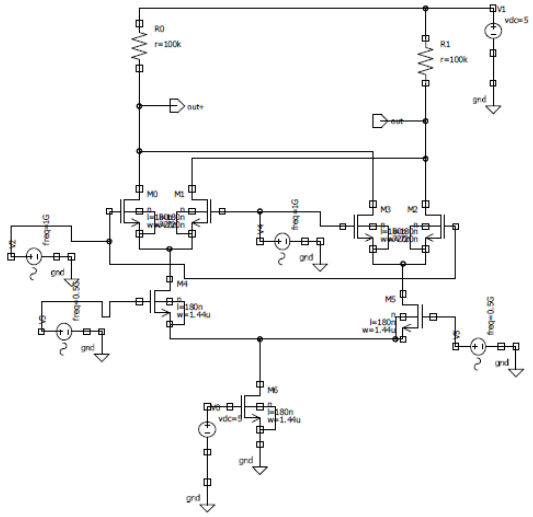

Fig. 6. Schematic of Gilbert cell multiplier
Source:"SymicaDE snapshot of schematic"

Waveform of simulated result is shown in Fig. 7.
We can see from waveform Fig. 7 that it is successfully multiplying input signals with 2V peak to peak . We can find Multiplication factor α from output waveform, which is coming out to be approximately 1.28.

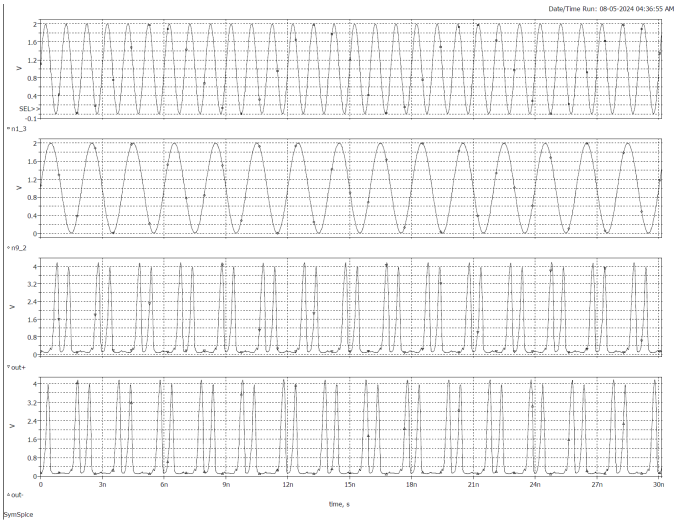

Fig. 7. waveform of multiplied signals.
Source:"SymicaDE snapshot of waveform"

III. RESULTS AND OBSERVATIONS

A. INPUTS and OUTPUTS

V_{dd}	5V
V_2, V_4	1V DC and 2V peak-to-peak
V_{out+}	upto 4.14V
R_0, R_1	100KΩ
M_0, M_1, M_2, M_3	4
M_4, M_5, M_6	8
α(multiplication factor)	1.28

TABLE I
INPUT / OUTPUT TABLE

B. observations

In this project, I have successfully completed the design of a multiplier, encompassing circuit design and simulation which multiplies two inputs with multiplication factor $\alpha = 1.28$. The multiplier was simulated using Symica and 180nm design kit.This study enhances the comprehension of Gilbert cell functionality and its utilization as a voltage multiplier, providing valuable insights for both researchers and practitioners. Future research directions may delve into optimization techniques, explore advanced applications, and investigate integration into broader electronic systems, thereby propelling the development of voltage multiplier design based on the Gilbert cell architecture.

REFERENCES

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[2] Nandini, A. S., Sowmya Madhavan, and Chirag Sharma. "Design and implementation of analog multiplier with improved linearity." international Journal of VLSI design and communication systems (VLSICS) 3.5 (2012): 631-637.
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