VLSI CIRCUIT DESIGN LAB REPORT

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***Abstract*—To design the schematic of CMOS inverter and to do its AC and DC analysis in Cadence Virtuoso.The Cadence Virtuoso System Design Platform is a holistic, system-based solution that provides the functionality to drive simulation and LVS-clean layout of ICs and packages from a single schematic. We are going to use the Virtuoso tool for making the schematic of a simple CMOS inverter and for seeing its different simulation and responses by varying certain parameters and will derive some conclusions and calculations.**

I. Introduction

The process to start the Cadence tool is as follows. As we click on open terminal the block will open here we have to write command csh then press 'Enter' key then type source/home/install/cshrc and then press 'Enter' then Type virtuoso press Enter then one block will open.

- Step 1: Click on File then click on New then click on Library.
- Step 2: New library block will open in the name field of library write the name.
- Step 3: Select 'Attach to an existing technology library' and click on OK then 'Attach Library to Technology Library' window would open.
- Step : I choose gpdk45 technology library and click on OK.gpdk45 technology is used for design a CMOS inverter circuit.
- Step 5: command Interpreter window will appear then click file then click on New then click on Cellview now we will make new file as follows. Library:vedhant, Cell:vedhantcell, View: schematic, Type: Schematic, Application open with: schematic L.
- Step 6: Click on OK when done a blank schematic block for the inverter design appears. here we will made design of CMOS inverter. Here we will do the analysis of CMOS circuit with the help of simulation.
  1) Transient analysis
     a) Delay Calulation at different temperature
     b) Dynamic power at different temperature.
     c) leakage powerat different temperature.
  2) DC analsis
  3) Process corners
     a) Delay and Dynamic power in FF
     b) Delay and Dynamic power in SS
     c) Delay and Dynamic power in FS
     d) Delay and Dynamic power in SF
  4) Monte Carlo

II. SIMULATION OF DIFFERNT PARAMETER OF CMOS CIRCUIT

First of all we will make schematic of CMOS circuit on cadence tools the procedure is as follows. for CMOS inverter we required NMOS and PMOS.

1) For this we will clik on create then click on instance or we can use shortcut key 'i'.The window would open of 'Add instance'.
2) Click on Browse to get library component another window would open choose Library as I select gpdk45. cell:nmos1v,View:symbol.
3) click on hide move your pointer to the schematic window and just place it in proper way. if we want to change the properties of nmos transistor we can change by selecting nmos and we have to press 'Q'.width of NMOS is 120nm.
4) Repeat the above for PMOS and I change the width of PMOS to 240nm.Keep both PMOS and NMOS in vertical position that we can connect both by wire. If we have to move the component then select the componentnwhich we need to move and press 'm' move it to your required location. press 'Esc' keeping your pointer in the schematic window.
5) Now we will take voltage sources vpulse and vdc.follow the step click create then instance window will open select Library:analogLib,cell:vpulse,view:symbol click on hide and place it. click 'Q' and I give period:40ns,pulse width:20ns,voltage1:0,voltage2:1.8V click apply and then OK.
6) for Vdc click create then instance window will open select Library:analogLib,cell:vdc,view:symbol click 'Q' and I will give DC voltage:1.8V and place it. after taking any component we place it then we will click on 'Esc'.
7) NOW we will take a pin for input ,output ,ground,and source vdd Click Create then pin or you can use shortcut 'P' then 'Add Pin' window will appear for input pin

Enter the pin name as I given vin,gnd,and vdd Direction:input and similarly for out pin enter pin name Vout Direction:output and place it on schematic window in proper way.

8) Click on ADD then wire or you can use shortcut 'W' to enter wiring mode click 'Esc' to exit.and connect the component accordingly. Now last step is to check our circuit click Check and Save button.We will save our work
9) Check command interpreter window for checking of error .If no error then we can do the simulation of CMOS circuit. The final schematic is shown below

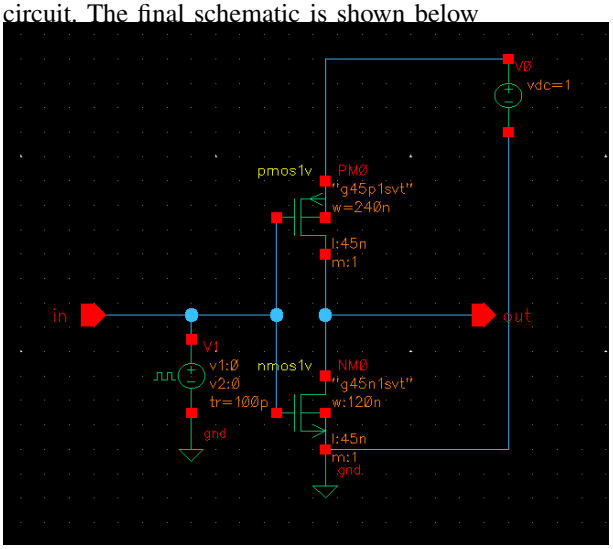

figure 1: Schematic

A. TRANSIENT ANALYSIS

In transient analysis as we apply pulse voltage to the input with period of 40ns and pulse width of 20ns.Input will be change from 0 to Vdd which is in pulsating wave then output will be change from Vdd to 0.But there is delay due to parasitic capacitance's For doing the simulation of CMOS circuit we need top follows step as below.

1) In the schematic window click Launch you we see the different option we have to choose ADE (Anolog Design Environment) L again 'ADE L' window will open.
2) Now we will do Analysis from 'Analyses'. Clickon Analyses then Choose then Select the trans i.e. transient analysis to be done.We have to provide stop time as 400ns, Accuracy Defaults:moderate then click on OK.
3) From the ADE L window click on OUTPUT then TO be plotted then Select on Design it will pop up the schematic editor window the select 'output' and 'input' to be plotted and save it.
4) Now we will run simulation by clicking on 'Simulation' then Netlist then and then Run. we can see the figure as shown in below.

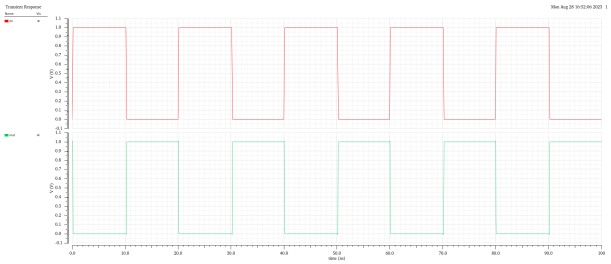

figure 2: Transient response analysis of CMOS inverter

1) Delay calculation at different temperature: In every CMOS inverter circuit there is parasitic capacitance due to which delay come into picture.Which play important role in the analysis of CMOS inverter.Here we are going to calculate delay of CMOS inverter circuit with the help calcula tor tools present in cadence tools.As the capacitance increases delay will also increases. For the calculation of Delay,Rise Time and Fall Time we will calculate from above figure 1 shown i.e. transient analysis of CMOS circuit. Calculator can be used to calculate many different parameter follow the following steps to calculate. Click on Tools and then Calculator "Virtuoso Visualization and Analysis XL calculator" window will open.

Delay calculation

a) Now click on 'vt' and from schematic editor window and select the input node 'input'.Expression will be appear we have to copy the expression.
b) From function panel choose 'Special functions' and choose the delay.
c) Window will appear put the expression previously obtained in the 'Signal1' .
d) Now for output select 'vt' go to schematic editor window and click on output node 'out'.Expression will be appear we have to copy the expression.
e) Copy that expression into 'Signal2'.
f) For signal1 Threshold value1:1.8,Edge Number1:1,Edge Type1:rising,Periodicity1:1 For signal2 Threshold value2:1.8,Edge Number2:1,Edge Type2:falling,Periodicity2:1 click on OK the expression will appear and then click on Evaluate buffer icon. then we we get the value of delay and we can send it to 'ADE L' .

$$t(d) = \frac{t(plh)+t(phl)}{2} \quad ...(1)$$

Rise time calculation

a) Now choose 'vt' and from schematic editor window and click on output node 'output'.Equation will be appear.
b) From function panel choose 'Special functions' and then choose risetime.
c) Then click on Evaluate buffer icon. Rise time will be shown in the window and we can send to ADE

L.

$t_{plh} = 0.69 \cdot RONp \cdot CL$ ... (2)

Fall time calculation

a) Now choose 'vt'and from schematic editor window and select output node 'output'.Equation will be appear.
b) From function panel choose "Special functions" and choose the falltime.
c) Then click on Evaluate buffer icon. Fall time will be shown in the window and we can send to ADE L.

$t_{phl} = 0.69 \cdot RONn \cdot CL$ ... (3)

From figure 1 we can find
$t_{plh} = 0.0255\,\text{ns}$
and
$t_{phl} = 0.03189\,\text{ns}$
now using formula (1)
$t_d = 0.028695\,\text{ns}$
Now given below is table for Delay at different temperatures.

Temp	Delay
0°	24.1 ps
25°	24.2 ps
50°	25.72 ps
75°	26.36 ps
100°	27.05 ps
125°	27.08 ps

Table 1: Delay at different temperature.

2) Dynamic power at different temperature: dynamic power" refers to the power consumption that occurs during the switching of digital signals. CMOS inverters are fundamental building blocks in digital integrated circuits, and they consist of a PMOS (p-channel) transistor and an NMOS (n-channel) transistor, connected in series between the power supply and ground.
Dynamic power primarily results from the charging and discharging of internal node capacitances within these transistors as they transition from one logic state to another. When an input signal to a CMOS inverter changes, either the PMOS or NMOS transistor conducts while the other is in the off state. During this transition, there is a brief moment when both transistors are partially on, which causes a direct path between the power supply and ground, leading to a short-circuit current. This results in a significant dynamic power consumption. The dynamic power is directly proportional to the frequency of signal transitions and the load capacitance (Cload) attached to the output of the CMOS gate.
The dynamic power dissipation in a CMOS inverter can be calculated using the following formula:

$P_{\text{dynamic}} = 0.5 \cdot C_{\text{load}} \cdot V_{\text{dd}}^2 \cdot f$
Given below table is Dynamic power at different temperature:

Temp	Dynamic power
0°	12.97 nW
25°	13.38 nW
50°	13.81 nW
75°	14.24 nW
100°	14.62 nW
125°	14.95 nW

Table 2: Dynamic power at different temperature.

3) Leakage Power at different temperature: Power dissipated in a digital circuit even when it is in a static or idle state, meaning there are no active signal transitions or computational tasks being performed. Leakage power is a significant component of a digital circuit's power consumption and can be a major concern in modern semiconductor technology. Given below table is Leakage power at different temperature:

Temp	Leakage power
0°	2.33 pW
25°	3.946 pW
50°	7.547 pW
75°	14.62 pW
100°	27.21 pW
125°	48.00 pW

B. DC Analysis

This is used to analyse the operating point of the circuit and to study the input and output characteristics of the circuit. D analyis is performed under static condition and it gives the input output characteristics for the steadty state condition and it is different from transient analysis. DC response of the CMOS inverter is shown in figure.

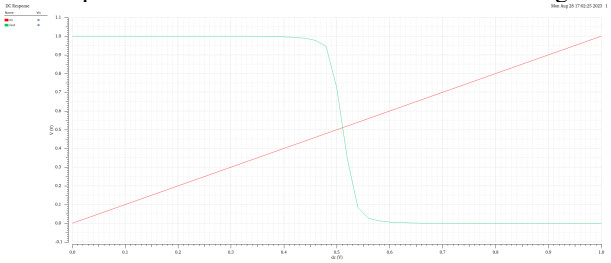

figure 1: DC response analysis of CMOS inverter

C. Width variation analysis

In CMOS technology, transistor performance is significantly affected by variations in the width (W) of MOSFET devices. The transistor width determines the current-carrying capability and, subsequently, the speed and performance of digital circuits. Given below table delay at different Width:

Nmos,Pmos	Delay
120, 240nm	25.22 ps
240,480nm	25.36 ps
360,720nm	25.93 ps
480, 960nm	25.89 ps

D. *Process Corner*

Process corner analysis assesses the CMOS inverter's resilience under different manufacturing scenarios. It involves testing at best-case, worst-case, and nominal conditions, revealing how process variations affect performance and reliability.

Process corner	**Delay (s)**	Power Dynamic
tt	275.9×10^{-12}	2.072×10^{-6}
ff	216.96×10^{-12}	2.071×10^{-6}
ss	381.29×10^{-12}	2.074×10^{-6}
fs	241.393×10^{-12}	2.072×10^{-6}
sf	322.642×10^{-12}	2.0723×10^{-6}

E. *Montecarlo Analysis*

Monte Carlo analysis is a method used to understand how random variations during manufacturing affect the performance of CMOS inverters. It does this by introducing randomness or variability into crucial parameters, such as the thresholds of transistors and oxide thickness. This process provides valuable insights into issues related to yield (the number of functioning chips produced) and the reliability of the chips. In essence, Monte Carlo analysis helps designers account for the uncertainties and variations that occur during the manufacturing process, allowing them to make more robust and reliable CMOS inverters.

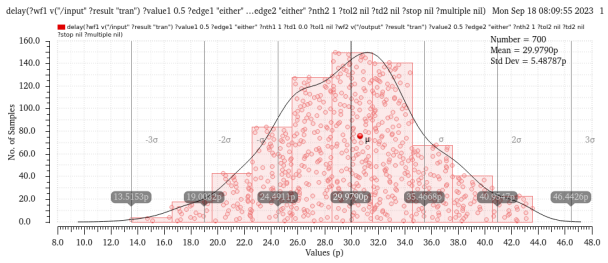

Fig. 1. Monte Carlo Delay For CMOS Inverter

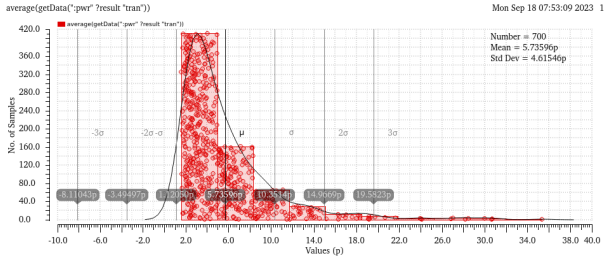

Fig. 2. Monte Carlo Leakage Power For CMOS Inverter

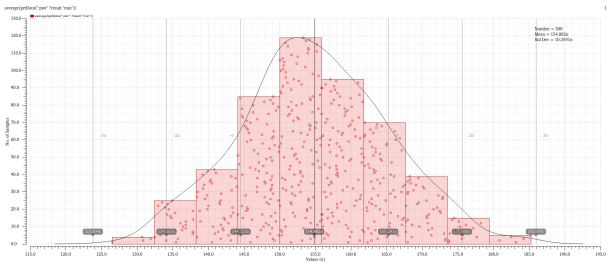

Fig. 3. Monte Carlo Dynamic Power For CMOS Inverter

F. *Layout of CMOS inverter*

The layout of CMOS Inverter is performed using Cadence Virtuoso ADEL-XL tool. ADEL-XL prepares and checks the layout for any error in the design by using DRC. The layout of the CMOS inverter is shown in figure 4.

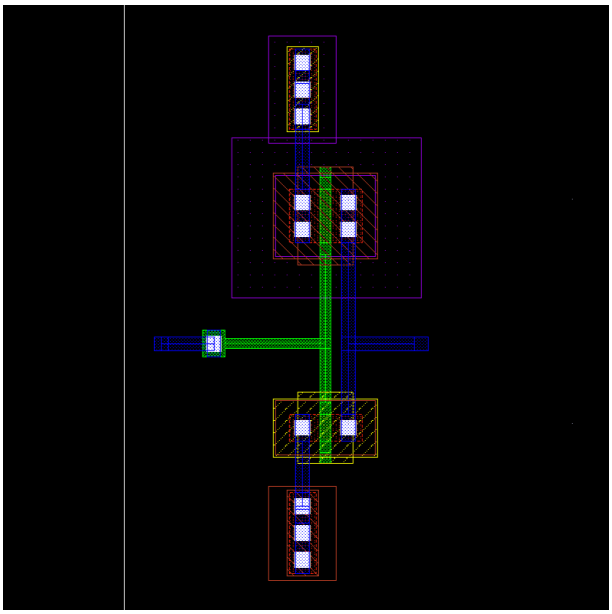

Fig. 4. CMOS layout

G. *Design rule check (DRC)*

Design Rule Checking (DRC) is an essential step in the physical design process of integrated circuits. It involves verifying that the layout of a chip adheres to the manufacturing rules and constraints. In the Cadence design environment, DRC is performed using tools such as Virtuoso and Assura.

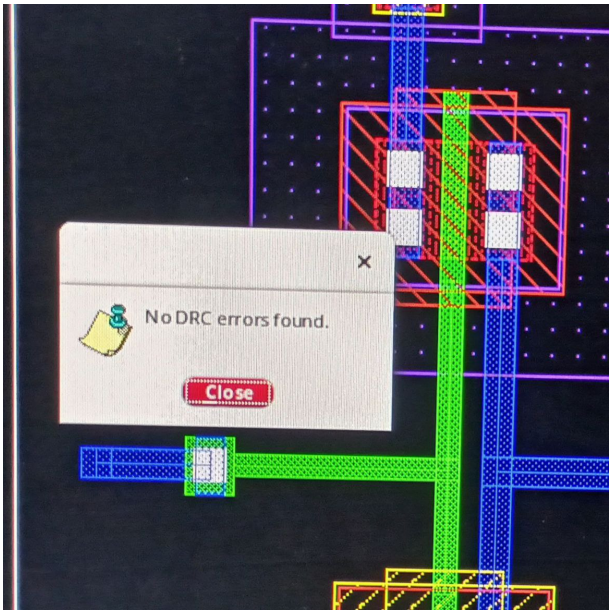

Fig. 5. DRC

We got zero DRC errors.

H. CMOS OR Gate

Implementing an OR gate using transistors at the transistor level provides more insight into the physical behavior of the circuit. Always refer to the documentation provided by your technology provider for accurate and up-to-date information specific to your chosen process node and technology.

a) CMOS OR gate schematic

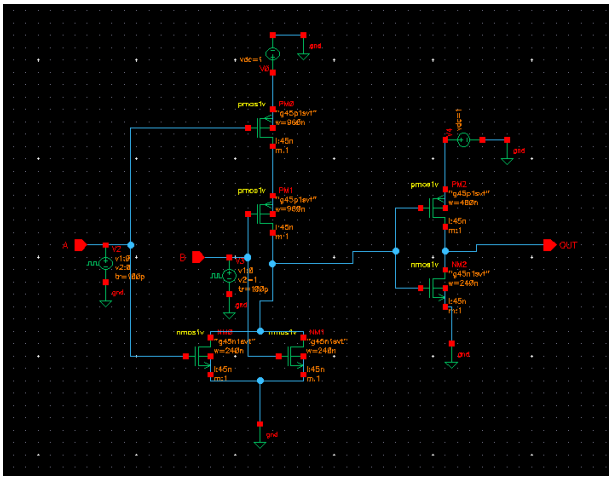

Fig. 6. OR Gate schematic

b) Transient response of CMOS OR gate.
The transient response of a CMOS inverter refers to how the output voltage of the inverter changes over time in response to a changing input signal. This analysis is crucial for understanding the dynamic behavior of the circuit, including its speed, delay, and overall performance.

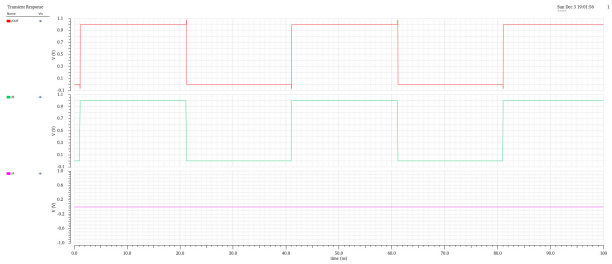

Fig. 7. OR Gate schematic

c) Dynamic Power of CMOS OR gate

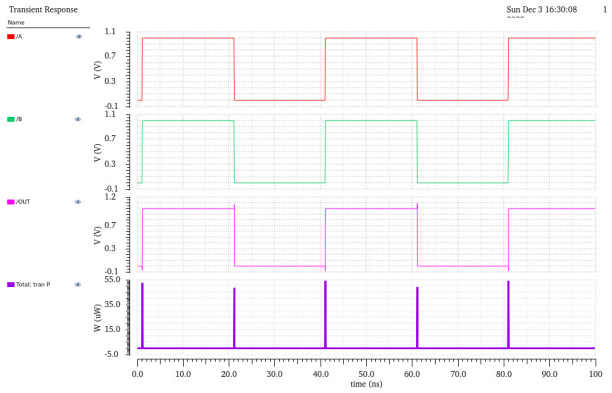

Fig. 8. Dynamic power of OR gate

$$P_{\text{dynamic}} = 0.5 \cdot C_{\text{load}} \cdot V_{\text{dd}}^2 \cdot f = 55.18\text{nW}.$$

I. Schmitt trigger

A Schmitt trigger is a type of comparator circuit with hysteresis, which means it has two different threshold levels for rising and falling input voltages. The hysteresis prevents the circuit from responding to noise and ensures a clean switching action. Inverting Schmitt triggers have an output that is the opposite (inverted) of the input signal.

a) Schmitt trigger schematic:
CMOS Schmitt trigger design with given circuit thresholds is described. The approach is based on studying the transient from one stable state to another when the trigger is in linear operation. The trigger is subdivided into two subcircuits; each of them is considered as a passive load for the other. This allows the relations governing the deviations of the circuit thresholds from their given values to be obtained. The trigger device sizes are thus determined by the threshold tolerances.

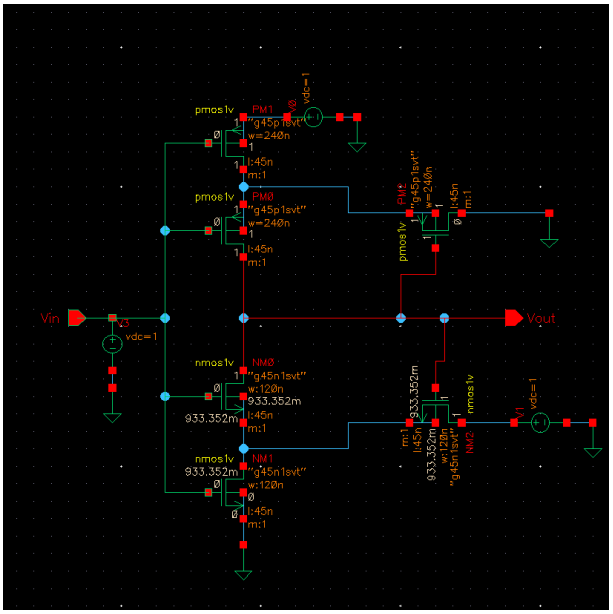

Fig. 9. Schmitt trigger Schematic

b) DC analysis of schmitt trigger.

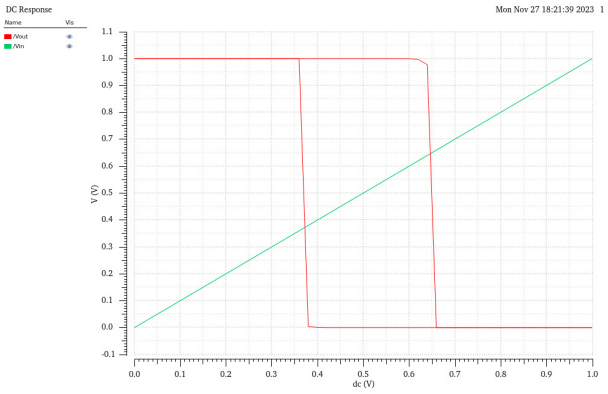

Fig. 10. Hysteresis curve of Schmitt trigger

From the graph we get Vth=609.18mV and Vtl=374.35mV Now, we will do transistor sizing and analize high threshold(Vth) , low threshold(Vlt) and hesteresis width. Now we have increased Pm1 transistor width 4 times and Nm1 by 2 times and we got vth =648.8mV and Vlt = 374.025 mV and we came on conclusion that hesteresis width has increased.

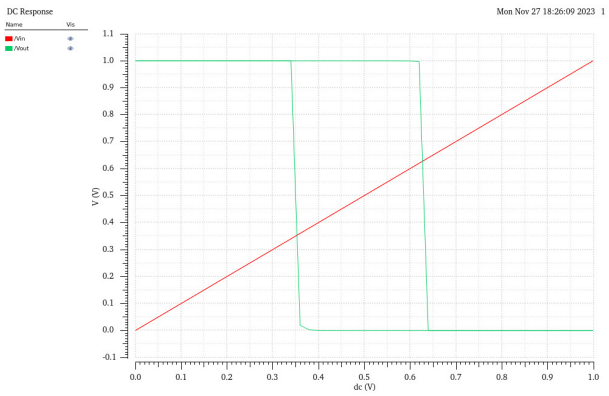

Fig. 11. increased hysteresis width

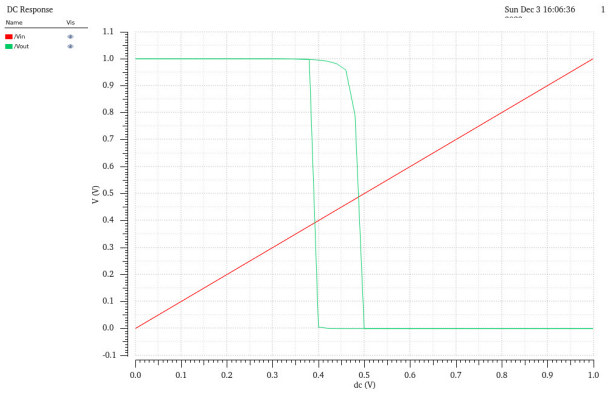

Fig. 12. increased hysteresis width

J. Conclusion

The main task of the lab was to make CMOS inverter with the help of PMOS and NMOS using 45nm technology using cadence tools.First of all we studied the basic characteristics of NMOS and PMOS and their operating region.After that we made the schematic digram of CMOS inverter and perform the following operations
1.Transient Analysis
2.Risetime,falltime and delay calculation
3.DC analysis
4.Tripping Point Vm = vdd/2 in DC analysis
5.Monte carlo
6.Temperature Variation. About MATLAB we also studied some basic operation and to use for loop ,while loop and if else statement and plotting of graph.

REFERENCES

[1] https://ee.usc.edu/tedekopp/ee209/virtuoso/setup/USCVLSI-VirtuosoTutorial.pdf
[2] CMOS DIGITAL INTEGRATED CIRCUITS BY SUNG KANG.