AN ENERGY EFFICIENT RECONFIGURABLE VITERBI DECODER ARCHITECTURE

VEDIKA.S[1] and DR.S.UMA MAHESWARI[2]

[1]M.E Research Scholar Electronics and Communication Engineering, Coimbatore Institute of Technology, Coimbatore, Email: vedikascit@gmail.com

2 Professor Electronics and Communication Engineering, Coimbatore Institute of Technology,Coimbatore Email: umamaheswari@cit.edu.in

***Corresponding Author**

VEDIKA .S

M.E Research Scholar, Electronics and Communication Engineering,
Coimbatore Institute of Technology, Coimbatore,
Email: vedikascit@gmail.com

ABSTRACT:

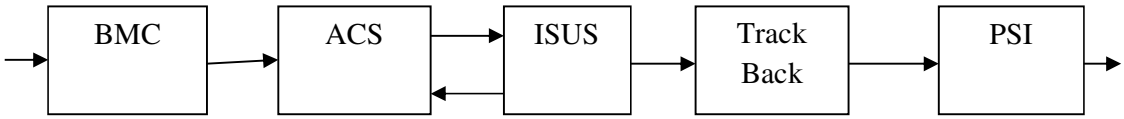
The viterbi algorithm is an efficient method for decoding convolutional codes, widely used in communication systems. This algorithm is utilized for decoding the codes used in various applications including satellite communication, cellular, and radio relay. Moreover, the algorithm has been applied to automatic speech recognition and storage devices. In this paper, efficient error detection schemes for architectures based on low-latency, low-complexity Viterbi decoders are presented. The merit of the proposed schemes is that reliability requirements, overhead tolerance, and performance degradation limits are embedded in the structures and can be adapted accordingly. We also present three variants of re-computing with encoded operands and its modifications to detect both transient and permanent faults, coupled with signature-based schemes. Further in order to make it power efficient Spurious-Power Suppression Technique (SPST) is applied. The proposed SPST separates the target designs into two parts, i.e., the most significant part and least significant part (MSP and LSP), and turns off the MSP when it does not affect the computation results to save power. Furthermore, this paper proposes an original glitch-diminishing technique to filter out useless switching power by asserting the data signals after the data transient period. The proposed fine-grained approaches can be utilized based on reliability objectives and performance/implementation metrics degradation tolerance.

Keywords: Error Detection, Speech recognition, Most Significant Part, Least Significant Part.

I. INTRODUCTION

The Viterbi algorithm is known as a maximum likelihood algorithm for convolutional code. The algorithm is based on calculating the Hamming distance for every branch in the trellis and the path that is most likely through the trellis will maximize that metric. The algorithm reduces the complexity by eliminating the least likely path at each transmission stage. The path with best metric is known as survivor, and the other entering paths are non-survivors. If the best metric is shared by two or more paths, the survivor is selected from among the best paths at random.

The selection of survivors lies at the heart of the Viterbi algorithm and ensures that the algorithm terminates with the maximum likelihood path. The algorithm terminates when all of the nodes in the trellis have been labeled and the entering survivors are determined.



Encoded i/p Sequence Decoded o/p

BASIC BUILDING BLOCKS OF VITERBI DECODER

The Branch Metric Computer, typically based on a look-up table containing the various bit metrics. The computer looks up the n-bit metrics associated with each branch and sums them to obtain the branch metric. The result is passed along to the path metric update and storage unit.

The Path Metric Updating and Storage takes the branch metric computed by the BMC and computes the partial path metrics at each mode in the trellis. The surviving path is identified and updated in storage unit. Add Compare Select Unit is being used repeatedly in the decoder. For a given code with rate 1/n and total memory M, the number of ACS required to decode a received sequence of length L is $L*2^M$.

The Information Sequence Updating and Storage (ISUS) is responsible for keep tracking the information bits associated with the surviving paths designated by the path metric updating and storage unit. Track Back Unit is responsible for tracking the survivor path after receiving the entire frame.

II. EXISTING SYSTEM

Reliable architectures have been devised to counteract natural or malicious faults, e.g., cryptographic architectures immune to faults through concurrent error detection. Error detection has been an important part of a number of hardware architectures in different domains, including various arithmetic unit sub-components.

III. PROPOSED SYSTEM

We propose error detection methods for the modified Viterbi decoder with the consideration of objectives in terms of performance metrics and reliability. Variants of re-computing with encoded operands on a number of architectures within the modified Viterbi decoder as well as signature-based approaches (including modified self-checking based on two-rail encoding) are proposed. Two approaches are followed for two types of sub-parts in the Viterbi algorithm. Our architectures also include hardware redundancy techniques through signature-based detection. Specifically for the adder components, we utilize a number of variants of self-checking based on two-rail encoding.

In proposed reliable scheme the operations are redone for different operands for detecting errors. During the first step, operands are applied normally. In the recomputed step, the operands are encoded and applied and after decoding, the correct results can be generated.

A. SIGNATURE BASED SCHEME

In order to make the ACS structure fast, parallelization of add and compare operations within the ACS itself is done (which leads to the reduction of iteration bound delay by 50%). For achieving that, the number of states is doubled and the channel response is extended by an extra bit. For a complex trellis to have P-level parallelism, there should be parallel paths for each branch. For the initial K − 1 steps, there is no compare operation, but for the remaining M − K + 1 steps, the add operation is followed by a compare operation which helps in eliminating parallelism. Add and compare operations need to be performed sequentially. For this algorithm, the order of operations from add-compare is changed to compare-add and that attributed as a carry-select-add (CSA) unit. The pre computed CSA (PCSA) is its speed-optimized type and is preferred only for large K and small M values.

We utilize signature-based prediction schemes for the CSA and PCSA units[1]. We note that even a single stuck-at fault in such units may lead to erroneous (multi-bit) result (the error may also propagate to the circuitry which lies ahead of the affected location, with the domino effect propagated system wise). Signatures (single-bit, multiple-bit, or interleaved parity, cyclic redundancy check, and the like, to name a few) are employed in our proposed scheme for all the registers. Moreover, a modified self-checking adders (MSeCA) based on dual-rail encoding are included for the adder modules.

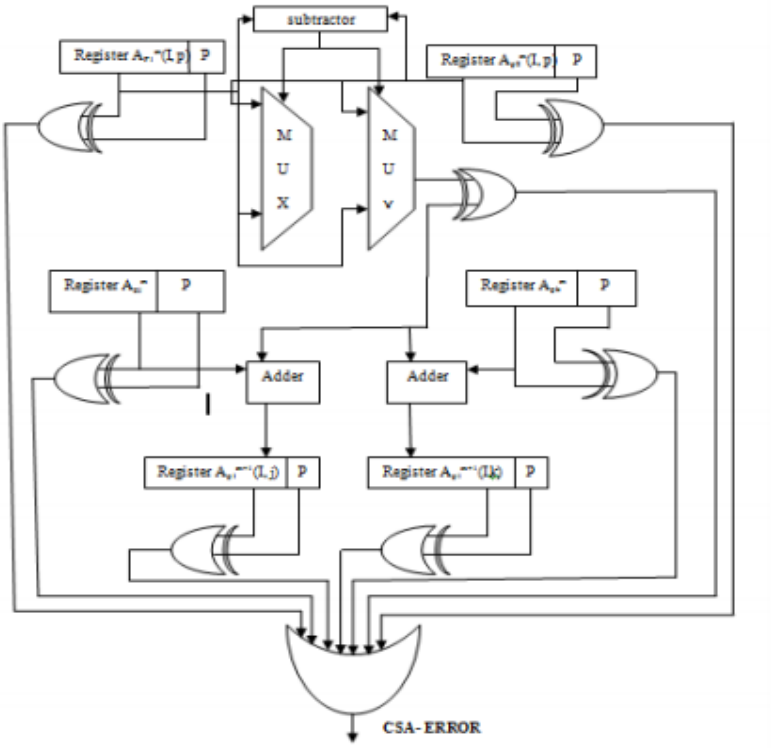


Fig 1. CSA Signature Based Error Detection Approach

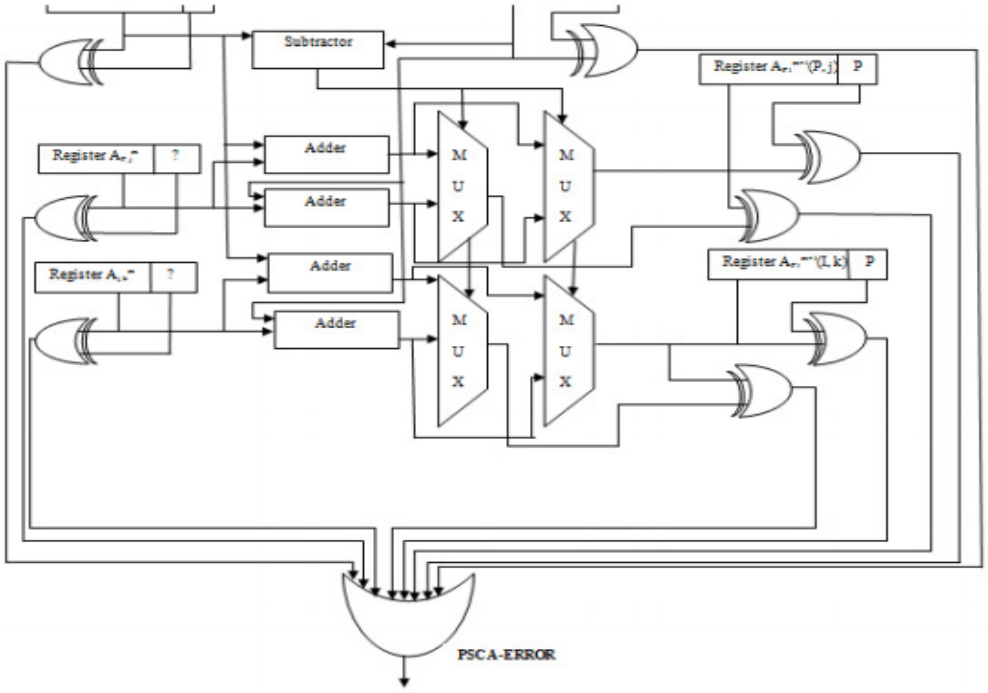


Fig 2. PCSA Signature Based Error Detection Approach

As shown in Fig 1and 2 respectively, in the CSA unit, there exists a single multiplexer whereas for the PCSA unit, the original design contains two multiplexers, for which the results of the original and the duplicated multiplexers are compared using an XOR gate whose output is connected as one of the inputs to the OR gate. The input and output registers are incorporated with additional signatures, e.g., single-bit, multiple-bit, or interleaved parity, cyclic redundancy check, to detect faults An OR gate for the units is required to derive the error indication flags. The OR gate raises the error indication flags (CSA_ Error in case of the CSA unit and PCSA_ Error in case of the PCSA unit) in case an error is detected.

The adders in both CSA and PCSA designs can also be implemented using the modified self-checking adder. In this variant, two n-bit full adders based on multiplexers are used to pre compute the sum bits with complemented values of carry-in, i.e., 0 and 1, and the original value of carry-in is used to select the actual sum bits. We employ this new adder in the architectures and evaluate its performance and efficiency.

IV. EXPERIMENTAL RESULTS

The following figure shows the simulation results of signature based schemes on both CSA and PCSA.

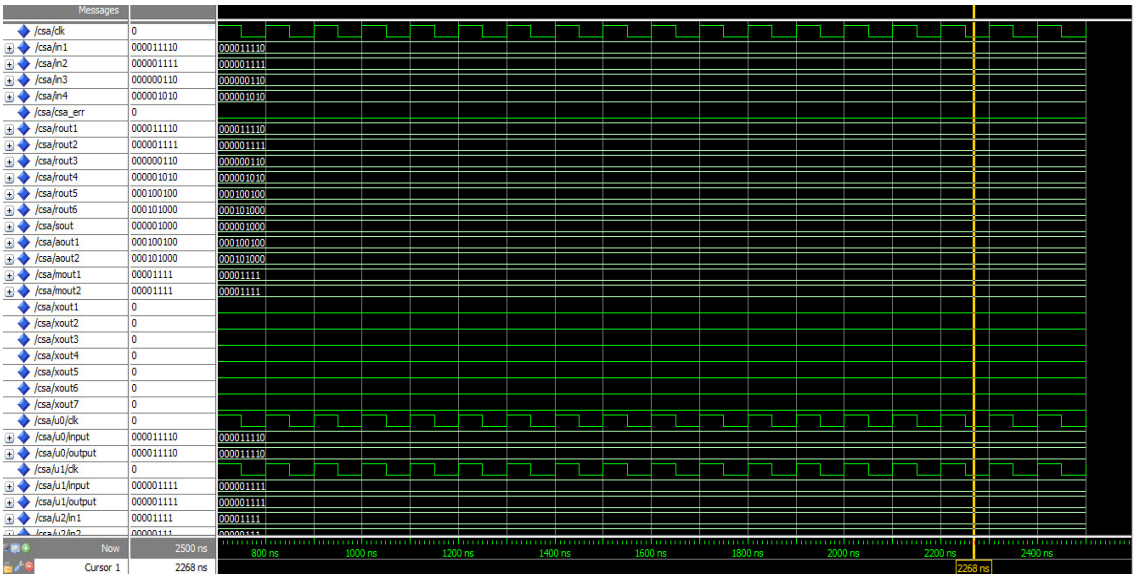


Fig 3. Simulation Result for CSA Error Detection Approach

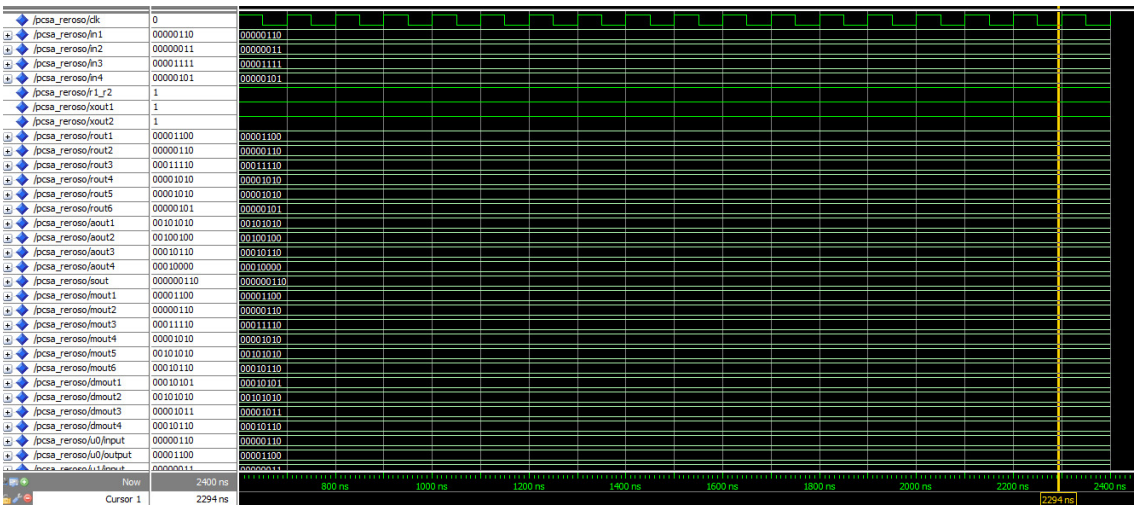


Fig 4. Simulation Result For PCSA Error Detection Approach

The fault coverage of the proposed architectures has been assessed by subjecting them to a fault model which considers permanent, transient, and single/multiple-bit stuck-at faults. The proposed error detection schemes are capable of detecting both permanent and transient faults. We inject faults at different locations and monitor the error indication flags. We have done two simulations and derived the number of detected faults for single stuck-at faults for RESO and RERO only.

COMPARISON TABLE:

ARCHITECTURE	AREA(GATE COUNT)	POWER(mW)
CSA_RCA	1179	133.75
PCSA_RCA	777	103.30
CSA_REROSO	686	486.67
PCSA_REROSO	881	515.87
CSA_SPST	726	122.65
PCSA_SPST	360	103.30
CSA_REROSO_SPST	548	472.86
PCSA_REROSO_SPST	680	444.09

V. CONCLUSION

In this paper, we have presented error detection architectures for the CSA and PCSA structures of low complexity and low latency Viterbi decoder. The proposed approaches are based on signatures and various, fine-tuned re-computing with rotated operands. The simulation results for the proposed architectures for both CSA and PCSA units show very high fault coverage (almost 100 percent) for the utilized fault model. Moreover, the FPGA implementation results show that overheads obtained are acceptable.

REFERENCES

[1]. Mehran Mozaffari Kermani and Reza Azarderakhsh, Reliable Low-Latency Viterbi Algorithm Architectures Benchmarked on ASIC and FPGA, IEEE Transactions on Circuits and Systems I: Regular Papers, October 2016:64:208-216.

[2]. R. Liu and K. Parhi, Low-latency low-complexity architectures for Viterbi decoders, IEEE Trans. Circuits Syst. I, Reg. Papers, 2009:56(10):2315-2324.

[3]. K. Parhi, An improved pipelined MSB-first add-compare select unit structure for Viterbi decoders, IEEE Trans. Circuits Syst. I, Reg. Papers,2004:51(3):504-511.

[4]. K. K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation. Hoboken, NJ, USA: Wiley, 1999.

[5]. G. Fettweis and H. Meyr, Parallel Viterbi algorithm implementation: Breaking the ACS-bottleneck, IEEE Trans.Commun, 1989:37(8):785-790.

[6]. T. Gemmeke, M. Gansen, and T. Noll, Implementation of scalable power and area efficient high-throughput Viterbi decoders, IEEE J. Solid-State Circuits,2002:37(7):941-948.

[7]. M. Mozaffari-Kermani and A. Reyhani-Masoleh, Efficient fault diagnosis schemes for reliable lightweight cryptographic ISO/IEC standard CLEFIA benchmarked on ASIC and FPGA, IEEE Trans. Ind. Electron,2013:60(12):5925-5932.

[8]. J. J. Kong and K. K. Parhi, Low-latency architectures for high throughput rate Viterbi decoders, IEEE Trans. Very Large Scale Integr. (VLSI) Syst, 2004:12(6):642-651.

[9]. D. Vasudevan, P. Lala, and J. Parkerson, Self-checking carry select adder design based on two-rail encoding, IEEE Trans. Circuits Syst. I, Reg. Papers, 2007:54(12):2696-2705.

[10]. M. Akbar and J.-A. Lee, Comments on 'self-checking carry select adder design based on two-rail encoding, IEEE Trans. Circuits Syst. I, Reg. Papers, 2014:61(7):2212-2214.

[11]. M. Nicolaidis, Carry checking/parity prediction adders and ALUs, IEEE Trans. Very Large Scale Integr. (VLSI) Syst, 2003:11(1):121-128.

[12]. C.-H. Yen and B.-F. Wu, Simple error detection methods for hardware implementation of advanced encryption standard, IEEE Trans. Comput, 2006:55(6):720-731.

[13]. M. Mozaffari-Kermani, R. Azarderakhsh, and A. Aghaie, Reliable and error detection architectures of Pomaranch for false-alarm-sensitive cryptographic applications, IEEE Trans. Very Large Scale Integr. (VLSI) Syst, 2015:23(12):2804-2812.

[14]. M. Mozaffari Kermani and R. Azarderakhsh, Reliable hash trees for post-quantum stateless cryptographic hash-based signatures, in Proc. IEEE Int. Symp. Defect Fault Tolerance VLSI Syst. (DFT), Oct. 2015:103–108.

[15]. M. Mozaffari-Kermani and A. Reyhani-Masoleh, Concurrent structure independent fault detection schemes for the advanced encryption standard, IEEE Trans. Comput., 2010:59(5):608-622.