# EE210: Analog Electronics - Quiz 4

| NAME (in capital) | Roll No |
|---|---|
| | |

Time: 15 minutes

*1) :* For the transistor in the following circuit $\mu_n C_{ox} = 200\mu A/V^2$, $V_{tn} = 1V$, Also, $V_{DD} = 5V$.

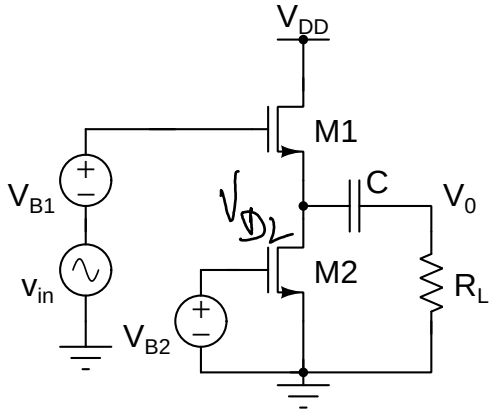



Fig. 1. Problem 1

*a) :* Assume $W/L = 10$ for both transistors. Find the minimum $V_{B1}$ and $V_{B2}$ such that a quiescent current of 1 mA flows through stack while keeping both transistors in saturation. **[3]**

$$V_{B2} = V_{th} + \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}} = 2V$$

$$V_{D2(min)}\Big|_{\text{sat for } M_2} = 1V$$

$$\therefore \quad V_{B1(min)} = V_{D2(min)} + V_{GS1}$$

$$= 3V$$

*b) :* What changes in the $W/L$ would you do to ensure M2 is in saturation and away from the edge of linear region by 500 mV while maintaining 1 mA of quiescent current? **[4]**

$V_{D_2}$ is set by M1.

$\therefore V_{D_2} = V_{B_1} - V_{GS_1}$

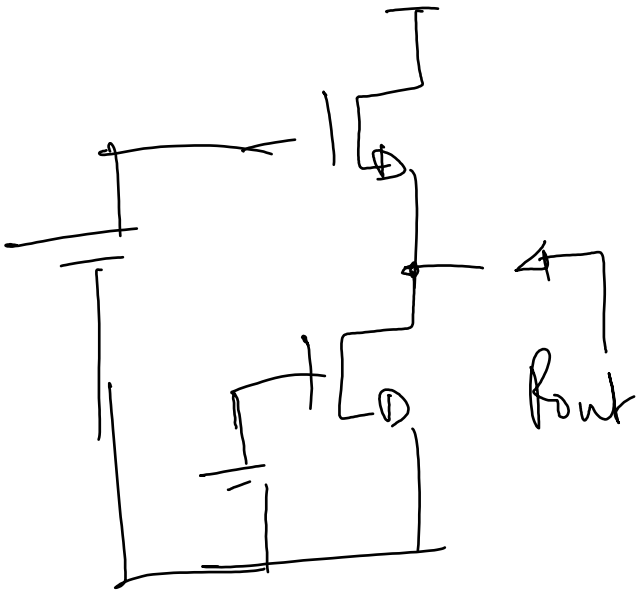
$= V_{B_1} - V_{th} - \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}}$

$V_{OV}$

For $\left(W/L\right) = 10$, $V_{OV} = 1V$

For $V_{OV} = 0.3V$ $\left(W/L\right) = 40$.

*c) :* What is the constraint on $R_L$ to ensure that $v_0$ is independent of $R_L$? **[3]**




$R_{out} = 1/g_m$

$\therefore$ Constraint :

$R_L >> 1/g_m$