
EE210: ANALOG ELECTRONICS

END-SEM
APRIL 25, 2024

For all transistors assume the following unless otherwise mentioned.
 $\mu_n C_{ox} = 200 \mu A/V^2$, $\mu_p C_{ox} = 100 \mu A/V^2$, $V_{tn} = 1V$ $|V_{tp}| = 1V$, $\lambda_n = \lambda_p = 0.1 V^{-1}$

Write all your answers in the spaces provided. Do your calculations in this sheet itself. All questions have the figures associated with them. The figures have also been provided separately at the end of the sheet. You may tear it out if you wish to. Extra sheet will be provided if you need it for rough work, but it will **NOT** be considered for evaluation. The page numbers are marked 1–20 in this question paper. Verify it before you start answering.

There are **five** places where you need to write your name and roll-number. *Fill them up before you start answering, and sign on top of each page. Each unfilled case will be penalized by 1 mark.*

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1) : Consider the circuit in Fig. 1(b) which contains a three terminal non-linear element (shown in Fig. 1(a)). The I-V characteristics of the element is defined as the following

$$I_B = 0 \text{ and } I_C = I_E = I_s \exp(\alpha V_{BE}) \text{ for } V_{BE} \geq 0$$

$$I_B = I_C = I_E = 0 \text{ otherwise.}$$

Assume $I_s = 0.1 \text{ nA}$, $\alpha = 0.05 \text{ mV}^{-1}$, $V_{CC} = 10 \text{ V}$. Also assume that $C1$ and $C2$ are large enough to be treated as a short circuit at non-zero signal frequencies wherever applicable.

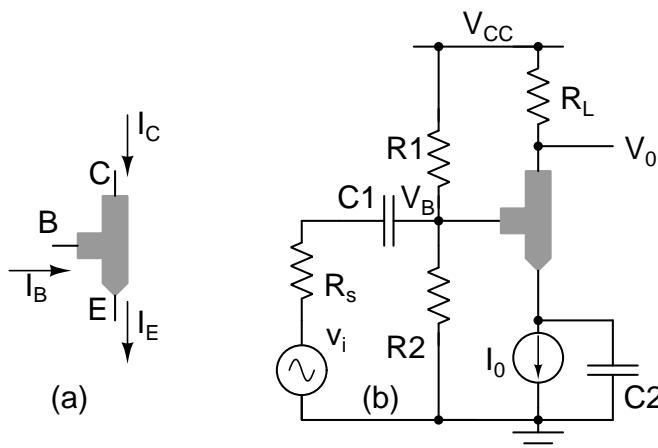


Fig. 1. Question 1

a) : Sketch the three-terminal small signal (y-parameter) model of the non-linear element in Fig. 1(a) for $V_{BE} > 0$ and find all four two-port y-parameters. Assume the input terminals to be B and E and the output terminals to be C and E for the two-port. Assume the $I_C = 1 \text{ mA}$ for your calculations. [4]

$y_{11} =$	$y_{12} =$	$y_{21} =$	$y_{22} =$
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Handwritten solution for the y-parameter model:

Sketch of the three-terminal non-linear element (a): A diode-like symbol with terminals B (base), E (emitter), and C (collector). A current I_B enters terminal B, and currents I_C and I_E exit terminal C. A note indicates $I_C = 1 \text{ mA}$.

Y-parameter equations derived from the sketch:

$$I_B = 0 \quad \therefore y_{11} = 0 \quad y_{12} = 0$$

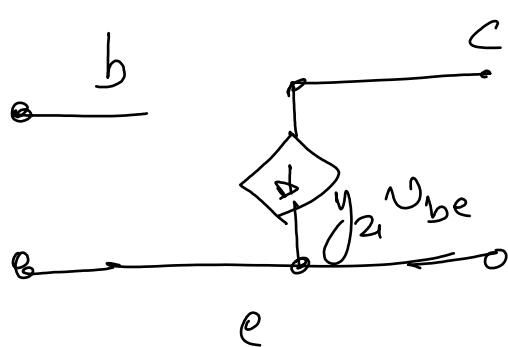
$$I_C = I_s e^{\alpha V_{BE}} \quad y_{21} = \frac{\partial I_C}{\partial V_{BE}} = \alpha I_s e^{\alpha V_{BE}}$$

$$y_{22} = \frac{\partial I_C}{\partial V_{CE}} = \alpha I_s e^{\alpha V_{BE}} \cdot \frac{1}{V_{CE} - V_{BE}}$$

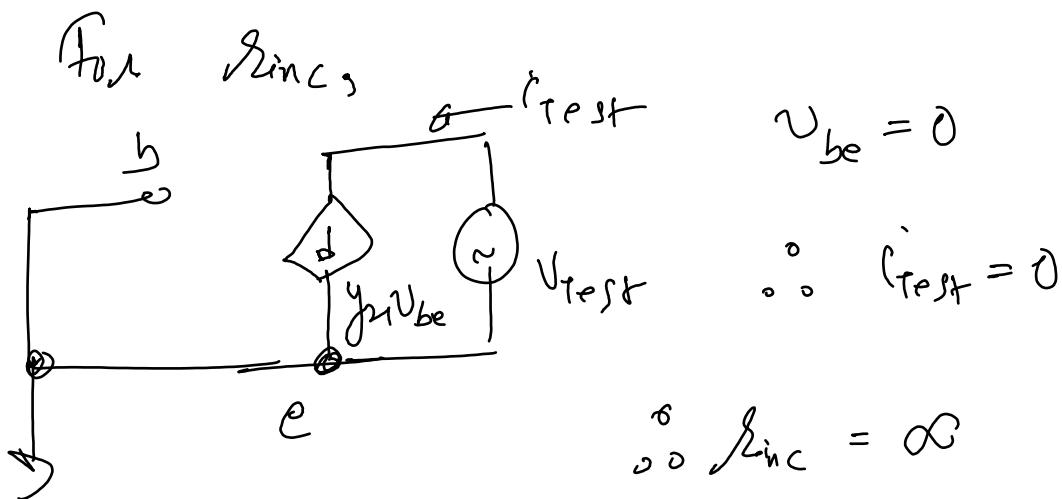
$$= \frac{0.05 \times 10^{-9} \times 10^3}{mV} \times 1 \text{ mA} = 50 \text{ mS}$$

contd..

b) : Find the small-signal resistances "looking into" each of the three terminals (B, C and E) for the condition of the previous part. Assume that all terminals are biased using ideal voltage sources. Assume the quiescent current to be 1 mA. You must sketch the small-signal model with test voltage (or current) sources for each case. [4]

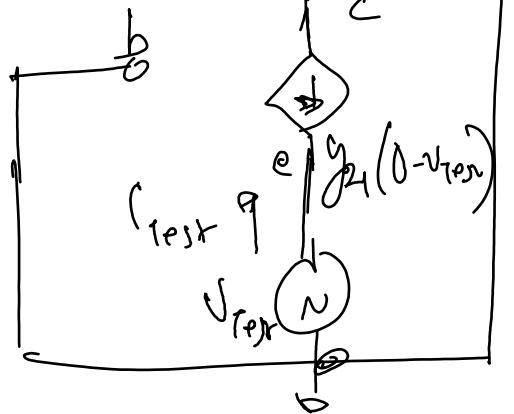


looking into terminal b.
open chkt.
 $\therefore R_{in\ b} = \infty$



contd..

Ckt. for line



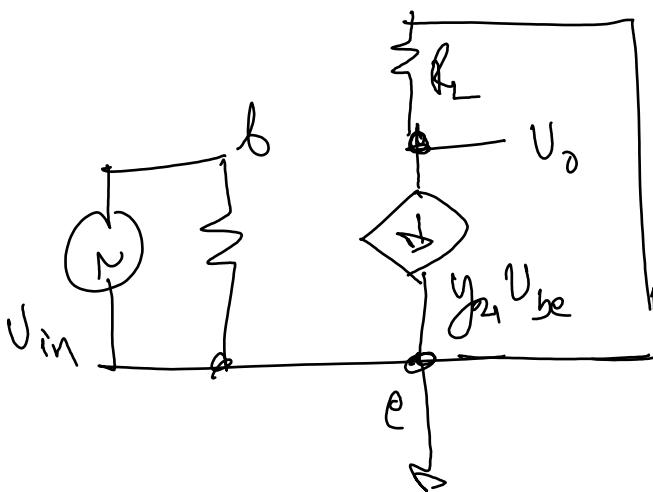
$$r_{\text{proj}} = y_{21} v_{\text{test}}$$

$$\therefore R_{\text{line}} = \frac{1}{y_{21}} = 20 \Omega$$

c) : $R_1 = R_2 = 10 k\Omega$. Find v_0/v_i in Fig. 1(b), if $R_L = 2 k\Omega$. Assume $R_s = 0$.

[3]

Ans:



$$v_{be} = v_{in}$$

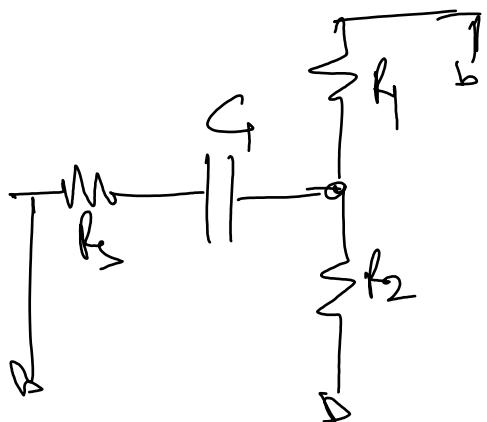
$$\therefore v_o = -y_{21} v_{in} R_L$$

$$\Rightarrow \frac{v_o}{v_{in}} = -y_{21} R_L \\ = -100$$

..contd..

d) : Find the time-constant associated with C_1 . Assume C_2 is large enough to be treated as a short circuit for this part. Assume $R_s = 1 k\Omega$ [2]

Ans:



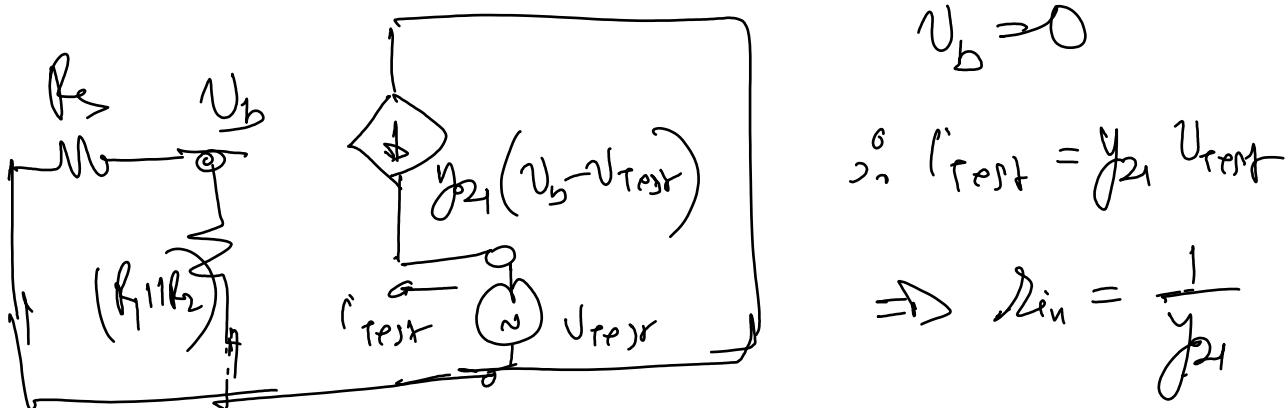
$$Z = G \left(R_f + R_1 // R_2 \right)$$

contd..

e) : Find the time-constant associated with C_2 . Assume C_1 is large enough to be treated as a short circuit for this part. [2]

Ans:

Find the incremental resistance across C_2 .



$$U_b = 0$$

$$\therefore I_{\text{rest}} = y_2 U_{\text{rest}}$$

$$\Rightarrow R_{\text{in}} = \frac{1}{y_2}$$

$$I_{\text{in}} Z_2 = \frac{C_2}{y_2}$$

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2) : Fig. 2(a) shows a differential amplifier and its incremental model in (b). Assume all transistors are in saturation and neglect channel length modulation. The diffamp has been excited with an incremental antisymmetric input. The aspect ratio (W/L) of each transistor is marked in the figure. Assume $\sqrt{2\mu_n C_{ox} I_0} = \sqrt{2\mu_p C_{ox} I_0} = g_m$ for $W/L = 1$.

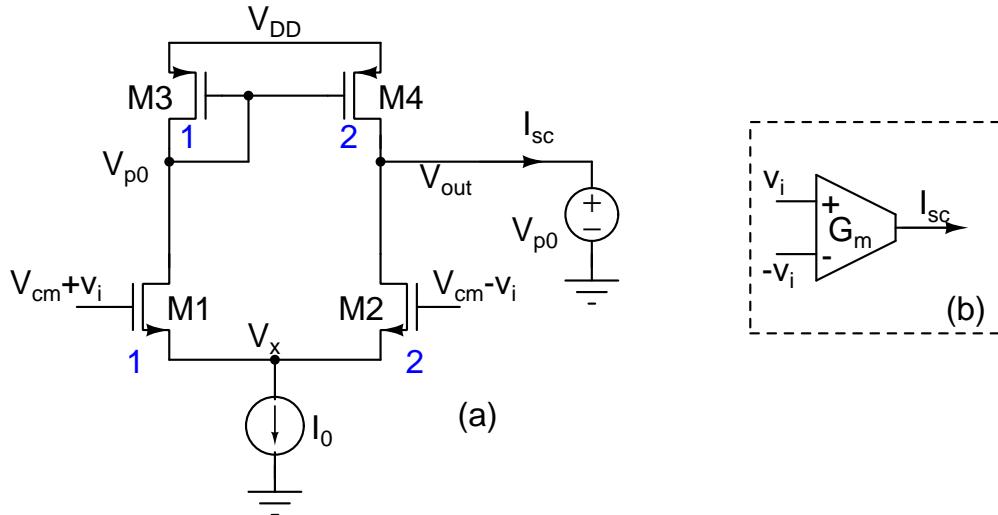


Fig. 2. Question -2

a) : Find the quiescent currents through M_1 and M_2 transistors in terms of I_0 . [2]

Ans:

$$\therefore V_{GS1} = V_{GS2} \text{ and } \left(\frac{W}{L}\right)_2 = 2 \left(\frac{W}{L}\right)_1$$

$$\therefore I_{DS2} = 2 I_{DS1}$$

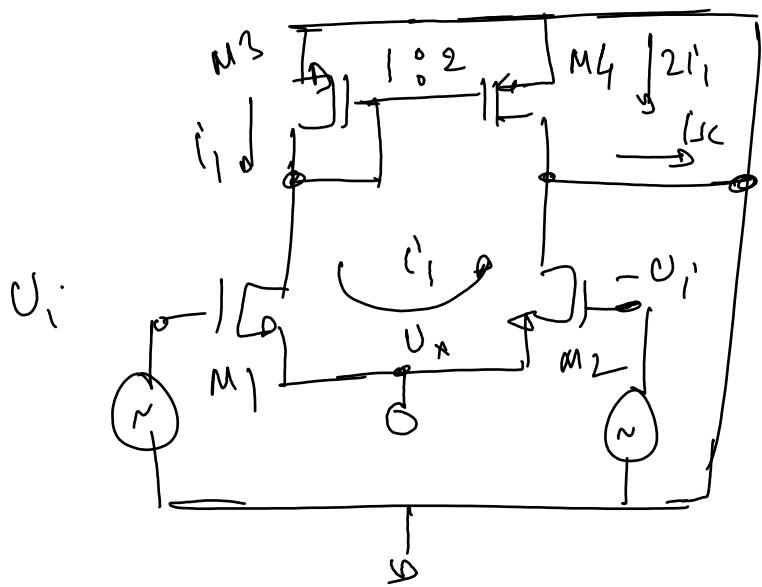
$$\therefore I_{DS1} = \frac{I_0}{3} \quad \text{and} \quad I_{DS2} = \frac{2 I_0}{3}$$

b) : Find G_m in terms of g_m so that figures (a) and (b) are incrementally identical. [3]

Ans:

From Fig (b); $i_{SC} = G_m + (2v_r)$

From Fig (a)



$$\bar{Z}_M = \sqrt{2 \mu_n C_{ox} \frac{W}{L} \left(2/\beta\right)}$$

$$= \bar{Z}/\sqrt{3}$$

$$\bar{Z}_{M2} = \frac{2\bar{Z}}{\sqrt{3}}$$

$$KCL @ U_x: U_x = \frac{\bar{Z}_M U_1 + \bar{Z}_{M2} (-U_1)}{\bar{Z}_M + \bar{Z}_{M2}}$$

$$= \left(\frac{\bar{Z}_M - \bar{Z}_{M2}}{\bar{Z}_M + \bar{Z}_{M2}} \right) U_1$$

$$\therefore i_1 = \bar{Z}_M (U_1 - U_x) = \frac{2\bar{Z}_M \bar{Z}_{M2}}{\bar{Z}_M + \bar{Z}_{M2}} U_1$$

$$i_{SDM} = 2i_1 \quad (\text{Due to mirroring by } 2)$$

$$\therefore i_{SC} = i_1 + 2i_1 = \frac{6\bar{Z}_M \bar{Z}_{M2}}{\bar{Z}_M + \bar{Z}_{M2}} U_1$$

$$\therefore G_m = \frac{i_{SC}}{2U_1} = \frac{3\bar{Z}_M \bar{Z}_{M2}}{\bar{Z}_M + \bar{Z}_{M2}}$$

$$= \frac{3 \times \frac{\bar{Z}_M}{\sqrt{3}} \times \frac{2\bar{Z}_M}{\sqrt{3}}}{\frac{\bar{Z}_M}{\sqrt{3}}} = \frac{2\bar{Z}_M}{\sqrt{3}}$$

c) : What is the swing at V_x when $v_i = V_p \sin(\omega t)$ in Fig. 2?

[3]

Ans:

$$\begin{aligned} V_x &= \left(\frac{\bar{x}_1 - \bar{x}_2}{\bar{x}_1 + \bar{x}_2} \right) V_p \sin(\omega t) \\ &= -\frac{1}{3} V_p \sin(\omega t) \end{aligned}$$

d) : Now consider channel length modulation for $M3$ and $M4$. What must the output quiescent voltage V_{out} be to ensure the current through $M4$ is exactly twice of that of $M3$. Express your answers in terms of I_0 , V_{DD} and g_m . [3]

$$I_{SD4} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_4 V_{DD}^2 (1 + \lambda V_{SD4})$$

$$I_{SD3} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_3 V_{DD}^2 (1 + \lambda V_{SD3})$$

$$\therefore \left(\frac{W}{L}\right)_4 = 2 \left(\frac{W}{L}\right)_3 \quad \therefore \text{To ensure } I_{SD4} = 2 I_{SD3}$$

V_{SD4} must be equal to V_{SD3} .

$$V_{SD3} = V_{SG3} \approx V_{TP} + \sqrt{\frac{2(20/3)}{\mu_p C_{ox} \left(\frac{W}{L}\right)}}$$

$$\therefore V_{G3} = V_{DD} - V_{TP} - \sqrt{\frac{2(20/3)}{\mu_p C_{ox} \left(\frac{W}{L}\right)}}$$

$$\therefore V_{P0} = V_{G3} = V_{DD} - V_{TP} - \sqrt{\frac{2^2 10^2 / 3}{2 \mu_p C_{ox} (W/L)}}$$

$$= V_{DD} - V_{TP} - \frac{2 \cdot 10}{\sqrt{3} g_m}$$

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3) : $(W/L)_{M1} = 10$, $(W/L)_{M2} = 20$, $V_{THN} = 1\text{V}$, $|V_{THP}| = 1\text{V}$, $R = 1\text{k}\Omega$. Ignore channel length modulation.

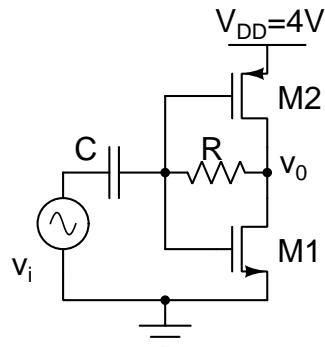


Fig. 3. Question -3

a) : Find quiescent V_0 .

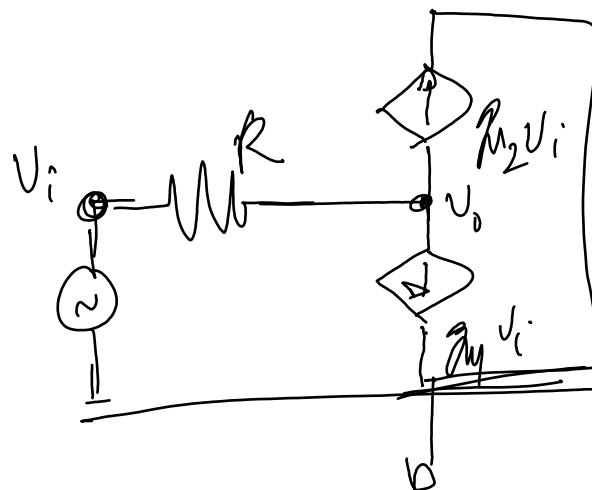
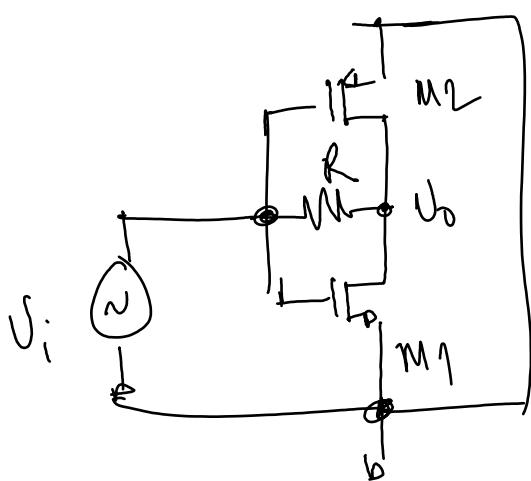
[3]

Ans:

$$\begin{aligned}
 & \text{Circuit diagram: } V_{DD} \text{ is at the top, ground at the bottom. M2 is a PMOS device with its drain connected to } V_{DD} \text{ and its source connected to the drain of M1. M1 is an NMOS device with its drain connected to the source of M2 and its source grounded. The input voltage } v_i \text{ is applied to the gate of M1 and to node A. Node A is connected to the drain of M1 and the source of M2 through a resistor } R. \text{ The gate of M2 is connected to node A and to the drain of M1. The source of M2 is connected to ground. A capacitor } C \text{ is connected between node A and ground.} \\
 & \text{Quiescent conditions: } I_{SD2} = I_{DS1}, \quad V_{G2} = V_o \quad (\because I_R = 0) \\
 & \Rightarrow \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_2 \left(V_{DD} - V_b - |V_{thp}| \right)^2 \\
 & = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_1 \left(V_{G2} - |V_{thn}| \right)^2 \\
 & \Rightarrow 4 - V_o - 1 = V_o - 1 \quad \left(\begin{array}{l} \text{The other solution} \\ \text{is invalid.} \end{array} \right) \\
 & \Rightarrow V_o = 2\sqrt{V_{DD} - |V_{thp}|} = 2\sqrt{4 - 1} = 2\sqrt{3} \text{ V}
 \end{aligned}$$

b) : Ignore channel length modulation and assume the capacitor is shorted at the signal frequencies.
Find the incremental gain v_0/v_i . [4]

Ans:



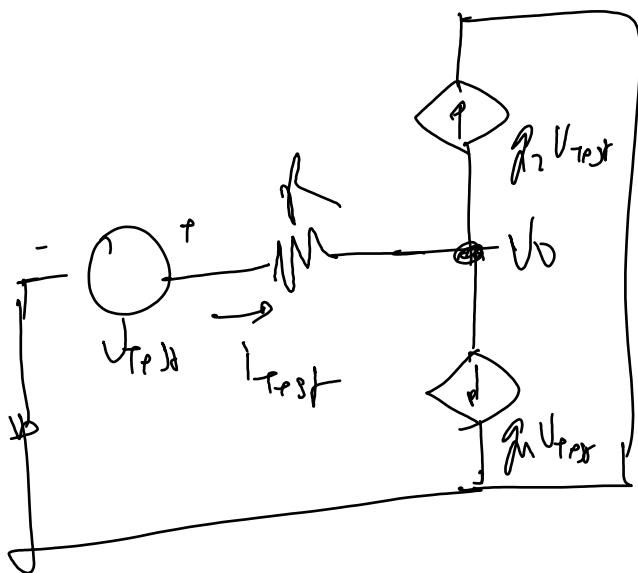
$$\begin{aligned} \text{KCL } @ \quad U_o \Rightarrow & \quad \frac{(U_i - U_o)}{R} = (\beta_M + \beta_L) U_i \\ \Rightarrow \quad U_o &= U_i \left(1 - (\beta_M + \beta_L) R \right) \\ \Rightarrow \quad \frac{U_o}{U_i} &= 1 - (\beta_M + \beta_L) R \end{aligned}$$

$$\beta_M = \mu_n C_{ox} \left(\frac{W}{L} \right)_1 \left(V_o - V_{th} \right)^2 = 2 \text{ mS}$$

$$\beta_L = \mu_p C_{ox} \left(\frac{W}{L} \right)_2 \left(V_{DD} - V_o - |V_{th}| \right) = 2 \text{ mS.}$$

$$\therefore \quad \frac{U_o}{U_i} = -3$$

c) : If $v_i = V_p \sin(\omega_0 t)$, where $\omega_0 = 100 \text{ Mrad/s}$ find the constraint on C for it to act as short circuit at ω_0 . [4]



ckt to find the Req
across C .

$\text{KCL} @ V_0$

$$R_{T\text{p},0} = (R_1 + R_2) V_{\text{test}}$$

$$\Rightarrow \frac{V_{\text{test}}}{R_{T\text{p},0}} = \frac{1}{R_1 + R_2} = R_{\text{eq}} \\ = 250 \Omega$$

$$\therefore Z = R_{\text{eq}} C$$

for short ckt @ ω_0

$$Z \gg \frac{1}{\omega_0}$$

$$\Rightarrow C \gg \frac{1}{100 \text{ Mrad/s} \times 250 \Omega} = 40 \mu\text{F}$$

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4) : Assume the loop in the Fig. 4 is in negative feedback. G_m is the figure refer to voltage controlled current source. $G_{m1} = 1 mS$, $G_{m2} = 1 mS$, $R2 = 10 k\Omega$, $C1 = 1 pF$.

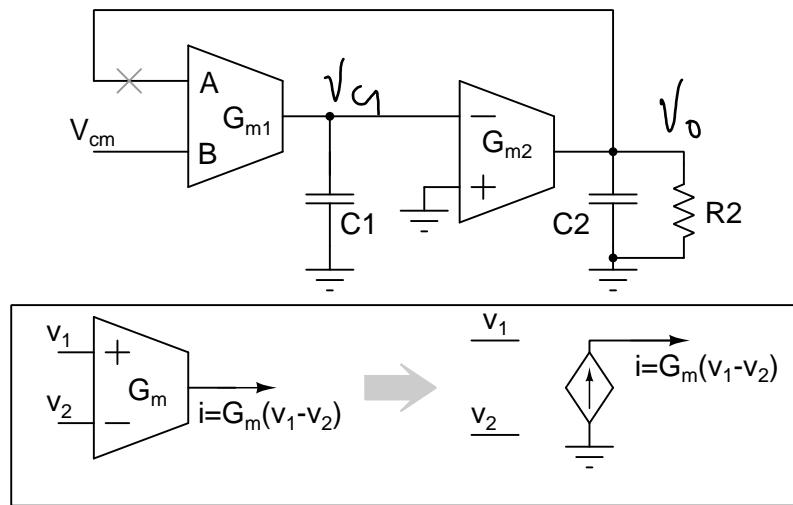


Fig. 4. Question -4

a) : Find the sign of A (with justification) to ensure that the loop is in negative feedback. [2]

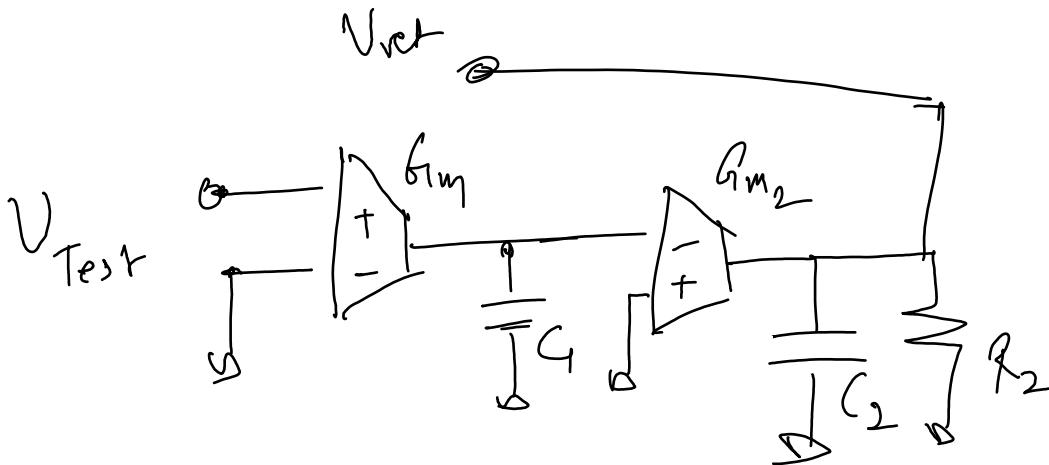
Ans:

Assume A is +ve.

$A \uparrow, V_{C1} \uparrow, V_o \downarrow$
 $\circ \quad -ve \quad if \quad A \uparrow +ve$

b) : Find the unity gain bandwidth of the loop if the phase margin of the loop is 60° . Use Bode approximation for to arrive at your answer. Break the loop at \times and apply a test voltage at the terminal A to evaluate loop gain. [7]

Ans:



$$V_{Vct} = - \frac{G_{m1}}{sG} V_{Test} \times \frac{G_{m2}}{(sC_2 + G_2)}$$

$$\Rightarrow L(s) = \frac{G_{m1} G_{m2} R_2}{sG (1 + s C_2 R_2)}$$

2nd order system.

For $PM > 45^\circ$, UGB must be before

the second pole,

Using Bode approx. $L(s)$ | $= \frac{G_{m1} G_{m2} R_2}{sG}$
for $\omega < \frac{1}{C_2 R_2}$

$$\therefore UGB = \frac{G_{m1} G_{m2} R_2}{G} = 1 \text{ rad/s.}$$

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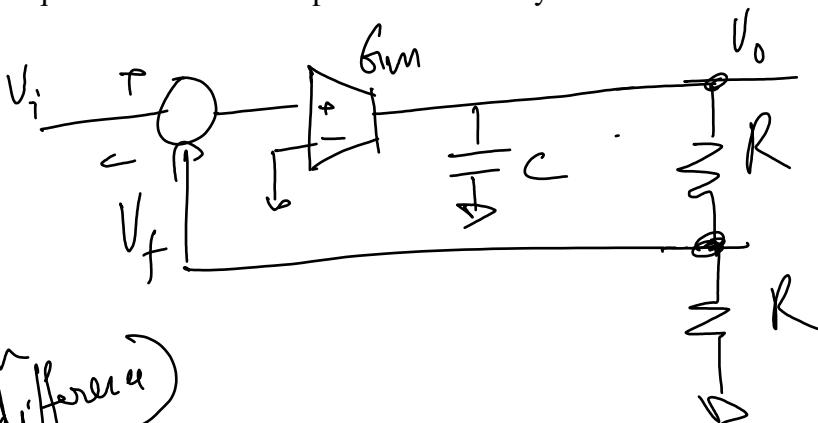
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5) : A first order negative feedback loop using one voltage controlled current source, one capacitor and resistor(s) is found to have the following characteristics.

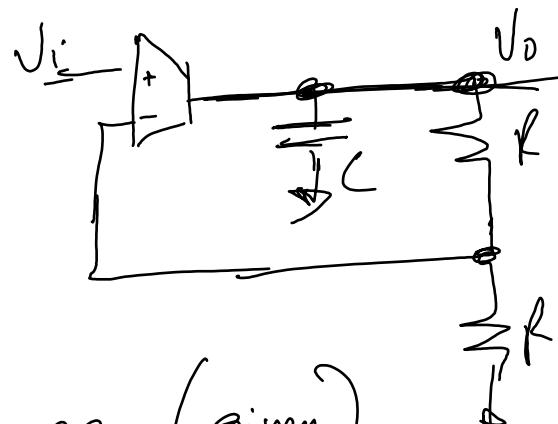
- An incremental step of +10 mV at the input causes the output voltage to settle with an increment of +19.9 mV.
- When a sinusoidal input of 10 Mrad/sec is applied at the input, a phase lag of 45° is observed at the output.

a) : Sketch the circuit in question with all the parameters clearly marked. [4]

Block diagram :



(Necessary to understand that V_i has to be compared with V_f and amplify the difference)



$$\left| \frac{V_o}{V_i} \right| @ DC = \frac{19.9}{10} = 1.99 \quad (\text{given})$$

$$\text{and } \omega_u (of L(s)) = 10 \text{ Mrad/s.} \quad (\because \text{UCR of } L(s) = -3dB \text{ of } \frac{V_o(s)}{V_i(s)})$$

$$\boxed{\omega_u = \frac{G_m}{2C} = 10M}$$

$$\text{and } \angle of \frac{V_o(s)}{V_i(s)} = -45^\circ @ -3dB$$

$$\left| \frac{V_o}{V_i} \right| @ DC = \frac{2 \times 1}{1 + \frac{1}{L(s)}} = \frac{2}{1 + \left(\frac{1}{G_m \times 2R} \right)} = 1.99 \Rightarrow \boxed{G_m \times R \approx 100}$$

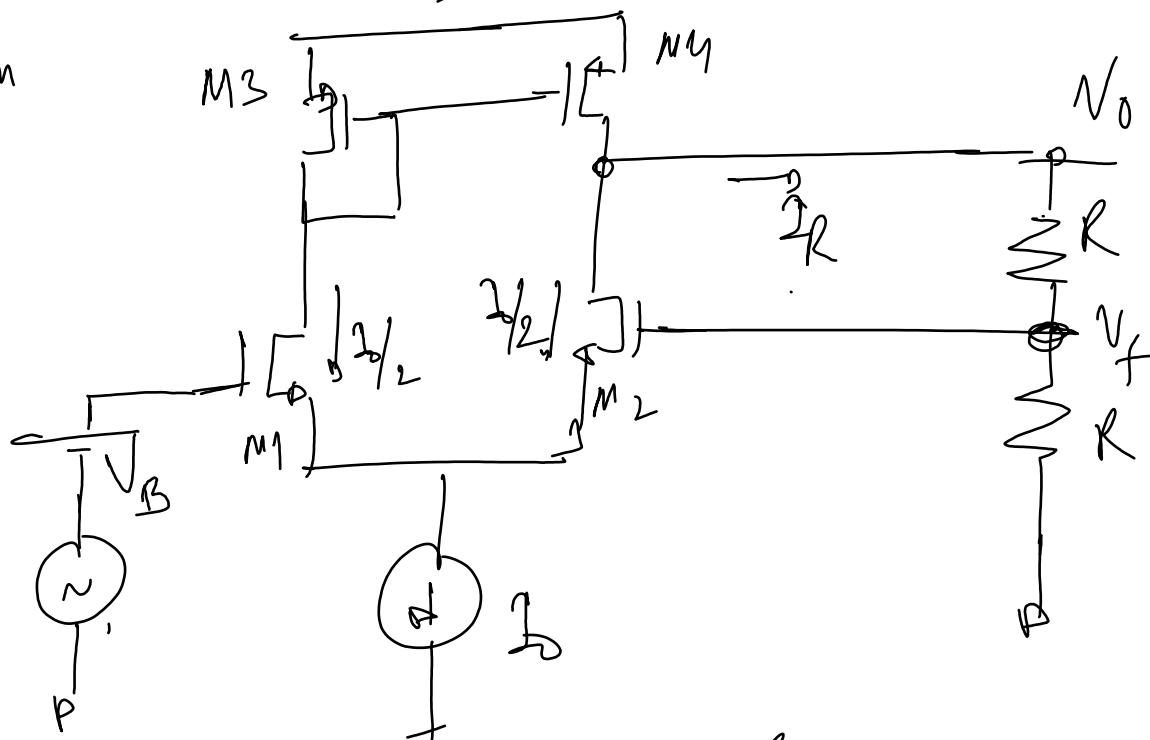
b) : Design the VCCS with a transistor level circuit using MOSFETs so that it can be used for the aforementioned application. Note, all the sizes of the transistors must be marked. You can use ideal DC current and DC voltage sources wherever necessary. Use the parameters marked in the table at the beginning of the question paper. Ignore channel length modulation of all transistors. [6]

Multiple solutions possible with $G_m R = 100$ and $\frac{G_m}{C} = 20 \text{ nA/s}$.

I choose $G_m = 1 \text{ mS}$ $R = 100 \text{ k}\Omega$

$$\therefore C = \frac{1 \text{ mS}}{20 \text{ nA/s}} = 50 \text{ pF}$$

For G_m



To ensure symmetric current (not necessary but cases design constraint) through M_1, M_2, M_3, M_4 ,

ensure $2/I_L \gg 2R$

$$G_m = 2/I_L$$

We choose $I_L = 2 \text{ mA}$

$$\therefore I_m S = \sqrt{2 \times 2 \text{ mA} \times (\omega/4)}, 1 \text{ mS}$$

$$\Rightarrow (\omega/L)_1 = 2.5$$

contd..

Let . $(\omega_L)_{1-4} = 5$

$$V_{AS1} = 1 + \sqrt{\frac{2 + 1mA}{0.2 \times 2.5m}} = 3V$$

\therefore Choose $V_B > 3V$. Let $V_B = 3.5V$.
 (not necessary with ideal I_D)

$$V_D \approx 2V_B = 7V \quad \therefore I_F = \frac{7V}{200k\Omega} \ll \text{Ind.}$$

To keep M_N in sat.

$$V_{DD} > V_0 + (V_{OV})_{M_N}$$

$$\text{Choose } V_{DD} = 10V.$$

c) : When applied with a step input, with what time-constant does the final output settle? [2]

$$T = \frac{1}{\omega_n} = \frac{1}{10Mrad/s} = 100ns.$$

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Figures for rough use:

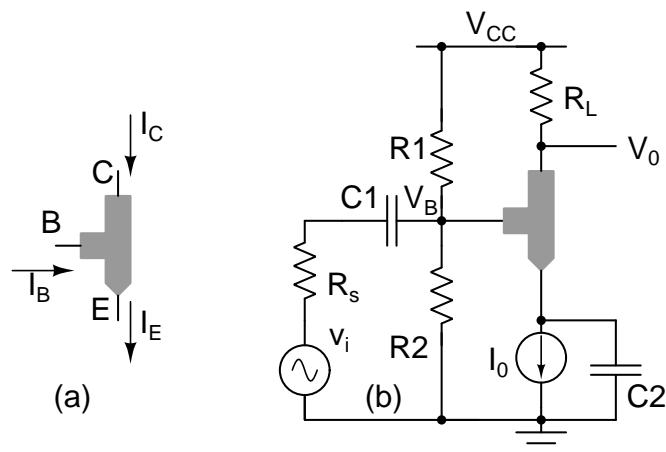


Fig. 5. Question -1

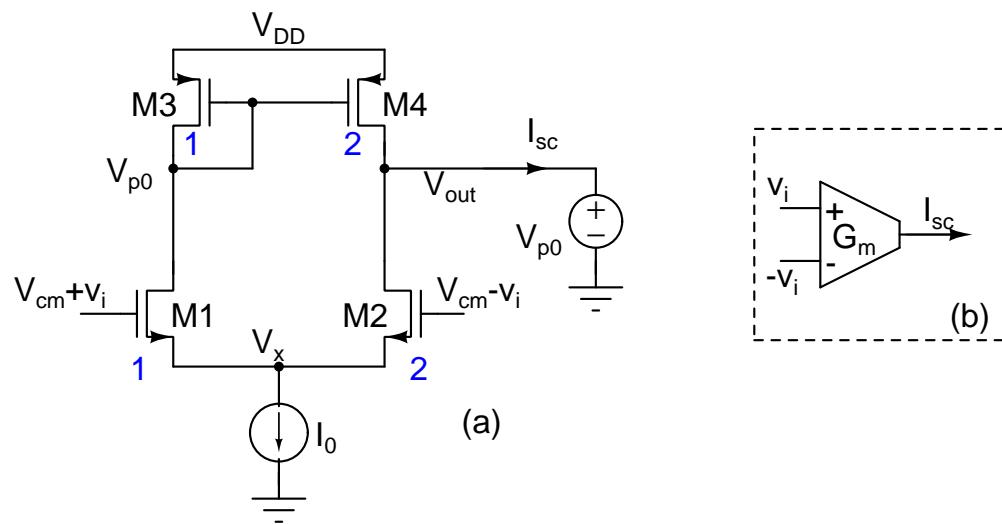


Fig. 6. Question -2

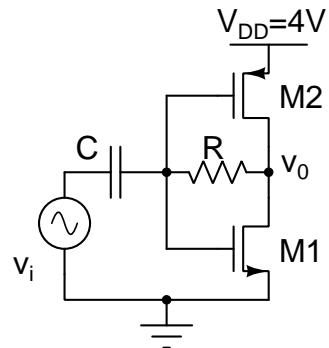


Fig. 7. Question -3

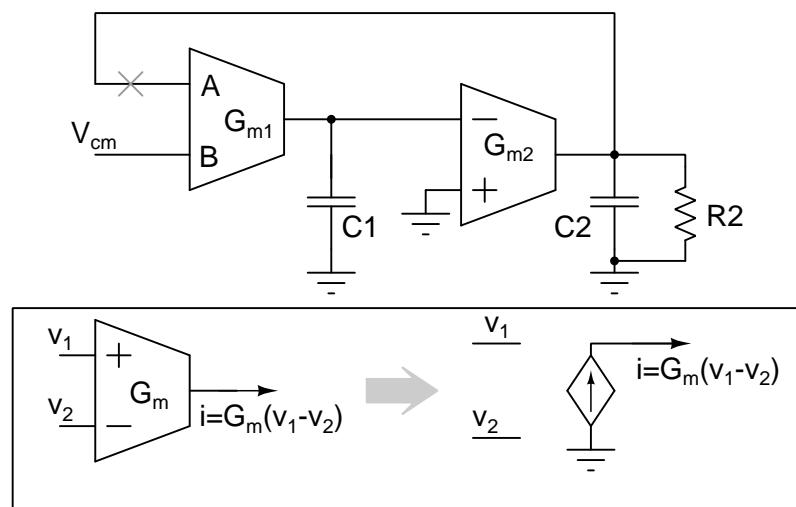


Fig. 8. Question -4