
EE210: ANALOG ELECTRONICS

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Write all your answers in the spaces provided. Do your calculations in this sheet itself. Extra sheet will be provided if you need it for rough work, but it will **NOT** be considered for evaluation. The page numbers are marked 1–11 in this question paper. Verify it before you start answering.

There are **three** places where you need to write your name and roll-number. *Fill them up before you start answering, and sign on top of each page. Each unfilled instance will be penalized by 1 mark.*

The figures used in the question paper are also provided in the last page. You may tear it off if you wish to.

NAME (in capital)

Roll No:

Assume $\mu_n C_{ox} = 200 \mu A/V^2$, $\mu_p C_{ox} = 100 \mu A/V^2$, $V_{tn} = 1V$ and $|V_{tp}| = 1V$ everywhere

1) : Consider the circuit in Fig. 1. Assume $V_{DD} = 8V$, $V_B = 5V$, $I_0 = 100 \mu A$, $R_1 = 5k\Omega$, $R_D = 5k\Omega$, $R_L = 5k\Omega$, $(W/L)_1 = 1$, and $(W/L)_2 = 4$, $(W/L)_3 = 4$. $v_i = V_p \cos(\omega_0 t)$.

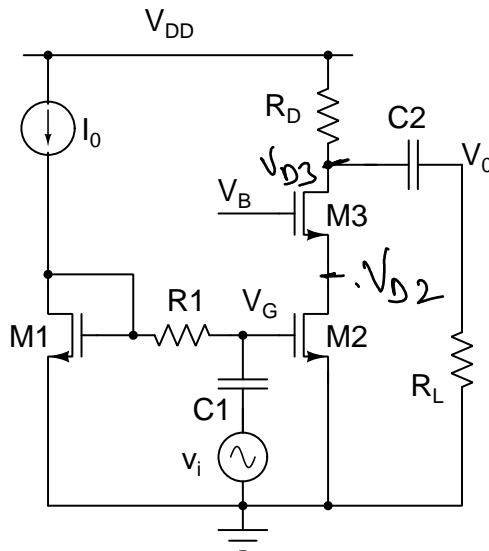


Fig. 1. Question 1

a) : Find the quiescent drain and gate voltages for M_2 and the current through M_2 . [4]

$$V_A = V_{tn} + \sqrt{\frac{2I_0}{\mu_n C_{ox} \left(\frac{W}{L}\right)_2}} = 2V$$

$$\therefore I_{DSM_2} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2 \left(V_A - V_g\right)^2 = 0.4 \mu A$$

(Assuming sat. region of operation)

If M_2 is in sat: $V_{D2} = V_B - V_{ds1}$

$$= 5 - \left(1 + \sqrt{\frac{2 \times I_{DS3}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_3}}\right) = 3V$$

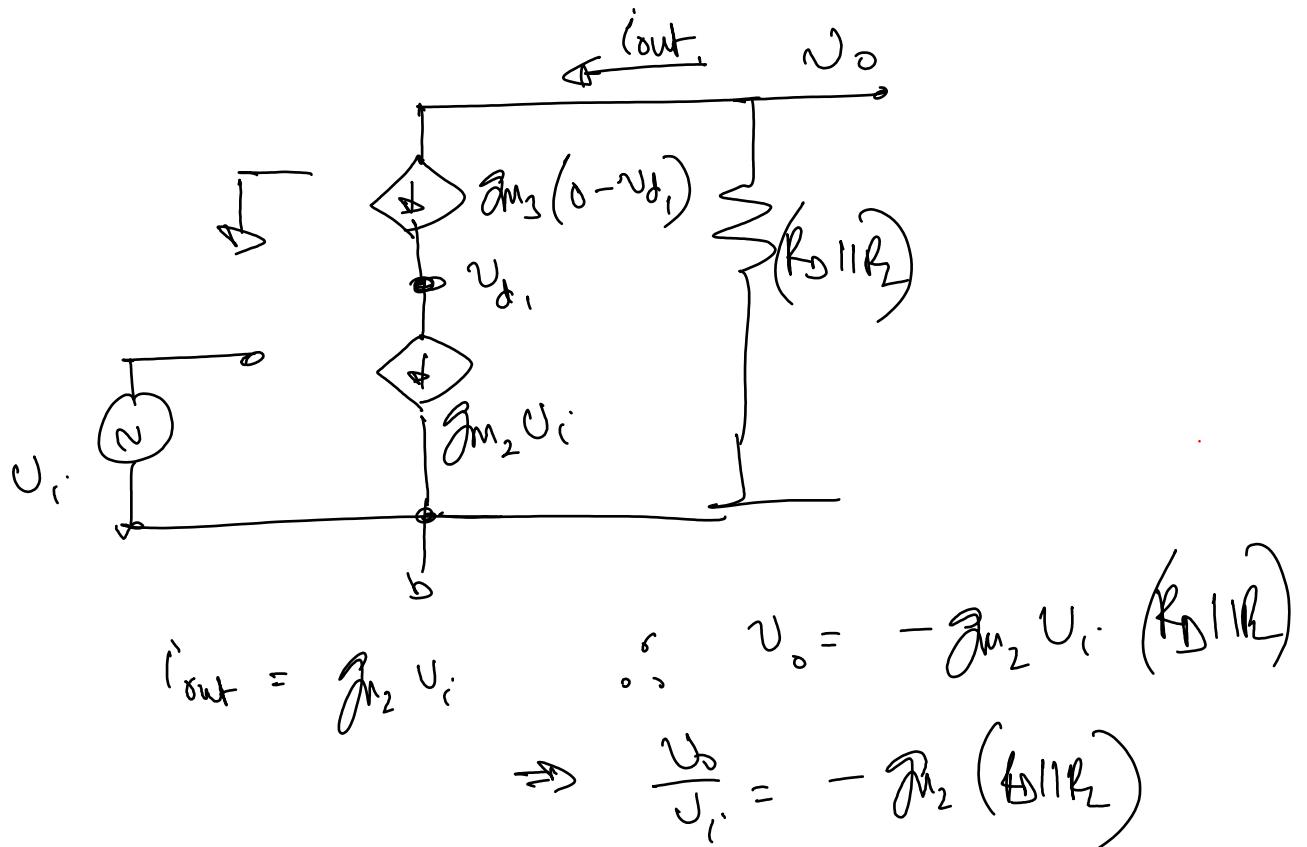
$$V_{D3} = V_{DD} - I_{DS3} \times R_D = 6V$$

\therefore All transistors in sat.

b) : If $v_i = V_p \sin(\omega_0 t)$, find the limiting constraint on R_1 such that $v_g \approx v_i$. (Assume C_1 to be shorted for your calculations) [2]

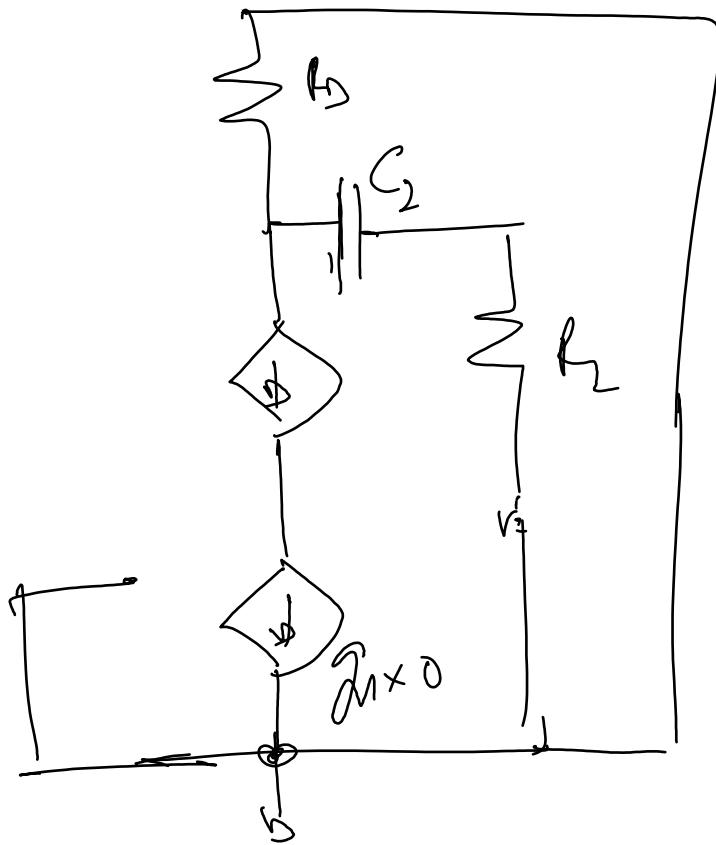
If C is shorted then no constraint is necessary.

c) : Assume the C_1 and C_2 are large enough to be treated as a short circuit at ω_0 . Find the small signal gain v_o/v_i . [5]



contd..

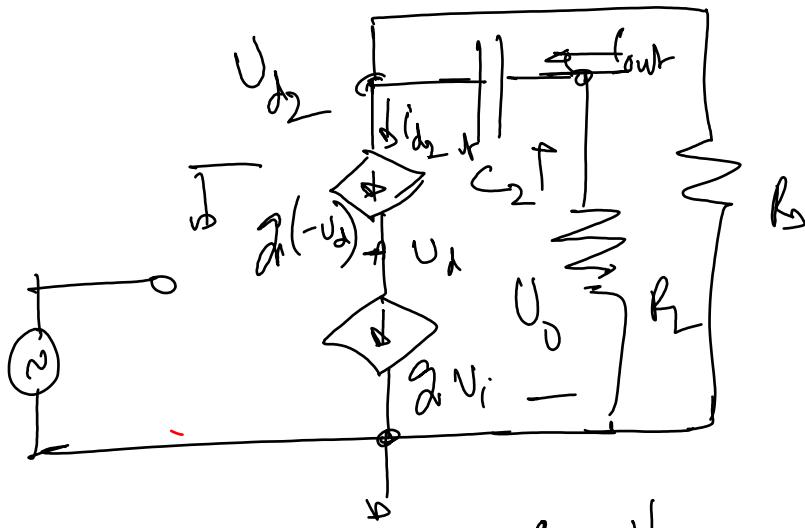
d) : What is the limiting constraint on C_2 such that it can behave like a short at ω_0 ? [2]



$$Z_{C_2} = C_2 (f_0 + R_2)$$

$$\therefore C_2 (f_0 + R_2) \gg \frac{1}{\omega_0}$$

e) : Assume C_1 to be infinitely large, and $C_2 = 1nF$. Sketch the Bode plot for $|V_0(j\omega)/V_i(j\omega)|$. [4]



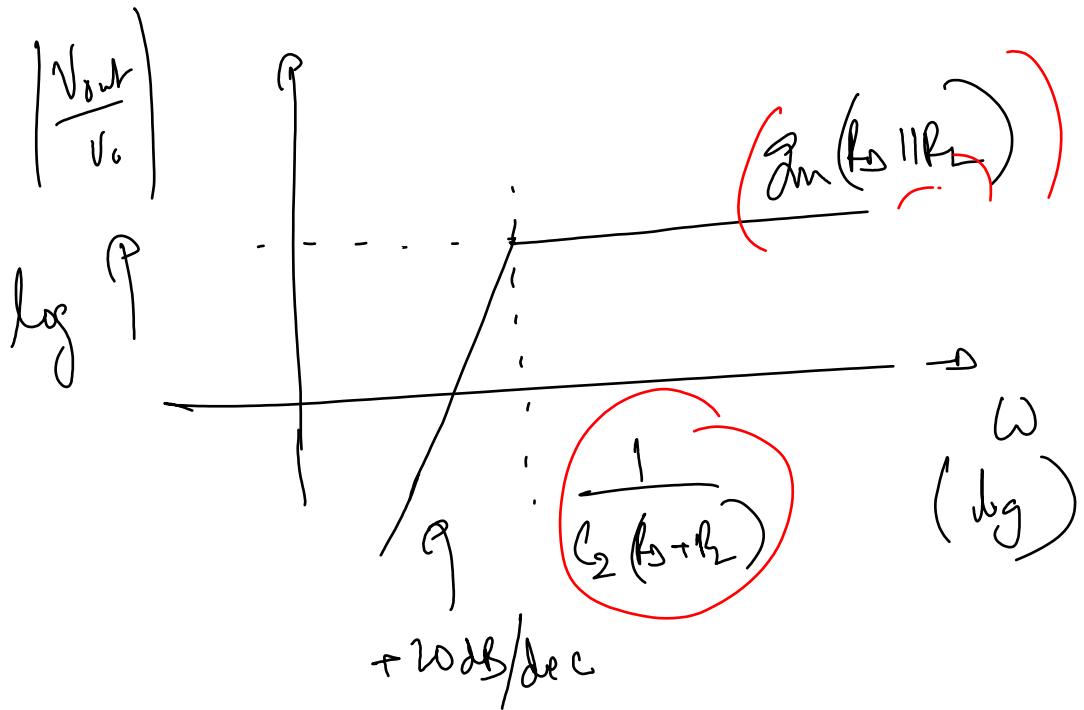
$$i_{D2} = \frac{d}{dt} V_i$$

$$KCL \circledast V_{D2}$$

$$i_{out} = i_{D2} \times \frac{R_L}{R_D + R_L + \frac{1}{j\omega C_2}}$$

$$\therefore V_{out} = -i_{out} R_L \\ = -\frac{\frac{d}{dt} V_i R_L}{(R_D + R_L) j\omega C_2 + 1}$$

$$\Rightarrow \left| \frac{V_{out}}{V_i} \right| = \frac{\omega C_2 R_D R_L \frac{d}{dt}}{\sqrt{1 + \omega^2 C_2^2 (R_D + R_L)^2}}$$



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2) : Consider the circuit in Fig. 2. $V_{DD} = 5V$, $V_B = 3V$, $(W/L)_1 = 10$.

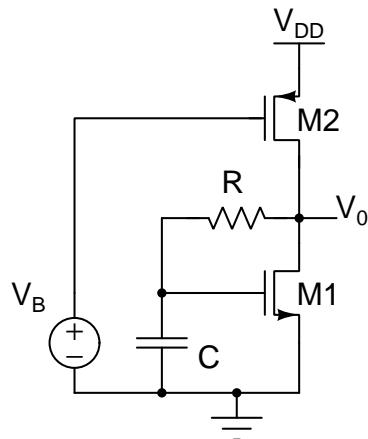


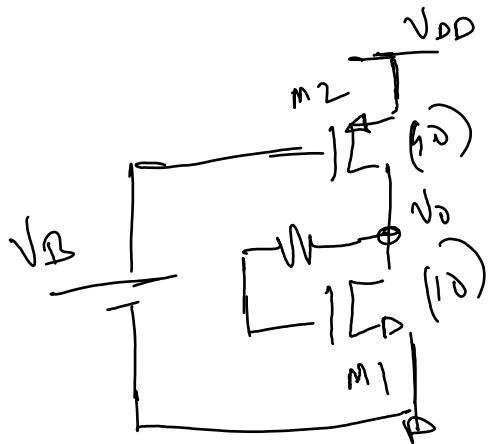
Fig. 2. Question 2

a) : Size M_2 (find W/L) such that quiescent $V_0 = 3V$.

[3]

$$\begin{aligned} I_{SD}|_{M_2} &= I_{DS}|_{M_1} \\ \Rightarrow \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_2 (2-1)^2 &= \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_1 (2-1)^2 \\ \Rightarrow \left(\frac{W}{L}\right)_2 &= 40 \end{aligned}$$

b) : Using the size that you found in question -2a), what is the minimum V_{DD} required to keep all transistors in saturation? (you are allowed to change V_B) [3]



Reducing V_{DD} will reduce current.
To ensure M_2 does not go into cutoff we need to decrease V_B .
 $\because M_1$ is always in sat, reducing V_B can cause M_2 to go into linear.

$$\therefore V_{B_{\min}} = V_0 - |V_{thn}|$$

$$\therefore \frac{1}{2} \mu_p C_{ox} \times \left(\frac{W}{L}\right) \cdot \left(V_{Dn} - V_0 + \frac{|V_{thn}|}{2}\right)^2 = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) \cdot (V_0 - |V_{thn}|)^2$$

$$\Rightarrow 2 (V_{DD} - V_0)^2 = (V_0 - i)^2$$

$$\Rightarrow V_{DD} - V_0 = 0.7(V_0 - i)$$

$$\Rightarrow V_{DD/\min} = 1.7V_0 - 0.7V$$

$$\text{If } V_{0\min} = 1.1V \quad (\text{To keep } |V_{thn}|_{\min} = 0.1V)$$

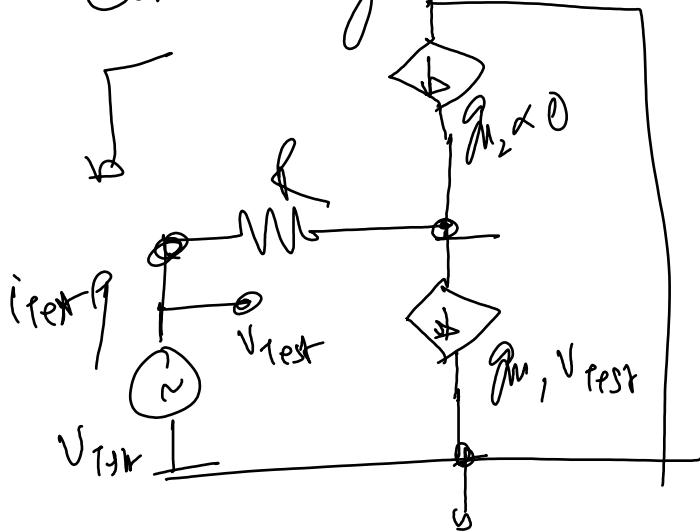
$$\text{then } V_{DD/\min} = 1.17V$$

(Okay if someone has assumed the current to be same as part (a) or has assumed $V_{0\min} = 1V$)

This question is open to interpretation.

c) : Assume $V_{DD} = 5V$ for the rest of the question. Find the time-constant (τ) associated with C . ($V_B = 3V$) [3]

Small signal model for finding Reg across C .

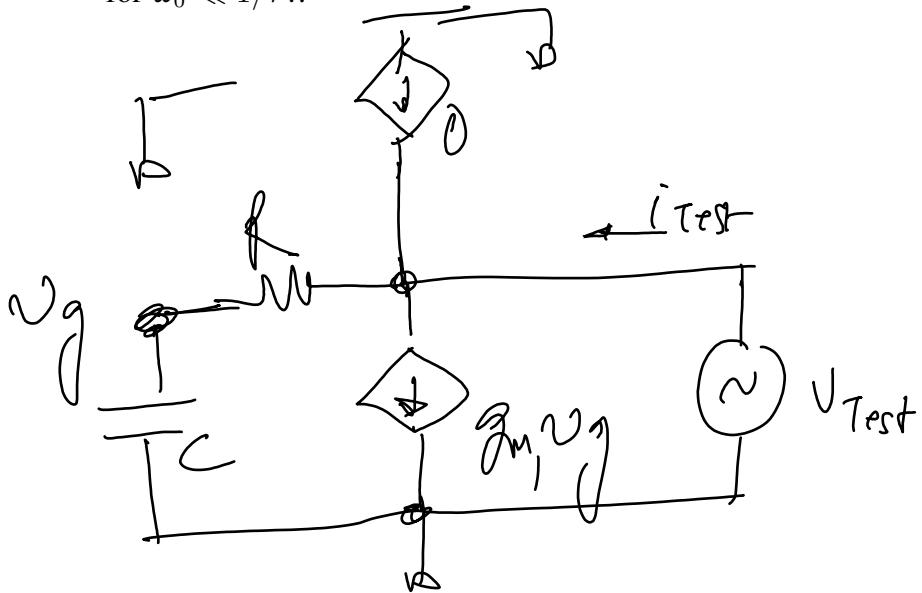


$$i_{1test} = g_m V_{1test}$$

$$\therefore \text{Reg} = \frac{1}{g_m}$$

$$\therefore \tau = \frac{C}{g_m}$$

d) : Find the incremental output resistance looking into v_0 at frequencies $\omega_0 \gg 1/\tau$? and for $\omega_0 \ll 1/\tau$? [4]



For $\omega_0 \gg 1/\tau$ C acts as a short chkt. $\therefore v_g = 0$

$$\therefore i_{\text{test}} = \frac{v_{\text{test}}}{R} \Rightarrow R_{\text{out}} = R.$$

For $\omega_0 \ll 1/\tau$ C acts as an open chkt.

$$\therefore v_g = v_{\text{test}} \text{ and } i_{\text{test}} = g_{m1} v_{\text{test}}$$

$$\Rightarrow R_{\text{out}} = \frac{1}{g_{m1}}$$

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3) : Consider Fig. 3. Assume $V_{DD} = 5 V$ $R_1 = 10 k\Omega$, $R_2 = 2 k\Omega$.

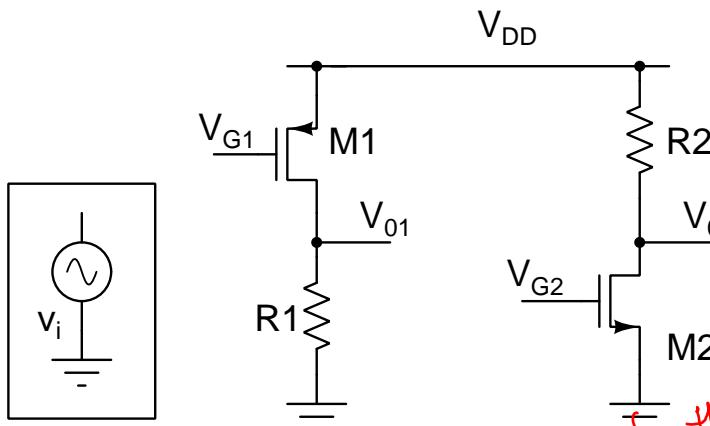
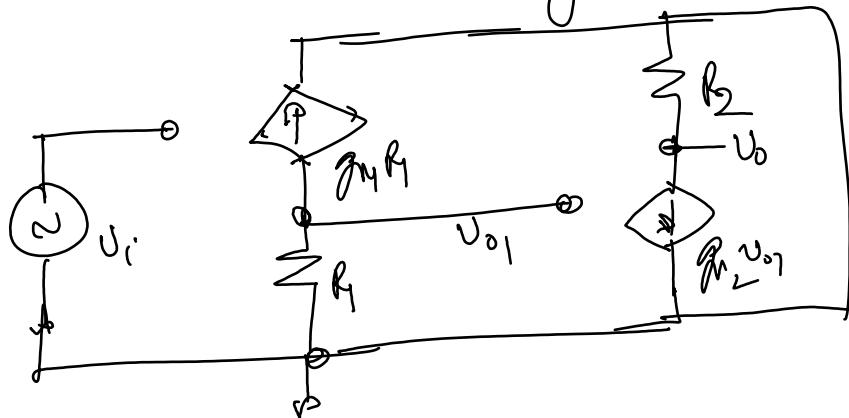


Fig. 3. Question 3

a) : The requirement is to apply the incremental input v_i at the gate of M_1 and observe the incremental output at V_{o2} . Design the network and connect it up such M_1 and M_2 are in saturation (and has a minimum overdrive voltage of 500 mV) and $v_{o2}/v_i \approx 100$. You may use additional components (only resistors and capacitors). If you plan to use them find their values and state all assumptions clearly.

Note: There can be multiple possible solutions. So sketch the final network with all the relevant values clearly marked for clarity of the grader. [6]

If incrementally V_{o1} is connected to V_{G2} , then the config. looks like two common source amps connected one after the other. The incremental picture looks like the following



$$\begin{aligned}
 V_{o1} &= -g_m R_1 V_i \\
 V_{o2} &= -g_m R_2 V_{o1} \\
 &= g_m g_m R_1 R_2 V_i \\
 \Rightarrow \frac{V_{o2}}{V_i} &= g_m R_1 g_m R_2
 \end{aligned}$$

This is a design problem with multiple possible approaches and answers. Grade liberally. Try to check if the student has understood the basic. Fundamental mistakes must be penalized harshly.

contd.. Let's assume a gain of 10 for each stage
 i.e. $\beta_{M1} = \beta_2 \beta_3 = 10$ (Note that the split of the gain of 100 can be anything).

$$\therefore T_M = \frac{10}{10k} = 1 \text{ ms} \quad T_{M2} = \frac{10}{2k} = 5 \text{ ms.}$$

Strategy: Design two C-S amps separately and couple them through a capacitor.

$$\beta_M = \mu_F \text{Cor} \left(\frac{W}{L} \right) V_{DD} = 1 \text{ ms} \dots \textcircled{i}$$

$$T_{SD1} = \frac{1}{2} \mu_F \text{Cor} \left(\frac{W}{L} \right) V_{DD}^2$$

$$V_{DD \text{ max}} = V_{DD} - (V_{DD} + V_{FB}) + V_{FB}$$

$$\Rightarrow T_{SD1} R_1 = V_{DD} - V_{DD}$$

$$\Rightarrow \frac{W}{L} V_{DD}^2 = 5 - V_{DD}$$

$$\Rightarrow \frac{1}{2} \left(\frac{W}{L} \right) V_{DD}^2 + V_{DD} - 5 = 0$$

$$\text{From } \textcircled{i} \quad \left(\frac{W}{L} \right) V_{DD} = 10$$

$$\therefore 6 V_{DD} = 10$$

$$\Rightarrow V_{DD} = \frac{5}{3}$$

$$\therefore \left(\frac{W}{L} \right)_1 = 12$$

$$V_{G1} = V_{DD} - (V_{FB} + V_{DD}) \\ = \frac{19}{6} V_{DD} = \frac{V_{DD} R_{B1}}{R_{B1} + R_{B2}}$$

and G such that

$$G \left(R_{B1} || R_{B2} \right) \Rightarrow \frac{1}{\omega_0}$$

To 2nd Stage

$$\text{Similarly: } \beta_2 = \mu_F \text{Cor} \left(\frac{W}{L} \right)_2 \quad V_{DD} = 5 \text{ ms}$$

$$V_{DD \text{ min}} = V_{DD} + V_{FB} - V_{DD} = V_{DD}$$

$$T_{SD2} = \frac{1}{2} \mu_F \text{Cor} \left(\frac{W}{L} \right)_2 V_{DD}^2$$

$$V_{DD \text{ min}} = V_{DD} = V_{DD} - T_{SD2} R_2$$

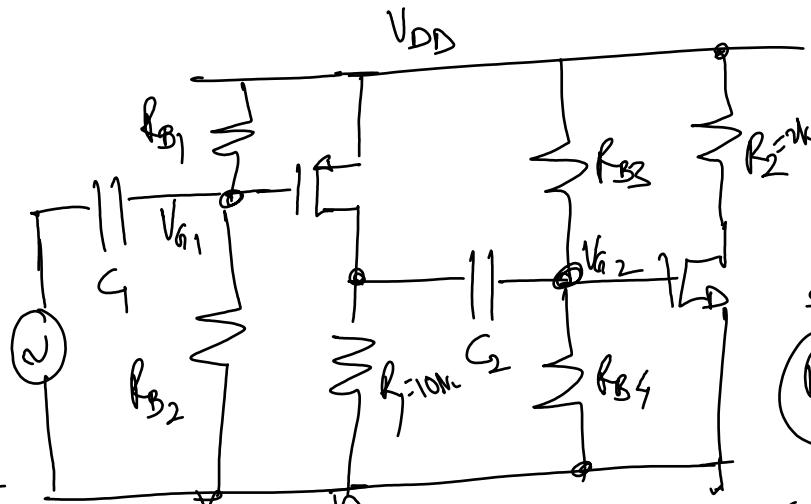
$$\Rightarrow V_{DD} = 5 - 0.2 \left(\frac{W}{L} \right) V_{DD}^2$$

$$\text{from } \textcircled{i} \quad \left(\frac{W}{L} \right)_2 V_{DD} = 10$$

$$\therefore V_{DD} = \frac{5}{3}$$

$$\left(\frac{W}{L} \right)_2 = 6$$

$$\therefore V_{G2} = V_{DD} + V_{FB} = \frac{8}{3} V$$



$$\therefore \frac{V_{DD} R_{B4}}{R_{B3} + R_{B4}} = \frac{8}{3}$$

and choose G_2
 such that

$$(R_1 + R_{B4} || R_{B3}) G_2 \Rightarrow \frac{1}{\omega_0}$$

$$\text{Also } (R_{B3} || R_{B4}) \Rightarrow R_1$$

b) : If $v_i = V_p \sin(\omega_0 t)$, what is the maximum V_p that you can apply while keeping $M1$ and $M2$ in saturation? [4]

The choice of the V_{in} and (W/L) is such that the devices are just at the edge of saturation, $V_{pmax} = 0$,

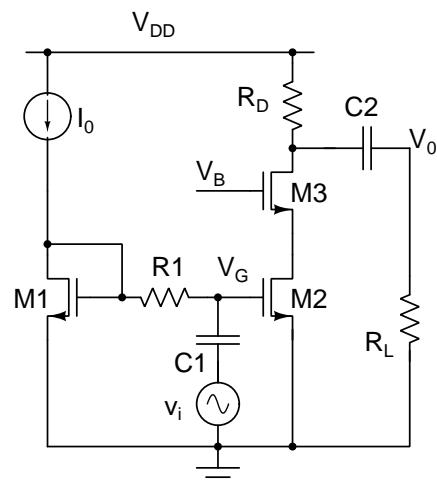


Fig. 4. Question 1

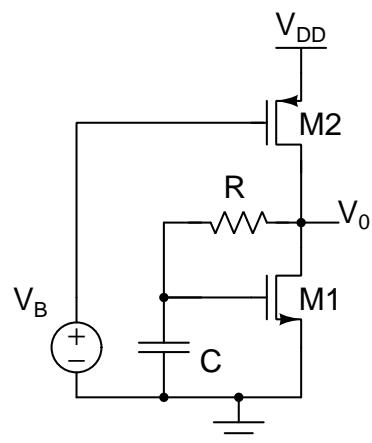


Fig. 5. Question 2

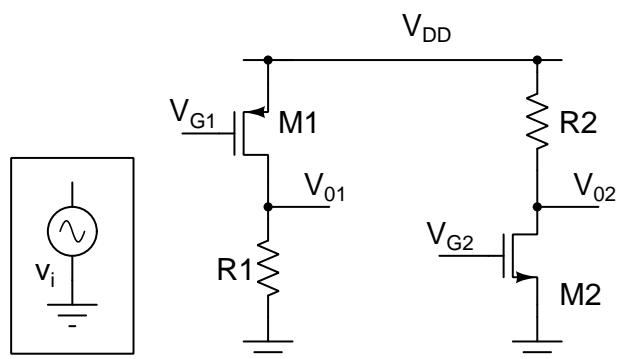


Fig. 6. Question 3