ABSTRACT

The constant downscaling of semiconductor technology has led to development of circuits that can pump charge required for functioning of circuit but at the same time the size of pump must be reduced as per requirement. However, in many state of art applications, some circuit components still need higher than the nominal supply voltage for proper operation. The function of charge pump circuits is to provide this higher voltage by stepping up the regular dc supply.

The reliability of current CMOS devices is a big challenge since CMOS devices are of extremely small in dimensions. This has pushed the industry to look for more high voltage tolerant CMOS devices instead of their low voltage counterparts.

Implementing a monolithic highly efficient ultralow photovoltaic (PV) power harvesting system is pivotal for smart nodes of Internet of things (IOT) networks.

The switching-mode dc–dc power converter using an inductor or a transformer, such as a boost converter, features high transferring power density and efficiency. However, the high-quality on-chip inductors are not widely available for the CMOS technology. Therefore, to achieve monolithic integration, a charge pump is chosen for its compact on-chip capacitor.

The following report is a portion of “Highly Efficient Ultralow Photovoltaic power”. Vsolar is the voltage generated by solar cell depending upon the intensity of light falling on solar cell.

The nested voltage tripler generated **Vout=3xVsolar** .

The following model of Voltage Tripler works as Vout=3xVs. The CMOS technology has dimensions of Tripler portion as follows:

PMOS: L=180nm, W=40um; NMOS: L=180nm, W=20um

For auxiliary charge pump, the dimensions are:

PMOS: L=180nm, W=5um; NMOS:L=180nm,W=2.5um

Non overlapping clock generator is used in here to generate a clock signal 250KHz.

And here are the Observation from the simulation:

Vsolar: 1.5V ;Vout:2.69V

Time to reach steady state for nested voltage Tripler =1.92ms

Vpb=2.67V