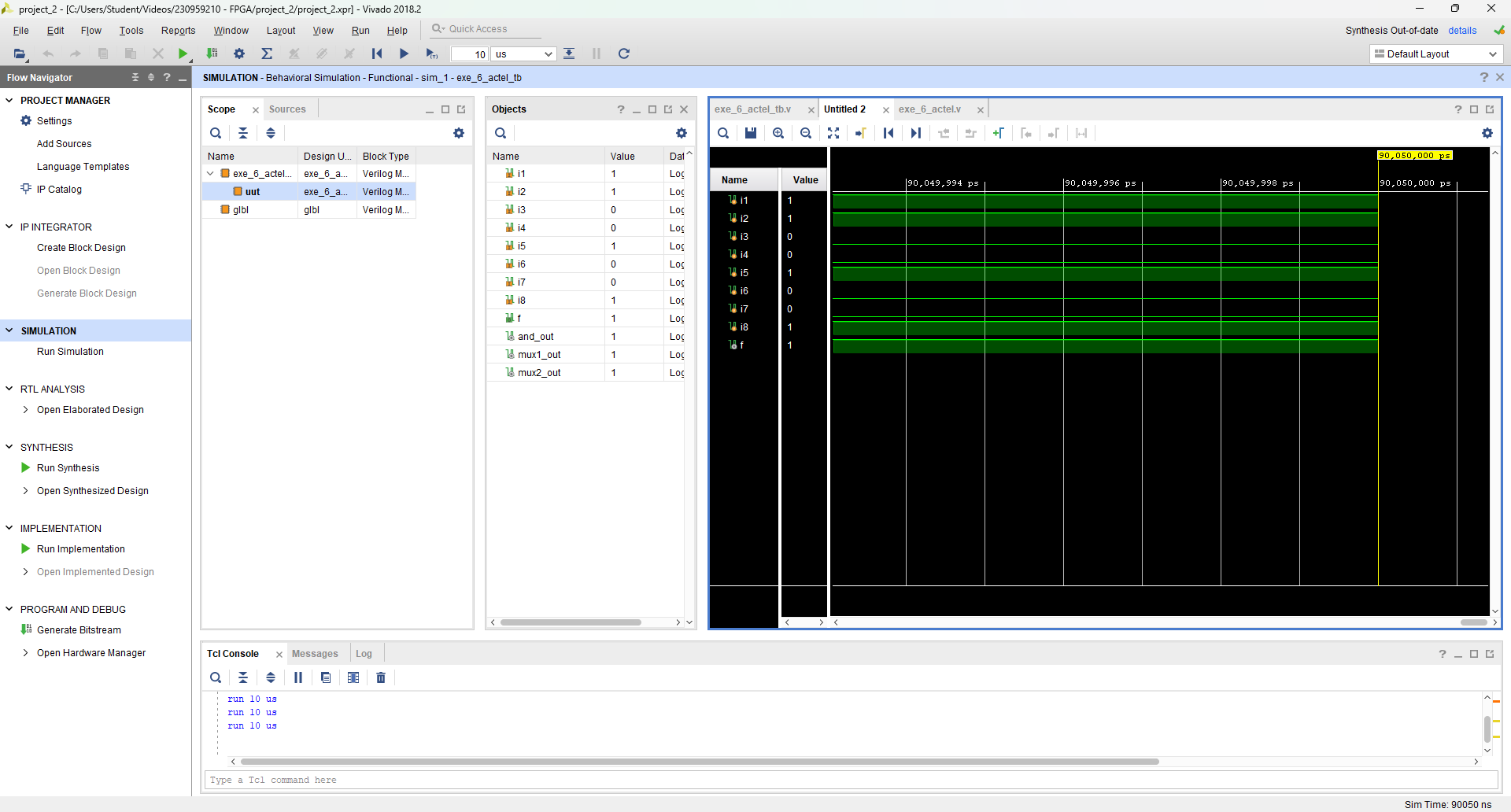
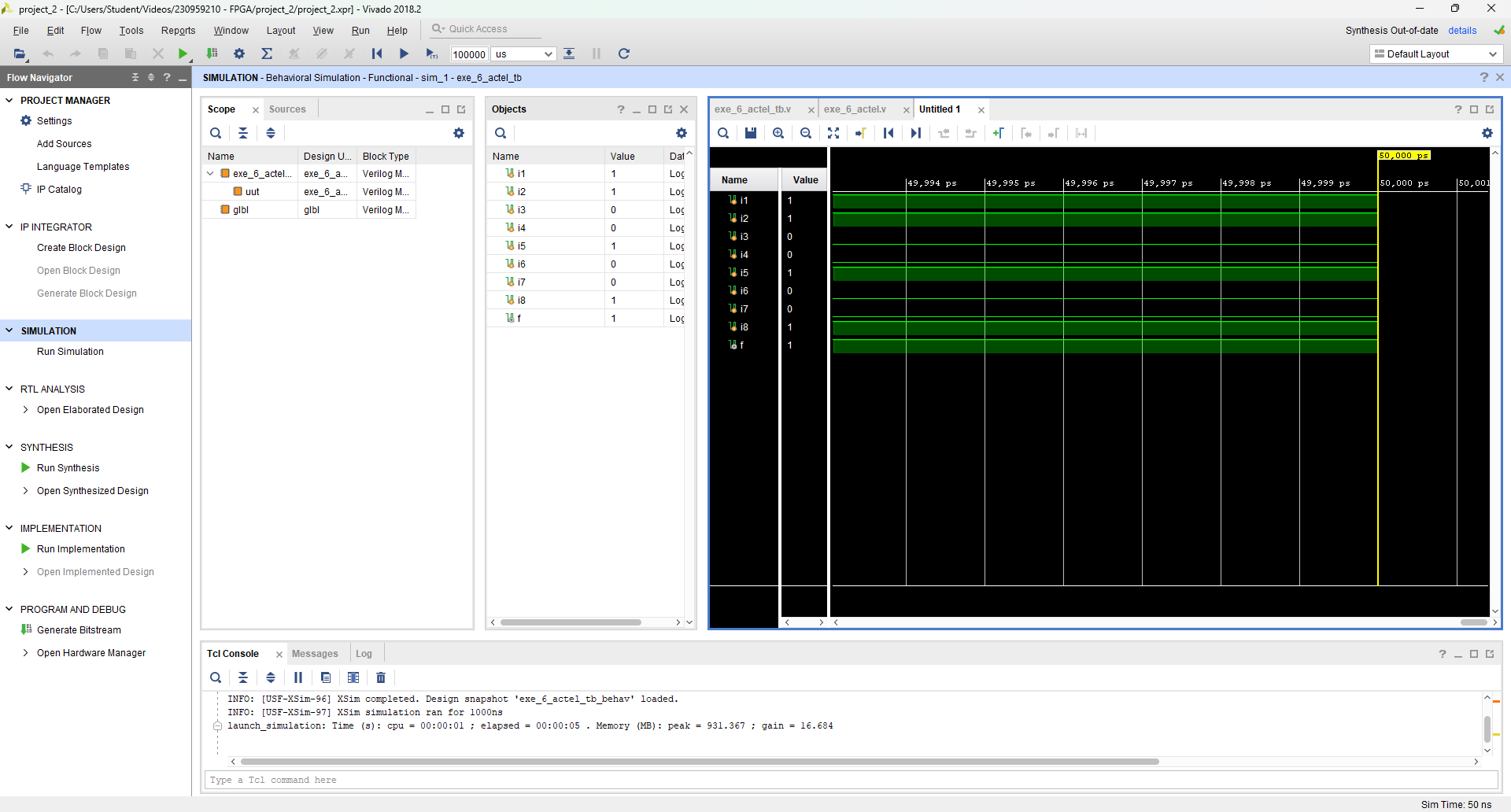
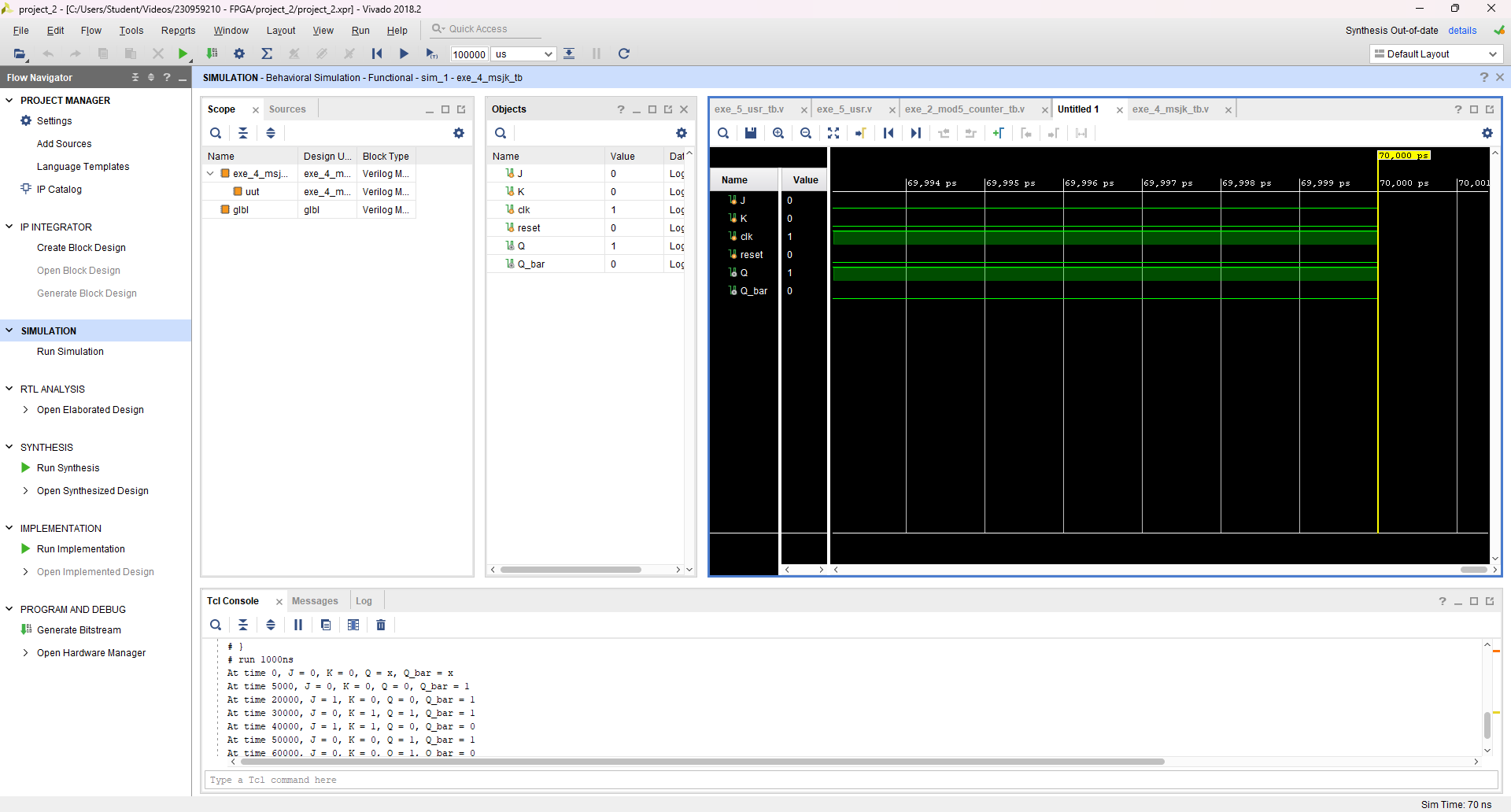
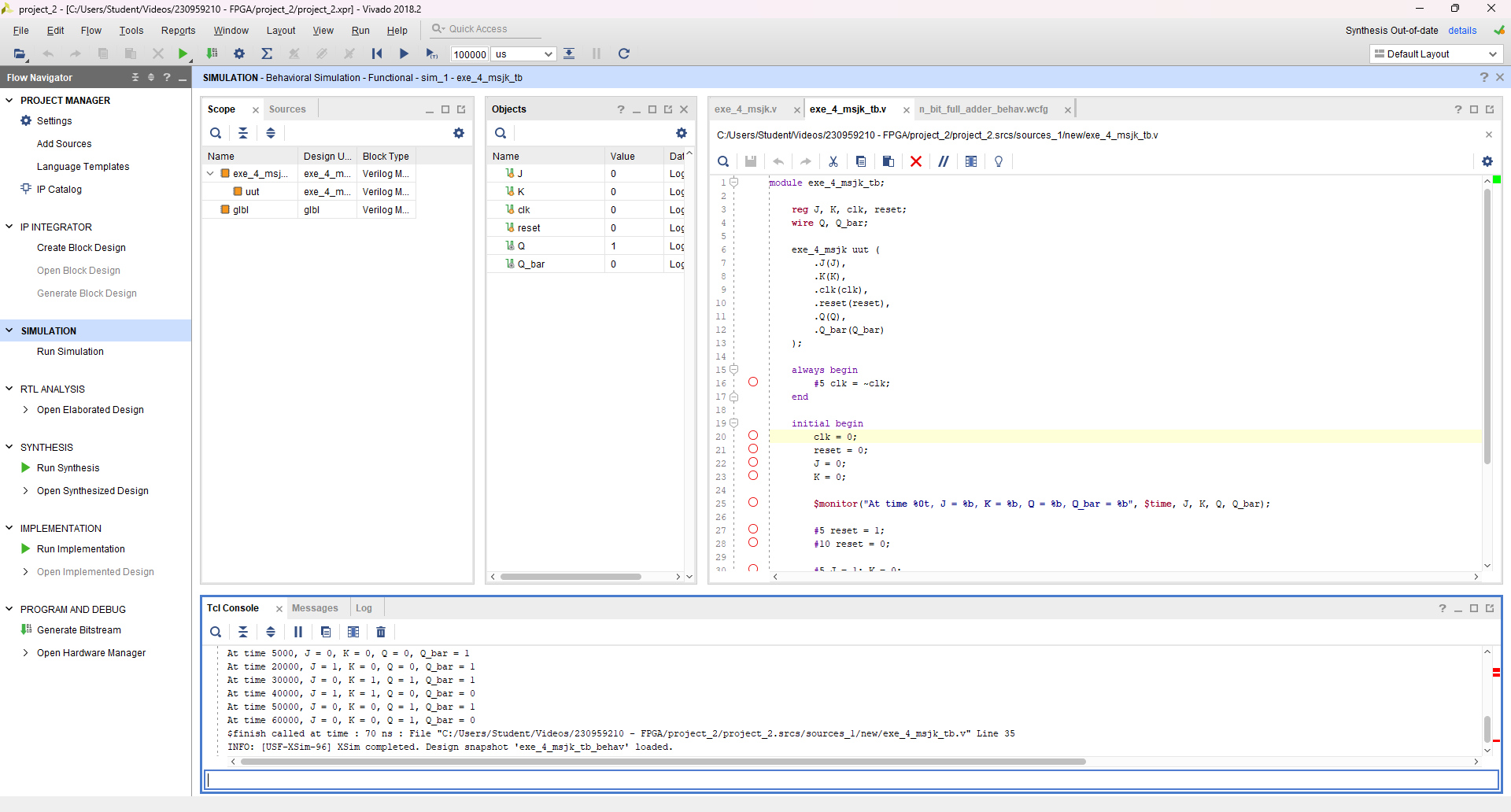
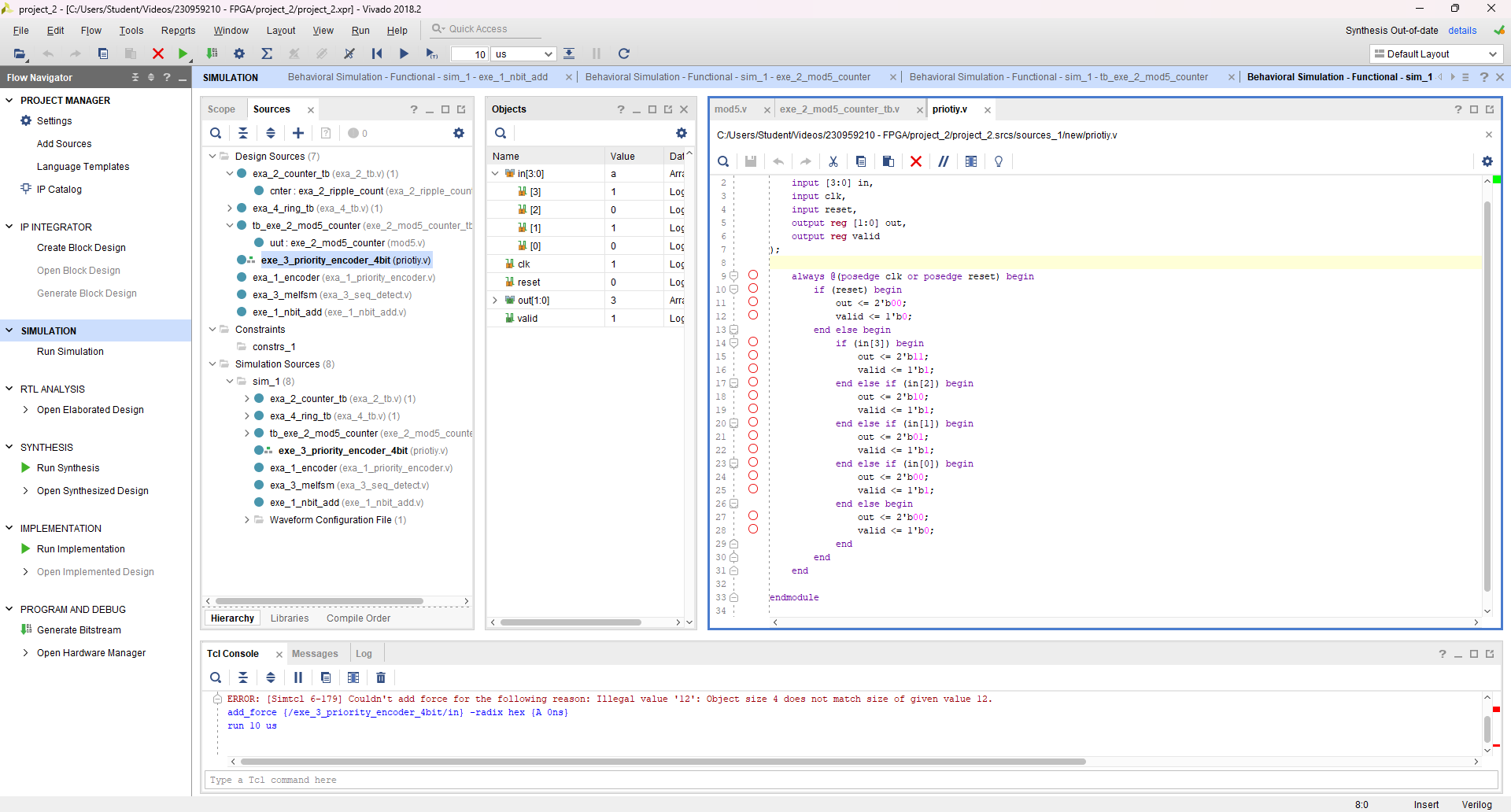
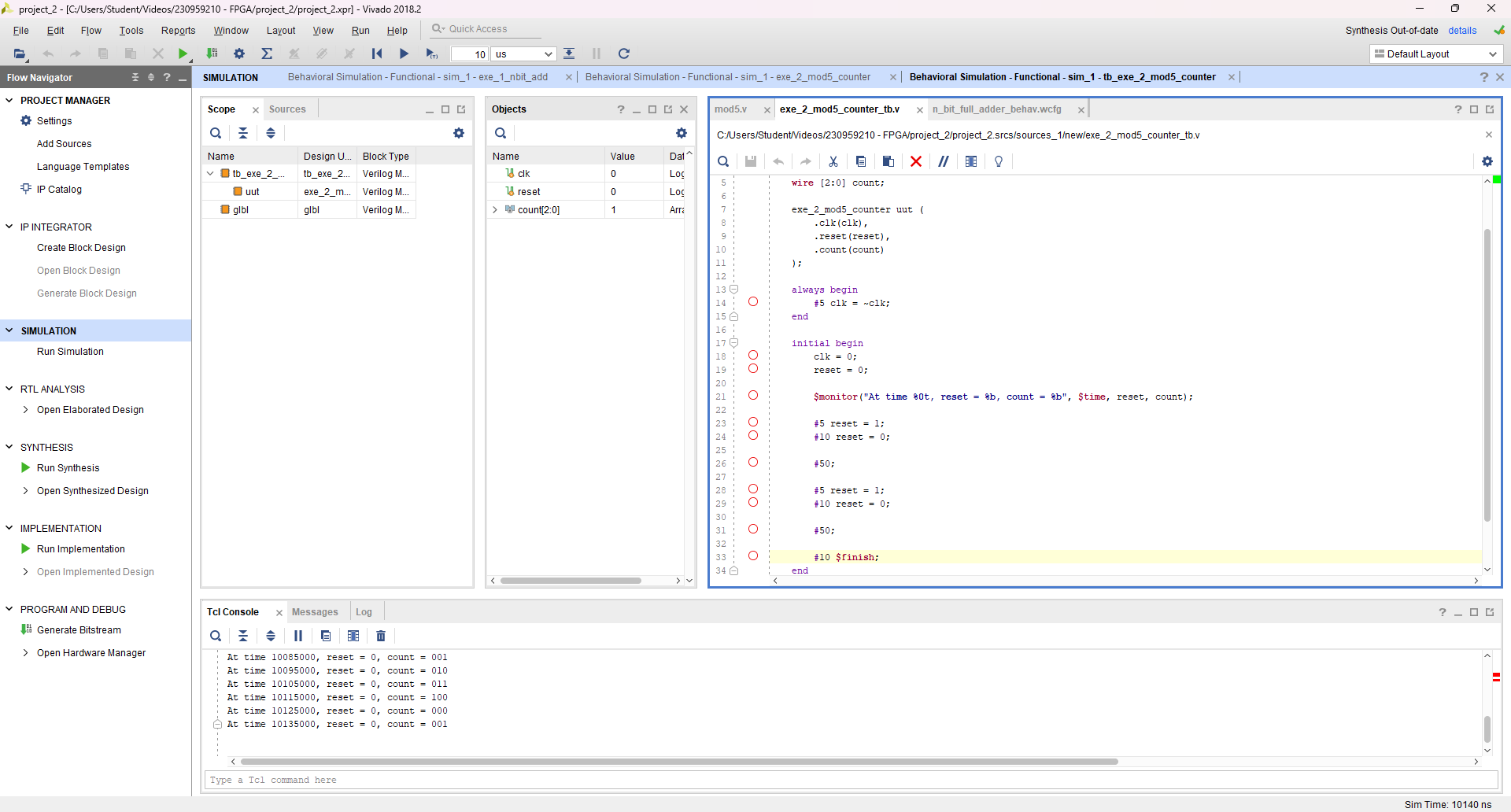
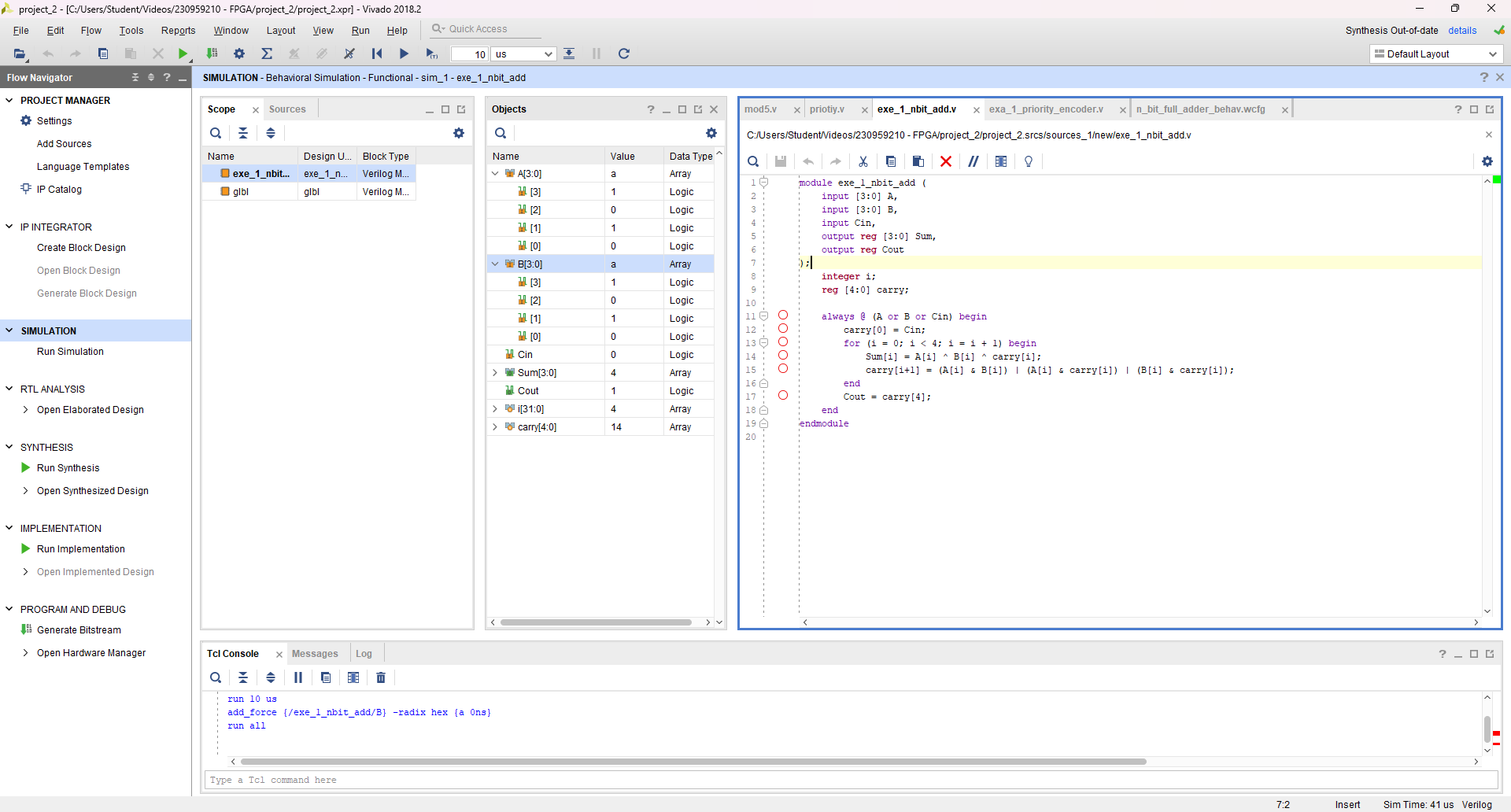
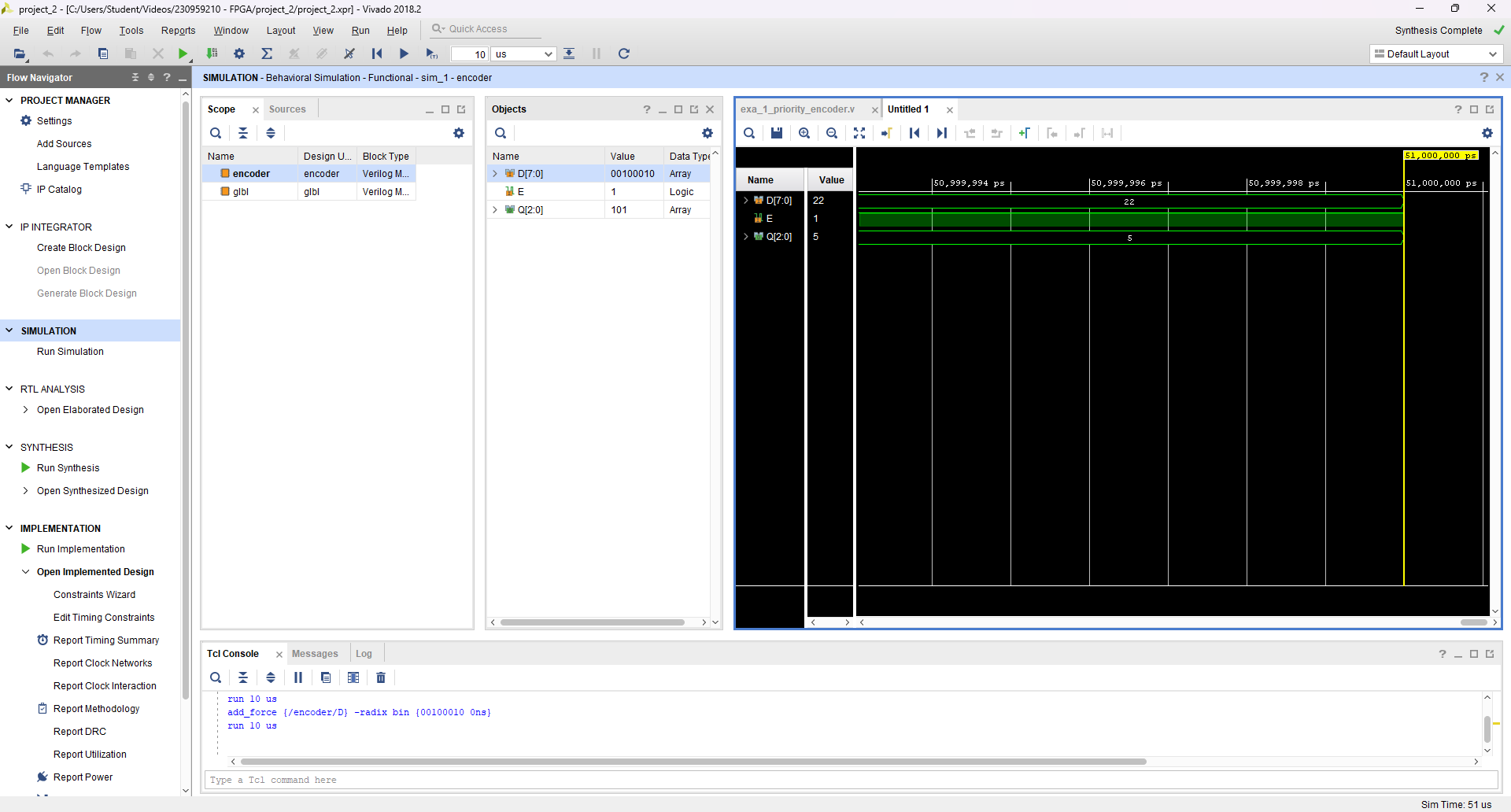
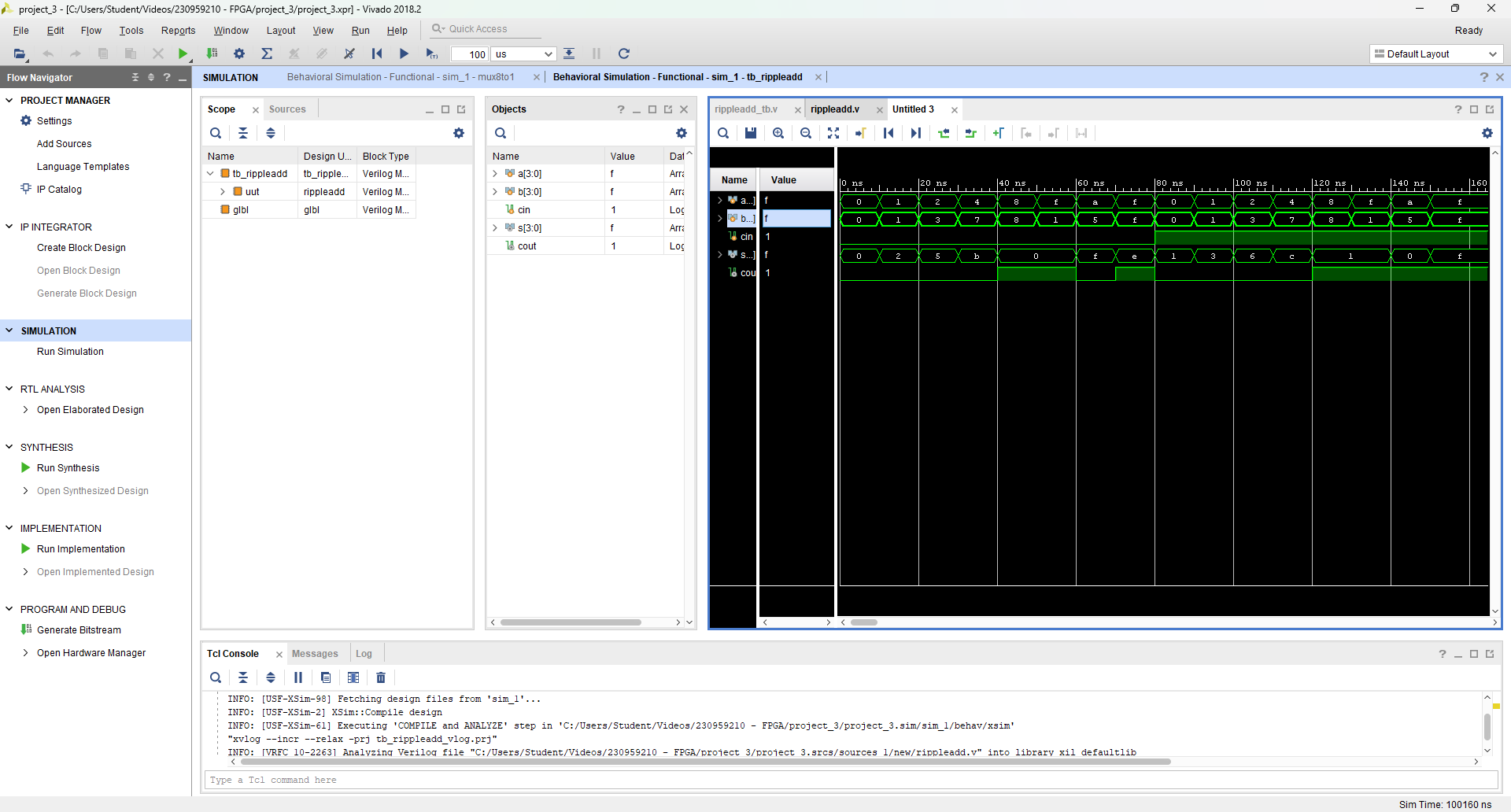
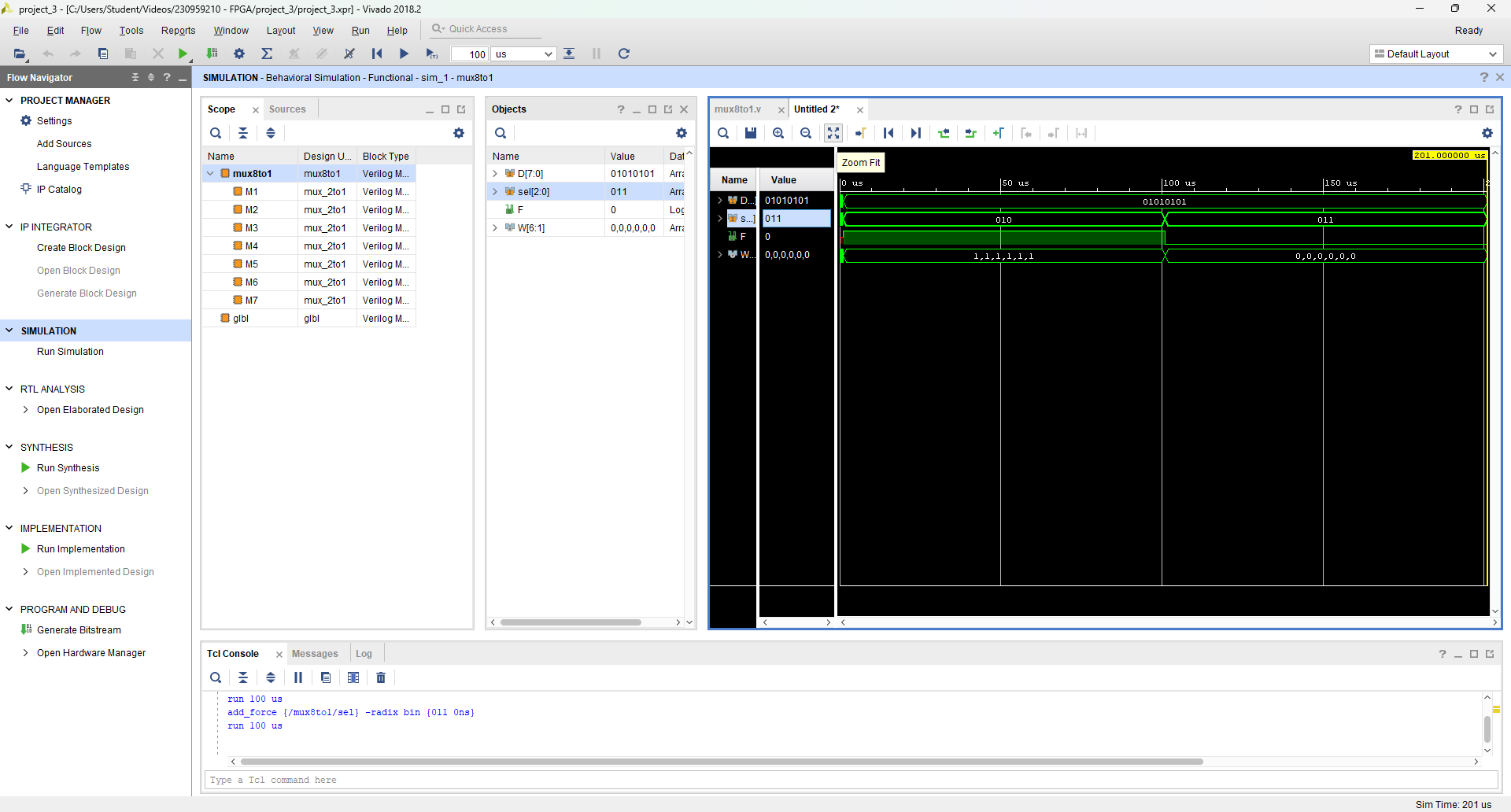
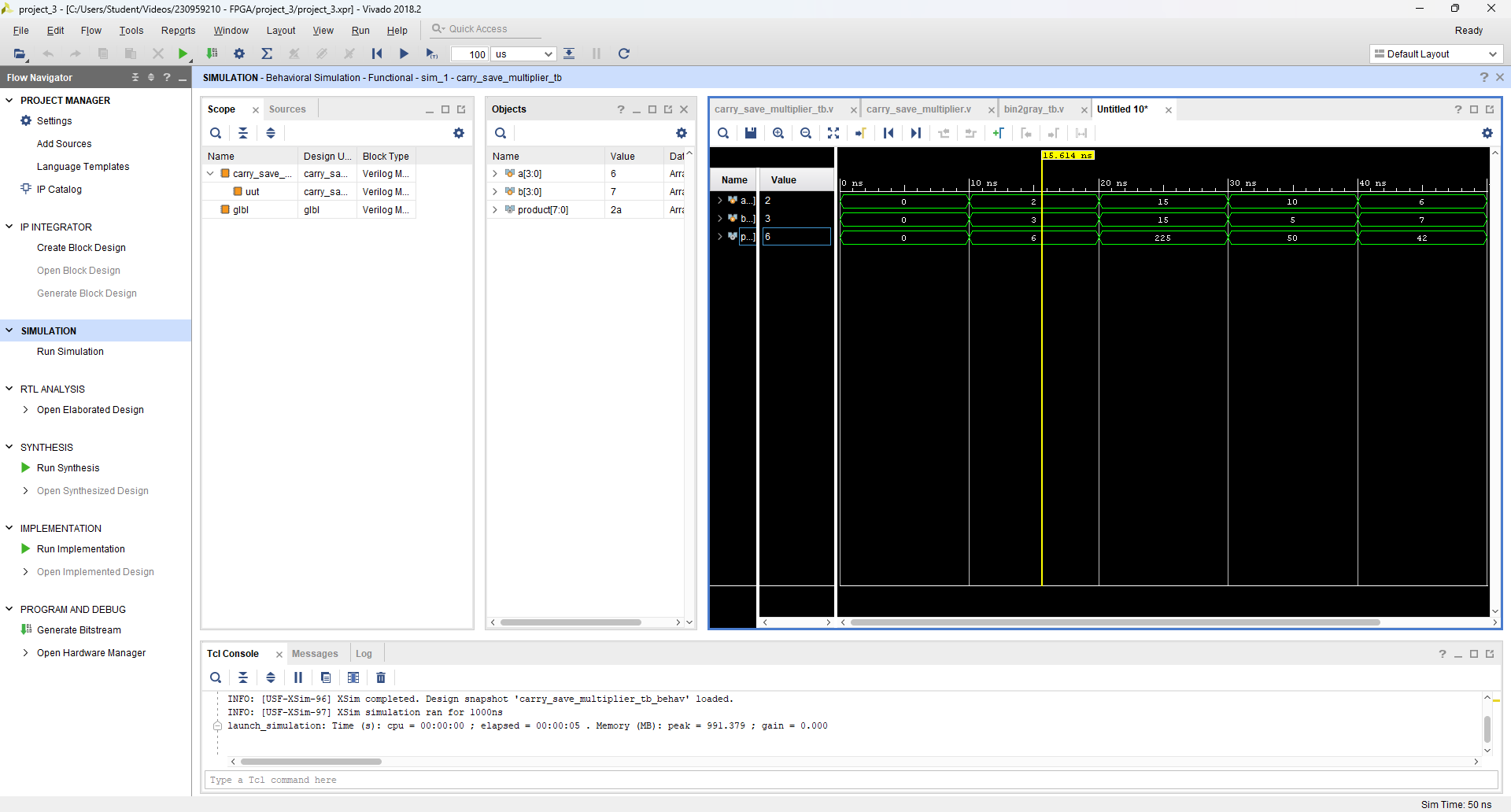
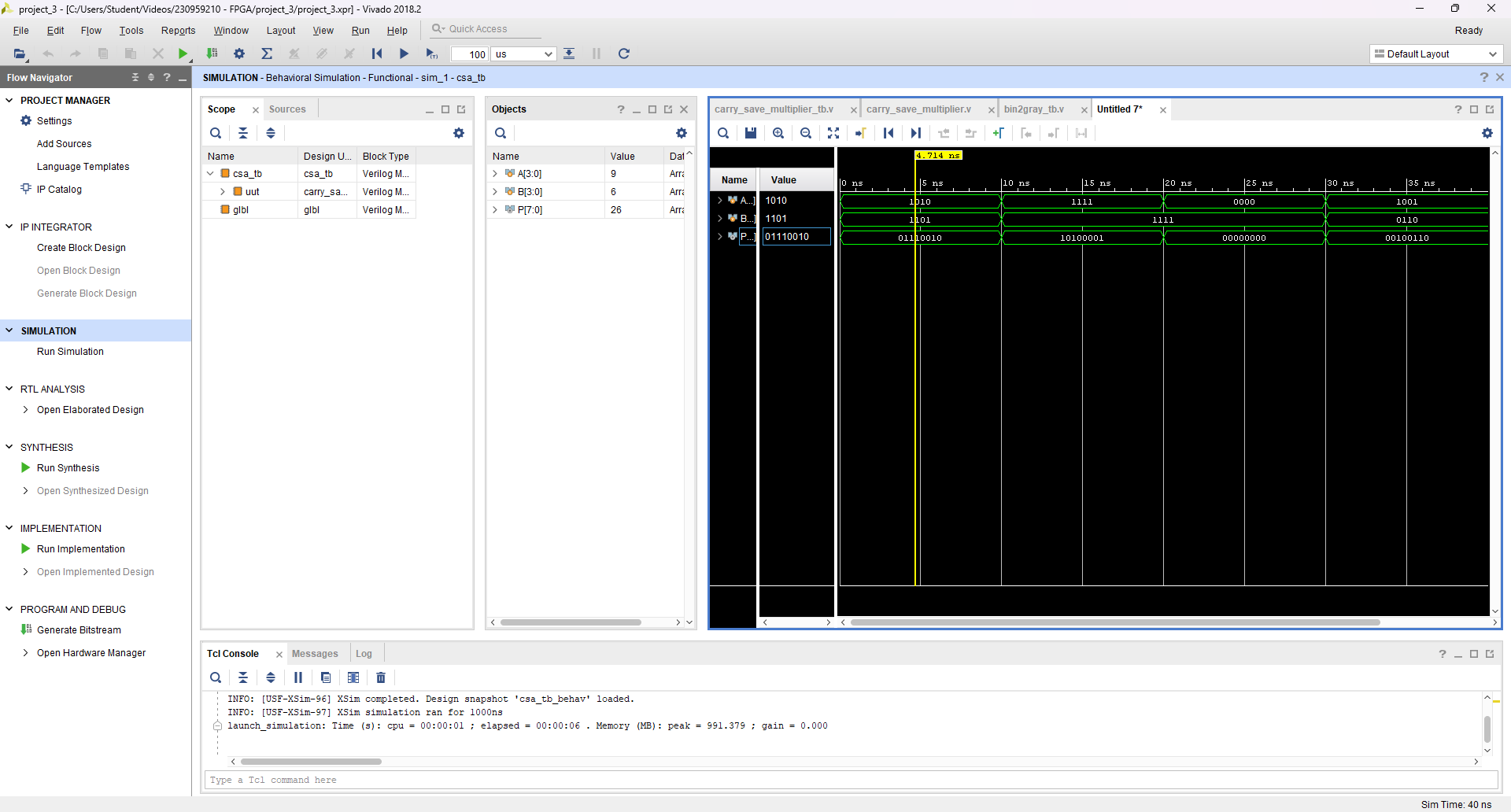
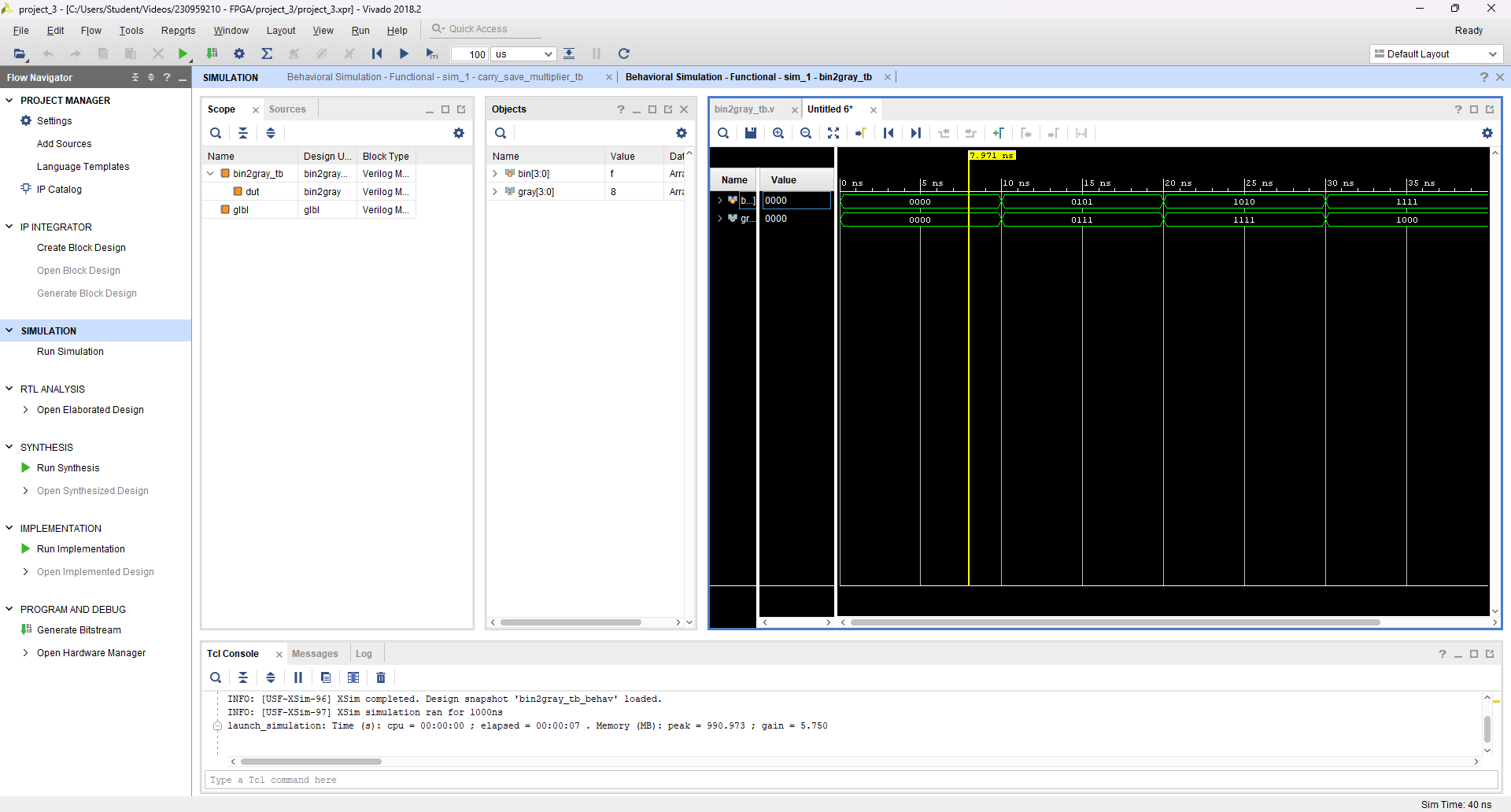
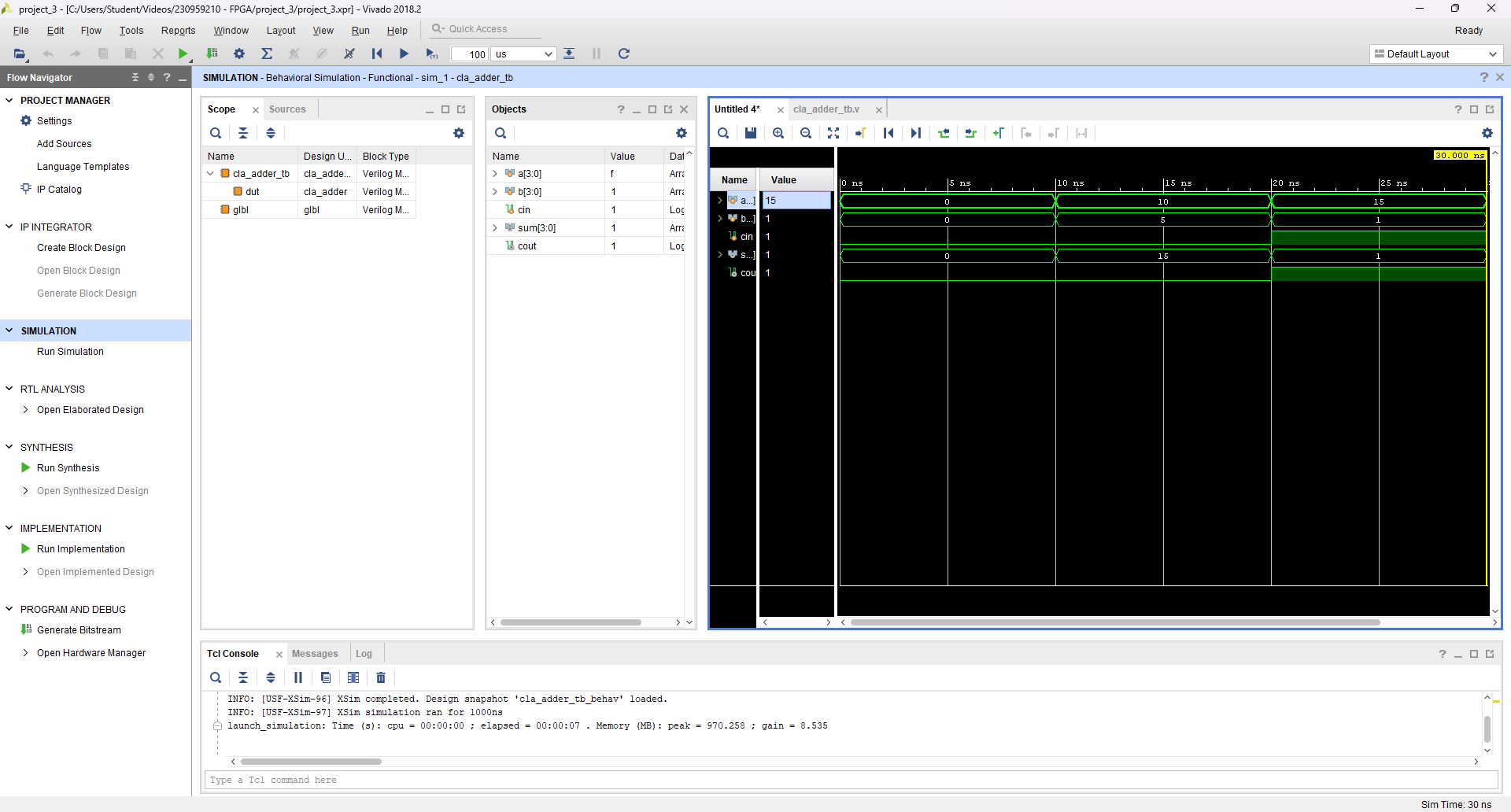
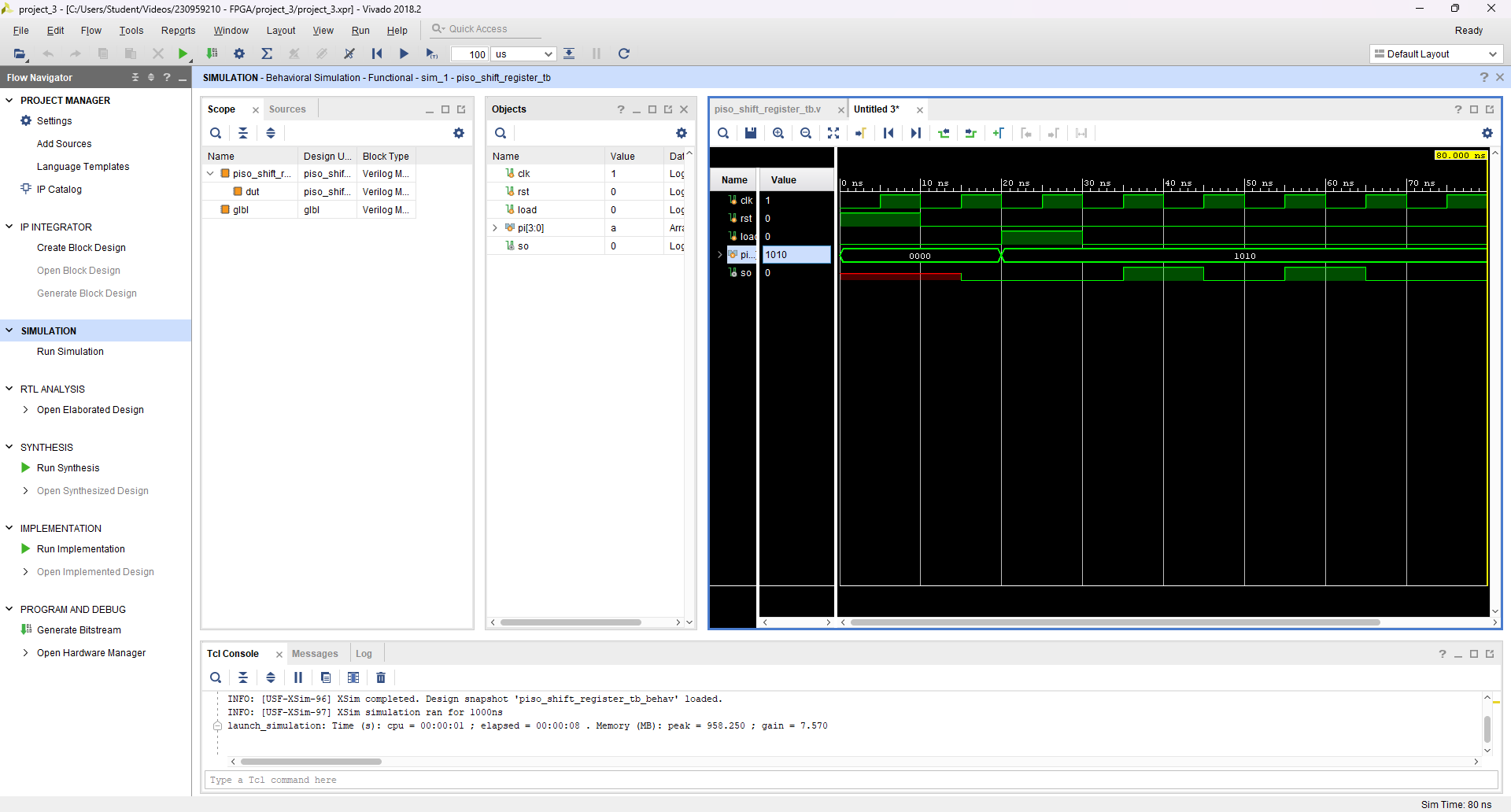
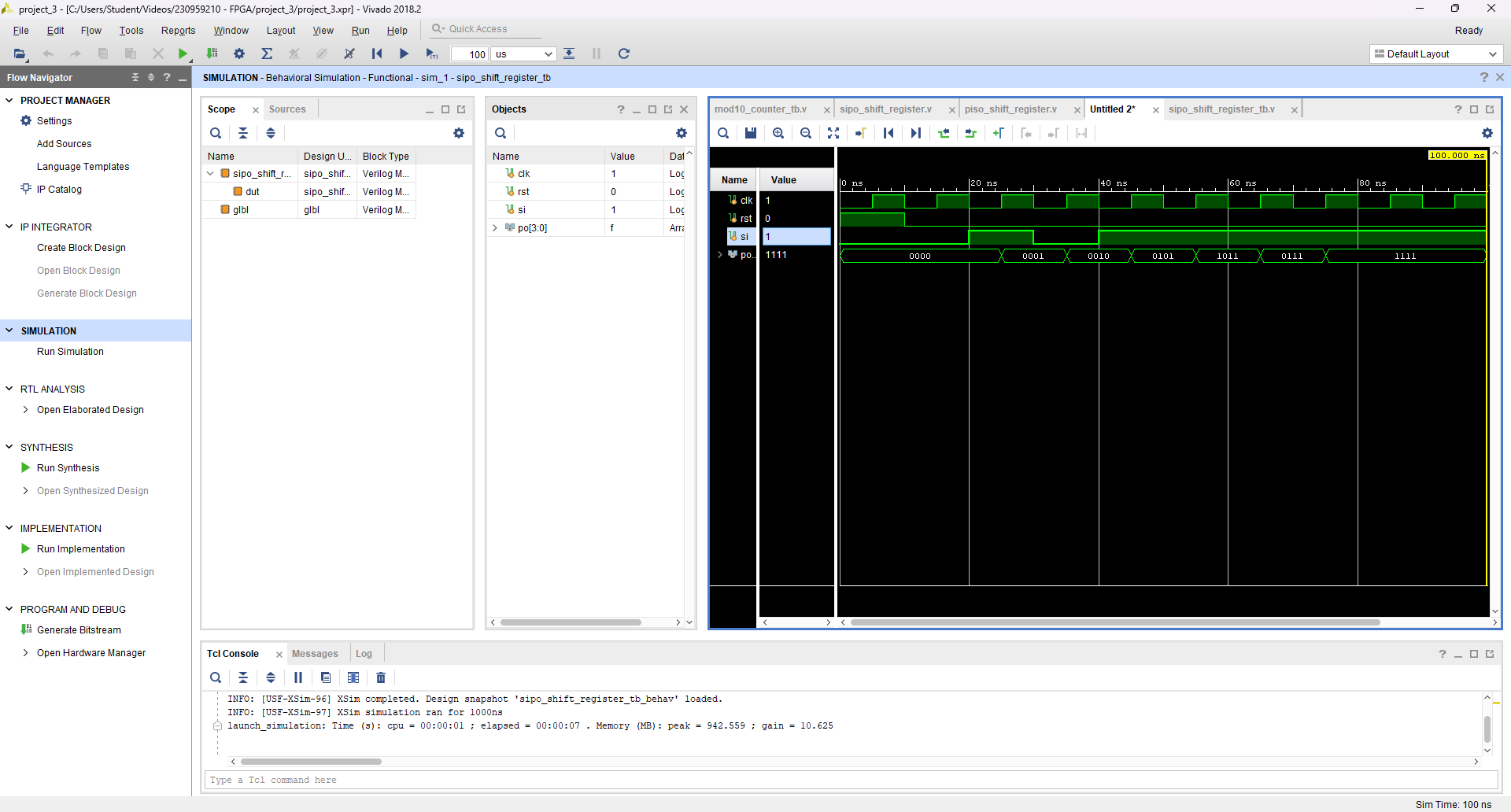
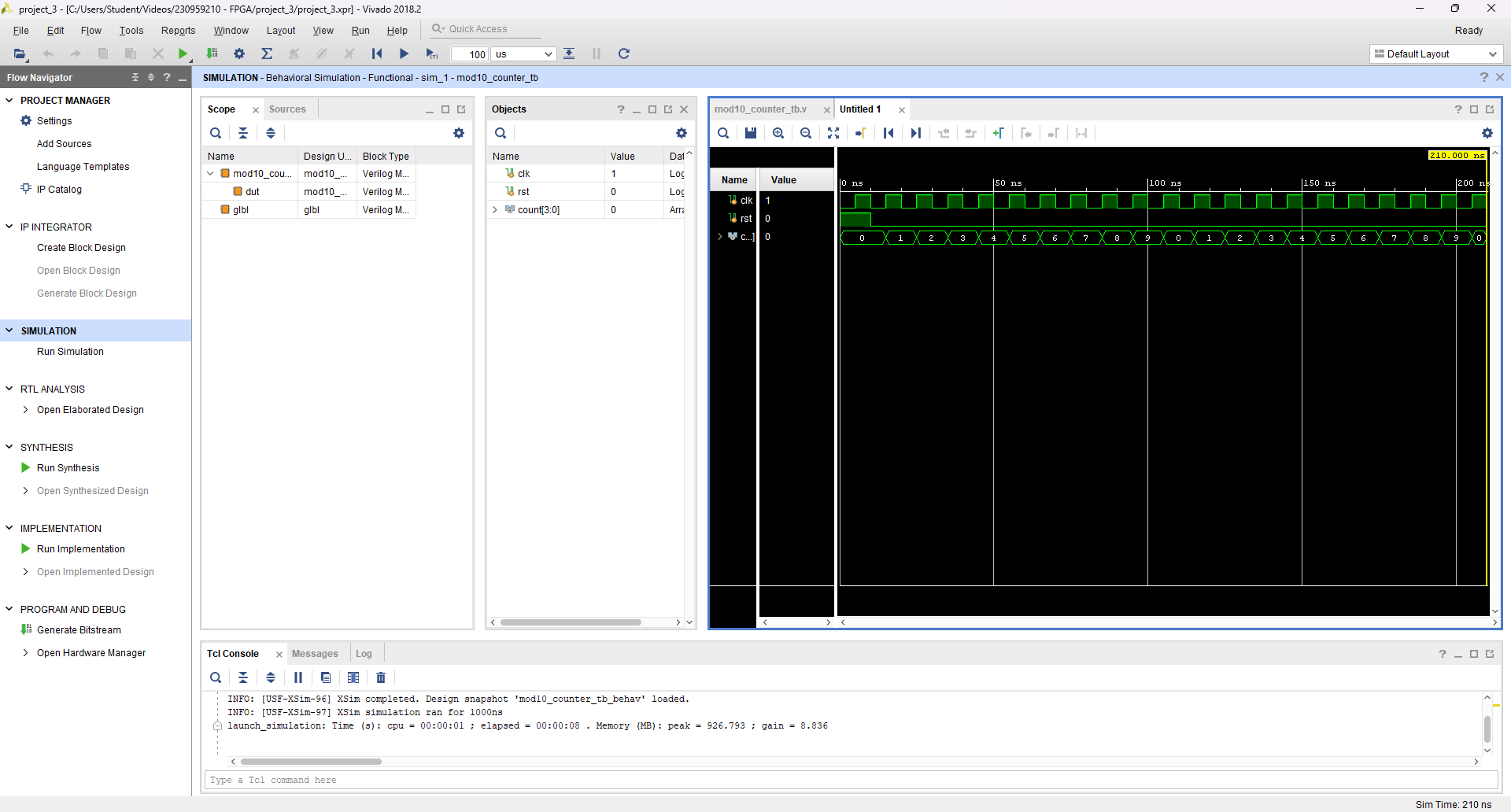
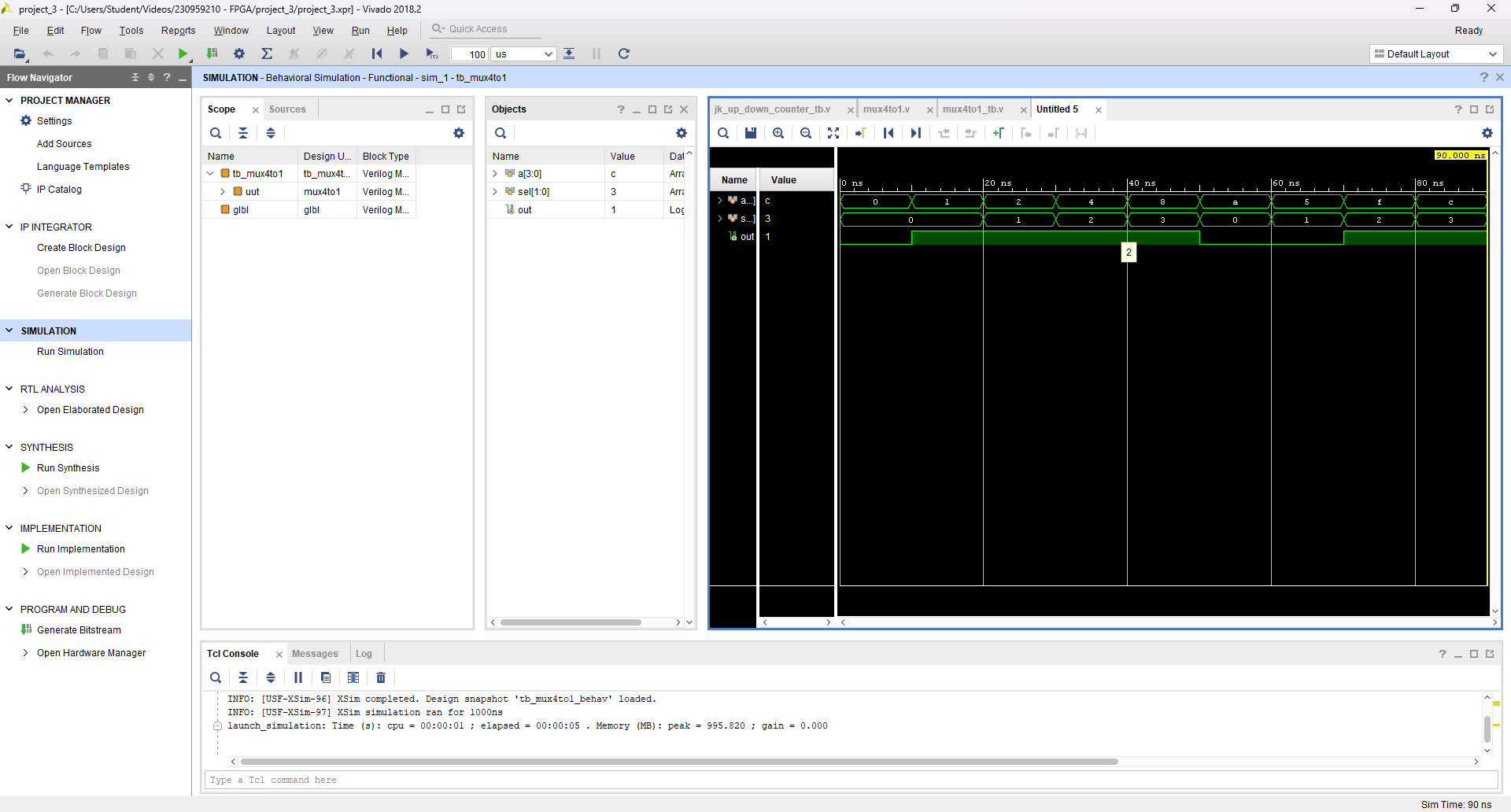
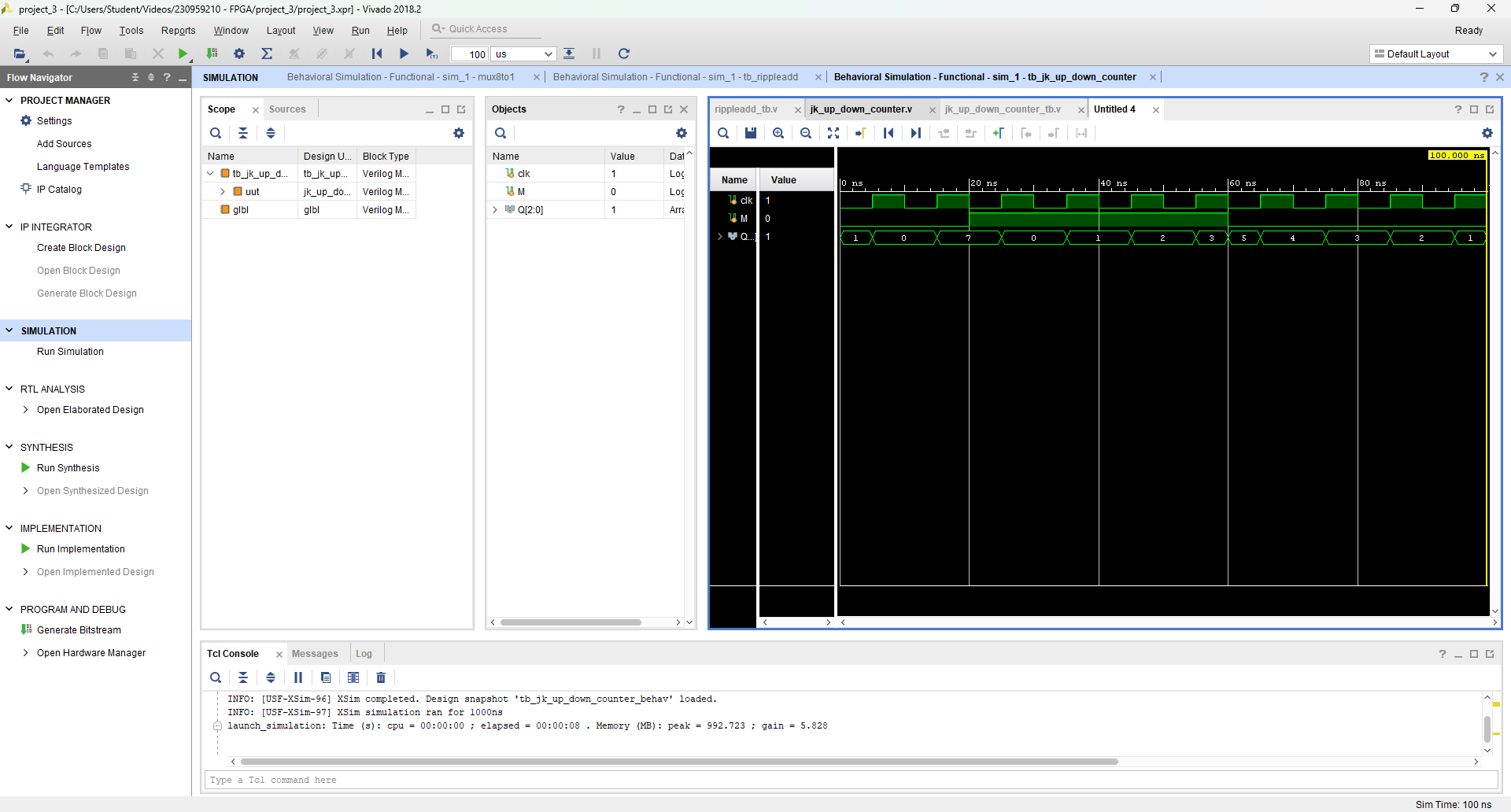
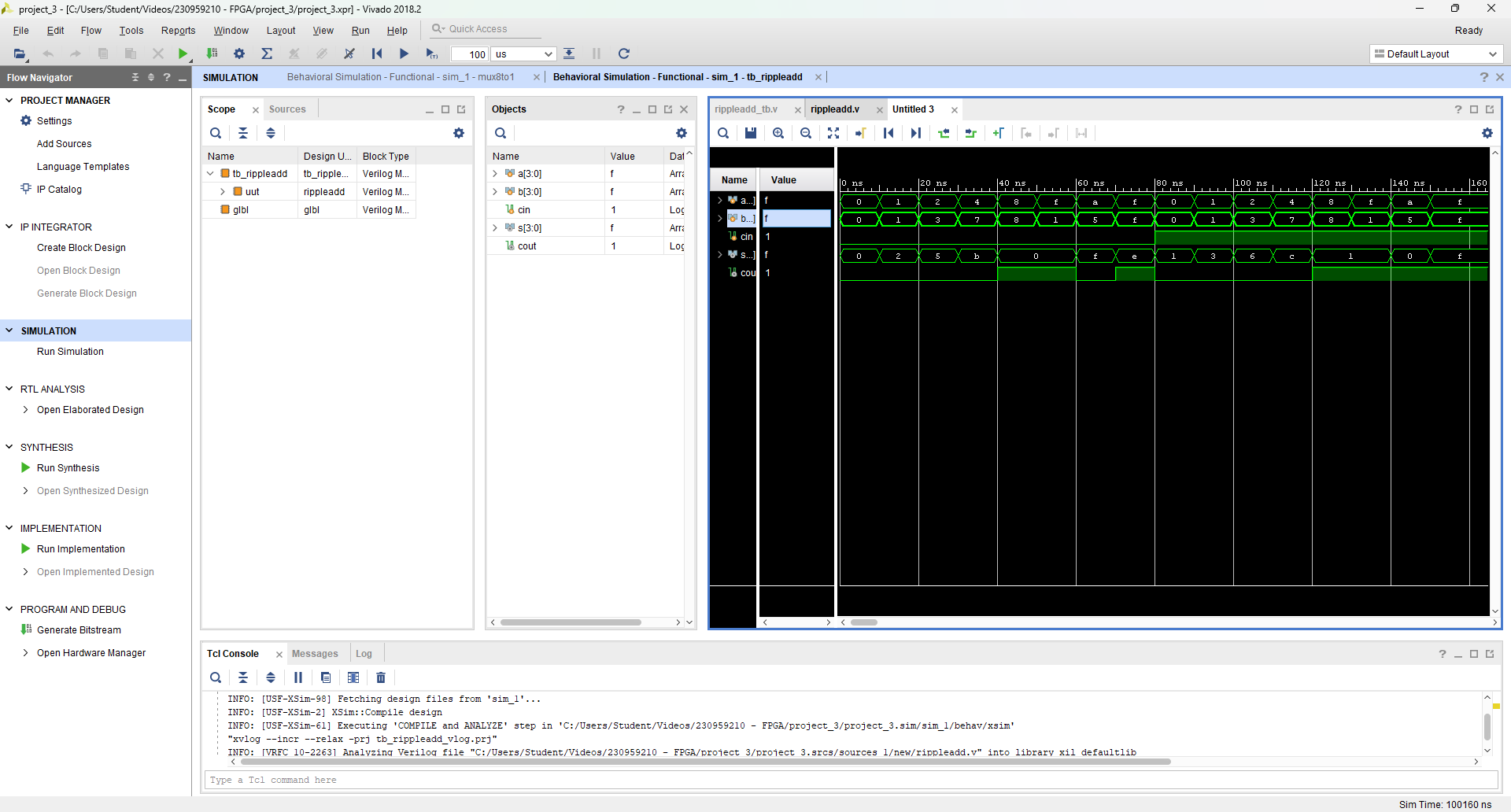
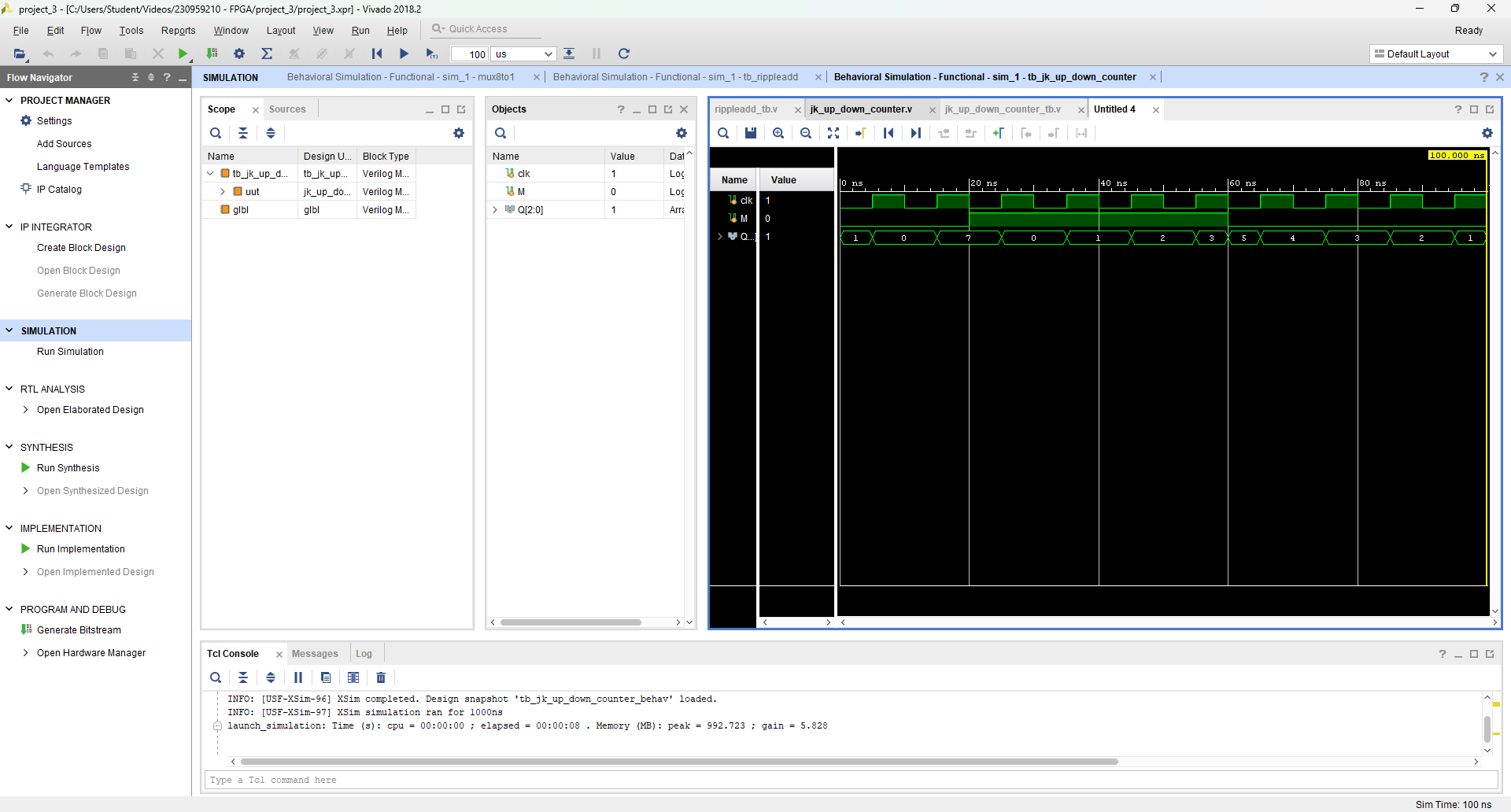
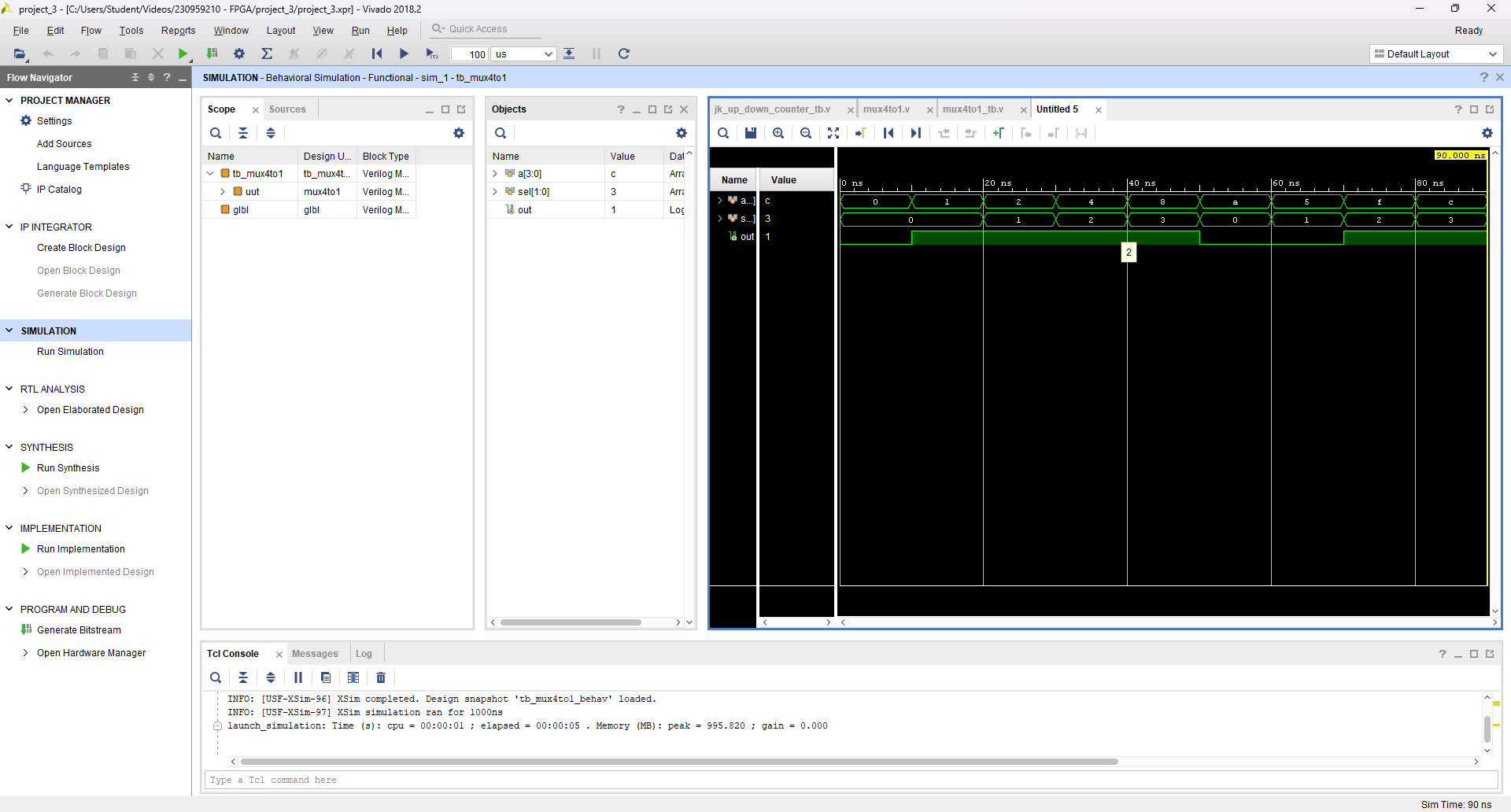
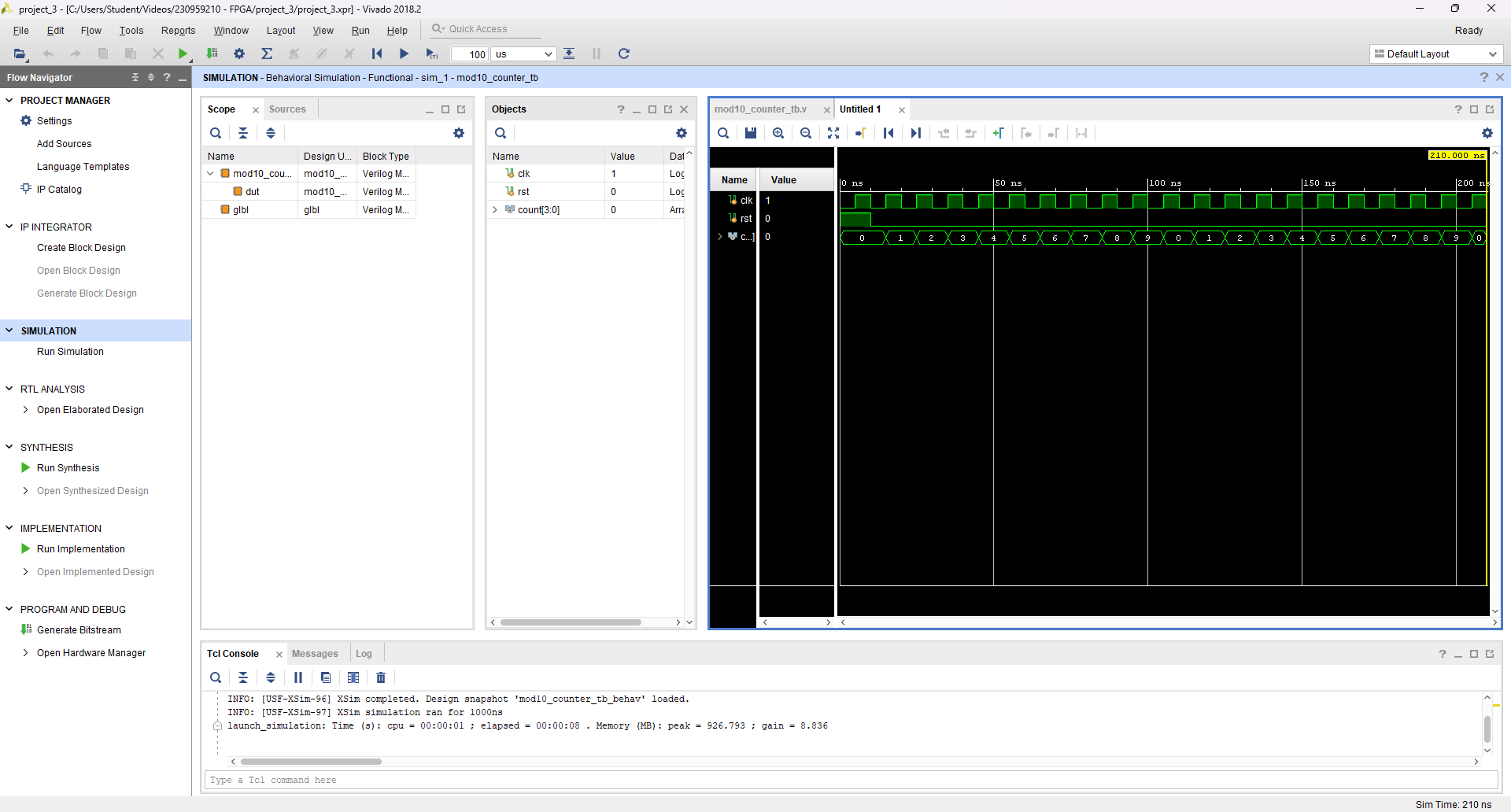
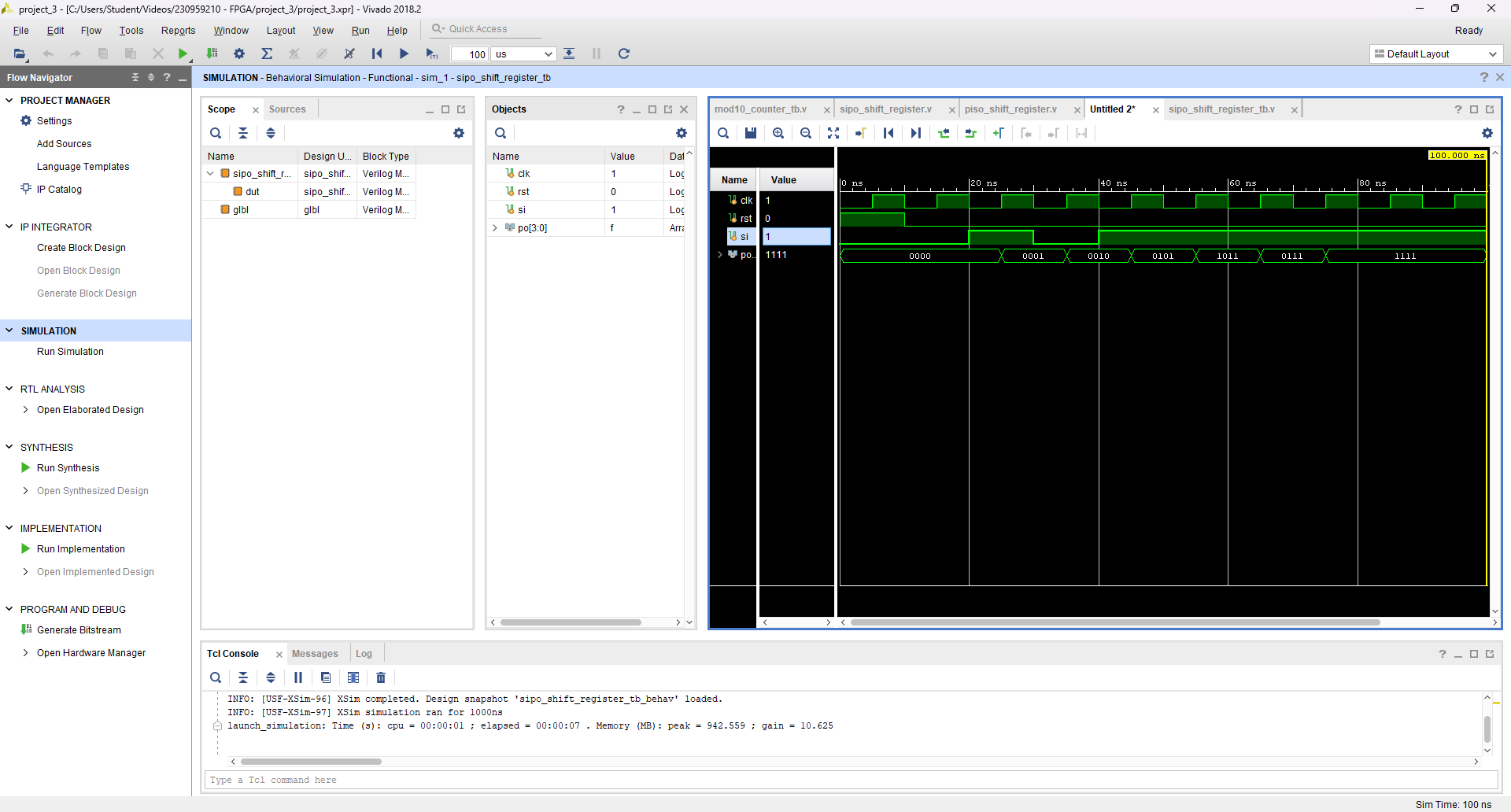
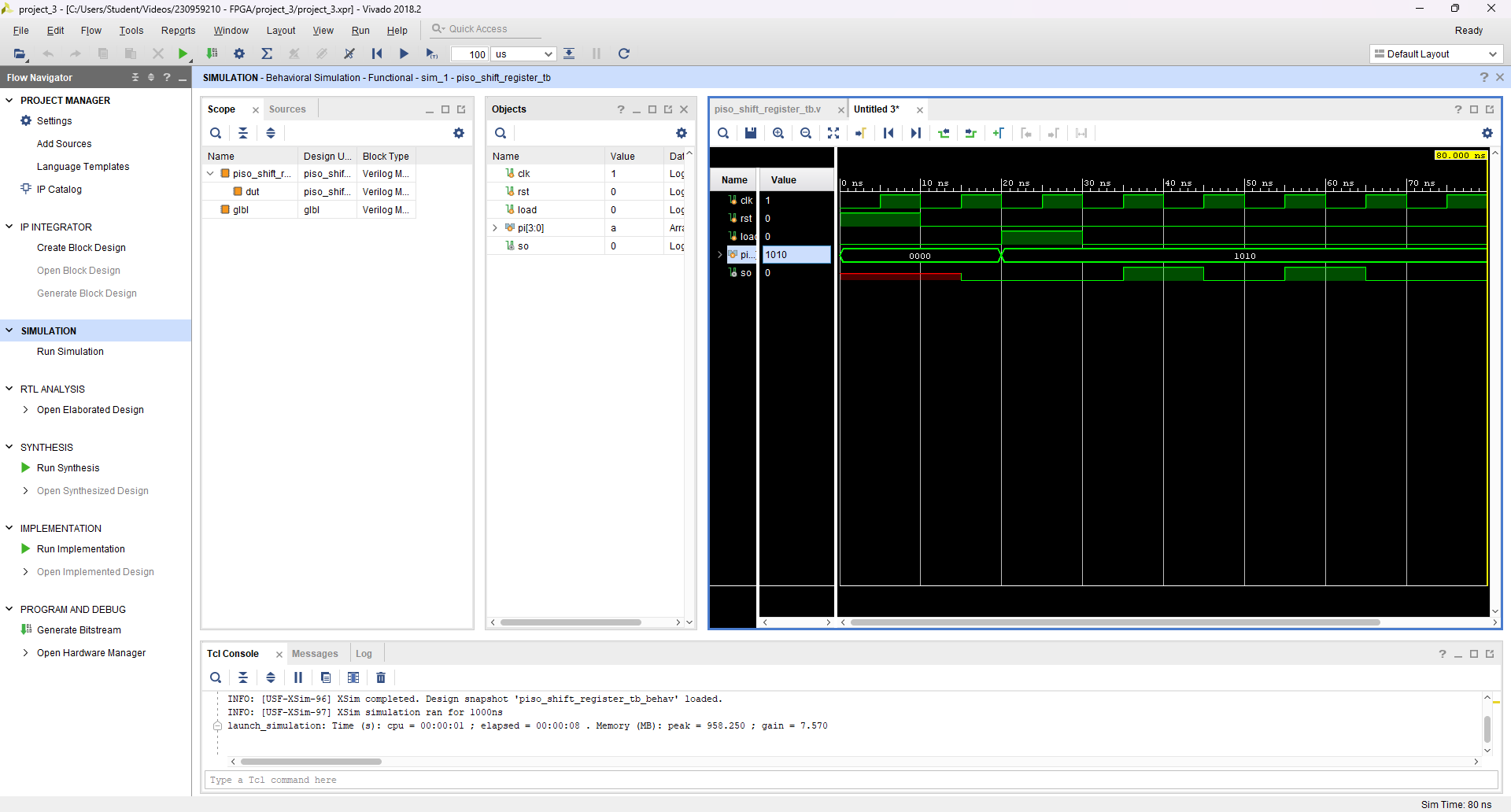
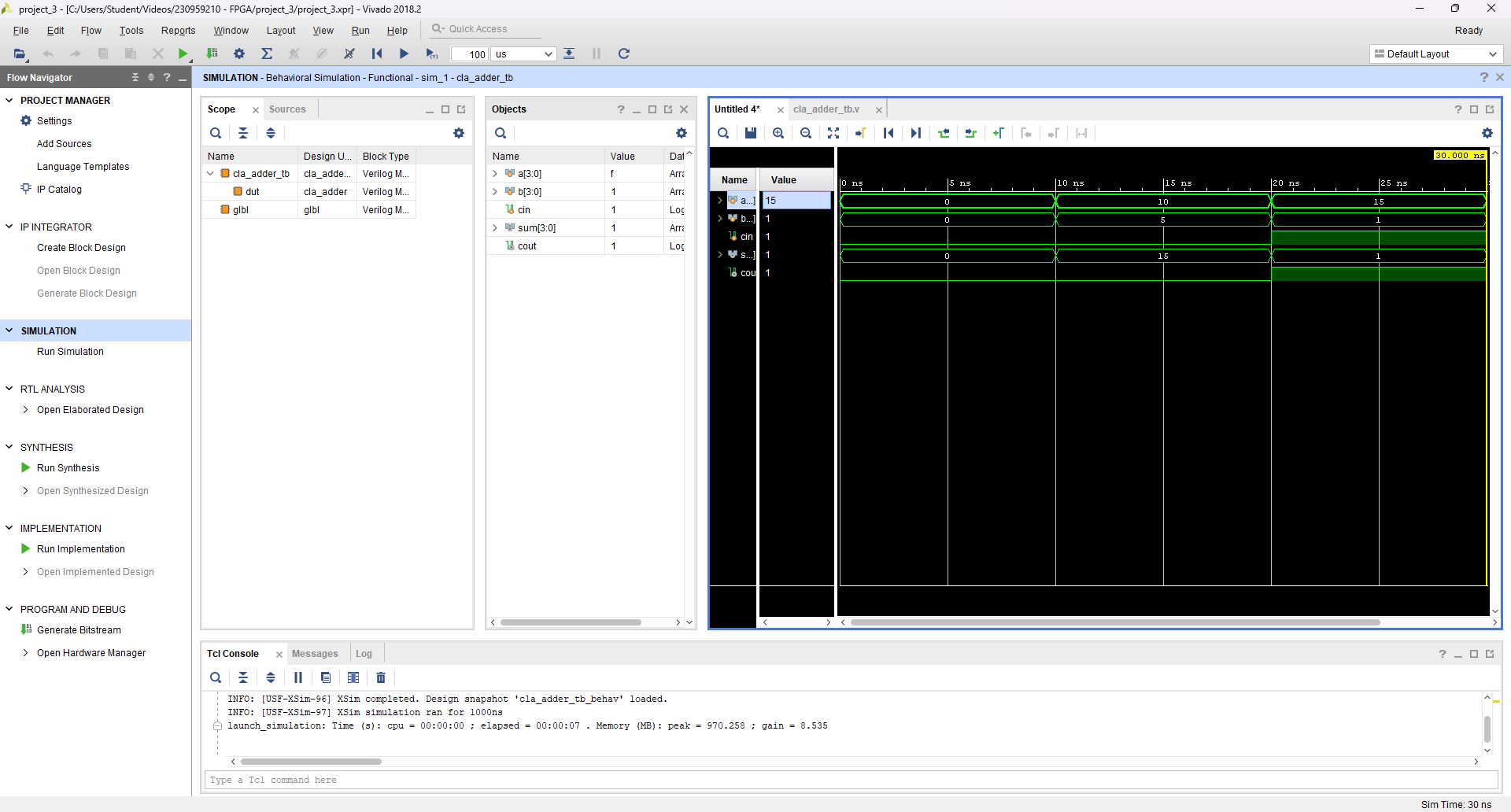
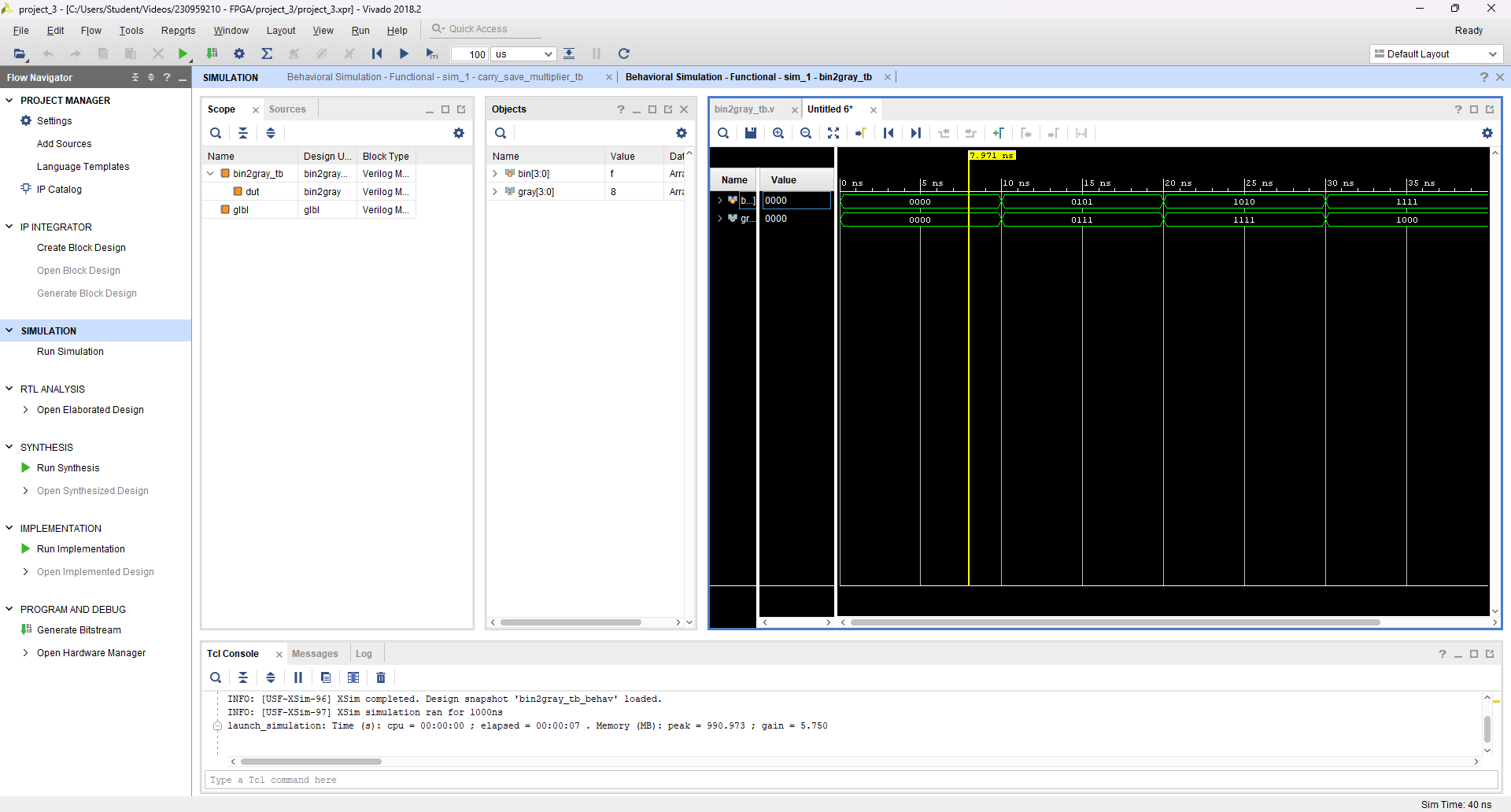
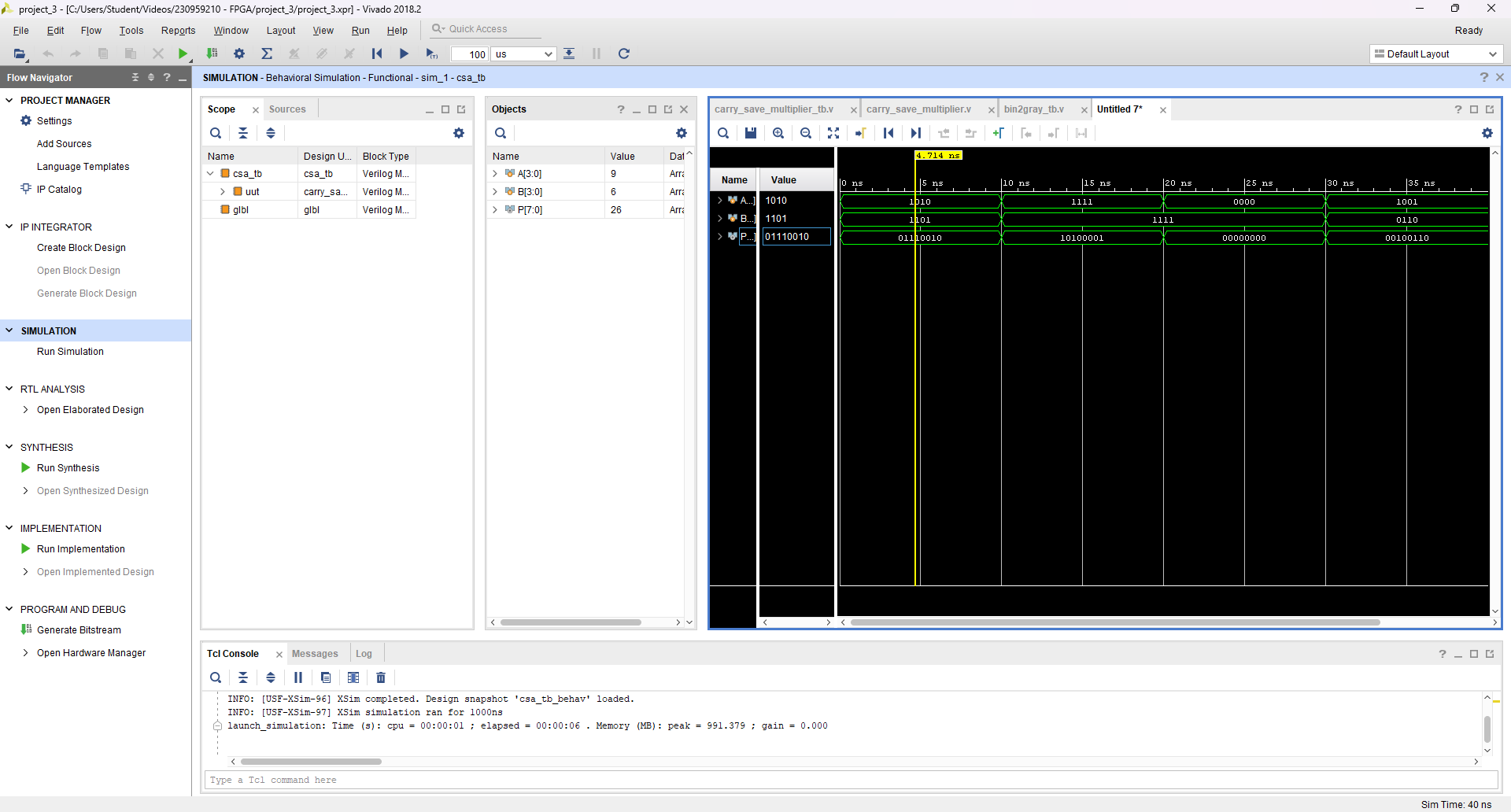
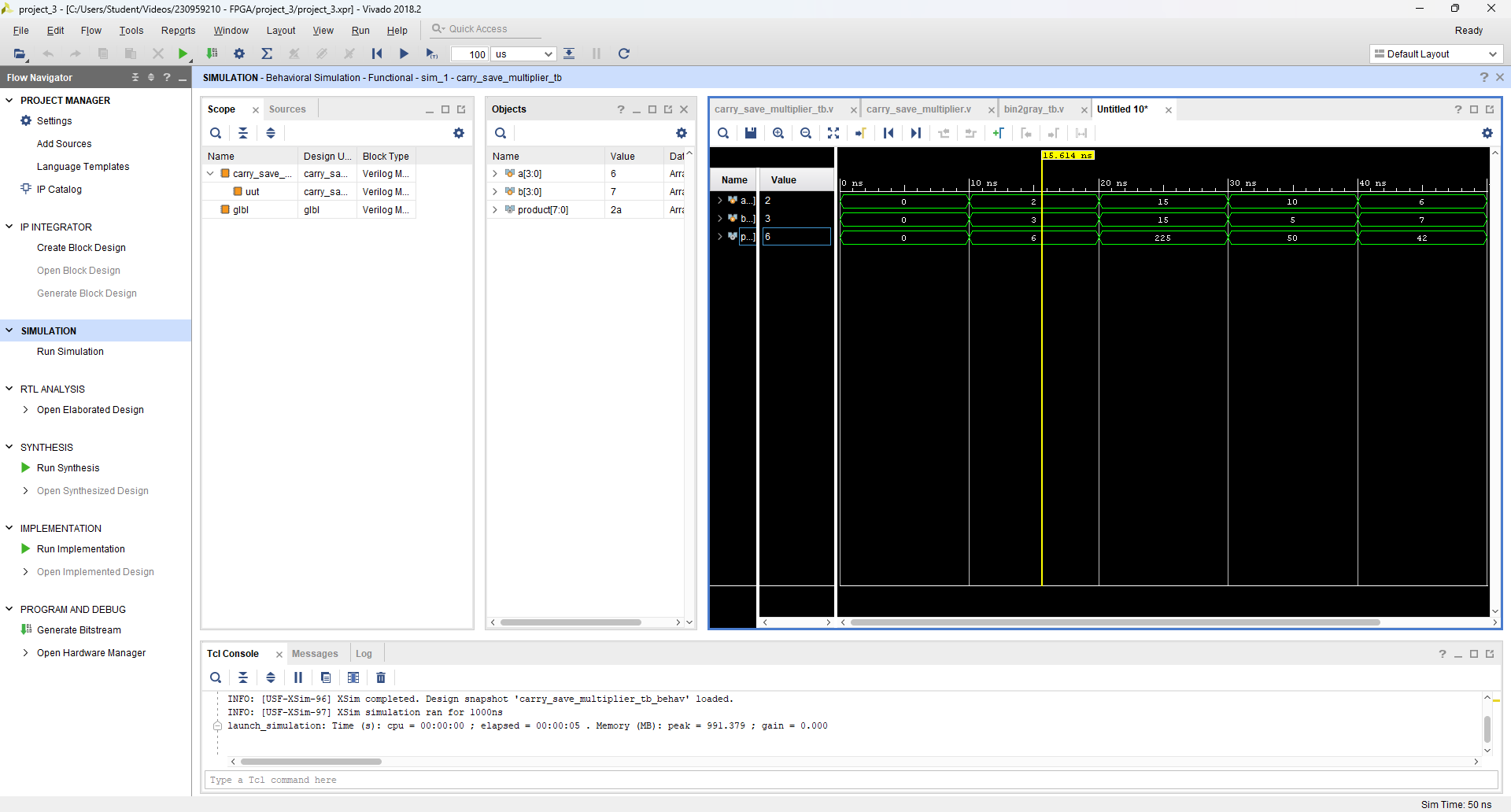
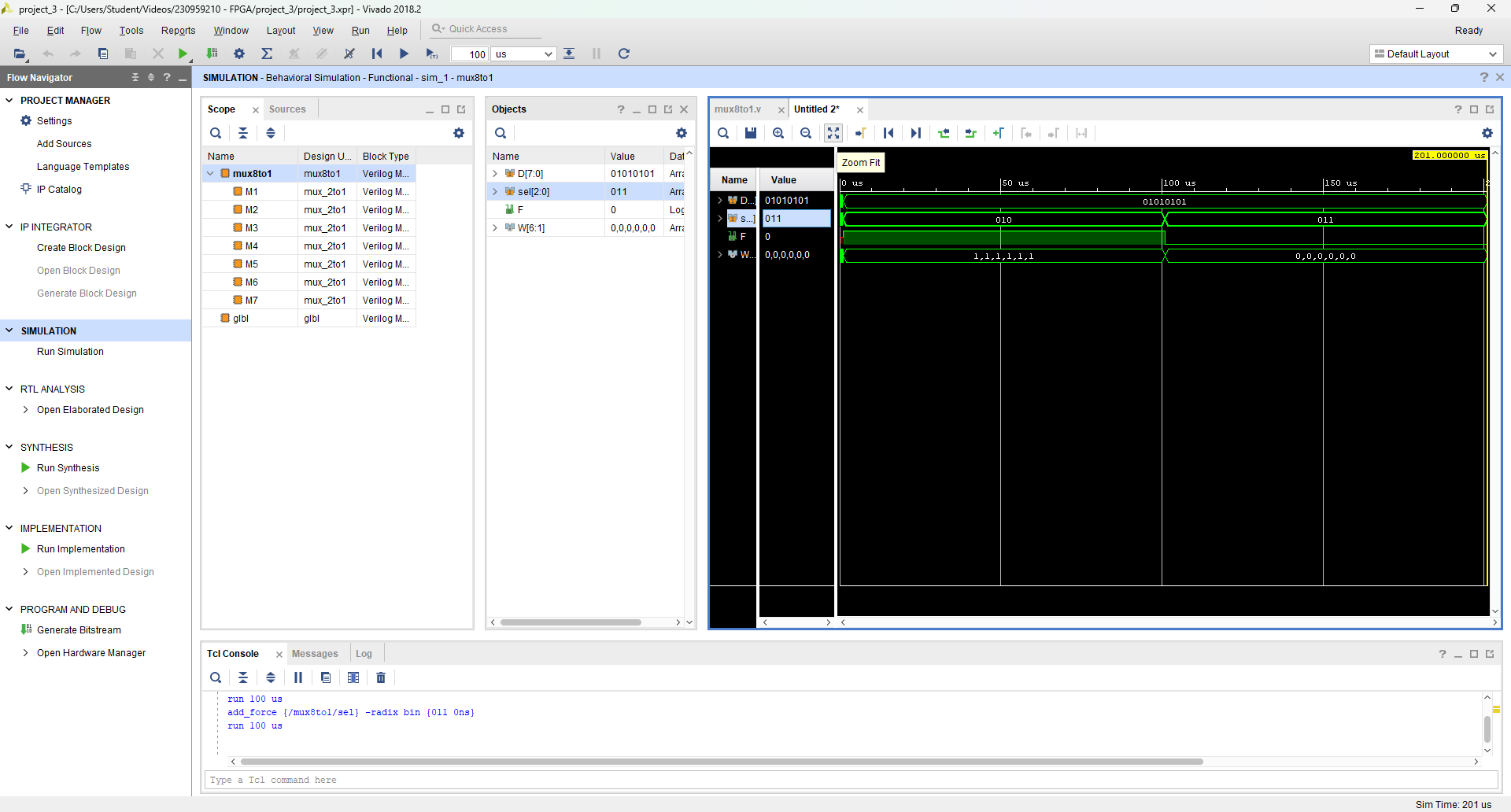
**Experiment 2: Verilog Dataflow Modelling**

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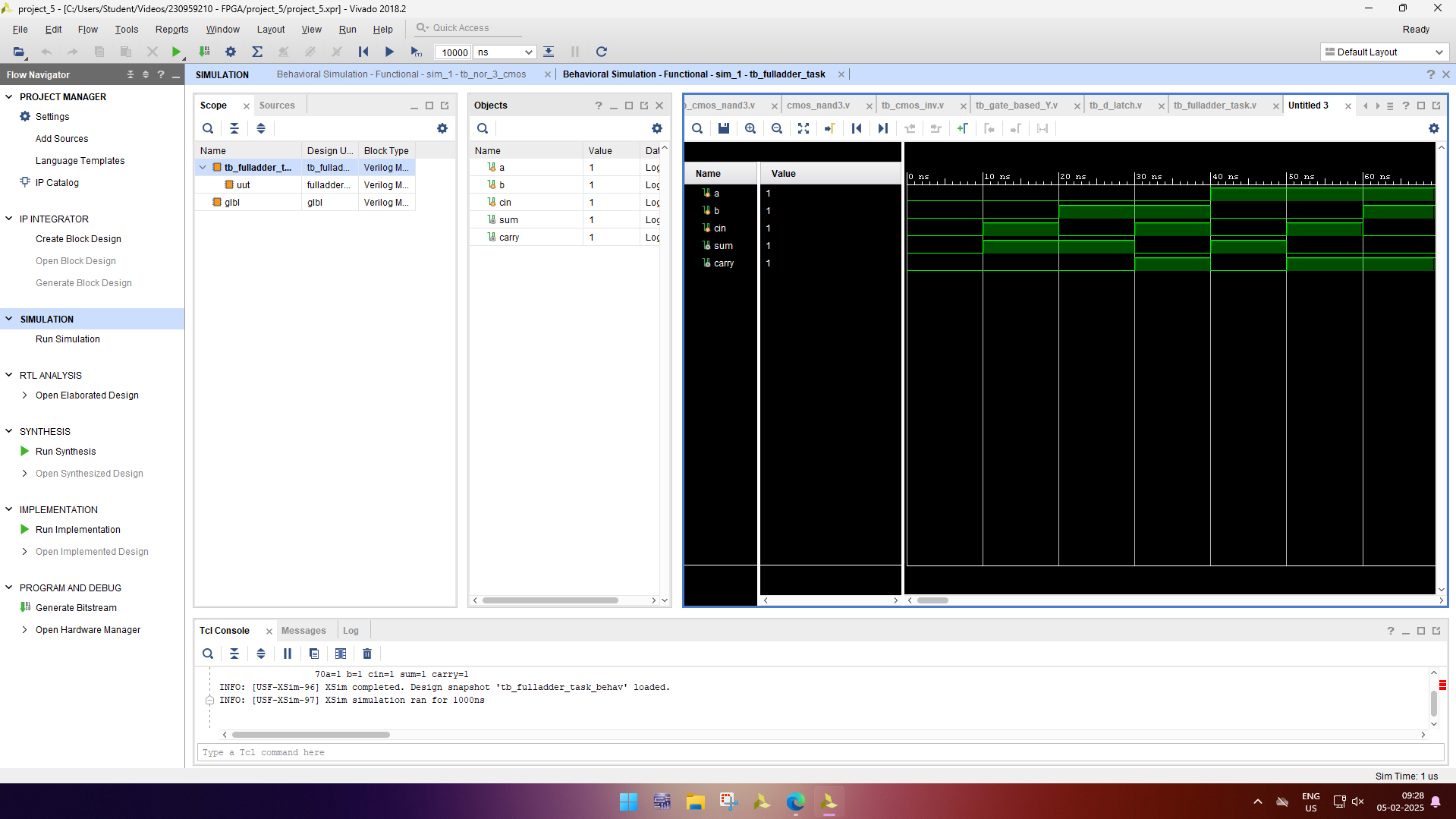
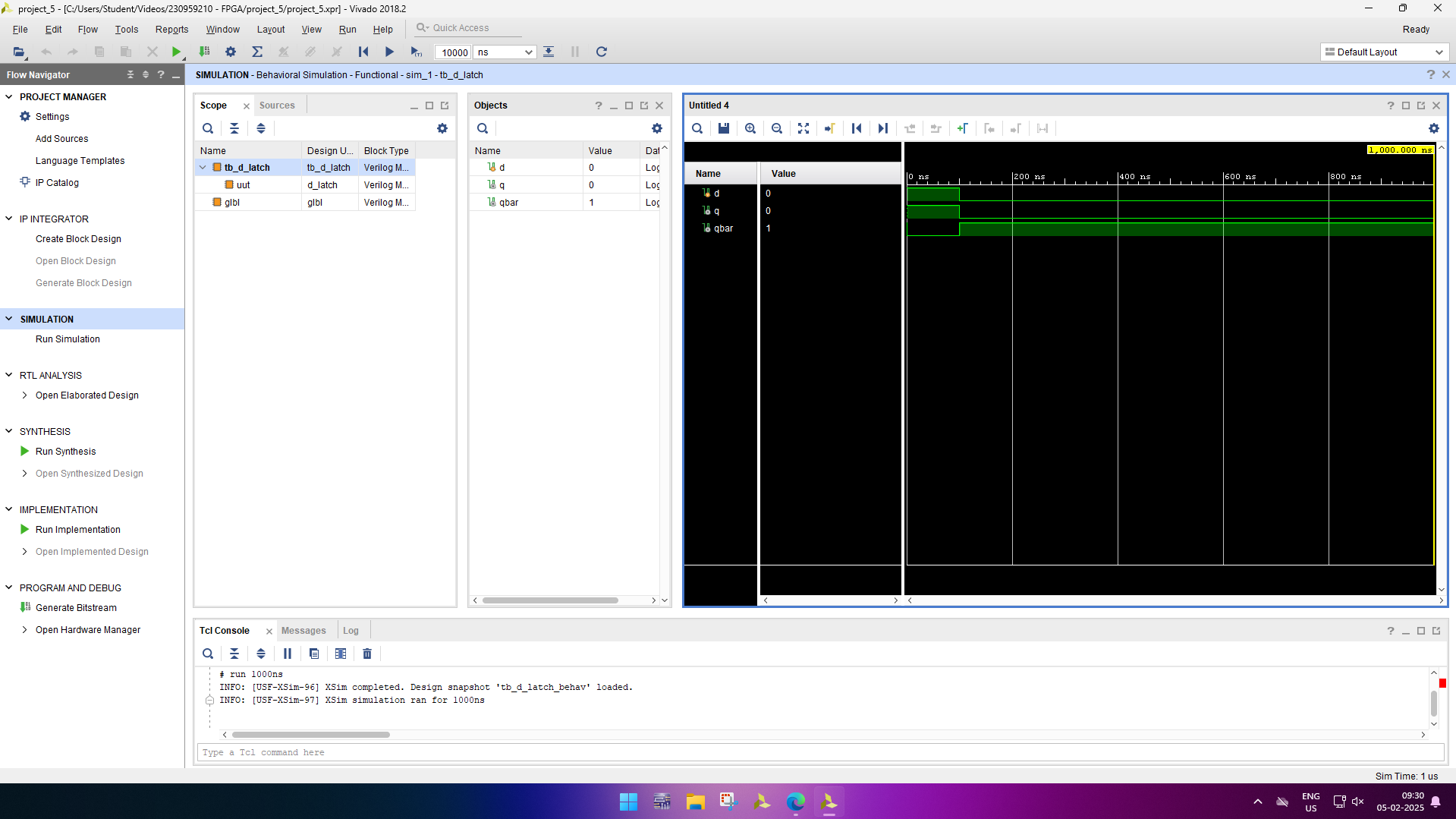
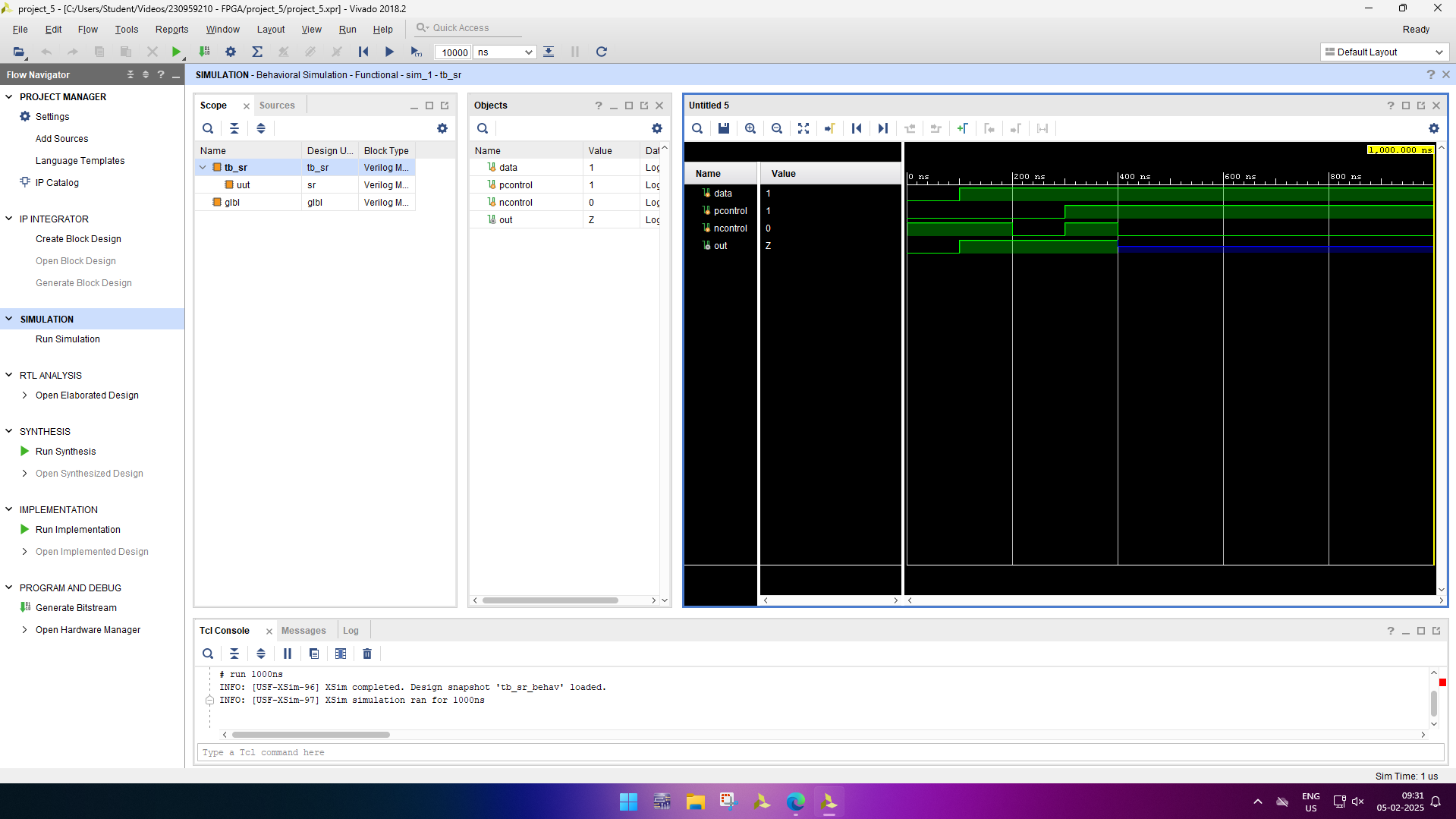
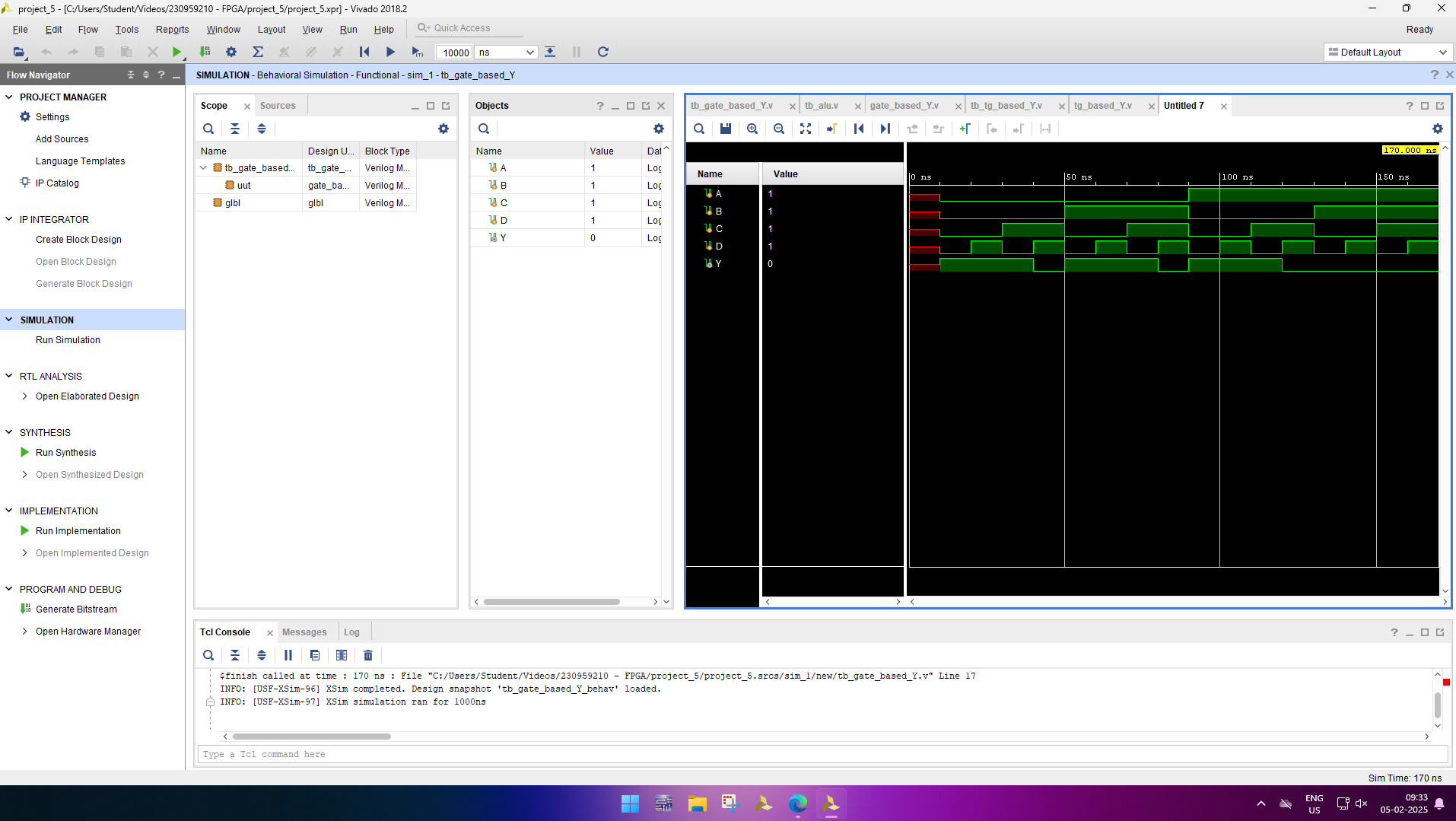
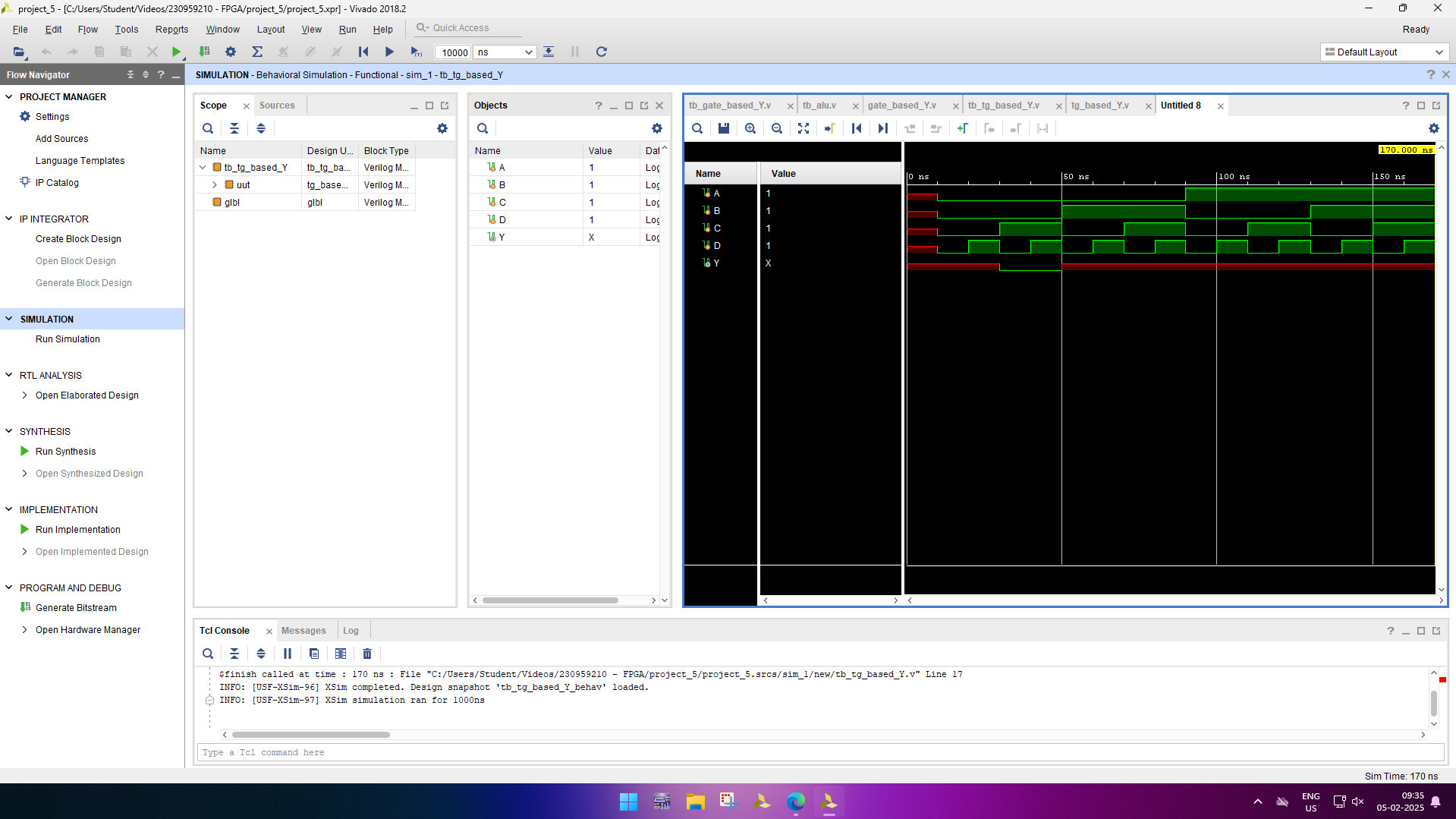
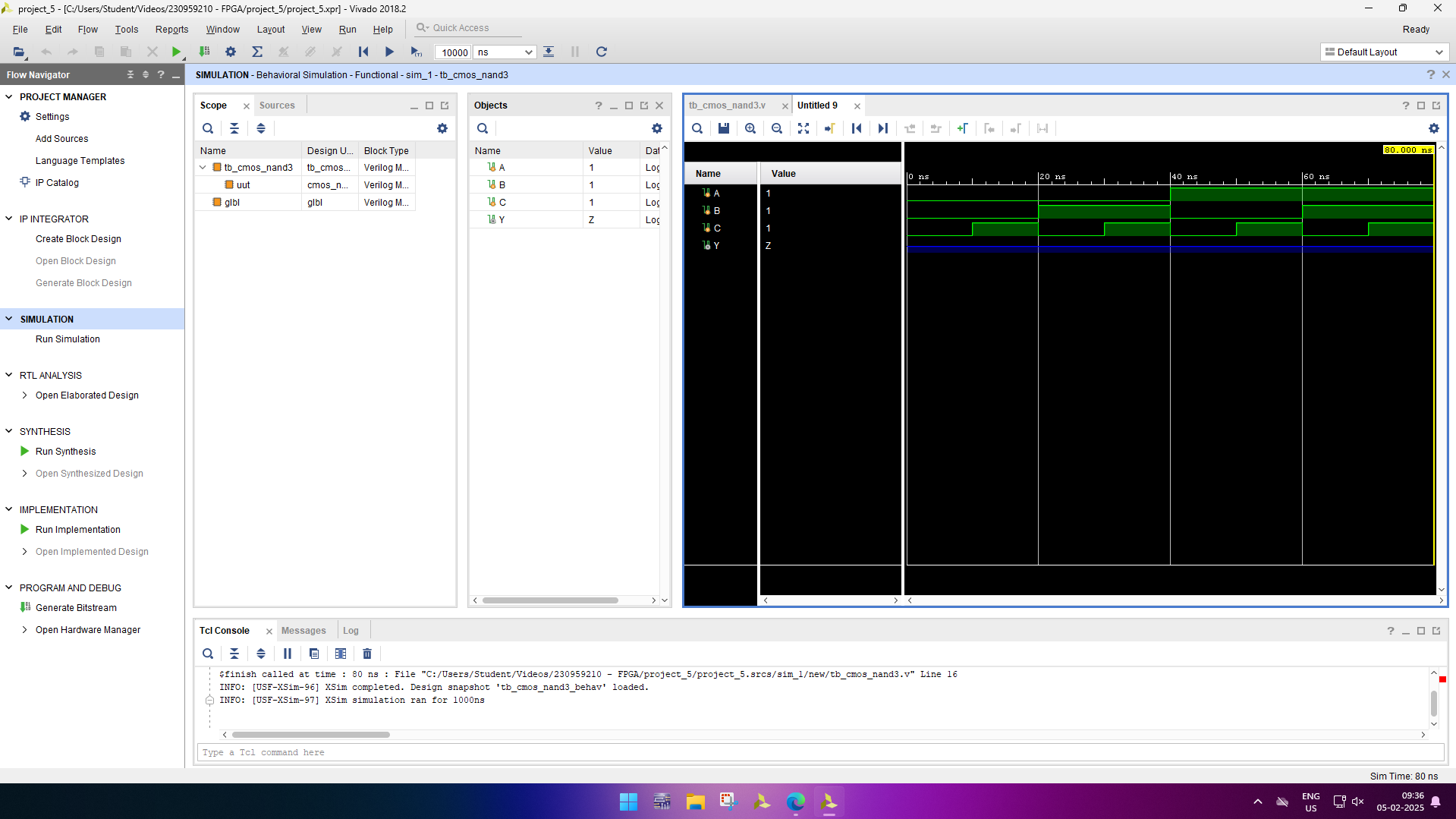
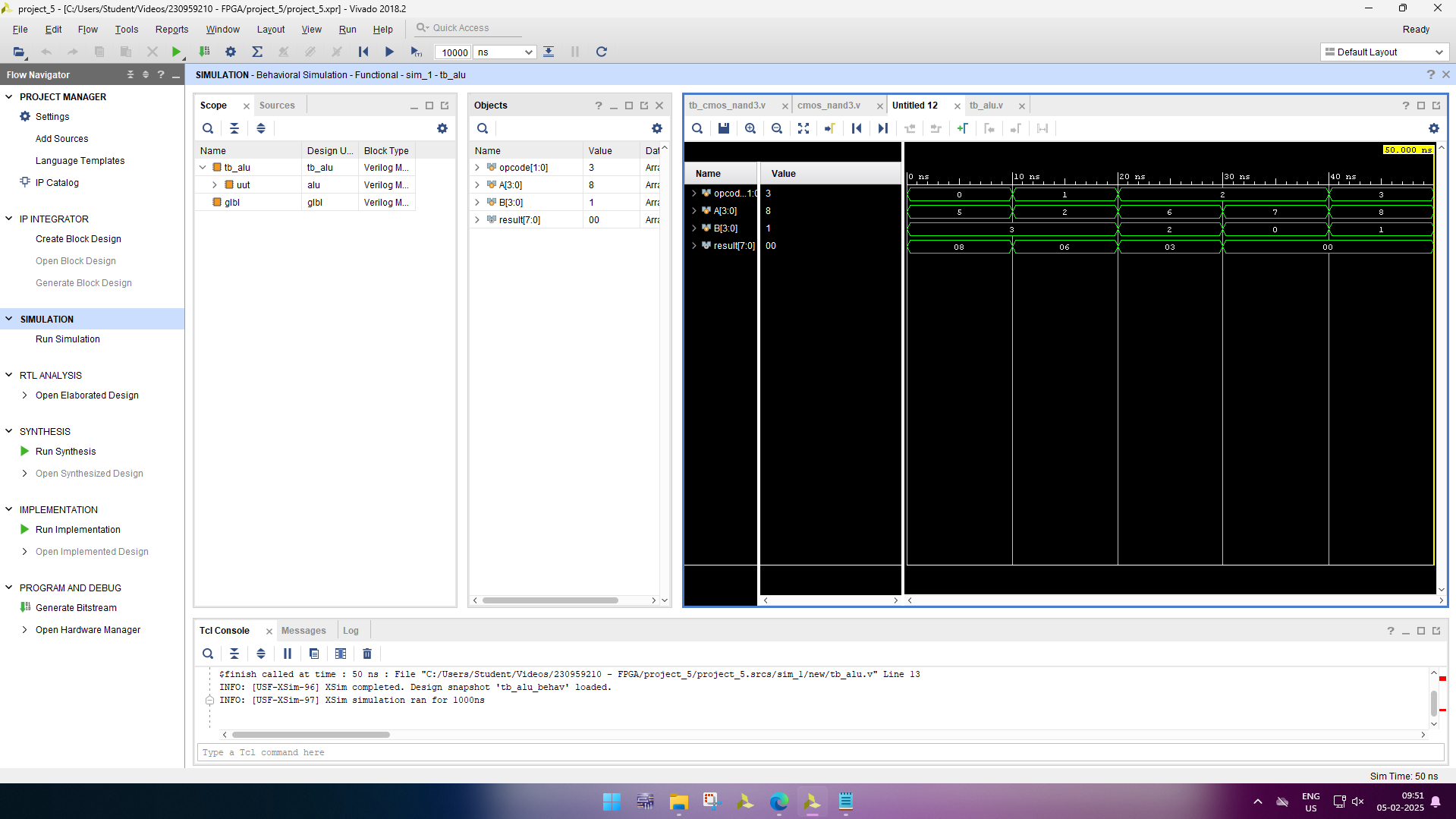
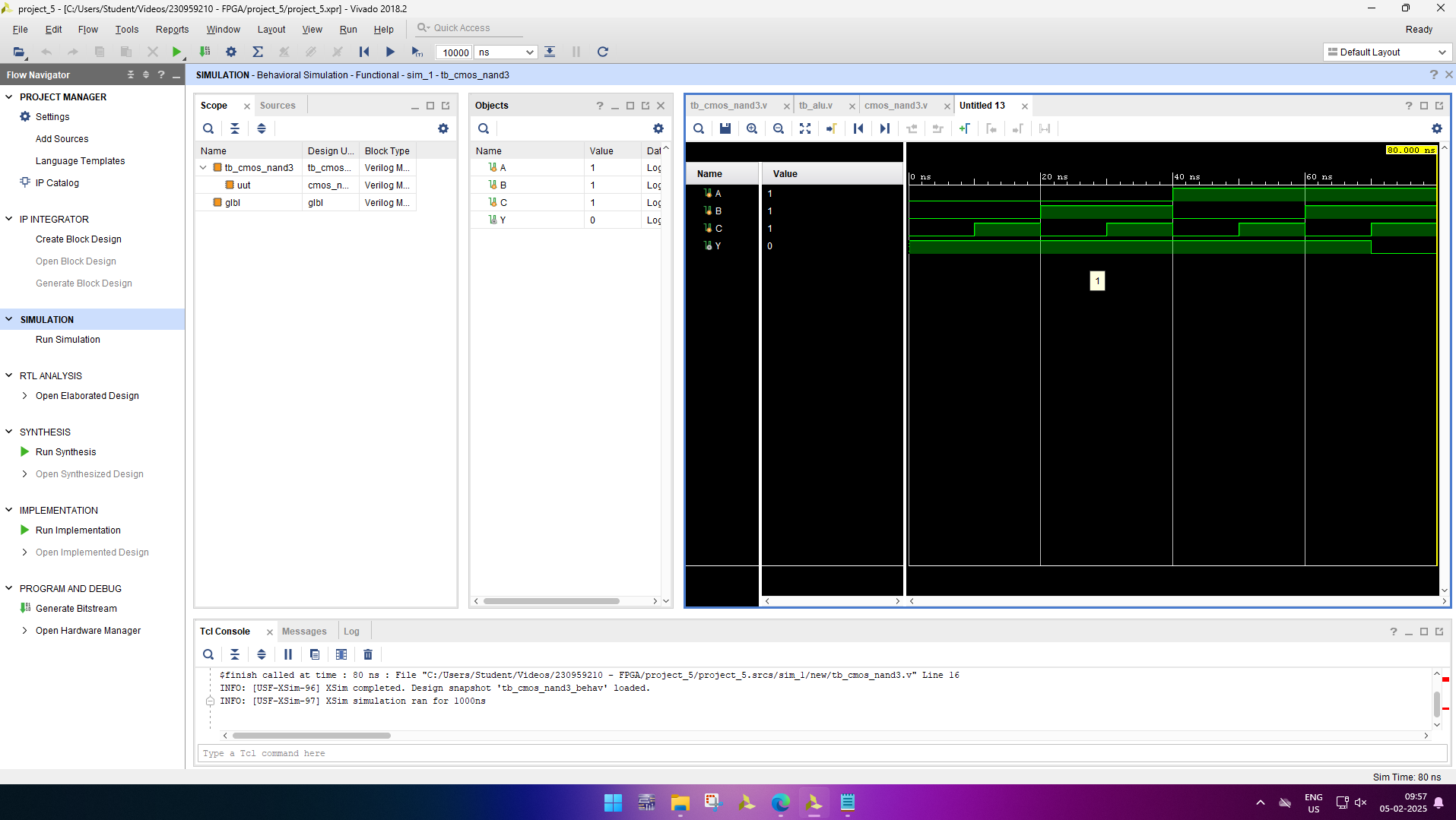
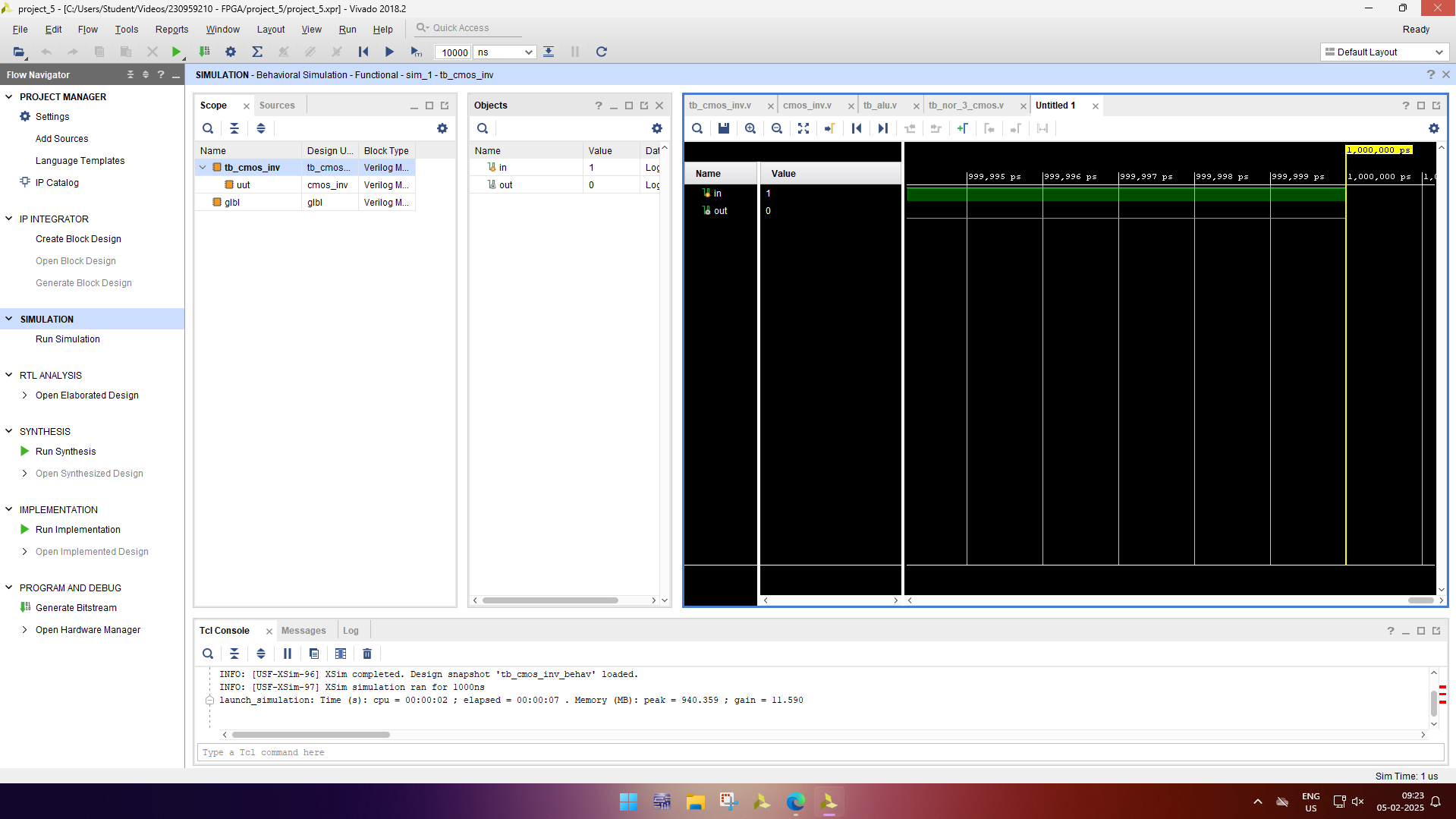
**Experiment 3: Verilog Sequential Modelling**

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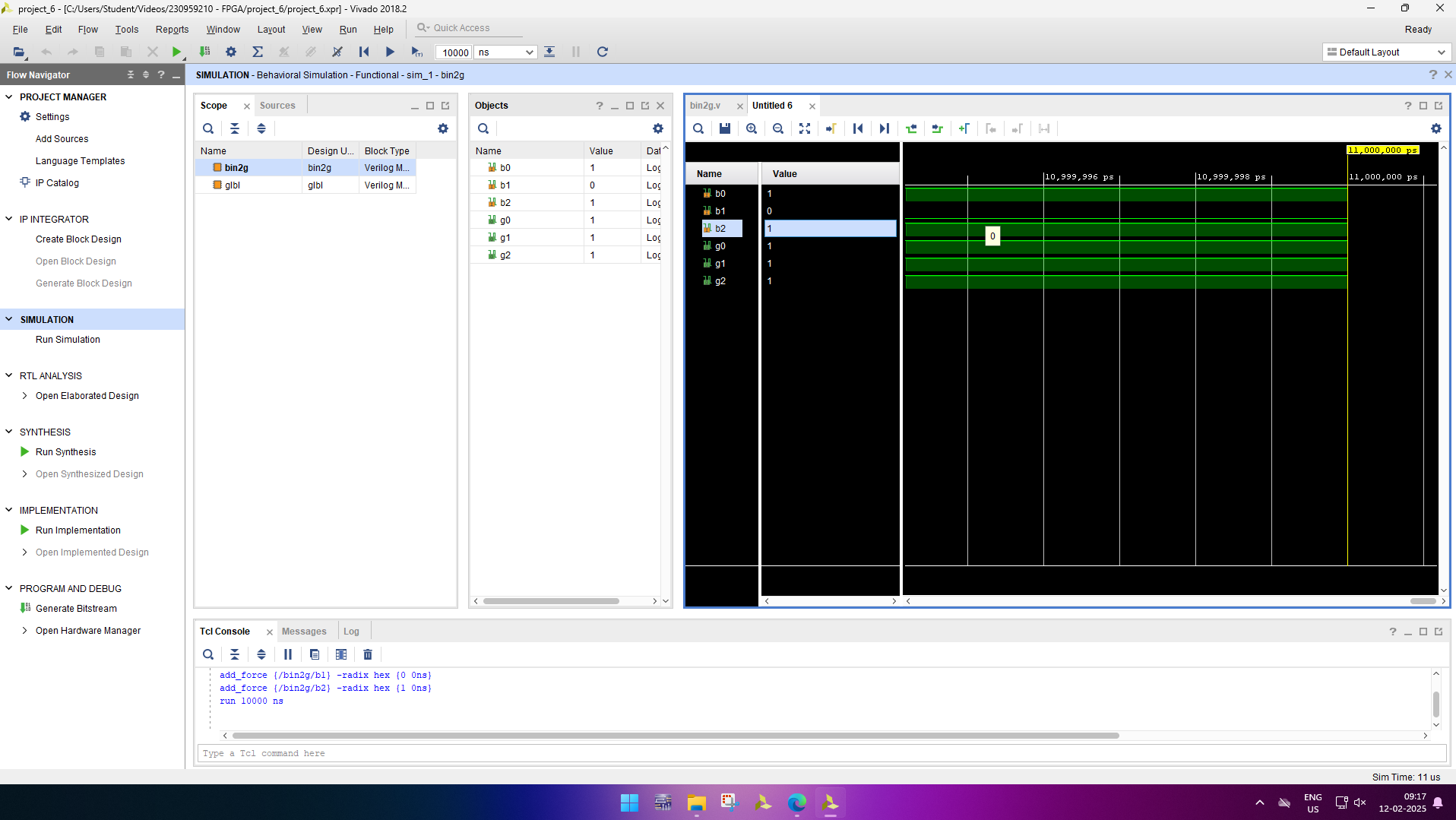
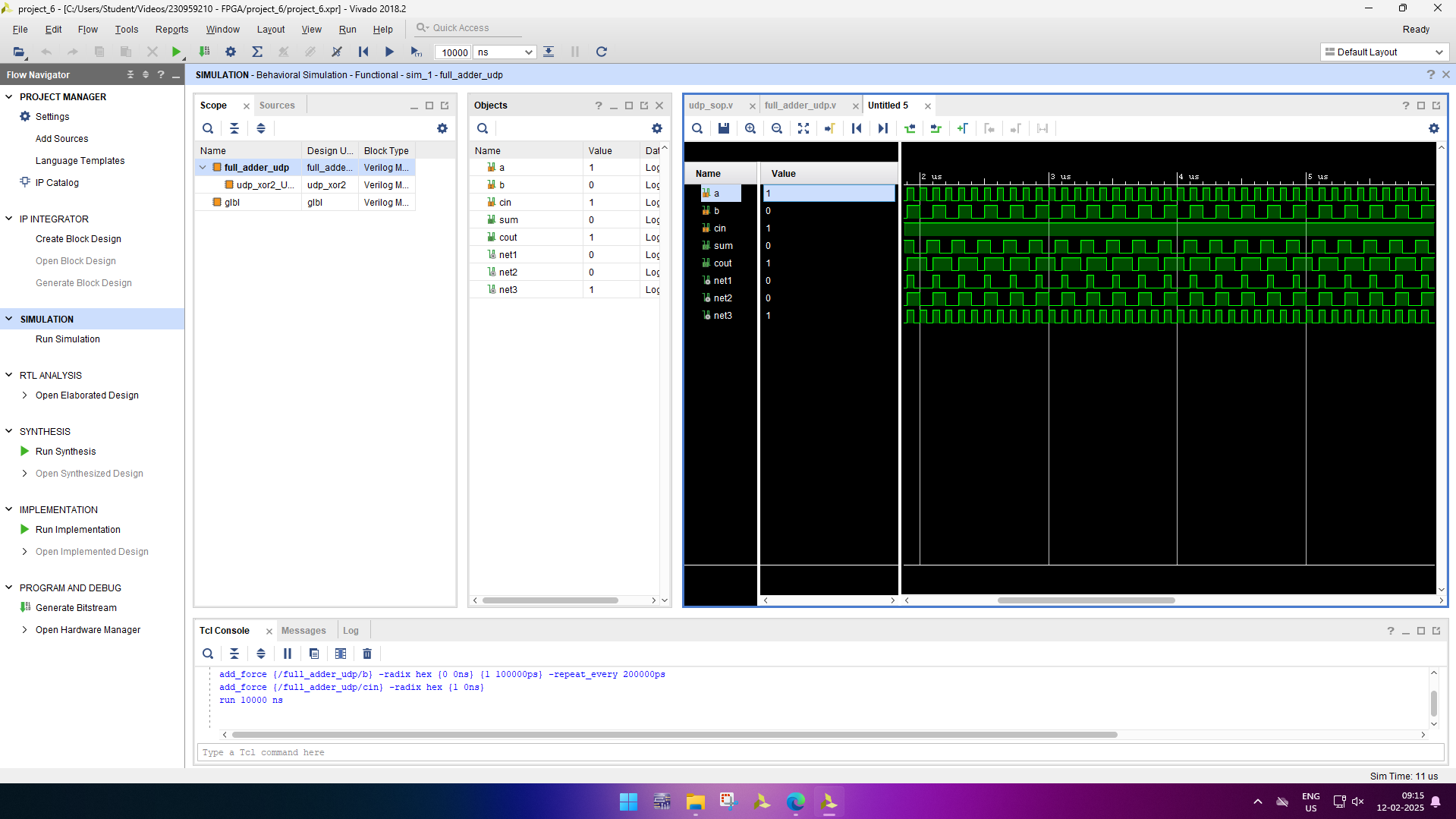
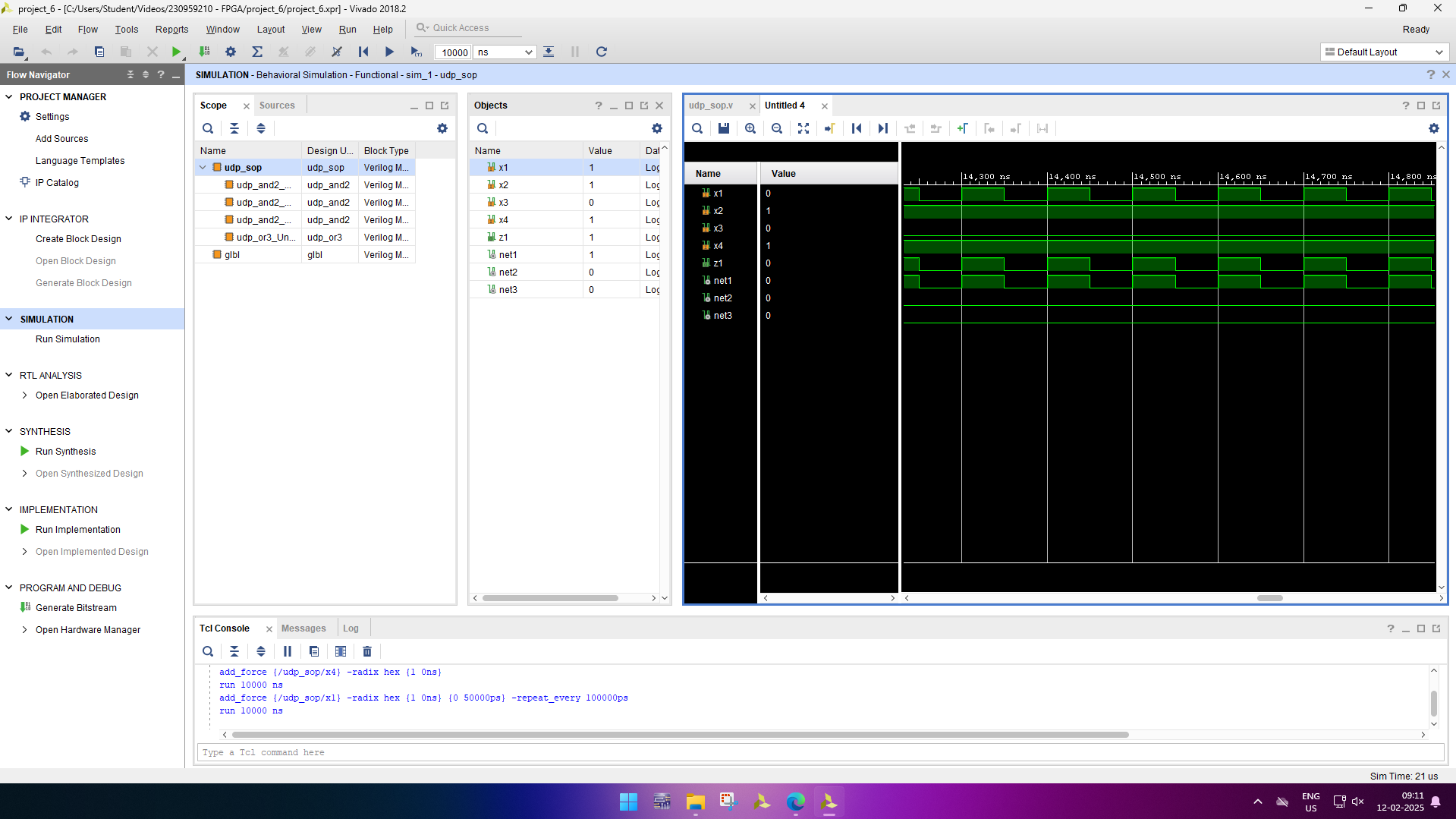
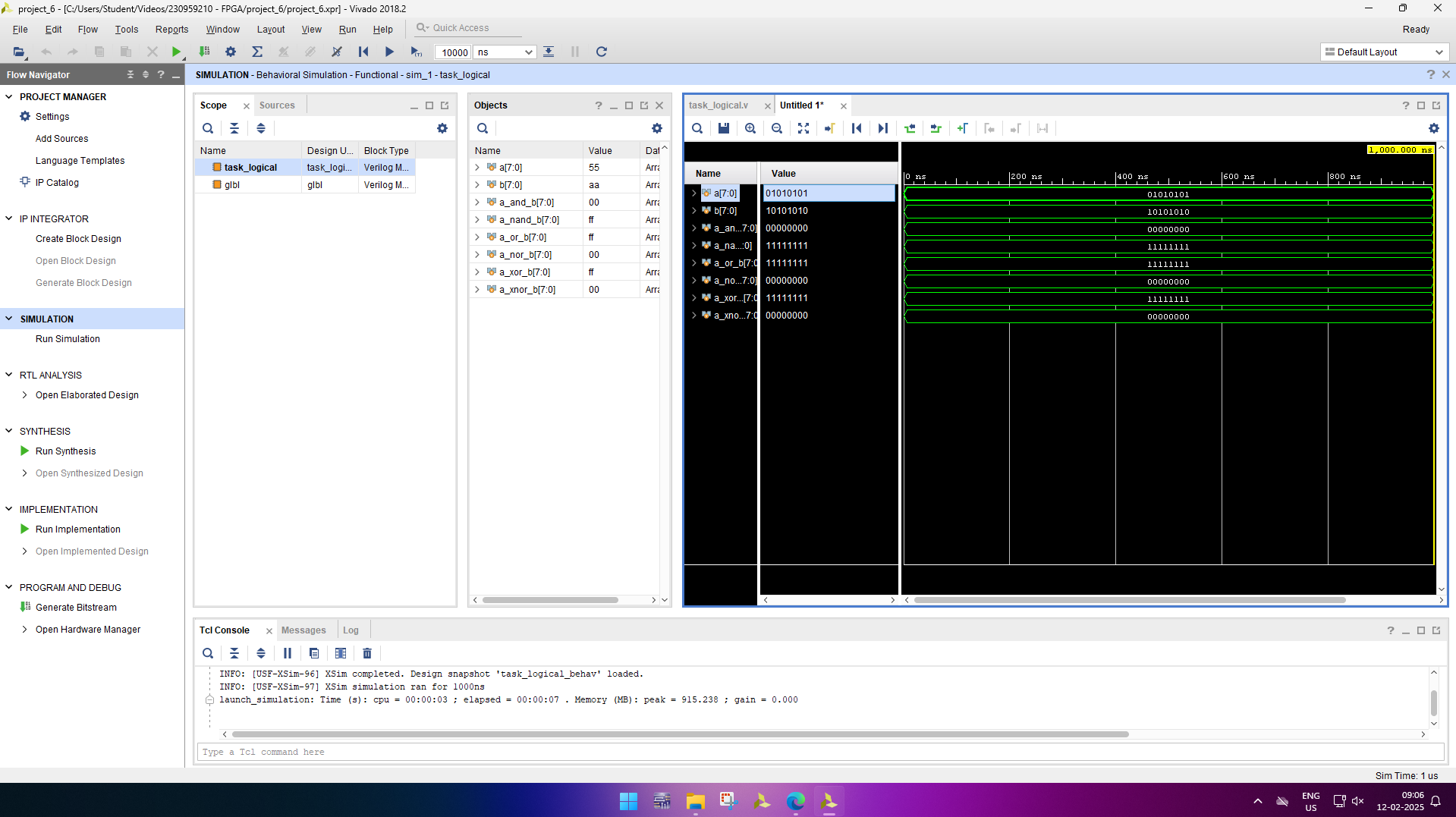
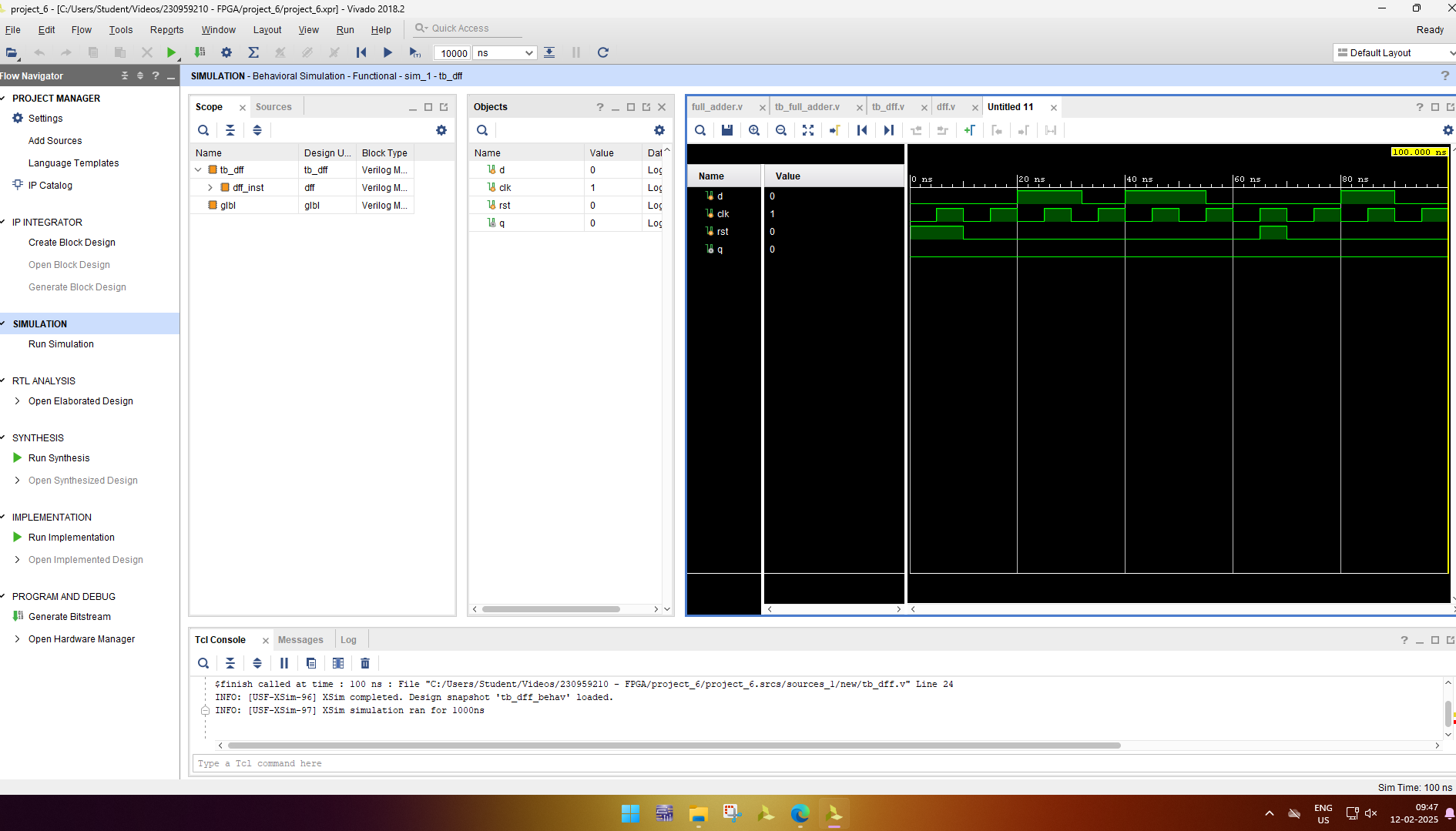
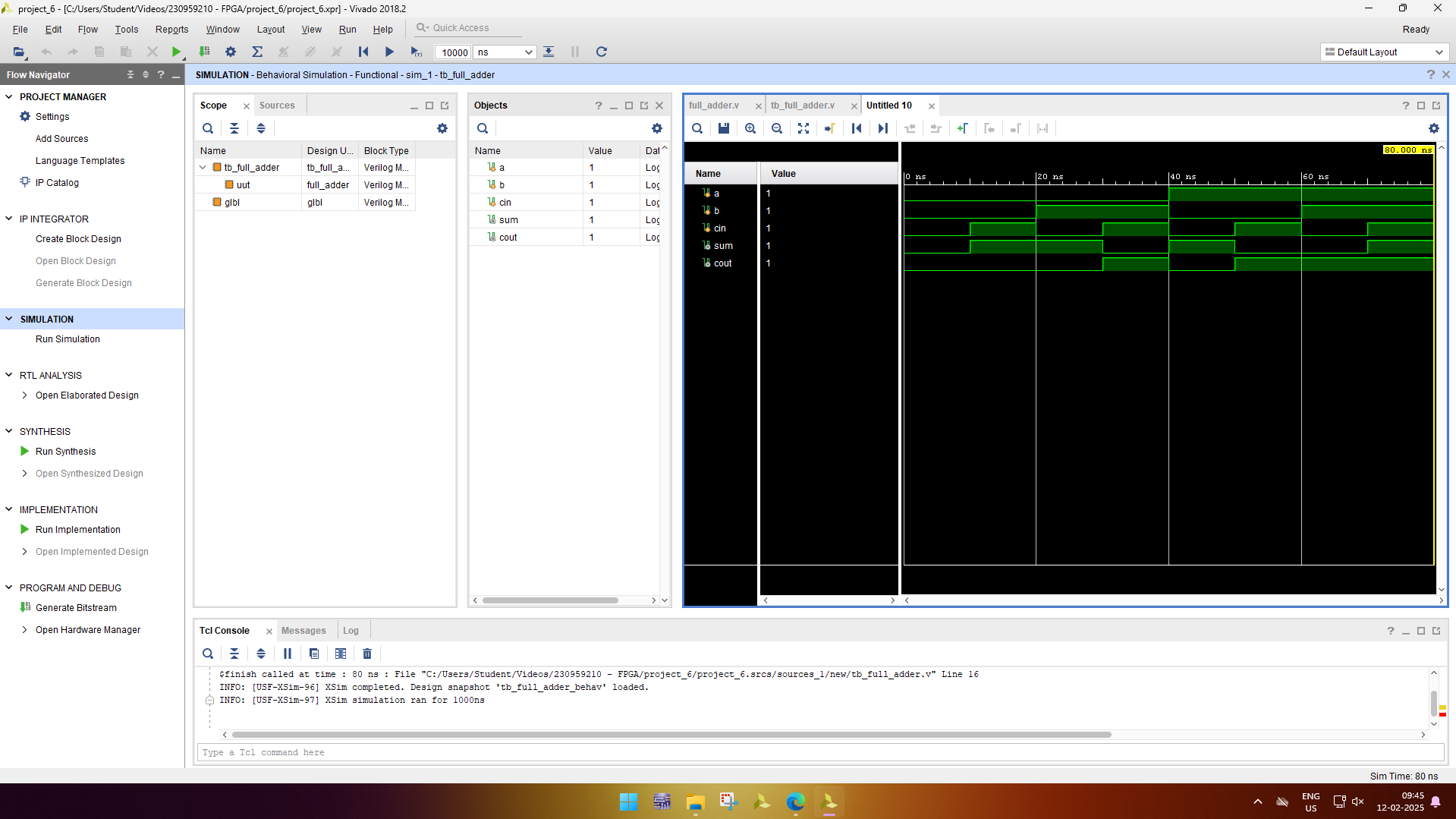
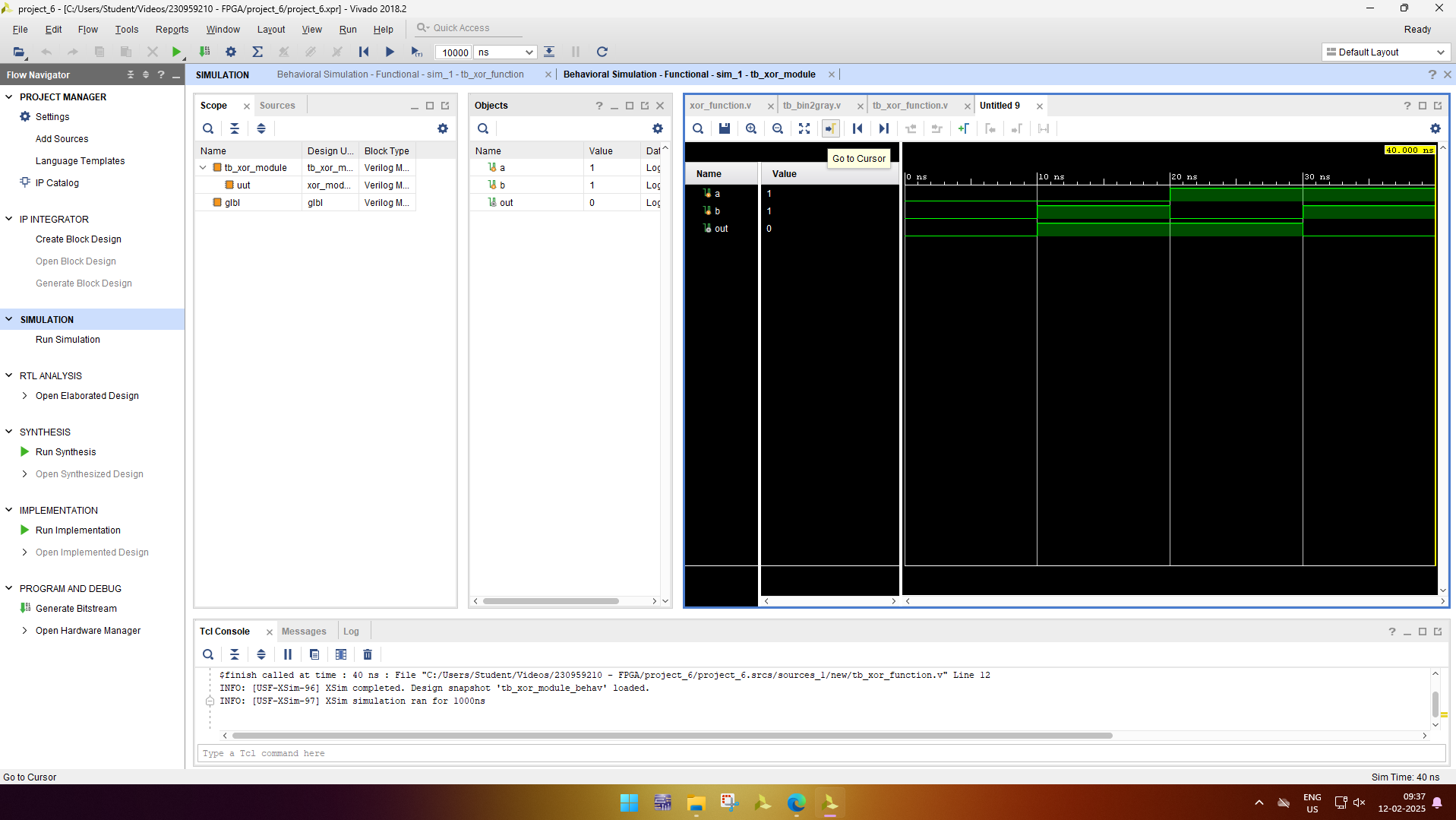
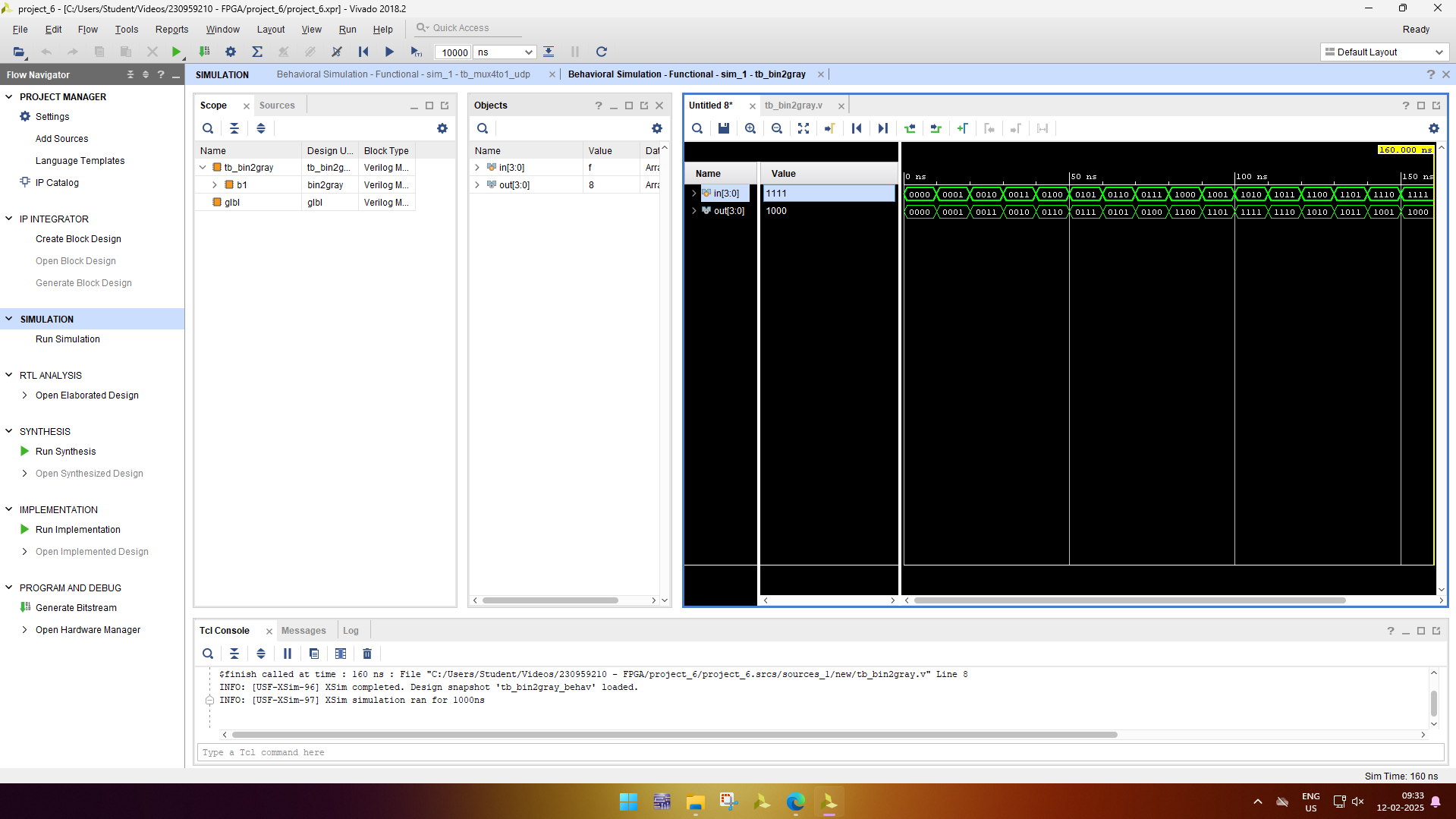
**Experiment 4: Verilog Structural Modeling**

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**Experiment 5: Verilog Switch Level and Mixed-mode Modeling**

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**Experiment 6: Verilog examples using tasks, functions, and user defined primitives**

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