TRANSISTORS :

Biploar Junction Transistor (BJT)

PART - A

MODULE 3: Bipolar Junction Transistor (5 L + 2 T)

3.1 Transistor configuration: common base, common emitter, and common collector
3.2 Transistor characteristics: input and output characteristics of CB and CE configurations
3.3 DC load line: quiescent (Q) point; cut-off, active, and saturation region
3.4 Amplifier: Principle of operation
3.5 Transistor as a switch
3.6 Transistor biasing
- 3.6.1 Need of biasing
- 3.6.2 Methods of biasing: base resistor or fixed bias, emitter feedback bias, and voltage divider bias
- 3.6.3 Stability of Q-point (qualitative discussions)
- 3.6.4 Numerical problems on biasing

【Outline】

4.1 Device Structure and Physical Operation

4.2 Current - Voltage Characteristics

4.3 BJT Circuits at DC

4.4 Applying the BJT in Amplifier Design

4.5 Small-Signal Operation and Models

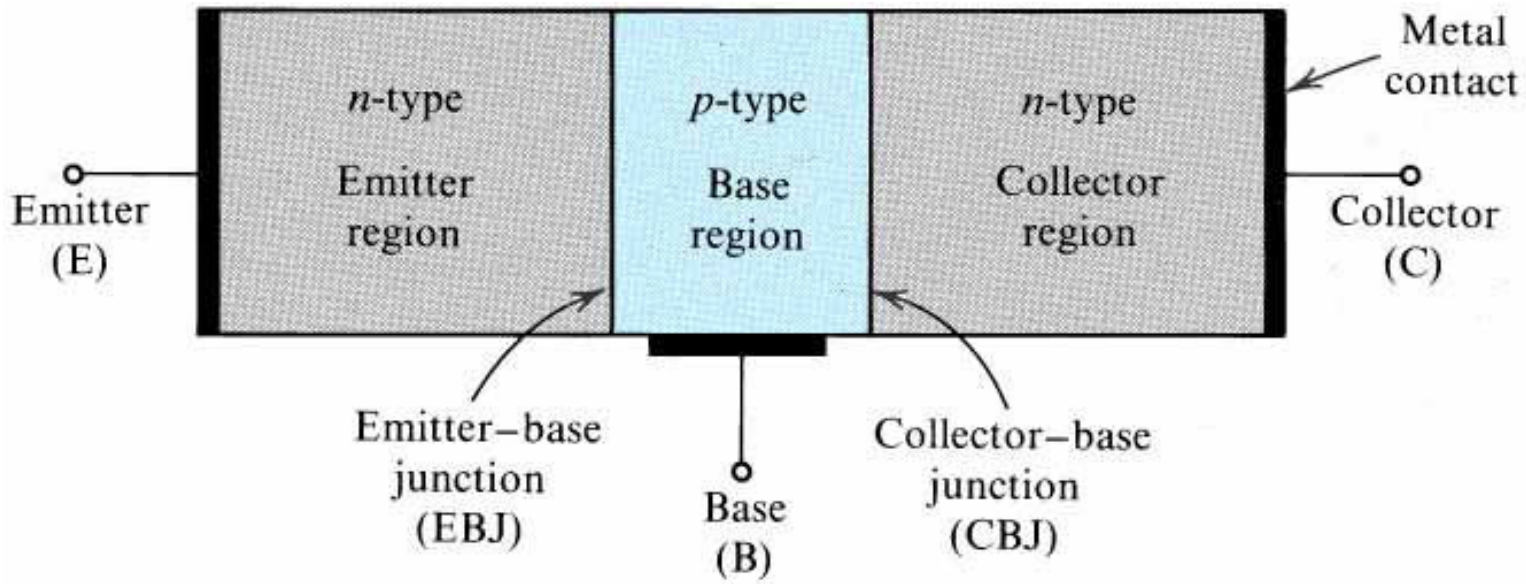
4.6 Basic BJT Amplifier Configurations

4.7 Biasing in BJT Amplifier Circuits

4.8 Discrete-Circuit BJT Amplifiers

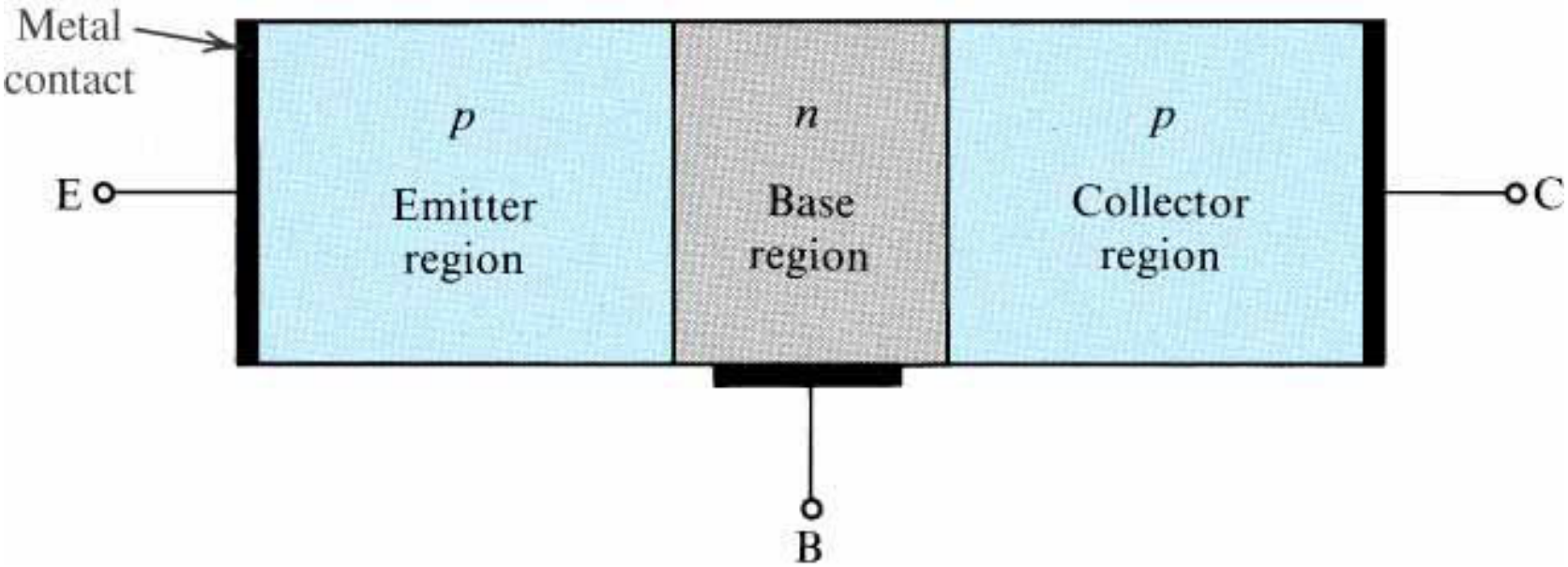
4.9 Transistor Breakdown and Temperature Effects

4.1 Device structure and physical operation



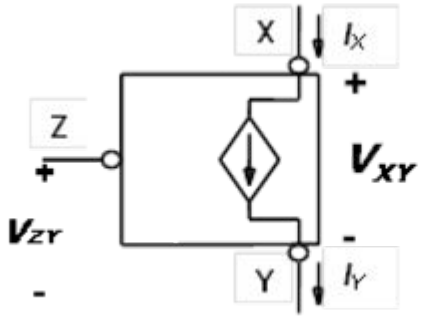
Emitter and collector regions having identical physical dimensions (C > E > B) and doping concentrations (E > C > B)

BASE WIDTH MUST BE SMALLER THAN DIFFUSION LENGTH
($W_B \ll L_{Diff}$)

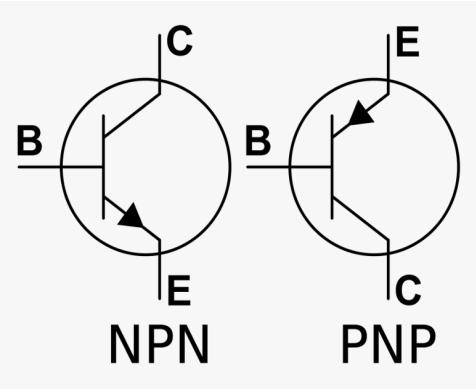


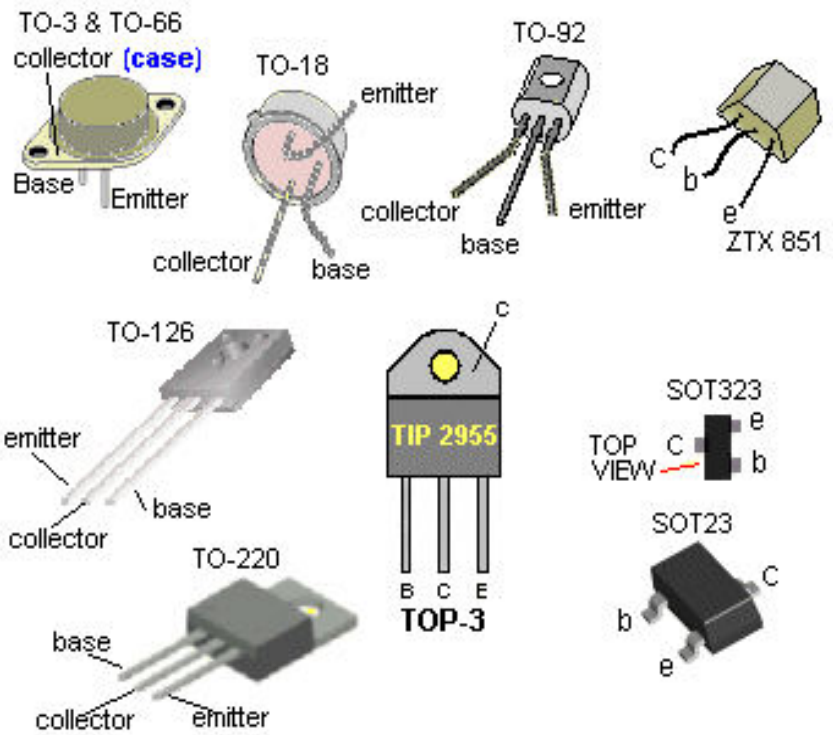
BJT modes operation

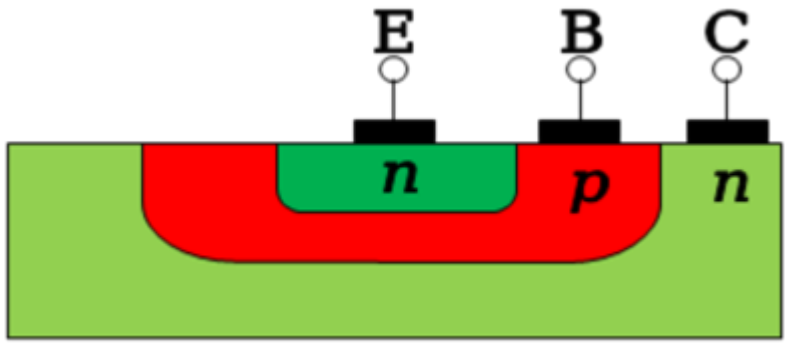
Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Reverse active	Reverse	Forward
Saturation	Forward	Forward



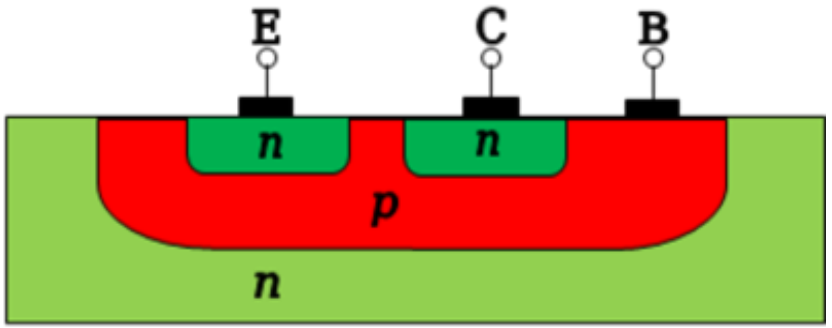
General Model of Transistor







Vertical NPN



Lateral NPN

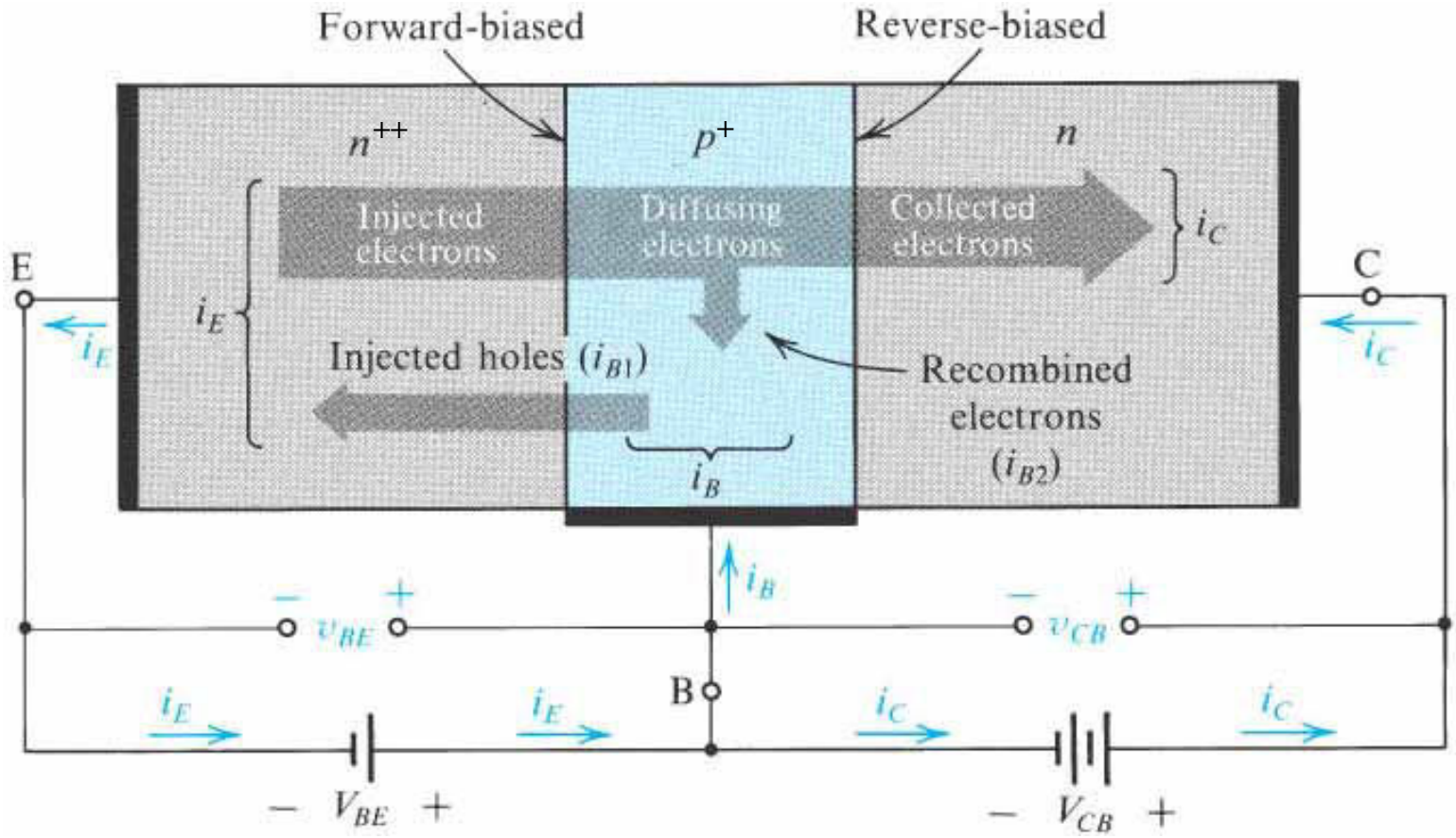


Figure 5.3 Current flow in an *npn* transistor biased to operate in the active mode. (Reverse current components due to drift of thermally generated minority carriers are not shown.)

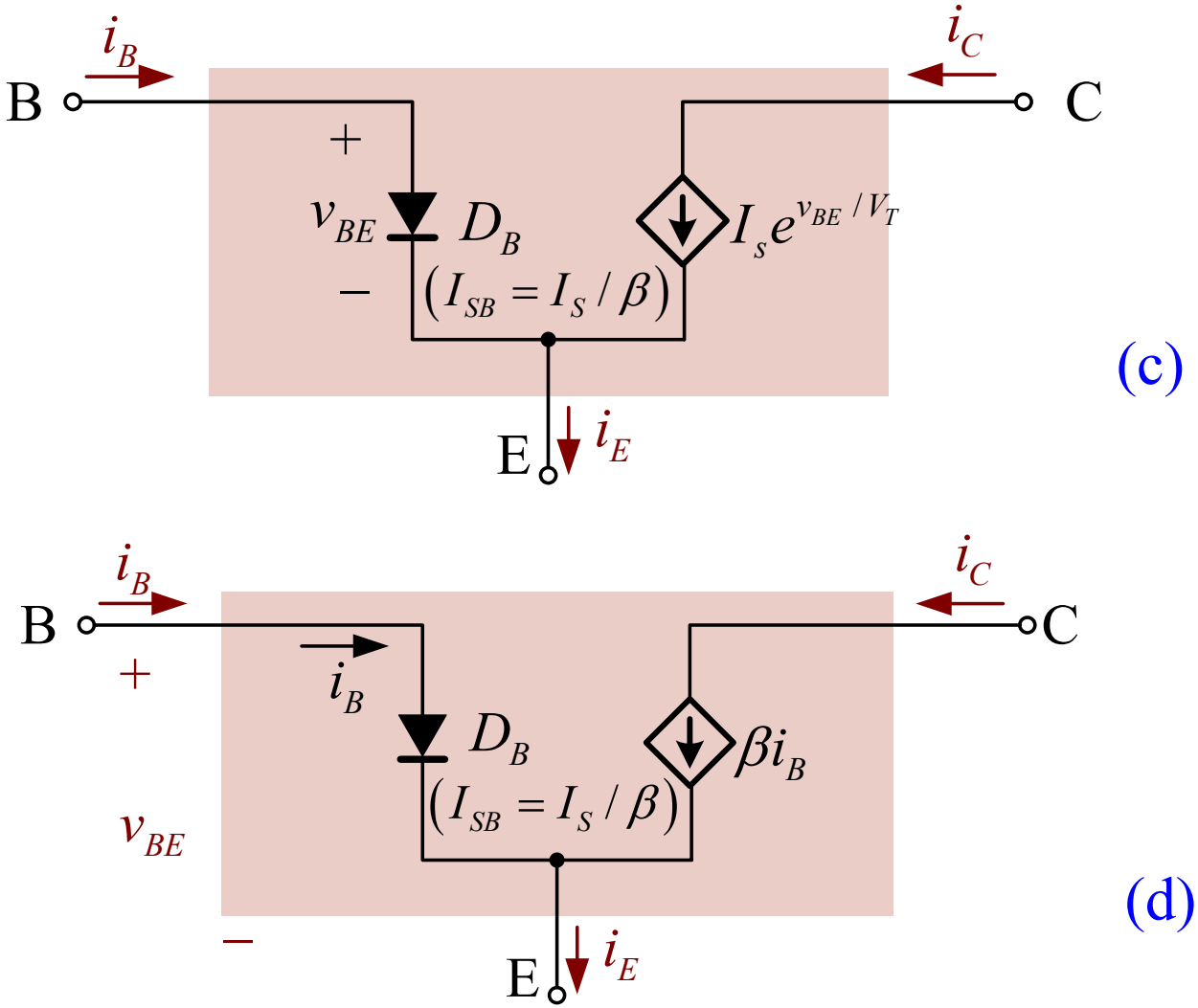


Figure 4.5 Large-signal equivalent-circuit models of the *npn* BJT operating in the forward active mode.

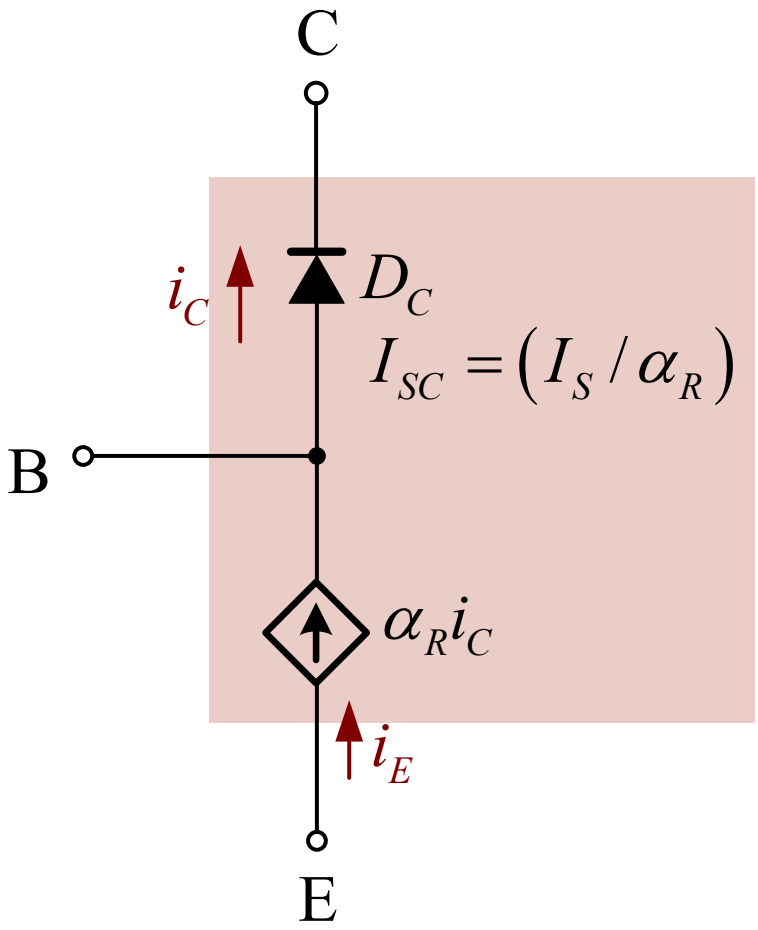


Figure 5.7 Model for the *npn* transistor when operated in the reverse active mode (i.e., with the CBJ forward biased and the EBJ reverse biased).

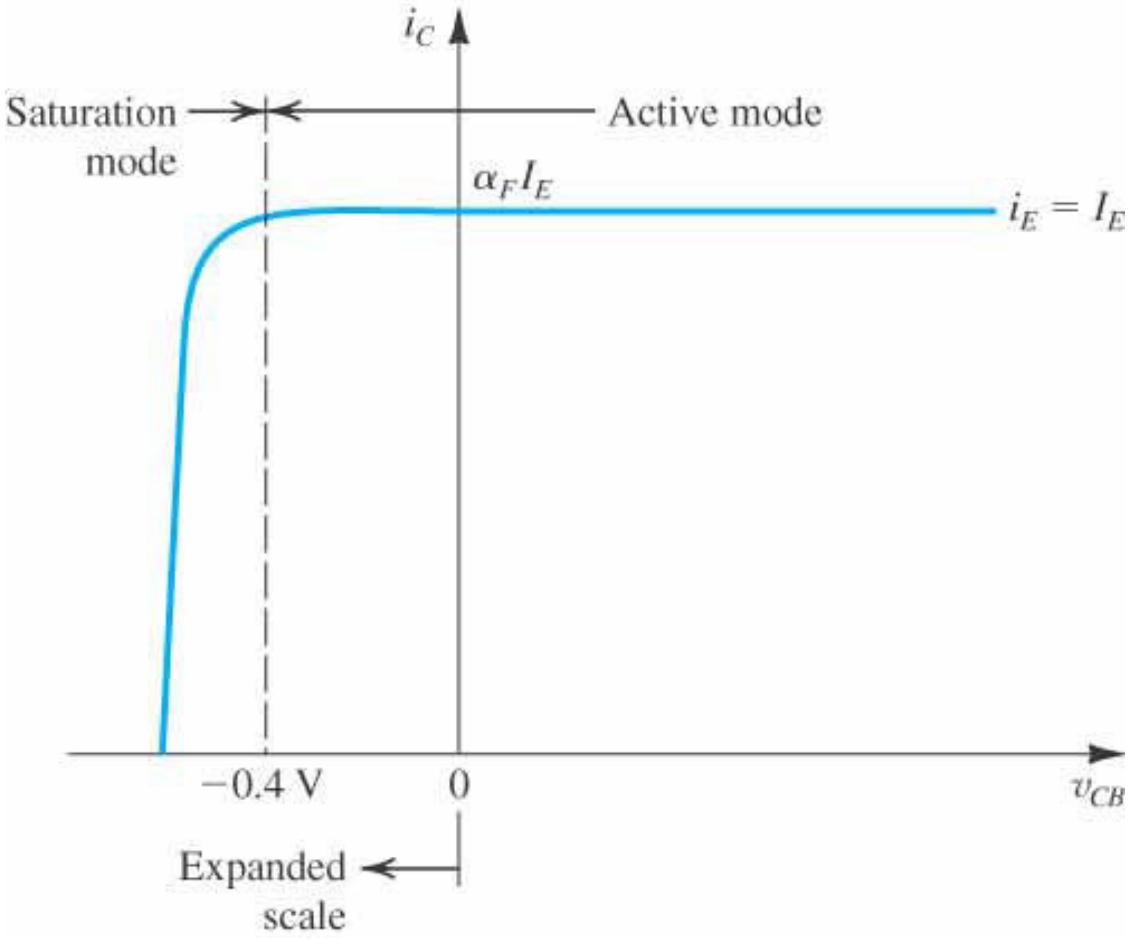


Figure 4.8 The i_C–v_{CB} characteristic of an *npn* transistor fed with a constant emitter current I_E. The transistor enters the saturation mode of operation for $v_{CB} < -0.4$ V, and the collector current diminishes.

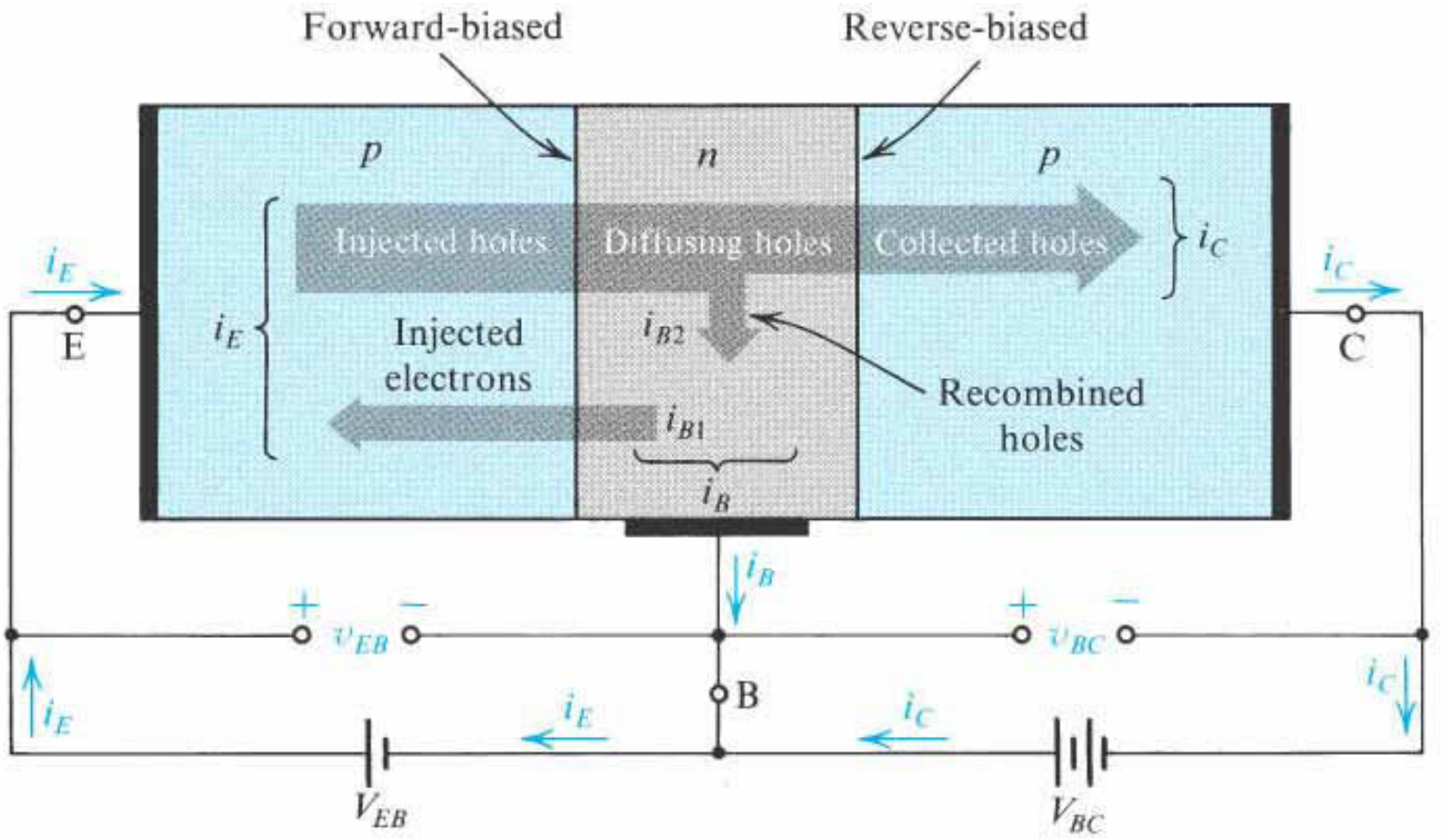


Figure 4.10 Current flow in a *pnp* transistor biased to operate in the active mode.

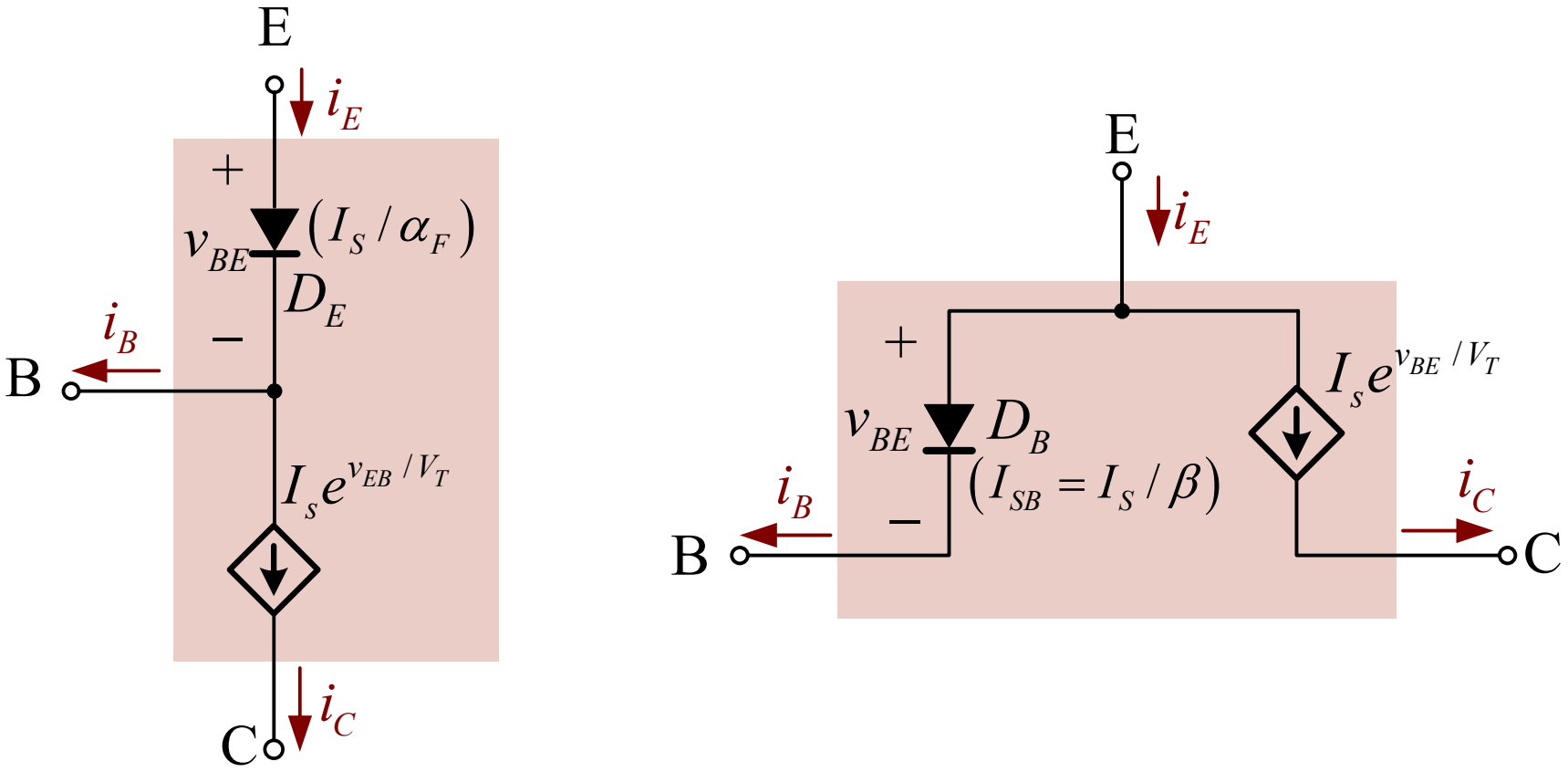
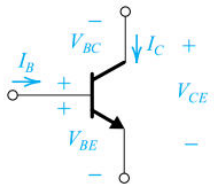
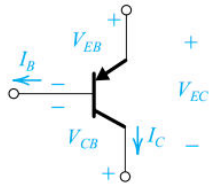
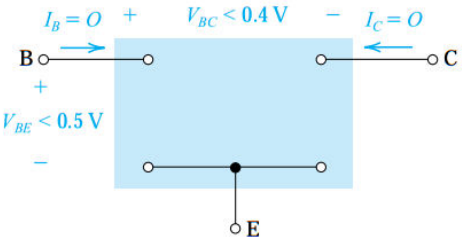
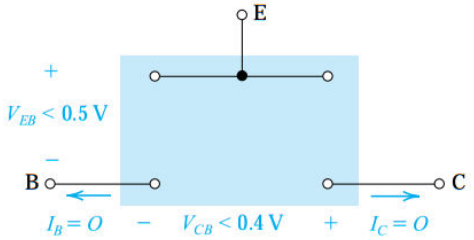
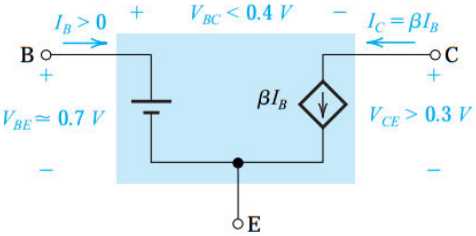
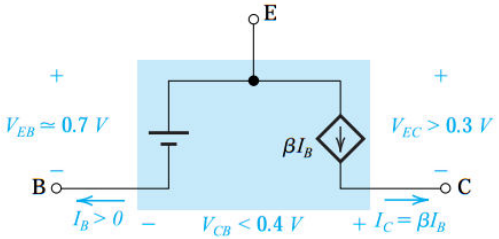
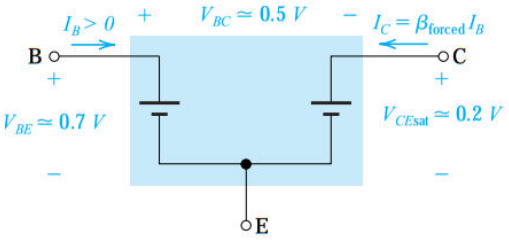
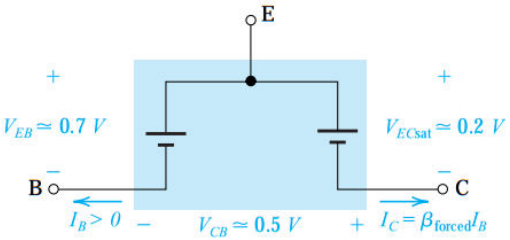


Figure 4.11 Large-signal model for the *pnp* transistor operating in the active mode.

DC MODELS OF BJT

Table 6.3 Conditions and Models for the Operation of the BJT in Various Modes

	npn	pnp
		
Cutoff EJB: Reverse Biased CBJ: Reverse Biased		
Active EBJ: Forward Biased CBJ: Reverse Biased		
Saturation EBJ: Forward Biased CBJ: Forward Biased		

BJT Currents in Forward-Active Mode

$I_E = I_B + I_C$

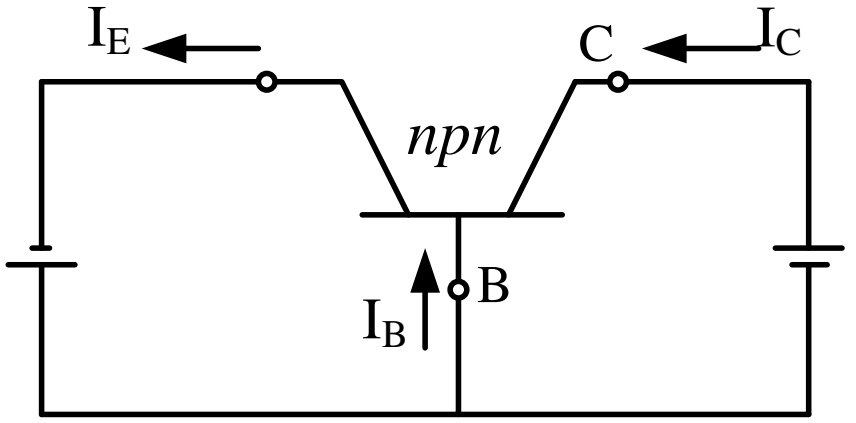
$I_C \sim \alpha I_E$ $\quad 0.95 < \alpha < 0.995$

α is the **emitter-to-collector gain**

In addition, due to the reverse biased C-B junction, a small reverse saturation current flows, $\boldsymbol{I_{CBO}}$ (collector-to-base leakage current with emitter open)

$\boldsymbol{\beta = \alpha/(1-\alpha)}$ is the **base-to-collector gain**

$20 < \beta < 200$



$$\boldsymbol{I_C = \alpha I_E + I_{CBO}} = \alpha(I_C + I_B) + I_{CBO}$$

$$=> (1-\alpha)I_C = \alpha I_B + I_{CBO}$$

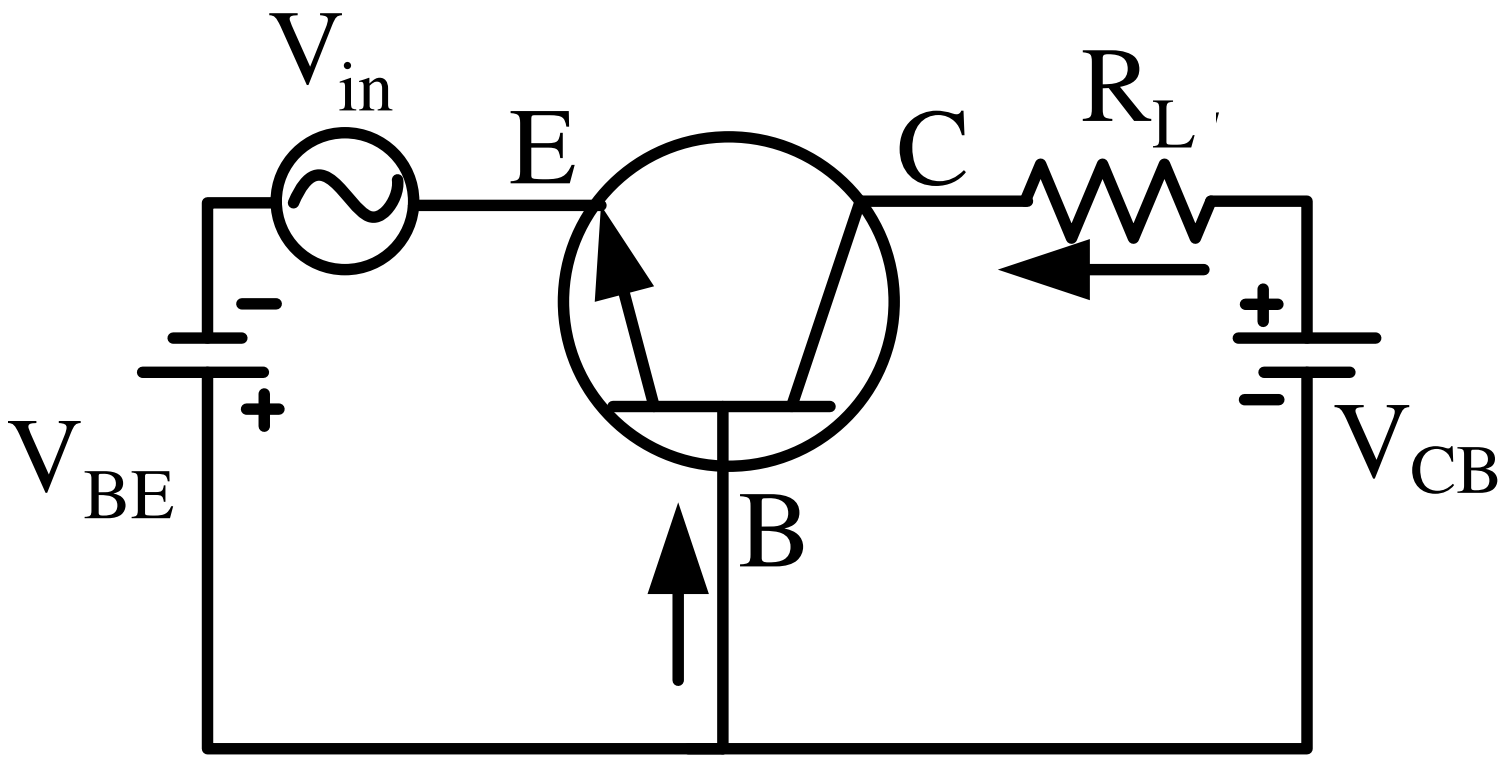
$$=> I_C = (\alpha/1-\alpha)I_B + (1/1-\alpha)I_{CBO}$$

$$=> \boldsymbol{I_C = \beta I_B + (\beta+1)I_{CBO}}$$

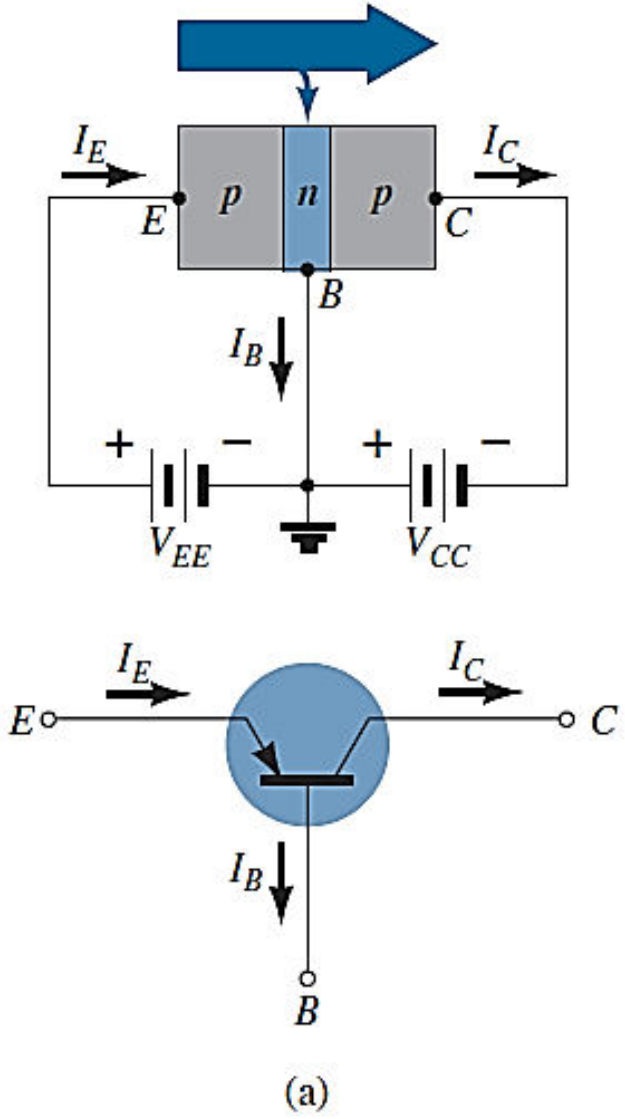
BJT Amplifier/Circuit Configurations

- ✓ Common-Base Configuration
- ✓ Common-Emitter Configuration
- ✓ Common-Collector Configuration

Common-Base Configuration

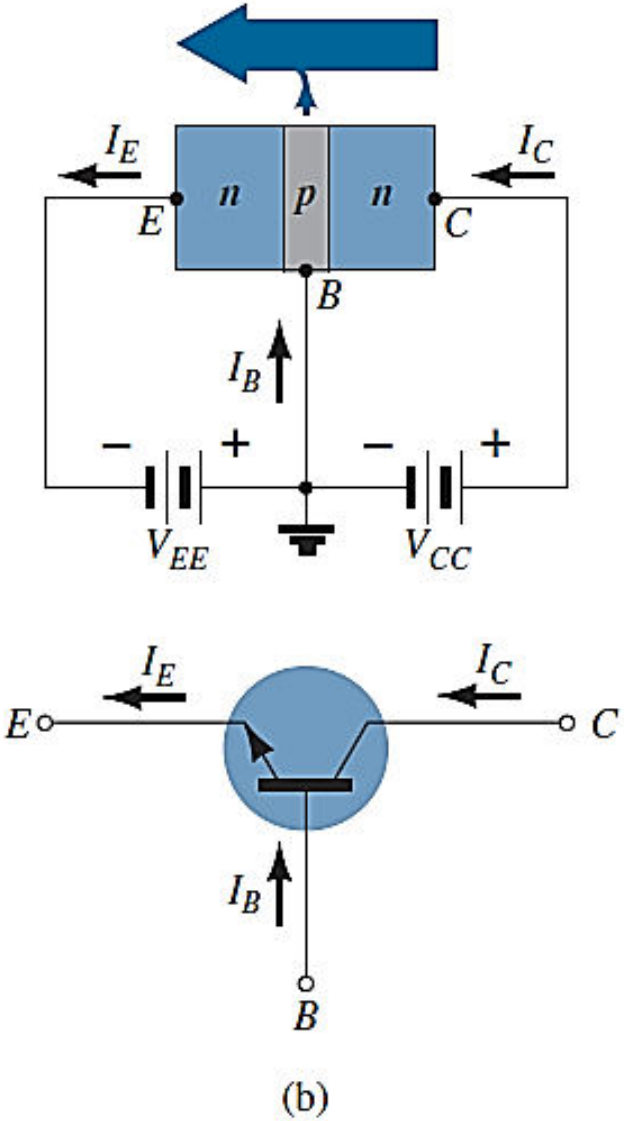


The base terminal is common to the input and output ports



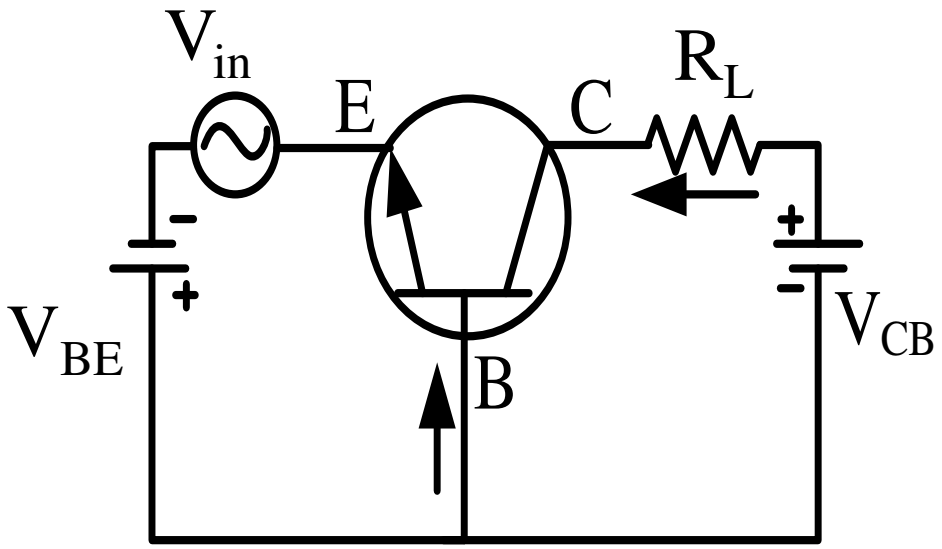
pnp transistor

The arrows in the graphics define the direction of current through the device.



npn transistor

Input dc characteristics in Common-Base configuration

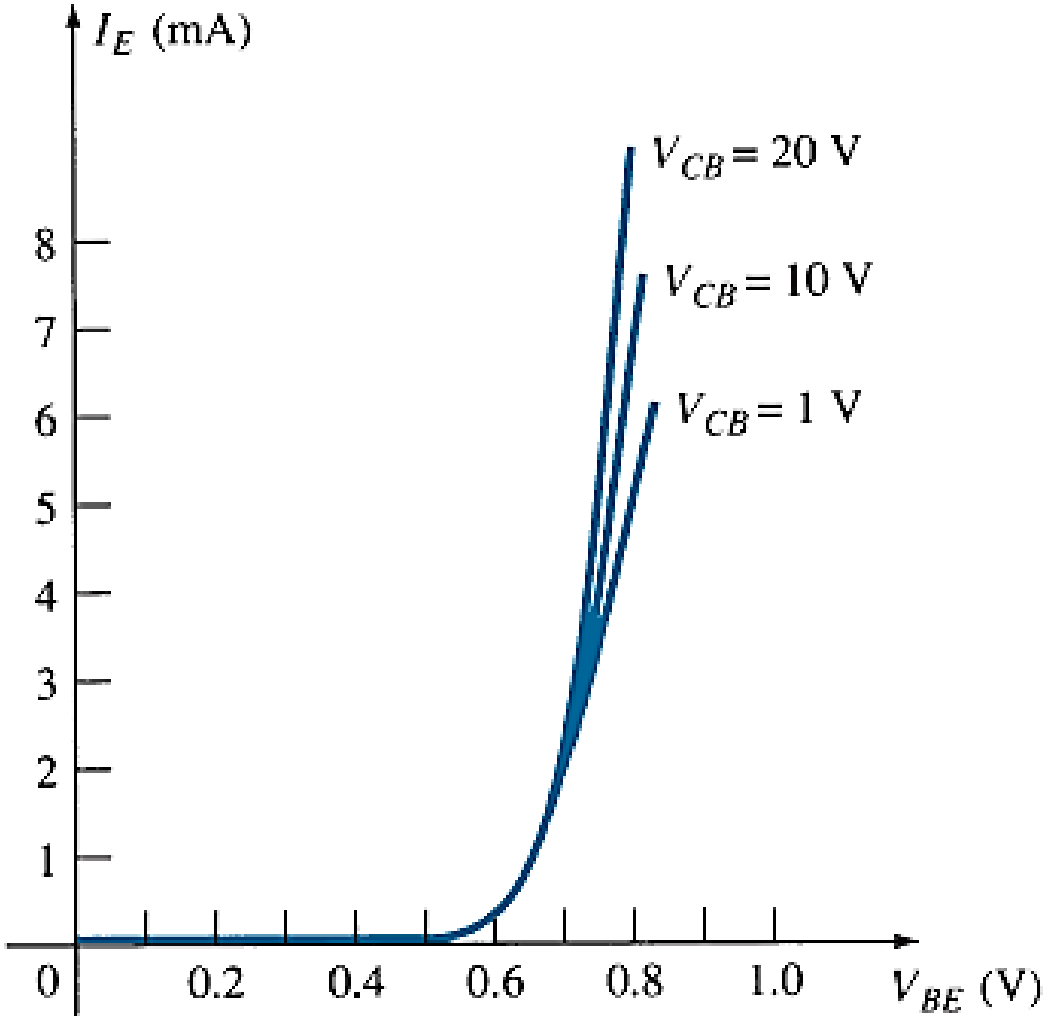


Notation:

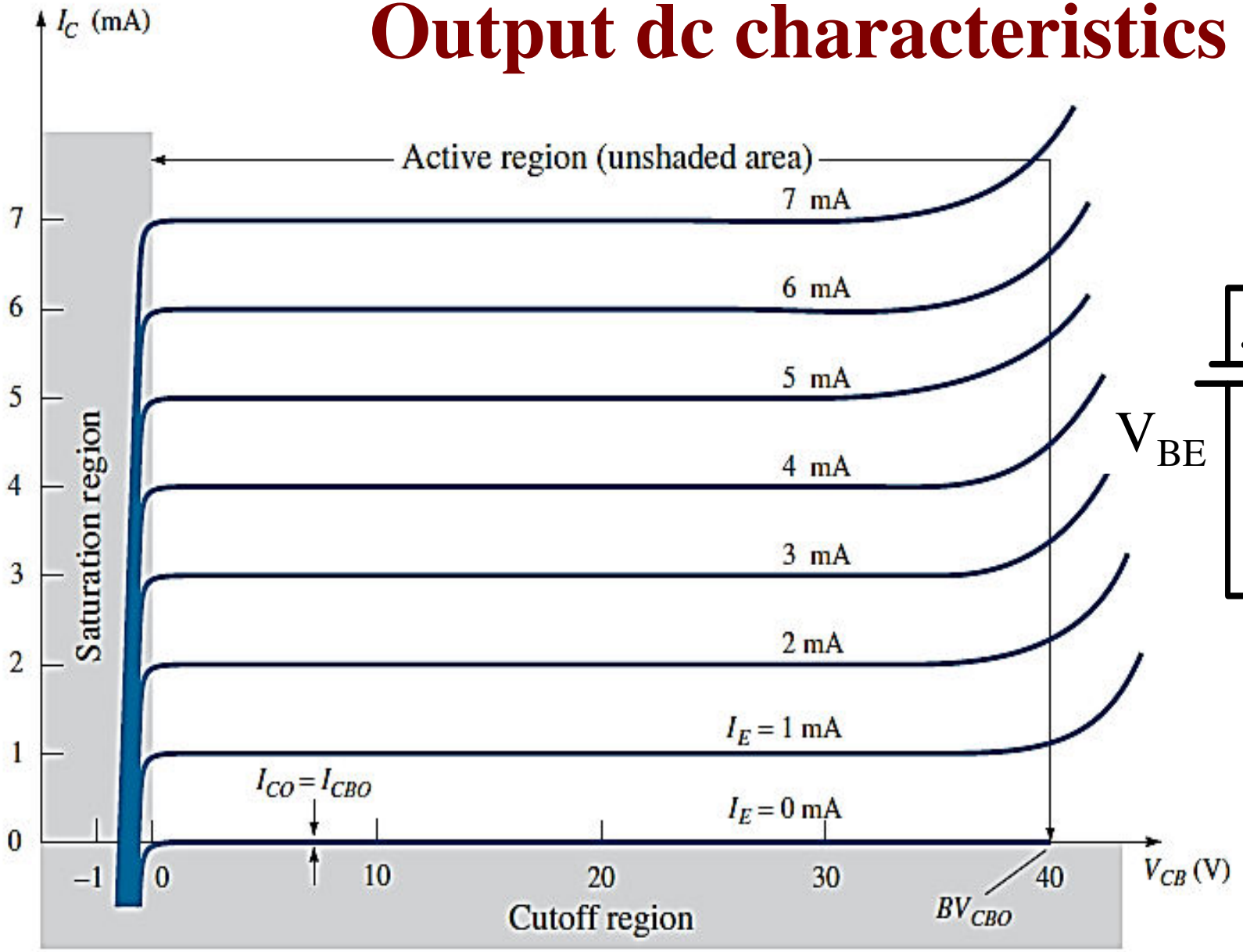
Input current (I_E)

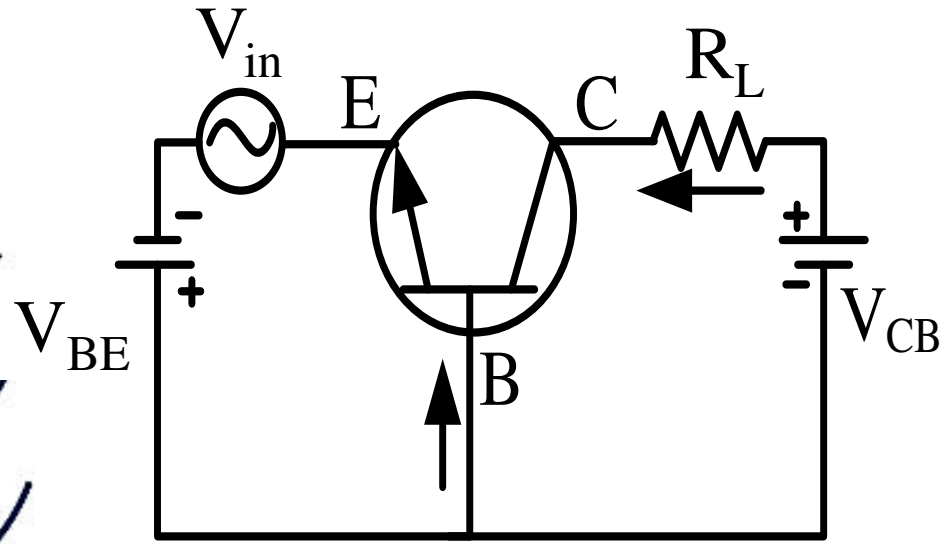
Input voltage (V_{BE})

Output voltage (V_{CB})



Output dc characteristics in Common-Base configuration





Notation:

Output current (I_C)

Output voltage (V_{CB})

Input current (I_E)

Modes of operation of *npn* transistor in Common-Base configuration

Cutoff region is defined as where the collector current $I_C = I_{CBO} \sim 0$ A

*The **base–emitter** and **collector–base** junctions are **both reverse-biased.***

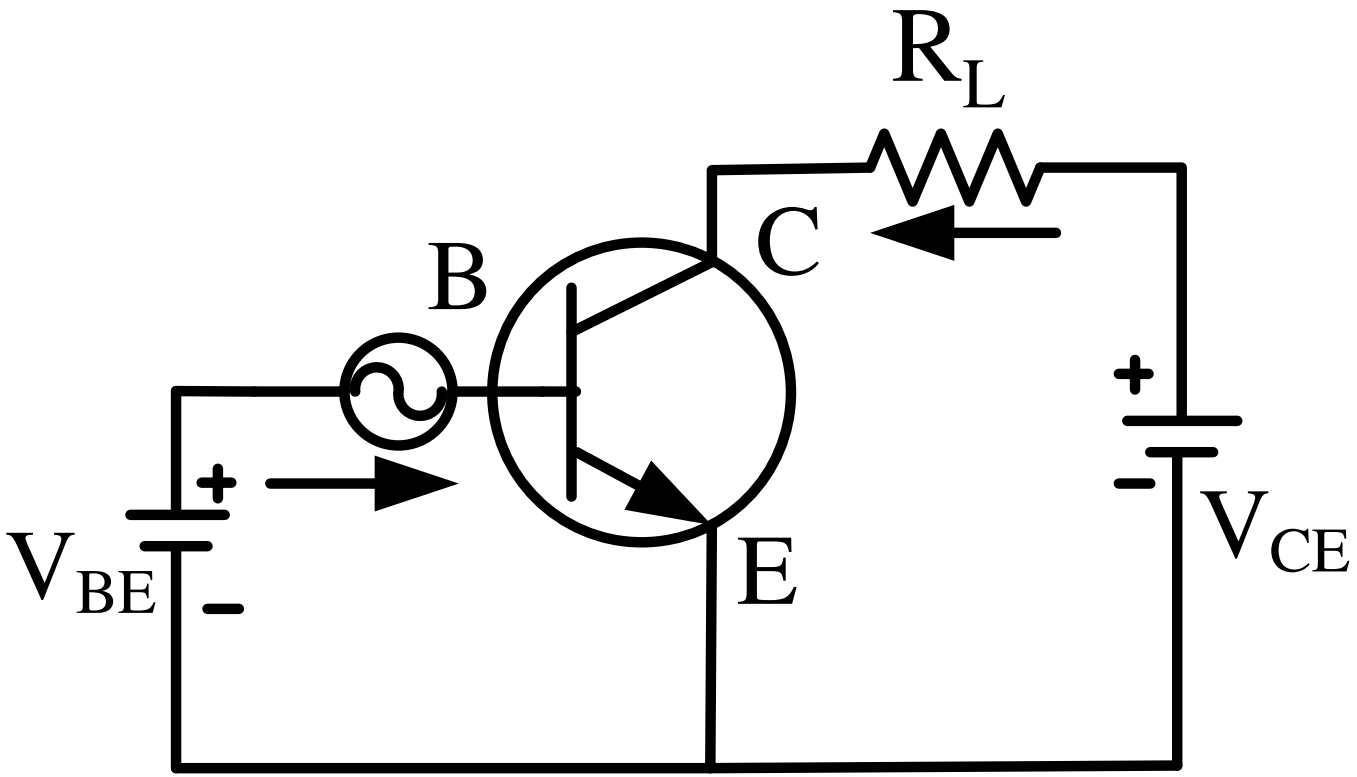
Saturation region is defined as where $V_{CB} < 0$ V

*The **base–emitter** and **collector–base** junctions are **both forward-biased.***

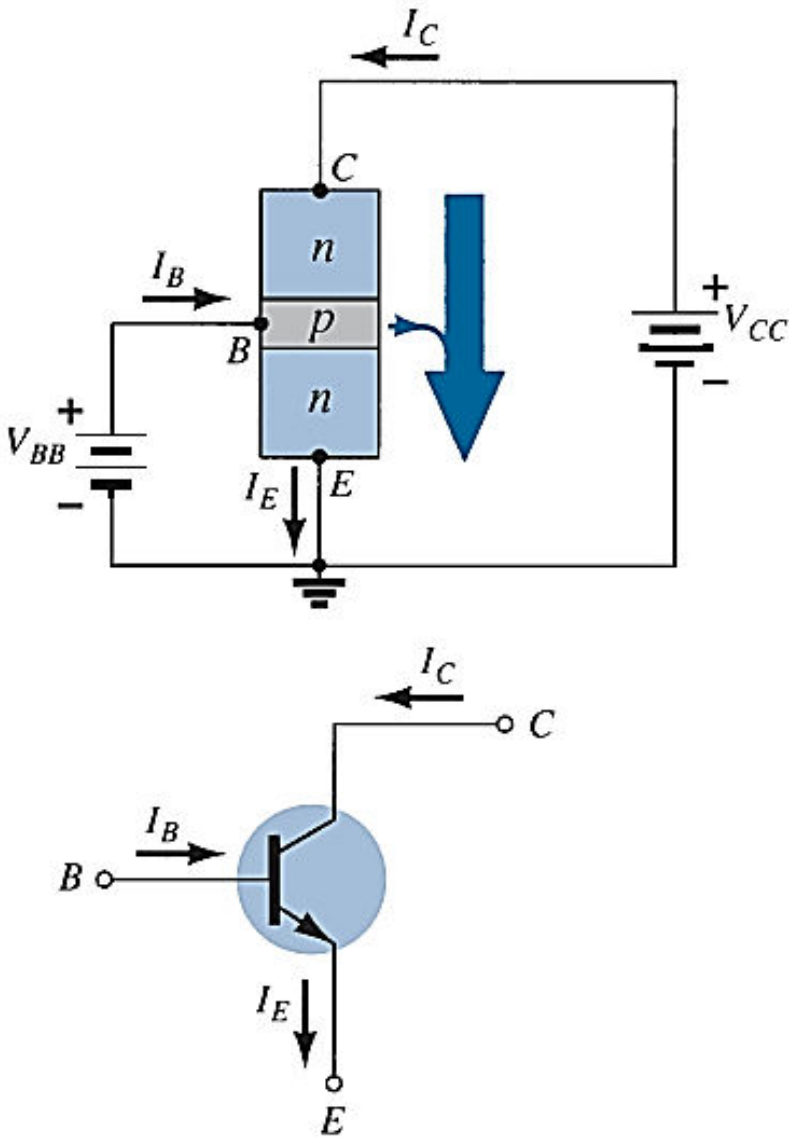
Active region is defined as where $V_{CB} > 0$ V

*The **base–emitter** junction is **forward-biased** and the **collector–base** junction is **reverse-biased.***

Common-Emitter Configuration

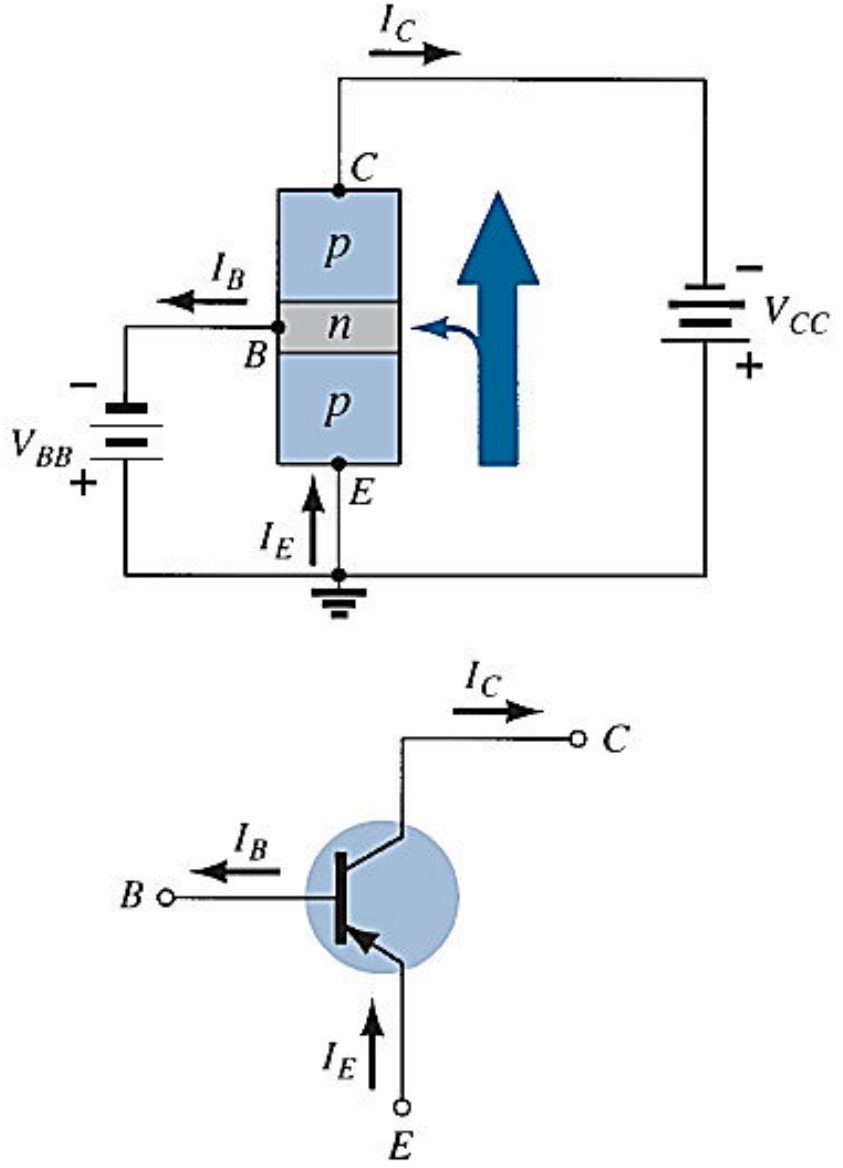


The emitter terminal is common to the input and output ports



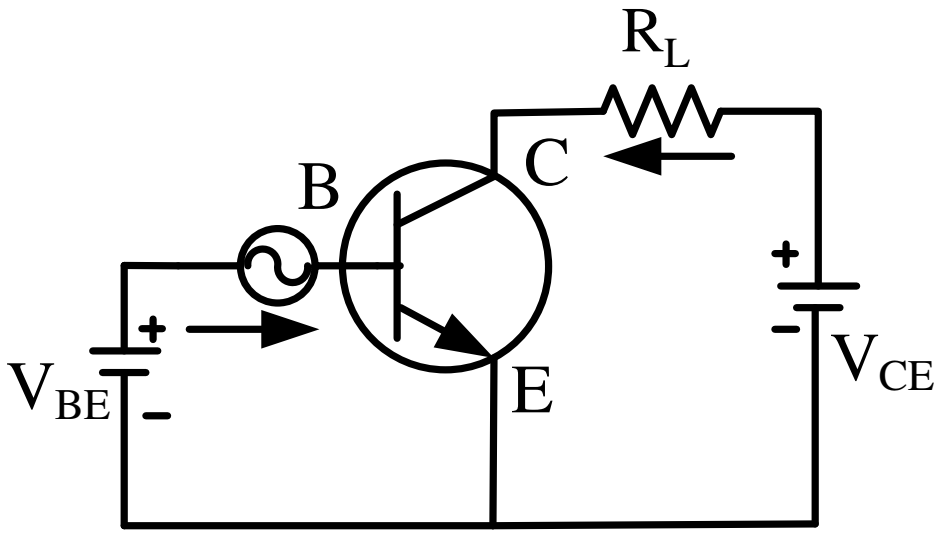
(a) *npn* transistor

The arrows in the graphics define the direction of current through the device.



(b) *pnp* transistor

Input dc characteristics in Common-Emitter configuration

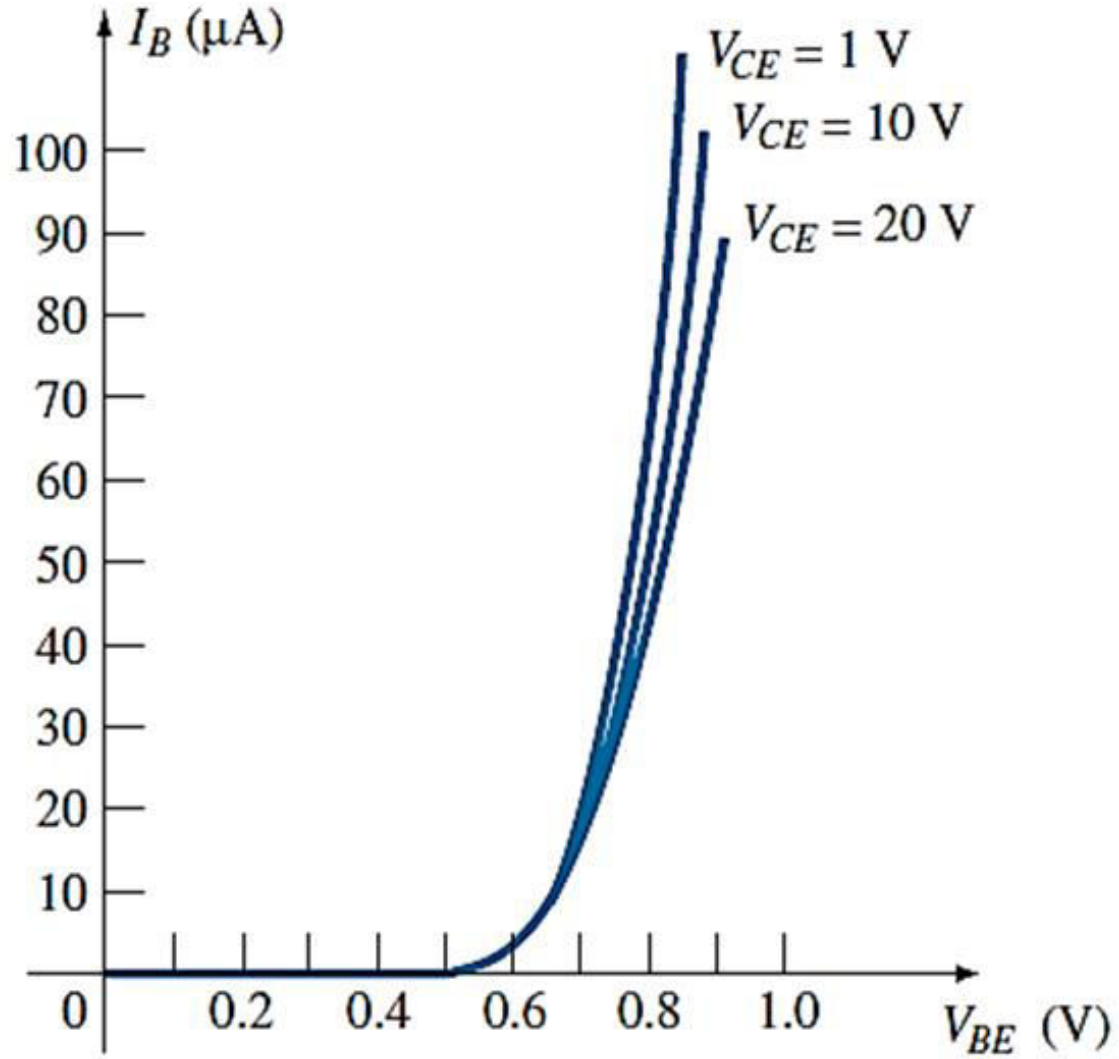


Notation:

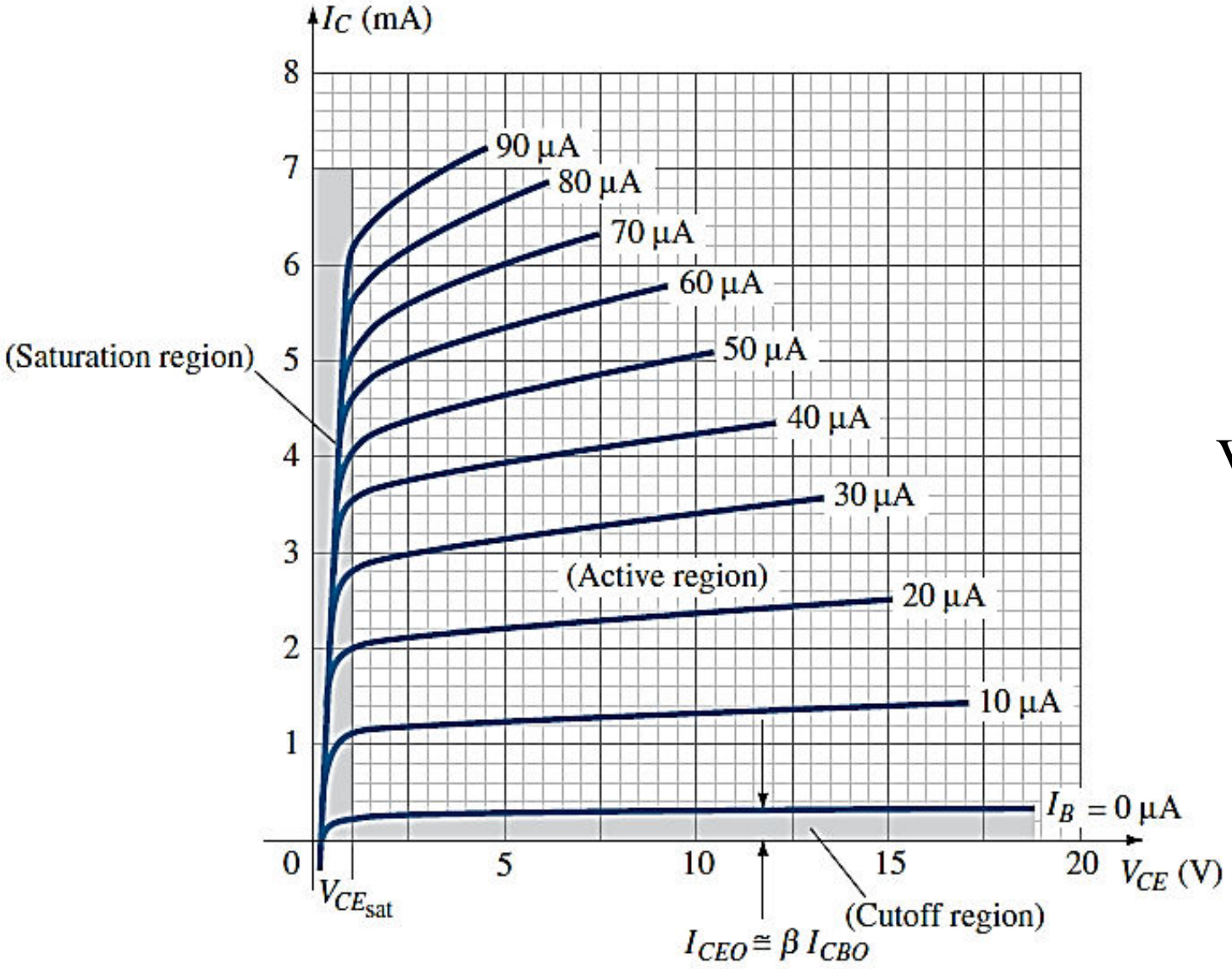
Input current (I_B)

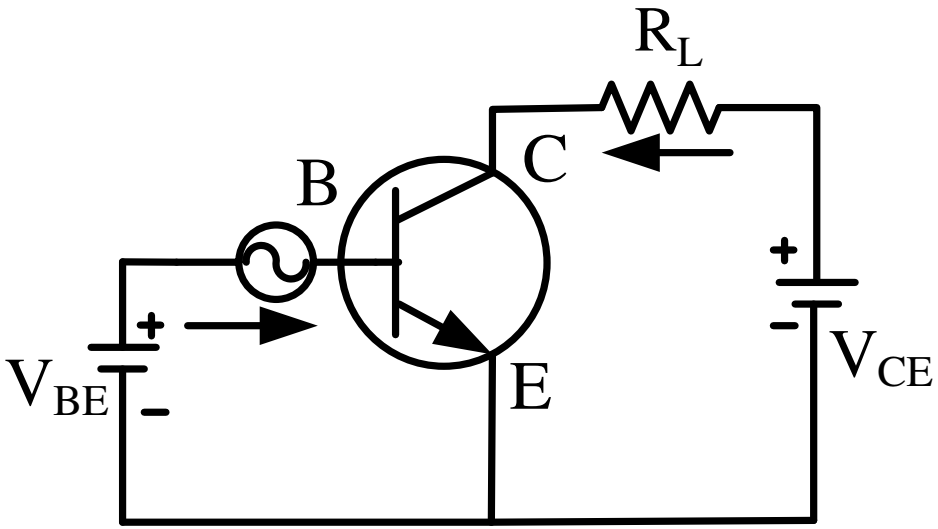
Input voltage (V_{BE})

Output voltage (V_{CE})



Output dc characteristics in Common-Emitter configuration





Notation:

Output current (I_C)

Output voltage (V_{CE})

Input current (I_B)

Saturation region is defined as where $V_{CE} < V_{CE(sat)} \sim$ **0.2 V (i.e. $V_{CB} < 0$ V)**

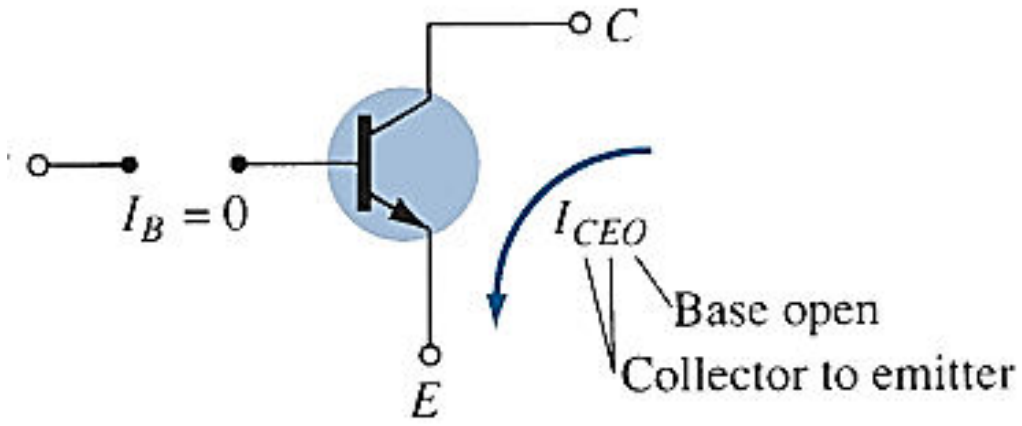
*The **base–emitter** and **collector–base** junctions are **both forward-biased.***

Active region is defined as where $V_{CE} > V_{CE(sat)} \sim$ **0.2 V (i.e. $V_{CB} > 0$ V)**

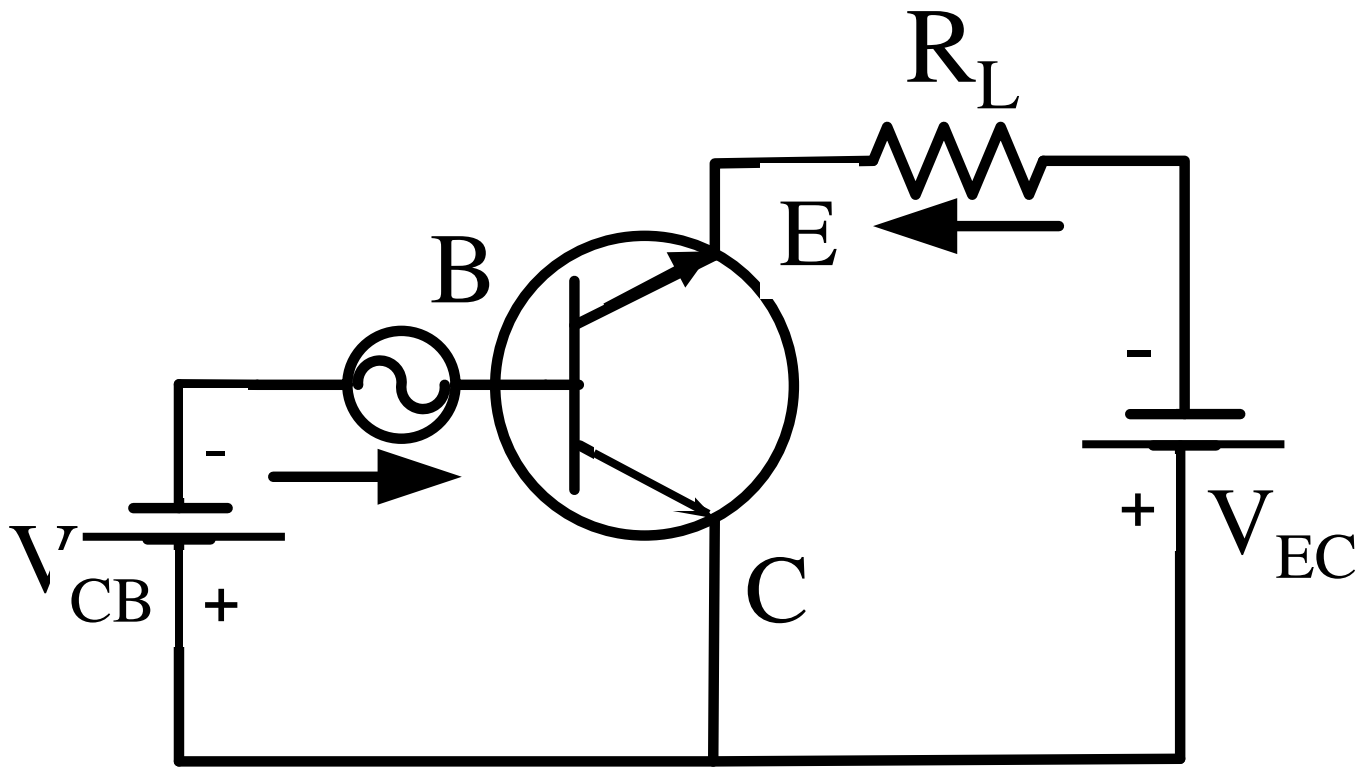
*The **base–emitter** junction is **forward-biased** and the **collector–base** junction is **reverse-biased.***

Cutoff region is defined as where the collector current $I_C = I_{CEO} = \beta I_{CBO}$

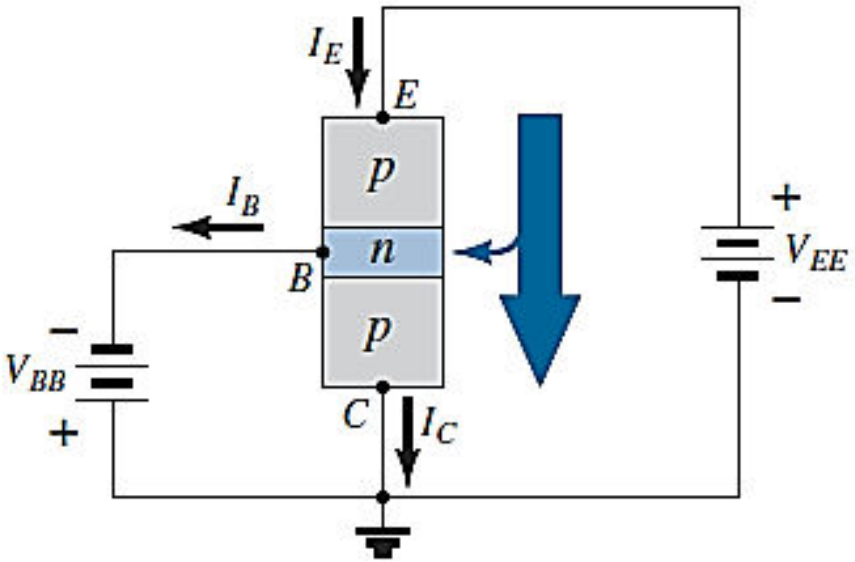
*The **base–emitter** and **collector–base** junctions are **both reverse-biased.***

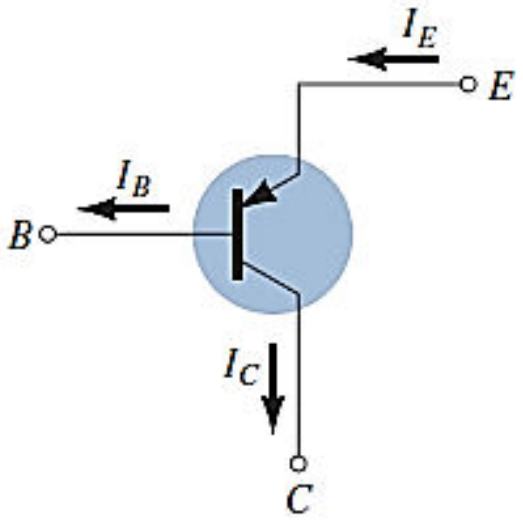


Common-Collector Configuration



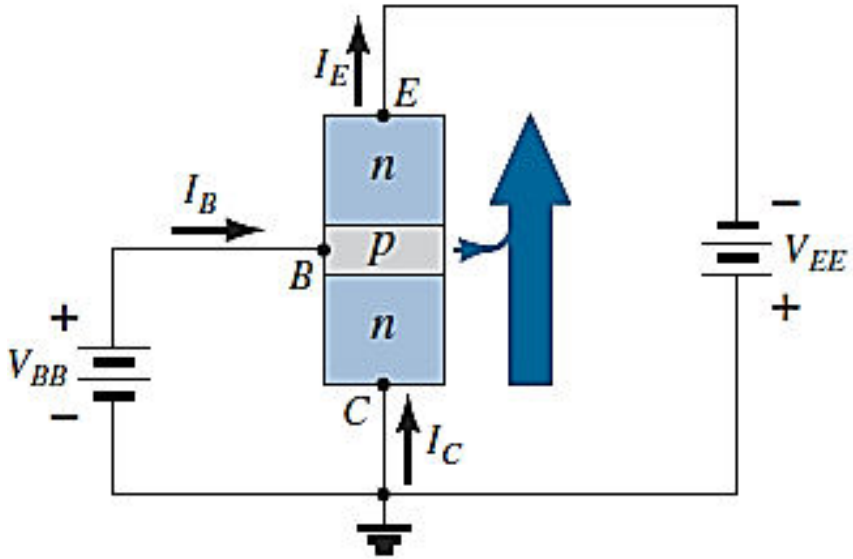
The common-collector configuration is used primarily for impedance-matching purposes: **High input impedance** and **low output impedance**

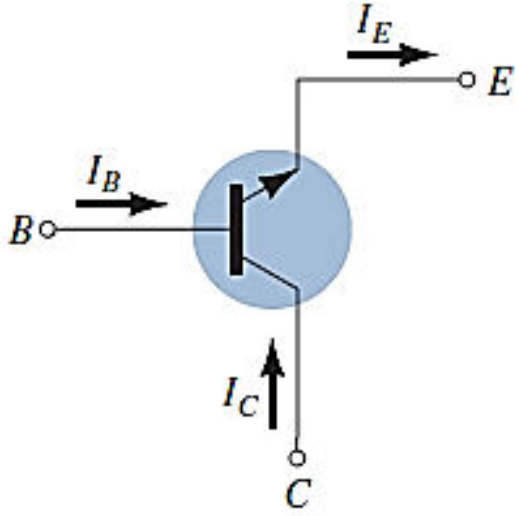




(a) *pnp* transistor

The arrows in the graphics define the direction of current through the device.

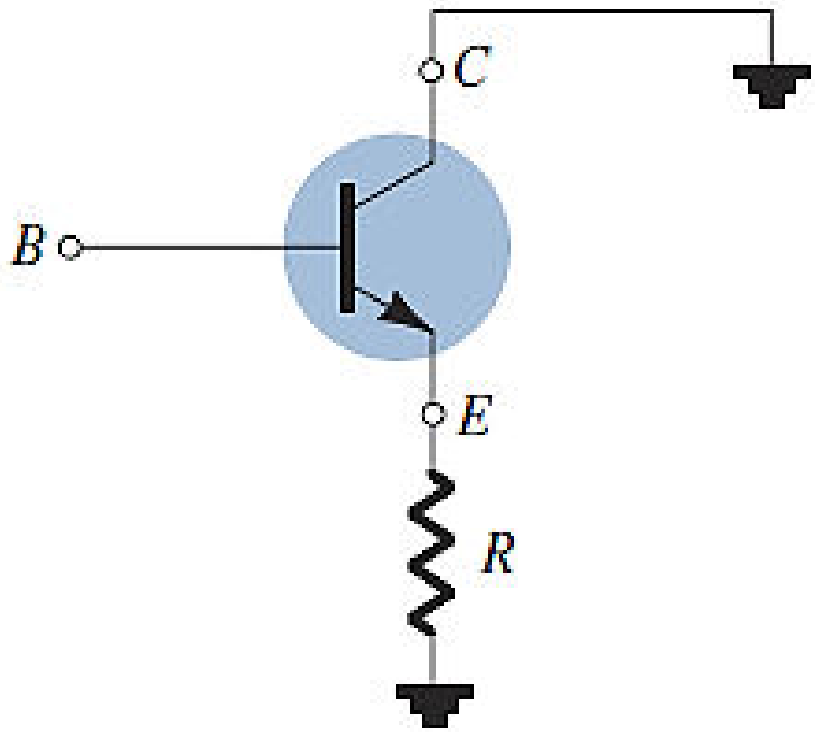




(b) *npn* transistor

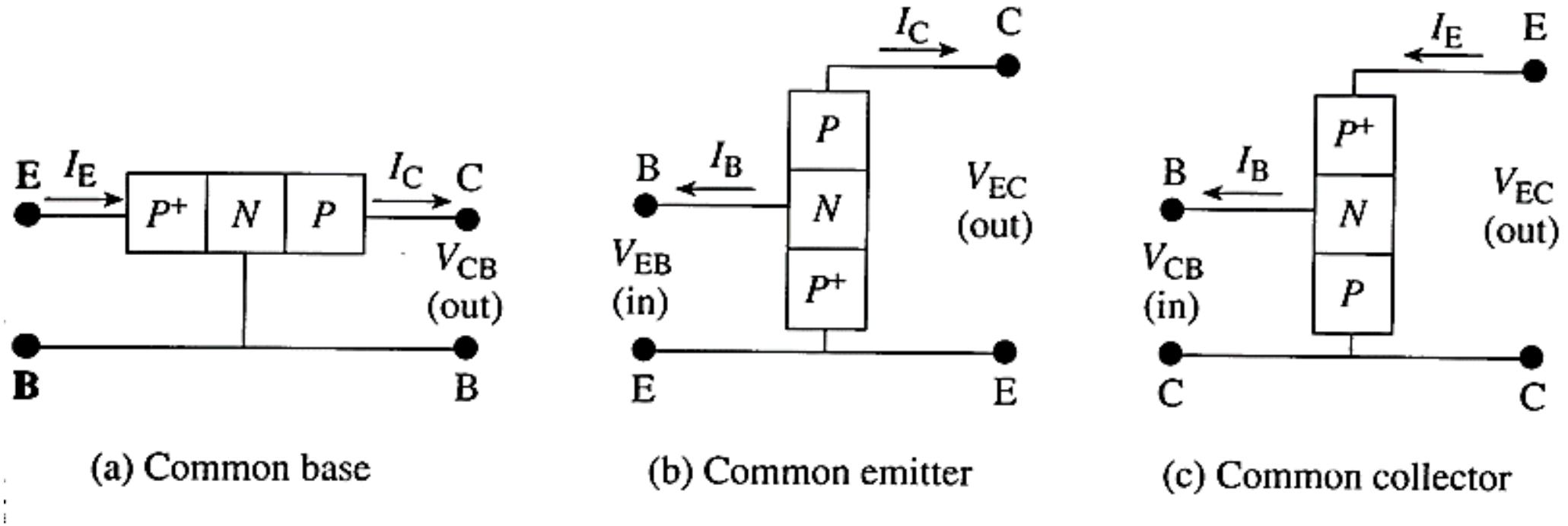
- The collector is tied to ground even though the transistor is connected in a manner similar to the common-emitter configuration

- The **output characteristics** of the common-collector configuration are **same as for the common-emitter configuration**



Common-collector configuration used for impedance-matching purposes.

BJT Configurations in *pnp* Transistor



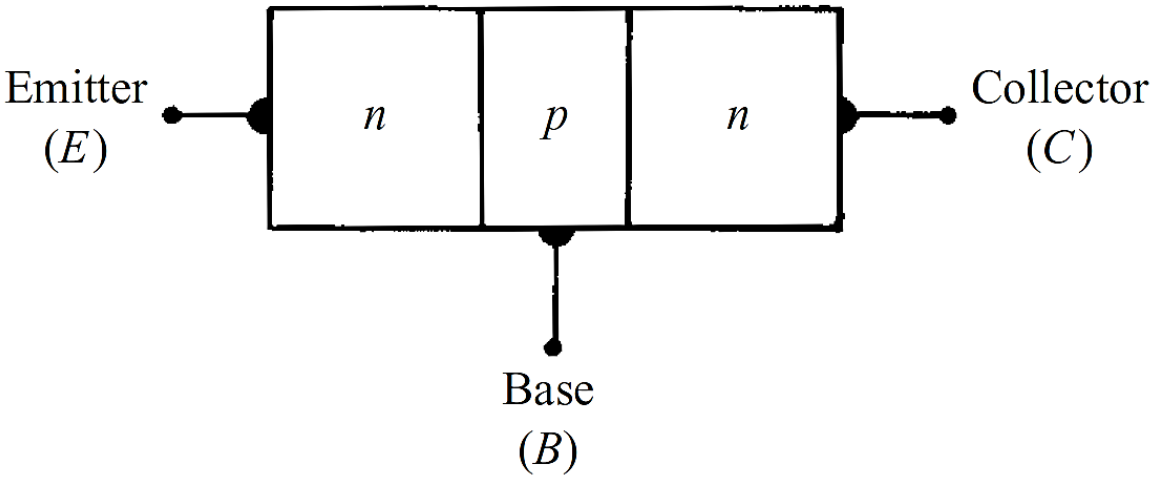
BJT amplifier configurations : Summary

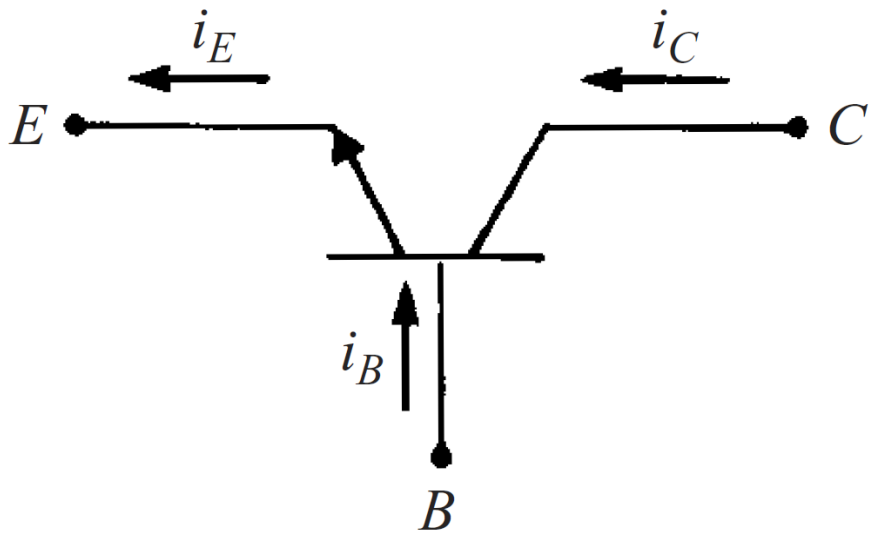
Characteristics	Common Base	Common Emitter	Common Collector
Input Impedance	Low	Medium	High
Output Impedance	Very high	High	Low
Phase shift	0^0	180^0	0^0
Voltage gain	High	Medium	Low
Current Gain	Low	Medium	High
Power gain	Low	Very High	Medium
Application	**Preamplifier**	**Most Common**	**Buffer**

Q1: In an *npn* transistor, 10^8 holes/μs move from the base to the emitter region while 10^{10} electrons/μs move from the emitter to the base region.

An ammeter reads the base current as $I_B = 16\ \mu A$.

Determine the emitter current I_E and the collector current I_C





Solution:

I_B **= 16 μA** (corresponding to 10^8 positive electronic charges/sec)

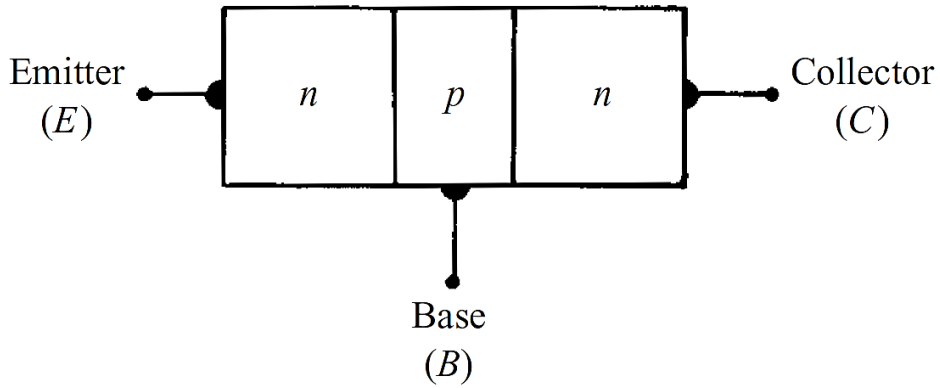
I_E = (100 × 16) μA (corresponding to 10^{10} negative electronic charges/sec)

+ 16 μA (corresponding to 10^8 positive electronic charges/sec)

= (101 x 16) μA = 1616 μA **= 1.616 mA**

$I_C = I_E - I_B$ **= 1.6 mA**

Q2: For the previous question (data given below), find the transistor α and β values, if the reverse collector-base leakage current is considered negligible

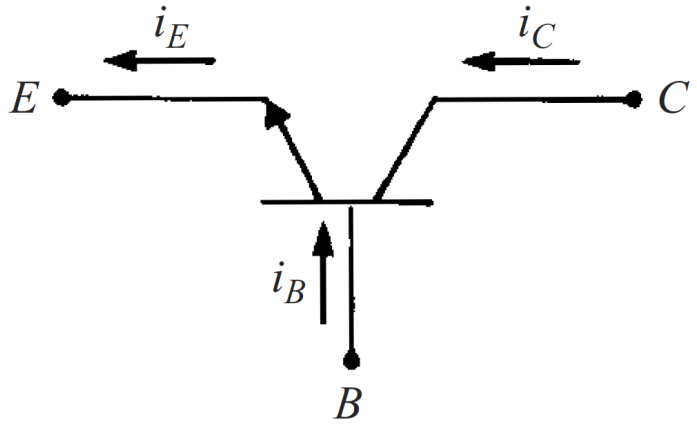


Transistor: *npn* transistor

Base current: I_B = 16 μA

Emitter current: I_E = 1.616 mA

Collector current: I_C = 1.6 mA



Solution:

If we assume $I_{CBO} = I_{CEO} = 0$, then

Emitter-collector current gain $\boldsymbol{\alpha = I_C / I_E} = 1.6/1.616 = \mathbf{0.99}$

Base-collector current gain $\boldsymbol{\beta = I_C / I_B} = 1.6/0.016 = \mathbf{100}$

Q3: A BJT has $\alpha = 0.99$, $I_B = 25\ \mu A$, $I_{CBO} = 200\ nA$.

Find the following parameters:

a) the dc collector current,

b) the dc emitter current, and

c) the percentage error in the emitter current when the leakage current is neglected.

Solution:

a) $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{0.99}{1-0.99} = 99$

$$I_C = \beta I_B + (\beta + 1) I_{CBO} = 99(25 \times 10^{-6}) + (99+1)(200 \times 10^{-9}) = 2.495 mA$$

b) $I_E = I_C + I_B = 2.495 + 0.025 = 2.52\ mA$

c) Neglecting the leakage current, we have

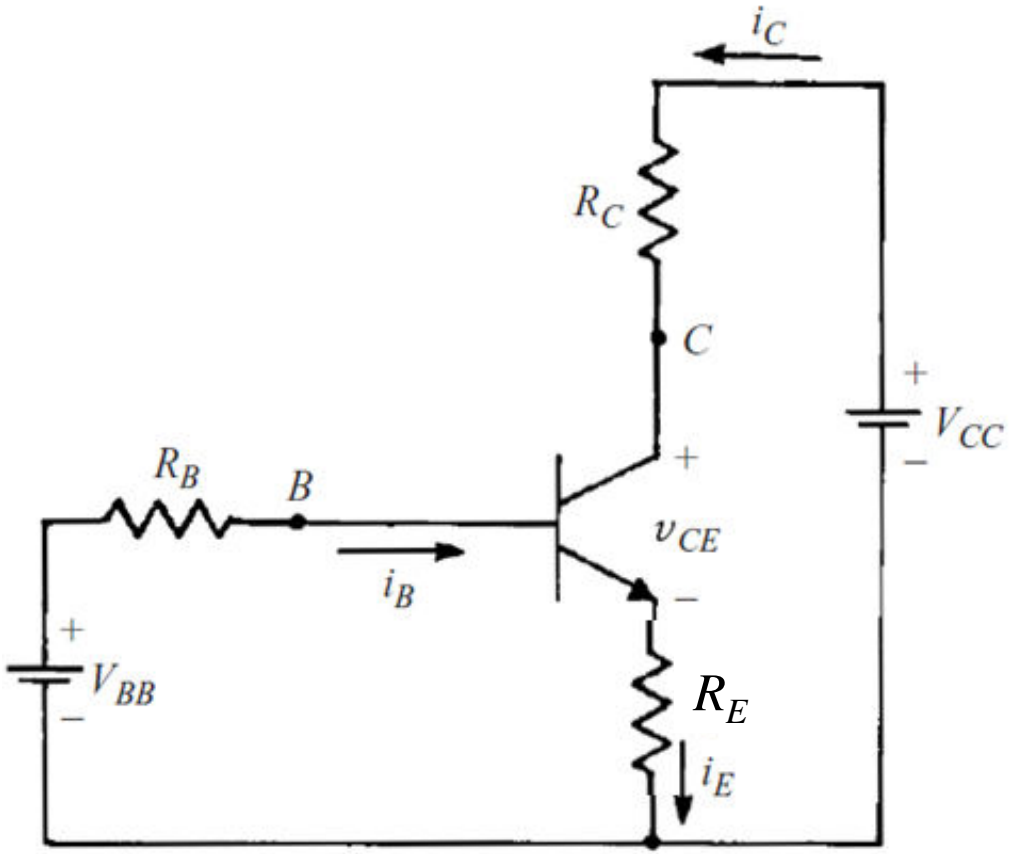
$$I_C = \beta I_B = 99(25 \times 10^{-6}) = 2.475 mA$$

$$I_E = \frac{I_C}{\alpha} = \frac{2.475}{0.99} = 2.5 mA$$

giving an emitter current error of

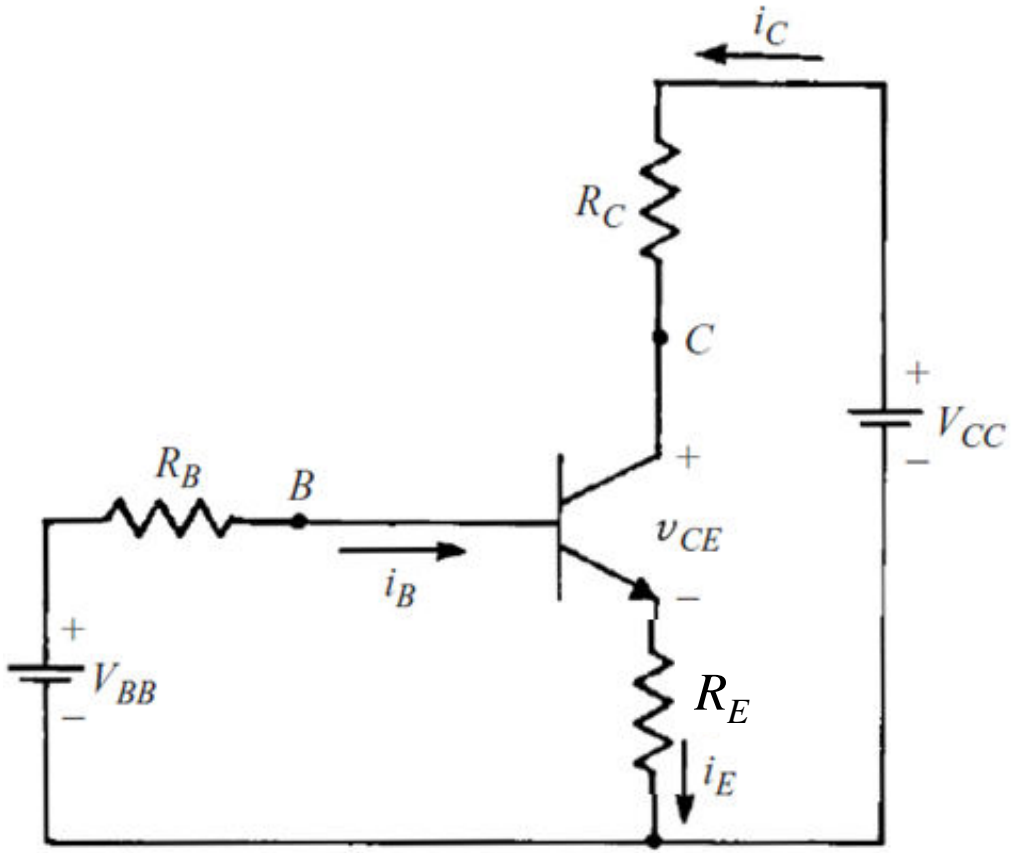
$$\frac{2.52 - 2.5}{2.52} \times 100\% = 0.793\%$$

Q4: A *Si* transistor connected in the common-emitter configuration (see fig.) has base current of 40 μA and $I_{CBO} = 0$. If $V_{BB} = 6$ V, $R_E = 1$ kΩ, and $\beta = 80$, find
(a) I_E, (b) R_B, (c) If $V_{CC} = 15$ V and $R_C = 3$ kΩ, find V_{CE}.



Solution:

a) $\boldsymbol{I_E} = (\beta+1)I_B = 81 \times 0.04 = \mathbf{3.24\ mA}$



b) KVL in input (B-E) loop:

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

$$\Rightarrow \boldsymbol{R_B} = (V_{BB} - V_{BE} - I_E R_E)/I_B$$

$$= (6 - 0.7 - 3.24\times1)/(0.04)\ \text{k}\Omega$$

$$= \mathbf{51.85\ k\Omega}$$

b) KVL in output (C-E) loop:

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \quad (I_C = \beta I_B = 80 \times 0.04 = 3.2\ \text{mA})$$

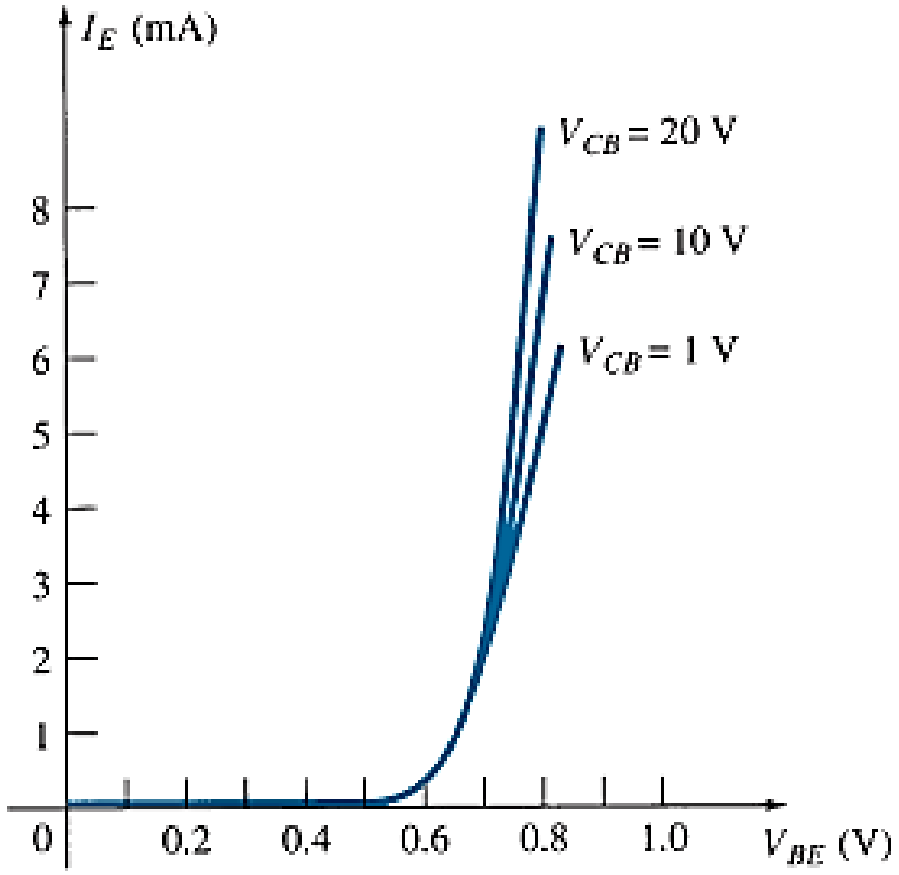
$$\Rightarrow \boldsymbol{V_{CE}} = V_{CC} - I_E R_E - I_C R_C = 15 - (3.24\times1) - (3.2\times3) = \mathbf{2.16\ V}$$

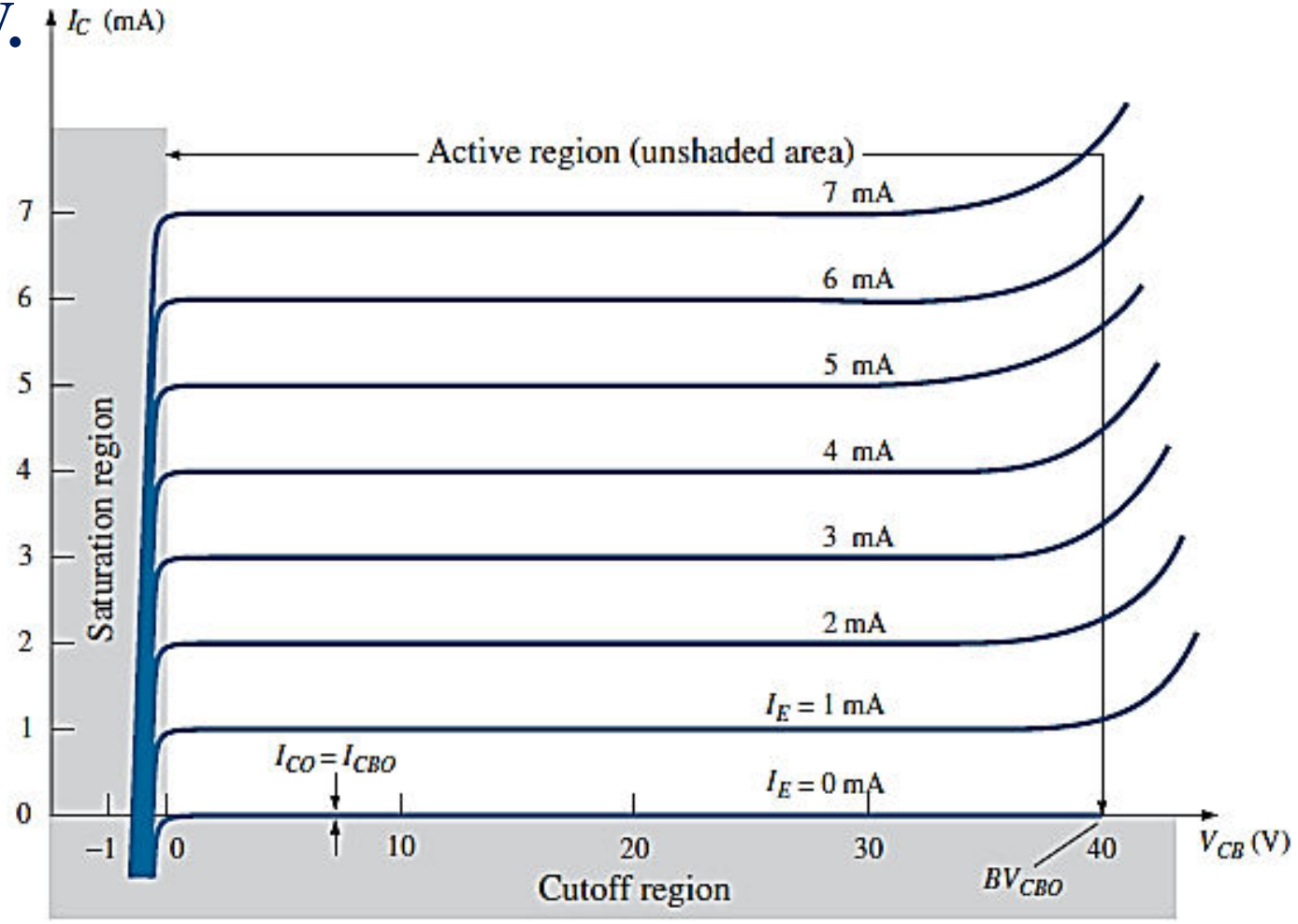
Q5: Using the characteristics shown below, determine

a. the resulting collector current if $I_E = 3$ mA and $V_{CB} = 10$ V.

b. the resulting collector current if I_E remains at 3 mA but V_{CB} is reduced to 2 V.

c. V_{BE} if $I_C = 4$ mA and $V_{CB} = 20$ V.





Solution:

a. The output characteristics clearly indicate that $I_C \sim I_E = 3$ **mA.**

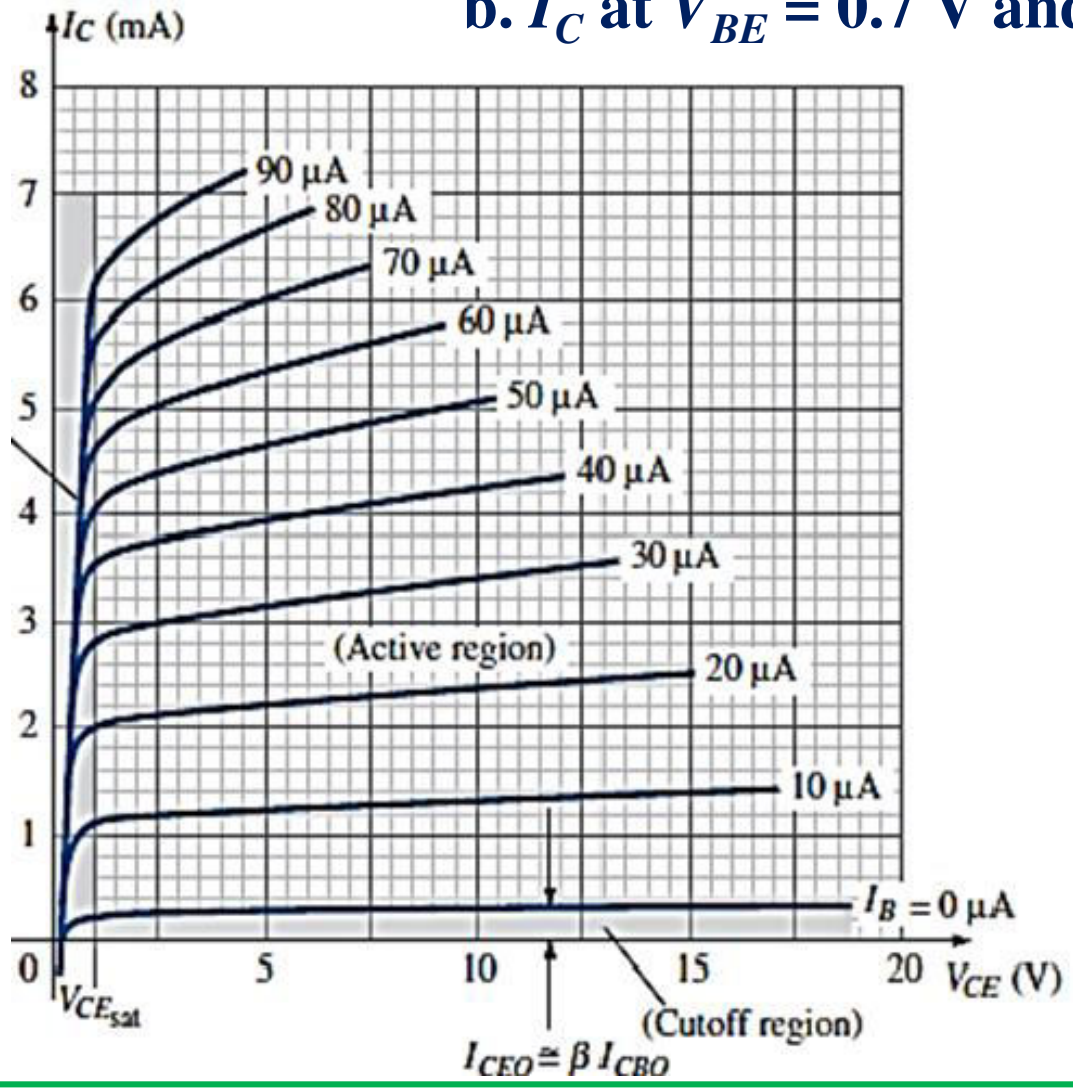
b. The effect of changing V_{CB} is negligible and I_C continues to be **3 mA**.

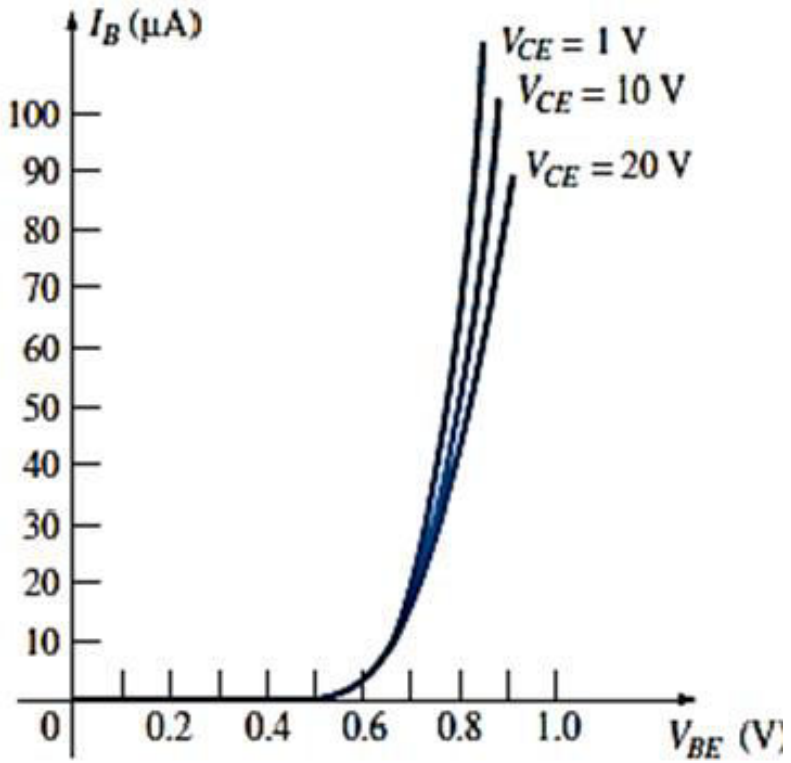
c. From output characteristics, $I_E = I_C = 4$ **mA**.
From input characteristics, for $I_E = 4$ **mA and** $V_{CB} = 20$ **V,**
the resulting value of V_{BE} is **~0.75 V**.

Q6: Using the characteristics shown below, determine

a. I_C at I_B = 30 µA and V_{CE} = 10 V.

b. I_C at V_{BE} = 0.7 V and V_{CE} = 15 V.





Solution:

a. From output characteristics, for $I_B = 30\ \mu A$ and $V_{CE} = 10\ V$, $\boldsymbol{I_C \sim 3.4\ mA}$.

b. From input characteristics, $\boldsymbol{I_B \sim 20\ \mu A}$ for $V_{BE} = 0.7\ V$ and $V_{CE} = 15V$
From output characteristics, $\boldsymbol{I_C \sim 2.5\ mA}$ for $I_B = 20\ \mu A$ and $V_{CE} = 15\ V$.