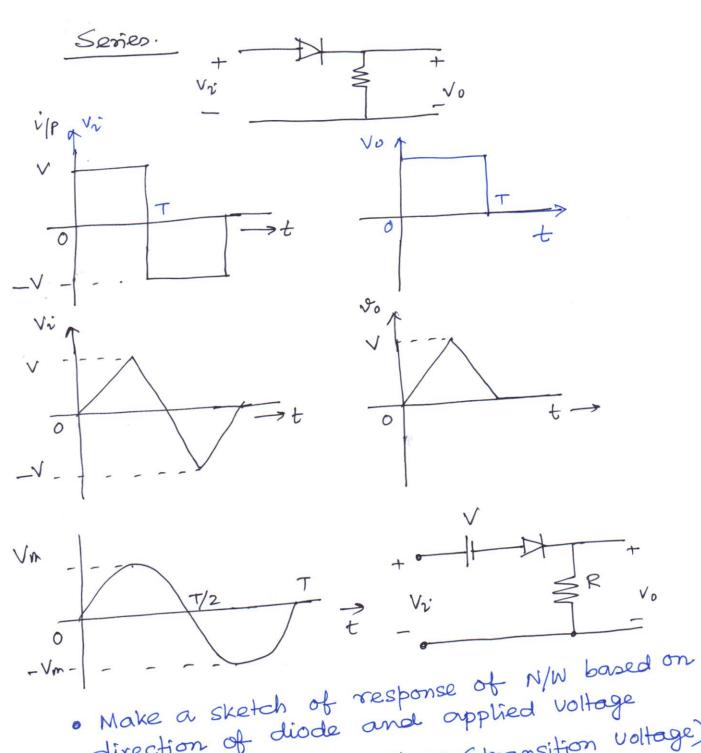
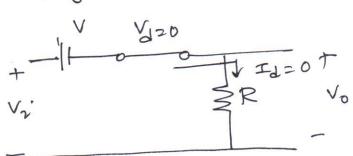
PORTION OF THE T/P SIGNAL "CLIP" OFF DISTORTING REMAINING PART OF THE WITHOUT AC WAVEFORM.



- direction of diode and applied voltage
- · Delécmine applied voltage (transition voltage) that causes a change in state of Diode.

For the ideal diode transition occurs at $i_0=0$, $i_0=0$

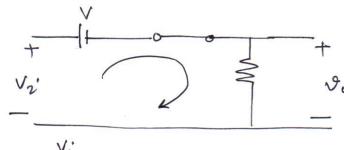
· Apply this condition to the network.



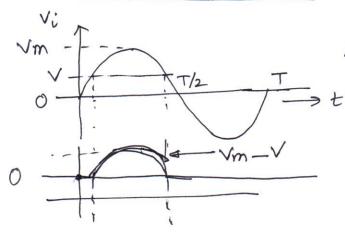
$$V_0 = I_R.R = I_d.R = 0$$
 $V_0 = 0$
 $V_1 = V$

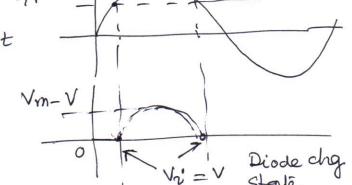
So level of $v_i = v$ will cause a change/transition in State.

- Thus for an i/p voltage greater than V, diode is in short-ckt state, while for i/p less than V' volt, it is in open ckt or OFF state.
- · When the dicde is in Short ckt State, the Opp voltage vo can be determined by KVL



$$-v_i + V + v_0 = 0$$
or $v_0 = v_i - V$

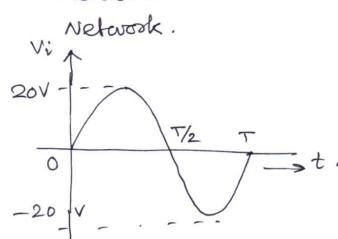


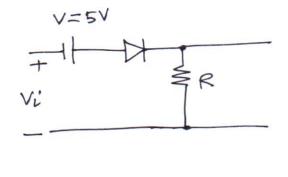




Delecmine the O/P waveform of the







Diode will be ON for +VR Vi

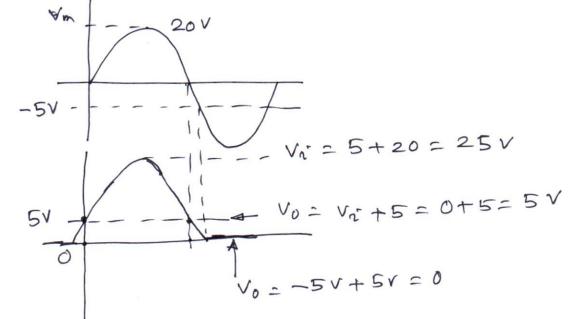
$$-V_{1}-5+V_{0}=0$$
or $V_{0}=V_{1}+5$

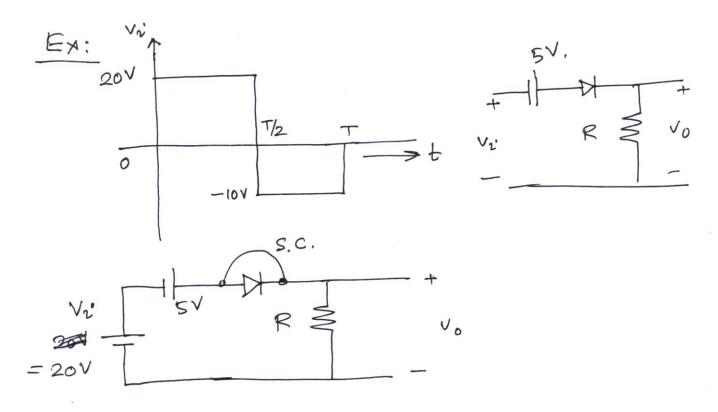
For transition level,

$$-V_{1}-5=0$$

$$V_{1}=-5$$

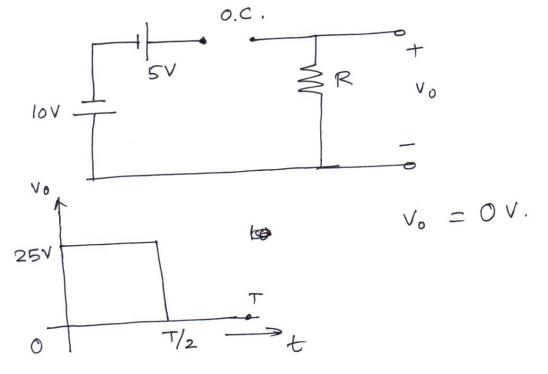
For Vi more negetive than -5V, Diode is OFF more +ve " -5V Diode ON

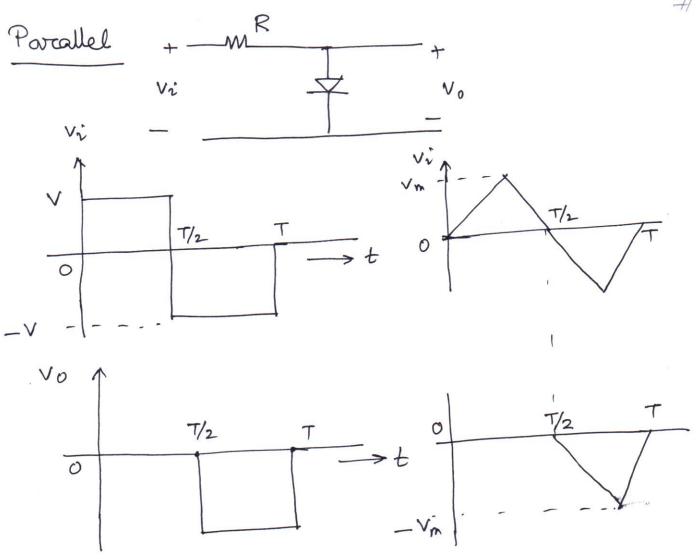


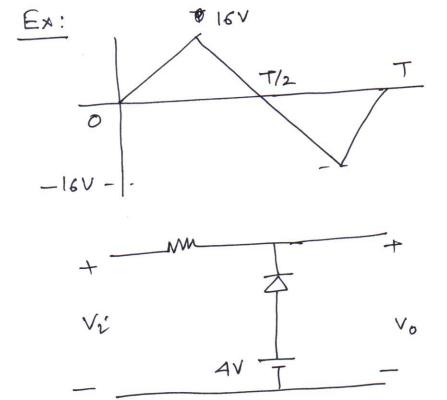


For
$$V_{i} = 20V$$
 $(0 \rightarrow 7/2)$, Diode is S.C. $V_{0} = 25V$.

For $V_{ii} = -10 \, \text{V}$, Diode is off / 0, cld. $V_{0} = 0 \, \text{V}$.

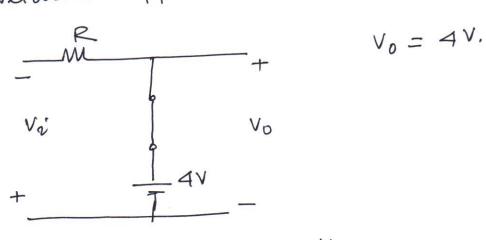






Diode will be ON for -ve region of ê/p.

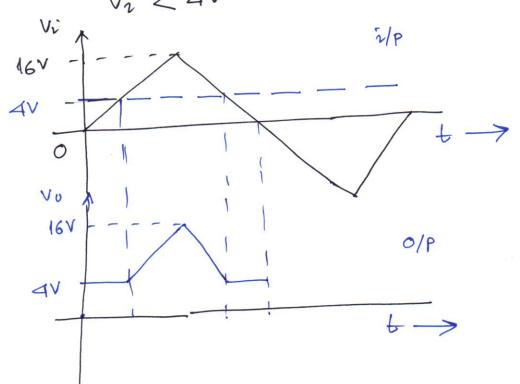
Network appears as



transition state to

 $-v_1 + 4 = 0$ $v_2 = 4 v.$

i/ρ Vi > 4V Vi < 4V Diode goes OFF Diode is ON.



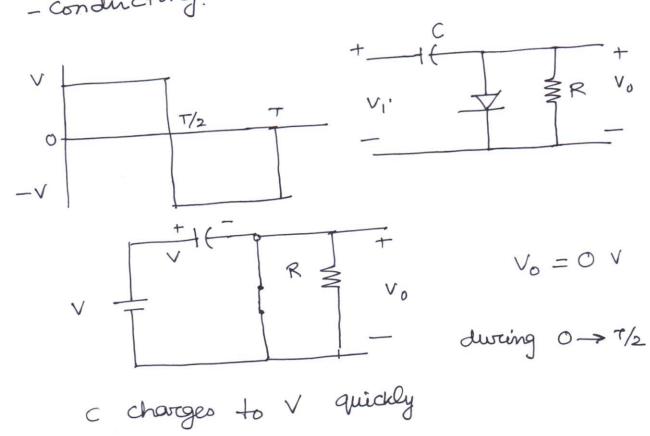
CLAMPERS

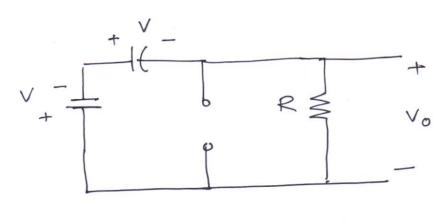
The clamping network will 'clamp' a Signal to a different d.c. level.

The Network will have a capacitor,

2+ com have an independent d.C. supply to introduce additional shift.

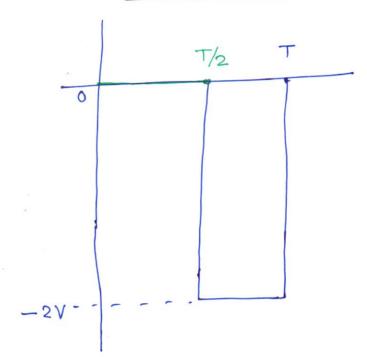
R&C chosen such that &= RC is large enough to ensure that the voltage across the capacitor does not discharge segnificantly, dwang the interval when diode is non-- conducting.





$$\vee_0 = -2 \vee$$

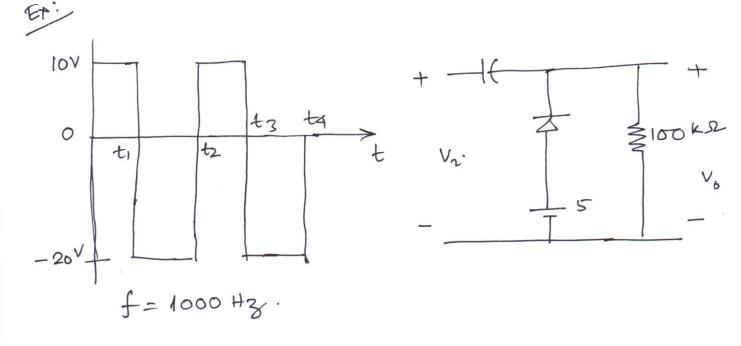
% wave form.



 $V_0 = -2V$.

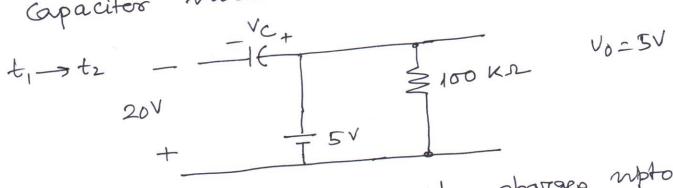
RC product is sufficiently large to establish a discharge period of 50 much greater than 7/2 -> T, greater than 7/2 -> T, therefore, voltage (V= 0/c) during this period. Therefore, voltage (V= 0/c) during this period.

 $+V +V +V_0 = 0$ Total swing of 0/P or. $V_0 = -2V$. = Total swing of i/P



$$5 + ep - 1$$
 $0 - t_1 = 0.5 ms$,
 $f = 1000 Hz$ period = 1 ms.

- Start the analysis by considering that part of i/p signal which will find bias the diode so we stort $t_1 \rightarrow t_2$
 - · During the period whom is diode is ON'
 Corpacitor will charge up enstantaneously.
 - During the period when diode is OFF' apacitor holds on its voltage level.



20
$$-Vc+5=0$$
 Corpacitor charges mpto
 $Vc=25V$ $Vo=5V$
 $t_1\rightarrow t_2$

$$t_{2} \longrightarrow t_{3} \quad \begin{array}{c} 25V \\ + \\ \hline 10 \end{array}$$

$$-10-25+0=0$$
 or $v_0=35V$ t_2-t_3 , $v_0=35V$

Time const for the discharging n/w T = RC = 100 × 10 × 0.1 × 10 = 10 ms

R=100 KR C= 011 MF

total discharge time = 52 = 50 ms.

