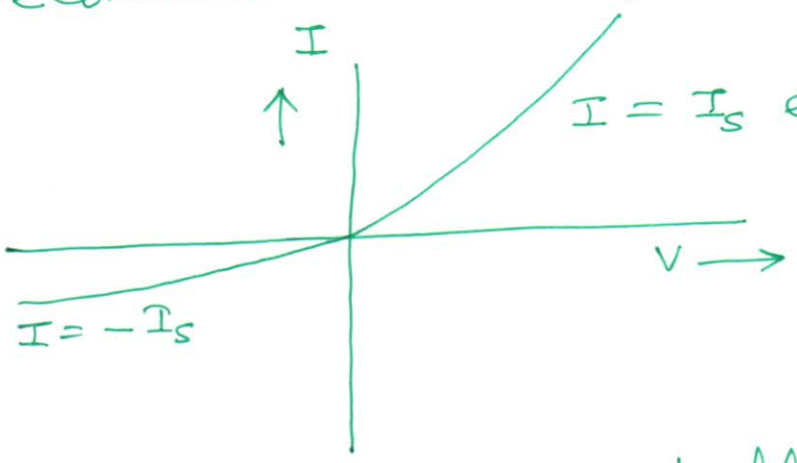
Diode current

$$I = I_S \left(e^{V/V_T} - 1 \right)$$

$$I = I_S \left(e^{V/\eta V_T} - 1 \right)$$

$\eta = 1$ for Ge, $\eta = 2$ Si.

$\eta \rightarrow$ Due to charge generation and recombination at space charge region.



under fwd bias : ct flows following $I = I_S e^{V/\eta V_T}$, it is exponential.

This ct is mainly due to diffusion.

Diffusion current does not obey Ohm's Law

Under Reverse Bias :

As the applied rev bias is large or higher than $V_T = 0.026V$ e^{-V/V_T} is negligible.

$\boxed{I = -I_S}$ ⇒ Reverse saturation current. and it is const. (at a given temp)

Ge and Si have cut in voltages of 0.3V and 0.7V. below which there is no current.

Cut in voltage or threshold voltage.

V_T =	0.7	Si
V_T =	0.3	Ge

Beyond the cut in voltage, the current rises rapidly (exponentially).

There is a delay in Si on account of $\eta = 2$, diffusion rate is low

At high voltages η becomes 1.

The rev. saturation ct I_S doubles every 10°c rise in temp.

For same temp rise Ge develops a much larger increase in reverse ct than Si.

I_S is in the order of 1–2 μA.

Si Vs Ge

Si : Higher PIV
Higher current rating
wider temp ranges

Si PIV — 1000 V operating temp 200°C

Ge PIV — 400V operating temp 100°C

V_T for Si 0.7 V

V_T for Ge 0.3 V.

Increased value of V_T in Si is due to the factor η.

At very low current η plays imp role.

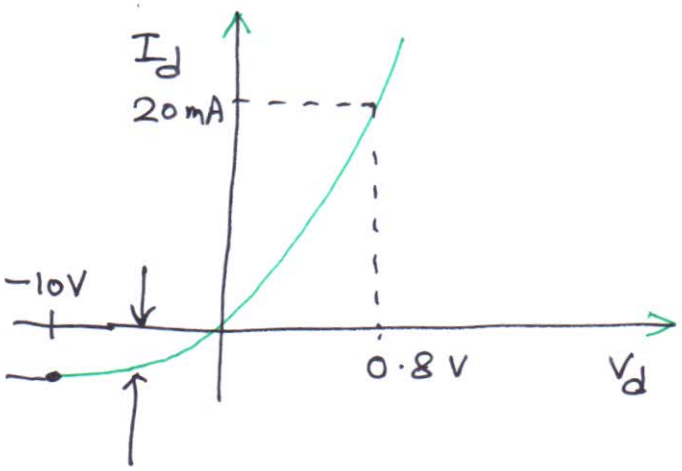
Once the curve starts vertical rise η drops to 1.

Ge — Higher freq applications

Si — Lower freq application.

Diode Resistance

DC Resistance

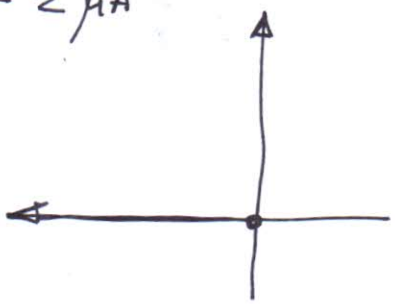


$$R_{dc} = \frac{V_D}{I_D} = \frac{0.8}{20\ mA}$$

$$= 40\Omega$$

Reverse $R_{dc} = \frac{-10\ V}{-2\ \mu A}$

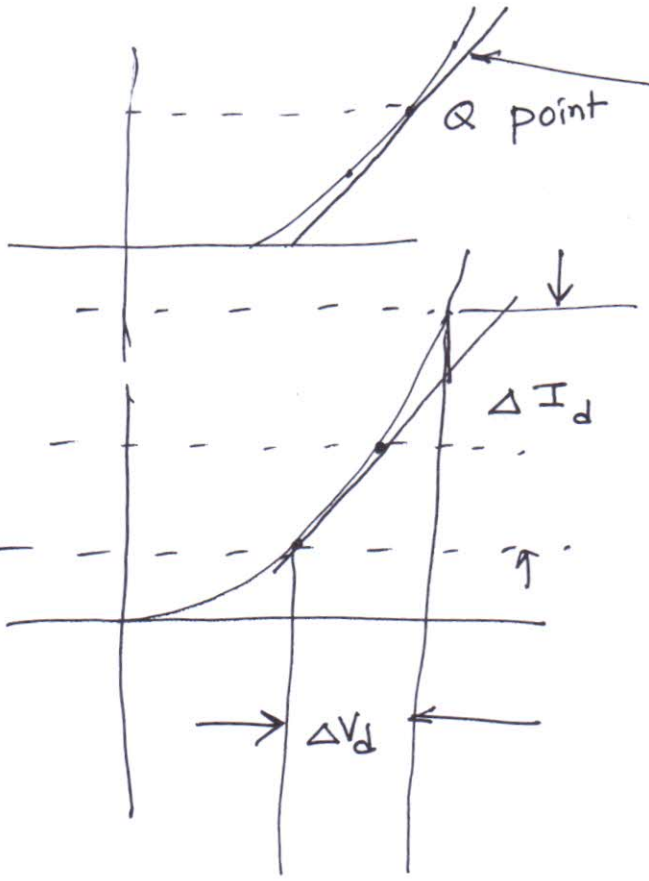
$$= 5\ M\Omega$$



R_{dc} (ideal) $= 0$

R_{dc} (rev) $= \frac{-10}{0} = \infty$

AC Resistance (Dynamic Resistance)

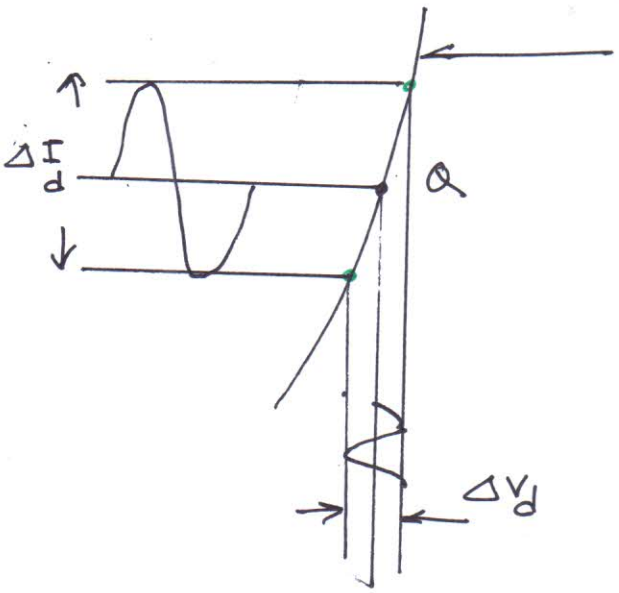


$r_d = R_{ac}$

$$R_{ac} = \frac{\Delta V_d}{\Delta I_d}$$

$$I = I_o \left(e^{V/\eta V_T} - 1 \right)$$

$$g = \frac{dI}{dV} = \frac{I_o\, e^{V/\eta V_T}}{\eta V_T}$$



A st. line drawn tangent to the curve through the Q point, A particular change in voltage and current can be used to define ac resistance or dynamic resistance.

An effort should be made to keep the change in voltage and current as small as possible. and equidistant to either side of Q point.

- Steeper the slope → less the value of ΔV_d for the same change in ΔI_d and the less the resistance
- AC resistance in the vertical-rise region of the characteristic is quite small, while ac resistance is much higher at low ct levels.

Lower the Q point (smaller ct or voltage), the higher the ac resistance.

$$I = I_0\left(e^{V/\eta E_T} - 1\right) \qquad E_T = \frac{kT}{q} = 26\ mV$$

$$\frac{dI}{dV} = \frac{I_0\, e^{V/\eta E_T}}{\eta E_T} \qquad I_0 e^{V/\eta E_T} = I + I_0$$

$$g = \frac{dI}{dV} = \frac{(I + I_0)}{\eta E_T}$$

$$\text{or} \quad r_{ac} = \frac{\eta E_T}{I + I_0}$$

- For a reverse bias greater than a few tenths of a volt $\frac{V}{\eta E_T} \gg 1$

  g, small, r_{ac} is very high ~ MΩ

$$g = \frac{I + I_0}{\eta E_T}$$

- For forward bias greater than a few tenth of a volt $I \gg I_0$ i.e. g is high

$$g = \frac{I}{\eta E_T} \rightarrow r_f = \frac{\eta E_T}{I} = \frac{26}{I\ (mA)}, \quad \eta = 1$$

For a ct of 1 mA, forward $r_f = 26\ \Omega$

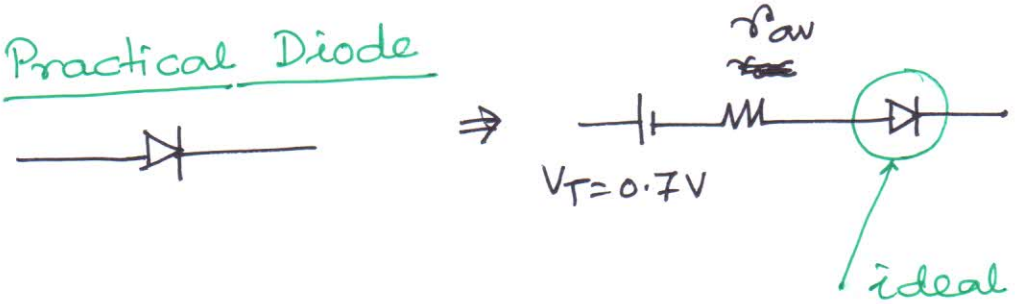
and for $I = 26$ mA $r_f = 1\ \Omega$

$r_b : r_f$

$4 \times 10^5 : 1$	for Ge
$1 \times 10^6 : 1$	for Si

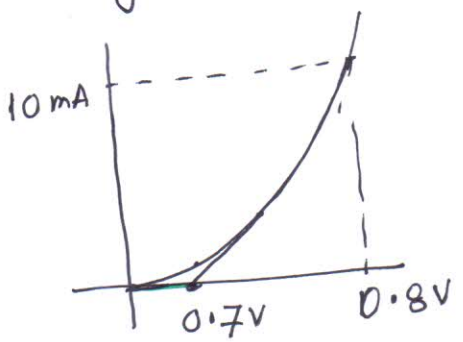
Diode Equivalent ckt

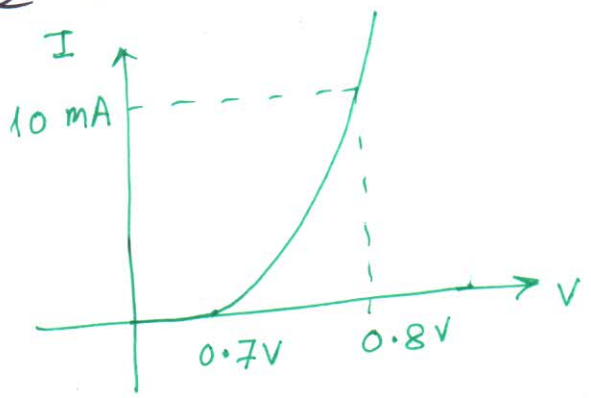
① Practical Diode



Si diode does not reach the conduction state until V_D reaches 0.7 V. with a fwd bias.

A battery V_T specifies that voltage across device must be greater than V_T before conduction through the device in the direction dictated by ideal diode is established.

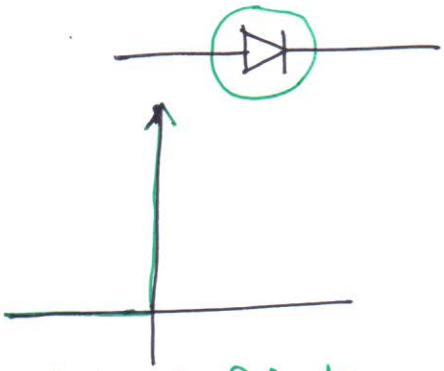




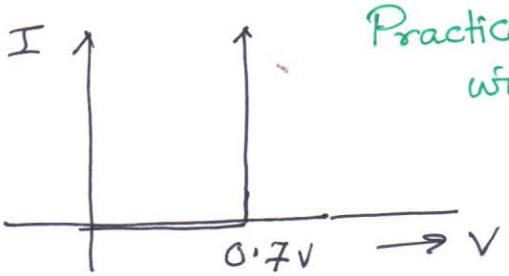
$$r_{av} = \frac{\Delta V_d}{\Delta I_d} = \frac{10 - 0}{0.8 - 0.7} =$$

$$= \frac{0.8 - 0.7}{(10 - 0)\ mA} = 10\ \Omega$$

Ideal Diode

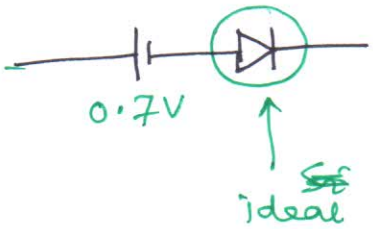


ideal Diode



Practical Diode with $r_{av} = 0$

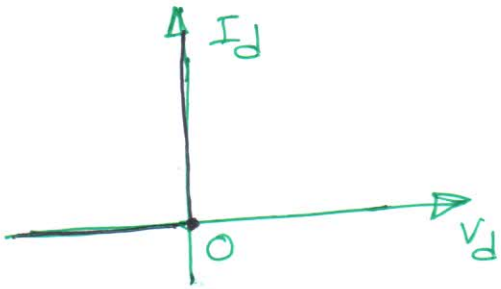
Si Diode



ideal ~~Si~~ Diode

② Simplified Eqv ckt when r_{av} is small

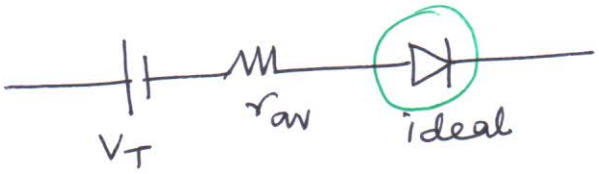
③ Ideal Eqv ckt

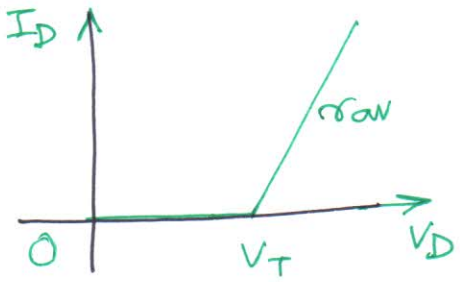


Ideal diode and its characteristics

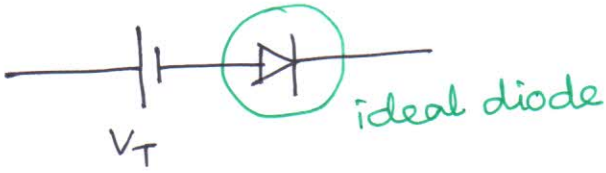
Diode Equivalent ckts

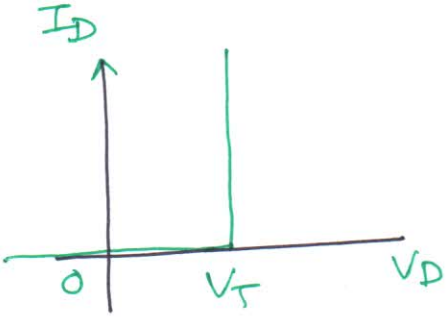
(1)





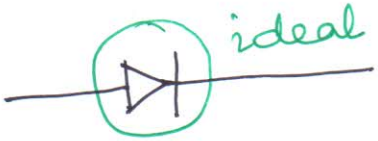
(2)

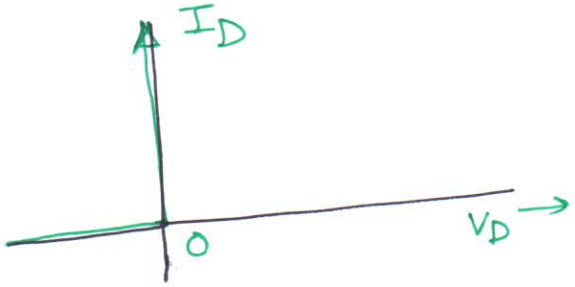




$R_{network} \gg r_{av}$

(3)



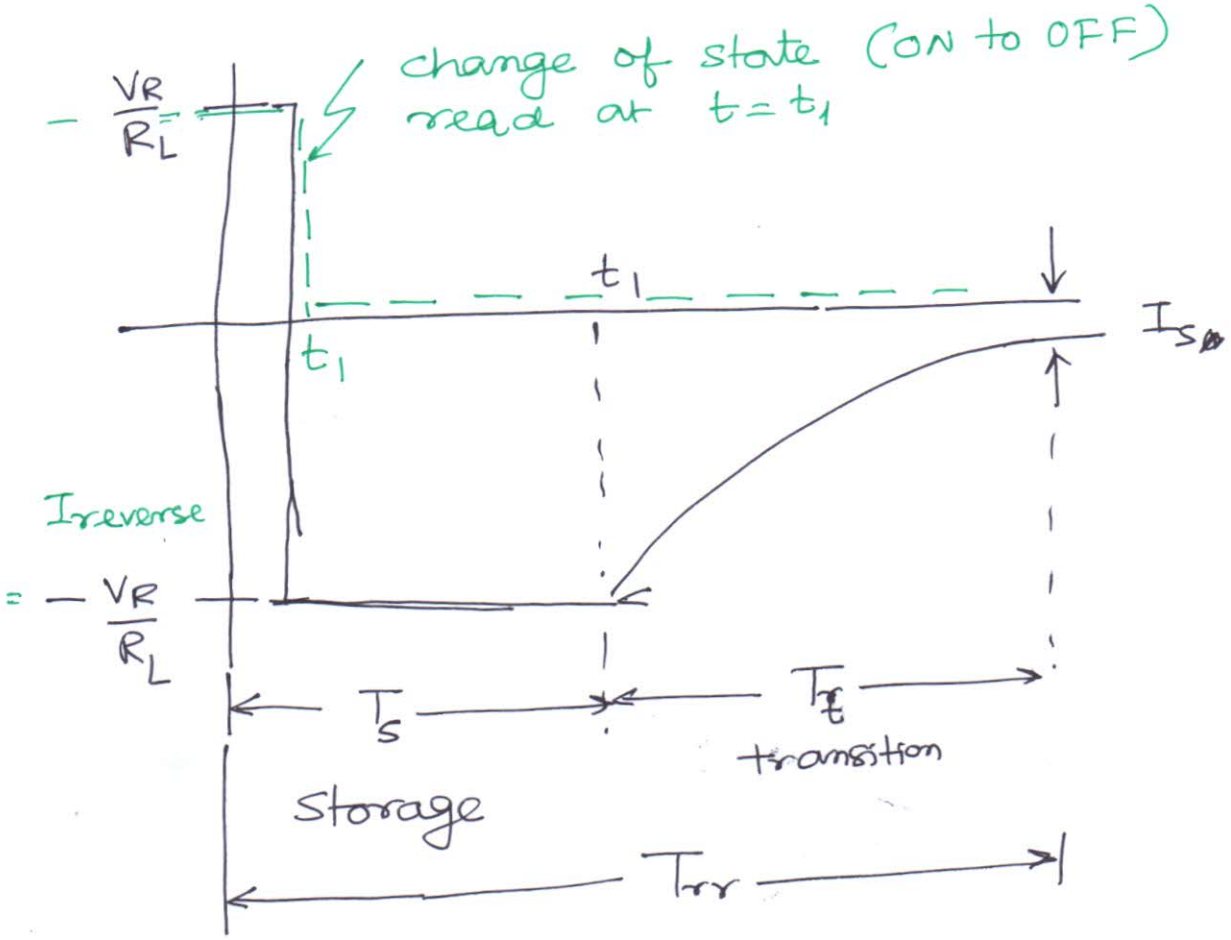


$R_{network} \gg r_{av}$

$E_{network} \gg V_T.$

Diode as a Switch

Reverse recovery time



In fwd bias Large no. of electrons from 'n' move to 'p' and a large no. of holes move to 'n'. The electrons in p and holes progressing in 'n' establish a large minority carrier ct.

If applied voltage is reversed, diode will change from the conduction state to non conduction state.

However due to presence of large number of minority carriers in each material (p or n), the diode ct will simply reverse. as shown $(-V_R/R_L)$ and stay at this level for the period of time T_s (storage time) required for minority carriers to return to their majority-carrier state. in opposite material. Diode will remain in the short ckt state with a current $I_{reverse}$ determined by the network parameters.

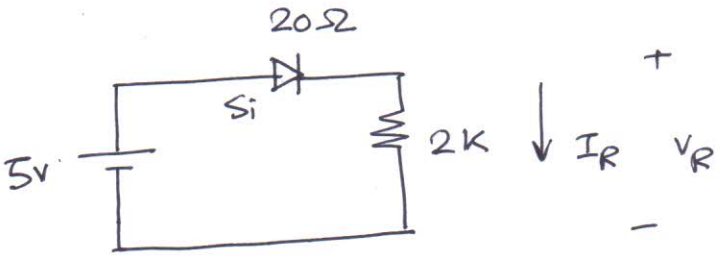
Eventually, after T_s, ct will reduce to a level associated with non conduction state.

The second time: t_t (transition time).

Reverse recovery time $T_{rr} = T_s + T_t$

It is imp considerations in high freqency application / high speed switch application.

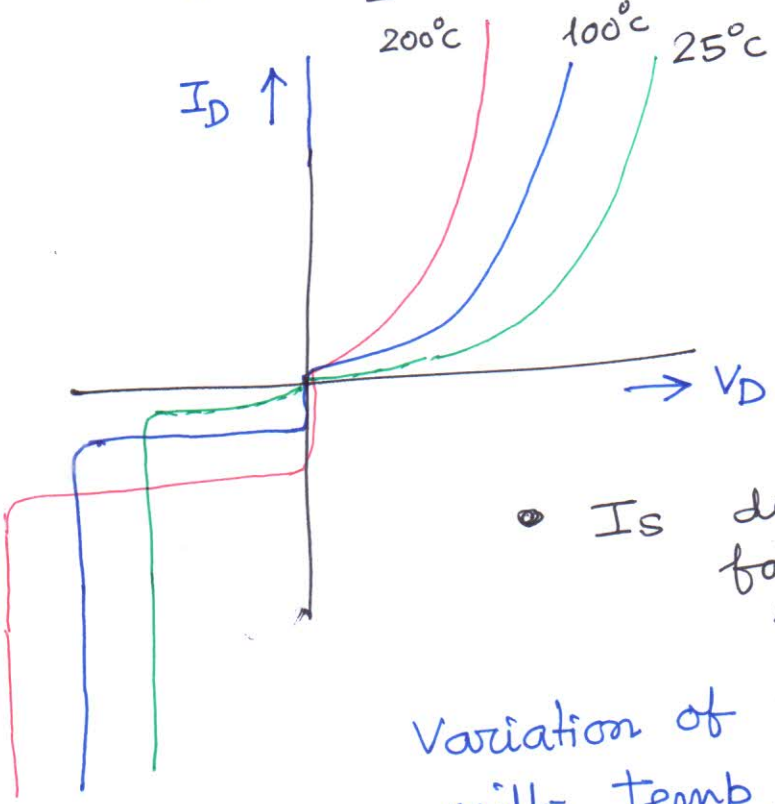
Most commercially available switching diodes have T_{rr} in the range of few nano sec to 1 μsec. T_{rr} with a few hundred pico sec is also available.



$V_R = 5 - 0.7 = 4.3\ V$

$I_R = \frac{4.3}{2} = 2.15\ mA$

$2K \gg 20\Omega$



Temp Effect

- I_S doubles in magnitude for every 10°C increase in temp.

Variation of Diode characteristic with temp.

- As temp increases the forward voltage drop V_T reduces but the saturation ct level increases.
- I_S ~ 1 or 2 μA at 25°C for Ge
  ~ 100 μA = 0.1 mA at 100°C

Typical values of I_S for Si are much lower than that of Ge for similar power and current levels.

- Even at high temp, I_S for Si diodes do not reach the same level of Ge.

Diode Specification

1. Forward voltage V_F (at a specified ct and temp).
2. Max forward ct I_F (Specific temp)
3. Max reverse saturation ct I_R (at speaific voltage and temp)
4. PIV or PRV
5. Maximum power dissipiation level at a particular temp.
6. Capacitance level.
7. Reverse recovery time
8. Operating temp range.

$P_{Dmax} = V_D I_D$

V_D : voltage at a particular point of operation

I_D : Diode ct.

Diode Capacitance

Transition and Diffusion Capacitance

Electronic Devices are sensitive to high frequencies.

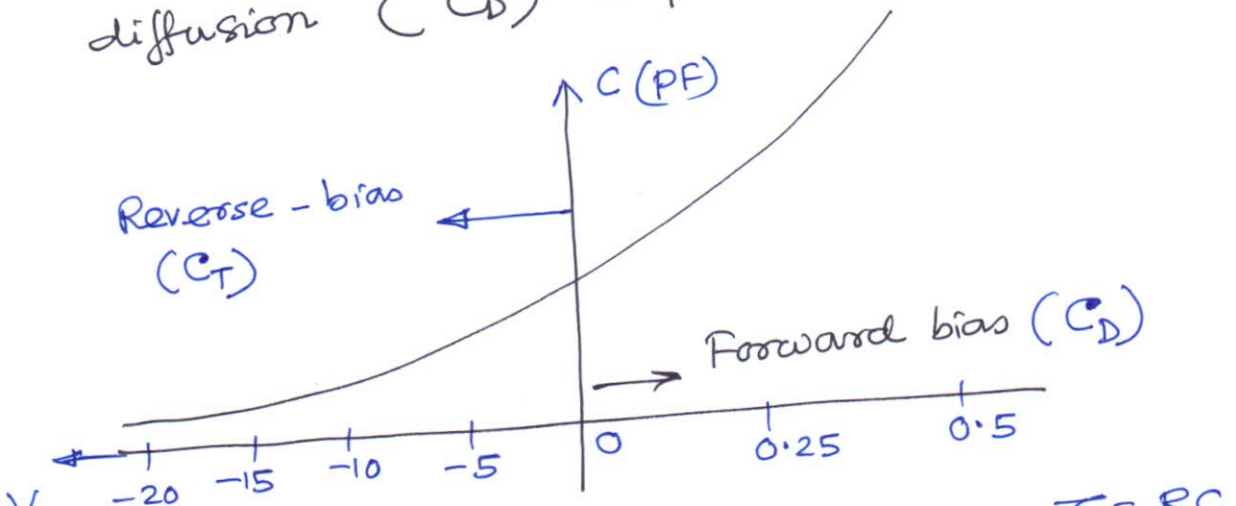
$X_C = \frac{1}{2\pi fC}$ is very large when f is small.

(open ckt).

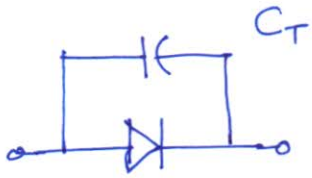
At high frequency, f is high X_C low

In p-n semiconductor diode, two capacitive effects are considered.

In reverse-bias region we have transition or depletion-region capacitance (C_T) while in forward-bias region we have diffusion (C_D) capacitance.



$\tau = RC$



Capacitance of a parallel plate capacitor

$C = \frac{\epsilon A}{d}$, ϵ permittivity of dielectric

In the reverse bias region, there is a depletion region (free of carriers) which behaves essentially like an insulator / dielectric.

Depletion width (d) increases with increase in reverse bias, so transition capacitance C_T reduces.

Capacitance (C_T) depends on applied reverse bias.

In Fwd bias: Capacitance effect directly dependent on the rate at which charge is injected into regions outside the depletion region.

Increased levels of ct ⟶ increased levels of diffusion ~~ct~~. capacitance.

Increased ct. level reduces associated resistance, resulting time const $\tau = RC$ does not become excessive. τ is imp in high speed application.