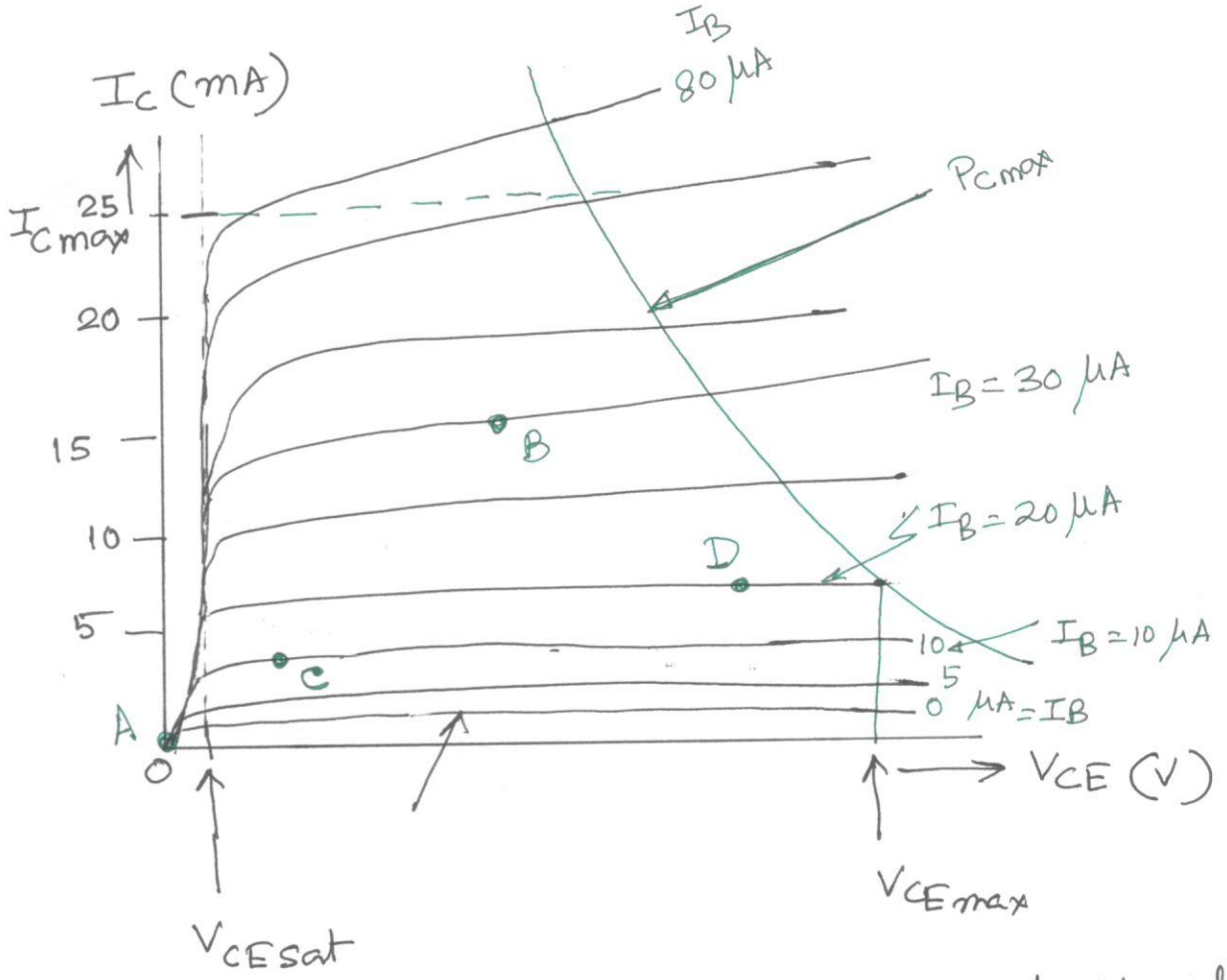
DC Biasing — BJT

- BJT to amplify i/p AC signal
- Improved output AC power level is the result of a transfer of energy from the applied dc supplies.
- The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics.

- Biasing : Application of dc voltages to establish a fixed level of current and voltage.

For transistor amplifiers, the resulting dc current and voltage establish an operating point on the characteristics which define the region that will be employed for amplification of the applied signal.

- Operating point is a fixed point on the characteristics, it is also called the quiescent point or Q point.



various operating points with in limits of operation of a transistor.

- The biasing ckt can be desegined to set the device operation at any of these points (A, B, C, D) or others with in the active region.

- Note the maximum rating I_{cmax}: a horizontal line drawn at I_{cmax}

A vertical line at max collector to Emitter voltage $V_{CE max}$. The max power constraint is defined by the curve P_{cmax}

- At the lower end of the scales are the cut off region, defined by $I_B \leq 0\,\mu A$ and saturation region defined by

$$V_{CE} \leq V_{CE\,sat}$$

- If no bias were used, the ~~dot~~ device would initially be completely OFF, resulting in a Q point at A.

- At 'B', if a signal is applied to the ckt, the device will vary current and voltage from operating point for both positive and negetive excursions of the i/p signal.

- Point 'C' would allow some positive and negetive variation of the output signal, but peak to peak value would be limited by proximity of $V_{CE} = 0\,V$, $I_C = 0\,mA$. Operating at C also raises concern about nonlinearity introduced by the fact that spacing between I_B curve is changing rapidly.

- Point D sets the device operating point near the maximum voltage and power level.

- Point 'B' is a region of more linear spacing and therefore more linear operation.

Thus point 'B' seems the best operating point interms of linear gain and largest voltage and current swing possible.

This is usually the desired condition for small-signal amplifier.

Having selected the operating point and biased the BJT at a desired operating point, the temparcature must also be taken into account.

Temp causes β_{dc} and I_{CEO} to change. Higher temps result in increased leakage ct in the device, thereby changing the operating condition set by the biasing N/W.

- Network design must also provide a degree of temparature stability so that temparature changes result in minimum changes in the operating point.

- Maintainance of the operating point can be specified by a stability factor S.

- For BJT to be biased in its linear or active operating region

1. The base emitter - jn must be forward biased with a resulting forward-bias voltage of about 0.6 to 0.7 V

2. The base collector jn must be reverse-biased

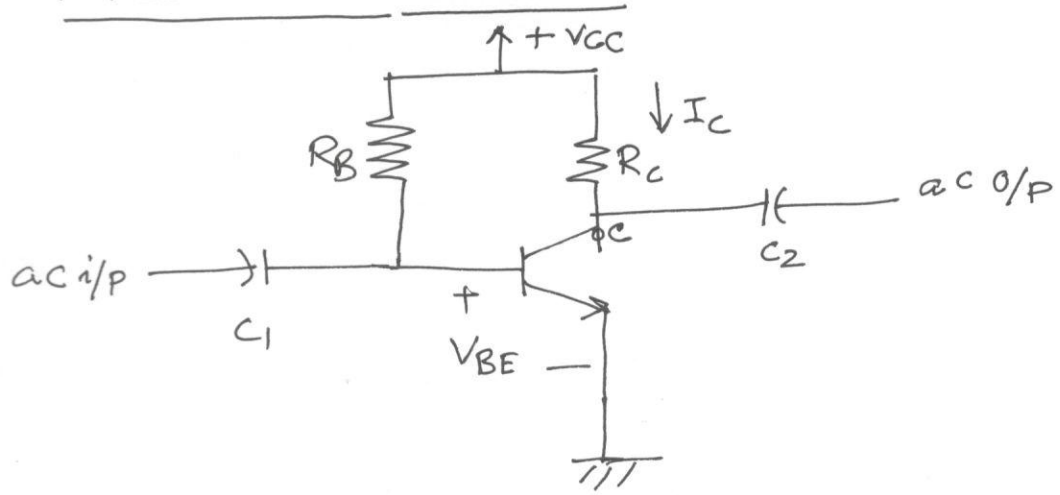
(A) Linear region operation
(1) Base emitter jn forward biased
(2) Base collector jn reverse biased

(B) Cut off region operation
Base emitter jn reverse biased

(C) Saturation - region operation
Base - emitter jn forward biased
Base - collector jn forward biased.

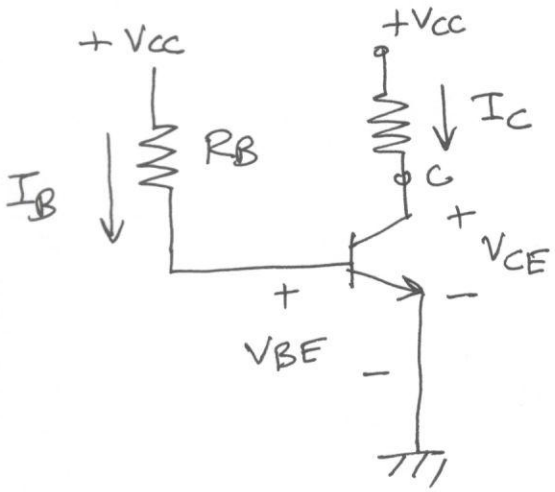
TRANSISTOR BIASING

Fixed Bias Circuit

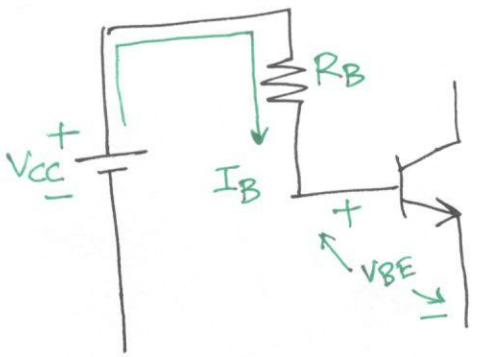


DC Analysis

replace the capacitor by open ckt.



D.C Equivalent Ckt.



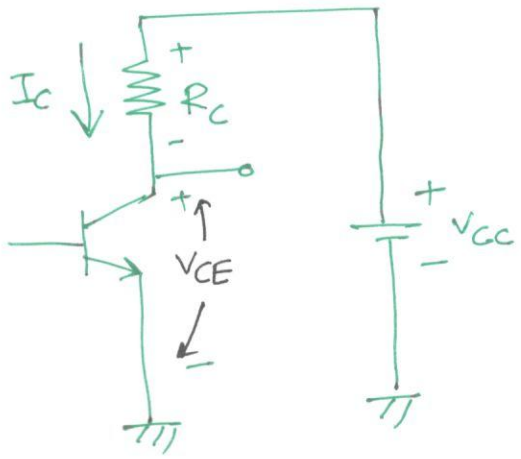
Base emitter Loop

Forward Bias of Base-Emitter

$$-V_{CC} + I_B R_B + V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$I_C = \beta I_B$



Collector Emitter Loop

$$-V_{CC} + I_C R_C + V_{CE} = 0$$

or $$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

$$V_{CE} = V_C - V_E$$

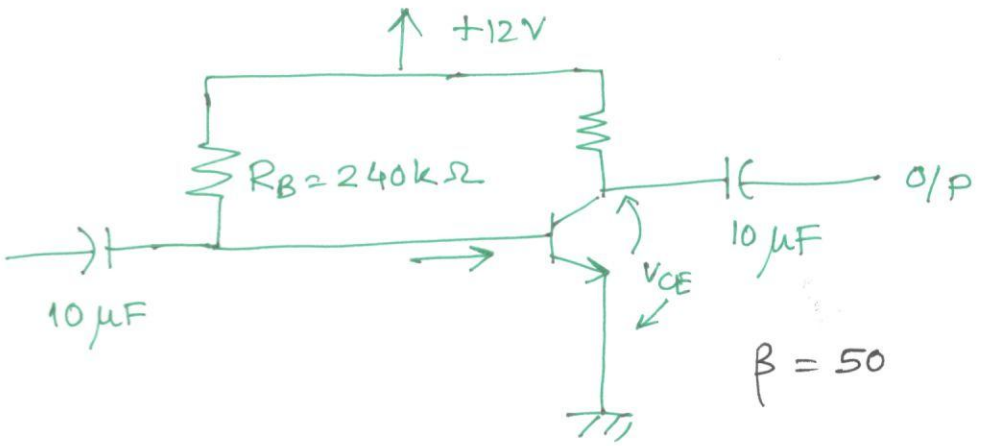
V_C : voltage of collector w.r.t ground.

V_E : voltage of Emitter w.r.t ground

Here $V_E = 0$

$$V_{BE} = V_B - V_E = V_B \quad \text{(present case)}$$

Ex:



(a) $I_{BQ} = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{12 - 0.7}{240} = 47.08\,\mu A$

(b) $I_{CQ} = \beta I_{BQ} = 50 \cdot (47.08\,\mu A)$

$= 2.35\,mA$

(b) $V_{CEQ} = V_{CC} - I_C R_C$

$= 12 - (2.35 \times 2.2)$

$= 6.83\,V$

(c) $V_B = V_{BE} = 0.7\,V$

$V_C = V_{CE} = 6.83\,V$

(d) $V_{BC} = V_B - V_C = 0.7 - 6.83\,V$

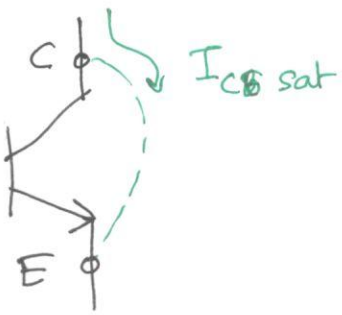
$= -6.13\,V$

-ve sign indicates that the jn is reversed biased.

Transistor Saturation

Saturation region is usually avoided because the base collector jn is no longer reverse biased and output amplified signal will be distorted.

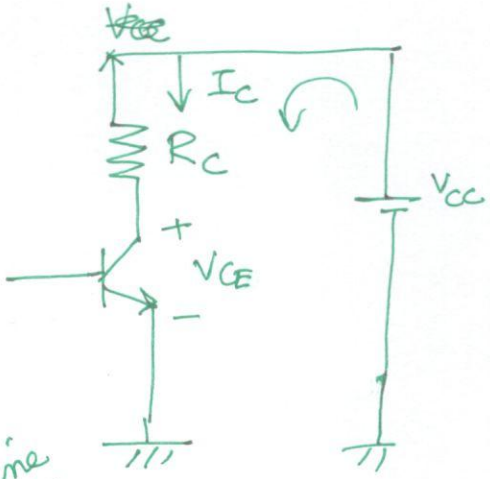
The collector to emitter voltage (V_{CE}) is at or below $V_{CE\,sat}$.



$$I_{C\,sat} = \frac{V_{CC}}{R_C}$$

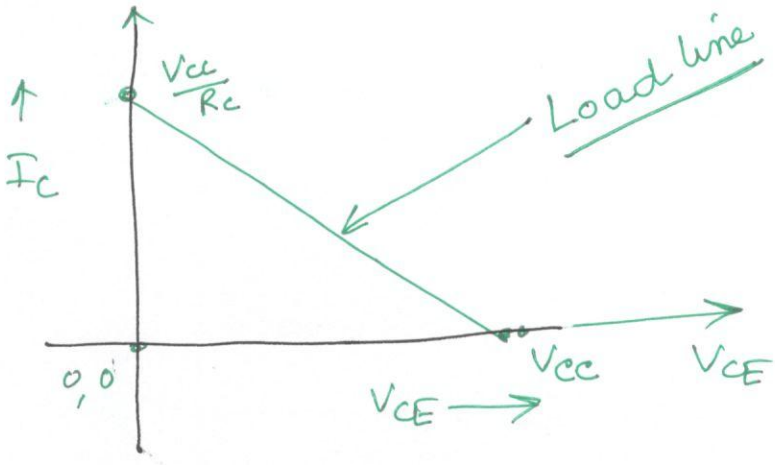
Thus we can determine the saturation current for fixed bias configuration.

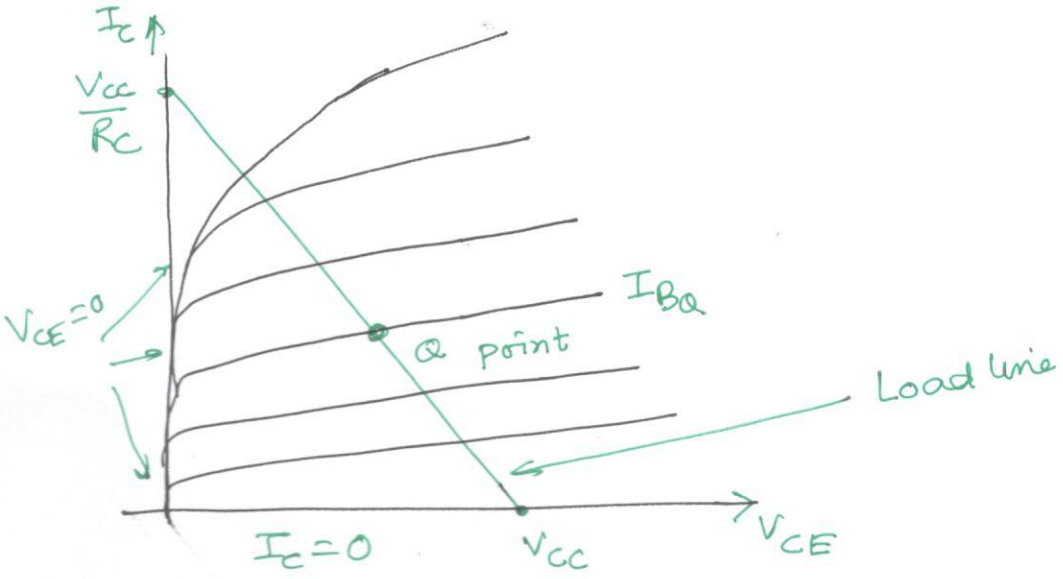
Load Line Analysis

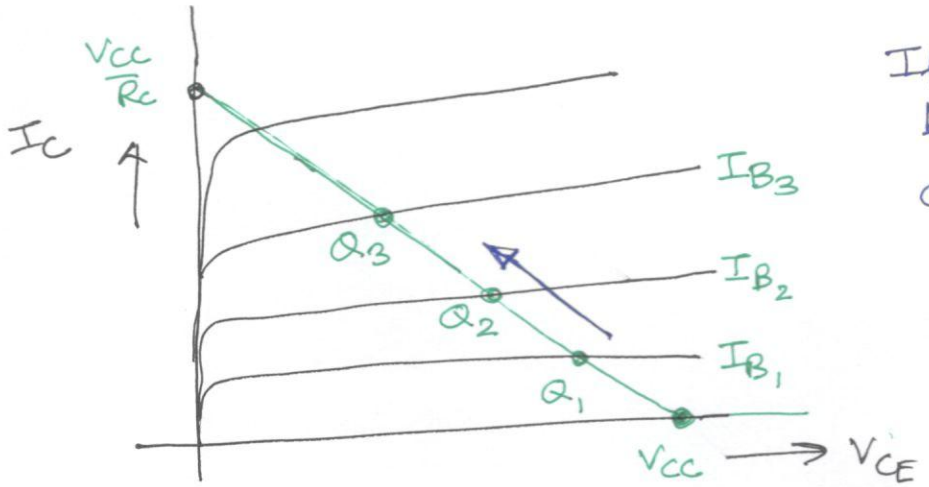


$$-V_{CC} + I_C R_C + V_{CE} = 0$$

or. $$I_C R_C = V_{CC} - V_{CE}$$

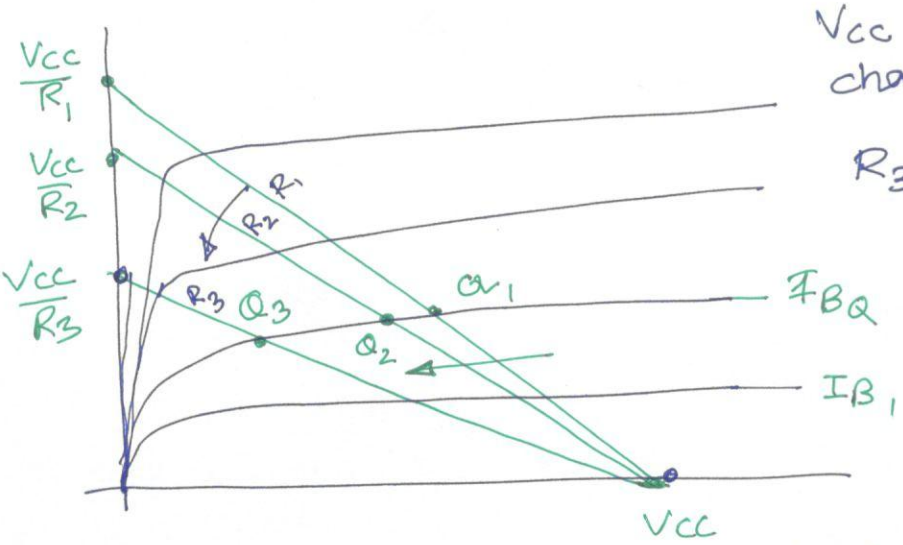






If I_B is changed by varying R_B Q point shifts

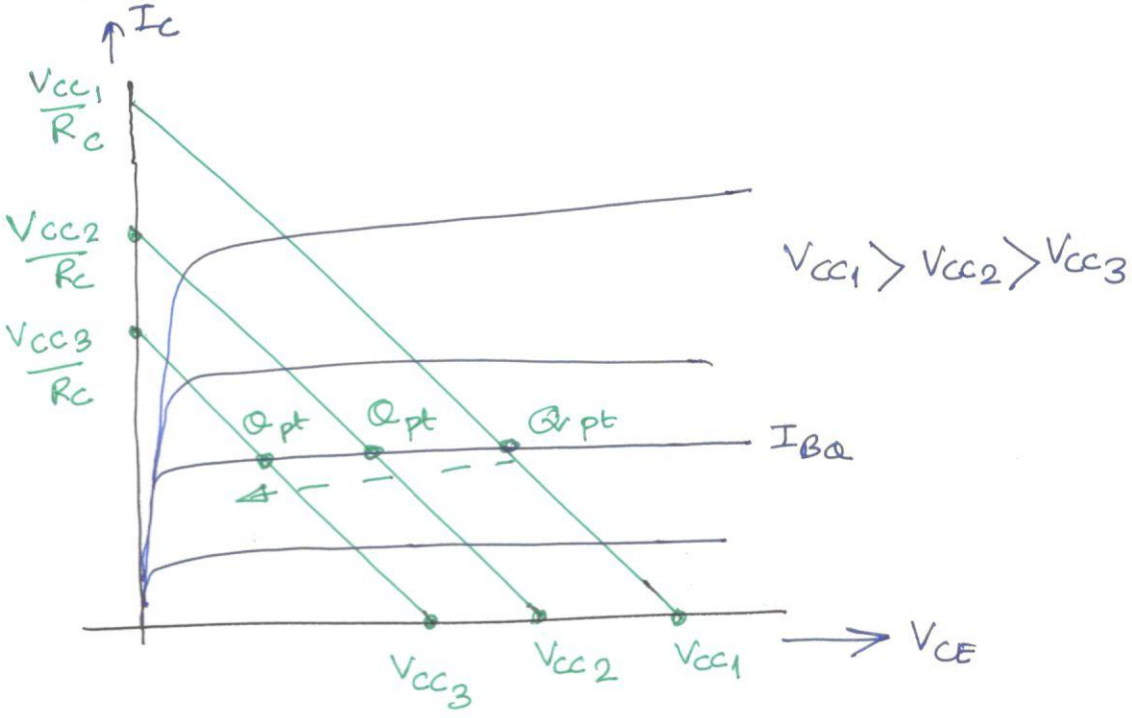
Movement of Q point with increasing I_B



V_{CC} is fixed, R_C changed, Load line changes

$R_3 > R_2 > R_1$

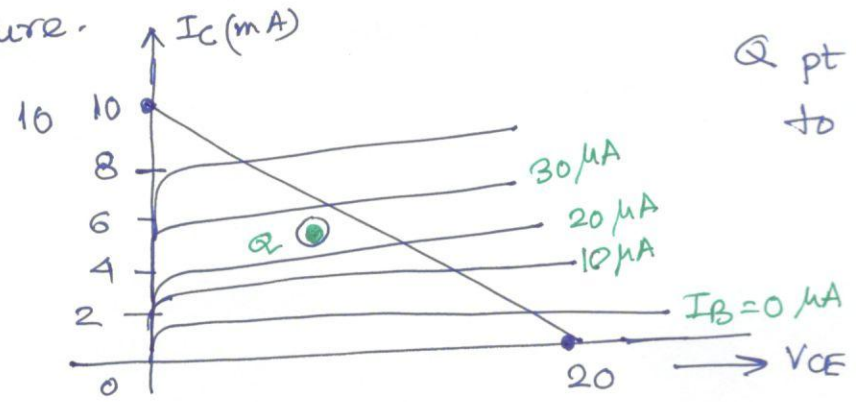
Effect of increasing levels of R_C on load line and Q point



Effect of variation of V_{CC} on Load line

If R_C is fixed and V_{CC} is varied the Load line shifts as shown above.

If the base at I_{BQ} is fixed, the Q point is shifted as shown in the figure.



Q pt corresponds to $I_B = 25\,\mu A$

$V_{CC} = 20V$ $\quad \frac{V_{CC}}{R_C} = 10$ $\quad$ or. $R_C = \frac{20}{10\,mA} = 2K\Omega$

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $\quad$ or $\quad R_B = \frac{20 - 0.7}{25\,\mu A} = 772\ k\Omega$

Bias stabilization

In any amplifier employing a transistor the collector current I_C is sensitive to the following parameters

(i) change in β

As I_B is fixed, variation in β shifts I_C

as $I_C = \beta I_B$, operating point is shifted.

AC signal may be shifted / swing to saturation or cut off

(ii) change in temp

$$I_C = \beta I_B + I_{CBO}(\beta+1)$$

(a) β varies with temp doubling from 25°C to 100°C

(b) V_{BE} changes due to temp

$|V_{BE}|$ decreases about 7.5 mV per °C increase in temp.

(c) I_{CO} or I_{CBO} doubles every 10°C increase

↑ in temp ⟶ may cause thermal runaway

In Si $I_{CO} \approx nA$, while in Ge, $I_{CO} \approx mA$

In Ge, thermal runaway is a problem.

Stability Factor Analysis

$$I_{CQ} = I_{CQ}(I_{CBO}, V_{BE}, \beta, \cdots)$$

I_{CQ} depends on I_{CBO}, V_{BE}, β etc.

These variables may undergo change

$$dI_{CQ} = \frac{\partial I_{CQ}}{\partial I_{CBO}} dI_{CBO} + \frac{\partial I_{CQ}}{\partial V_{BE}} dV_{BE} + \frac{\partial I_{CQ}}{\partial \beta} \cdot d\beta + \cdots$$

$$S_I = \left.\frac{\Delta I_{CQ}}{\Delta I_{CBO}}\right|_{\beta, V_{BE}}$$

$$S_V = \frac{\Delta I_{CQ}}{\Delta V_{BE}}$$

$$S_\beta = \frac{\Delta I_{CQ}}{\Delta \beta}$$

If the changes in the independent variables are small, then $S_I = \frac{\partial I_{CQ}}{\partial I_{CBO}}$

$$S_V = \frac{\partial I_{CQ}}{\partial V_{BE}}, \quad S_\beta = \frac{\partial I_{CQ}}{\partial \beta}$$

and $\Delta I_{CQ} \cong \partial I_{CQ}$, $\Delta I_{CBO} \approx \partial I_{CBO}$ $\Delta\beta \simeq \partial\beta$

Therefore $\Delta I_{CQ} \approx S_I \Delta I_{CBO} + S_V \Delta V_{BE} + S_\beta \Delta\beta + \cdots$

$$S_I = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$I_C = \beta I_B + (\beta+1) I_{CO} \qquad I_{CO} = I_{CBO}$$

$$\frac{\partial I_C}{\partial I_C} = \beta \frac{\partial I_B}{\partial I_C} + (\beta+1) \frac{\partial I_{CO}}{\partial I_C}$$

$$\text{or. } 1 = \beta \frac{\partial I_B}{\partial I_C} + \frac{(\beta+1)}{S_I}$$

$$\text{or. } S_I = \frac{\beta+1}{\left[1 - \beta \frac{\partial I_B}{\partial I_C}\right]}$$

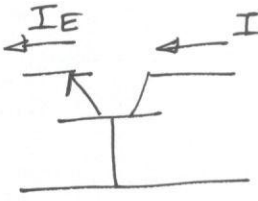
for fixed Bias ckt. I_B is independent of I_C

$$\boxed{S_I = (\beta+1)}$$

If $\beta = 50$, $S_I = 51$ i.e. $I_C = 51\, I_{CO}$

Value of S above 25 is unsatisfactory

In CB



$$I_C = \alpha I_E + I_{CO}$$

$$S_I = \frac{\partial I_C}{\partial I_{CO}} = 1$$