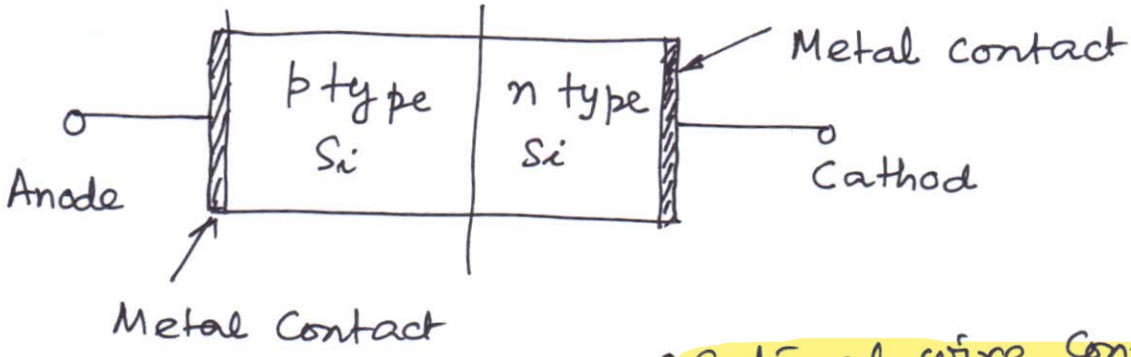
PN Junction with Open-Circuit

p-type semiconductor (Si) brought into close contact with an n-type semiconductor.

In actual practice, both p and n regions are part of same silicon crystal. i.e. p-n jn is formed in a single Si crystal. by creating regions of different dopings (p and n regions).



• external wire connected to via metal (Aluminium) contacts.

• For p-n jn diode, these constitute diode terminals

Operation with open ckt

• External terminals are left open

"+" in p-type material ⇒ majority holes

The charge of these holes is neutralized by an equal amount of bound -ve charge associated with acceptor atom.

Bound charges are not shown.

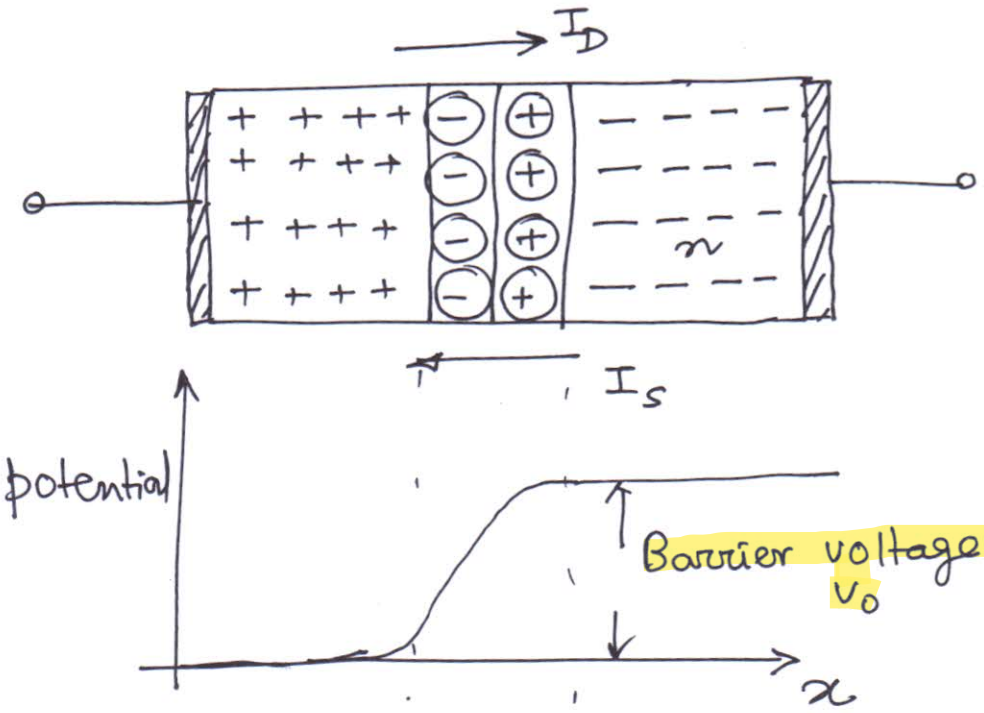
In n-type material ⇒ majority electrons indicated by "—" signs.

Bound positive charge, which neutralizes the charge of majority electrons is not shown.

In p type : minority electrons generated by thermal ionization

In n type : minority holes generated by thermal ionization.

(Minority carriers are not shown)



Diffusion current (I_D) : Due to majority carrier

Hole diffuses from p side to n side across jn

Electrons diffuse from n side to p side "

Two component add to form I_D

$I_D \longrightarrow$ hole diffusion from p to n
electron diffusion from n to p

Direction of ct : from p to n

Depletion Region

holes diffuse across jn quickly recombine with some majority 'e' present and thus disappear
Some free 'e' disappear from 'n' type material.
Bound +ve charge will no longer be neutralized by free electrons, this charge is said to be uncovered.
Region close to the jn is depleted of free electrons and contains uncovered bound +ve charge.

Electrons which diffuse across the junction into p region quickly recombine with some of majority holes and disappear.
Some majority holes disappear ⇒ some bound negetive charge uncovered (no longer neutrilized by holes).

Thus in 'p' material close to junction region depleted of holes.

Carrier-depletion region on both side of the junction.

Space charge region 'n' side +ve ly charged and 'p' side negetively charged.

An electric field is established from n to p

A potential difference across the depletion region with n side +ve ~~and~~ voltage relative to p side appears. called as Barrier potential or Barrier voltage

Resulting Electric field opposes diffusion of 'e' from n to p and holes from 'p' to 'n'.

Appearance of the barrier voltage V_0 limits carrier diffusion process.

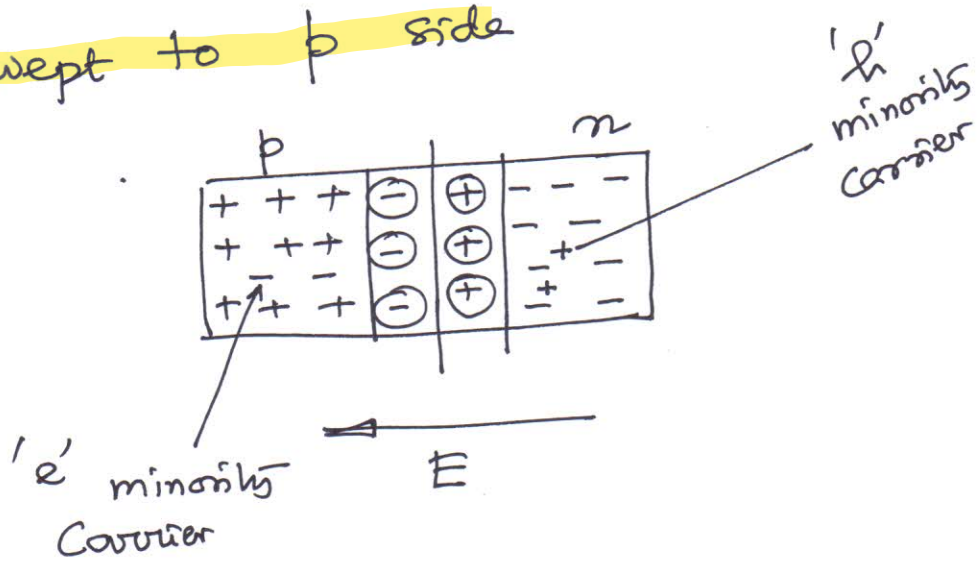
Diffusion ct I_d depends on the voltage drop V_0 across the depletion region.

Drift current (I_s) and Equilibrium

I_D : Diffusion of majority carrier.

Thermally generated minority carriers 'h' in n side and 'e' in p side, move toward the junction.

Electric field in depletion region sweeps them across the region. 'e' in p side is swept to 'n'-side and 'h' in n-side is swept to p side



'e' moved from p to n
'h' moved from n to p

Causes ~~Diffusion~~ Drift current from 'n' to 'p'

I_D (Diffusion ct by majority carrier) →

← I_s (Drift current by minority carrier)

I_S : Drift current from n to p

I_D : Diffusion current from p to n

I_S : Drift current by thermally generated minority carrier, strongly depends on temp

Independent of depletion layer voltage V_0.

Upon open ckt condition $I_D = I_S$

The equilibrium condition is maintained by the barrier voltage V_0.

If $I_D > I_S$ ⇒ more bound charge will be uncovered ⇒ depletion layer widen ⇒ V_0 increases

⇒ I_D to reduce until equilibrium is acheived with $I_D = I_S$

If $I_S > I_D$ ⇒ uncovered charge decreases

⇒ depletion layer will be narrow

⇒ V_0 will reduce ⇒ I_D increases

till $I_D = I_S$ at equilibrium.

Junction built in voltage

no external voltage, barrier voltage V_0 across pn junction can be given as

$$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

A steady-state balance of carriers is achieved at the junction where diffusive flux of the carriers is balanced by the drift flux. The loss of charge neutrality at the junction can be also expressed in terms of the potential, which is referred to as built-in voltage Vbi

N_A : Doping conc of p side

N_D : Doping conc. of n side.

$V_T = \frac{kT}{q}$, V_0 depends on doping conc. and temp.

V_0 : In built in voltage

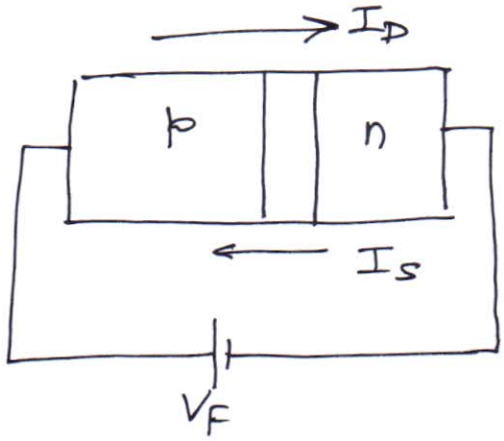
For Si at room temperature, $V_0 \approx 0.6$ to 0.9 V.

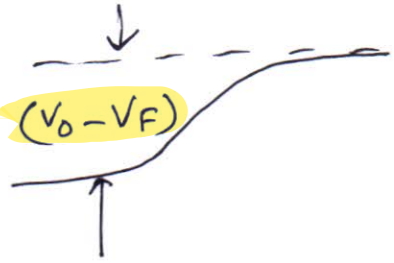
pn jn terminals are left open circuited, voltage measured between the terminals is 0,

Contact voltage existing at metal semiconductor junctions at the terminals counter and exactly balance the barrier voltage.

Otherwise we were able to draw energy from isolated pn junction violating principle of conservation of Energy.

Fwd Bias P–N Jn





Under open ckt case, a barrier voltage V_0 develops making n more positive than p

→ limits the diffusion ct $I_D = I_S$ (drift ct)

V_0 : Barrier voltage establishes the current equilibrium.

Now when a forward bias V_F is applied the barrier voltage is reduced to $(V_0 - V_F)$ across the jn/depletion region.

⇒ reduced depletion region charge

⇒ depletion region width reduces

More holes diffuse from p to n

More electron diffuse from n to p.

I_D increases significantly

I_D much larger than I_S

Net ct $I = I_D - I_S$

So under fwd bias

Net ct $\boxed{I = I_D - I_S}$ and it flows in the forward direction of jn from p to n.

PN jn can conduct a substantial ct in fwd ~~direction~~ bias region and the ct is mostly a diffusion ct whose value is determined by the forward bias voltage V_F.

$$\boxed{I = I_S\left(e^{kV_D/T_k} - 1\right)}$$

This is the expression of diode current when a fwd voltage V_D is applied.

I_S : reverse saturation ct.

$k = 11600/\eta$ with $\eta = 1$ for Ge, $\eta = 2$ for Si for relatively low level of diode ct.

$\eta = 1$ for Ge and Si for higher levels of diode ct.

$T_k = T_c + 273$

Reverse Bias

Externally applied reverse bias voltage V_R is in a direction to add the barrier voltage, and it increases the effective barrier voltage to $(V_0 + V_R)$.

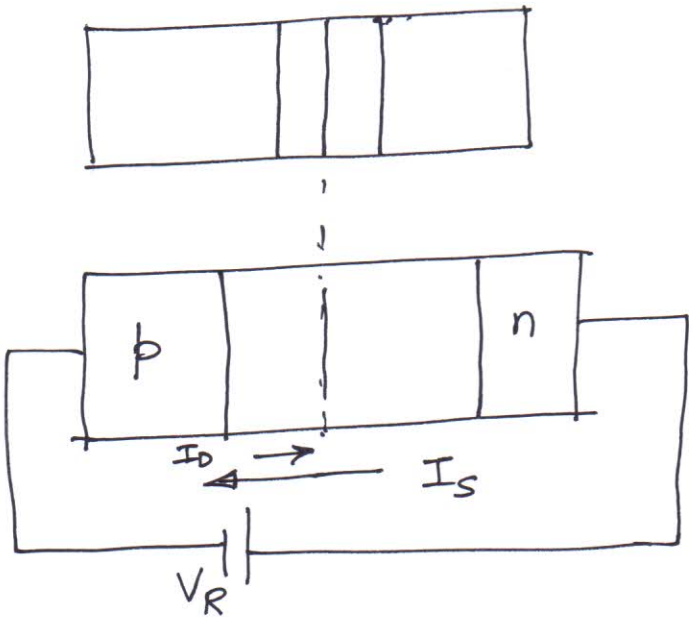
This reduces the no. of holes that diffuse into 'n' region and the number of electrons that diffuse into 'p' region.

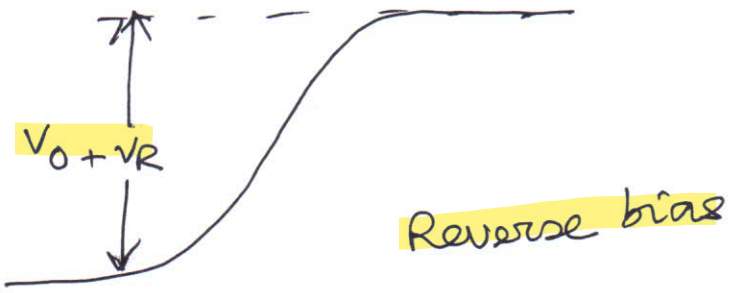
Diffusion ct I_D is dramatically reduced.

Reverse bias voltage of a volt or so is sufficient to cause $I_D \approx 0$.

So current across the jn and through the external ckt will be $= I_S$.

- I_S is the drift ct due to drift of thermally generated minority carriers across the depletion region, I_S is very small and temperature dependent.





- Drift ct is relatively insensitive to height of barrier potential.
- Drift ct is limited not by how fast the carriers are swept down the barrier but rather how often.
- ct is small because there are very few minority electron in p side.

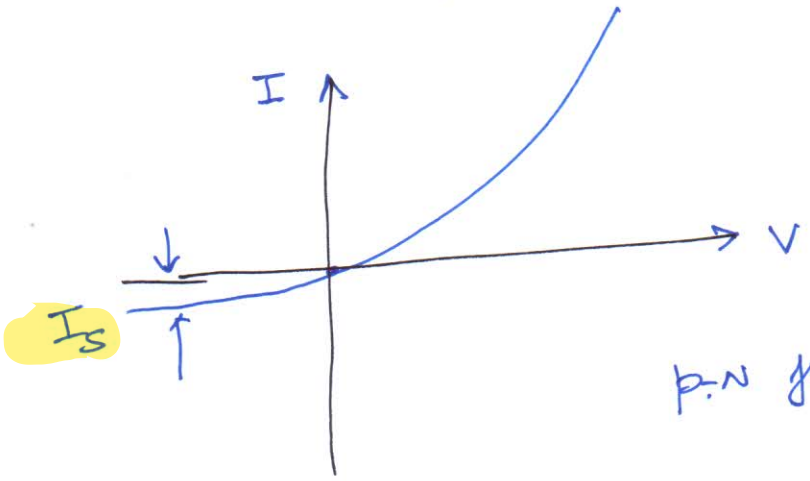
$$I = I_s \left(e^{qV/KT} - 1\right)$$

$$= I_s \left(e^{V/V_T} - 1\right) \qquad V_T = \frac{KT}{q}$$

K: boltzman const

① V is +ve and greater than a few $\frac{KT}{q}$, current increases exponentially

② If V is −ve (rev. bias), exponential term $\rightarrow 0$ $\qquad I = -I_s$



p-N junction I-V characteristics.

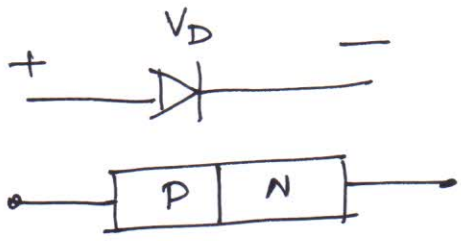
$$\boxed{I = I_s \left(e^{kV_D/T_k} - 1\right)}$$

$k = 11,600/\eta$

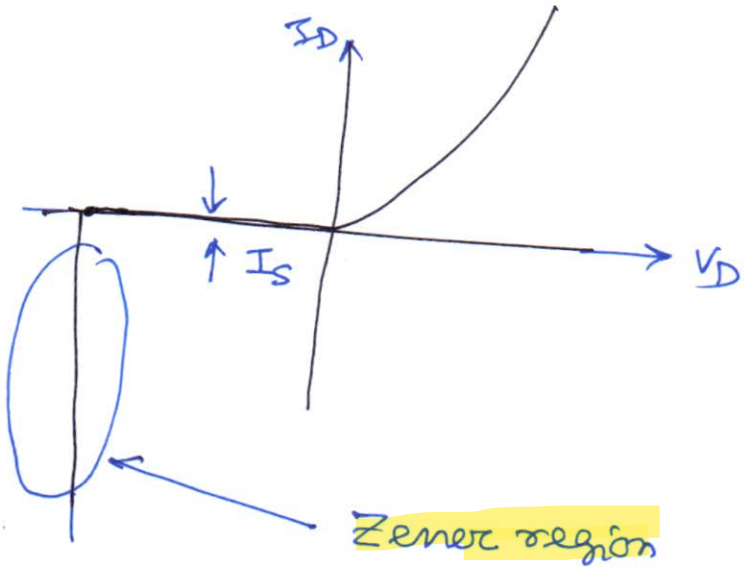
V_D: Diode voltage

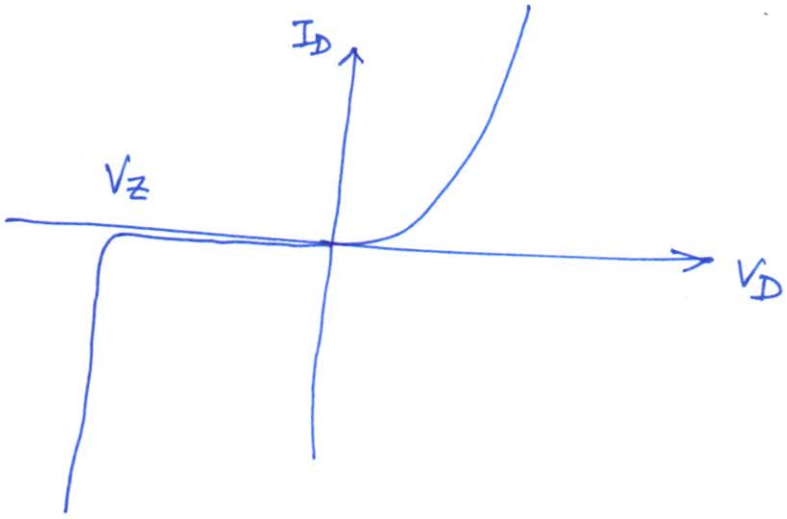
Both eqns. of current are same

$V_T = \frac{KT}{q} = 26$ mV at $T = 300$ K



Zener Region





At a reverse - bias voltage $-V$, with $V \gg V_T$

Reverse ct $\approx I_S$ and it is very small

As rev bias voltage V_D is increased, a value is reached at which a large reverse ct flows.

When the reverse voltage across the jn remains very close to V_Z, we observe a dramatic increase in reverse ct at voltage $V = V_Z$, at which it occurs is called junction breakdown phenomena

Rev break down ct is limited by external ckt.

Breakdown phenomena

1. Zener Effect
2. Avalanche effect.

1. Zener. $V_Z < 5V$

Electric field in depletion Layer increases to point of breaking the covalent bond. Electrons generated will be swept by the Electric field to n side and holes to p side. They constitute a reverse ct. Once zener effect starts a large no. of carriers can be generated, with a negligible increase in junction voltage. Reverse ct can be large (value to be determined by external ckt), while the reverse voltage will remain close to V_Z.

Application : Voltage Regulator

Depletion region Narrow 100 - 200 Å
Electric field intensity is very high 10^6 V/cm.
Below 6V, Zener breakdown voltage decreases with increase in temp, above 6V, it increases with increase in temp.

2. Avalanche Break down

At $V_Z \approx 7V$

As rev. voltage is increased, the velocity of minority carrier increases $\longrightarrow$ kinetic energy increases $\longrightarrow$ release additional carriers through collisions with otherwise stable atoms.

Ionization process : valance electrons absorb sufficient energy to leave parent atom.

These additional carriers can aid the ionization process to the point where a high avalanche current is established and the avalanche breakdown region is reached.

The avalanche region can be brought closer to vertical axis by increasing the doping levels in p and n materials

But at low V_Z such as $-5V$, Zener breakdown occurs.

The maximum reverse bias potential that can be applied before entering the zener region is called peak inverse voltage (PIV) or peak reverse voltage (PRV)

Note:
For junctions that breakdown between 5V and 7V, the breakdown mechanism may be either <u>Zener</u> or <u>Avalanche</u> effect or a combination of the two.

Avalanche effect

$$M = \frac{1}{1 - (V/V_B)^n}$$

M: Avalanche multiplication factor
V: Applied reverse bias
V_B: Breakdown voltage

as $V \longrightarrow V_B$ M increases rapidly.
rev. ct $I_R = M I_0$
Break down voltage depends on doping.
r high doping $V_B = 5V$ for 10^{17} impurity atom/cc
& over 1000V for 10^{14} impurity atom/cc