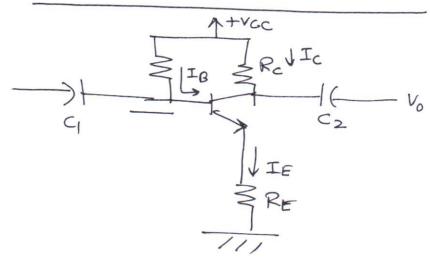
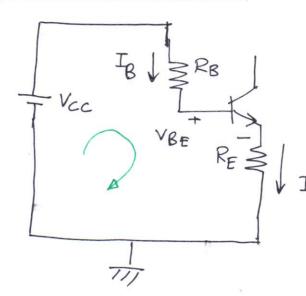
Emiller Stabilized Bias Cht



BJT Bias ckt with Emitter resider

Base Emiller Loop

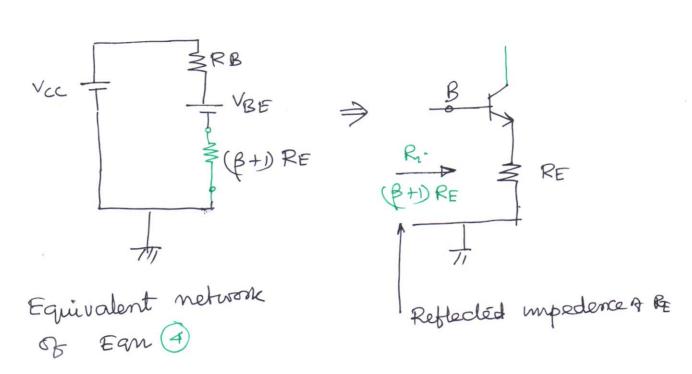


Substitule IE = (BH)IB

IB = $\frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ This term is new hore.

Note: The Difference w. r.t. Fixed bias is the inclusion of term (B+1) RE.

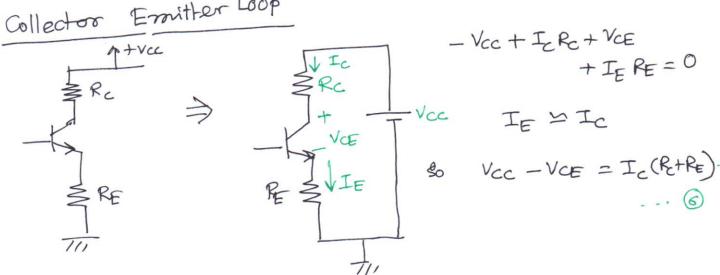
$$\frac{T_{B}}{R_{B}} = \frac{V_{CC} - V_{BE}}{R_{B} + (\beta +)R_{E}}$$



The smiller resistance RE which is part of the Collector emillion Loop appears as (B+1) RE in the base emiller loop.

$$R' = (\beta + 1) R_E - - . \qquad (5)$$

Collector Emitter Loop



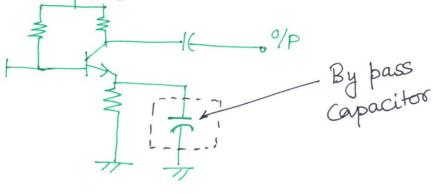
$$V_{CE} = V_{CC} - I_{C}(R_{C} + R_{E})$$
 $V_{E} = I_{E}R_{C} = T_{C}R_{C}$

Voltage at the base w.r. t ground

The d.c. renistance RE emproves the stability But it & reduces the voltage gain for small a.c. Signal.

Thus the resistance RE is desired for d.c. bias to improve stability) but not desired for AC.

implification. Hence it is bypassed by a Capacitor



$$\approx \frac{V_{CC}}{R_B + \beta R_E}$$

$$or 0 = \frac{dIB}{dI}(RB+RE) + RE$$

$$= \beta \frac{dIB}{dI_c} + \frac{(\beta+1)}{S}$$

$$= \frac{(\beta+1)}{1-\beta \frac{dIB}{dI_c}} = \frac{(\beta+1)}{1+\beta \frac{RE}{RB+RE}}$$

$$S(I_{co}) = \frac{(\beta+1)}{1+\beta \cdot \frac{RE}{(RB+RE)}}$$

$$= (\beta + 1) \left[\frac{1 + \frac{RB}{RE}}{(1+\beta). + \frac{RB}{RE}} \right]$$

$$\frac{RB}{RE} \gg (\beta + 1)$$

$$S(I_{co}) = (\beta + 1)$$

Same as fixed bias

SCIO)
$$S = \frac{RB}{RE} \qquad (1 < RB/RE < \beta + 1)$$

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$$S(V_{BE}) = \frac{\partial I_c}{\partial V_{BE}}$$

$$= \frac{\beta/RE}{\frac{RB}{RE} + (\beta+1)}$$

$$(\beta+1)\gg \frac{RB}{RE} = -\frac{\beta/RE}{(\beta+1)} \cong -\frac{\beta}{RE}$$

Larger RE' vill ensure higher stability.

Voltage Divider Bias

- In the previous configurations, the bias ct Ica and voltage VCEQ were a function of Current gain (β). of the transistor.
 - · However, since β is temperature sensitive,

 barticularly for Si transistors and actual

 value of β is not usually well defined,

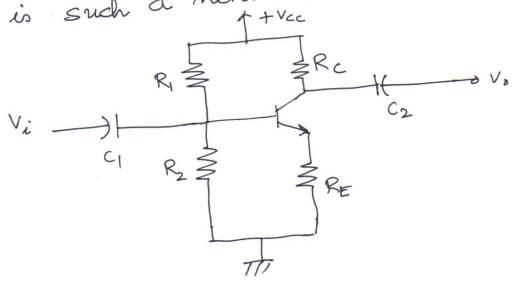
 it would be desirable to develop a bias

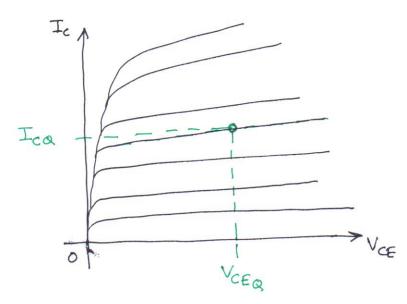
 it would be desirable to infact, independent

 Ckt that is less dependent, or infact, independent

 of transistor. β.

The voltage-divider bias config of Fig below is such a network.

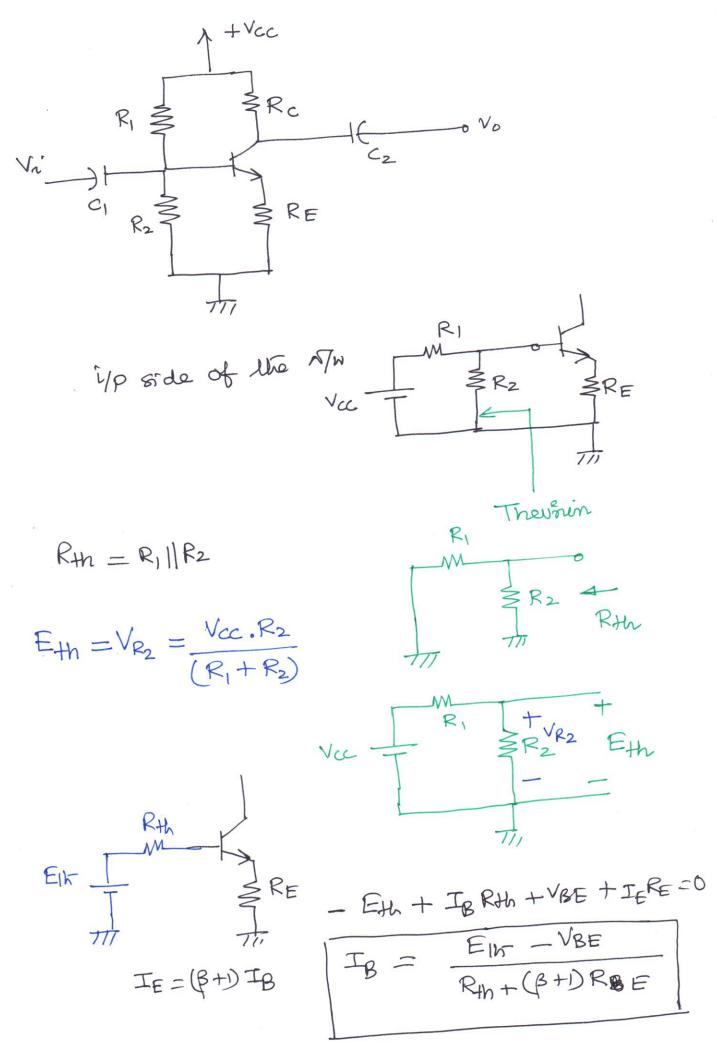




Sensitivity to changes in B is small

By proper choice of circuit parameters, resulting level of Ica and VCEa can be made totally undependent of β .

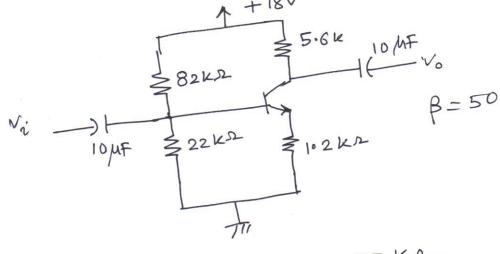
The level of IBQ will change with change in B, but the operating point on the characteristics defined by Ica and VCEQ can remain fixed.



Once IB is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias config.

or
$$I_c = \frac{V_{cc} - V_{cE}}{R_c + R_E}$$

Example



$$R+h = R_1 ||R_2| = 82 ||22| = 17-35 KL$$

$$E_{1K} = \frac{18 \times 2^{2}}{82 + 22} = 3.81 \text{ V}$$

$$IB = \frac{E_{IK} - V_{BE}}{R_{IM} + R_{E}(I+B)} = \frac{3.81 - 0.7}{17.35 + 1.2 \times 51} = 39.6 \mu A$$

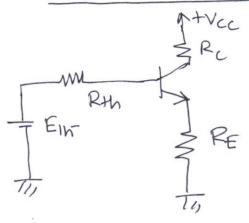
$$I_{CQ} = \beta I_{B} = 50 \times 39.6 \mu A = 1.98 mA$$

$$V_{CEQ} = V_{CC} - I_{C}(P_{C} + P_{E})$$

$$= 18 - 1.98(5.6 + 1.2) = 4.54V$$

Voltage Divider Bias

Equivalent ckt.



Following the some approach of Emitter Stabilized Bias ckt, we obtain

$$S(I_{co}) = (\beta+1) \frac{(1+R+n/R_E)}{(\beta+1)+R+n/R_E}$$

Now for Emilla stabilized Bias, we have greatest Stability when $\frac{RB}{RE} < 1$ or $\frac{RE}{RE} > RB$ $S \approx 1$ Similarly here $S \approx 1$ when $\frac{RE}{RE} > \frac{R}{RE}$

For voltage divider bias, Rth can be much less than the corresponding RB of the emiller-bias Configuration, and Still have an effective design.

$$I_{B} = \frac{E_{IN} - V_{BE}}{R_{IN} + (\beta + D)R_{E}}$$

$$= \beta \left(-\frac{1}{R1K + (\beta+1)RE} \right)$$

$$= \frac{\beta/RE}{Rir} + (\beta+1)$$

$$RE$$

$$\frac{RIh}{RE} \angle (\beta + 1) = \frac{-\beta/RE}{(\beta + 1)}$$

$$\frac{\beta/RE}{RE}$$

$$PE$$
 PRE
 PRE

Larger the resistance RE, Lower the stability factor, and more stable the system.