MODULE - 3 : BIPOLAR JUNCTION TRANSISTOR (BJT)

PART-B

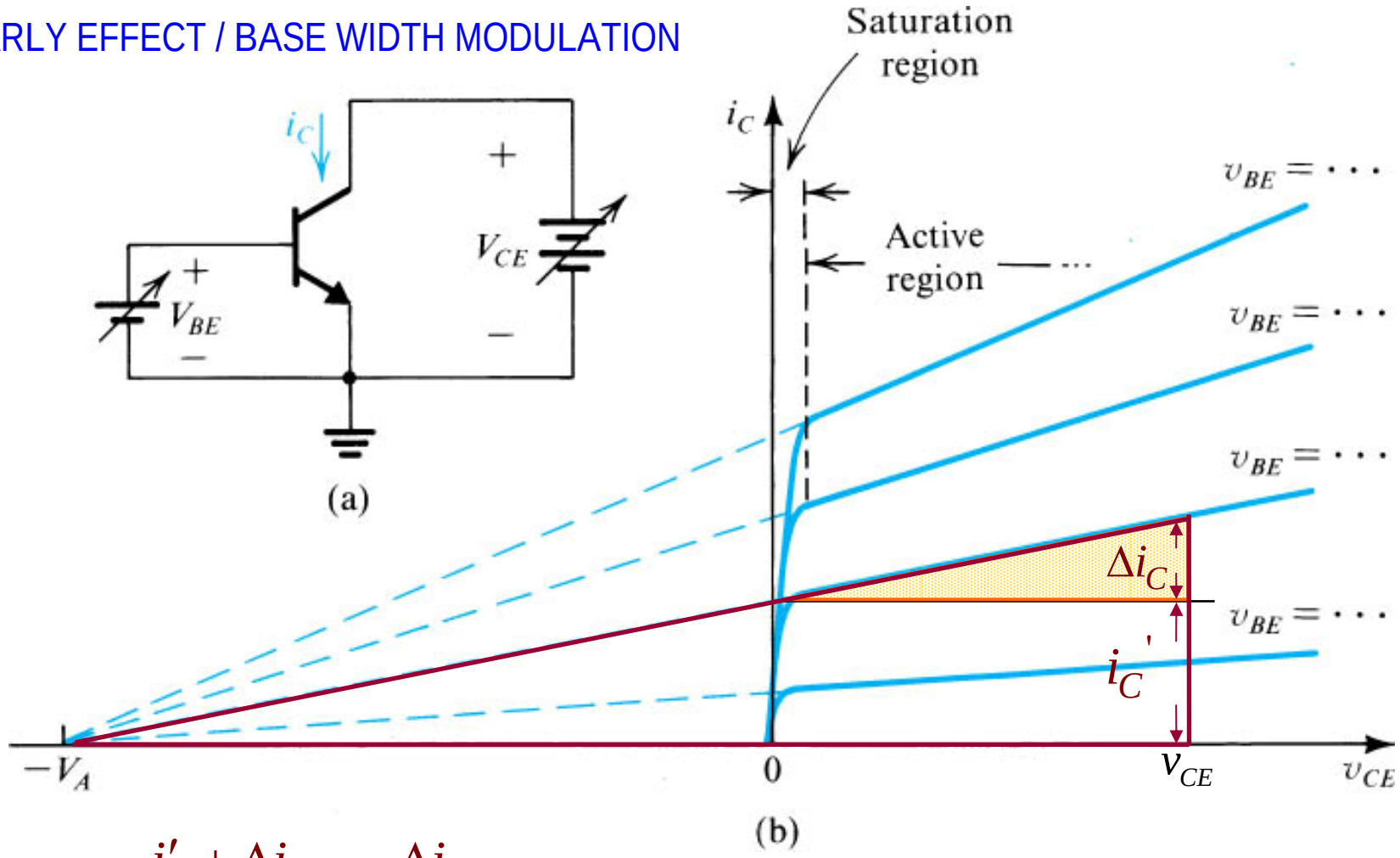
MODULE 3: Bipolar Junction Transistor (5 L + 2 T)

3.1 Transistor configuration: common base, common emitter, and common collector
3.2 Transistor characteristics: input and output characteristics of CB and CE configurations
3.3 DC load line: quiescent (Q) point; cut-off, active, and saturation region
3.4 Amplifier: Principle of operation
3.5 Transistor as a switch
3.6 Transistor biasing
- 3.6.1 Need of biasing
- 3.6.2 Methods of biasing: base resistor or fixed bias, emitter feedback bias, and voltage divider bias
- 3.6.3 Stability of Q-point (qualitative discussions)
- 3.6.4 Numerical problems on biasing

Sedra/Smith
Microelectronic Circuits

Chapter 4-A
Bipolar Junction Transistors (BJTs)

EARLY EFFECT / BASE WIDTH MODULATION

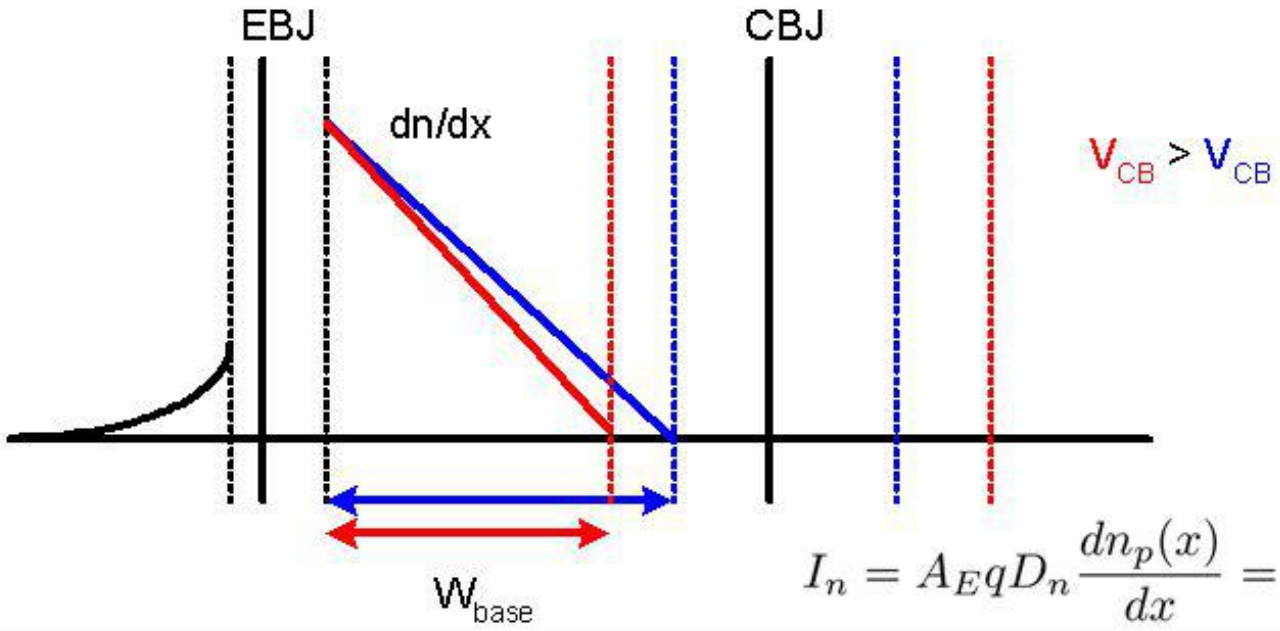


$$\frac{i_C' + \Delta i_C}{V_A + v_{CE}} = \frac{\Delta i_C}{v_{CE}}$$

$$i_C' v_{CE} + \cancel{\Delta i_C v_{CE}} = \Delta i_C V_A + \cancel{\Delta i_C v_{CE}} \Rightarrow \Delta i_C = \frac{v_{CE}}{V_A} i_C'$$

Early Effect

- What causes the Early Effect?
  - Increasing V_{CB} causes depletion region of CBJ to grow and so the effective base width decreases (base-width modulation)
  - Shorter effective base width → higher dn/dx



$$I_n = A_E q D_n \frac{dn_p(x)}{dx} = A_E q D_n \left(-\frac{n_p(0)}{W} \right)$$

The collector current (operation in the active mode)

neglected the Early effect: $i_C' = I_S e^{v_{BE}/V_T}$

including the Early effect: $i_C = i_C' + \Delta i_C = i_C' + i_C' \frac{v_{CE}}{V_A}$

$$= I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$$

The nonzero slopeof the $i_C - v_{CE}$ straight line indicates that the output resistance looking into the collector is not infinite. Rather, it is finite and defined by

$$r_o \equiv \left[\left.\frac{\partial i_C}{\partial v_{CE}}\right|_{v_{BE}=\text{constant}}\right]^{-1} = \frac{V_A + V_{CE}}{I_C} = \frac{V_A}{I_C'}$$

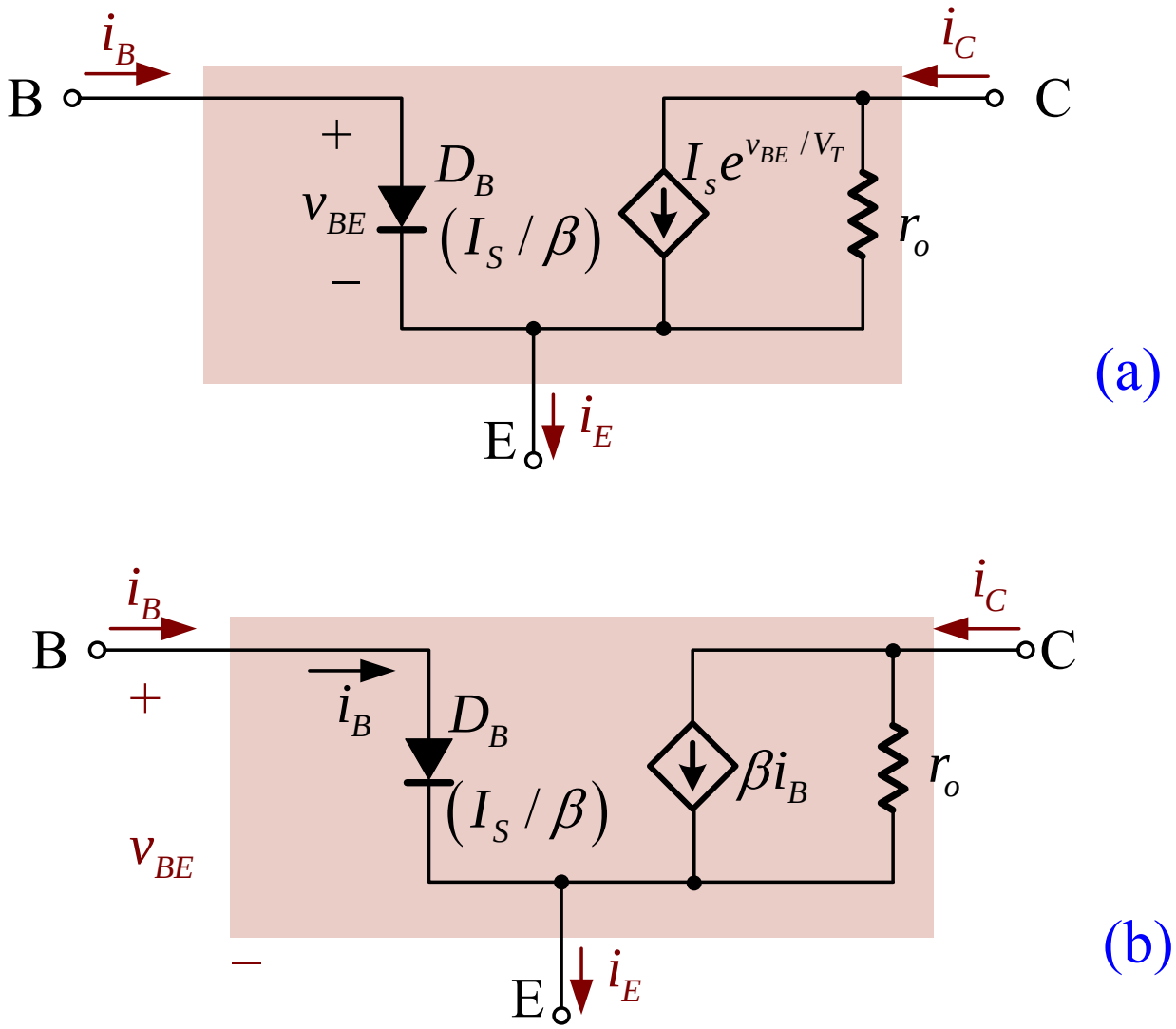


Figure 4.18 Large-signal equivalent-circuit models of an *npn* BJT operating in the active mode in the common-emitter configuration. Those in Fig.5.5(c) and (d), P.13, with the resistance ro connected between the C and E terminals

BJT Circuits at DC

- Simple BJT model at DC
  - $|V_{BE}|$ of a conducting transistor = 0.7 V
  - $|V_{CE}|$ of a saturated transistor = 0.2 V
  - No Early effect
- Accurate results by SPICE simulation
- Quick pencil-and-paper circuit analysis

  1) In which mode is transistor operating ?

  2) Assume the transistor is operating in the active mode

  3) check for consistency

     - v_{CB} of *npn* transistor > -0.4 V
     - v_{CB} of *pnp* transistor < 0.4 V

     →If yes, the task is complete

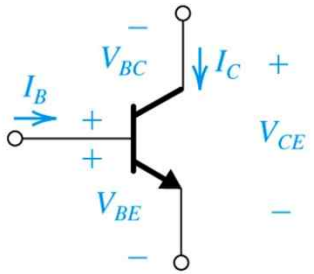
  4) If no, assume saturation-mode operation

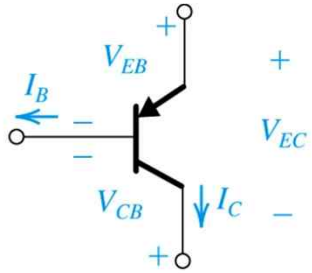
  5) check for *consistency*

     - $\beta_{forced} = I_C/I_B <$ the lowest specified β of the transistor

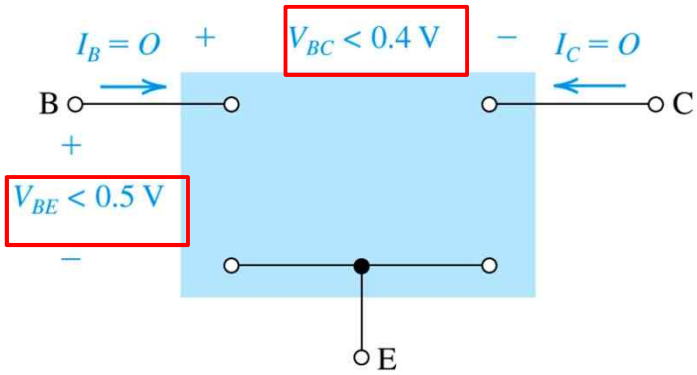
BJT Circuits at DC

npn *pnp*





Cutoff
EBJ : Reverse biased
CBJ : Reverse biased



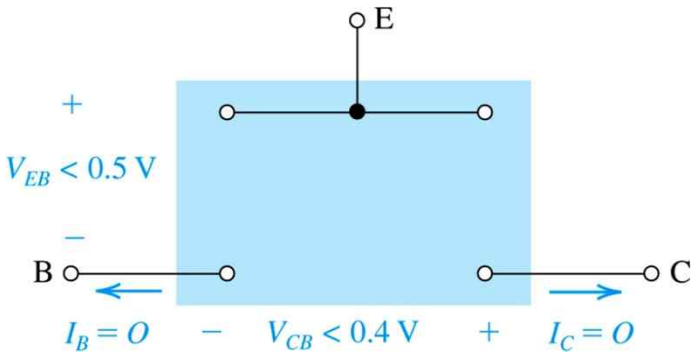
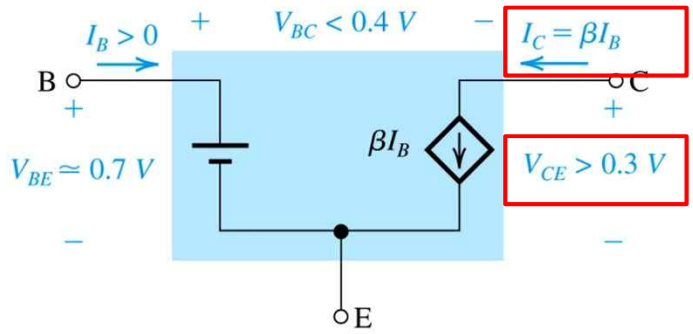
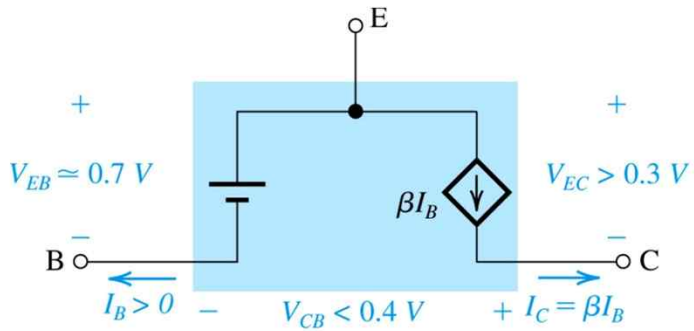


Table 6.3 Conditions and Models for the Operation of the BJT in Various Modes *(continued)*

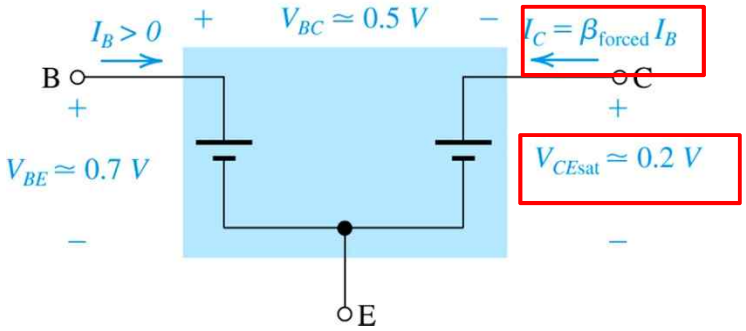
BJT Circuits at DC

Active
EBJ : Forward biased
CBJ : Reverse biased





Saturation
EBJ : Forward biased
CBJ : Forward biased



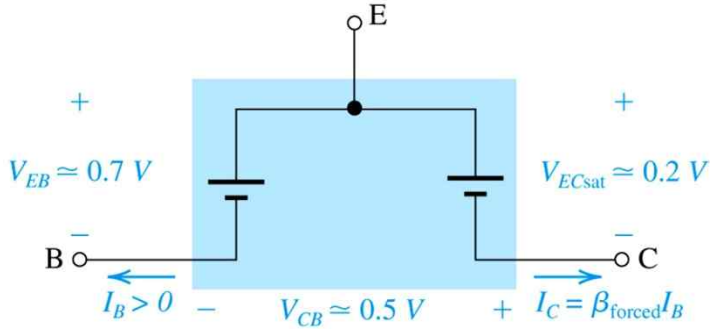
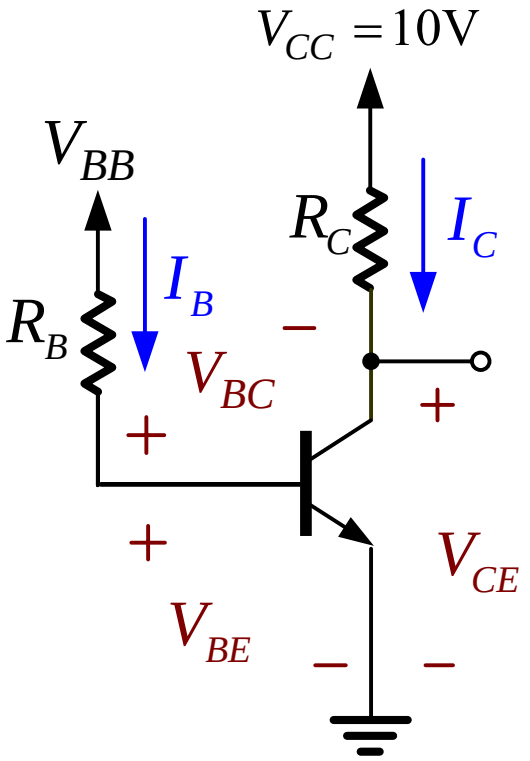


Table 6.3 Conditions and Models for the Operation of the BJT in Various Modes *(continued)*

Example 4.3 For the circuit in Fig.4.21 has $R_B = 10\text{k}\Omega$ and $R_C = 1\text{k}\Omega$, it is required to determine the value of the voltage V_{BB} that results the transistor operating (a) in the active mode with $V_{CE} = 5\text{V}$, (b) at the edge of saturation, (c) deep in saturation with $\beta_{\text{forced}} = 10$

For simplicity, assume that $V_{BE} = 0.7\text{V}$. The transistor $\beta = 50$



Solution:

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{(10-5)\text{V}}{1\text{k}\Omega} = 5\text{mA}$$

$$I_B = I_C / \beta = 5\text{mA} / 50 = 0.1\text{mA}$$

$$V_{BB} = I_B R_B + V_{BE}$$

$$= 0.1 \times 10 + 0.7 = 1.7\text{V}$$

$$(b)\ I_C = \frac{V_{CC} - V_{CE_{sat}}}{R_C} = \frac{(10 - 0.3)\text{V}}{1\text{k}\Omega} = 9.7\text{mA}$$

$$I_B = I_C / \beta = 9.7\text{mA} / 50 = 0.194\text{mA}$$

$$V_{BB} = I_B R_B + V_{BE} = 0.194 \times 10 + 0.7 = 2.64\text{V}$$

$$(c)\ V_{CE} = V_{CE_{sat}} \approx 0.2\text{V}$$

$$I_C = \frac{V_{CC} - V_{CE_{sat}}}{R_C} = \frac{(10 - 0.2)\text{V}}{1\text{k}\Omega} = 9.8\text{mA}$$

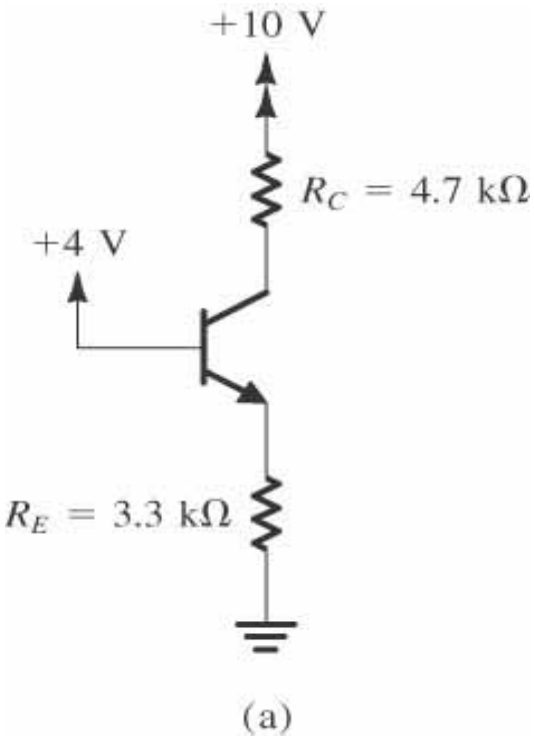
$$I_B = \frac{I_C}{\beta_{forced}} = \frac{9.8\text{mA}}{10} = 0.98\text{mA}$$

the requred V_{BB} can now be found as

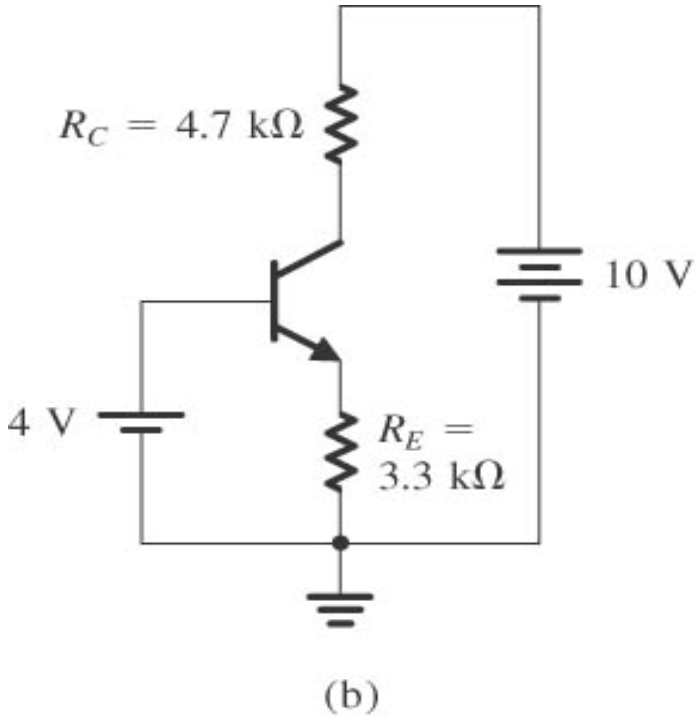
$$V_{BB} = I_B R_B + V_{BE} = 0.98 \times 10 + 0.7 = 10.5\text{V}$$

4.3 BJT circuits at DC

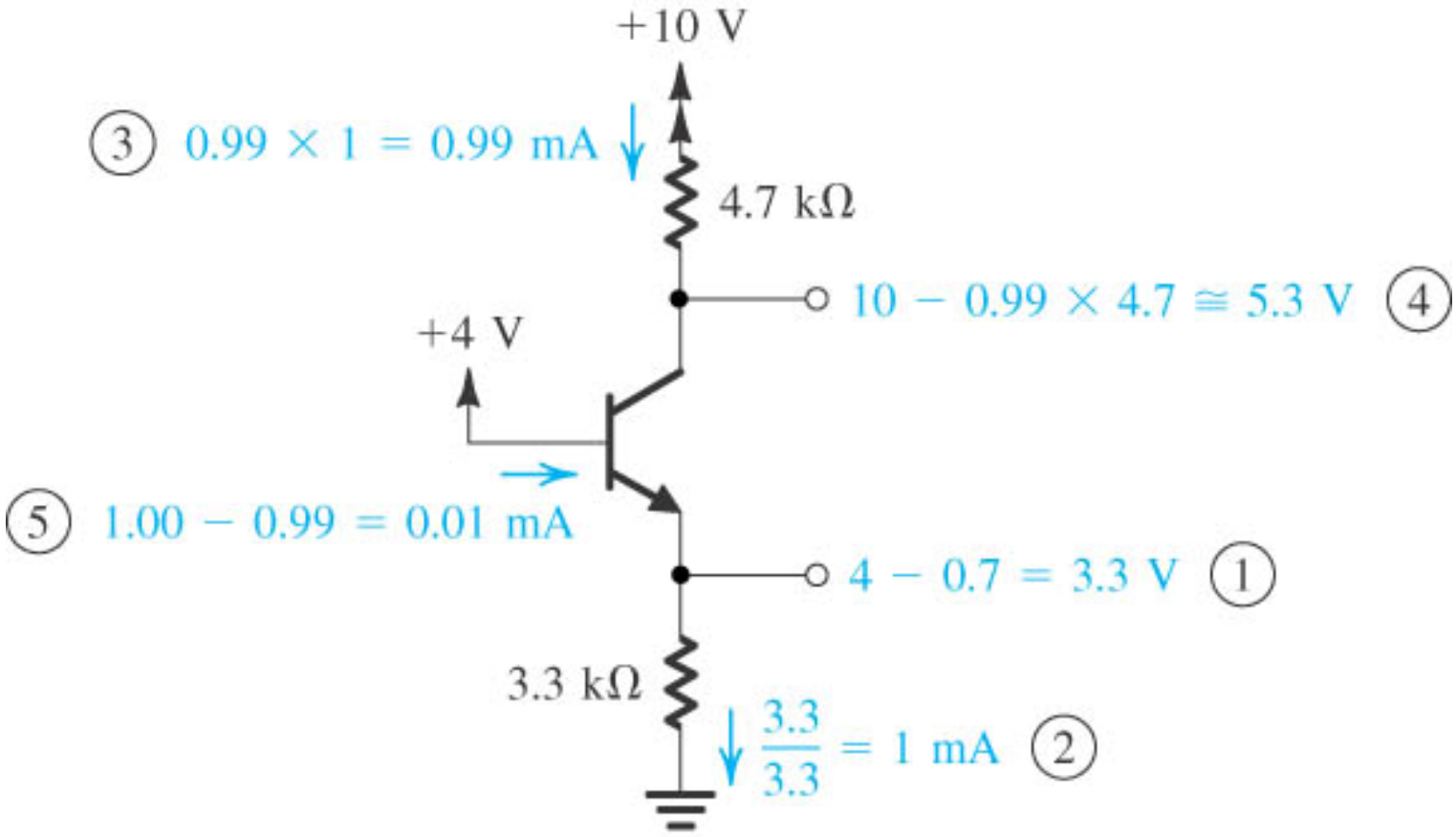
Example 4.4 Consider the circuit shown in below Fig. We wish to analyze this circuit to determine all node voltages and branch currents. We will assume that β is specified to be 100



(a)

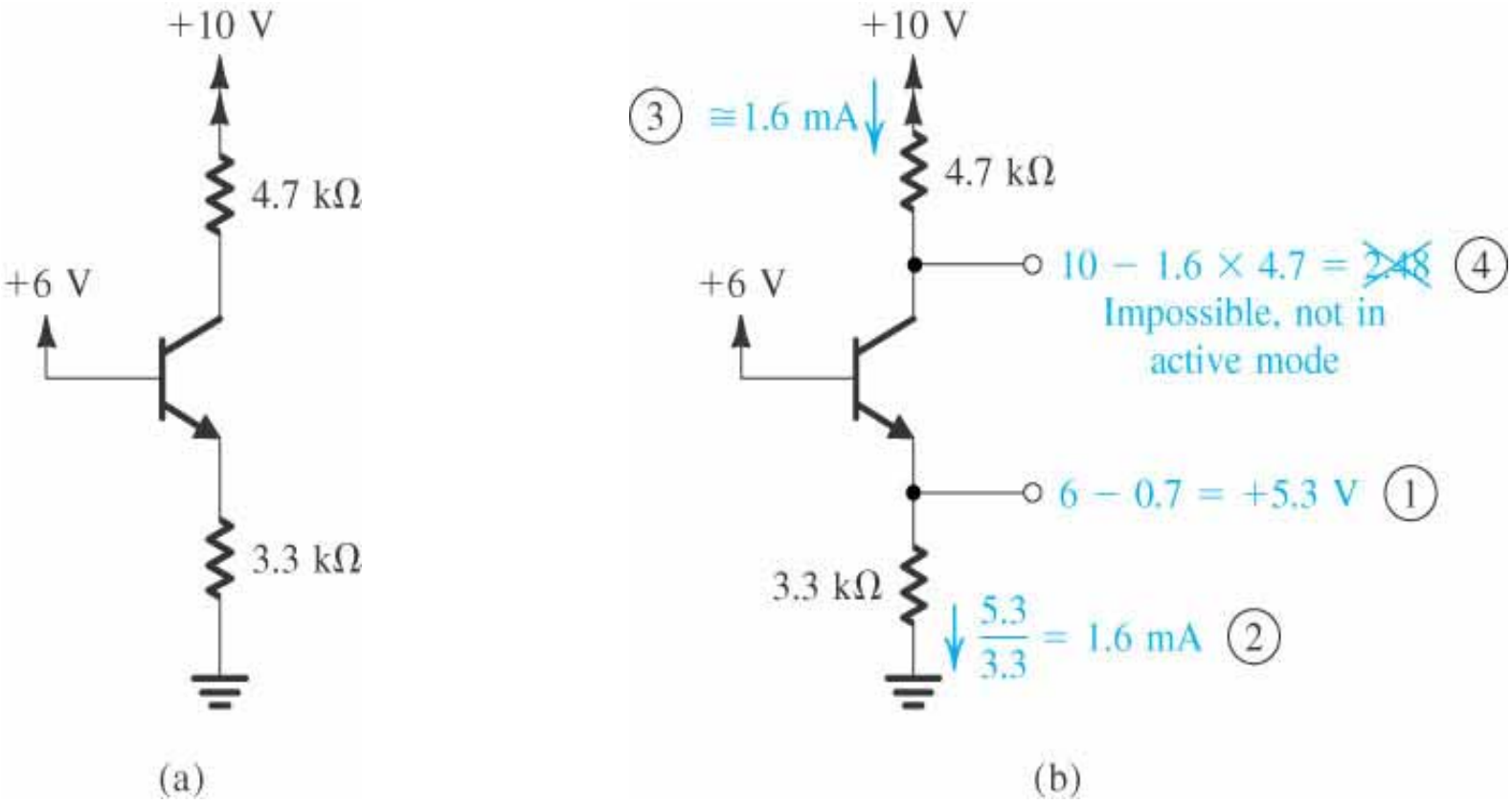


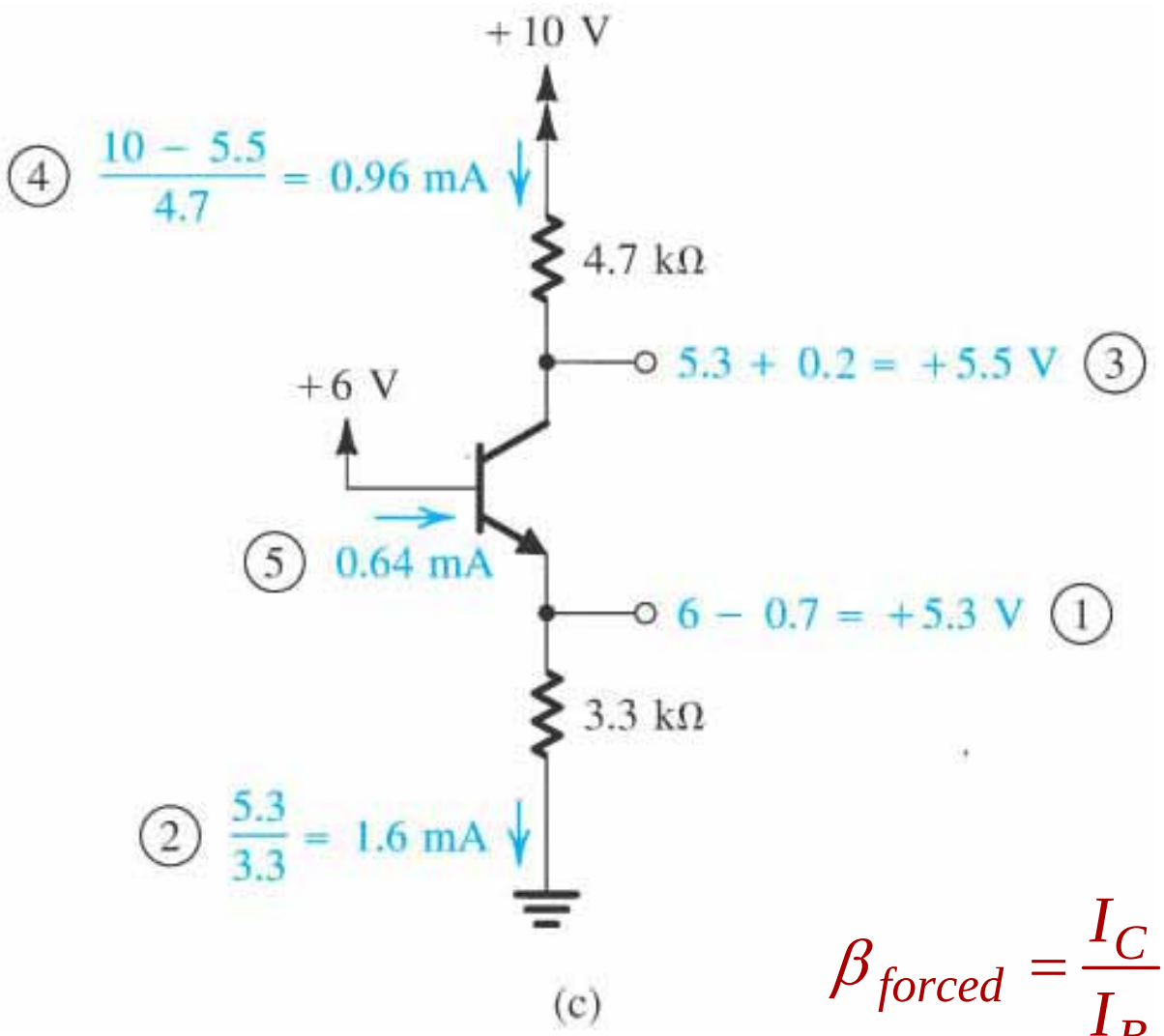
(b)


+10 V
③ 0.99 × 1 = 0.99 mA
4.7 kΩ
10 − 0.99 × 4.7 ≅ 5.3 V ④
+4 V
⑤ 1.00 − 0.99 = 0.01 mA
4 − 0.7 = 3.3 V ①
3.3 kΩ
3.3/3.3 = 1 mA ②

(c)

Example 4.5 We wish to analyze this circuit below Fig. to determine all node voltages and branch currents.We will assume that β is specified to be at least 50.

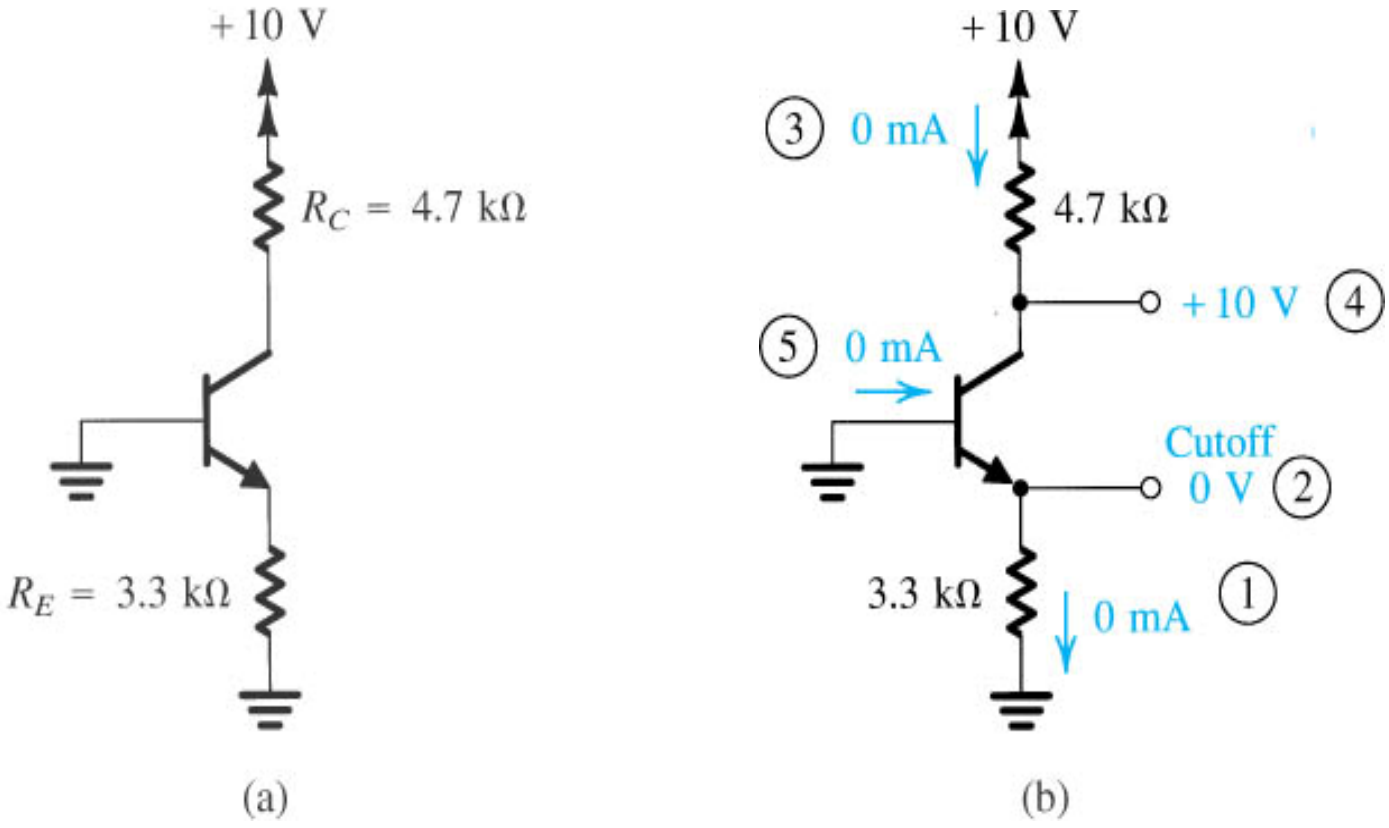




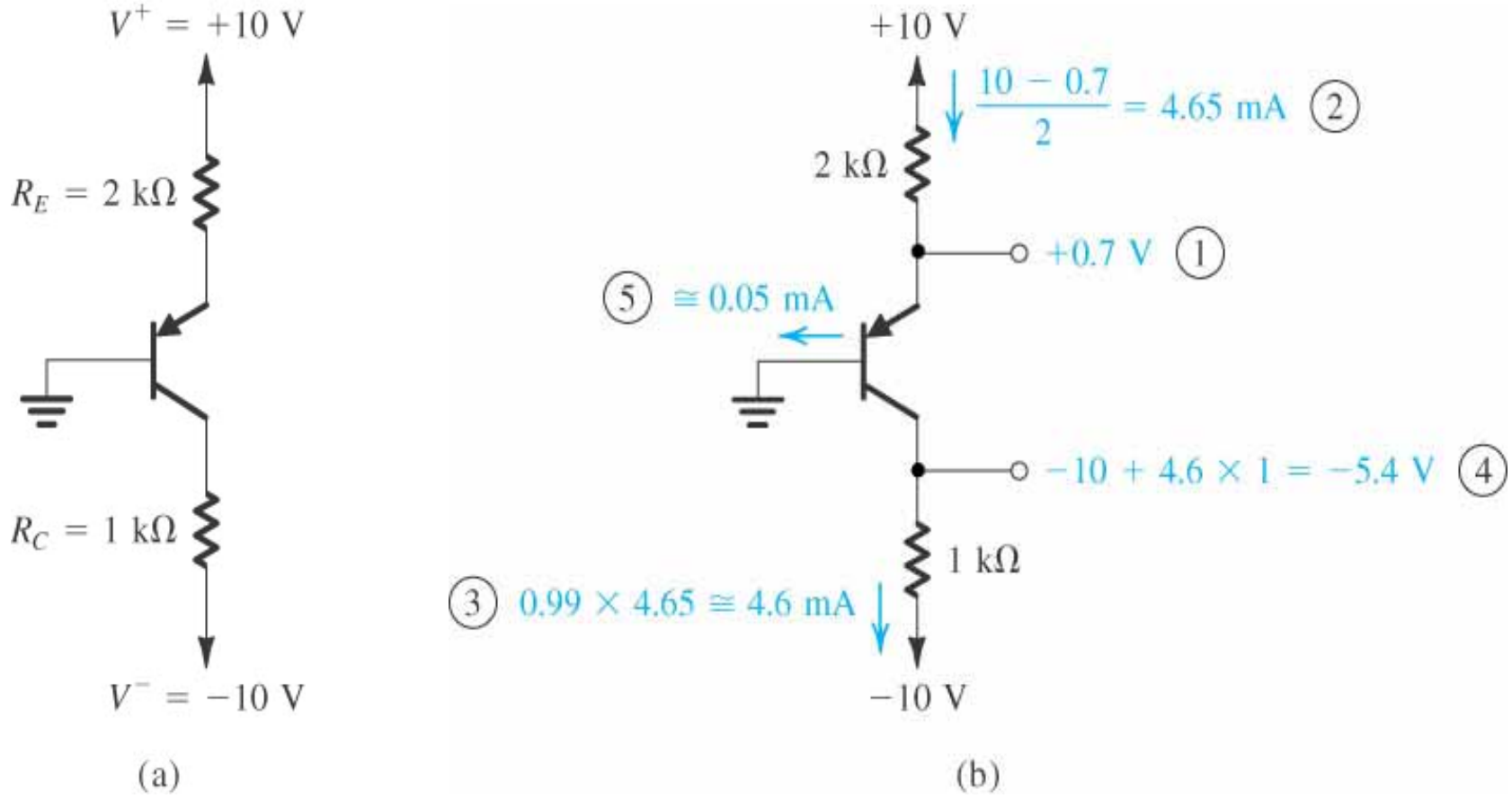
(c)

$$\beta_{forced} = \frac{I_C}{I_B} = \frac{0.96}{0.64} = 1.5$$

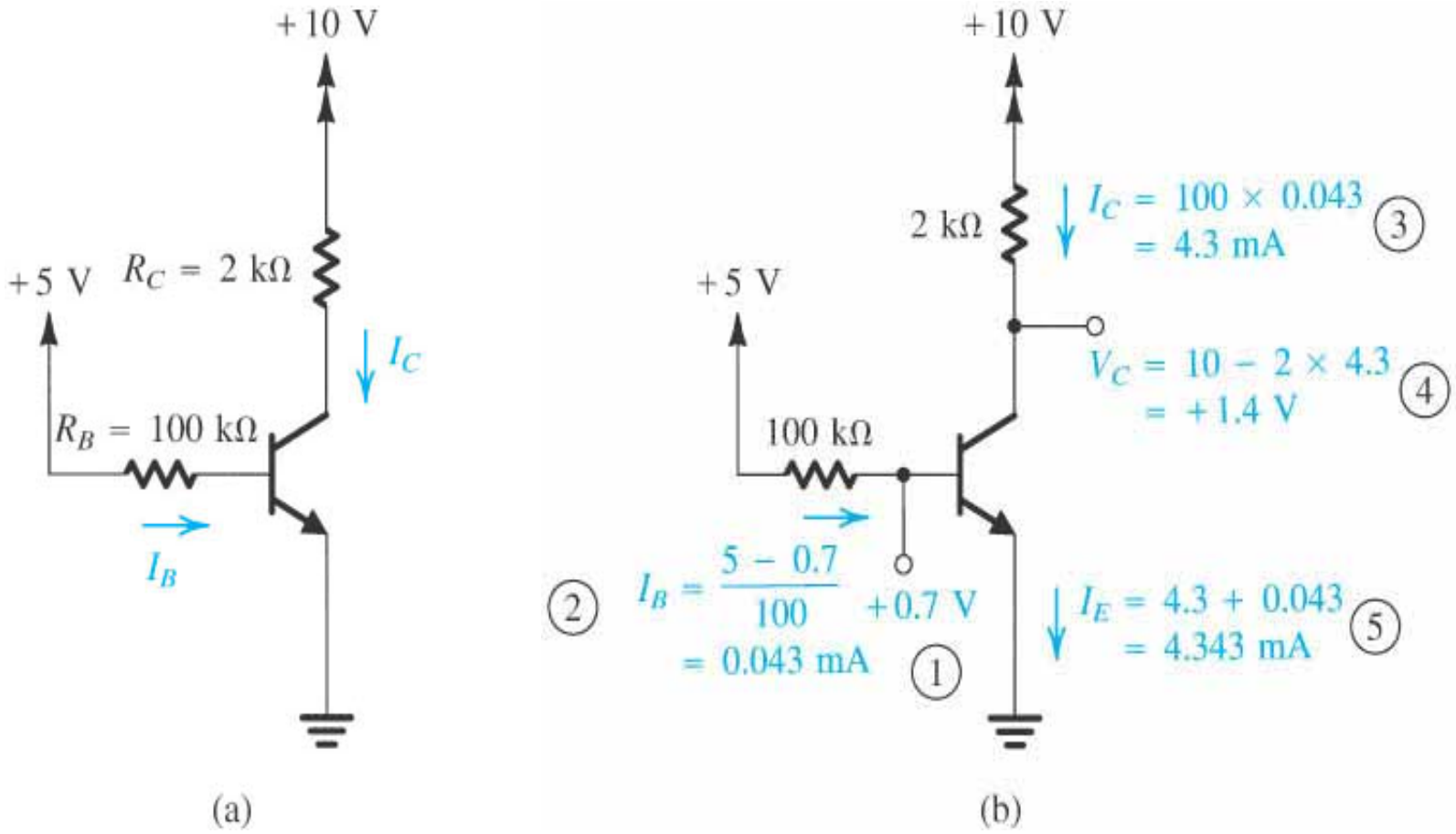
Example 4.6 We wish to analyze this circuit below Fig., to determine all node voltages and branch currents.



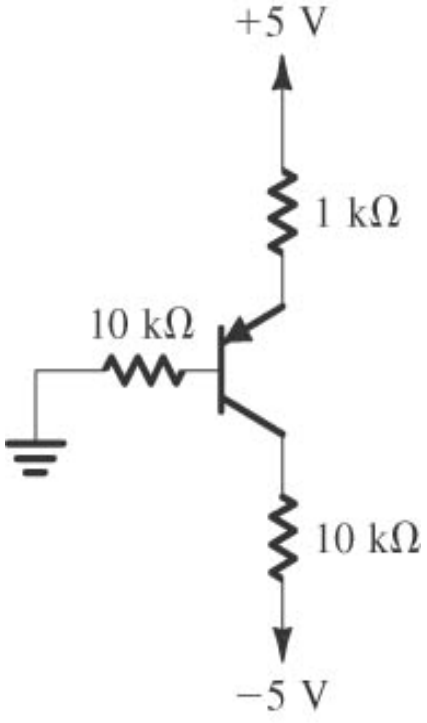
Example 4.7 We desire to analyze this circuit below Fig., to determine the voltages at all nodes and the currents though all branchs .Assume $\beta = 100$



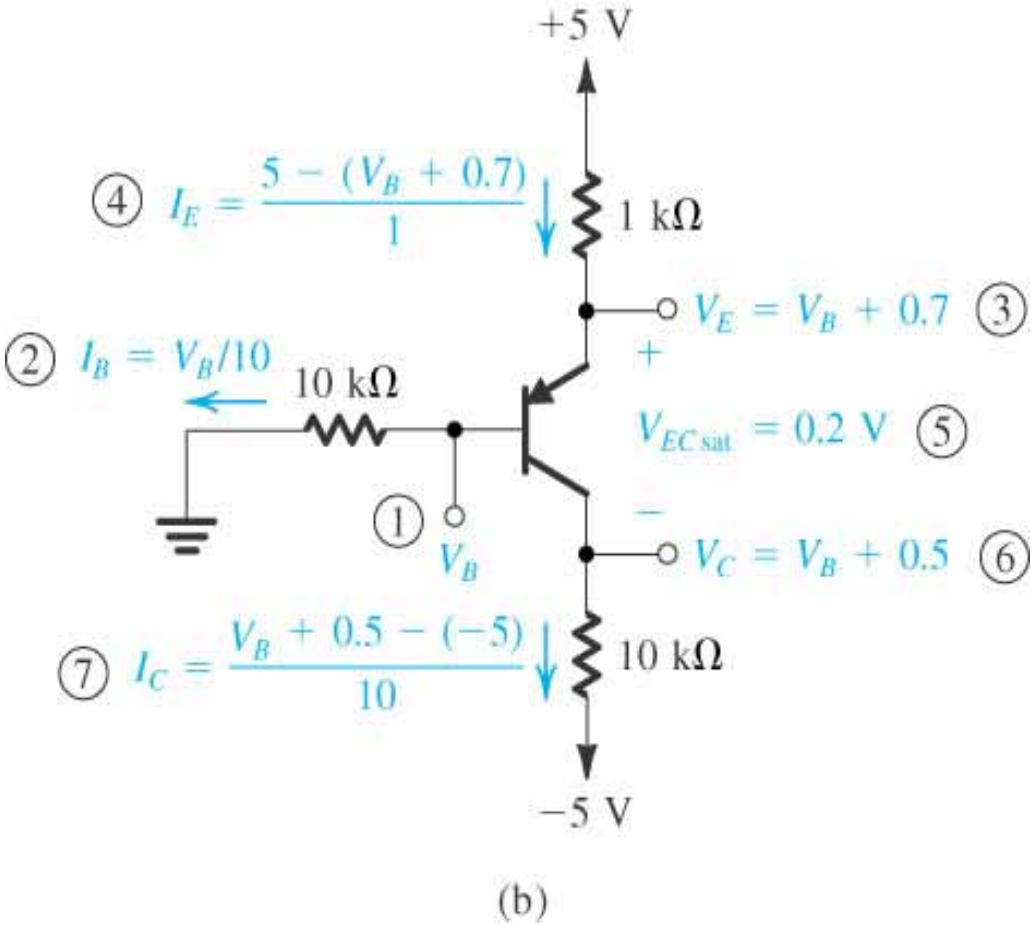
Example 4.8 We want to analyze the circuit in below Fig., to determine the voltages at all nodes and the currents in all branchs .Assume $\beta = 100$



Example 4.9 We want to analyze the circuit in below Fig., to determine the voltages at all nodes and the currents in all branchs .The minimum value of β is specified to be 30.

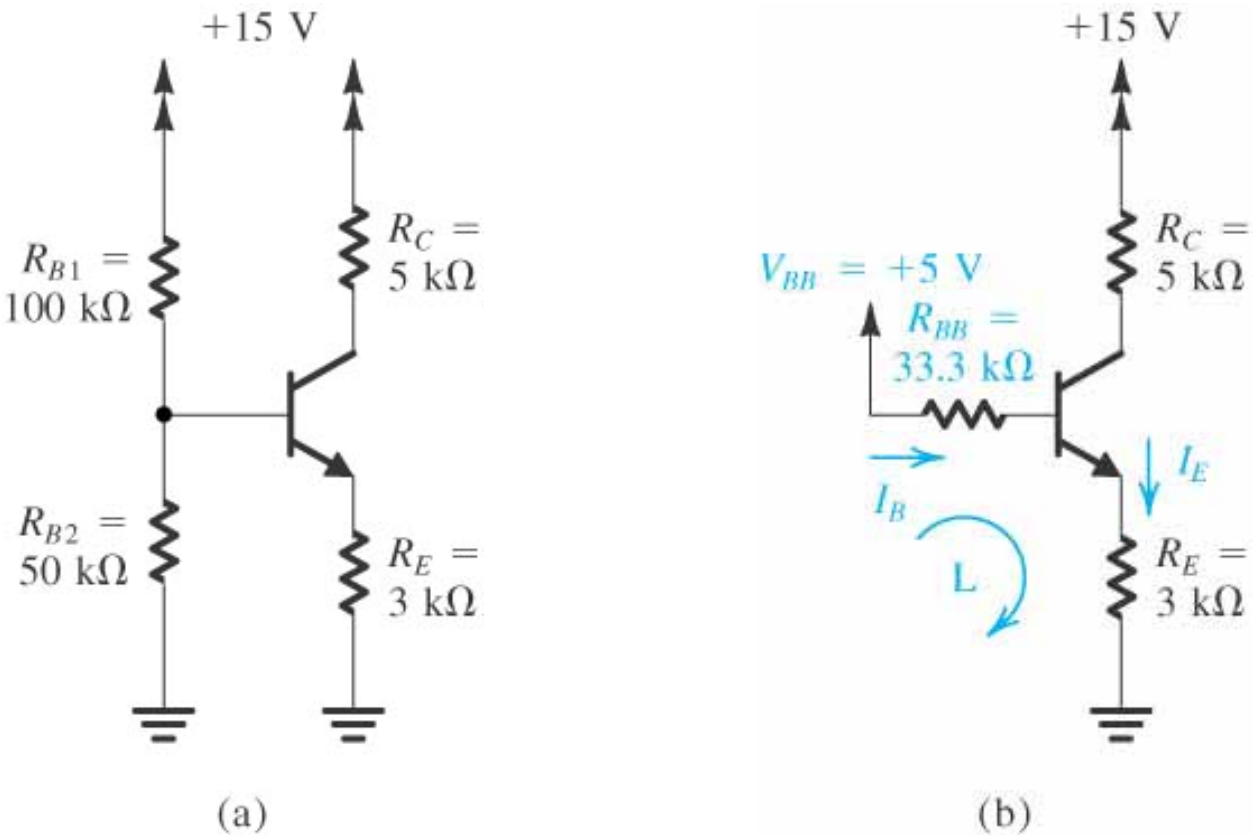


(a)

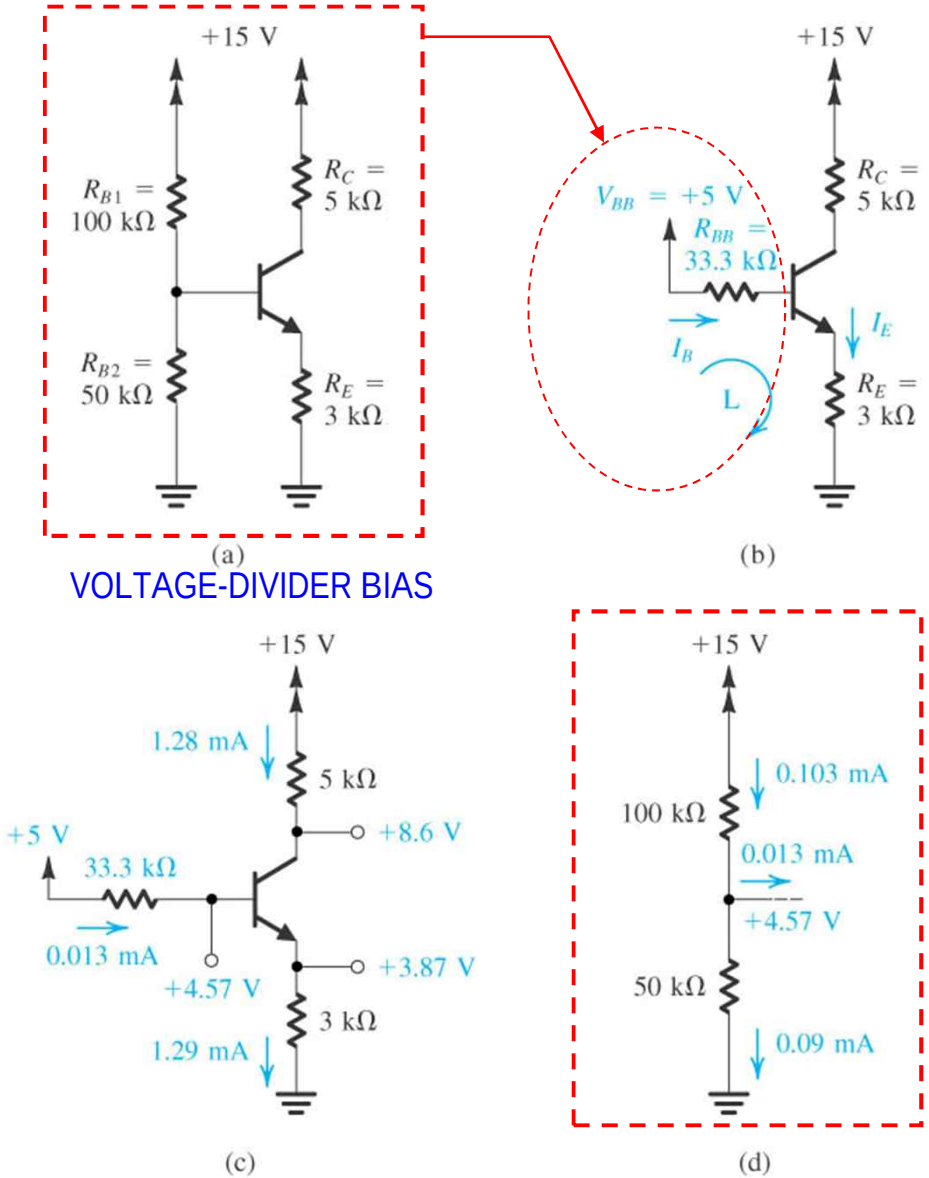


(b)

Example 4.10 We want to analyze the circuit in below Fig., to determine the voltages at all nodes and the currents though all branchs . Assume $\beta = 100$



Analysis of BJT Biasing Circuits at DC



VOLTAGE-DIVIDER BIAS

Ex. 4.10 $\beta = 100$

By Thevenin's theorem

$$V_{BB} = +15\frac{R_{B2}}{R_{B1}+R_{B2}} = +5\ V$$

$$R_{BB} = (R_{B1} \,//\, R_{B2}) = 33.3\ k\Omega$$

by loop equation around the loop L

$$V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E$$

$$Substituting\ I_B = \frac{I_E}{\beta+1}$$

$$\rightarrow I_E = \frac{V_{BB}-V_{BE}}{R_E + [R_{BB}/(\beta+1)]} = 1.29\ mA$$

$$I_B = 0.0128\ mA \approx 0.013\ mA$$

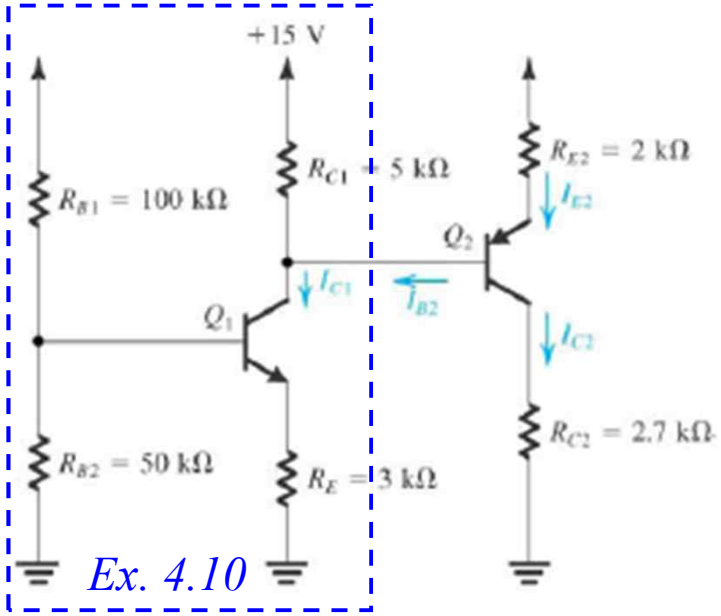
$$I_C = \alpha I_E = 1.28mA$$

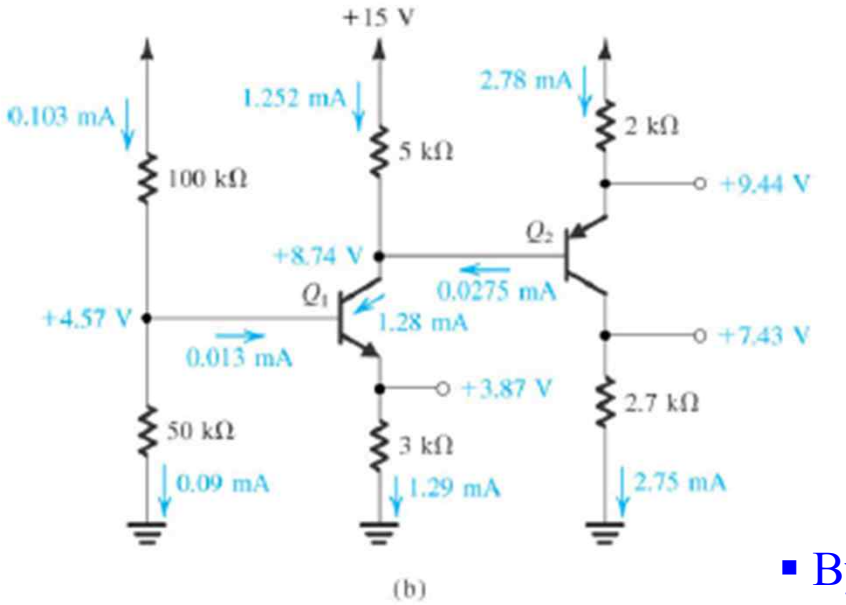
$$V_B = V_{BE} + I_E R_E = 4.57V$$

$$V_C = 15 - I_C R_C = 8.6V$$

$V_C = V_B + 4.03V$ → active mode O.K

Analysis of BJT Circuits at DC





Ex. 4.11

Assume Q_1 is still in the active mode

$$V_{B1} = +4.57\ V,\quad I_{E1} = 1.29\ mA$$

$$I_{B1} = 0.0128\ mA,\quad I_{C1} = 1.28\ mA$$

Assume $I_{B2} << I_{C1}$

$$V_{C1} \approx +15 - I_{C1}R_{C1} = +8.6\ V$$

Q_1 in active mode
Forward biased EBJ of Q_2

$$V_{E2} = V_{C1} + V_{EB}\big|_{Q_2} \approx +9.3\ V$$

$$I_{E2} = \frac{+15 - V_{E2}}{R_{E2}} = 2.85\ mA$$

$$I_{C2} = \alpha_2 I_{E2} = 2.82\ mA\ (assume\ \beta_2 = 100)$$

$$I_{B2} = \frac{I_{E2}}{\beta_2 + 1} = 0.028\ mA$$

Q_2 in active mode

$$V_{C2} = R_{C2}I_{C2} = 2.7 \cdot 2.82 = +7.6\ V$$

$$V_{B2} = V_{C1} = +8.6\ V$$

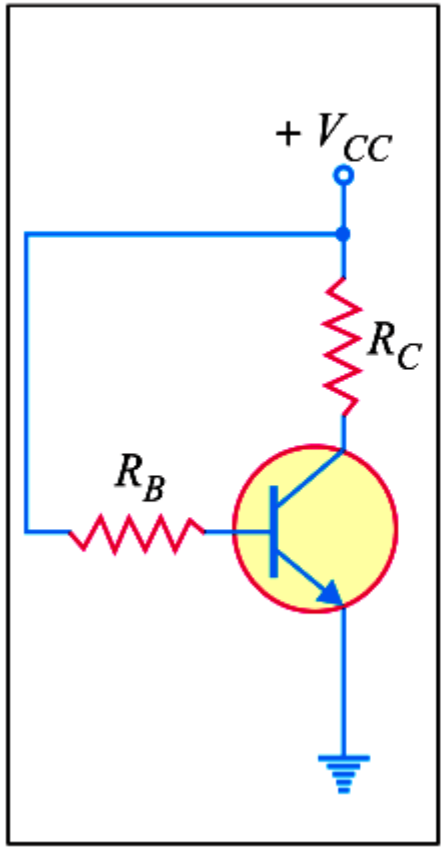
$$\rightarrow V_{BC}\big|_{Q_2} = +1.0\ V > 0$$

Q_2 in active mode O.K

- By iteration, more accurate results are obtained

OTHER BIASING SCHEMES

BASE BIAS

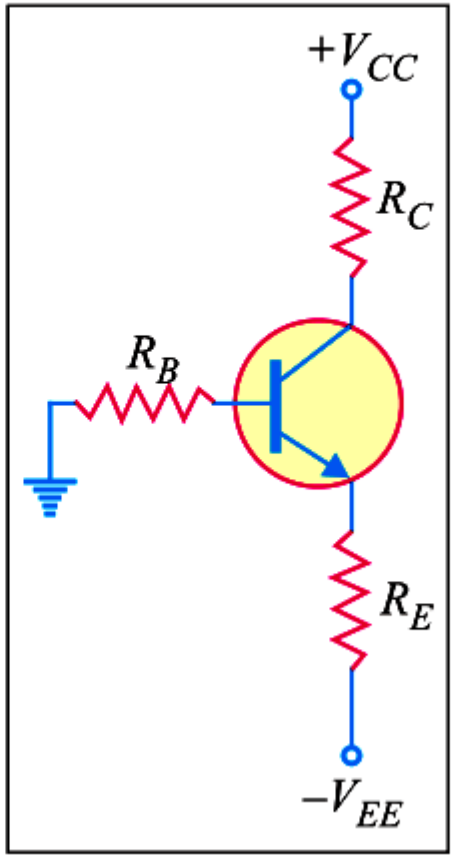


- Q-point values ($I_C \simeq I_E$)
- Collector current:

$$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

- Collector-to-emitter voltage:
- $V_{CE} = V_{CC} - I_C R_C$

EMITTER BIAS 1



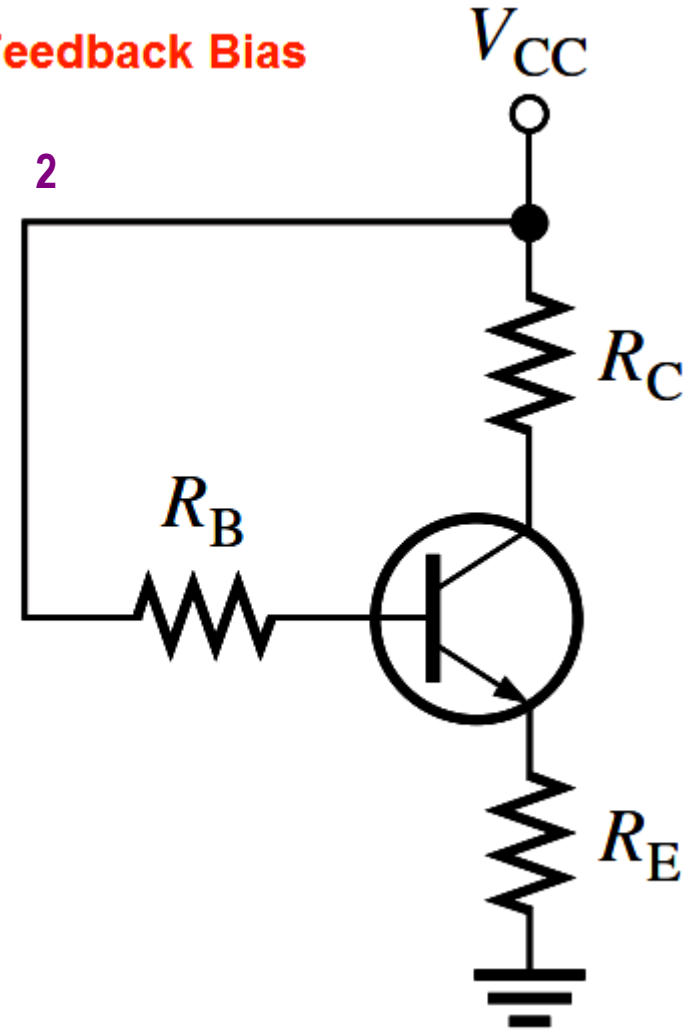
- Q-point values ($I_C \simeq I_E$)
- Collector current:

$$I_C \simeq \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

- Collector-to-emitter voltage:
- $V_{CE} \simeq V_{CC} - V_{CE} - I_C(R_C + R_E)$

Emitter Feedback Bias

2



$$
\begin{aligned}
V_{CC} &= I_B R_B + V_{BE} + I_E R_E \\
&= I_B R_B + V_{BE} + (\beta + 1) I_B R_E \\
I_B &= \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}
\end{aligned}
$$

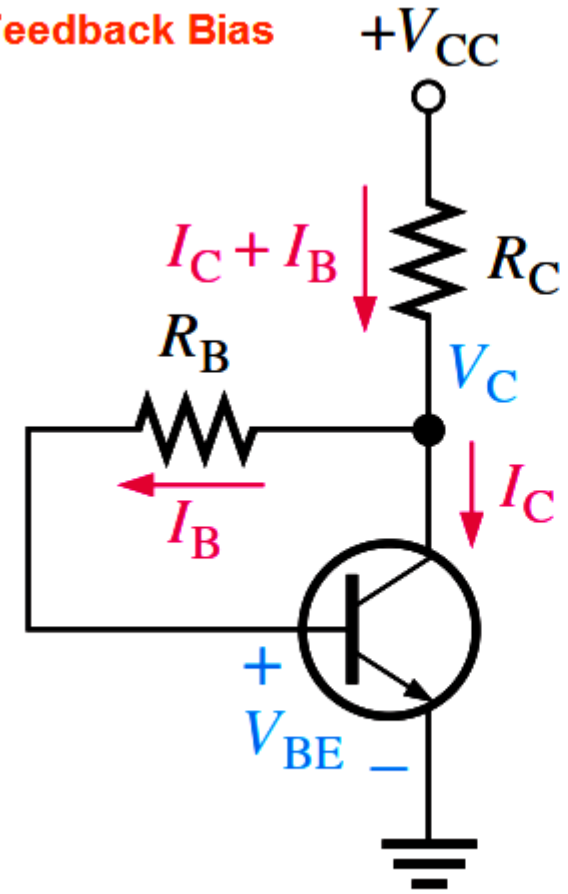
Therefore,

$$
I_C = \beta \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}
$$

and,

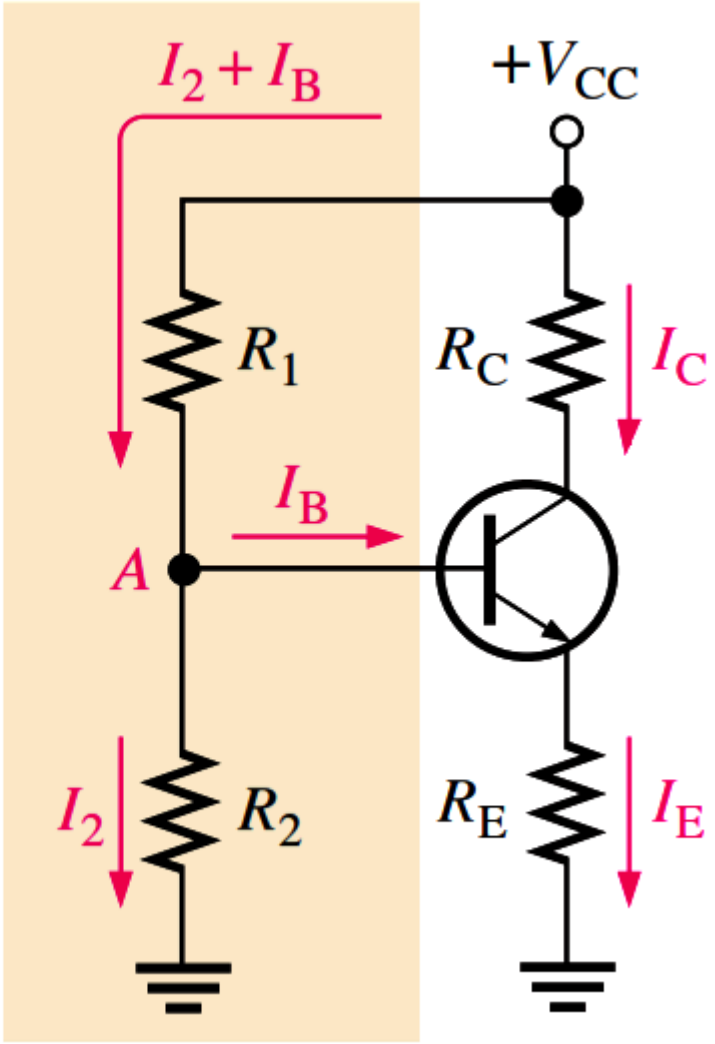
$$
\begin{aligned}
V_{CE} &= V_{CC} - I_C R_C - I_E R_E \\
&\approx V_{CC} - I_C (R_C - R_E)
\end{aligned}
$$

Collector Feedback Bias



$$
\begin{aligned}
V_{CC} &= (I_C + I_B)R_C + I_B R_B + V_{BE} \\
&= (\beta + 1) I_B R_C + I_B R_B + V_{BE} \\
I_B &= \frac{V_{CC} - V_{BE}}{(\beta+1)R_C + R_B} \\
I_C &= \beta I_B \\
&= \beta \frac{V_{CC} - V_{BE}}{(\beta+1)R_C + R_B}
\end{aligned}
$$

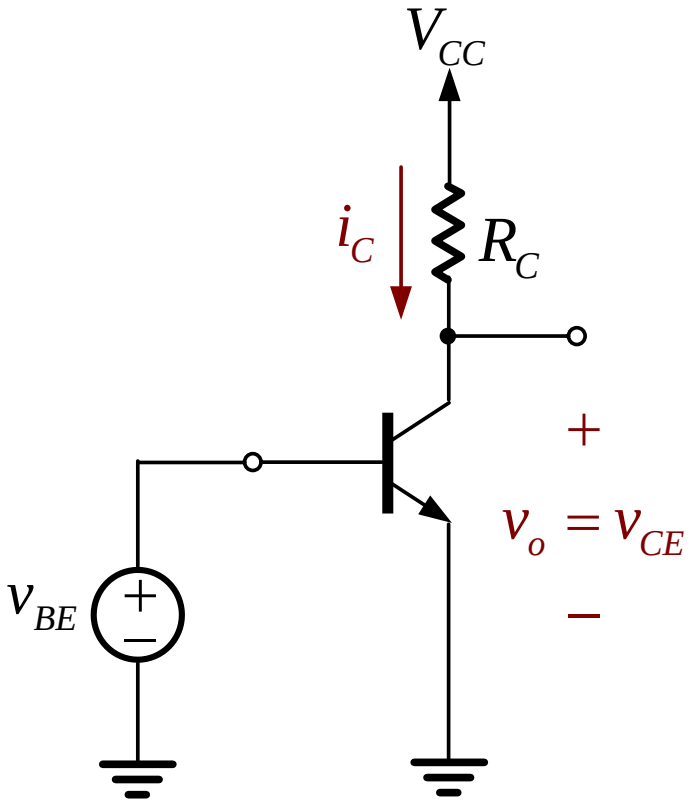
Voltage Divider Bias

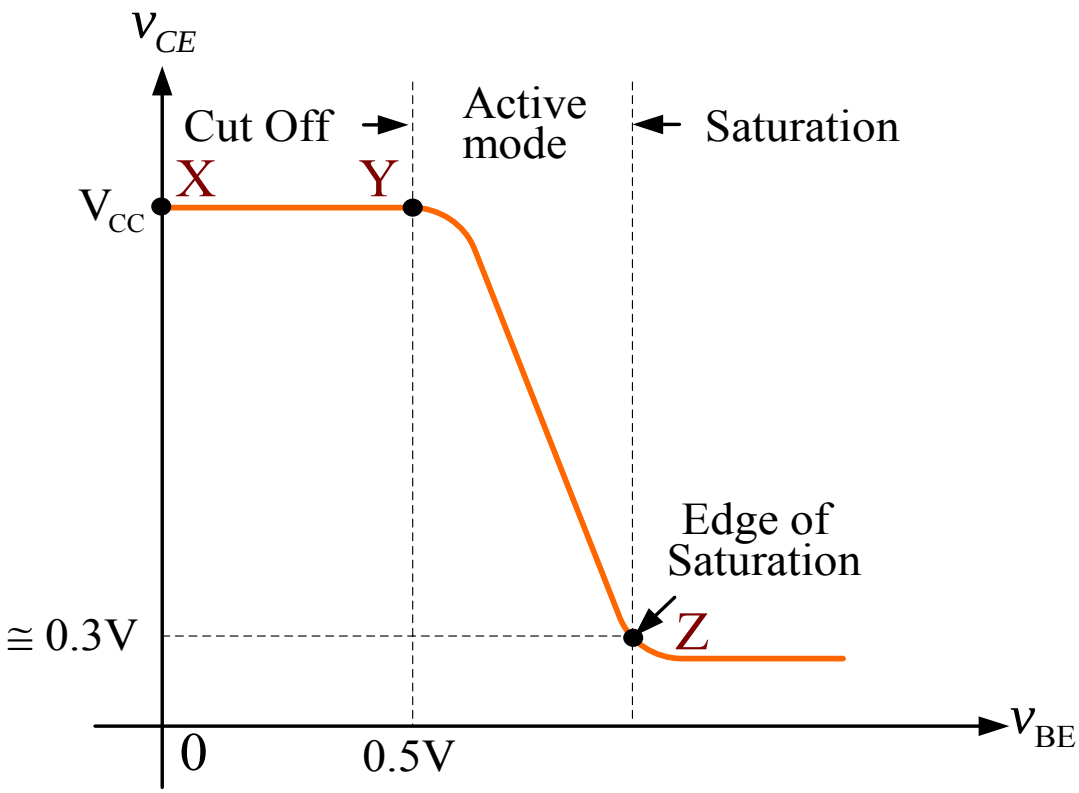


See Example 4.10

4.4 Applying the BJT in Amplifier Design

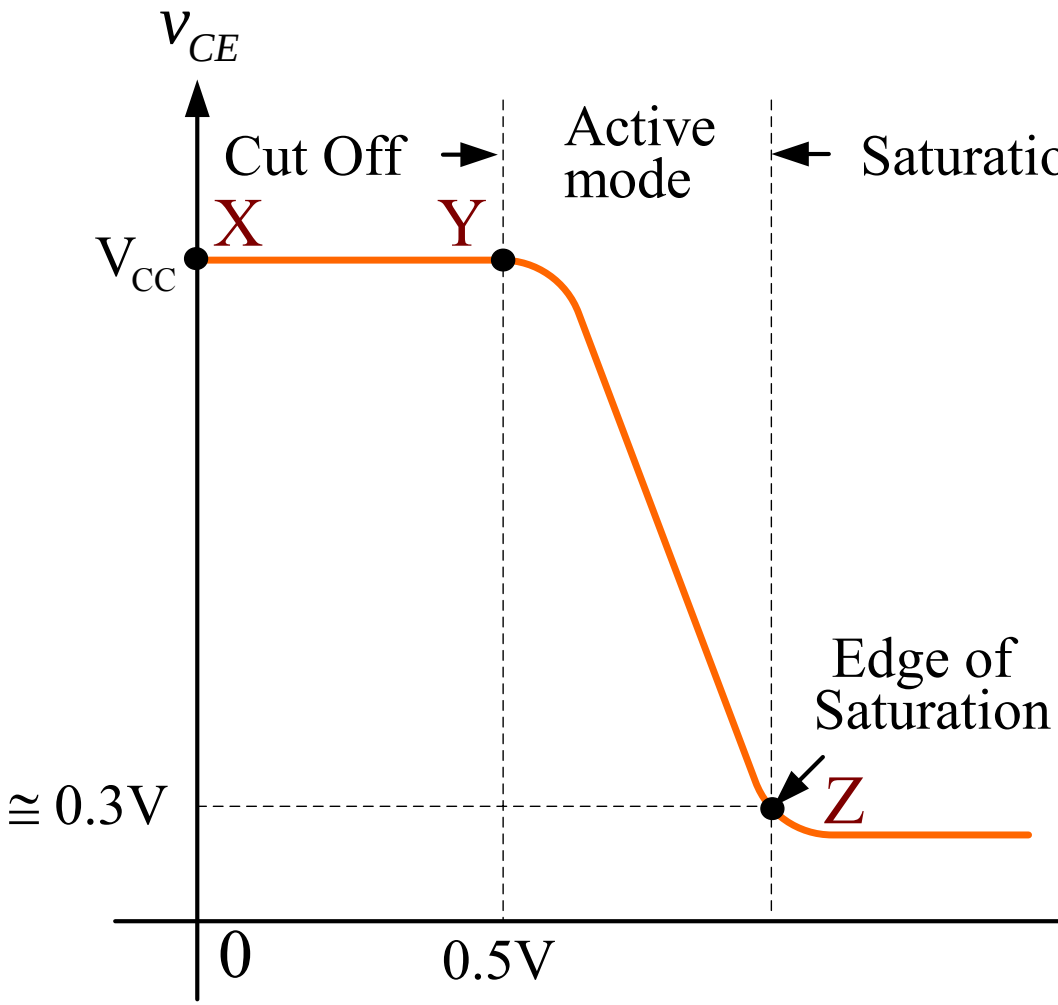
4.4.1 Obtaining a Voltage Amplifier





VOLTAGE TRANSFER CHARACTERISTICS

4.4.2 The Voltage Transfer Characteristic (VTC)

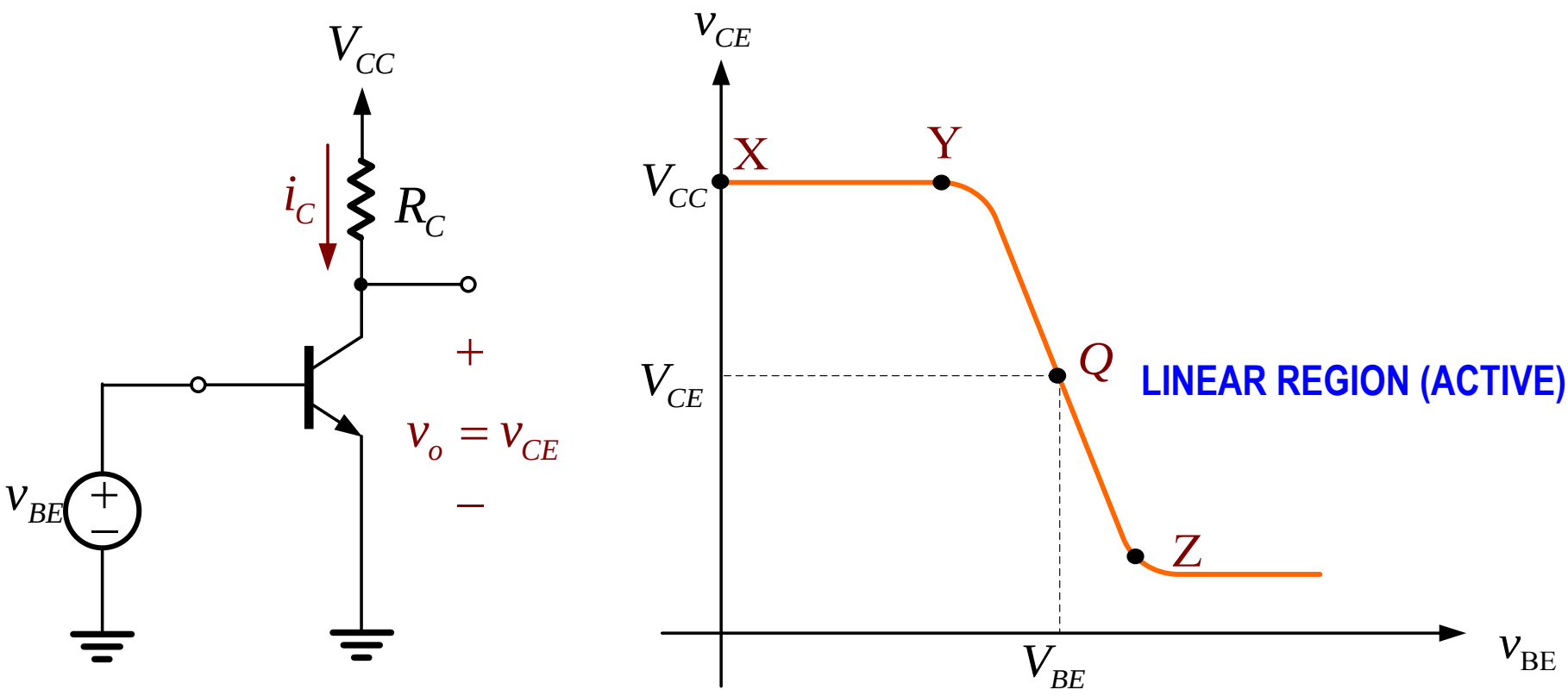


$$i_C = I_S e^{v_{BE}/V_T}$$

$$v_{CE} = V_{CC} - i_C R_C$$

$$= V_{CC} - R_C I_S e^{v_{BE}/V_T}$$

4.4.3 Biasing the BJT to Obtain Linear Amplification



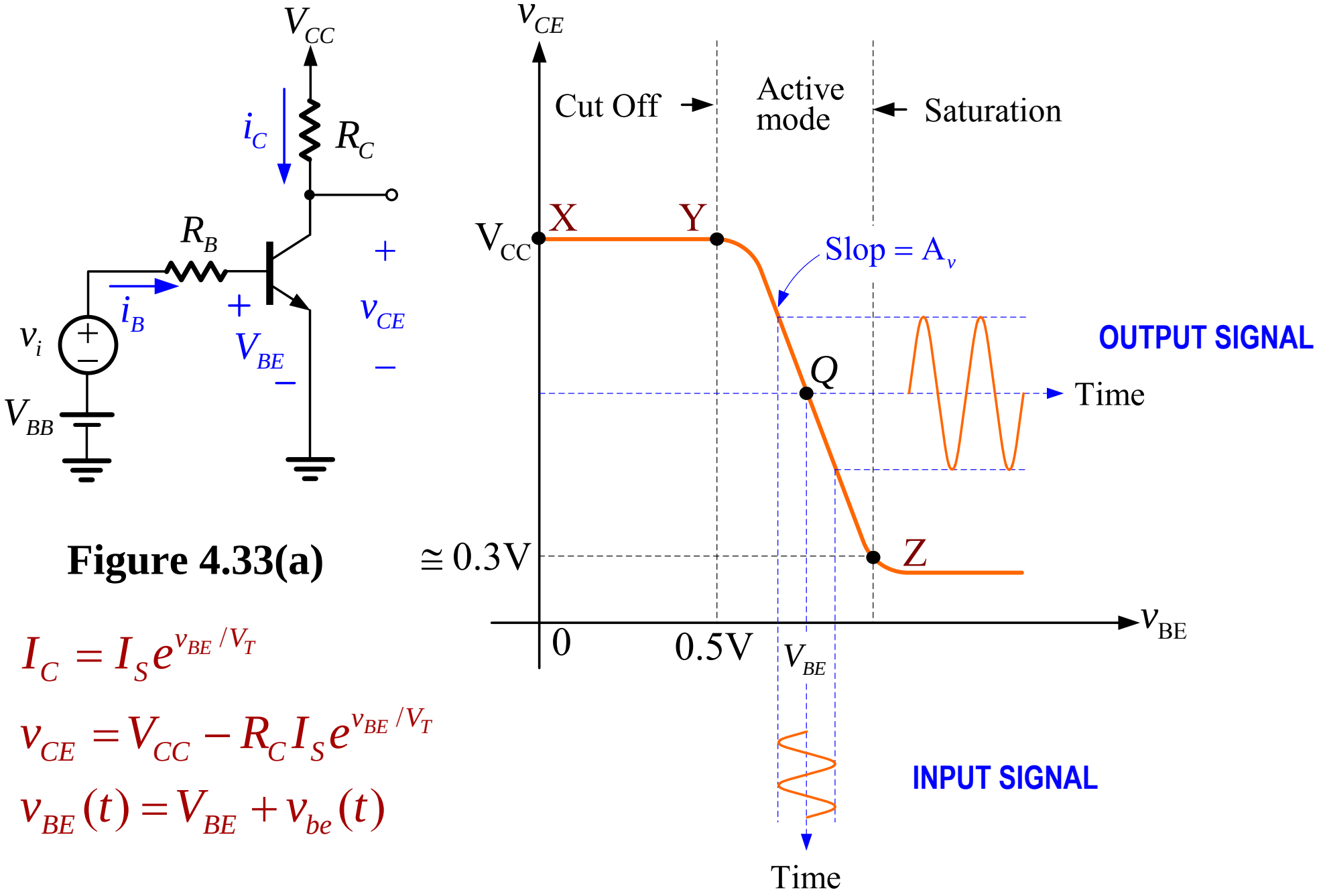


Figure 4.33(a)

$$I_C = I_S e^{v_{BE}/V_T}$$

$$v_{CE} = V_{CC} - R_C I_S e^{v_{BE}/V_T}$$

$$v_{BE}(t) = V_{BE} + v_{be}(t)$$

4.4.4 The Small-Signal Voltage Gain

$$A_v \equiv \left.\frac{dV_{CE}}{dV_{BE}}\right|_{v_{BE}=V_{BE}} \qquad (4.29)$$

$$\frac{dV_{CE}}{dV_{BE}} = -\frac{R_C}{V_T} I_S e^{v_{BE}/V_T} \Rightarrow A_v = -\left(\frac{I_C}{V_T}\right) R_C \qquad (4.30)$$

$$A_v = -\frac{I_C R_C}{V_T} = -\frac{V_{R_C}}{V_T}, \text{where } V_{R_C} = V_{CC} - V_{CE} \qquad (4.32)$$

The observations on this expression for the voltage gain:

❶ The gain is negative, which signifies that the amplifier is inverting ; that is, there is a 180^o phase shift between the input and the output.

❷ The gain is propotional to the collector bias current I_C and to the load resistance R_C.

4.4.5 Determining The VTC by Graphical Analysis / Load Line

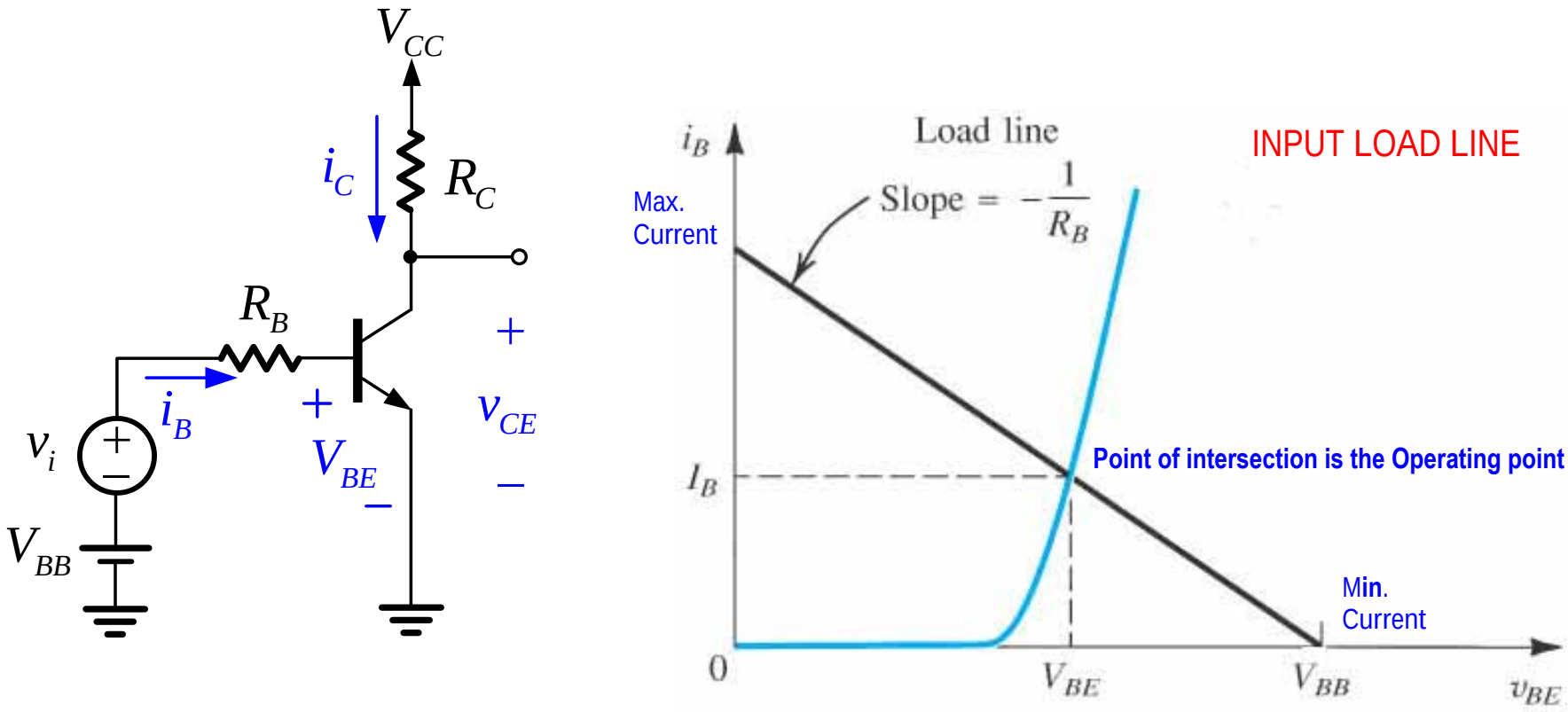
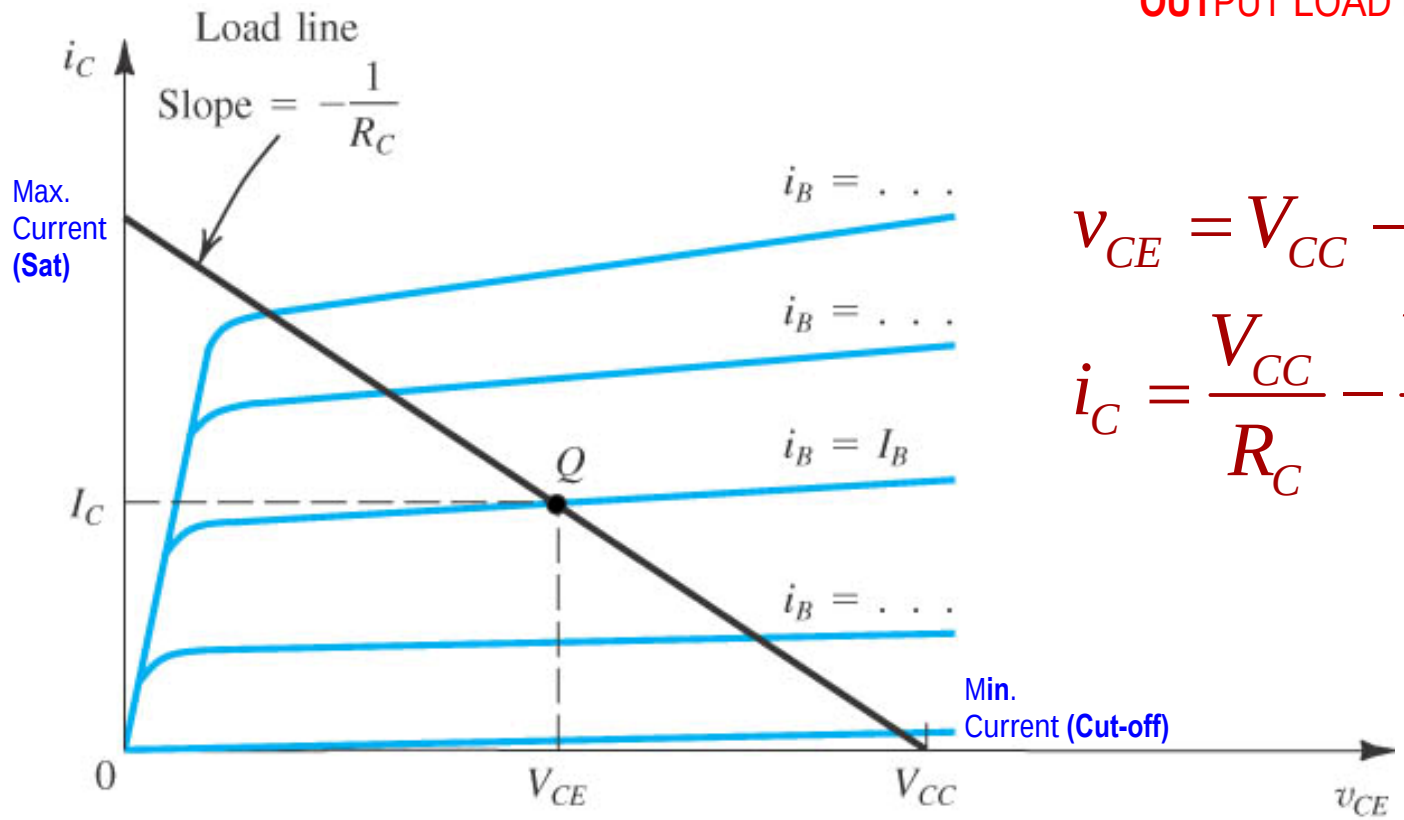


Figure 4.33(a)

Figure Graphical construction for the determination of the dc base current in the circuit of Fig.**4.33(a)**.

OUTPUT LOAD LINE



$$v_{CE} = V_{CC} - i_C R_C$$

$$i_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

Q-Point / Bias Point is the Intersection point (For a specific Base Current)

Figure 4.34 Graphical construction for determining the dc collector current I_C and the collector-to-emitter voltage V_{CE} in the circuit of Fig.4.33(a).

4.4.6 Locating the Bias Point (Q-point)

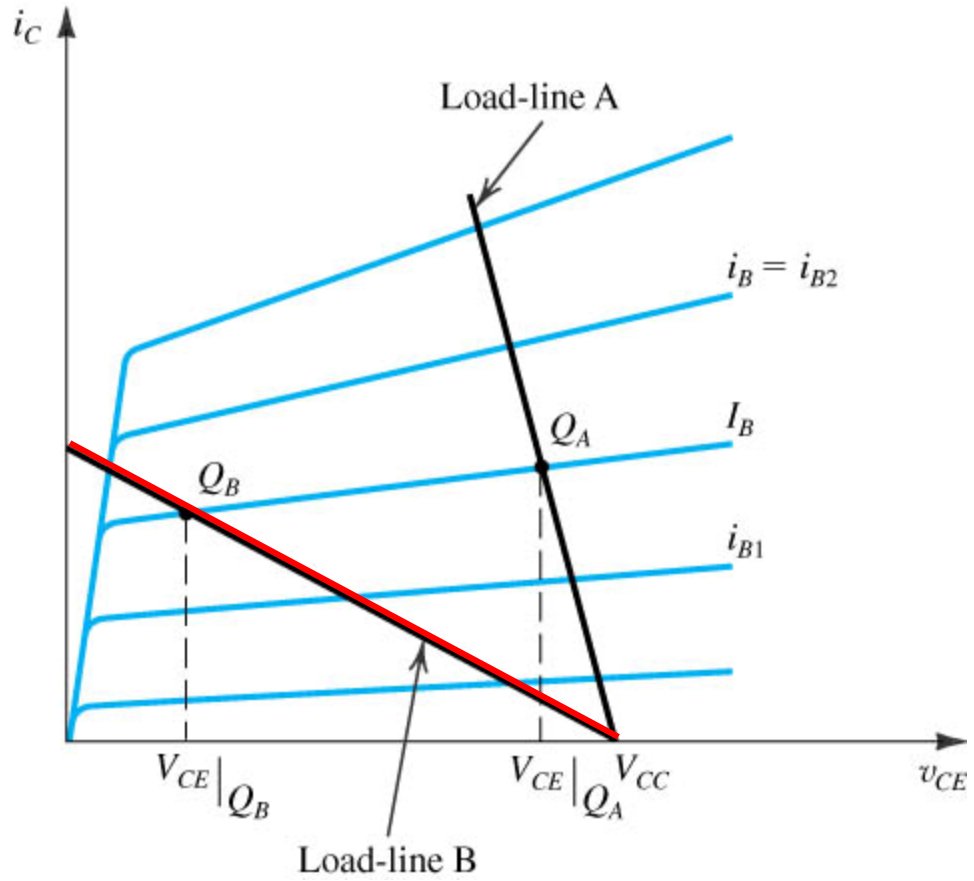
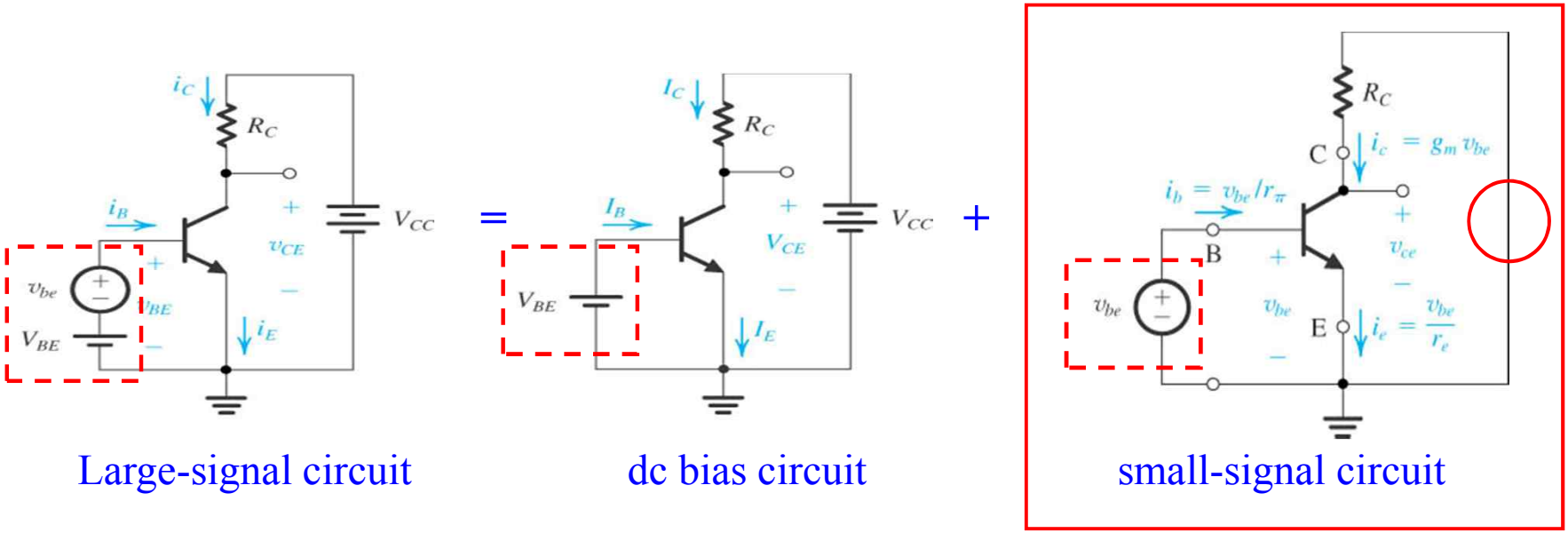


Figure 4.35 Effect of bias-point location on allowable signal swing: Load-line A results in bias point Q_A with a corresponding V_{CE} which is too close to V_{CC} and thus limits the positive swing of v_{CE}. At the other extreme, load-line B results in an operating point too close to the saturation region, thus limiting the negative swing of v_{CE}.

HIGHER LOAD MOVES Q POINT TOWARDS SATURATION (QA -> QB)

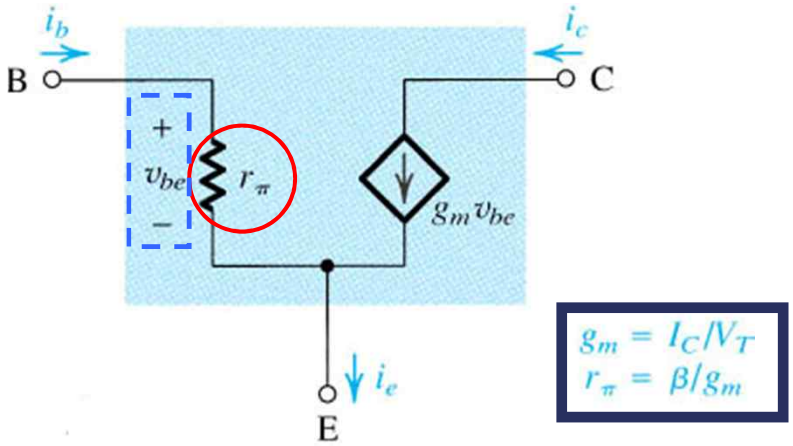
Separating the signal and DC quantities



Large-signal circuit dc bias circuit small-signal circuit

- Small-signal representation of BJT by eliminating the dc sources
  - Since the voltage of an ideal dc voltage source does not change, the signal voltage across it will be zero.
    V_{CC}, V_{BE} → ***SHORT*** circuits
  - Since the current of an ideal dc current source does not change, the signal current through it will be zero.
    Current source → ***OPEN*** circuits
  - resulting circuit is *equivalent to the transistor as far as small-signal operation is concerned* → equivalent small-signal model

Hybrid-π Model



$g_m = I_C/V_T$
$r_\pi = \beta/g_m$

- Voltage-controlled current source (transconductance amplifier)

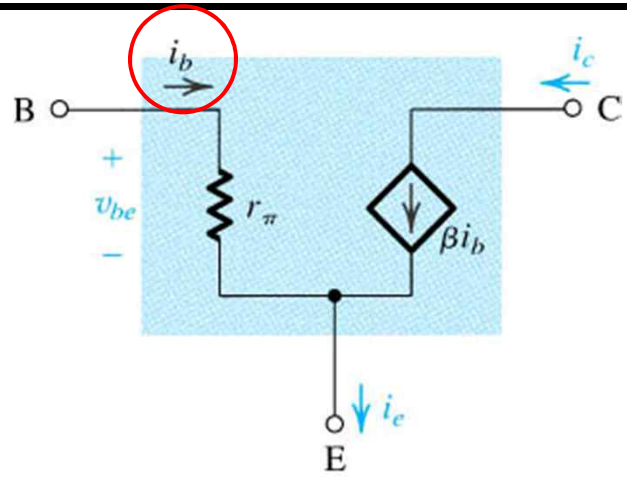
  - r_π : input resistance looking into the base

$$i_c = g_m v_{be}$$

$$i_b = v_{be} / r_\pi$$

$$i_e = \frac{v_{be}}{r_\pi} + g_m v_{be} = \frac{v_{be}}{r_\pi}\left(1 + g_m r_\pi\right)$$

$$= \frac{v_{be}}{r_\pi}\left(1+\beta\right) = v_{be} / \left(\frac{r_\pi}{\left(1+\beta\right)}\right) = v_{be} / r_e$$



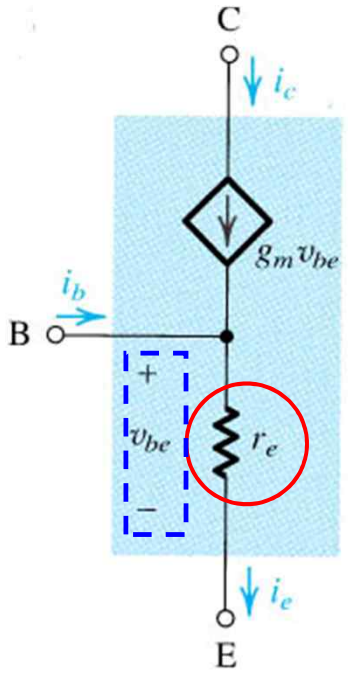
- Current-controlled current source (current amplifier)

$$i_c = g_m v_{be} = g_m\left(i_b r_\pi\right)$$

$$= \left(g_m r_\pi\right) i_b = \beta i_b$$

- The most widely used hybrid–π model
- The model parameters g_m and r_π depend on the value of the dc bias current I_C

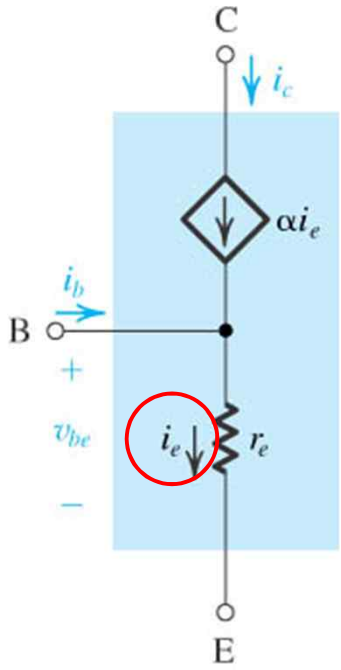
T Model



$$g_m = I_C/V_T$$

$$r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m}$$

Emitter resistance r_e



- VCCS

$$i_b = \frac{v_{be}}{r_e} - g_m v_{be} = \frac{v_{be}}{r_e}(1 - g_m r_e)$$

$$= \frac{v_{be}}{r_e}(1-\alpha) = \frac{v_{be}}{r_e}\left(1 - \frac{\beta}{\beta+1}\right)$$

$$= \frac{v_{be}}{r_e(\beta+1)} = \frac{v_{be}}{r_\pi}$$

- CCCS

$$i_c = g_m v_{be} = g_m(i_e r_e)$$

$$= (g_m r_e) i_e = \alpha i_e$$

- r_e : input resistance looking into the emitter

Application of the Small-signal Equivalent circuits

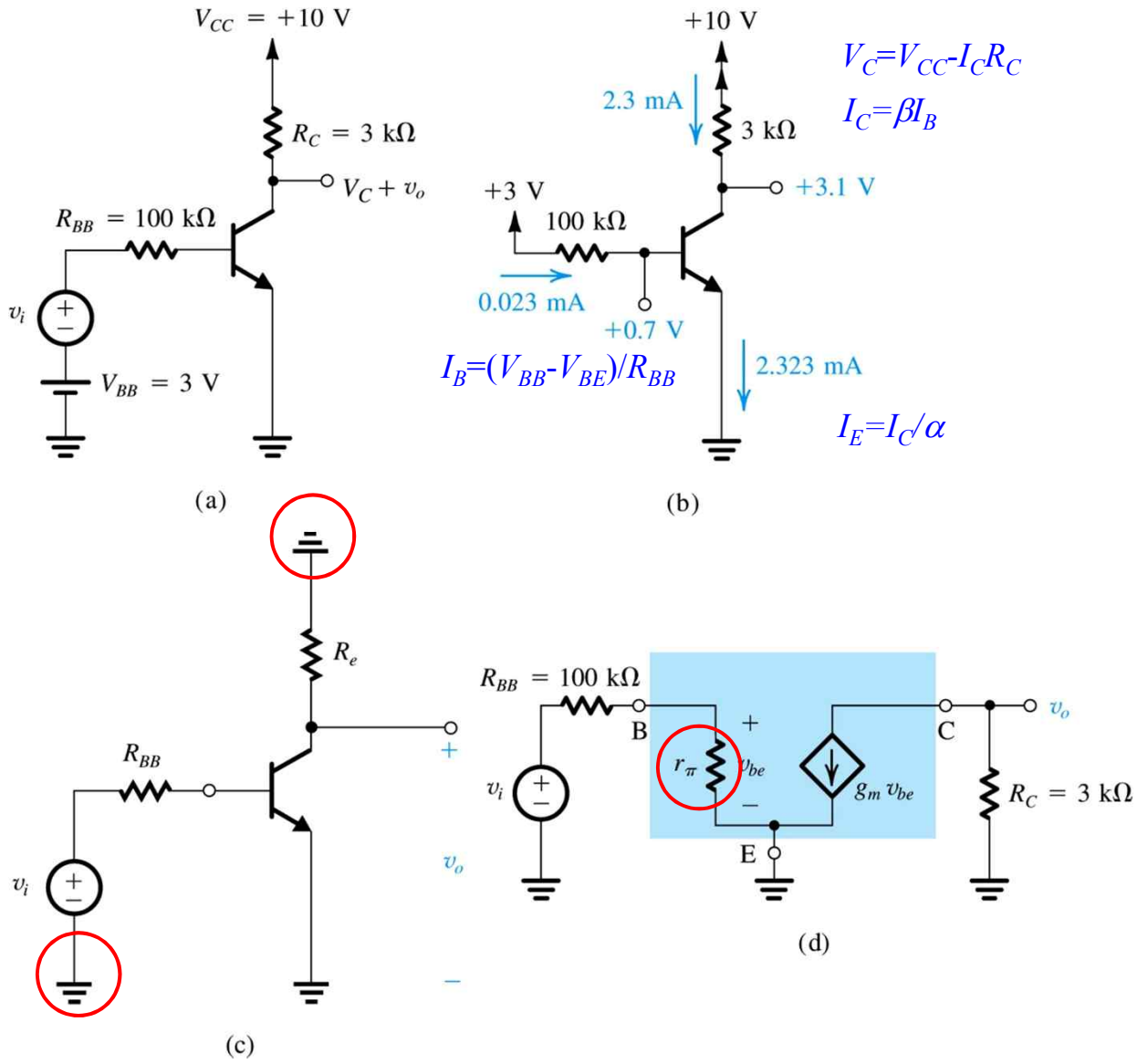
- Systematic process to analyze transistor amplifier circuits

1. Determine the *dc operating point* of the BJT and in particular the dc collector current I_C.
2. Calculate the values of the *small-signal model parameters*:

$$g_m = \frac{I_C}{V_T}, \quad r_\pi = \frac{V_T}{I_B} = \frac{\beta}{g_m}, \quad r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m} \approx \frac{1}{g_m}$$

3. Eliminate the dc sources by replacing each *dc voltage* source with a *short* circuit and each *dc current* source with an *open* circuit.
4. Replace the BJT with one of its *small-signal equivalent circuit models*.
5. Analyze the resulting circuit to determine the required quantities.
(e.g., voltage gain, input resistance)

Example 4.14



- Voltage gain ($\beta = 100$)

(b) dc analysis
- Q point by setting $v_i = 0$

$$r_e = \frac{V_T}{I_E} = 10.8\ \Omega$$

$$g_m = \frac{I_C}{V_T} = 92\ mA/V$$

$$r_\pi = \frac{\beta}{g_m} = 1.09\ k\Omega$$

(c) small-signal analysis
- No dc : V_{CC} → signal ground

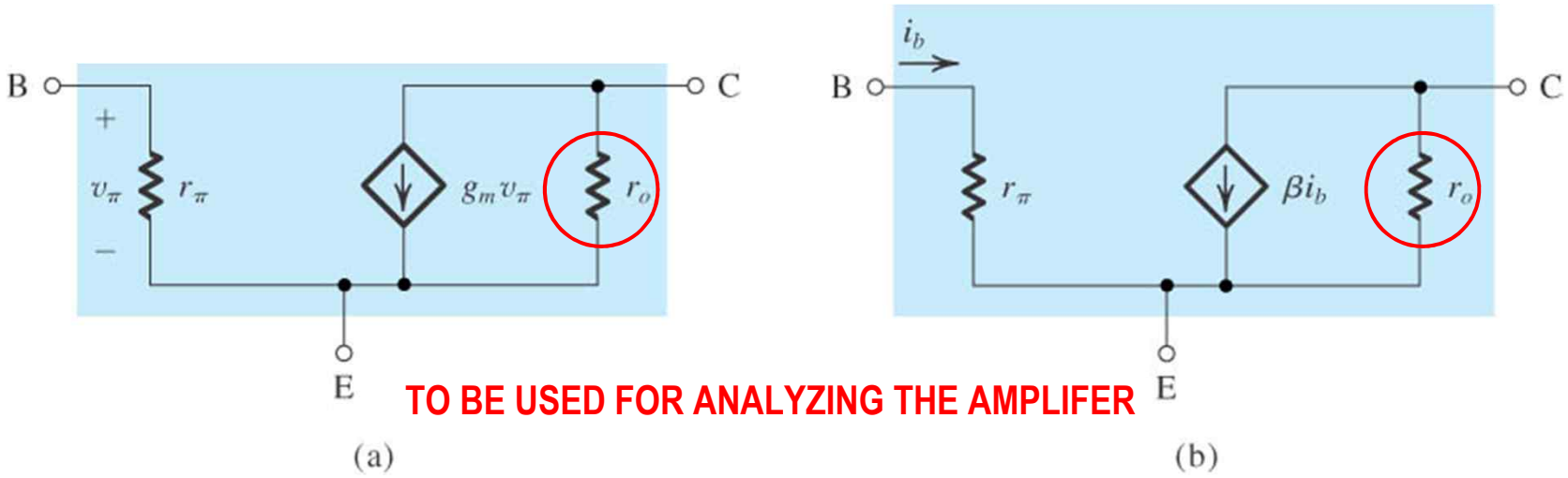
$$v_{be} = v_i \frac{r_\pi}{r_\pi + R_{BB}} = 0.011 v_i$$

$$v_o = -g_m v_{be} R_C = -3.04 v_i$$

$$A_v = \frac{v_o}{v_i} = \frac{v_o}{v_{be}} \frac{v_{be}}{v_i} = -g_m R_C \frac{r_\pi}{r_\pi + R_{BB}}$$

$$\Rightarrow A_v = -3.04\ V/V$$

Augmented Hybrid-π Model (*Early* Effect)



TO BE USED FOR ANALYZING THE AMPLIFER

- Early effect : i_C depends on v_{BE} & v_{CE} → finite r_o

$$r_o = \left[\frac{\partial i_C}{\partial v_{CE}}\right]^{-1}_{v_{BE}=constant} = \frac{V_A + V_{CE}}{I_C} \approx \boxed{\frac{V_A}{I_C}} \quad \triangleright \quad i_c = g_m v_{be} + \boxed{v_{ce}/r_o}$$

- The effect of r_o on the operation of the transistor as an amplifier → reduced gain

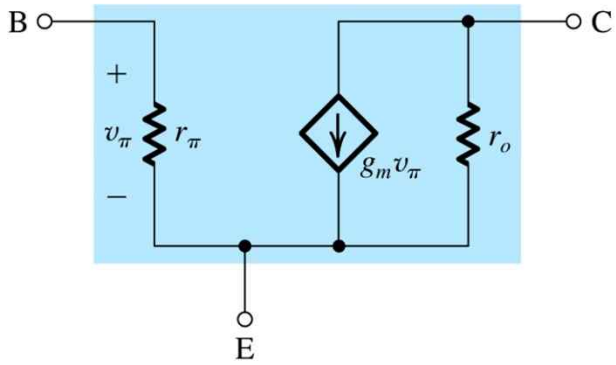
$$v_o = -g_m v_{be} R_C \Rightarrow v_o = -g_m v_{be} \boxed{(R_C \,//\, r_o)}$$

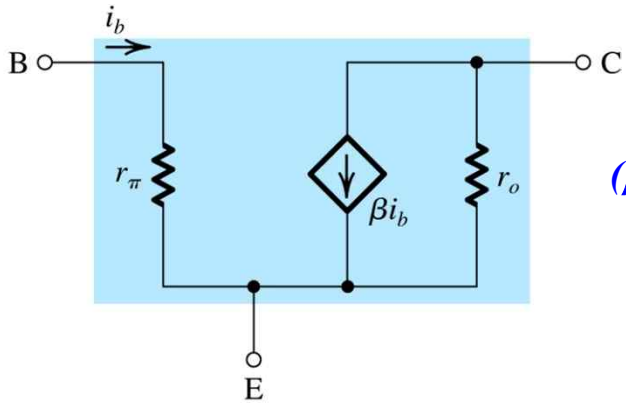
- in integrated-circuit BJT amplifiers, r_o plays a dominant role and cannot be neglected

BJT Small Signal Model

Hybrid-π Model

($g_m v_\pi$) Version

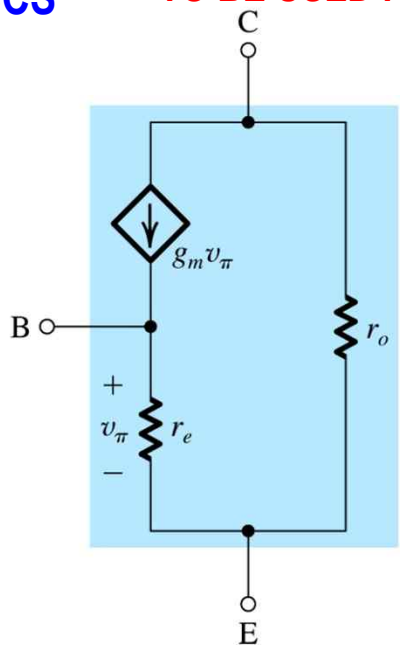


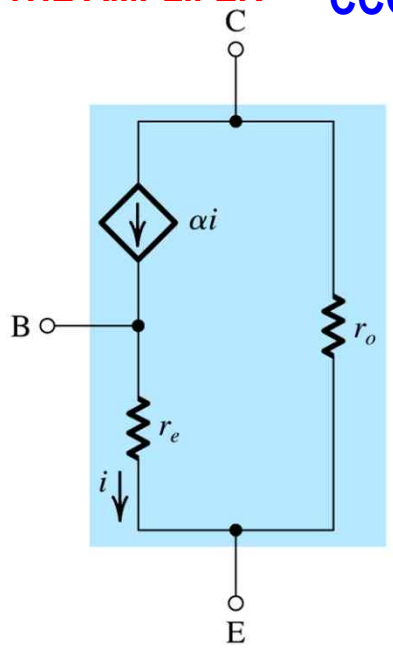


(βi_b) Version

VCCS **TO BE USED FOR ANALYZING THE AMPLIFER** **CCCS**

($g_m v_\pi$) Version





(αi) Version

Table 6.4 Small-Signal Models of the BJT

$$
\begin{aligned}
g_m &= \delta I_C/\delta V_{BE} &&= I_C/V_T \\
r_\pi &= \delta V_{BE}/\delta I_B &&= \beta/g_m \\
r_o &= \delta V_{CE}/\delta I_C &&= V_A/I_C \\
r_e &= \delta V_{BE}/\delta I_E &&= V_T/I_E \\
\beta &= \delta I_C/\delta I_B &&= g_m r_\pi
\end{aligned}
$$

ALL SMALL SIGNAL PARAMETERS ARE TO BE EVALUATED AT BIAS (Q) POINT

Small Signal Parameter Summary

Model Parameters in Terms of DC Bias Currents

$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha\left(\frac{V_T}{I_C}\right) \qquad r_\pi = \frac{V_T}{I_B} = \beta\left(\frac{V_T}{I_C}\right) \qquad r_o = \frac{|V_A|}{I_C}$$

In Terms of g_m

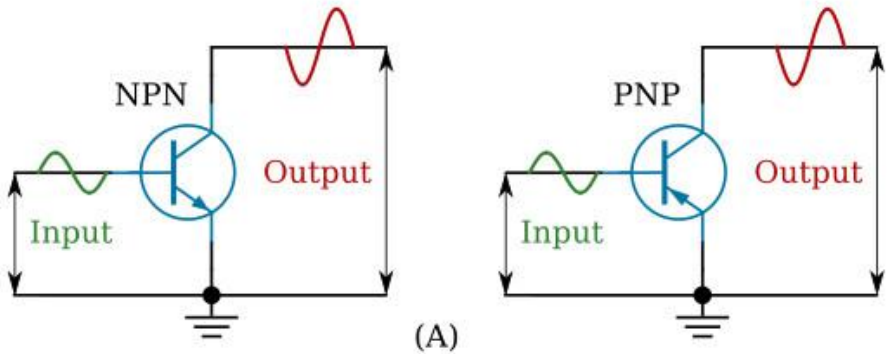
$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m}$$

In Terms of r_e

$$g_m = \frac{\alpha}{r_e} \qquad r_\pi = (\beta+1)r_e \qquad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

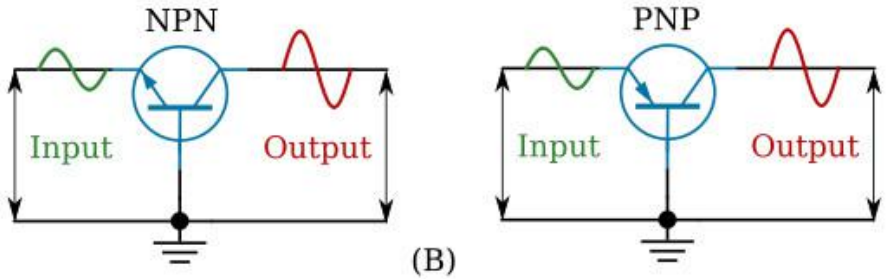
Relationships Between α and β

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad \beta+1 = \frac{1}{1-\alpha}$$



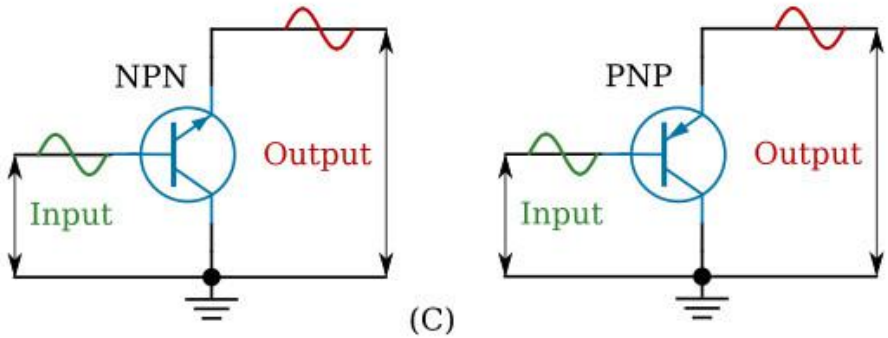
(A)

Common emitter



(B)

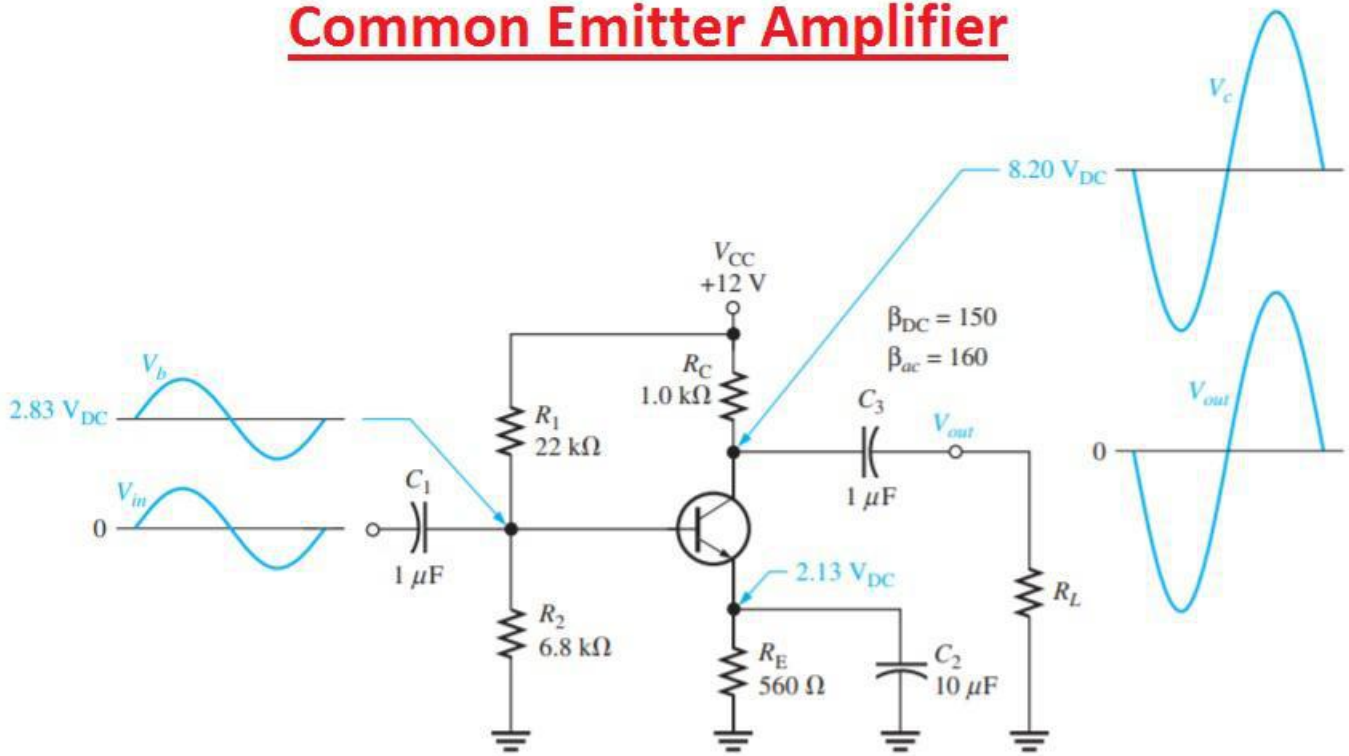
Common base



(C)

Common collector

Common Emitter Amplifier



a) For the emitter-follower amplifier circuit with source and load resistances shown in Figure 3:
   i) Draw the dc equivalent circuit and calculate the values of I_B, and r_e assume the transistor has a $\beta = 120$.
   ii) Draw the ac equivalent circuit using the r_e model for the BJT.
   iii) Find the input Z_i and output Z_o impedances of the circuit (assume r_o is very large compared to R_c).
   iv) Find the no load voltage gain A_{VNL}, the voltage gain A_{VL} with R_L= 2.7 kΩ, and the overall voltage gain of the amplifier A_{VS}.
   v) Find the output voltage if Vs = $20x10^{-3}$ sinωt volts.

COMMON COLLECTOR AMPLIFIER

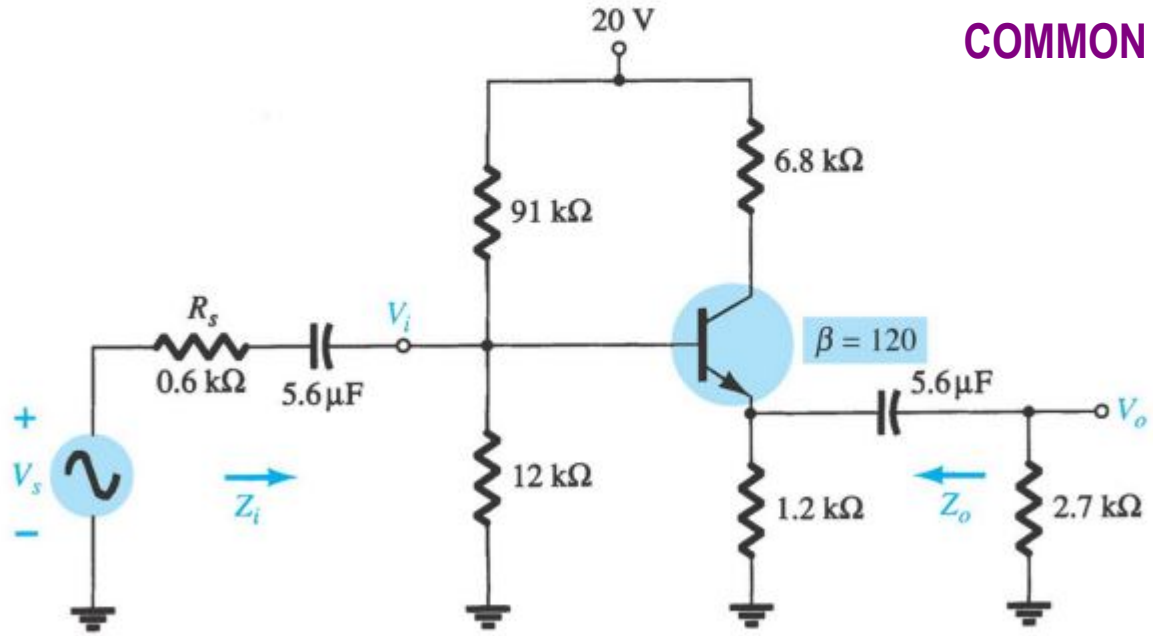
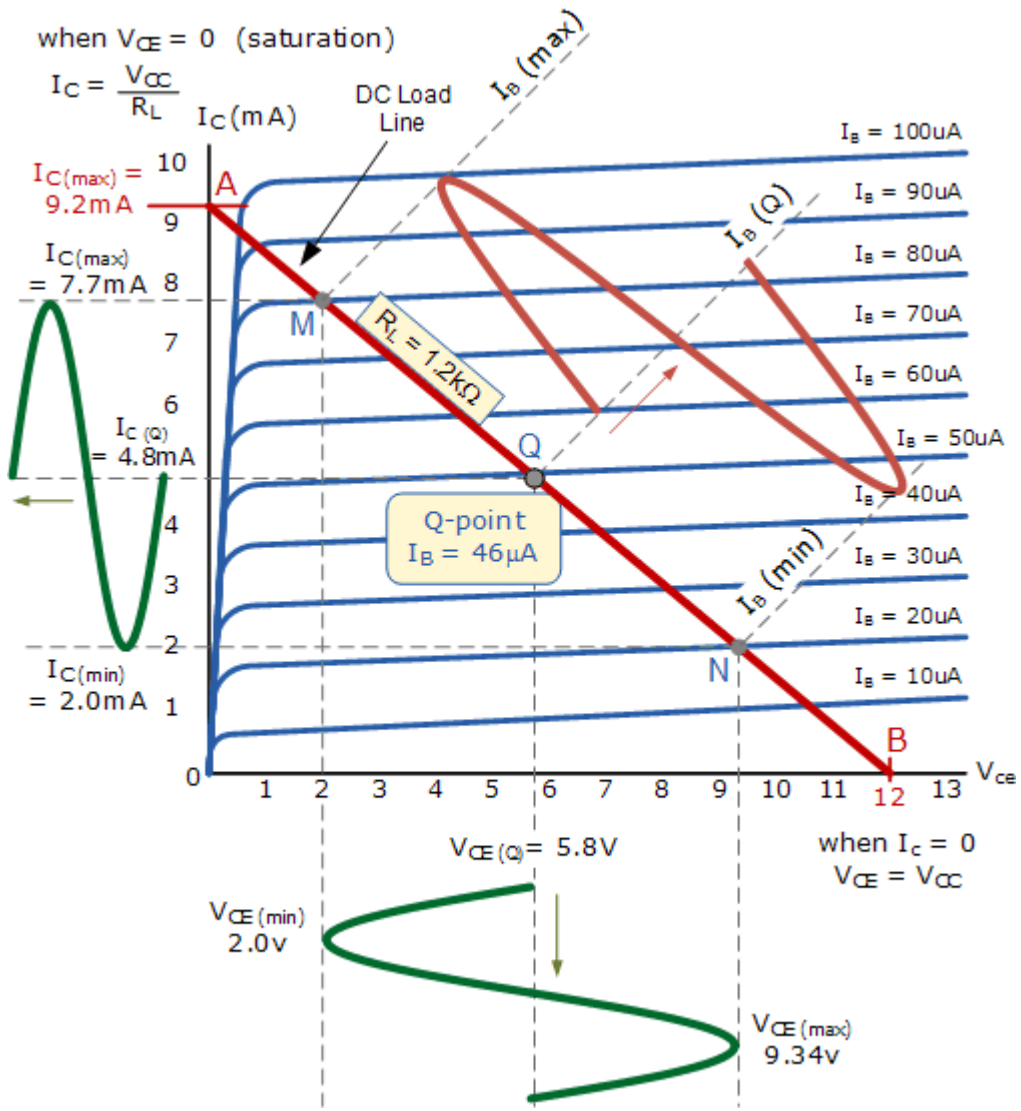


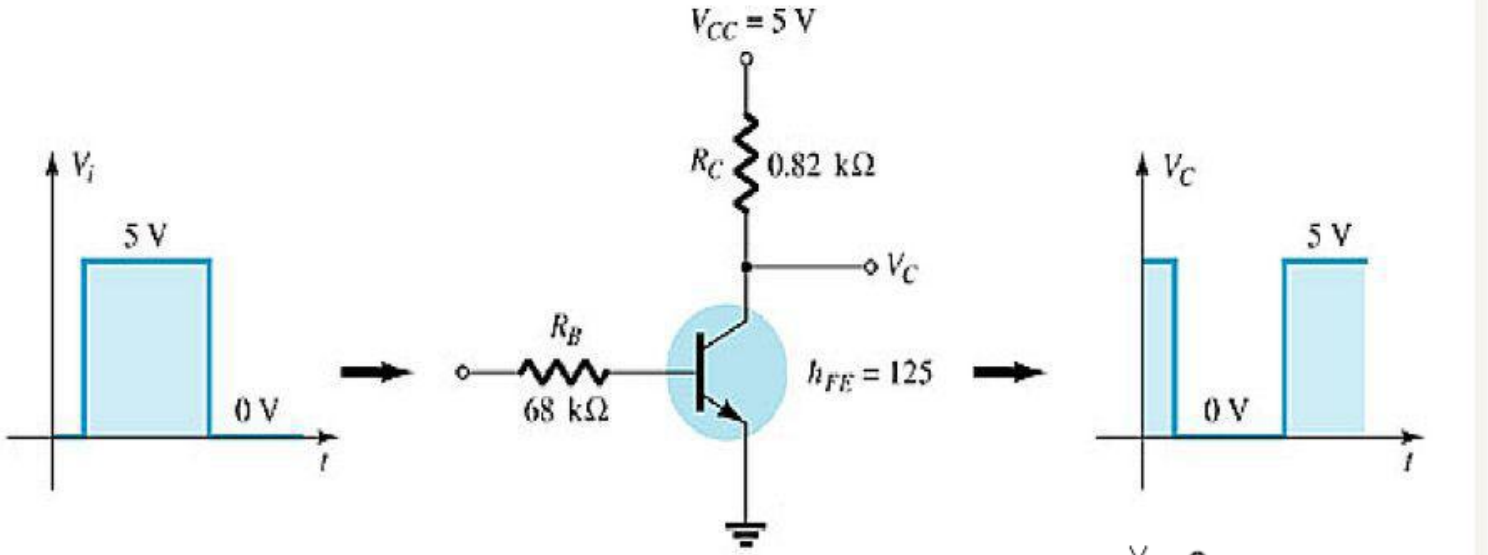
Figure 3 Transistor amplifire circuit with source Vs and load R_L

GRAPHICAL METHOD TO OBTAIN THE AMPLIFIER RESPONSE



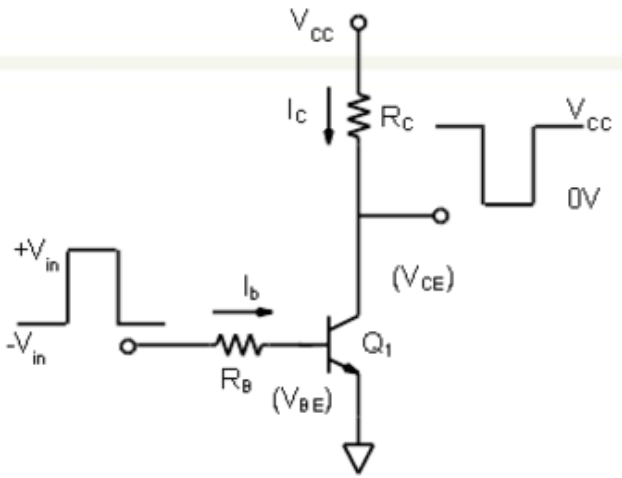
Transistor Switching Networks

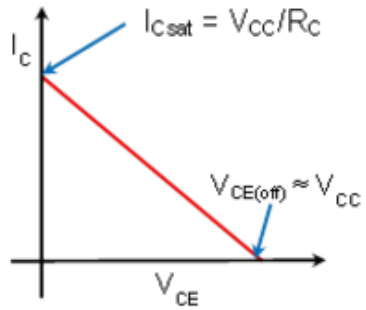
TRANSISTOR CAN BE USED AS VOLTAGE CONTROLLED SWITCH



WHEN BASE VOLTAGE LOW => SWITCH O**FF**

WHEN BASE VOLTAGE **HIGH** => SWITCH **ON**





Load Line

Transistor As Switch

WHEN BASE VOLTAGE LOW => SWITCH OFF

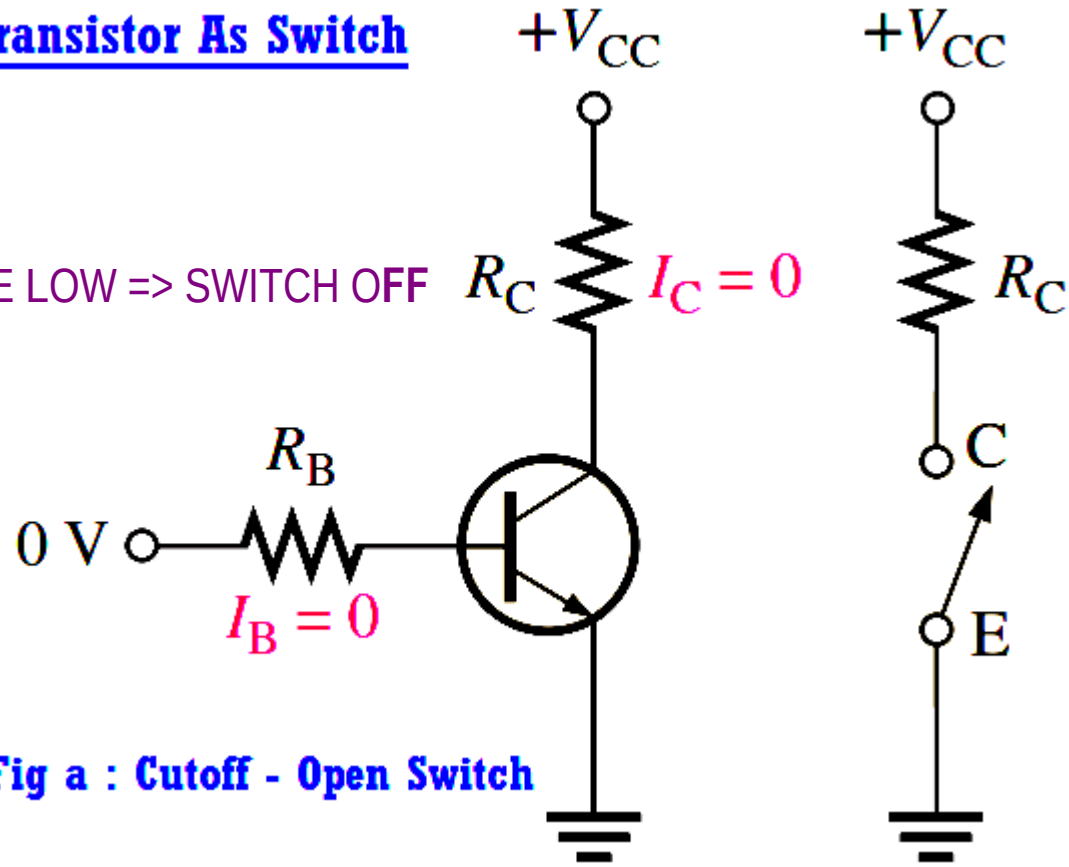


Fig a : Cutoff - Open Switch

Transistor As Switch

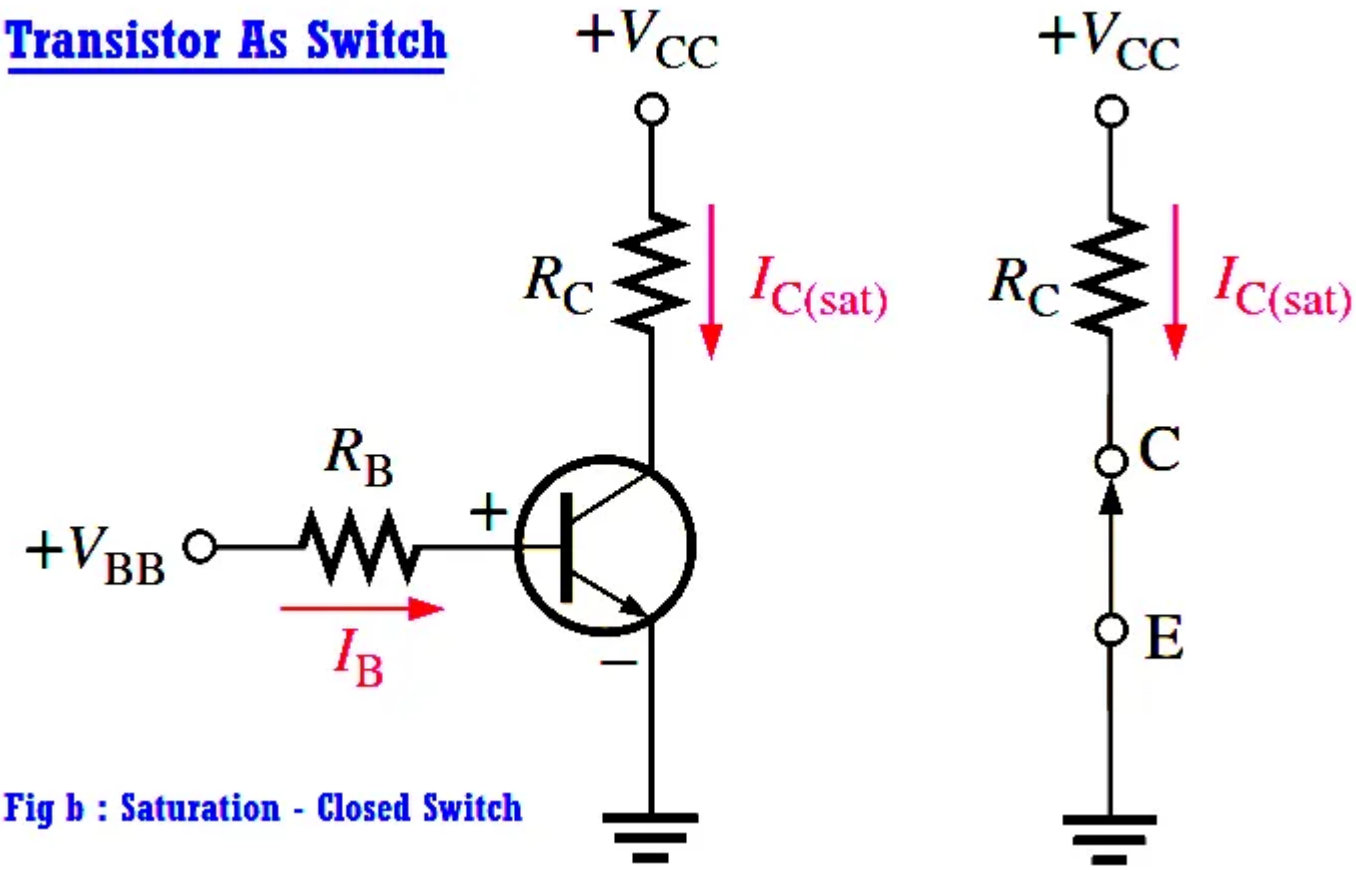


Fig b : Saturation - Closed Switch

WHEN BASE VOLTAGE HIGH => SWITCH **ON**

STABILITY OF BIASING CIRCUITS

Objective of Biasing :
To Operate the BJT in Desired Mode (eg., Active)
To Set the Q point such the it is independent of Transistor parameters (Beta, V_BE, I_CO)
No Distortion
Q-point should not vary as transistor parameters change.

In reality, Transistor parameters change with Temperature :

a) Reverse saturation current I_CO doubles per 10 degree rise in Temperature
b) Base-Emitter junction drop (V_BE) decreases by 2 mV per degree rise in Temperature
c) Current gain Beta increases with Temperature

All these changes tend to increase the Collector current I_C; shifts the Q point upward as T increases

Stability Factor determines How Collector Current Changes with Transistor parameter variations

(namely I_CO, V_BE, Beta)

Based on how I_C varies with I_{CO}, Stabilty Factor $S_{I_{CO}}$ is defined as

$$S_{I_{CO}} = \delta I_C / \delta I_{CO} \quad : \quad \beta, V_{BE} = Constant$$

Similarly,

$$S_{\beta} = \delta I_C / \delta \beta \quad : \quad I_{CO}, V_{BE} = Constant$$

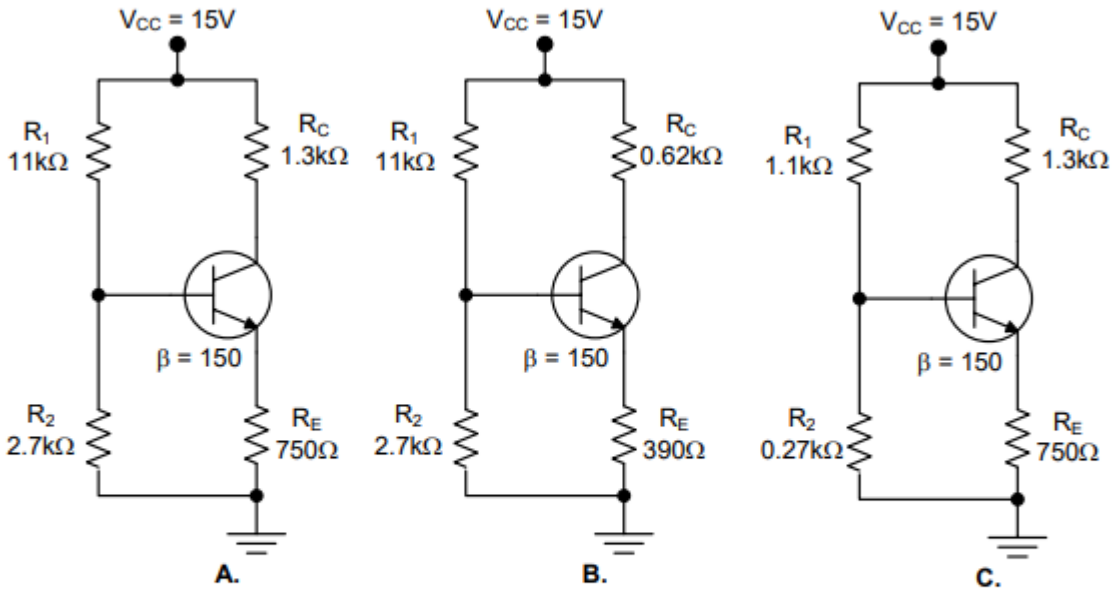
$$S_{V_{BE}} = \delta I_C / \delta V_{BE} \quad : \quad \beta, I_{CO} = Constant$$

Therefore,

$$\Delta I_C = S_{I_{CO}} \Delta I_{CO} + S_{\beta} \Delta \beta + S_{V_{BE}} \Delta V_{BE}$$

THESE STABILITY FACTORS ARE TO BE COMPUTED FROM THE BIAS NETWORK

4. Consider the emitter-stabilized and voltage divider bias circuits shown below.



a) Find the bias stability factors S(β) and S(V_{BE}) for circuit A.
b) Find the bias stability factors S(β) and S(V_{BE}) for circuit B.
c) Find the bias stability factors S(β) and S(V_{BE}) for circuit C.
d) Which circuit is least sensitive to variations in β?
e) Which circuit is least sensitive to variations in V_{BE}?