Q1.v | Q1_test.v | Q2.v | Q2_test.v

Generate Simulate

```
1  `include "Q1.v"
2  module top;
3  reg [7:0] a,b;
4  reg s0,s1,s2;
5  output [7:0] out;
6  bitwise mux (a,b,s0,s1,s2,out);
7  initial
8  begin
9  a=8'b10011010;
10 b=8'b11001101;
11 s0=1'b0; s1=1'b0; s2=1'b0;
12 #5 s0=1'b0; s1=1'b0; s2=1'b1;
13 #5 s0=1'b0; s1=1'b1; s2=1'b0;
14 #5 s0=1'b0; s1=1'b1; s2=1'b1;
15 #5 s0=1'b1; s1=1'b0; s2=1'b0;
16 #5 s0=1'b1; s1=1'b0; s2=1'b1;
17 #5 s0=1'b1; s1=1'b1; s2=1'b0;
18 #5 s0=1'b1; s1=1'b1; s2=1'b1;
19 end
20 initial
21 $monitor($time," a=%b and b=%b output=%b",a,b,out);
22 endmodule
```

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL

Verilog

```
[Run] Q1_test
                   0 a=10011010 and b=11001101 output=10001000
                   5 a=10011010 and b=11001101 output=01010111
                  10 a=10011010 and b=11001101 output=01110111
                  15 a=10011010 and b=11001101 output=11011111
                  20 a=10011010 and b=11001101 output=01100101
                  25 a=10011010 and b=11001101 output=00110010
                  30 a=10011010 and b=11001101 output=00100000
                  35 a=10011010 and b=11001101 output=10101000[Done] exit with code=0 in 0.016 seconds
```

Q1.v | Q1_test.v | Q2.v | Q2_test.v

Generate Simulate

```
1  `include "Q2.v"
2  module top;
3  reg [7:0] a;
4  output out_1,out_2;
5  parity_bit bit(a,out_1,out_2);
6  initial
7  begin
8  a=8'b11010010;
9  #5 a=8'b10011101;
10 end
11 initial
12 $monitor($time,"a=%b evenparity=%b oddparity=%b",a,out_1,out_2);
13 endmodule
```

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL

Verilog

```
[Compile] Q2_test.v
[Done] exit with code=0 in 0.023 seconds

[Run] Q2_test
                0a=11010010 evenparity=0 oddparity=1
                5a=10011101 evenparity=1 oddparity=0[Done] exit with code=0 in 0.02 seconds
```