File Edit Selection View Go Run Terminal Help

andgate_test.v - bin - Visual Studio Code

EXPLORER

BIN

- a.out
- andgate_test.v
- andgate.v
- andgatenor_test.v
- andgatenor.v
- full_adder_test.v
- full_adder.v
- half_adder_nand_t...
- half_adder_nand.v
- iverilog-vpi.exe
- iverilog.exe
- libbz2-1.dll
- libgcc_s_seh-1.dll
- libhistory8.dll
- libreadline8.dll
- libstdc++-6.dll
- libtermcap-0.dll
- libwinpthread-1.dll
- mux4x1_test.v
- mux4x1.v
- nandgate_test.v
- nandgate.v
- norgate_test.v
- norgate.v

OUTLINE

TIMELINE

andgate_test.v

andgate_test.v

```
1  `include "andgate.v"
2
3  module testbench;
4      reg b,c,d;
5      wire out;
6
7      andgate and2(out,b,c,d);
8
9      initial begin;
10         b = 1'b0;
11         c = 1'b1;
12         d = 1'b1;
13         #5;
14         b = 1'b1;
15         c = 1'b1;
16         d = 1'b1;
17     end
18
19     initial
20         $monitor($time, " : b=%b c=%b d=%b out=%b", b, c, d, out);
21 endmodule
```

Windows PowerShell

```
Windows PowerShell
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Try the new cross-platform PowerShell https://aka.ms/pscore6

PS C:\iverilog\bin> iverilog andgate_test.v
PS C:\iverilog\bin> vvp a.out
                    0 : b=0 c=1 d=1 out=0
                    5 : b=1 c=1 d=1 out=1
PS C:\iverilog\bin>
```

0 0 Connect Ln 1, Col 1 Spaces: 4 UTF-8 LF Verilog Go Live Go Live Prettier

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File Edit Selection View Go Run Terminal Help

orgate_test.v - bin - Visual Studio Code

EXPLORER

BIN

- libhistory8.dll
- libreadline8.dll
- libstdc++-6.dll
- libtermcap-0.dll
- libwinpthread-1.dll
- mux4x1_test.v
- mux4x1.v
- nandgate_test.v
- nandgate.v
- norgate_test.v
- norgate.v
- notgate_test.v
- notgate.v
- orgate_test.v
- orgate.v
- vvp.exe
- xnorgate_test.v
- xnorgate.v
- xorgate_test.v
- xorgate.v
- xorgatenand_test.v
- xorgatenand.v
- zlib1.dll

OUTLINE

TIMELINE

orgate_test.v

orgate_test.v

```
1  `include "orgate.v"
2
3  module testbench;
4      reg b,c,d;
5      wire out;
6
7      orgate or2(out,b,c,d);
8
9      initial begin;
10         b = 1'b0;
11         c = 1'b1;
12         d = 1'b1;
13         #5;
14         b = 1'b0;
15         c = 1'b0;
16         d = 1'b0;
17     end
18
19     initial
20         $monitor($time, " : b=%b c=%b d=%b out=%b", b, c, d, out);
21 endmodule
```

Windows PowerShell

```
Windows PowerShell
Copyright (C) Microsoft Corporation. All rights reserved.

Try the new cross-platform PowerShell https://aka.ms/pscore6

PS C:\iverilog\bin> iverilog andgate_test.v
PS C:\iverilog\bin> vvp a.out
                    0 : b=0 c=1 d=1 out=0
                    5 : b=1 c=1 d=1 out=1
PS C:\iverilog\bin> iverilog orgate_test.v
PS C:\iverilog\bin> vvp a.out
                    0 : b=0 c=1 d=1 out=1
                    5 : b=0 c=0 d=0 out=0
PS C:\iverilog\bin>
```

0 0 Connect Ln 1, Col 1 Spaces: 4 UTF-8 LF Verilog Go Live Go Live Prettier

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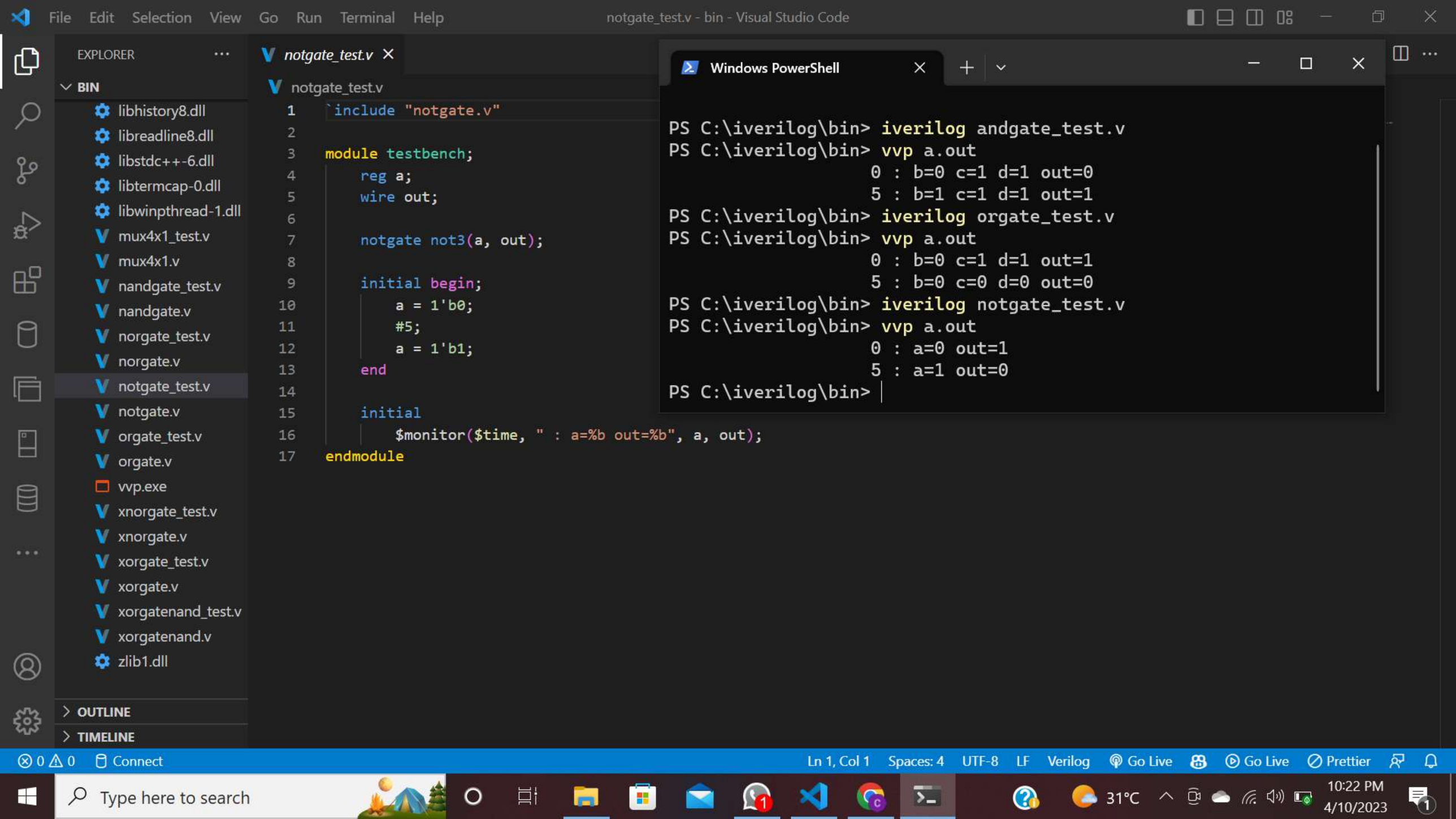
File Edit Selection View Go Run Terminal Help
notgate_test.v - bin - Visual Studio Code
EXPLORER
BIN
libhistory8.dll
libreadline8.dll
libstdc++-6.dll
libtermcap-0.dll
libwinpthread-1.dll
mux4x1_test.v
mux4x1.v
nandgate_test.v
nandgate.v
norgate_test.v
norgate.v
notgate_test.v
notgate.v
orgate_test.v
orgate.v
vvp.exe
xnorgate_test.v
xnorgate.v
xorgate_test.v
xorgate.v
xorgatenand_test.v
xorgatenand.v
zlib1.dll
OUTLINE
TIMELINE
notgate_test.v
notgate_test.v
1 `include "notgate.v"
2
3 module testbench;
4 reg a;
5 wire out;
6
7 notgate not3(a, out);
8
9 initial begin;
10 a = 1'b0;
11 #5;
12 a = 1'b1;
13 end
14
15 initial
16 $monitor($time, " : a=%b out=%b", a, out);
17 endmodule
Windows PowerShell
PS C:\iverilog\bin> iverilog andgate_test.v
PS C:\iverilog\bin> vvp a.out
0 : b=0 c=1 d=1 out=0
5 : b=1 c=1 d=1 out=1
PS C:\iverilog\bin> iverilog orgate_test.v
PS C:\iverilog\bin> vvp a.out
0 : b=0 c=1 d=1 out=1
5 : b=0 c=0 d=0 out=0
PS C:\iverilog\bin> iverilog notgate_test.v
PS C:\iverilog\bin> vvp a.out
0 : a=0 out=1
5 : a=1 out=0
PS C:\iverilog\bin>
0 0 Connect
Ln 1, Col 1 Spaces: 4 UTF-8 LF Verilog Go Live Go Live Prettier
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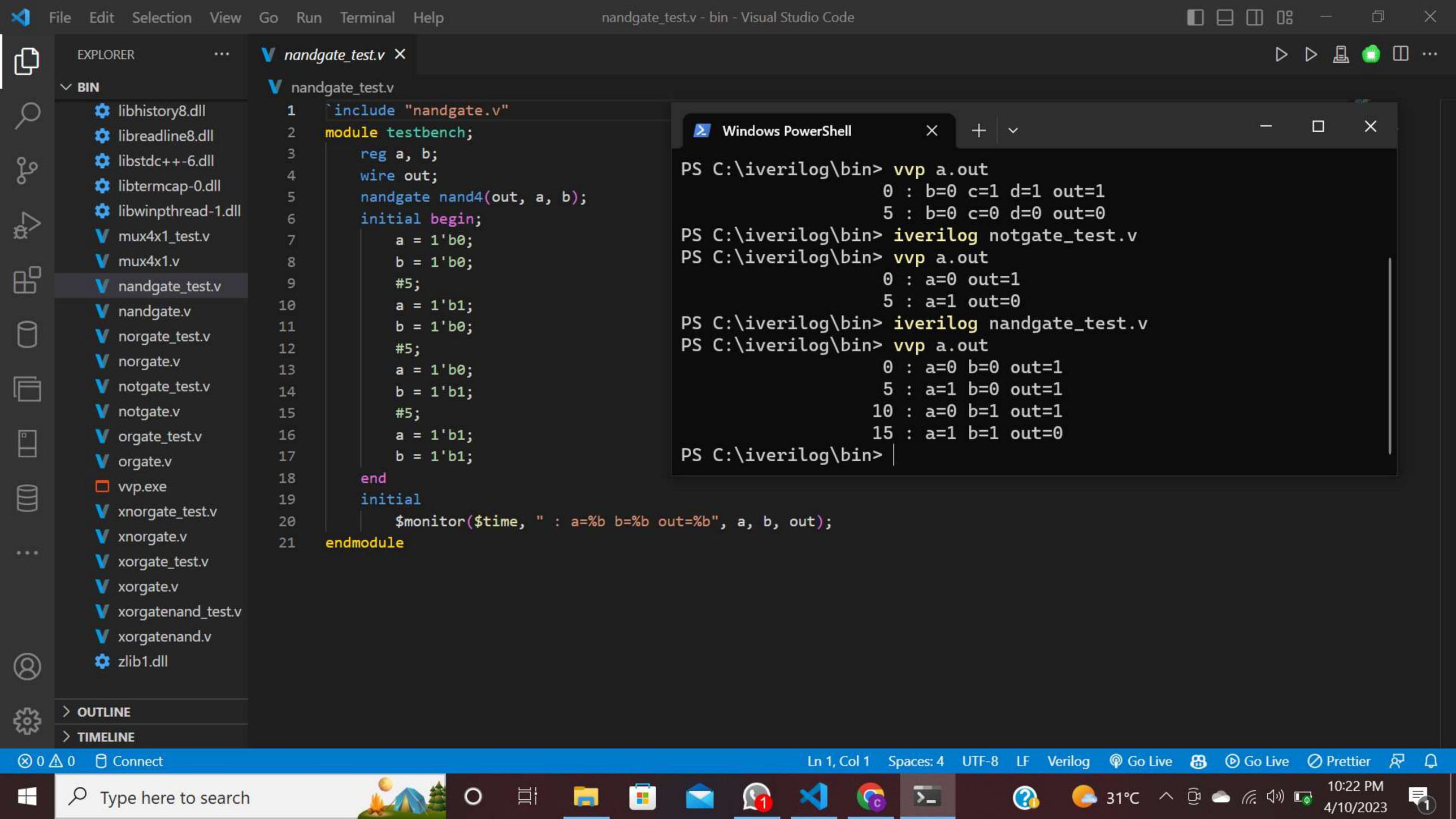
File Edit Selection View Go Run Terminal Help
nandgate_test.v - bin - Visual Studio Code
EXPLORER
BIN
libhistory8.dll
libreadline8.dll
libstdc++-6.dll
libtermcap-0.dll
libwinpthread-1.dll
mux4x1_test.v
mux4x1.v
nandgate_test.v
nandgate.v
norgate_test.v
norgate.v
notgate_test.v
notgate.v
orgate_test.v
orgate.v
vvp.exe
xnorgate_test.v
xnorgate.v
xorgate_test.v
xorgate.v
xorgatenand_test.v
xorgatenand.v
zlib1.dll
OUTLINE
TIMELINE
nandgate_test.v
nandgate_test.v
1 `include "nandgate.v"
2 module testbench;
3 reg a, b;
4 wire out;
5 nandgate nand4(out, a, b);
6 initial begin;
7 a = 1'b0;
8 b = 1'b0;
9 #5;
10 a = 1'b1;
11 b = 1'b0;
12 #5;
13 a = 1'b0;
14 b = 1'b1;
15 #5;
16 a = 1'b1;
17 b = 1'b1;
18 end
19 initial
20 $monitor($time, " : a=%b b=%b out=%b", a, b, out);
21 endmodule
Windows PowerShell
PS C:\iverilog\bin> vvp a.out
0 : b=0 c=1 d=1 out=1
5 : b=0 c=0 d=0 out=0
PS C:\iverilog\bin> iverilog notgate_test.v
PS C:\iverilog\bin> vvp a.out
0 : a=0 out=1
5 : a=1 out=0
PS C:\iverilog\bin> iverilog nandgate_test.v
PS C:\iverilog\bin> vvp a.out
0 : a=0 b=0 out=1
5 : a=1 b=0 out=1
10 : a=0 b=1 out=1
15 : a=1 b=1 out=0
PS C:\iverilog\bin>
0 0 Connect
Ln 1, Col 1 Spaces: 4 UTF-8 LF Verilog Go Live Go Live Prettier
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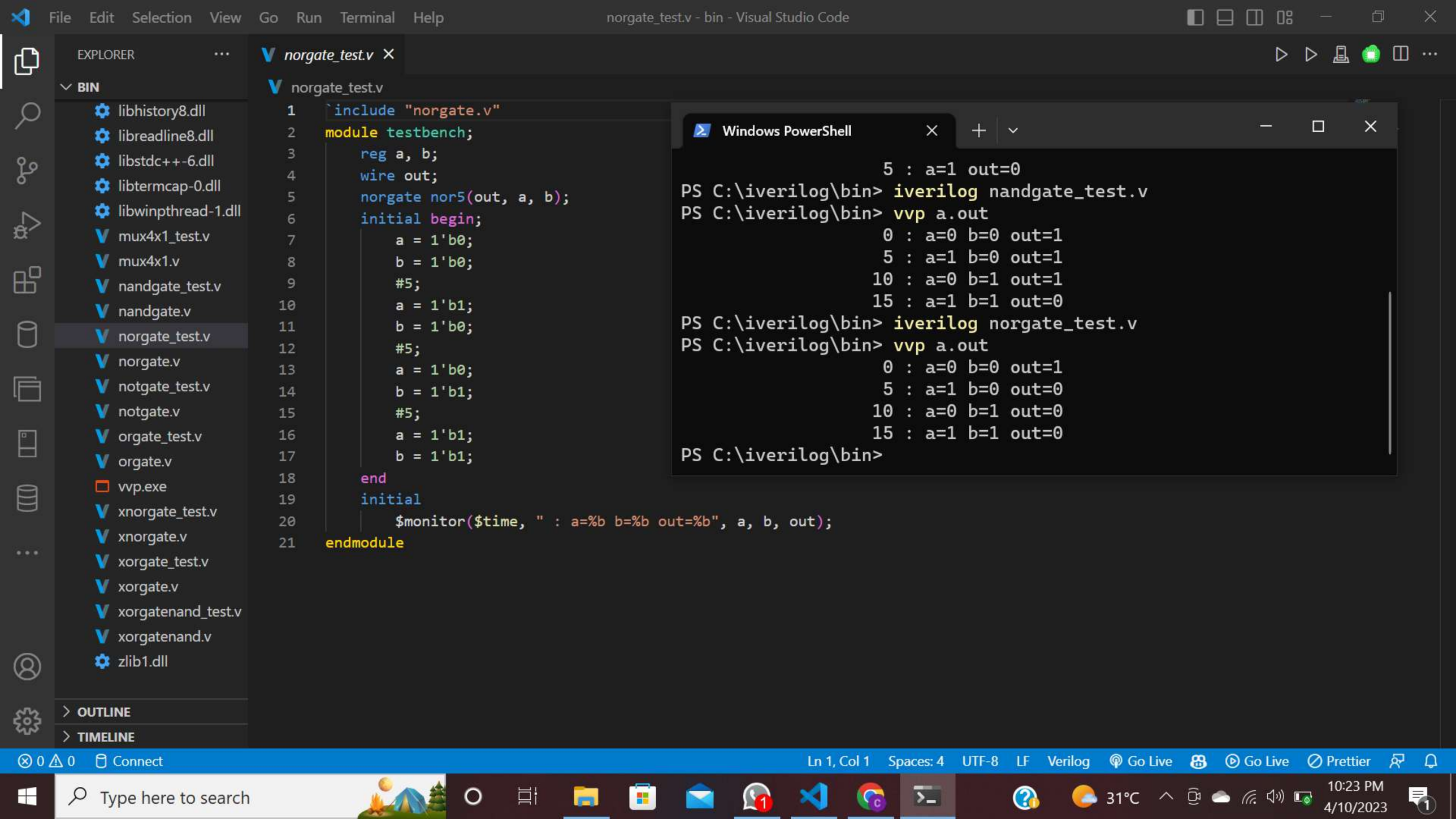
4/10/2023


File Edit Selection View Go Run Terminal Help
norgate_test.v - bin - Visual Studio Code
EXPLORER
BIN
libhistory8.dll
libreadline8.dll
libstdc++-6.dll
libtermcap-0.dll
libwinpthread-1.dll
mux4x1_test.v
mux4x1.v
nandgate_test.v
nandgate.v
norgate_test.v
norgate.v
notgate_test.v
notgate.v
orgate_test.v
orgate.v
vvp.exe
xnorgate_test.v
xnorgate.v
xorgate_test.v
xorgate.v
xorgatenand_test.v
xorgatenand.v
zlib1.dll
OUTLINE
TIMELINE
norgate_test.v
norgate_test.v
1 `include "norgate.v"
2 module testbench;
3 reg a, b;
4 wire out;
5 norgate nor5(out, a, b);
6 initial begin;
7 a = 1'b0;
8 b = 1'b0;
9 #5;
10 a = 1'b1;
11 b = 1'b0;
12 #5;
13 a = 1'b0;
14 b = 1'b1;
15 #5;
16 a = 1'b1;
17 b = 1'b1;
18 end
19 initial
20 $monitor($time, " : a=%b b=%b out=%b", a, b, out);
21 endmodule
Windows PowerShell
5 : a=1 out=0
PS C:\iverilog\bin> iverilog nandgate_test.v
PS C:\iverilog\bin> vvp a.out
0 : a=0 b=0 out=1
5 : a=1 b=0 out=1
10 : a=0 b=1 out=1
15 : a=1 b=1 out=0
PS C:\iverilog\bin> iverilog norgate_test.v
PS C:\iverilog\bin> vvp a.out
0 : a=0 b=0 out=1
5 : a=1 b=0 out=0
10 : a=0 b=1 out=0
15 : a=1 b=1 out=0
PS C:\iverilog\bin>
0 0 Connect
Ln 1, Col 1 Spaces: 4 UTF-8 LF Verilog Go Live Go Live Prettier
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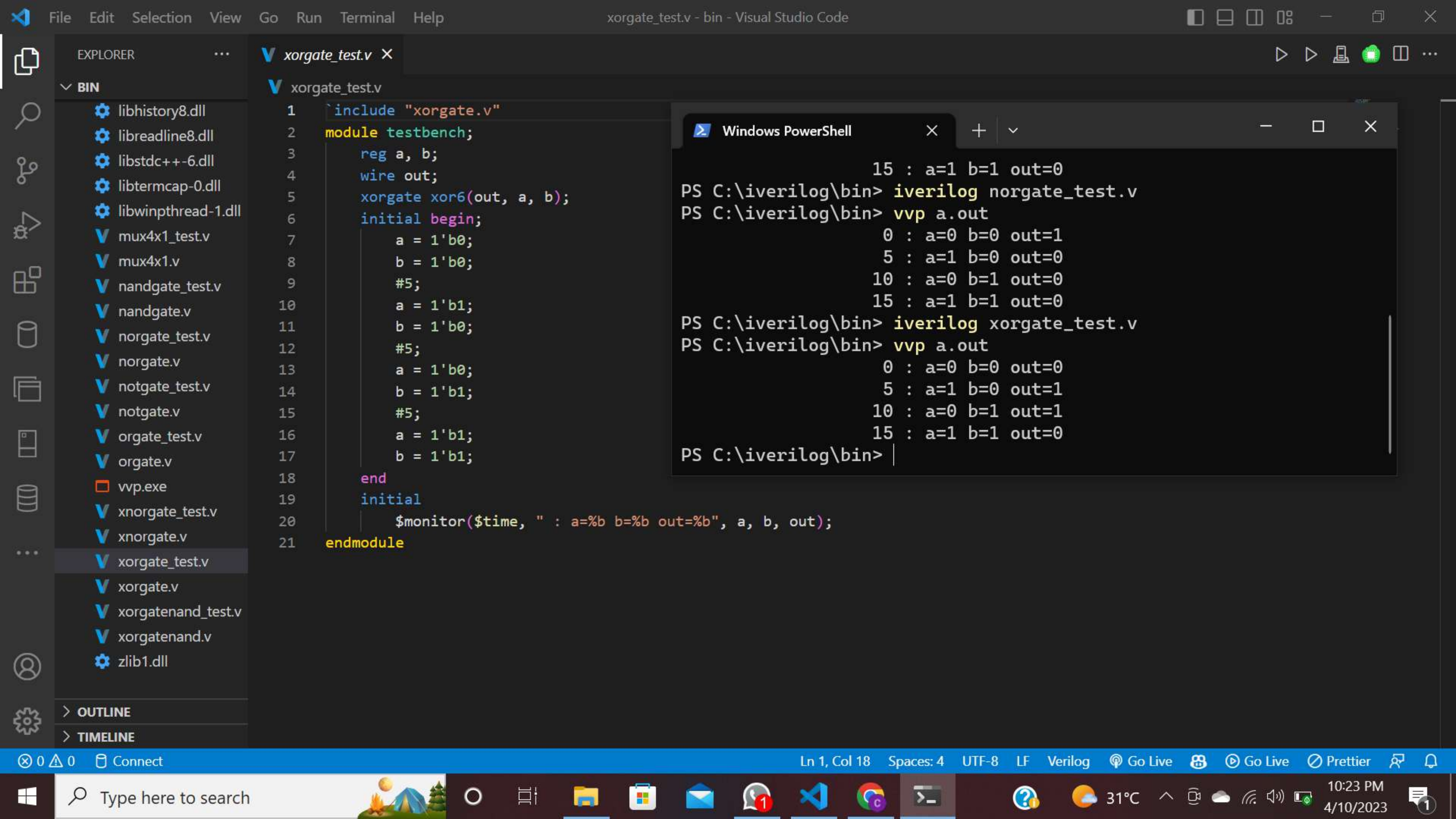
File Edit Selection View Go Run Terminal Help
xorgate_test.v - bin - Visual Studio Code
EXPLORER
BIN
libhistory8.dll
libreadline8.dll
libstdc++-6.dll
libtermcap-0.dll
libwinpthread-1.dll
mux4x1_test.v
mux4x1.v
nandgate_test.v
nandgate.v
norgate_test.v
norgate.v
notgate_test.v
notgate.v
orgate_test.v
orgate.v
vvp.exe
xnorgate_test.v
xnorgate.v
xorgate_test.v
xorgate.v
xorgatenand_test.v
xorgatenand.v
zlib1.dll
OUTLINE
TIMELINE
xorgate_test.v
xorgate_test.v
1 `include "xorgate.v"
2 module testbench;
3 reg a, b;
4 wire out;
5 xorgate xor6(out, a, b);
6 initial begin;
7 a = 1'b0;
8 b = 1'b0;
9 #5;
10 a = 1'b1;
11 b = 1'b0;
12 #5;
13 a = 1'b0;
14 b = 1'b1;
15 #5;
16 a = 1'b1;
17 b = 1'b1;
18 end
19 initial
20 $monitor($time, " : a=%b b=%b out=%b", a, b, out);
21 endmodule
Windows PowerShell
15 : a=1 b=1 out=0
PS C:\iverilog\bin> iverilog norgate_test.v
PS C:\iverilog\bin> vvp a.out
0 : a=0 b=0 out=1
5 : a=1 b=0 out=0
10 : a=0 b=1 out=0
15 : a=1 b=1 out=0
PS C:\iverilog\bin> iverilog xorgate_test.v
PS C:\iverilog\bin> vvp a.out
0 : a=0 b=0 out=0
5 : a=1 b=0 out=1
10 : a=0 b=1 out=1
15 : a=1 b=1 out=0
PS C:\iverilog\bin>
0 0 Connect
Ln 1, Col 18 Spaces: 4 UTF-8 LF Verilog Go Live Go Live Prettier
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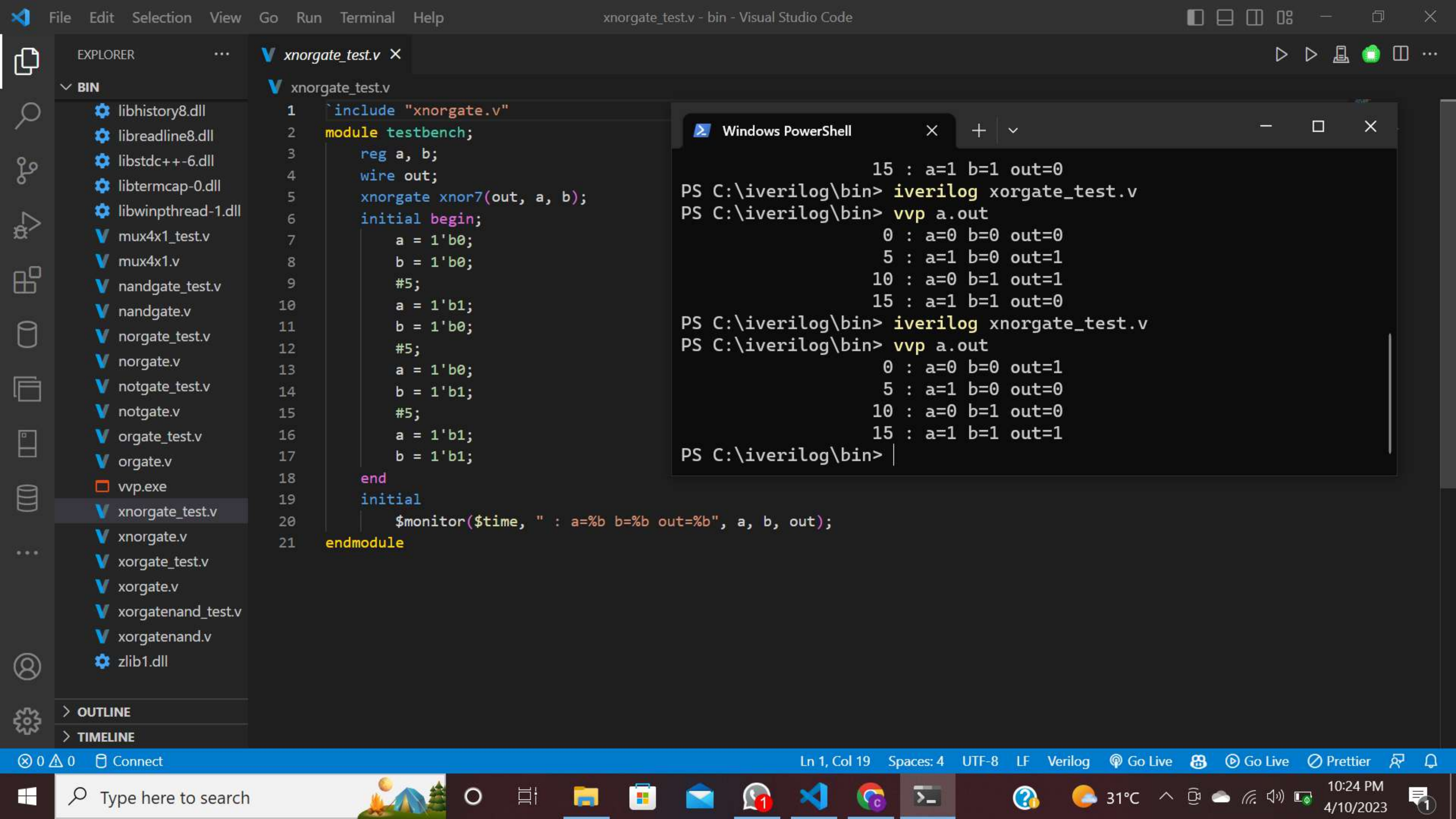
4/10/2023


File Edit Selection View Go Run Terminal Help
xnorgate_test.v - bin - Visual Studio Code
EXPLORER
BIN
libhistory8.dll
libreadline8.dll
libstdc++-6.dll
libtermcap-0.dll
libwinpthread-1.dll
mux4x1_test.v
mux4x1.v
nandgate_test.v
nandgate.v
norgate_test.v
norgate.v
notgate_test.v
notgate.v
orgate_test.v
orgate.v
vvp.exe
xnorgate_test.v
xnorgate.v
xorgate_test.v
xorgate.v
xorgatenand_test.v
xorgatenand.v
zlib1.dll
OUTLINE
TIMELINE
xnorgate_test.v
xnorgate_test.v
1 `include "xnorgate.v"
2 module testbench;
3 reg a, b;
4 wire out;
5 xnorgate xnor7(out, a, b);
6 initial begin;
7 a = 1'b0;
8 b = 1'b0;
9 #5;
10 a = 1'b1;
11 b = 1'b0;
12 #5;
13 a = 1'b0;
14 b = 1'b1;
15 #5;
16 a = 1'b1;
17 b = 1'b1;
18 end
19 initial
20 $monitor($time, " : a=%b b=%b out=%b", a, b, out);
21 endmodule
Windows PowerShell
15 : a=1 b=1 out=0
PS C:\iverilog\bin> iverilog xorgate_test.v
PS C:\iverilog\bin> vvp a.out
0 : a=0 b=0 out=0
5 : a=1 b=0 out=1
10 : a=0 b=1 out=1
15 : a=1 b=1 out=0
PS C:\iverilog\bin> iverilog xnorgate_test.v
PS C:\iverilog\bin> vvp a.out
0 : a=0 b=0 out=1
5 : a=1 b=0 out=0
10 : a=0 b=1 out=0
15 : a=1 b=1 out=1
PS C:\iverilog\bin>
0 0 Connect
Ln 1, Col 19 Spaces: 4 UTF-8 LF Verilog Go Live Go Live Prettier
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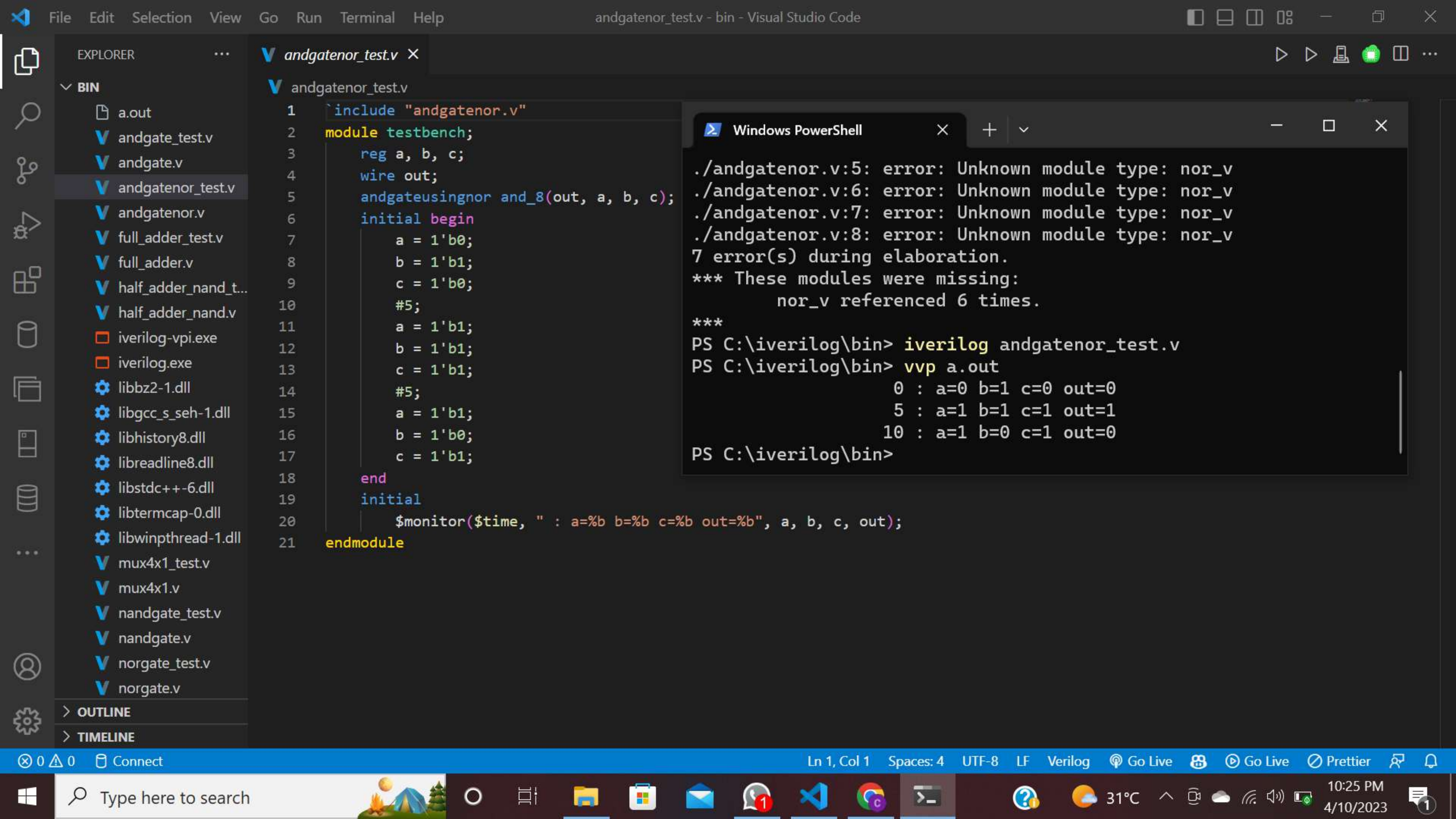
4/10/2023


File Edit Selection View Go Run Terminal Help
andgatenor_test.v - bin - Visual Studio Code
EXPLORER
BIN
a.out
andgate_test.v
andgate.v
andgatenor_test.v
andgatenor.v
full_adder_test.v
full_adder.v
half_adder_nand_t...
half_adder_nand.v
iverilog-vpi.exe
iverilog.exe
libbz2-1.dll
libgcc_s_seh-1.dll
libhistory8.dll
libreadline8.dll
libstdc++-6.dll
libtermcap-0.dll
libwinpthread-1.dll
mux4x1_test.v
mux4x1.v
nandgate_test.v
nandgate.v
norgate_test.v
norgate.v
OUTLINE
TIMELINE
andgatenor_test.v
andgatenor_test.v
1 `include "andgatenor.v"
2 module testbench;
3 reg a, b, c;
4 wire out;
5 andgateusingnor and_8(out, a, b, c);
6 initial begin
7 a = 1'b0;
8 b = 1'b1;
9 c = 1'b0;
10 #5;
11 a = 1'b1;
12 b = 1'b1;
13 c = 1'b1;
14 #5;
15 a = 1'b1;
16 b = 1'b0;
17 c = 1'b1;
18 end
19 initial
20 $monitor($time, " : a=%b b=%b c=%b out=%b", a, b, c, out);
21 endmodule
Windows PowerShell
./andgatenor.v:5: error: Unknown module type: nor_v
./andgatenor.v:6: error: Unknown module type: nor_v
./andgatenor.v:7: error: Unknown module type: nor_v
./andgatenor.v:8: error: Unknown module type: nor_v
7 error(s) during elaboration.
*** These modules were missing:
nor_v referenced 6 times.
***
PS C:\iverilog\bin> iverilog andgatenor_test.v
PS C:\iverilog\bin> vvp a.out
0 : a=0 b=1 c=0 out=0
5 : a=1 b=1 c=1 out=1
10 : a=1 b=0 c=1 out=0
PS C:\iverilog\bin>
0 0 Connect
Ln 1, Col 1 Spaces: 4 UTF-8 LF Verilog Go Live Go Live Prettier
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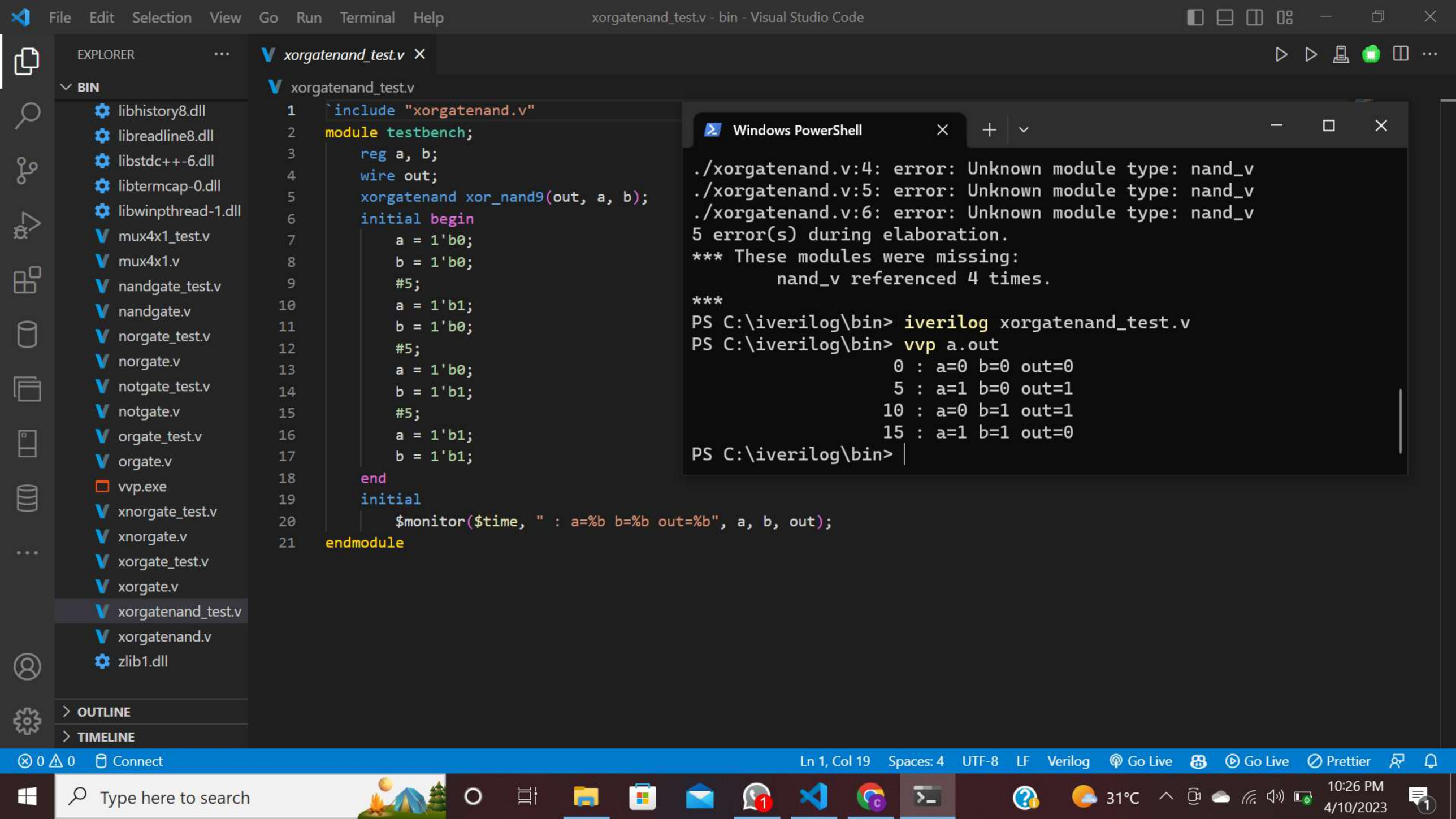
4/10/2023


File Edit Selection View Go Run Terminal Help
xorgatenand_test.v - bin - Visual Studio Code
EXPLORER
BIN
libhistory8.dll
libreadline8.dll
libstdc++-6.dll
libtermcap-0.dll
libwinpthread-1.dll
mux4x1_test.v
mux4x1.v
nandgate_test.v
nandgate.v
norgate_test.v
norgate.v
notgate_test.v
notgate.v
orgate_test.v
orgate.v
vvp.exe
xnorgate_test.v
xnorgate.v
xorgate_test.v
xorgate.v
xorgatenand_test.v
xorgatenand.v
zlib1.dll
OUTLINE
TIMELINE
xorgatenand_test.v
xorgatenand_test.v
1 `include "xorgatenand.v"
2 module testbench;
3 reg a, b;
4 wire out;
5 xorgatenand xor_nand9(out, a, b);
6 initial begin
7 a = 1'b0;
8 b = 1'b0;
9 #5;
10 a = 1'b1;
11 b = 1'b0;
12 #5;
13 a = 1'b0;
14 b = 1'b1;
15 #5;
16 a = 1'b1;
17 b = 1'b1;
18 end
19 initial
20 $monitor($time, " : a=%b b=%b out=%b", a, b, out);
21 endmodule
Windows PowerShell
./xorgatenand.v:4: error: Unknown module type: nand_v
./xorgatenand.v:5: error: Unknown module type: nand_v
./xorgatenand.v:6: error: Unknown module type: nand_v
5 error(s) during elaboration.
*** These modules were missing:
nand_v referenced 4 times.
***
PS C:\iverilog\bin> iverilog xorgatenand_test.v
PS C:\iverilog\bin> vvp a.out
0 : a=0 b=0 out=0
5 : a=1 b=0 out=1
10 : a=0 b=1 out=1
15 : a=1 b=1 out=0
PS C:\iverilog\bin>
0 0 Connect
Ln 1, Col 19 Spaces: 4 UTF-8 LF Verilog Go Live Go Live Prettier
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4/10/2023

File Edit Selection View Go Run Terminal Help half_adder_nand.v - bin - Visual Studio Code

EXPLORER

BIN

- a.out
- andgate_test.v
- andgate.v
- andgatenor_test.v
- andgatenor.v
- full_adder_test.v
- full_adder.v
- half_adder_nand_t...
- half_adder_nand.v
- iverilog-vpi.exe
- iverilog.exe
- libbz2-1.dll
- libgcc_s_seh-1.dll
- libhistory8.dll
- libreadline8.dll
- libstdc++-6.dll
- libtermcap-0.dll
- libwinpthread-1.dll
- mux4x1_test.v
- mux4x1.v
- nandgate_test.v
- nandgate.v
- norgate_test.v
- norgate.v

OUTLINE

TIMELINE

half_adder_nand.v

half_adder_nand.v

```verilog
module half_adder_nand(output sum, output carry,input a, input b);
    wire w1;
    xorgatenand xor1(sum, a, b);
    nandgate nand1(w1, a, b);
    nandgate nand2(carry, w1, w1);
endmodule

module xorgatenand(output out, input a, input b);
    wire w1, w2, w3;
    nandgate nand1(w1, a, b);
    nandgate nand2(w2, a, w1);
    nandgate nand3(w3, b, w1);
    nandgate nand4(out, w2, w3);
endmodule

module nandgate (output out, input a, input b);
    wire w1;
    and (w1, a, b);
    not (out, w1);
endmodule
```

Windows PowerShell

```
                  10 : a=0 b=1 sum=1 carry=0
                  15 : a=1 b=1 sum=0 carry=1
PS C:\iverilog\bin> vvp a.out
                   0 : a=0 b=0 sum=0 carry=0
                   5 : a=1 b=0 sum=1 carry=0
                  10 : a=0 b=1 sum=1 carry=0
                  15 : a=1 b=1 sum=0 carry=1
PS C:\iverilog\bin> iverilog half_adder_nand_test.v
PS C:\iverilog\bin> vvp a.out
                   0 : a=0 b=0 sum=0 carry=0
                   5 : a=1 b=0 sum=1 carry=0
                  10 : a=0 b=1 sum=1 carry=0
                  15 : a=1 b=1 sum=0 carry=1
PS C:\iverilog\bin>
```

0 0 Connect Ln 13, Col 29 Spaces: 4 UTF-8 LF Verilog Go Live Go Live Prettier

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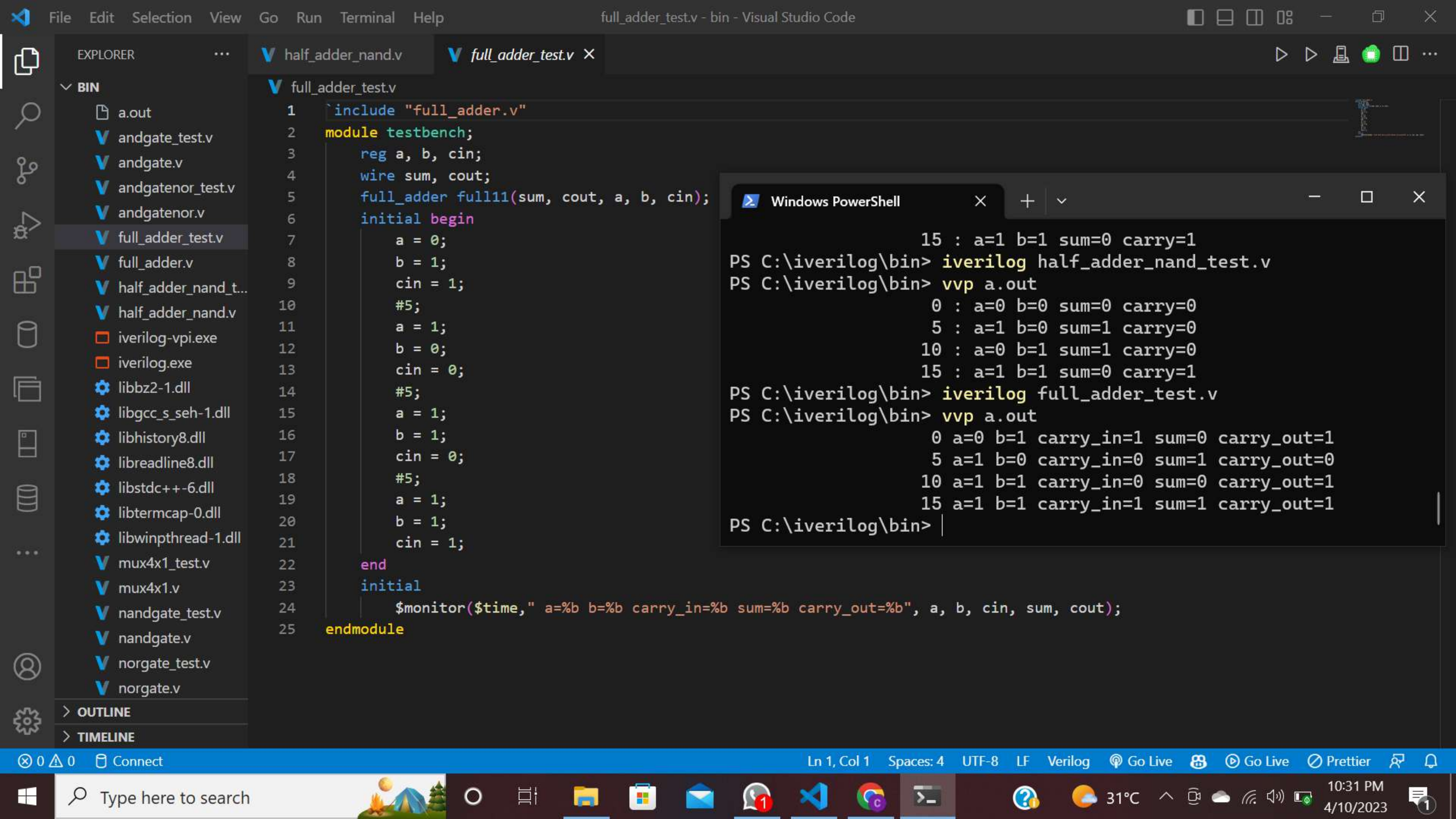
File Edit Selection View Go Run Terminal Help
full_adder_test.v - bin - Visual Studio Code
EXPLORER
BIN
a.out
andgate_test.v
andgate.v
andgatenor_test.v
andgatenor.v
full_adder_test.v
full_adder.v
half_adder_nand_t...
half_adder_nand.v
iverilog-vpi.exe
iverilog.exe
libbz2-1.dll
libgcc_s_seh-1.dll
libhistory8.dll
libreadline8.dll
libstdc++-6.dll
libtermcap-0.dll
libwinpthread-1.dll
mux4x1_test.v
mux4x1.v
nandgate_test.v
nandgate.v
norgate_test.v
norgate.v
OUTLINE
TIMELINE
half_adder_nand.v
full_adder_test.v
full_adder_test.v
1 `include "full_adder.v"
2 module testbench;
3 reg a, b, cin;
4 wire sum, cout;
5 full_adder full11(sum, cout, a, b, cin);
6 initial begin
7 a = 0;
8 b = 1;
9 cin = 1;
10 #5;
11 a = 1;
12 b = 0;
13 cin = 0;
14 #5;
15 a = 1;
16 b = 1;
17 cin = 0;
18 #5;
19 a = 1;
20 b = 1;
21 cin = 1;
22 end
23 initial
24 $monitor($time," a=%b b=%b carry_in=%b sum=%b carry_out=%b", a, b, cin, sum, cout);
25 endmodule
Windows PowerShell
15 : a=1 b=1 sum=0 carry=1
PS C:\iverilog\bin> iverilog half_adder_nand_test.v
PS C:\iverilog\bin> vvp a.out
0 : a=0 b=0 sum=0 carry=0
5 : a=1 b=0 sum=1 carry=0
10 : a=0 b=1 sum=1 carry=0
15 : a=1 b=1 sum=0 carry=1
PS C:\iverilog\bin> iverilog full_adder_test.v
PS C:\iverilog\bin> vvp a.out
0 a=0 b=1 carry_in=1 sum=0 carry_out=1
5 a=1 b=0 carry_in=0 sum=1 carry_out=0
10 a=1 b=1 carry_in=0 sum=0 carry_out=1
15 a=1 b=1 carry_in=1 sum=1 carry_out=1
PS C:\iverilog\bin>
0 0 Connect
Ln 1, Col 1 Spaces: 4 UTF-8 LF Verilog Go Live Go Live Prettier
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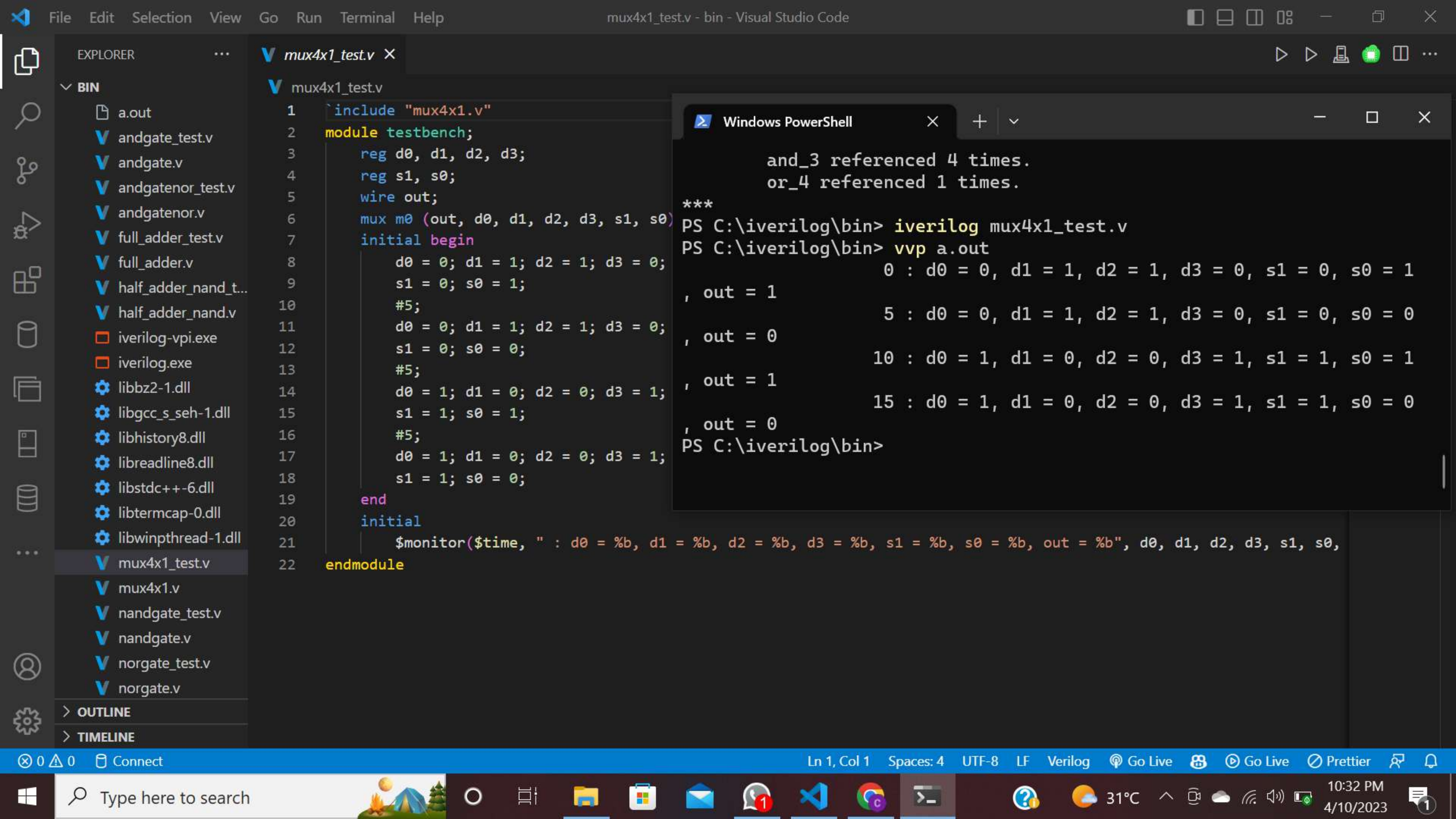
4/10/2023


File Edit Selection View Go Run Terminal Help
mux4x1_test.v - bin - Visual Studio Code
EXPLORER
BIN
a.out
andgate_test.v
andgate.v
andgatenor_test.v
andgatenor.v
full_adder_test.v
full_adder.v
half_adder_nand_t...
half_adder_nand.v
iverilog-vpi.exe
iverilog.exe
libbz2-1.dll
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libhistory8.dll
libreadline8.dll
libstdc++-6.dll
libtermcap-0.dll
libwinpthread-1.dll
mux4x1_test.v
mux4x1.v
nandgate_test.v
nandgate.v
norgate_test.v
norgate.v
OUTLINE
TIMELINE
mux4x1_test.v
mux4x1_test.v
1 `include "mux4x1.v"
2 module testbench;
3 reg d0, d1, d2, d3;
4 reg s1, s0;
5 wire out;
6 mux m0 (out, d0, d1, d2, d3, s1, s0);
7 initial begin
8 d0 = 0; d1 = 1; d2 = 1; d3 = 0;
9 s1 = 0; s0 = 1;
10 #5;
11 d0 = 0; d1 = 1; d2 = 1; d3 = 0;
12 s1 = 0; s0 = 0;
13 #5;
14 d0 = 1; d1 = 0; d2 = 0; d3 = 1;
15 s1 = 1; s0 = 1;
16 #5;
17 d0 = 1; d1 = 0; d2 = 0; d3 = 1;
18 s1 = 1; s0 = 0;
19 end
20 initial
21 $monitor($time, " : d0 = %b, d1 = %b, d2 = %b, d3 = %b, s1 = %b, s0 = %b, out = %b", d0, d1, d2, d3, s1, s0,
22 endmodule
Windows PowerShell
and_3 referenced 4 times.
or_4 referenced 1 times.
***
PS C:\iverilog\bin> iverilog mux4x1_test.v
PS C:\iverilog\bin> vvp a.out
0 : d0 = 0, d1 = 1, d2 = 1, d3 = 0, s1 = 0, s0 = 1
, out = 1
5 : d0 = 0, d1 = 1, d2 = 1, d3 = 0, s1 = 0, s0 = 0
, out = 0
10 : d0 = 1, d1 = 0, d2 = 0, d3 = 1, s1 = 1, s0 = 1
, out = 1
15 : d0 = 1, d1 = 0, d2 = 0, d3 = 1, s1 = 1, s0 = 0
, out = 0
PS C:\iverilog\bin>
0 0 Connect
Ln 1, Col 1 Spaces: 4 UTF-8 LF Verilog Go Live Go Live Prettier
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31°C
10:32 PM
4/10/2023