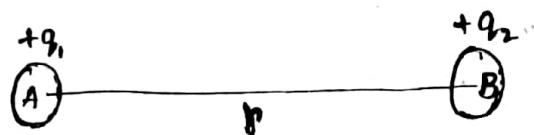


* Coulomb's law of force between electric charges:

The force between two electric charges is directly proportional to the product of their charges and inversely proportional to the square root of the distance between them.

The second part of the law is known as inverse square law.

Statement: The force between the two charges is inversely proportional to the square of the distance between them.



Explanation: Let q_1 and q_2 be the two charges separated by a distance r . The force F between them is given by

$$\left. \begin{aligned} F &\propto q_1 q_2 \\ F &\propto 1/r^2 \end{aligned} \right\} \text{i.e., } F \propto \frac{q_1 q_2}{r^2}$$

$$F = \frac{1}{K} \frac{q_1 q_2}{r^2}$$

Where K is a constant depending upon the nature of the medium between the charges and is known as the dielectric constant or specific inductive capacity or permittivity of the medium.

The M.K.S unit of charge is coulomb.

In the Internationalized M.K.S system or S.I System,

$$\frac{1}{K} = \frac{1}{4\pi\epsilon_0\epsilon_r}$$

Where ϵ_0 is the permittivity of the free space

and ϵ_r is the relative permittivity of the medium.

Hence the force F between the charges is given by

$$F = \frac{q_1 q_2}{4\pi \epsilon_0 r^2}$$

In rationalised M.K.S system, F is Newton's, r is in metres and $\frac{1}{4\pi \epsilon_0} = 9 \times 10^9 \frac{\text{Newton-meter}^2}{\text{coulomb}^2}$

$$\text{and } \epsilon_0 = 8.85 \times 10^{-12} \text{ coulomb}^2/\text{n-m}^2$$

When the two charges are in free space, ϵ_r of free space = 1.

Then

$$F = \frac{q_1 q_2}{4\pi \epsilon_0 r^2}$$

Let $q_1 = q_2 = 1$ coulomb; $r = 1$ metre and $1/4\pi \epsilon_0 = 9 \times 10^9$ then

$$F = \frac{1 \times 1 \times 9 \times 10^9}{1^2} = 9 \times 10^9 \text{ newtons.}$$

Def: coulomb is that much charge which when placed at a distance of 1 metre in air from a similar and equal charges repels it with a force of 9×10^9 newtons.

Rationalised M.K.S unit of charge is 1 coulomb.

The charge of an electron (e) is given by

$$e = 1.60 \times 10^{-19} \text{ coulomb}$$

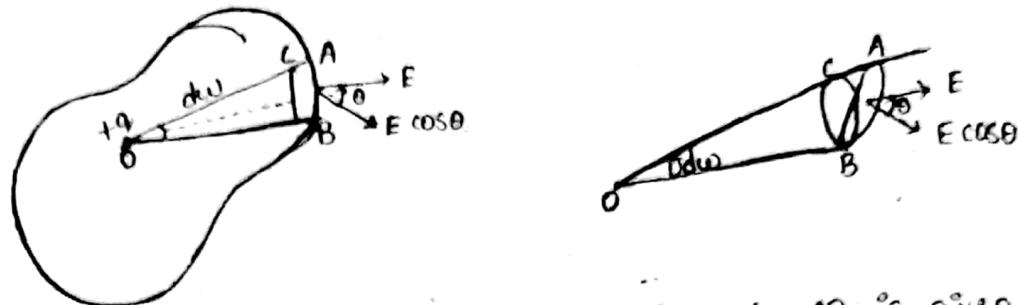
Scope of coulomb's law: coulomb's law is true over a wide range from 10^{-5} m , to many kilometers.

(a) State and explain Gauss theorem. Apply it to find the electric intensity due to a uniformly charged sphere at a point (i) outside (ii) on the surface and (iii) inside the sphere.

A: Gauss Theorem: The total normal electric induction for electric flux over any closed surface is equal to $1/\epsilon_0$ times the total charge enclosed by the surface.



Proof: Consider a closed surface with a charge $+q$ at the point 'O'. Imagine a small element of area AB ($= ds$) at a distance 'r' from the charge.



The electric intensity E at the element AB is given by

$$E = \frac{q}{4\pi\epsilon_0 r^2}$$

Let θ be the angle between the direction of electric field and the normal to the surface at ds .

$$\therefore \text{Component of } E \left. \begin{array}{l} \\ \text{towards the surface} \end{array} \right\} = E \cos\theta$$

$$\text{Hence electric flux through } \left. \begin{array}{l} \\ \text{the area } ds \end{array} \right\} = E \cos\theta ds$$

$$\therefore \text{Total electric flux through } \left. \begin{array}{l} \\ \text{entire closed surface} \end{array} \right\} = \oint E \cos\theta ds$$

$$= \frac{q}{4\pi\epsilon_0} \oint \frac{ds \cos\theta}{r^2}$$

But $ds \cos\theta/r^2$ is the solid angle $d\omega$ subtended by the surface ds at the point 'O' where the charge q is present.

$$\therefore \text{Total electric flux through } \left. \begin{array}{l} \\ \text{the entire closed surface} \end{array} \right\} = \frac{q}{4\pi\epsilon_0} \oint d\omega$$

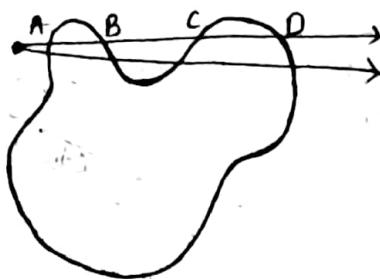
Inspite of the shape of the volume involved, the integration over the entire closed surface gives 4π .

$$\text{Hence total electric flux through } \left. \begin{array}{l} \\ \text{the entire closed surface} \end{array} \right\} = \frac{q}{4\pi\epsilon_0} 4\pi = \frac{q}{\epsilon_0}$$

Case (ii): This proof can be extended to any number of point charges contained in the closed surface by treating each point charge separately.

$$\therefore \text{Total electric flux } \Phi = \frac{\sum q}{\epsilon_0}$$

Case (ii): If the charge q is outside the surface, draw a small cone from the charge cutting the closed surface at A, B, C and D. Then



$$\text{Electric flux at A (inwards)} = -\frac{1}{4\pi\epsilon_0} q \, d\omega$$

$$\text{Electric flux at B (outwards)} = +\frac{1}{4\pi\epsilon_0} q \, d\omega$$

$$\text{Electric flux at C (inwards)} = -\frac{1}{4\pi\epsilon_0} q \, d\omega$$

$$\text{Electric flux at D (outwards)} = +\frac{1}{4\pi\epsilon_0} q \, d\omega$$

$$\therefore \text{Total electric flux through the entire closed surface} = \frac{1}{4\pi\epsilon_0} \sum q \, d\omega = 0.$$

Electric intensity due to a uniformly charged sphere:

(i) When the point is outside the sphere:

Let a charge $+q$ be uniformly distributed over a sphere of radius R . P is a point outside the sphere at a distance r from the centre O. Imagine a concentric sphere to be described with 'O' as centre and OA ($=r$) as radius. Let E be the electric intensity at P. As the surface of the sphere is an equipotential surface, the electric intensity E at any point on the imaginary sphere is the same.

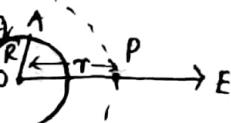
$$\therefore \text{Total electric flux through the entire closed surface} = E \times \text{Area}$$

$$= E \times 4\pi r^2$$

By Gauss theorem,

$$\text{Total electric flux through the entire surface} = \frac{q}{\epsilon_0}$$

$$\therefore 4\pi r^2 E = \frac{q}{\epsilon_0}$$



$$\text{or } E = \frac{q}{4\pi\epsilon_0 r^2}$$

thus the electric intensity at any external point due to a uniformly charged sphere is the same as if the charge is concentrated at its centre.

(ii) When the point is on the sphere: In this case $r=R$.

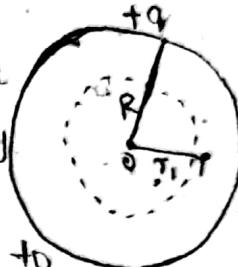
$$E = \frac{q}{4\pi\epsilon_0 R^2} \dots$$

(iii) When the point is inside the sphere:

Let P be a point inside the sphere at a distance r_1 from 'O' where the intensity of the electric field E is to be determined. Imagine a concentric sphere to be described with 'O' as centre and $OP = r_1$ as radius.

Let σ be the charge density. Then

$$\sigma = \frac{\text{charge}}{\text{volume}} = \frac{q}{(4/3)\pi r^3}$$



The sphere can be imagined to be made up of concentric spherical shells. The electric intensity at P is due to the combined effect of the shells outside and inside P.

But the electric intensity due to the outer spherical shell is zero.

The electric intensity due to the inside shells is obtained though the charge were concentrated at the centre.

$$\text{charge in the sphere of radius } r_1 = \frac{4}{3}\pi r_1^3 \sigma$$

$$\therefore E = \frac{(4/3)\pi r_1^3 \sigma}{4\pi\epsilon_0 r_1^2} = \frac{r_1 \sigma}{3\epsilon_0}$$

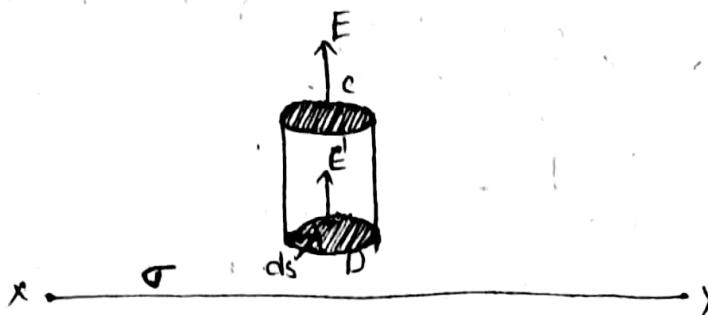
$$\text{i.e., } E \propto r_1$$

Thus, the electric intensity falls from maximum to zero as we go from the surface to the centre.

Q) Apply Gauss theorem to find electric intensity due to an infinite uniform plane sheet of charge.
 Find the intensity of electric field strength near a charged conductor and also determine the mechanical force per unit area of charged conductor.

A: Electric intensity - infinite plane sheet of charge:

xy is a part of the plane charged sheet whose surface density is σ . Near the plane consider two points C and D, where the values of electric density are E and E' respectively. Imagine a cylinder CD to be drawn with plane faces of area ds parallel to xy. As the charged surface is infinite, the electric intensity every where is normal to the surface xy.



The total electric flux through the curved surface of CD is zero, as the sides are parallel to the direction of the electric field.

$$\therefore \text{Total electric flux through the } \left. \begin{array}{l} \text{entire closed surface } CD \\ \text{entire closed surface } CD \end{array} \right\} = E ds - E' ds$$

The -ve sign is due to the fact that the electric intensity E at D is along the inward drawn normal.

By Gauss theorem,

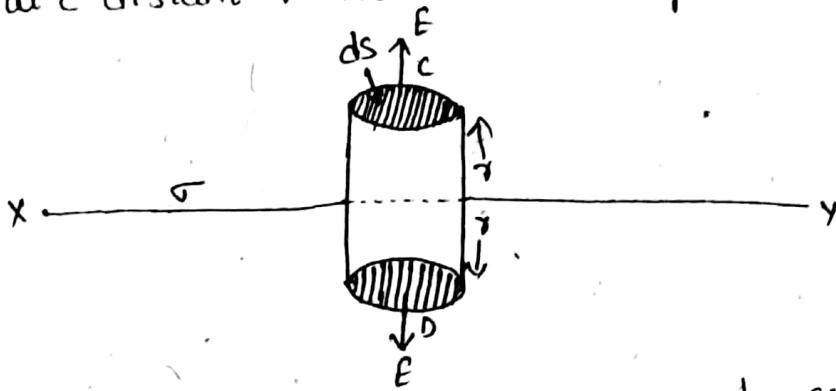
$$\text{total electric flux through the } \left. \begin{array}{l} \text{entire closed surface } CD \\ \text{entire closed surface } CD \end{array} \right\} = \frac{1}{\epsilon_0} \times 0 = 0$$

$$\therefore E ds - E' ds = 0 \quad \text{or} \quad E = E'$$

This shows that the electric intensity at any point near a charged infinite plane is the same.

Calculation of E - the electric intensity:

XY is a part of an infinite charged sheet of surface density σ . It is required to determine the electric intensity E at c distant r from the charged sheet.



through c draw a cylinder of sectional area ds with its sides perpendicular and the ends parallel to the charged surface. Imagine the cylinder to extend by an amount r to the other side of the conductor. The electric flux passes through the top and bottom plane surface only and through the curved surface it is zero.

$$\therefore \text{Total electric flux through the entire closed surface } CD = E ds + E' ds = 2E ds$$

By Gauss theorem,

$$\text{Total electric flux through the entire closed surface } CD = \frac{\sigma ds}{\epsilon_0}$$

$$\text{Hence } 2E ds = \frac{\sigma ds}{\epsilon_0} \quad \text{or. } E = \frac{\sigma}{2\epsilon_0}$$

This also shows that the electric intensity at any point near a charged infinite sheet is the same and is independent of the distance of the point from XY.

Explain electric potential with calculate the potential equation?

Electric potential:

The electric potential is the amount of work energy needed to move a unit of electric charge from a reference point to the specific point in an electric field.

$$E.P = V = \frac{W}{q}$$

S.I units = Volts.

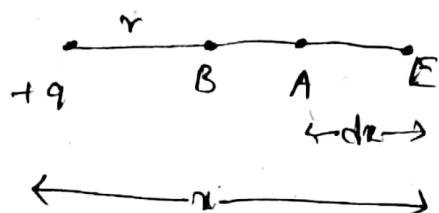
Equation:

x = distance at B point the electric intensity is given by

$$E = \frac{1}{4\pi\epsilon_0} \frac{q}{r^2}$$

Now E to A point distance dx

Potential given by



$$E = -V$$

$$dV = -Edx$$

$$dV = \frac{1}{4\pi\epsilon_0} \frac{q}{r^2} dx$$

at ∞ distance at point P the potential given by

$$\text{potential } \int dV = \int_{\infty}^{r_1} -\frac{q}{4\pi\epsilon_0} \cdot \frac{dx}{r^2}$$

$$\begin{aligned} V &= \frac{-q}{4\pi\epsilon_0} \int_{\infty}^{r_1} \frac{1}{r^2} dr \\ &= \frac{-q}{4\pi\epsilon_0} \left(-\frac{1}{r} \right)_{\infty}^{r_1} \end{aligned}$$

Now potential

$$V = \frac{q}{4\pi\epsilon_0} \left(\frac{1}{r_1} \right)$$

(Q) obtain the relation between D, E and P.

* Electric field intensity:

The electric field intensity at point is the force experienced by unit positive charge placed at that point.

* Electric field intensity is a vector quantity if it is denoted by 'E'

$$E = \frac{F}{q}$$

Electric Displacement:

The displacement D is proportional to an external electric field E in which the dielectric is placed.

(or)

The magnitude of vector D is equal to the free surface charge density.

$$D = \epsilon_0 E + P$$

ϵ_0 = permittivity of free space.

P = polarisation.

E = external electric field.

Electric polarisation:

The electric polarisation refers to the separation of centre of positive charge and the centre of negative charge in a material.

The separation can be caused by a sufficiently high electric field. This is a vector.

$$\oint E \cdot dS = \frac{q}{\epsilon_0}$$

$$\oint \epsilon_0 E \cdot dS = q$$

$$\oint D \cdot dS = q$$

$$D \oint ds = q$$

$$D = \frac{q}{A}$$

* capacitor final electric intensity

$$E = E_0 - E_1.$$

by using Gauss law

$$\Rightarrow \frac{q}{K\epsilon_0 A} = \frac{q}{\epsilon_0 A} = \frac{q'}{\epsilon_0 A}$$

$$\frac{q}{\epsilon_0 A} = \frac{q}{K\epsilon_0 A} + \frac{q'}{\epsilon_0 A}$$

$$\frac{q}{A} = \epsilon_0 \left(\frac{q}{K\epsilon_0 A} \right) + \frac{q'}{A}$$

$$\frac{q}{A} = E_0 (E) + \bar{P}$$

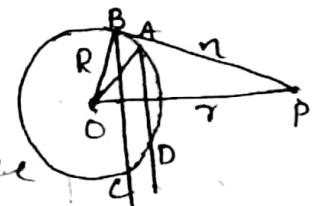
$$\bar{D} = \epsilon_0 \bar{E} + \bar{P}$$

a) calculate the potential due to a charged spherical conductor.

b) Equipotential surface:

An equipotential surface is a surface drawn through all the points at the same potential in an electric field.

The surface of charged conductor is an example of an equipotential surface. Around a point charge, concentric spheres are drawn on equipotential surfaces.



Case (ii): potential at point due to a charged spherical shell:

At a point 'P' outside the shell:

- * P is a point outside the spherical shell of radius R at a distance 'r'.
- * from the centre 'O'.
- * let σ be the surface density of charge.
- * Join OP drawn two planes very closed to each other and perpendicular to OP, cutting the shell AB and BC.

Now the relation between V & E

$$E = -dv$$

$$dv = -Ed\sigma \quad \text{--- (1)}$$

but at 'P' point :

$$E = \frac{1}{4\pi\epsilon_0} \frac{q}{\sigma^2} \quad \text{--- (2)}$$

from (1) & (2)

$$dv = \frac{1}{4\pi\epsilon_0} \frac{q}{\sigma^2} d\sigma \quad \text{--- (3)}$$

- * The potential V at P due to the whole shell is obtained by eq (3) between the limits ∞ to σ_1 .

$$\int dv = \int_{\infty}^{\sigma_1} \frac{1}{4\pi\epsilon_0} \cdot -\frac{q}{\sigma^2} d\sigma$$

$$= -\frac{q}{4\pi\epsilon_0} \cdot \int_{\infty}^{\sigma_1} \frac{1}{\sigma^2} d\sigma$$

$$= \frac{+q}{4\pi\epsilon_0} \cdot -\frac{1}{\sigma_1}$$

$$V = \frac{1}{4\pi\epsilon_0} \cdot \frac{q}{\sigma_1}$$

- * The electric potential at a point outside a charged spherical shell is the same, as if the charge on the shell is concentrated at the center.

At a point p on the shell :

In this case $r = R$

$$\therefore V = \frac{1}{4\pi\epsilon_0} \frac{q}{R}$$

At a point 'p' inside the shell :

In case, the limits of integration are a to R and R to ∞ .

The relation between E & V .

$$dV = -E dr \quad \text{--- (1)}$$

by using Gauss law

$$E = \frac{1}{4\pi\epsilon_0} \frac{q}{r^2} \quad \text{--- (2)}$$

from (1) & (2)

$$dV = -\frac{1}{4\pi\epsilon_0} \cdot \frac{q}{r^2} dr$$

Integration both sides by using limits

$$\int dV = \int_{\infty}^R -\frac{1}{4\pi\epsilon_0} \frac{q}{r^2} dr + \int_R^{\infty} -\frac{1}{4\pi\epsilon_0} \frac{q}{r^2} dr$$

$$= \frac{q}{4\pi\epsilon_0} \left[\frac{1}{R} \right] - \frac{q}{4\pi\epsilon_0} \left[\frac{1}{r} - \frac{1}{R} \right]$$

$$= \frac{q}{4\pi\epsilon_0} \left(\frac{1}{R} + \frac{1}{r} - \frac{1}{R} \right)$$

$$V = \frac{q}{4\pi\epsilon_0} \left(\frac{1}{r}\right).$$

* thus the potential at any point inside a charge spherical shell is equal to the potential on the surface.

* state and explain Gauss law in dielectric.
Explain why the introduction of a dielectric between the plates of a capacitor changes its capacitance.

Dielectrics and Gauss law:

The electric flux through any closed surface is equal to $\frac{1}{\epsilon_0}$ times the net charge enclosed by the surface.

* Let us consider a parallel plate capacitor with plate area A and having a vacuum between its plates.

* Let +q and -q be the charges on its plates and E_0 the uniform electric field between the plates.

* Let PQRS be a Gaussian surface

* The electric flux through this surface is $\oint E_0 \cdot d\vec{s}$.

* The net charge enclosed by surface is +q.

\therefore By Gauss law

$$\oint E_0 \cdot d\vec{s} = \frac{q}{\epsilon_0} \quad \text{--- (1)}$$

$$\text{But } E_0 \cdot d\vec{s} = \epsilon_0 \cdot A$$

($d\vec{s}$ = small area
 $\oint d\vec{s} = A$)

from eq (1)

$$\epsilon_0 A = \frac{q}{\epsilon_0}$$

$$\epsilon_0 = \frac{q}{\epsilon_0 A} \quad \text{--- (2)}$$



* Let us now suppose that a dielectric material of dielectric constant k is filled completely between the plates.

(Case ii):

* A negative charge $-q$ is induced on one surface and an equal positive charge $+q$ on the other.

* These induced charges produce their own field which oppose the external field \vec{E}_0 . Let \vec{E} be the resultant field within the dielectric.

The new flux through the Gaussian surface PQRS is

$$\oint \vec{E} \cdot d\vec{s}$$

* Net charge enclosed by the surface is now $(q-q')$ by using Gauss law $\frac{q}{\epsilon_0}$

$$\oint \vec{E} \cdot d\vec{s} = \frac{q-q'}{\epsilon_0} \quad \text{--- (2)}$$

$$[\oint d\vec{s} = A]$$

$$E \cdot A = \frac{q-q'}{\epsilon_0}$$

$$E = \frac{q-q'}{\epsilon_0 A} \quad \text{--- (3)}$$

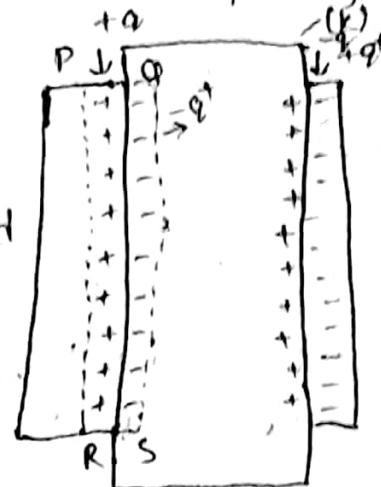
$\epsilon_0 / \epsilon = k$, ' k ' is dielectric constant.

combining this with eq (1)

$$E = \frac{q}{k \epsilon_0 A} \quad \text{--- (4)}$$

in substituting above eq in (3)

$$\frac{q}{k \epsilon_0 A} = \frac{q-q'}{\epsilon_0 A}$$



$$q - q' = \frac{q}{K}$$

Substitute $q - q'$ values in eq(2)

$$\oint \vec{E} \cdot d\vec{s} = \frac{q}{K\epsilon_0}$$

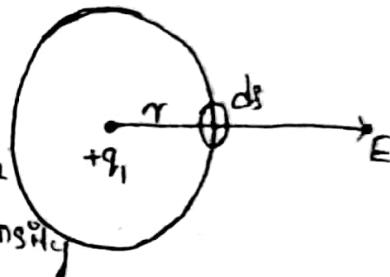
$$\boxed{\oint K \vec{E} \cdot d\vec{s} = \frac{q}{\epsilon_0}}$$

The above relation, through dielectric for a parallel plate capacitor holds good in all cases when the dielectric are present.

Q) Derive coulomb's law from Gauss law. what is a Gaussian surface?

A: coulomb's law from Gauss law:

Imagine a sphere of radius r with a point charge q_1 at its centre. Consider an elementary area $d\vec{s}$ on it. If E be the electric intensity at $d\vec{s}$, then



$$\text{flux through } \} = d\phi = E \cdot d\vec{s}$$

the area $d\vec{s}$

The value of E is the same at any point on the sphere

$$\begin{aligned} \therefore \text{Total flux through the } & \} = \phi = \oint \vec{E} \cdot d\vec{s} \\ \text{entire closed surface } \} & = E \oint d\vec{s} \\ & = E \times 4\pi r^2 \end{aligned}$$

By Gauss theorem,

$$\text{total flux through the } \} = \phi = \frac{q_1}{\epsilon_0}$$

$$\therefore E \times 4\pi r^2 = \frac{q_1}{\epsilon_0}$$

$$(or) E = \frac{q_1}{4\pi r^2 \epsilon_0}$$

At any point on the surface of the surface, if a charge q_2 were to be present, the force F due to the charge q_1 is given by

$$F = \text{Electric intensity} \times \text{charge}$$

$$= \frac{q_1}{4\pi\epsilon_0 r^2} \times q_2$$

$$= \frac{q_1 q_2}{4\pi\epsilon_0 r^2}$$

This is coulomb's law.

Gaussian Surface:

consider a sphere of radius r . let a point charge $+q$ be present at the centre. Then

$$\text{Total flux through the } \} = \frac{q}{\epsilon_0}$$

entire closed surface

This value is independent of the radius of the sphere.

thus the total flux through the entire closed surface of a sphere when a point charge is at its centre is independent of the radius. such a closed surface is called a Gaussian surface.

~~Q = Epsilon P~~

Q) Derive the relation between permability and susceptibility.

A: Relation between dielectric constant and electric susceptibility:

For most dielectric materials, the polarisation P is proportional to the electric field E within the dielectric
i.e $P \propto E$ or $P = \chi_e E$

where the constant χ_e is called the electric susceptibility of the material.

$$\therefore \chi_e = \frac{P}{E}$$

The polarisation P is given by $P = (\kappa - 1) \epsilon_0 E$.

where κ is the dielectric constant of material. Hence

$$\epsilon_r = \frac{(\kappa+1)\epsilon_0 E}{E} = (\kappa+1)\epsilon_0$$

$$(iii) \kappa = 14 \frac{\epsilon_r}{\epsilon_0}$$

Digital Electronics

Logic Gates:

Circuits which are used to process digital signals are called as logic gates.

Logic gates are 2 types.

i) Combinational gates.

ii) Sequential gates.

Combinational gates:

In combinational gates, the output at any instant depends upon the inputs.

Eg: OR gate, NOT gate, AND gate, NAND, NOR, XOR gate.

Sequential gates:

In sequential gates, the output depends upon the order of inputs.

Eg: flip-flops, counters and registers.

OR-gate:

An OR gate has 2 or more input signals but only one output signal.



OR gate Electrical circuit:



OR gate can be represented by $X = A + B$.

Truth table:

Input	Output	
A	B	$X = A + B$
0	0	0
1	0	1
0	1	1
1	1	1

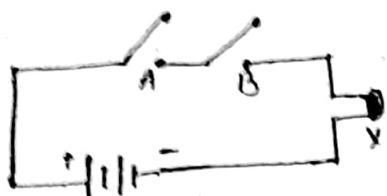
i) If $A=0, B=0$, then O/P $X=0$
ii) If $A=0, B=1$, then O/P $X=1$
iii) If $A=1, B=0$, then O/P $X=1$
iv) If $A=1, B=1$, then O/P $X=1$

AND gates

An AND gate has 2 or more input signals and one output signal.



AND gate electrical circuit



* AND gate can be represented by $X = A \cdot B$.

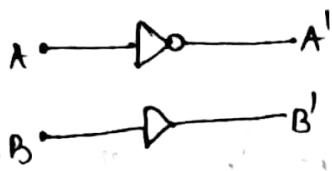
Truth tables

Input	Output	
A	B	$X = A \cdot B$
0	0	0
1	0	0
0	1	0
1	1	1

If $A=0 \& B=0$, then O/P $X=0$
If $A=1 \& B=0$, then O/P $X=0$
If $A=0 \& B=1$, then O/P $X=0$
If $A=1 \& B=1$, then O/P $X=1$

NOT gate :

The NOT-Gate has one input and one output signal.



* NOT gate can be represented by $x = \bar{A}$.

Truth table :

Input output

A $x = \bar{A}$

0 1

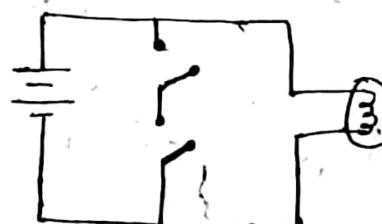
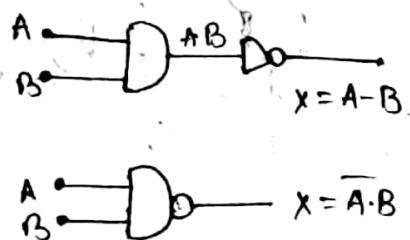
1 0

i) if $A = 0$ then output $x = 1$

ii) if $A = 1$ then output $x = 0$.

NAND gate :

NAND gate is a combination of AND gated and NOT gate.



Truth table :

Input output

A B $A \cdot B$ $x = \bar{A} \cdot \bar{B}$

0 0 0 1

if $A=0 \& B=0$ then output $x=1$

1 0 0 1

if $A=1 \& B=0$ then output $x=1$

0 1 0 1

if $A=0 \& B=1$ then output $x=1$

1 1 1 0

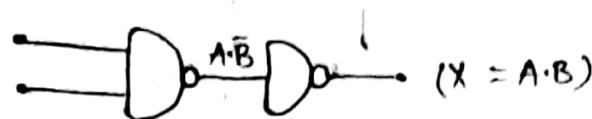
if $A=1 \& B=1$ then output $x=0$

* NAND gate is universal gate, since any logic circuit can be built by using NAND gate only.

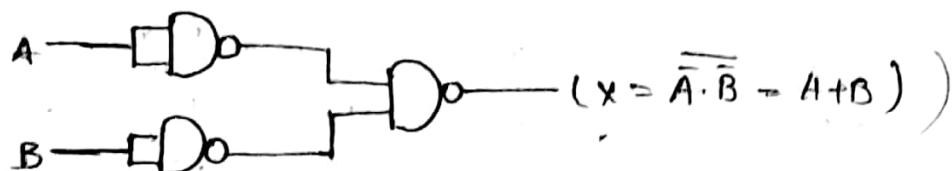
i) The NOT gate can be produced by one NAND gate.



ii) The AND gate can be produced by connecting two NAND gates.

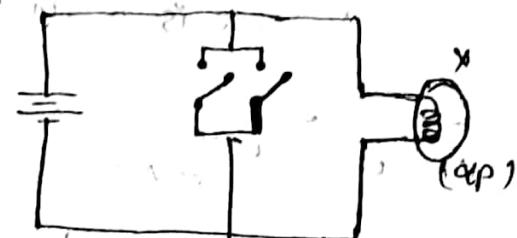
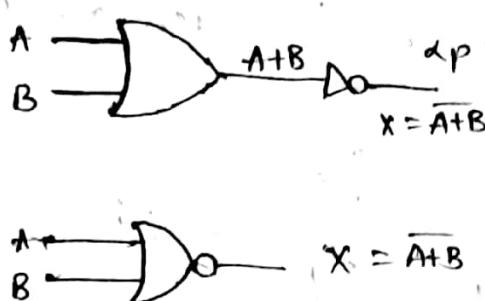


iii) OR gate can be produced by connecting three NAND gates.



NOR gate:

NOR gate is a combination of OR gate and NOT gate.



Truth table:

Input			Output
A	B	A + B	X = Ā + B̄
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

- if $A=0 \& B=0$ then output $x=1$
- if $A=1 \& B=0$ then output $x=0$
- if $A=0 \& B=1$ then output $x=0$
- if $A=1 \& B=1$ then output $x=0$

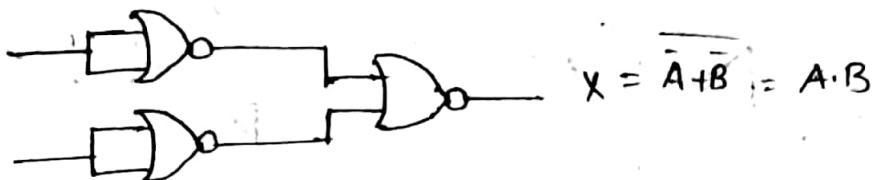
- * NOR gate is a universal gate, since any logic gate can be built by using NOR gate only.
- * The NOT gate can be produced by one NOR gate.



* The OR gate can be produced by connecting two NOR gates.

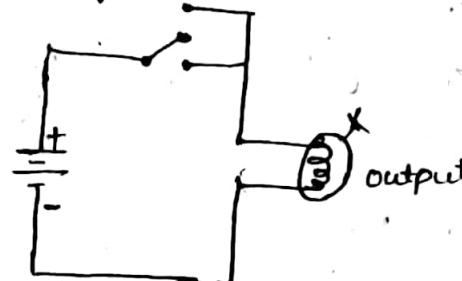
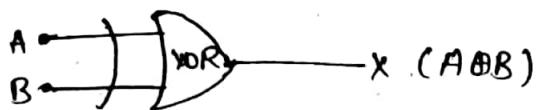


* The AND gate can be produced by connecting three NOR gates.



Exclusive OR gate (XOR-gate):

The XOR-gate has two input signals but only one output signal.

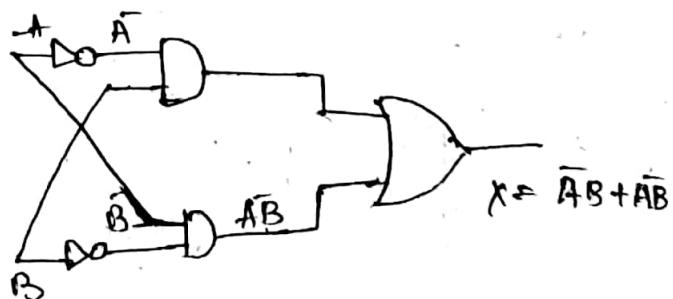
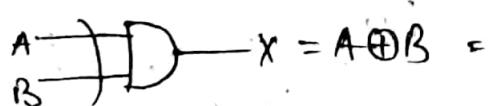


* XOR gate can be represented by $X = A \oplus B$

Truth Table:

Input	Output	if $A=0, B=0$ then Output $X=0$	
A	B	$X = A \oplus B$	if $A=0, B=1$ then Output $X=1$
0	0	0	if $A=1, B=0$ then Output $X=1$
1	0	1	if $A=1, B=1$ then Output $X=0$
0	1	1	
1	1	0	

In XOR gate output $X = A \oplus B = AB + \bar{A}\bar{B}$



$$A \oplus B = \bar{A}B + A\bar{B}$$

De morgan's theorem:

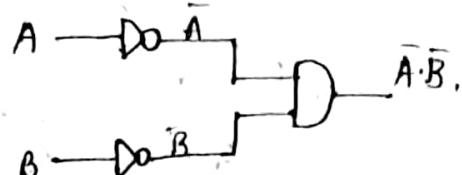
Theorem: The complement of the sum of two (or) more variables is equal to the product of the complement of the variables.

$$\overline{A+B} = \bar{A} \cdot \bar{B}$$

Theorem 1 - representation:



$$\overline{A+B} =$$



proof:

A	B	\bar{A}	\bar{B}	$A+B$	$\overline{A+B}$	$\bar{A} \cdot \bar{B}$
0	0	1	1	0	1	1
1	0	0	1	1	0	0
0	1	1	0	1	0	0
1	1	0	0	1	0	0

From the De-morgan's 1st theorem is proved

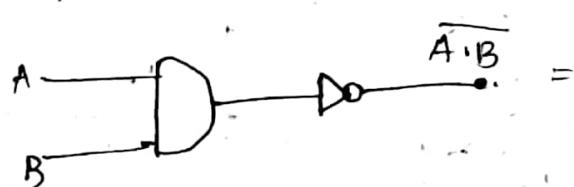
$$i.e., \overline{A+B} = \bar{A} \cdot \bar{B}$$

De-morgan's theorem:

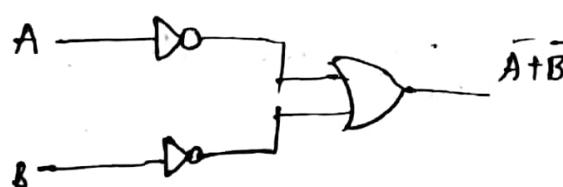
The complement of the product of two (or) more variables is equal to the sum of the complement of the variables.

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

Representation:



$$=$$



proof:

A	B	\bar{A}	\bar{B}	$A \cdot B$	$\bar{A} \cdot \bar{B}$	$\bar{A} + \bar{B}$
0	0	1	1	0	1	1
1	0	0	1	0	1	1
0	1	1	0	0	1	1
1	1	0	0	1	0	0

From table de-morgan's 8rd theorem is proved.

$$A \cdot B = \bar{A} + \bar{B}$$

De-morganization:

De-morgan's theorem can be used to determine the equivalent forms of boolean expression the process is called De-morganisation.

Step-1: complement the given expression.

Step-2: change all AND-gates to OR-gates and all OR gates to AND-gates.

Step-3: complement all individual variables.

Ex: $\sqrt{(A+B) \cdot (C+D)}$

Step-1: $\sqrt{(A+B) \cdot (C+D)} = (A+B) \cdot (C+D)$

Step-2: $(A+B) \cdot (C+D) = (A \cdot B) + (C \cdot D)$

Step-3: $(A \cdot B) + (C \cdot D) = (\bar{A} \cdot \bar{B}) + (\bar{C} \cdot \bar{D})$

$(A+B) \cdot (C+D) = (\bar{A} \cdot \bar{B}) + (\bar{C} \cdot \bar{D})$

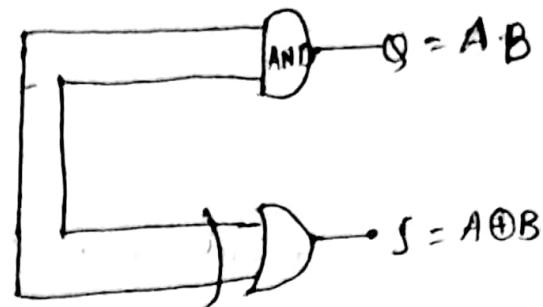
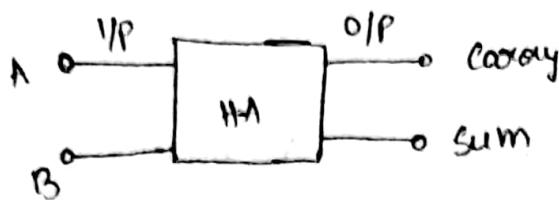
Half-adder:

The half-adder adds 2 binary digital at a time and produce a 2-bit data sum and carry.

The half-adder consists of an exclusive OR gate and an AND gate. The output of XOR-gate is called

the sum while the output of the AND gate is called the carry.

Half-adder having two inputs and two outputs.



Truth table:

Input		Output	
A	B	carry(C)	sum(S)
0	0	0	0
1	0	0	1
0	1	0	1
1	1	1	0

* when $A=0$ and $B=0$ then carry(C) = 0 and sum(S) = 0

when $A=1$ and $B=0$ then carry(C) = 0 and sum(S) = 1

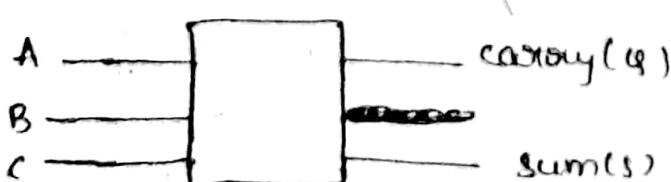
when $A=0$ and $B=1$ then carry(C) = 0 and sum(S) = 1

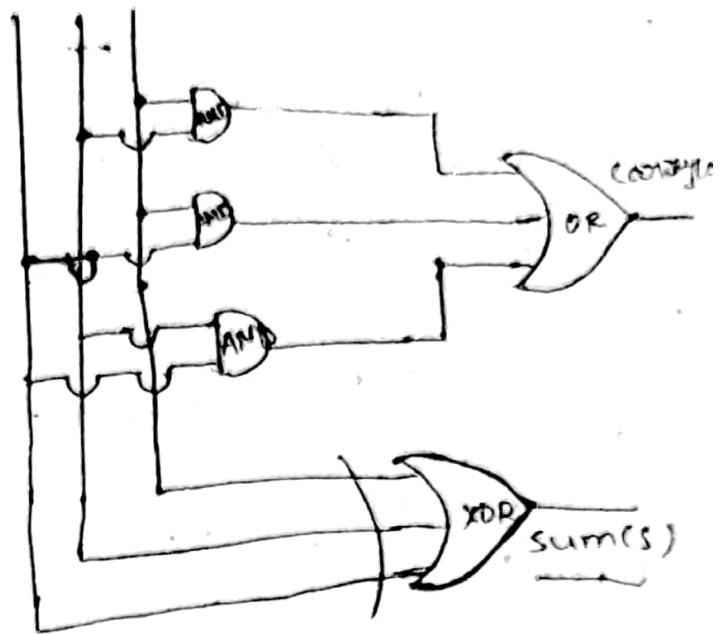
when $A=1$ and $B=1$ then carry(C) = 1 and sum(S) = 0

Full adder:

The full adder adds 3 binary digits at a time and produces 2-bit data i.e. sum and carry.

Full adder having three inputs and two outputs





Truth table:

Input	out put	sum(S)	carry(C)	
A	B	C		
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

- a. If $A=0 \& B=0 \& C=0$ then $\text{sum}(S)=0 \& \text{carry}(C)=0$
- if $A=0, B=0, C=1$ then $\text{sum}(S)=0 \& \text{carry}(C)=1$
- if $A=0, B=1, C=0$ then $\text{sum}(S)=0 \& \text{carry}(C)=1$
- if $A=1, B=0, C=0$ then $\text{sum}(S)=0 \& \text{carry}(C)=1$
- if $A=1, B=1, C=0$ then $\text{sum}(S)=1 \& \text{carry}(C)=0$
- if $A=1, B=0, C=1$ then $\text{sum}(S)=1 \& \text{carry}(C)=0$

Recomplement
1100
0011

But negative - 0011 ← final result.)

Laws of Boolean Algebra:

i) Laws of complementation (NOT laws)

The term complement means to invert the symbol is an over-bar. In boolean algebra this will mean to change 1 to 0 (or) 0 to 1. Thus we have

$$\text{law 1 } \bar{0} = 1$$

$$\text{law 2 } \bar{1} = 0$$

$$\text{law 3 if } A=0 \text{ then } \bar{A}=1$$

$$\text{law 4 if } A=1 \text{ then } \bar{A}=0$$

ii) OR laws:

The OR is represented by + sign.

If A and B are inputs and C is output then OR operation is written.

$$A+B=C$$

$$\text{so, } 0+0=0$$

$$0+1=1$$

$$1+0=1 \text{ and}$$

$$1+1=1$$

If both the inputs are 0, then output will be zero and if any input or both inputs is 1, then output will be 1.

3) AND laws:

The AND operation is represented by multiplication

$A \cdot B = C$ shows the AND laws. so,

$$0 \cdot 0 = 0, 0 \cdot 1 = 0$$

$$1 \cdot 0 = 0, 1 \cdot 1 = 1$$



so, it is clear that if any input is '0' or both inputs are zero; then output will be zero while if both the inputs are 1, the output will be one.

The four AND laws are

$$\text{Law-1 } A \cdot 0 = 0;$$

$$\text{Law-2 } A \cdot 1 = A$$

$$\text{Law-3 } A \cdot A = A$$

$$\text{Law-4 } A \cdot \bar{A} = 0$$

The fourth law represents that if one input logic is then other output \bar{A} would be zero. so that output is on the other hand, if $A=0, \bar{A}=1$ then again output will be zero (0).

4) commutative laws:

There are two commutative law. These laws allow change in the position of variable in OR and AND expression. These are

$$\text{Law-1 } A+B = B+A$$

$$\text{Law-2 } A \cdot B = B \cdot A$$

5) Associative laws:

There are two associative laws. These always allow removal of bracket from logical expression and regrouping of variables. These laws can be stated.

$$\text{Law-1 } A + (B+C) = (A+B)+C$$

$$\text{Law-2 } A \cdot (B \cdot C) = (A \cdot B) \cdot C$$

6) Distributive laws:

There are three distributive laws. These laws show that we can expand expressions by multiplying terms as in ordinary algebra. The distributive laws are

$$\text{law-1 } A \cdot (B+C) = (A \cdot B) + (A \cdot C)$$

$$\text{law-2 } A + (B \cdot C) = (A+B) \cdot (A+C)$$

$$\text{law-3 } A + (A \cdot B) = A+B$$

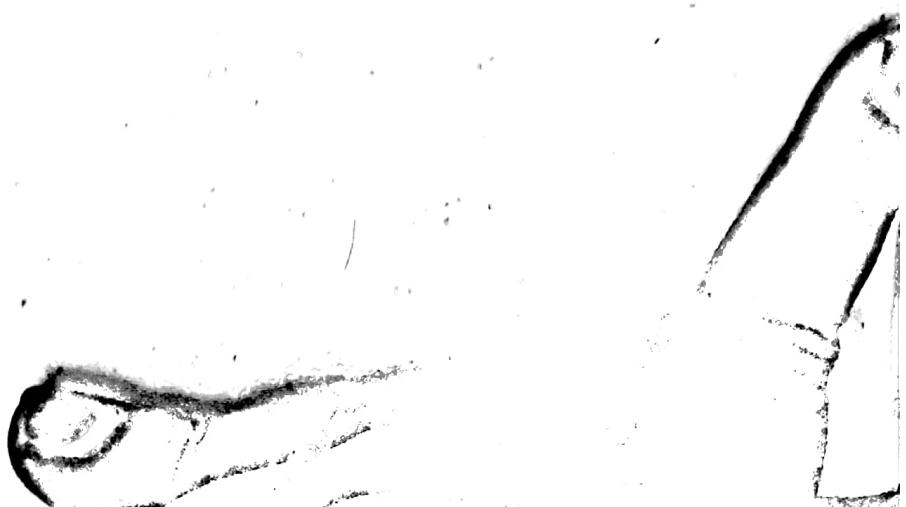
7) Absorptive laws:

There are three absorptive laws. They are.

$$\text{law-1 } A + (A \cdot B) = A$$

$$\text{law-2 } A \cdot (A+B) = A$$

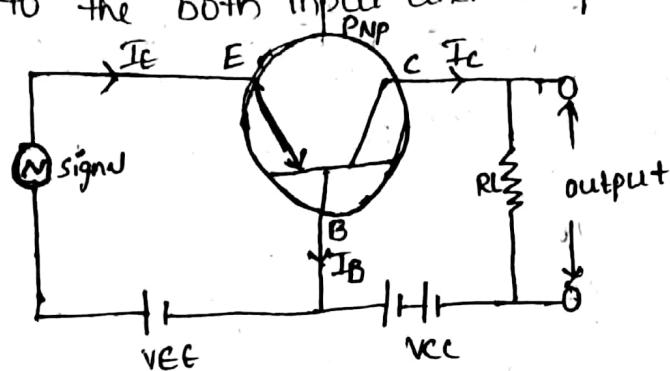
$$\text{law-3 } A \cdot (A+B) = A \cdot B$$



Q) Explain CB, CE, cc mode and also define α, β, γ for a transistor and derive relation between them.

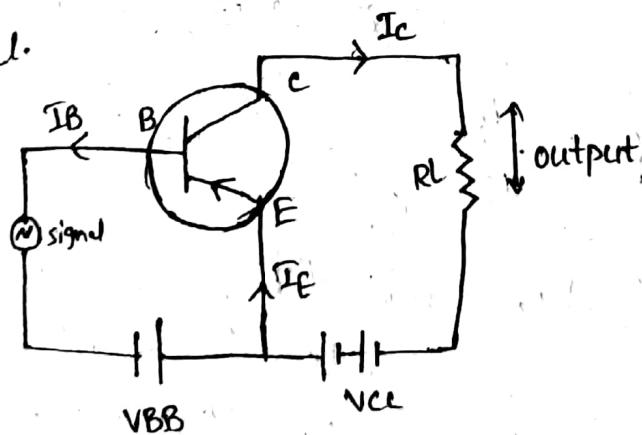
A: CB (common Base mode):

This mode is called the grounded base configuration. In this mode emmiter is the input terminal, collector is the output terminal and base is the common terminal to both input and output circuits.



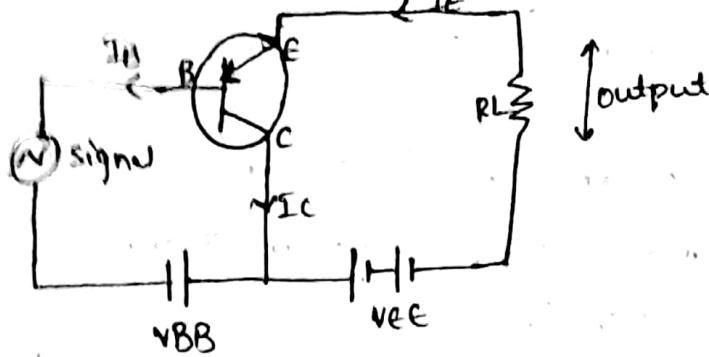
CE (common Emitter mode):

This mode is also called the ground ~~collector~~^{emitter} configuration. In this mode the base is the input terminal, collector is the output terminal and emmiter is the common terminal to both input and output terminal.



CC (common collector mode):

This mode is called the grounded collector configuration. In this mode base is the input terminal, emmiter is the output terminal and collector is the common terminal to both input and output terminal.



Current amplification factor (α):

The ratio of the collector current to the emitter current, without the amplification of a signal is called the current amplification factor (α_{dc}) or simply (α) of a transistor (CCB).

$$\alpha = \frac{-I_C}{I_E}$$

Current amplification factor (β):

The ratio of collector current to the base current, without the amplification of a signal is called the current amplification factor (β_{dc}) or simply (β) of a transistor with CE configuration.

$$\beta = \frac{I_C}{I_B}$$

Current amplification factor (γ):

The ratio of the emitter current to the base current, without the amplification of the signal is called the current amplification factor of the transistor.

$$\gamma = \frac{I_E}{I_B}$$

Relation between α , β and γ :

we know that

$$I_E = I_B + I_C \quad \dots \text{--- (1)}$$

$$\alpha = \frac{I_C}{I_E}, \beta = \frac{I_C}{I_B}, \gamma = \frac{I_E}{I_B}$$

(i) α in terms of β and γ : (common - Base)

(a) α in terms of β :

we know that $\alpha = \frac{I_C}{I_E}$

$$= \frac{I_C}{I_B + I_C}$$

$$\alpha = \frac{I_C / I_B}{\frac{I_B}{I_B} + \frac{I_C}{I_B}} = \frac{\beta}{1 + \beta}$$

$$\boxed{\alpha = \beta / 1 + \beta}$$

(b) α in terms of γ :

we know that $\alpha = \frac{I_C}{I_E}$

$$= \frac{I_E - I_B}{I_E}$$

$$\alpha = \frac{\frac{I_E}{I_B} - \frac{I_B}{I_B}}{\frac{I_E}{I_B}} = 1 - \frac{1}{\gamma}$$

$$\boxed{\alpha = \frac{\gamma - 1}{\gamma}}$$

(2) β in terms of α and γ : (common - Emitter)

(a) β in terms of α :

we know that $\beta = \frac{I_C}{I_B}$



$$= \frac{I_C}{I_E - I_C}$$

$$= \frac{I_C / I_E}{\frac{I_E}{I_E} - \frac{I_C}{I_E}}$$

$\beta = \frac{\alpha}{1-\alpha}$

(b) β in terms of γ :

we know that $\beta = \frac{I_C}{I_B}$

$$= \frac{I_E - I_B}{I_B}$$

$$= \frac{\frac{I_E}{I_B} - \frac{I_B}{I_B}}{\frac{I_B}{I_B}}$$

$\beta = \gamma - 1$

(c) γ in terms of α and β :

(a) γ in terms of α :

we know that $\gamma = \frac{I_E}{I_B}$

$$= \frac{I_E}{I_E - I_C}$$

$$= \frac{I_E / I_E}{\frac{I_E}{I_E} - \frac{I_C}{I_E}}$$

$$\phi = \Phi$$

$$\gamma = \frac{I_E}{I_B - I_0}$$

(b) γ in terms of β :

$$\text{we know that } \gamma = \frac{I_E}{I_B}$$

$$= \frac{I_B + I_C}{I_B}$$

$$= \frac{\frac{I_B}{I_B} + \frac{I_C}{I_B}}{I_B/I_B}$$

$$\gamma = \frac{1 + \beta}{1}$$

$$\boxed{\gamma = 1 + \beta}$$

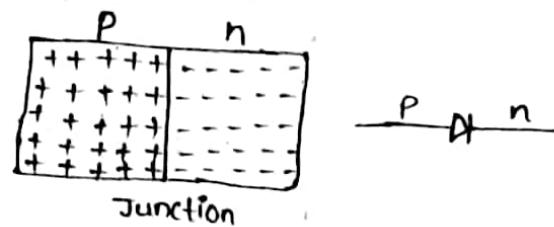
Q) Explain the working of junction diode?

Junction diode: A junction diode consists of p-type crystal joined to a n-type crystal so that they form one continuous crystal structure. The junction joining the two types is known as p-n junction diode. P-n junction is prepared in two ways (i) grown junction layer and (ii) fused junction type.

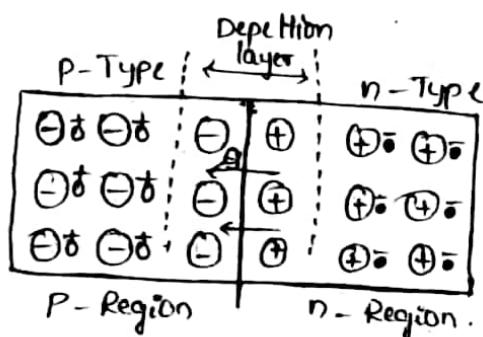
In grown junction method, p-type or n-type material is heated and impurities of opposite type are combined in the middle and then the original crystal is allowed to grow.

In the case of fused p-n junction, a small dot of indium is placed on a thin wafer of n-type germanium. After a few minutes of heat treatment, the indium fuses to the surface of germanium and produces p-type germanium just below the surface of contact. This p-type germanium along with n-type germanium ~~wafer~~ wafer forms a p-n junction.

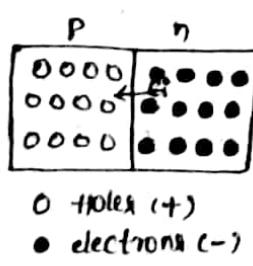
P-n junction diode is symbolically represented. The horizontal arrow represents the p-type position and the thick vertical line represents the n-type position of the semiconductor diode. The plane dividing the two zones is called the junction.



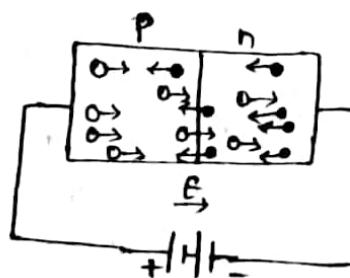
As soon as the junction is formed, electrons and holes diffusing at the junction due to thermal agitation. After diffusion, these charge carriers combine with their counter part and neutralise each other. This sets up a potential difference across the junction and hence an internal electric field E_i directed from n-region to p-region.



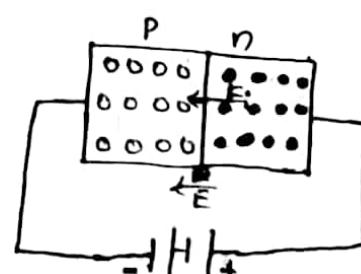
The layer on either side of the junction which becomes depleted of the mobile charge carriers is called the depletion layer for region. The potential difference across the depletion layer is called the potential barrier.



NO Bias



Forward Bias



Reverse Bias

As soon as battery is connected with its +ve pole joined to the p-region and -ve pole to the n-region. An external field E is set up

directed from p to n. It neutralise the small internal field (E_i). Under the influence of the electric field E , the holes move in the direction of the field from the n-region to the p-region. The battery connection that permits current to flow across the p-n junction is called forward bias.

When the battery voltage is reversed in polarity i.e., the +ve pole of the battery is joined to the n-region and the -ve to the p-region. The external field E is directed from n towards p and this adds to the internal field E_i . The holes in the p-region and electrons in the n-region are now pushed away from the junction and their motion stops. (The battery connection that prevents current to flow across the p-n junction is called reverse bias.)

(When the junction is in the reverse bias, a small reverse current still flows across the junction. The p-region and few holes in the n-region are called minority carriers. The reverse bias opposes the majority carriers and aids the minority ~~from holes in the p-region~~ ~~are called minority carriers~~ carriers to flow across the junction. Hence a small reverse current flows. The reverse current is referred to as leakage current of p-n junction diode)

From the above discussion it is clear that the junction diode offers a low resistance for the current to flow in one direction but a very high resistance in the opposite direction (reverse biased). Thus the junction diode acts as a rectifier.

③ Semiconductors:

A substance which has resistivity in between conductors and insulators is known as semiconductors.

(OR)

Semiconductors are materials whose electrical properties lie between conductors and insulators.

Types of semiconductors:

Semiconductors are 2 types they are

- 1) Intrinsic Semiconductor.
- 2) Extrinsic Semiconductor.

Intrinsic Semiconductors:

A semiconductor in an extremely pure form is known as intrinsic semiconductor (OR) pure semiconductor.

(OR)

Semiconductor in which electrons and holes are solely created by thermal excitations is called a pure (OR) intrinsic semiconductor.

- * In Intrinsic Semiconductors, current flows due to the motion of free electrons as well as holes.
- * Number of holes in valence band = number of electrons in the conduction band. (OR) In intrinsic semiconductor the no. of free electrons is always equal to the number of holes.

Eg: Si, Ge.

Extrinsic Semiconductors:

The semiconductor in which impurities are added is called extrinsic semiconductor. When the impurities are added to the intrinsic semiconductor it becomes an extrinsic semiconductor.

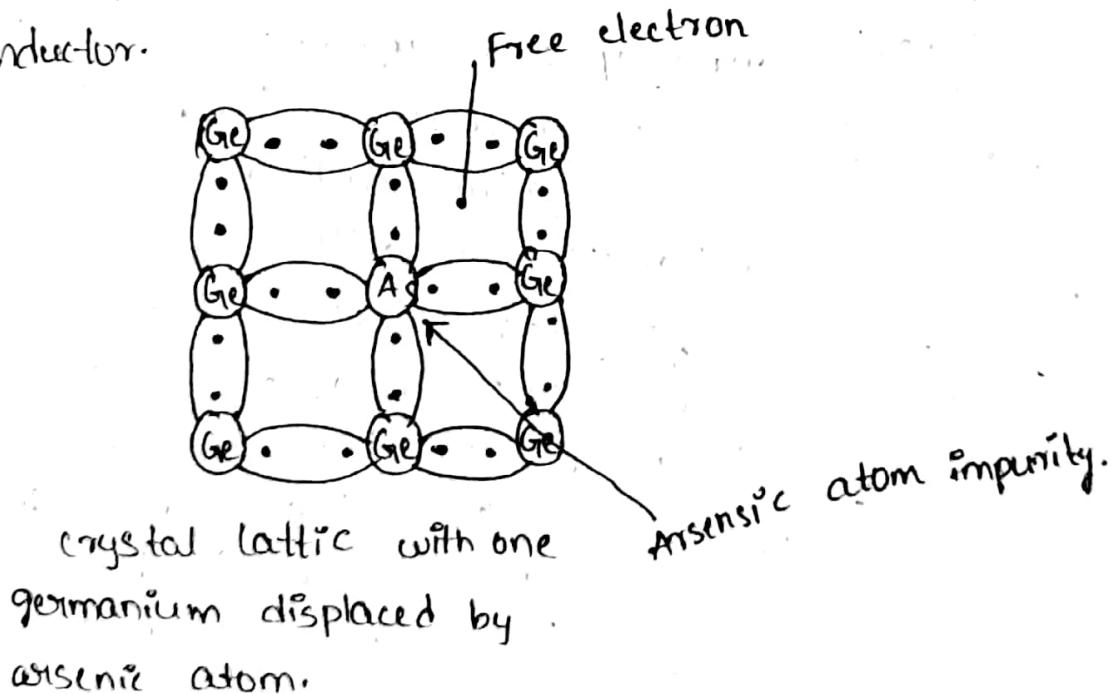


- * the process by which an impurity is added to a semiconductor is known as doping.
- * Generally, one impurity atom is added to a 10^8 atoms of a semiconductor.
- * Extrinsic semiconductor has high electrical conductivity.
- * Hence the extrinsic semiconductors are used for the manufacturing of electronic devices such as diodes, transistors etc.
- Extrinsic semiconductors are 2 types:

 - i) N-type Semiconductor.
 - ii) P-type Semiconductor.

N-Type Extrinsic Semiconductor:

When a small amount of pentavalent impurity is added to a pure semiconductor crystal during the crystal growth, the resulting crystal is called N-Type semiconductor.



Let us consider the case when pentavalent arsenic is added to pure germanium crystal. The arsenic atom fits in the germanium crystal in such a way that its four valence electrons form covalent bond with the

⑨ Transistor: (10m)

The transistor means transistor of resistance from input circuit to output circuit.

* Transistor is Bipolar device, it is also known as bipole.

* Junction transistor.

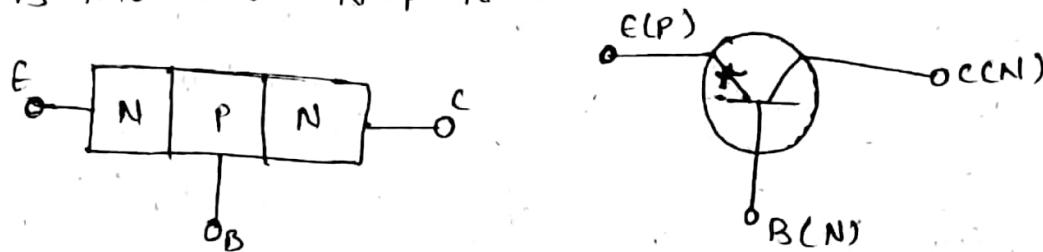
* There are two types of transistors.

1) N-P-N transistor

2) P-N-P transistor

1) N-P-N transistor:

When a layer of P-type material is sandwiched between two layers of N-type material the transistor is known as N-P-N transistor.



Transistor have 3 regions:

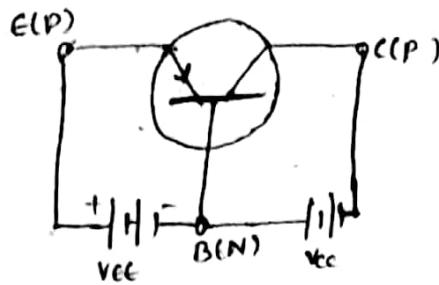
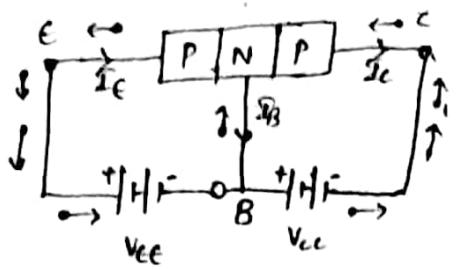
1) Emitter: The main function of this region is to majority charge carriers to the base and it is heavily doped region.

2) Base: The main function of this region is to injected charge carriers to the collector and it is lightly doped region.

3) collector: The main function of this region is the collect majority charge carriers through the base. It is "moderated region".

Forward biased while the collector-base junction is always reversed biased.

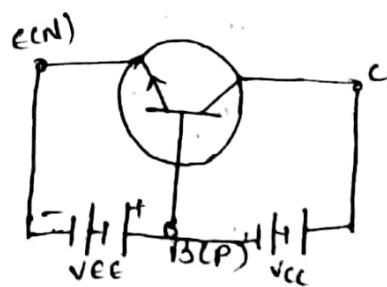
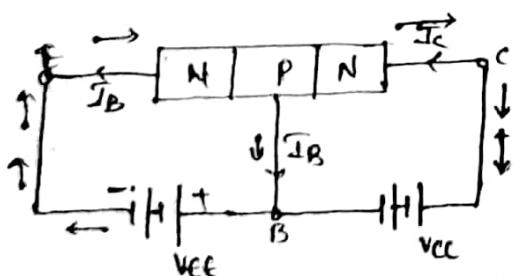
Operation of P-N-P transistor:



- (1) A P-N-P transistor, emitter, Base junction will forward biased by V_{EE} , it reducing depletion region.
- (2) collector-base junction as reverse biased by V_{CC} . it increasing depletion region.
- (3) Forward bias causes holes to flow towards base, this constitutes emitter current I_E .
- (4) As holes flow into the base, which is n-type. They combine with very few electrons and constitute base equivalent I_B .
- (5) The remaining large amount of holes cross the base region and through the collector region to the negative terminal of V_{CC} , it constitute collector current I_C .
- (6) Holes are majority charge carriers in P-N-P transistor
- (7) We can say that emitter current is the sum of collector current and base current.

$$I_E = I_B + I_C$$

Operation of N-P-N transistor:



- (1) In N-P-N transistor emitter, Base junction as forward biased by V_{EE} , it reduce depletion region.
- (2) collector-base junction as reverse biased by V_{CC} it increased depletion region.

(3) Forward bias cause electrons to flow - forward bias this constitutes emitter current I_E .

(4) As the electron flow into the base, which is p-type they combine with very few holes and constitutes base current I_B .

(5) the remaining large amount of electrons cross the base region and through the collector region to the positive terminal of V_{CC} , it constitutes collector current.

(6) Electrons are majority charge carriers in N-P-N transistor.

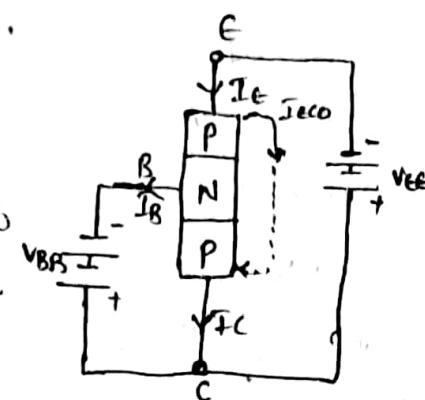
(7) we can say that emitter current is the sum of base current and collector current.

$$I_E = I_B + I_C$$

Total Emitter Current :

(1) The current is produced due to the majority charge carriers. from eq (3)

$$I_E = \gamma I_B$$

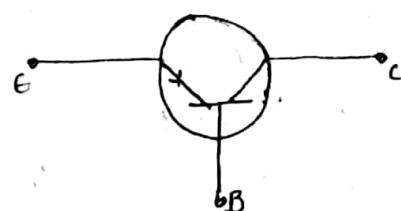
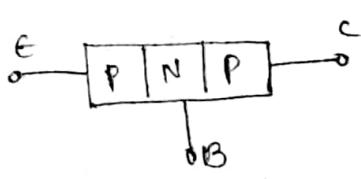


(2) The leakage current I_{EB} this current is due to minority charge carriers. It is represented by βI_B .

∴ The total emitter current

$$I_E = \gamma I_B + I_{ECO}$$

P-N-P transistor:



when a layer of n-type material is sandwiched between two layers of p-type material the transistor is known as P-N-P+ transistor.

Q) Explain the characteristic of semiconductor diode.

characteristic of semiconductor diode:

the characteristic curve ($V-i$) of a junction

diode is shown in the figure. If

the battery voltage $V=0$, the diode current is zero. As the voltage is increased, current begins to flow

in the diode. The forward current

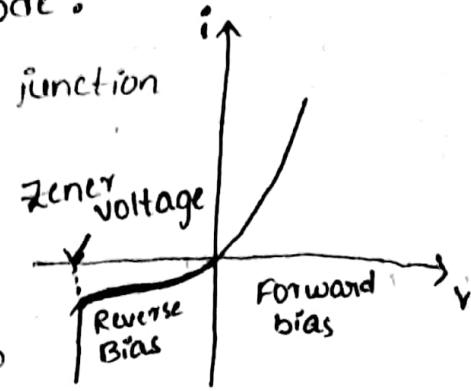
increases slowly at first, but as the battery voltage increases beyond the junction barrier voltage, the

current increases rapidly, approximately exponentially.

(It is of the order of 50 mA for a small forward voltage of 0.6 V). However, there is a limit to the amount of current which a diode can pass without burning it.

When the battery voltage is reversed in polarity, the junction is said to be reverse biased. As the reverse voltage is increased from zero, the current remains very small over a long range, increasing very slightly with increasing bias.

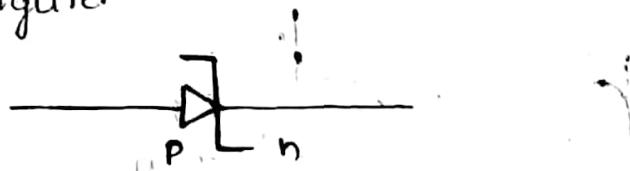
If the reverse bias is made very high, the covalent bonds near junctions break down and a large number of electron-hole pairs are liberated. The reverse current then increases abruptly to a relatively large value. This is known as avalanche breakdown. The curve indicates almost zero resistance at the point. The corresponding voltage is called the breakdown voltage or zener voltage. Any further increase in voltage may damage the junction by the excessive heat generated unless the current is limited by external circuit. This



phenomenon is made use of in Zener diodes which are employed as voltage regulators.

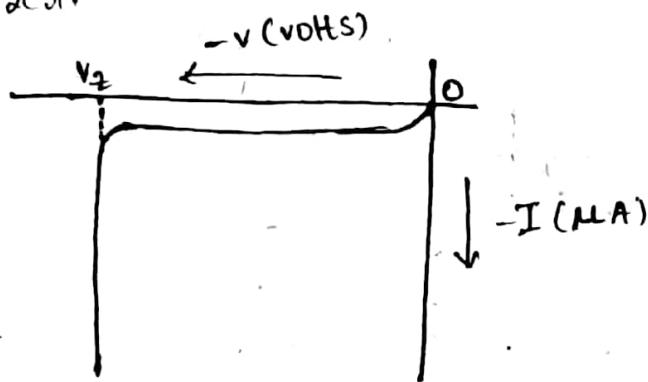
(Q) Explain about Zener diode and its V-I characteristics.

A: A properly doped p-n junction diode which has sharp break down voltage when operated in the reverse bias condition is called 'Zener diode'. This diode is operated in the reverse breakdown region without getting damaged. Silicon is preferred over Germanium while constructing Zener diodes, due to its high thermal stability and excellent compatibility. Zener diode is symbolized similar to the ordinary diode except that, the base is turned into 'Z' shape. The symbol of Zener diode is shown in the figure.



The breakdown voltage of a junction diode depends on the amount of doping. If the doping is heavy the depletion layer will be thin and it is less than 10^{-7} m. consequently, the breakdown occurs at lower reverse voltage (< 4 V) and further the breakdown voltage is sharp. whereas as a lightly doped diode has a higher breakdown voltage upto 200V. Due to small width of depletion layer for heavily doped p-n junction, a powerful junction field is created. An applied voltage of 6V or less may give a field as large as 10^7 V/m⁻¹ making conditions suitable for Zener breakdown. When the reverse bias voltage is increased to a critical value called Zener voltage or breakdown voltage, the diode breaks down and the electric field becomes

Strong enough to remove electrons from valence band and create electron hole pair which can tunnel through thin depletion layer. Electron - hole pairs so created increase the reverse current without change in voltage figure gives voltage current characteristics of reverse biased zener diode. (In forward bias, the characteristics are same as that of ordinary diode. In the reverse bias, as voltage is increased beyond 'Zener voltage' or the breakdown voltage the current increases sharply.) For widely different Zener currents, the voltage across zener diode remains constant. Hence, the diode can be used as a voltage regulator or stabilizer.



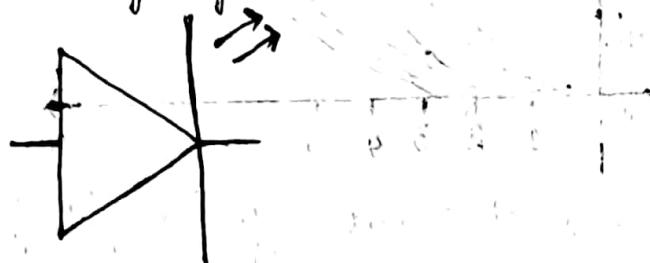
The properties of zener diode can be summarised as follows:

- 1) Zener diode is like an ordinary diode except that it is suitably doped to have sharp breakdown voltage in reverse bias called zener voltage (V_Z).
- 2) When it is forward biased, its characteristics are like that of ordinary diode.
- 3) Zener diode is operated in the reverse bias.
- 4) By changing doping concentration, zener diodes with widely different zener voltages can be designed.

- 5) They have high terminal stability and can accommodate large current without getting burnt out.
- 6) At zener voltage, the diode voltage remains constant over a wide range of currents.
- Q) Explain working of Light Emitting Diode (or)
Ans: Write short note on LED.

A: LED's are capable of emitting either visible light or invisible infrared when connected in forward biased condition. So, in short, we can define LED's as a device which converts electrical energy to light energy.

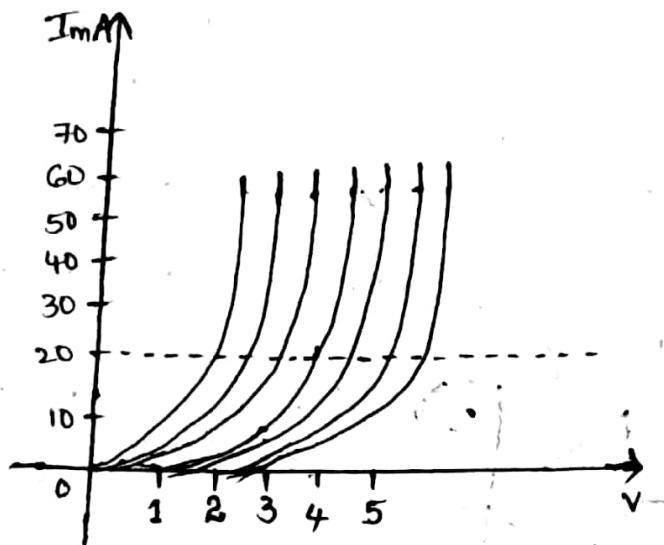
As diodes, LED's also have a unique symbol for representation. The symbol for an LED and a p-n junction diode is similar, except that LED contains an arrow pointing away from the diode that indicates the diode is emitting light.



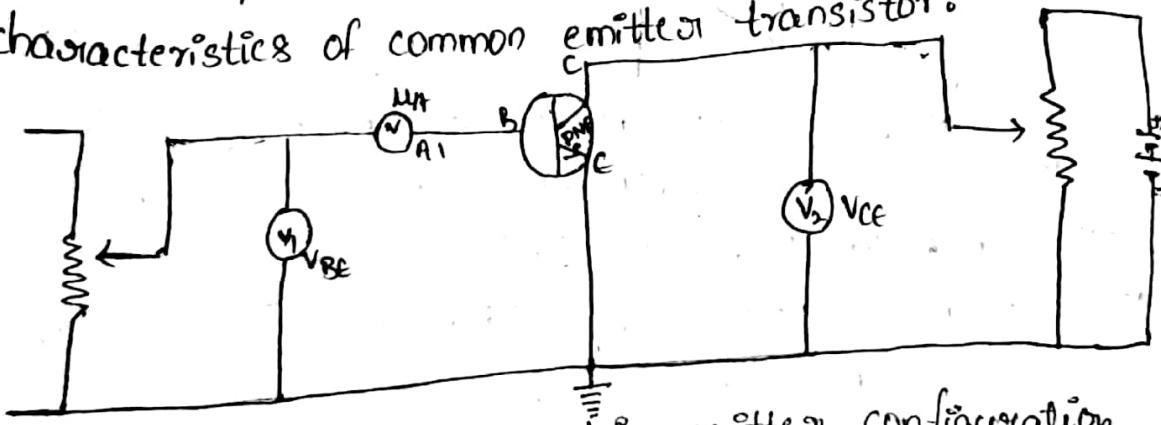
Now, we will discuss the mechanism and connection of an LED in a circuit. We know LED is a forward biased p-n junction diode which emits light when electricity is applied. This light energy is produced due to the recombination of holes and electrons at the junction of diode. If an LED is connected in reverse biased condition, it will not emit light. Moreover, the LED will be damaged in reverse biased condition. Mechanism of spontaneous emission explains the mechanism of emission of light energy from an LED.

We know that there are two different energy bands present in a semiconductor. conduction band with higher energy and valence band with lower energy. Also, there may be energy bands due to donor impurities near the conduction band and acceptor impurities near the valence band. when an electron transits from a higher to lower energy level, light energy is released.

Now, V-I characteristics of LED's are similar as of diode connected in forward biased condition,



③ Characteristics of common emitter transistor:



PNP transistor connected in emitter configuration.

- In the circuit, the battery V_{BB} provides forward bias to emitter and base with the help of potential divider R_B , the voltmeter V_1 measures the base-emitter

voltage V_{BB} the microammeter A_1 measures the base current I_B .

2) the battery V_{CC} provides reverse bias to collector and emitter with the help of potential divider R_2 .

— the voltmeter V_2 measures the collector-emitter voltage V_{CE} .

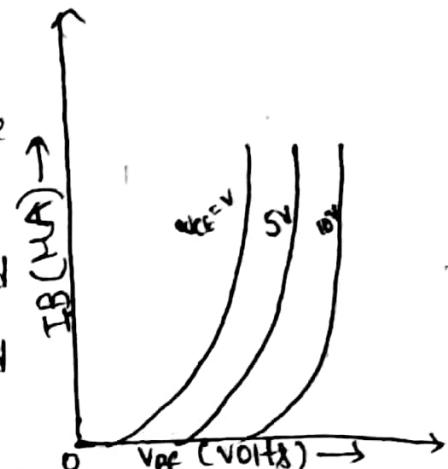
— the milliammeter A_2 measures the collector current I_C .

Input characteristics:

the curve between the base current I_B and base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE} represents input characteristics.

For plotting input characteristics the collector-emitter voltage V_{CE} is fixed.

The base-emitter voltage V_{BE} is varied with the help of potential divider R_1 and the base current I_B is drawn.



(a) It can show forward-biased diode curve.

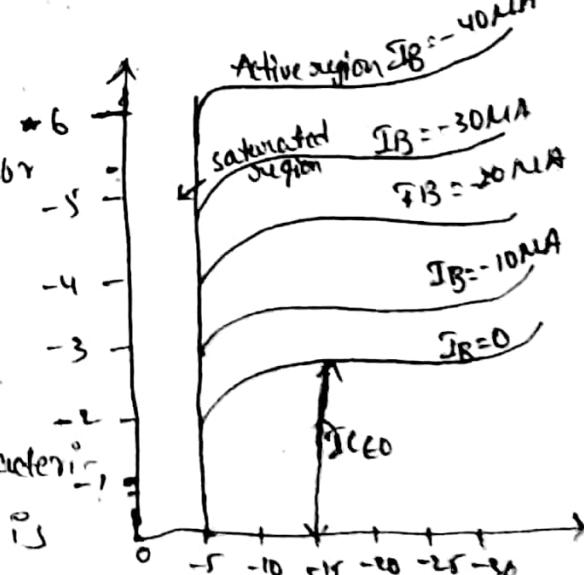
(b) The input resistance of common-emitter circuit is higher than that of common-base circuit.

(c) Input resistance: the ratio of change in ΔV_{BE} to the change ΔI_B at constant V_{CE} as defined as input resistance.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad (V_{CE} = \text{constant})$$

Output characteristics:

The curve between collector current I_C and collector-emitter voltage V_{CE} at constant base current I_B represents the output characteristic.



For plotting output characteristic, the base current I_B is

kept fixed with the help of potential divider R_2 , the value of V_{CE} is varied in steps and the collector current I_C is noted for each value of V_{CE} .

A graph of I_C against V_{CE} is drawn.

- a) In active region the output current I_C is independent of output voltage V_{CE} and depends on ~~constant~~ input current I_B . In this region transistor can be used as amplifying device.
- b) In saturated region, the change in base current I_B doesn't produce a corresponding change in collector current I_C .
- c) In the cutoff region, a small amount of collector current flows when base current $I_B = 0$. This is due to minority charge carriers I_{CEO} .
- d) Output resistance: The ratio of change in collector emitter voltage (ΔV_{CE}) to the resulting change in collector current (ΔI_C) at constant base current I_B is defined as output resistance.

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} / I_B = \text{constant}$$