Unit-5

Each memory data lines contains datalines (i/p or o/p), address lines and control lines.

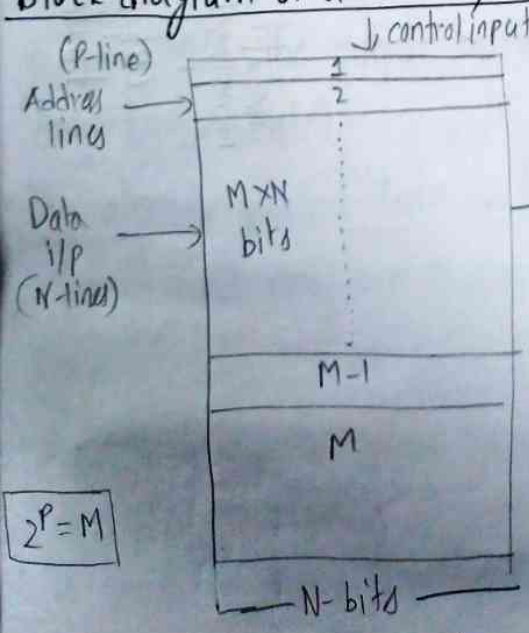
Termindogy in memory:

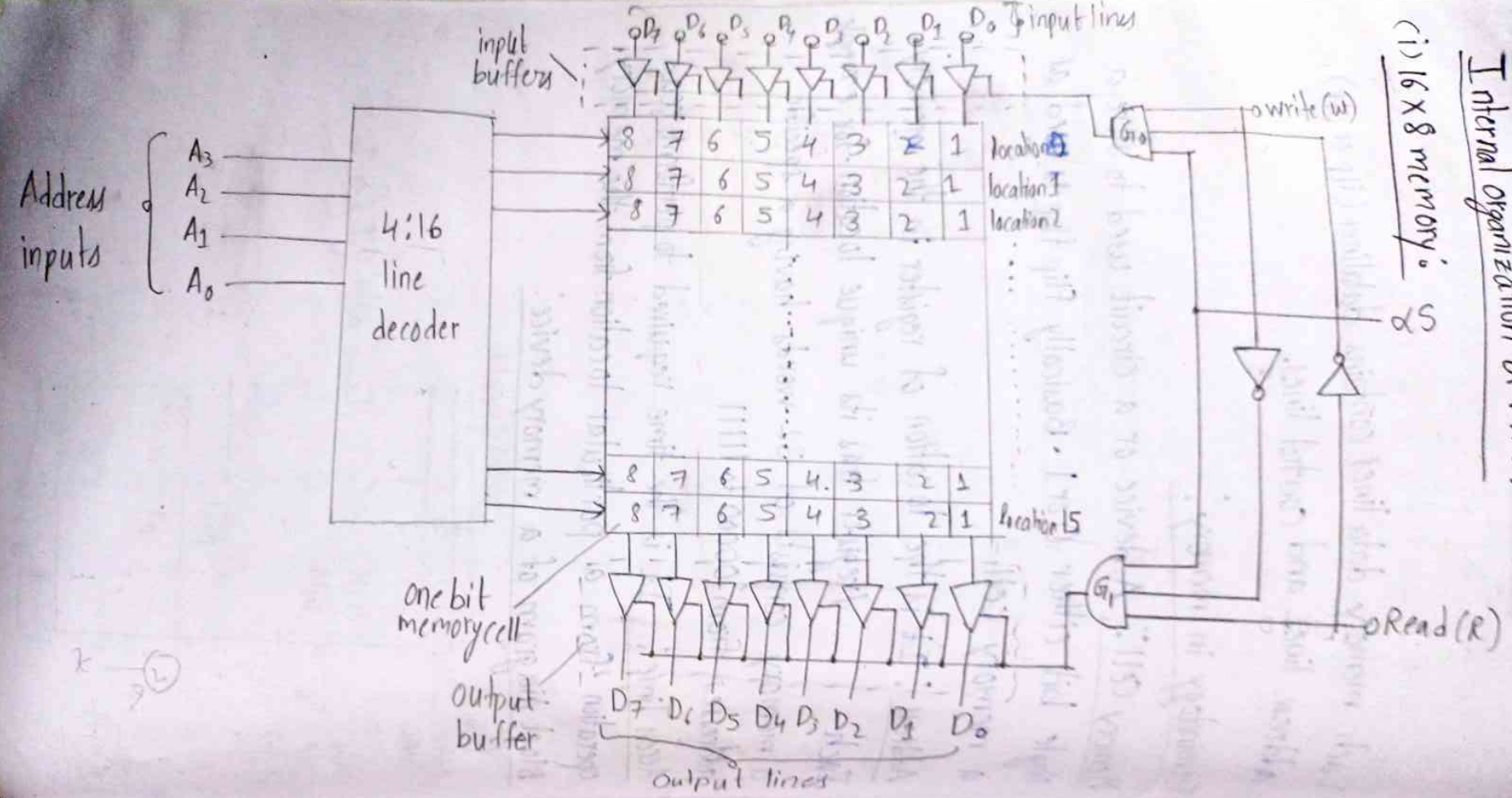
Memory Cell: A device or a circuit used to store a single bit either 0 or 1. Basically flip flop is used as a memory cell.

Address: It is the location of register in the memory. Each register has its unique location. for example a memory consists of 32 words having a specific addresses from 00000 to 11111

Access Time: It is the time required to perform read operation from a particular location from the memory.

Block diagram of a memory device:




Internal organization of RAM:
(i) 16 × 8 memory:
input buffers
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 8 input lines
write (W)
CS
Read (R)
G_0
G_1
Address inputs
A_3
A_2
A_1
A_0
4:16 line decoder
location 0
location 1
location 2
location 15
one bit memory cell
output buffer
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
output lines

- RAM is also called as 'Read' and 'Write' memory. It is a volatile in nature. The time it takes to transfer information to (or) from any desired location is same. Hence it is called Random Access Memory.
- Data can be written into and read from a RAM at any selected address in any sequence.
- The internal organization of 16 by 8 (16x8) memory chip is as shown in figure. It contains 4 address lines to select 16 addresses locations and 8 data lines to put 8 bit data into specific memory location.
- For 4 to 16 line conversion 4:16 decoder is used.

Write Operation:

- Set CS=1 for memory enable W=1 and R=0. This will enable G_0 and disable G_1 means input buffers are enables and output buffers are disabled.
- During this operation G_1=0 data will not enable (disable) at the output lines. The output buffers are goes into tri-state (impedence state).
- The already placed data on that particular location is cleared and new one is stored.

Read operation:

- Read operation means to access the data from a selected memory location.
- To read the data from the RAM following steps are as follows:

- CS=R=1 and W=0 this will enable gate (G_1) and disable gate (G_0).
- The address of memory location is applied to the address lines.
- After this input buffers are disabled and output buffers are enabled.
- The output buffers will pass the data of selected memory location to the output data lines.

Types of RAM:

There are two types of RAM.

(i) Static Ram (S-RAM)

(ii) Dynamic RAM (D-RAM)

(i) **Static Ram:** SRAM is a volatile memory, it requires power to maintain the data.

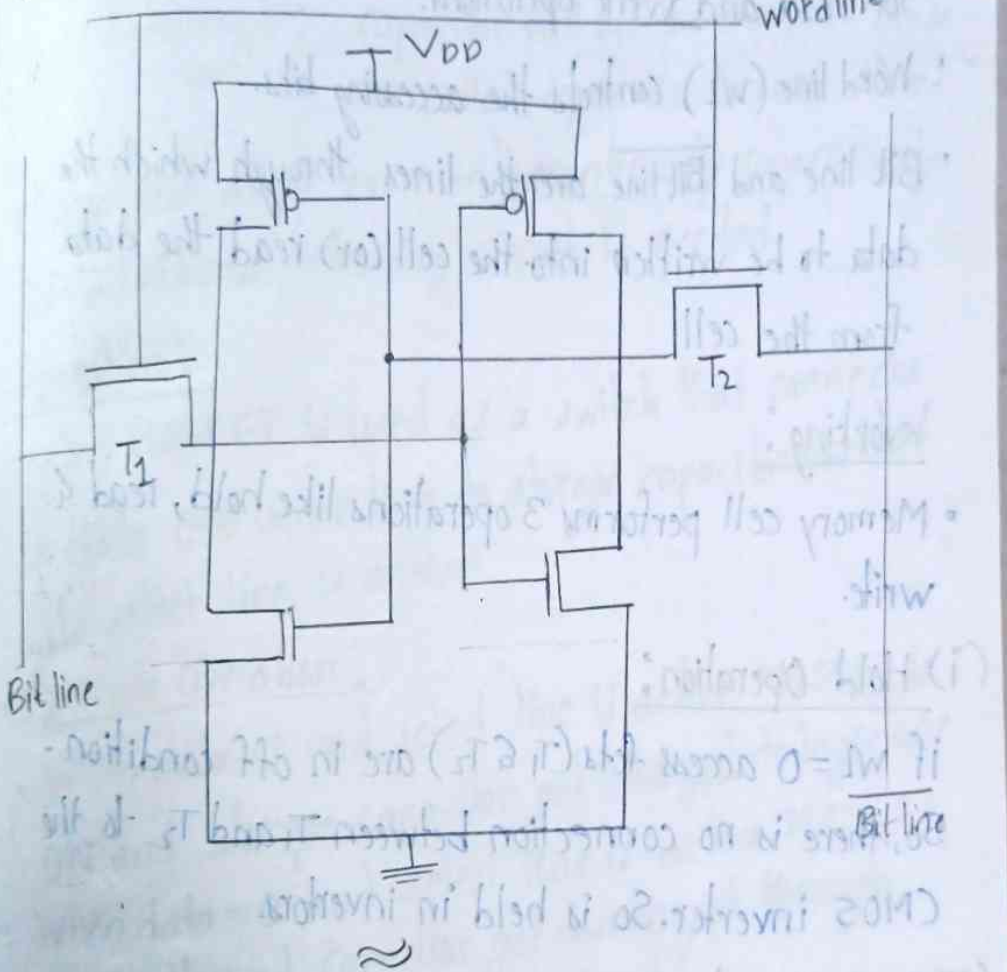
- SRAM is a matrix of static, volatile memory cells & address decoding system integrated on chip to allow read or write operations
- It can be implemented by using bipolar as well as most technology.
- It is basically a flip flop which stays in a given state i.e., store a bit either 0 (or) 1 as long as power is given.
- In the SRAM memory cells are arranged in parallel so that all the data can be received (or) retrieved

simultaneously.

- The SRAM is available in two types.

(i) TTL RAM Cell (ii) MOS RAM Cell

SRAM (using MOS Technology):



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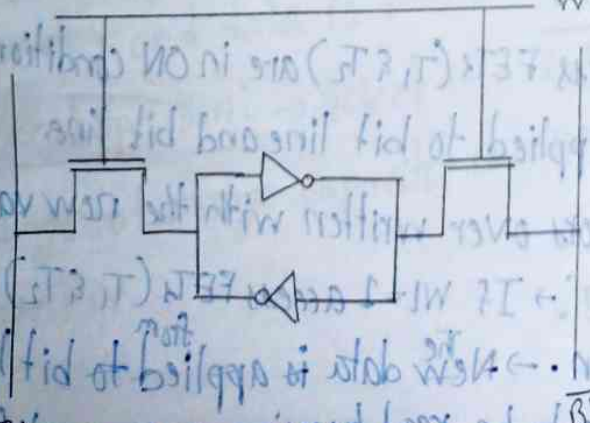


- In this there are 6 MOSFETS are used. There are cross coupled CMOS invertoers for storage purpose of bit either 0 (or) 1.
- T_1 and T_2 are access FETs i.e., access the stored data for read and write operations.
- Word line (WL) controls the accessing bits.
- Bit line and $\overline{\text{Bit line}}$ are the lines through which the data to be written into the cell (or) read the data from the cell.

Working:

- Memory cell performs 3 operations like hold, read & write.

(i) Hold Operation:

if WL=0 access fets (T_1 & T_2) are in off condition. So, there is no connection between T_1 and T_2 to the CMOS inverter. So is held in invertors.

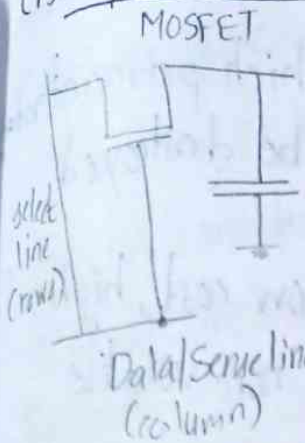
(ii) Write Operation:

If WL=1 access FETs (T_1 & T_2) are in ON condition.

- New data is applied to bit line and $\overline{\text{bit line}}$.
- Data in inverters over written with the new value.

(iii) Read Operation: → If WL=1 access FETs (T_1 & T_2) are in ON condition. → The data from bit line & $\overline{\text{bitline}}$. → Data are to be read by using sense amplifier.

(i) Dynamic RAM (DRAM):



• In DRAM the data is stored in the form of charge in the capacitor When data is one, the capacitor is charged and when data is zero the capacitor will not be charged. These are called dynamic because stored charge leak away even with continously power supply. So additional refreshing circuit is needed.

Operation:

→ The MOSFET is used as a switch that connects data or sense line to storage capacitor. when its select line is active.

(i) Write Operation:

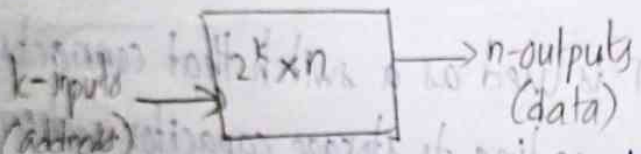
• When data = 1 and select line is active. MOSFET is ON and storage capacitor get charged to logic one
• When data = 0 and select line is active MOSFET is ON charged capacitor get discharged through MOSFET and data is zero stored.

(ii) Read Operation:

→ Select line is active and voltage of storage capacitor is sensed by using sense line.

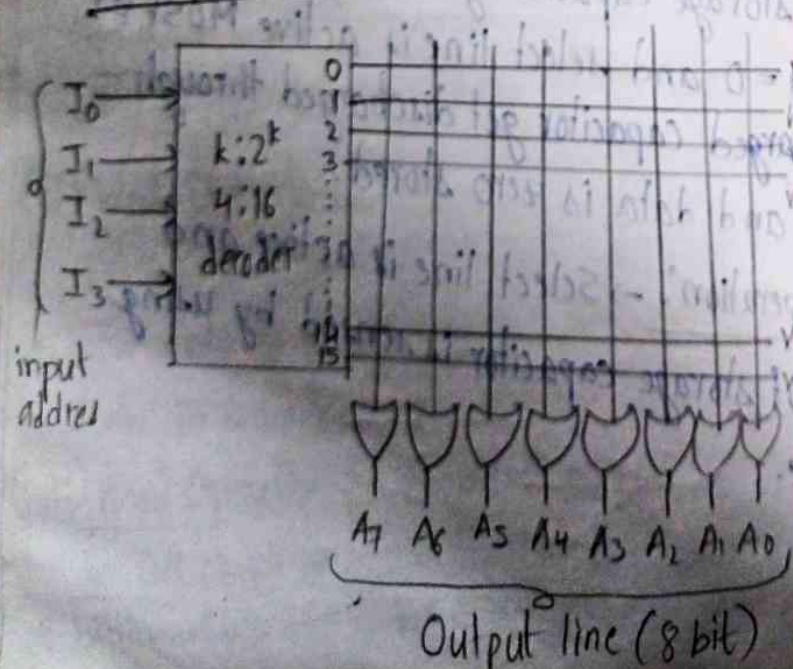
ROM (Read Only Memory):

- ROM is a memory device in which permanent binary data is stored. it could not be destroyed even when power is turned off.
- It is very useful because of it's low cost, high speed, system design flexibility and non-volatile in nature.
- The block diagram of ROM is as shown in the figure. It consists of k-inputs and n-outputs.



- The k-input lines provides the k-bit memory address and n-bit is the data output stored in a ~~word or register~~ i.e. selected by address.

Internal Construction of ROM:



- A $2^k \times n$ ROM consists of $k:2^k$ decoder and n OR gates. Therefore, n OR gates it contains 2^k words or registers of n bits each.
- Let us consider 16 x 8 ROM, for this we require 4:16 decoder and 8 OR gates as shown in the figure.
- Each OR gate must be considered as having 16 inputs.
- Each output of the decoder is connected to one of the inputs of each OR gate. Total internal connection in the ROM may be $16 \times 8 = 128$
- All 128 connections are programmable.
- A programmable connection between 2 lines inter
- connection is logically equivalent to a switch can be considered close (logic one stored) (or) open (logic 0 stored).

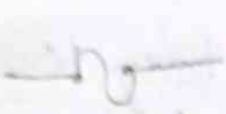
PROM (Programmable Read Only Memory):

- The PROM can be electrically programmed by the user and can't be re-programmed.
- For this reason these devices are refers to as one time programmable (OTP) [OTP ROM].
- The fuesable link are used in PROM to store one (or) zero in the memory cell.
- If the fuesable link is burnt / blow the cells become open at one end in order to program that

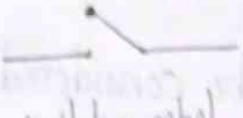
memory cell as "zero" storage.

- If the fuseable link is not burnt the cell is connected to circuit in order to program that memory cell has "1" storage.

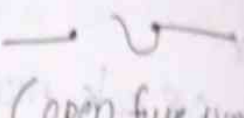
closed switch symbol



fuse symbol (closed fuse)



switch symbol (open)



(open fuse symbol)

EPROM (Erasable programable Read Only Memory):

- An EPROM can be programable by an user and it can also be erased and re-programmed according to requirement.
- This ROM is electrically programmable by applying special voltage level (10 to 25 volts) to the chip input for a specified amount of time.
- The programming process is performed by seperate programming circuit (dumper). i.e, seperated from the circuit.
- This programming process can take up to several minutes.
- Once an EPROM cell has been programmed it can be erased by exposing it to ultra violet light (UV) through a window on the chip package.

. The erasing process typically required 15-20 minutes.
. UV light erases all the cells at the same time not only selected cells.
. Once erased the EPROM can be re-programmable.

EEPROM (Electrically Erasable PROM):

. This is similar to EPROM except that, the data is erased by electrical signal (by applying a high voltage -21 volts instead of UV light).
. The main advantage is it can selectively erase the memory location and re-programmed with out disturbing the correct data in the other memory location. It is also known as Electrically Alterable Programmable Read Only Memory (EAPROM).

PLA (Programmable Logic Array):

inverter → buffer (or) ▽ ← buffer inverter

structure:

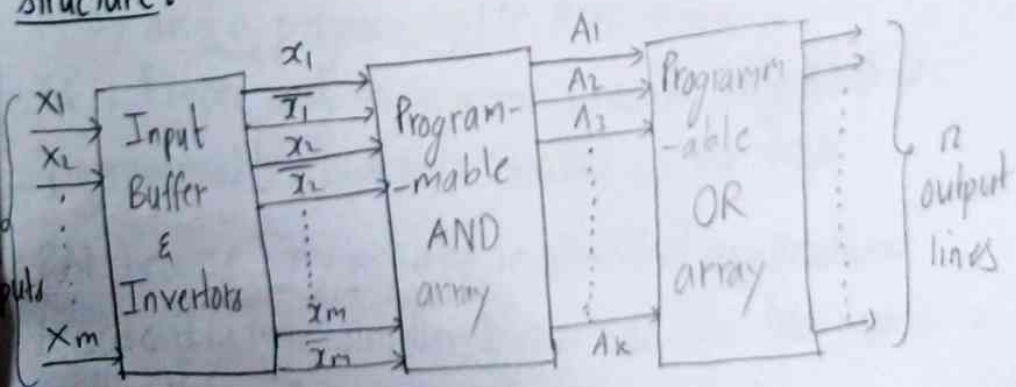


fig: PLA Structure

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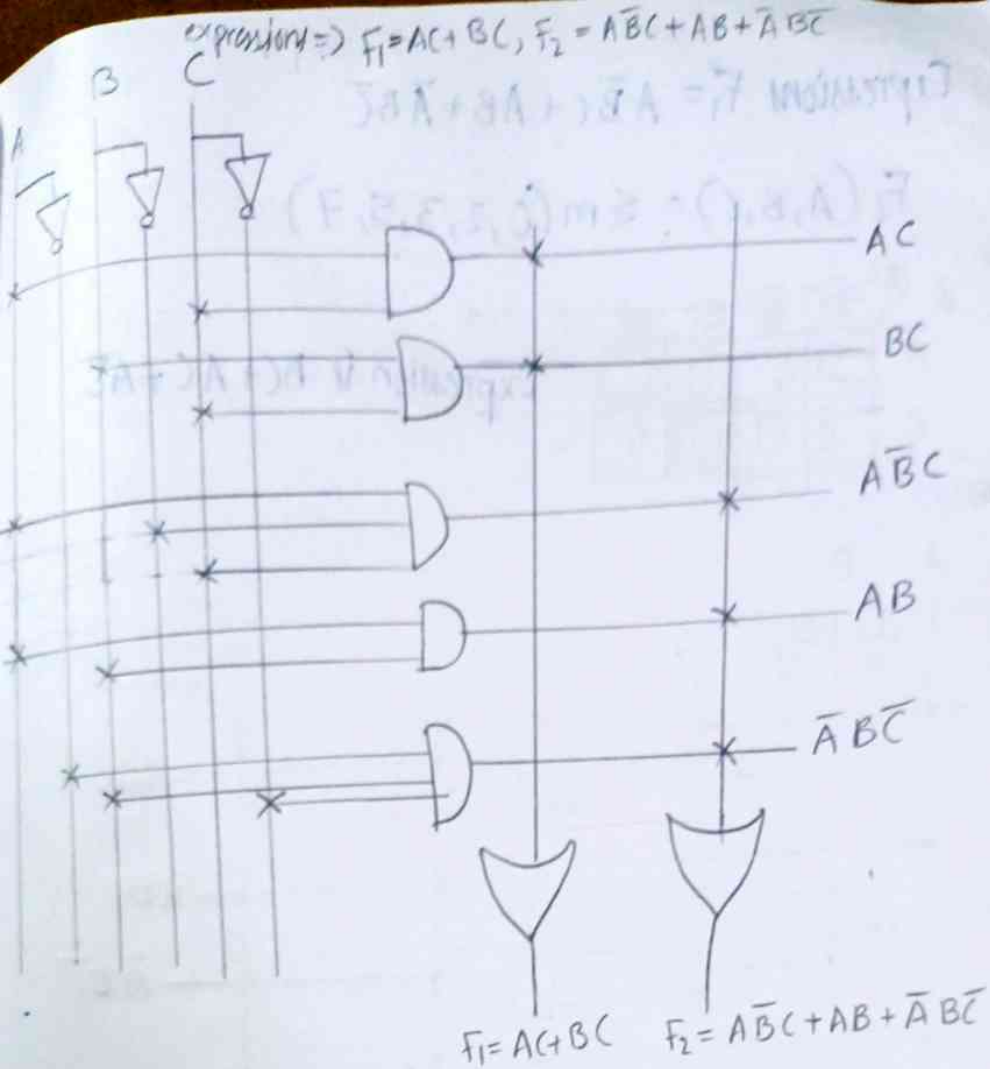
[expressions ni implement chese device]

- The input variables are connected to AND array which produces selected product terms of the input variables.
- The product terms are then connected to OR gate to provide sum of products for the required boolean functions.
- In PLA both AND and OR array is programmable
- In this figure shows the structure of PLA with 'm' inputs and 'n' outputs.
- PLA circuits are very small. So they are not useful commercially.
- The internal logic of PLA with 3 inputs and 2 outputs is as shown in the figure each input and its complement value are connected to the inputs of each gate as connected by inter connections between vertical and horizontal lines



PAL (Programmable Array logic):

- The PAAL is programmable logic device with a fixed OR array and a programmable AND array.
- It is more easy to program because only AND is programmable, but less flexible as the PLA.
- PAL become very popular in practical applications because it is more simplier to manufacture less expensive and better performance.
- When designing with a PAL the boolean functions must be simplified to fit into each sections.

Expression $F_1 = A\bar{B}C + AB + \bar{A}B\bar{C}$

$F_2(A,B,C) = \Sigma m(0,2,3,5,7)$

A \ BC	$B\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	0	1	1
A	0	1	1	0

Expression is $BC + AC + A\bar{C}$