Unit - 2.

Op-Amp as a voltage comparator :-

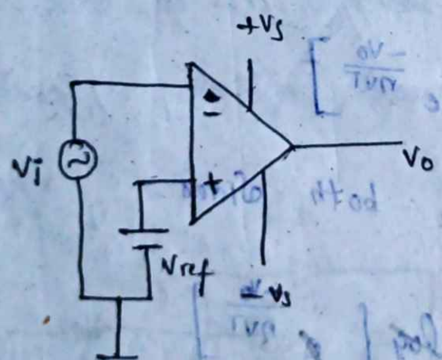
→ It is a circuit used compare the Input voltages of an op amp.

→ It is an open loop op-amp.

→ comparator is also called as square wave generator.

Inverting comparator :-

→ If Input votage is given to the inverting terminal and refference voltage is given non-inverting terminal then it is called inverting comparator.



→ Compare the input voltages V_{in} & V_{ref} then it produces output either +ve (or) -ve saturation voltage

Case - 1 :-

$V_{in} > V_{ref}$

$V_{id} = V_{ref} - V_{in}$

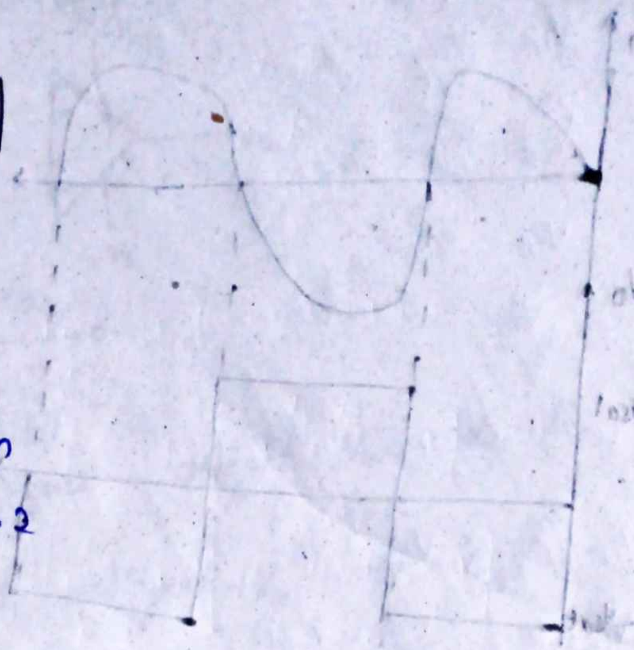
$V_{id} = 0.3 - 1$

$= -0.7$

$V_{id} = -Ve$

$V_0 = -Ve$

$$\boxed{V_0 = -V_{sat}}$$



Case - 2 :-

0.2 0.3

$V_{in} < V_{ref}$

$V_{id} = V_{ref} - V_{in}$

$V_{id} = 0.3 - 0.2$

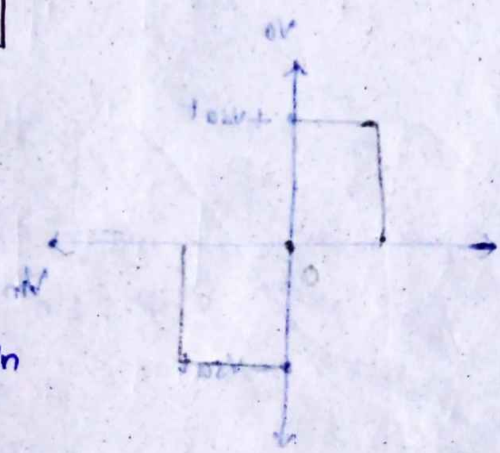
$V_{id} = 0.1$

$V_{id} = +Ve$

$V_0 = +Ve$

$$\boxed{V_0 = +V_{sat}}$$

Case - 3 :-



$V_{in} = V_{ref}$

$V_{id} = V_{ref} - V_{in}$

$V_{id} = 0$

$$\boxed{V_0 = 0}$$

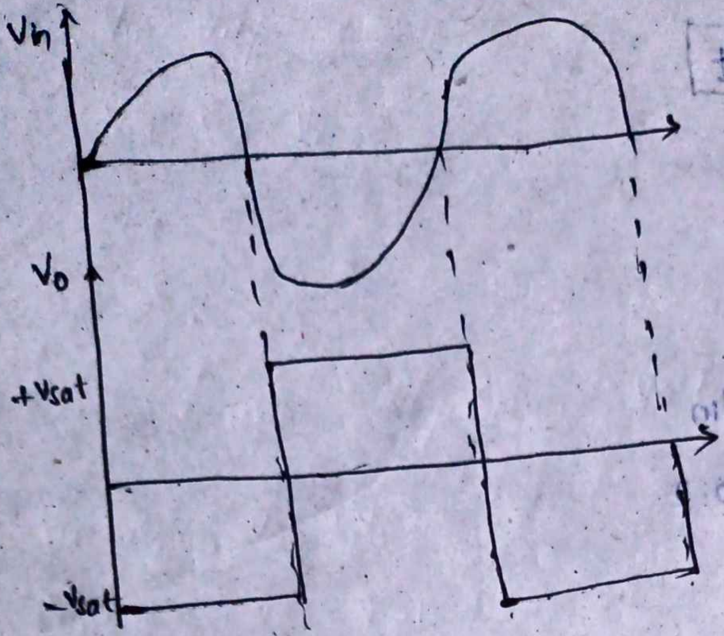
Let us assume $V_{ref} = 0$

1) $V_{in} > 0$; $V_0 = -V_{sat}$

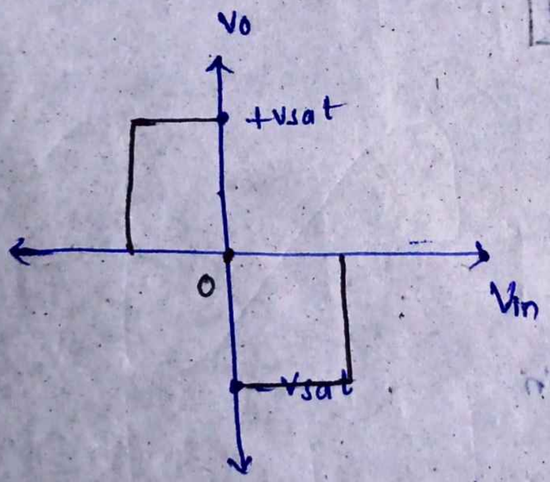
2) $V_{in} < 0$; $V_0 = +V_{sat}$

3) $V_{in} = 0$; $V_0 = 0$.

wave form:-

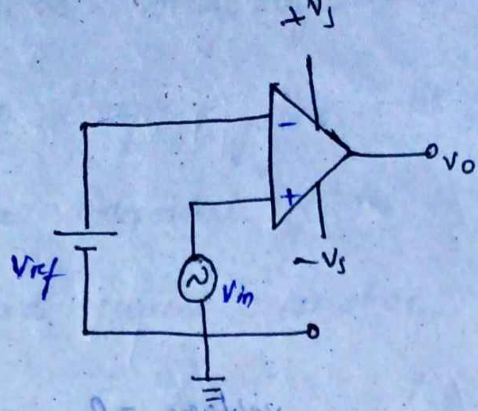


Transfer Curve:-



NON-Inverting comparator:-

→ If input voltage is given to the non-inverting terminal and reference voltage is given to the inverting terminal then it is called as non-inverting comparator.



→ Compare the input voltages V_{in} and V_{ref} then it produces output voltages $+V_{sat}$ and $-V_{sat}$.

Case-1 :- $V_{in} > V_{ref}$

$V_{in} = 5V$

$V_{ref} = 0.3V$

$V_{id} = V_{in} - V_{ref}$

$= 5 - 0.3 = 4.7V$

$V_{id} = +Ve$

$V_o = +Ve$

$\boxed{V_o = +V_{sat}}$

Case-2 :- $V_{in} < V_{ref}$

$V_{ref} = 0.3$

$V_{in} = 0.1$

$V_{id} = V_{in} - V_{ref}$

$= 0.1 - 0.3 = -0.2$

$V_{id} = -Ve$

$V_o = -Ve$

$\boxed{V_o = -V_{sat}}$

Case (iii):-

$V_{in} = V_{ref}$

$V_{id} = V_{in} - V_{ref}$

$V_{id} = 0$

$V_0 = 0$

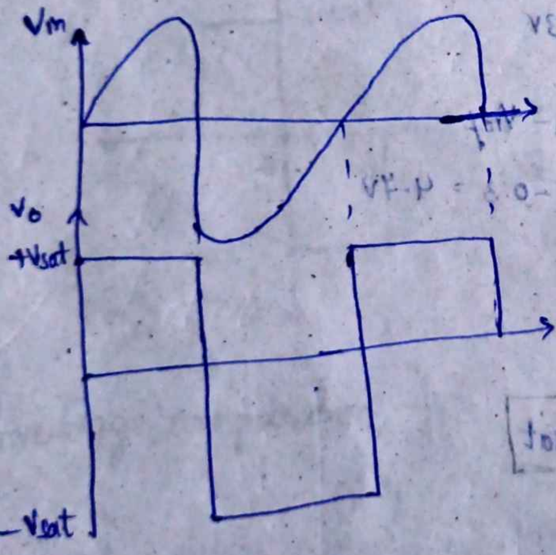
Let us assume reference voltage $= 0$

1) $V_{in} > 0$; $V_0 = +V_{sat}$

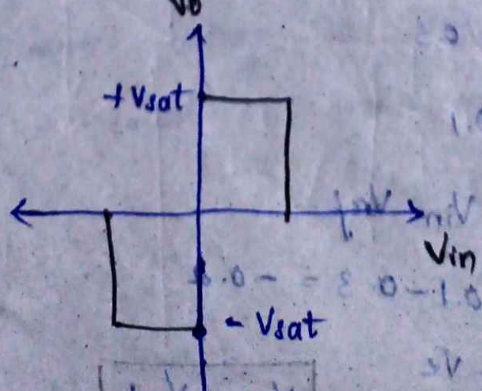
2) $V_{in} < 0$; $V_0 = -V_{sat}$

3) $V_{in} = 0$; $V_0 = 0$

Wave form:-



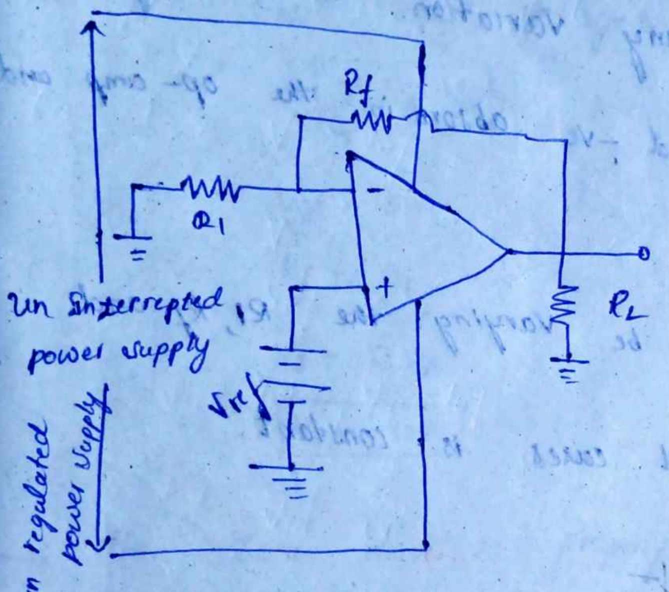
Transfer curve:-



Op-Amp as Voltage regulator:-

In Voltage regulator the output Voltage V_0 should be independent of the input valtage variation and load current variation.

→ If reference voltage is fixed then output Voltage show in the below circuit.



The gain of the non-inverting op-Amp is

$$A = 1 + \frac{R_f}{R_1}$$

$$\frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

$$\frac{V_0}{V_{ref}} = 1 + \frac{R_f}{R_1}$$

$$V_0 = \left(1 + \frac{R_f}{R_1}\right) V_{ref}$$

If $V_{ref} = 5V$

$R_f = R_1$

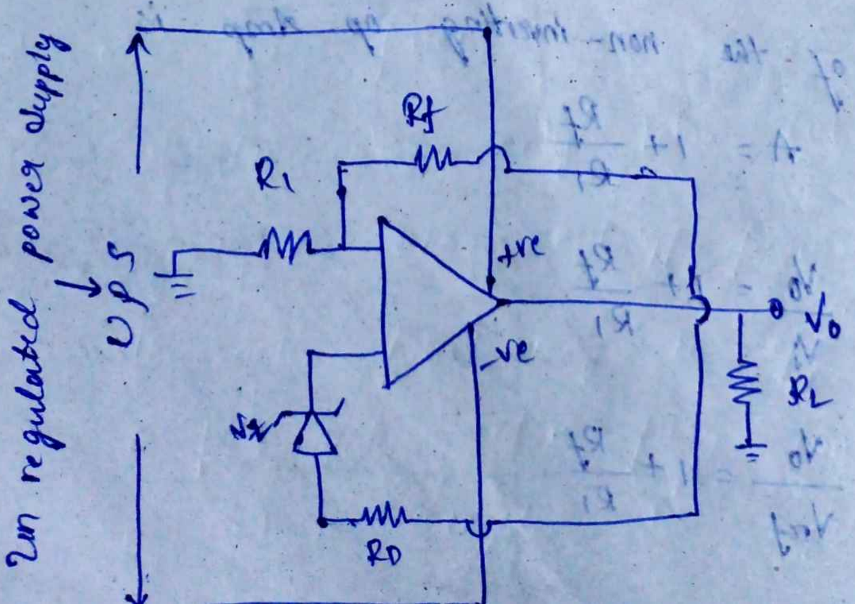
$V_0 = 2 V_{Ref}$

$V_0 = 10$.

If V_{ref} is fixed and $R_f = R_1$ the $V_0 = 2 V_{ref}$ that is the output voltage is fixed at 10 volts. and any variation in un regulated power supply +ve and -ve absorb in the op-amp and output is constant.

→ the output can be varying the R1, Rf and V_{ref} remaining all cases is constant.

With Zener diode :-



→ the above diagram shows the op-Amp as regulated circuit with Zener diode.

→ Zener diode should be made to operate only in the break down region.

→ the value of the Zener voltage (V_Z) should be less than the output voltage

$$\boxed{V_Z < V_0}$$

$V_Z = 5V$

$R_f = R_1$

$V_0 = 2V_Z$

$$\boxed{V_0 = 10V}$$

→ the Zener diode is properly loaded a given fixed voltage (V_Z) to the non-inverting terminal

→ hence, output voltage is fixed at $2V_Z$ by eliminating any variations in the output due to supply voltage +ve and -ve and load current I_L

Active filters:- A frequency selective electric circuit that passes electrical signals of specified random frequencies and atinudes then signals of frequency outside the ~~bag~~ band is called as active filters.

→ filters may be called as active (or) passive according to the presence (or) absence of an active devices respectively

→ RC active filters:- op-amp is used as an active device while resistance and capacitense are used as passive device.

Types of filters:-

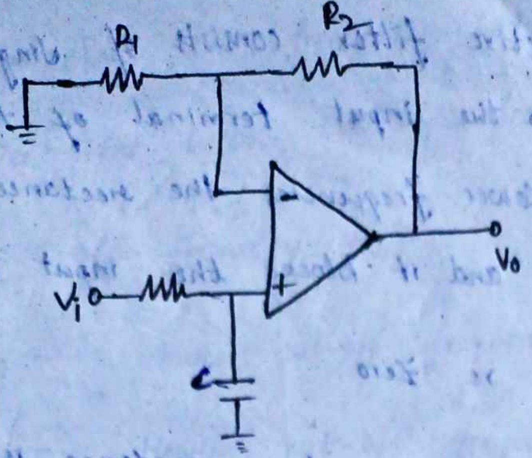
i) Low pass filter
ii) High pass filter
iii) Band pass filter

i) Low pass filter:-

→ It can allow only below cut-off frequency and reject the above cut-off frequency.

→ the active filters may be of different orders

→ A first order active filter consists of single RC Network connected to input terminal of the op-amp.



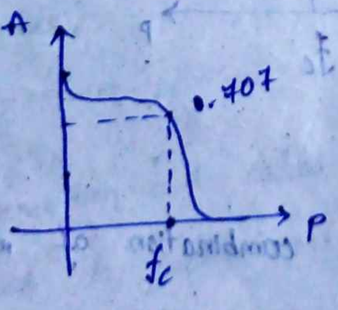
→ Capacitor reactance $X_C = \frac{1}{\omega C}$

$$X_C = \frac{1}{2\pi f C}$$

→ At low frequency capacitor appears as a open.

→ As the frequency increases capacitor rectance is increases then decreases in the voltage input.

→ Here f_c be the value of the signal frequency at which the o/p decreases to 0.707 times its low frequency value $f_c = \frac{1}{2\pi RC}$



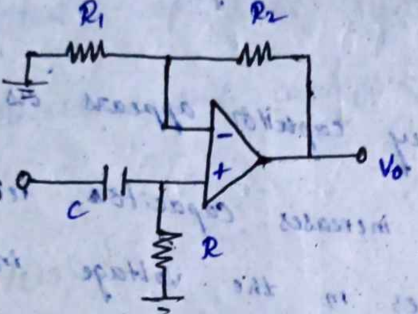
(ii) High pass filter:-

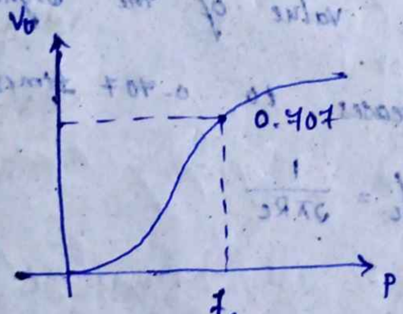
→ It can allow only above cut-off frequency and reject the below cut-off frequency.

→ A first order active filter consists of single RC Network connected to the input terminal of the op-Amp.

→ In this case at lower frequencies the reactance of capacitor is infinite and it blocks the input signal. Hence the output is zero.

→ Increasing the frequency capacitive reactance is decreases and output is Increases.





Band filters:-

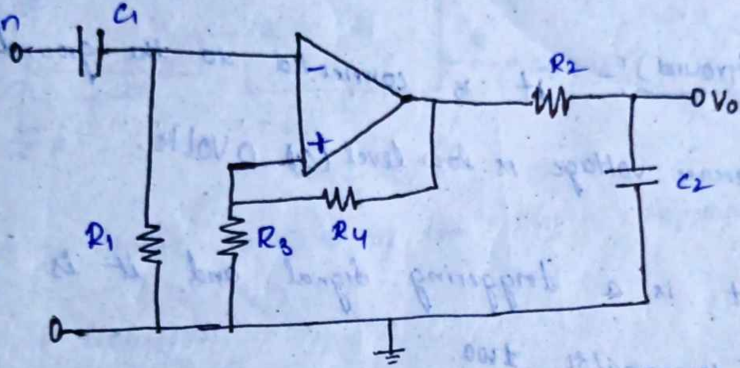
→ Band filter is the combination of low pass filter and high pass filter.

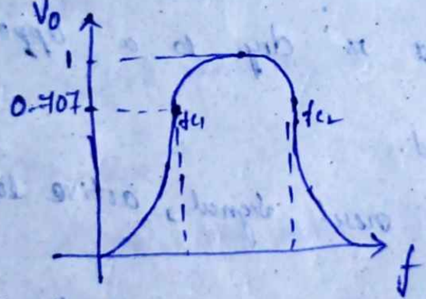
→ It can allow only certain band of frequencies and ~~remain~~ reject the remaining band of the frequency.

→ It can allow the frequency between f_{c_1} and f_{c_2} and reject the below cut-off frequency f_{c_1} and above cut-off frequecy f_{c_2}

f_{c_1} → Lower cut-off frequency

f_{c_2} → Higher cut-off frequency.





555-IC Timer:-

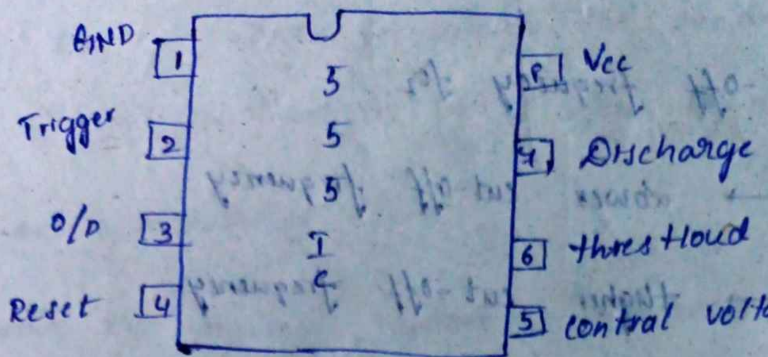
→ If ~~the~~ 555 timer is an integrated circuit used in ~~oscil~~ osllations applications. Timer pulse generation and Time delay.

→ It is used to provide the Time delay.

→ It is an 8-pin IC developed by using, C-MOS technology

→ A 555 timer can be used to modulate the signals and create accurate clock signals, create pulse with modulated signals.

Pin diagram of 555 Ic :-



PIN (I) (Ground) :- It is connected to the ground the ground reference voltage is low level (or) 0 volts.

PIN II :- It is a triggering signal and it is inverting input of comparator two.

PIN III :- the output is dry to a approximately 0.707 below Vcc (on ground.

PIN IV :- It is a reset signal, active low signal (0)

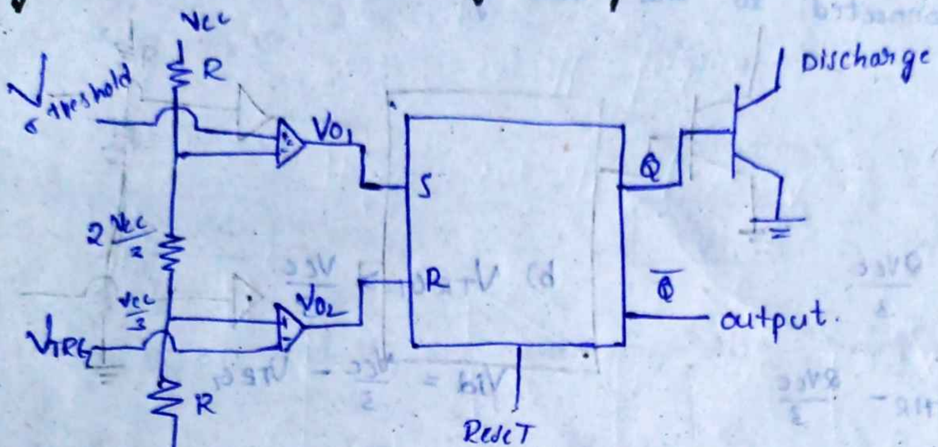
PIN V :- provides control accross to the internal voltage divider $\frac{2}{3}$th of Vcc

PIN VI :- (threshold) :- It is a non- inverting input of comparator.

PIN VII (Discharge) :- open collector output which may discharge a ~~they~~ capacitor b/w intervals.

PIN VIII (V_{cc}) :- It is a +ve supply voltage b/w the 3V & 15V depending upon the ~~variants~~. Variations.

functional block diagram of 555 IC :-



→ 555 IC timer consists of the two comparators, 1 SR-flipflop, 1 transistor.

→ the inputs to the comparator 1, is $V_{theshold}$ and $\frac{2V_{cc}}{3}$ and its output is V_{o1} then it is connected to the input to the SR flip-flop.

→ the inputs to the comparator $\frac{2V_{cc}}{3}$, V_{trg} and its output is V_{o2} then it is connected to the input of SR-flip flop

S	R	Q	$\bar{Q}$
0	0	m.s	
0	1	0	1 (ReseT)
1	0	1	0 (SeT)
1	1	IV	

→ the outputs of SR flipflop is Q and $\bar{Q}$.

→ the 555 timer IC can be taken at $\bar{Q}$.

→ Q is connected to the base of the transistor

Working:-

case ①:-

a) $V_{THR} > \frac{2V_{cc}}{3}$

$V_{id} = V_{THR} - \frac{2V_{cc}}{3}$

$V_{id} = +ve$

$V_{o1} = +ve$

$\boxed{V_{o1} = +ve}$

b) $V_{TRIG} > \frac{V_{cc}}{3}$

$V_{id} = \frac{V_{cc}}{3} - V_{TRIG}$

$V_{id} = -V_{c}$

$V_{o2} = -ve$

$\boxed{V_{o2} = -ve}$

→ $V_{o1} = 1$, and $V_{o2} = 0$ then inputs to the SR flipflop is $S = 1$, $R = 0$

→ If $S = 1$, $R = 0$ then SR-flip flop is in "SET condition" that $Q = 1$ and $\bar{Q} = 0$

→ $\bar{Q}$ is the 555 timer output that is Zero.

→ Q is connected to the base of the transistor then transistor is in saturation region. It will be acts a short circuit and Q ~~sat~~ is connected to the ground they output is Zero. then capacitor is Zero.

Case 2 :-

a) $V_{thR} < \frac{2V_{CC}}{3}$

$V_{id} = V_{thR} - \frac{2V_{CC}}{3}$

$V_{id} = -ve$

$V_{o1} = -ve$

$\boxed{V_{o1} = 0}$

b) $V_{TRG} < \frac{V_{CC}}{3}$

$V_{id} = \frac{V_{CC}}{3} - V_{TRG}$

$V_{id} = +ve$

$V_{o2} = +ve$

$\boxed{V_{o2} = 1}$

→ If $V_{o1} = 0$ and $V_{o2} = 1$ ~~then~~ are the inputs of SR-flip flop then its outputs are $Q = 0$, $\bar{Q} = 1$

→ the 555 timer IC output is $\bar{Q}$ that is 1.

→ If $Q = 0$. It is connected to the base of the transistor then transistor is in cut-off region and it is acts a open circuit voltage will be existing at the open circuited terminal. then output = 1.

Applications :-

→ Temparature, measurement and control devices

→ Traffic signal light control circuits.

→ It is used to make an alarm circuit.

→ used in digital counter circuit.

→ pulse generation, time delay generation, voltage controlled osillations, frequency division applications.

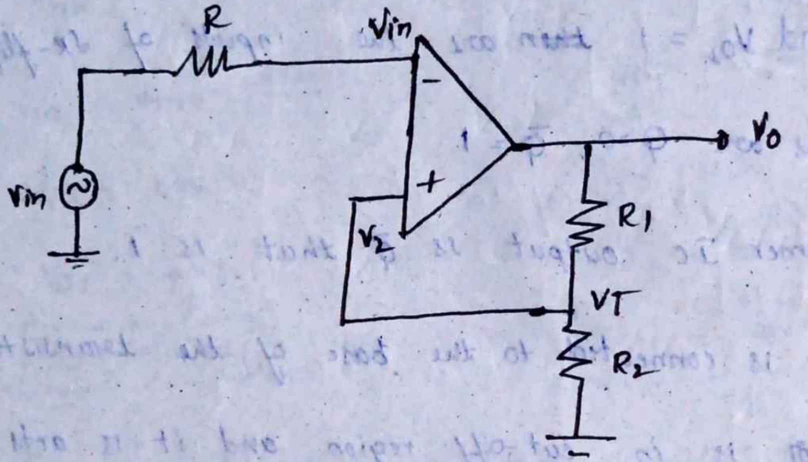
→ All electronic projects.

Square wave generator:-

It is also called as Schmitt trigger.

→ If positive feedback is added to the comparator circuit then it is set to be Schmitt trigger (or) Square wave generator.

→ It is also called Re-generatic comparator.



→ Some position of the output will go back to the input.

Now, voltage dividend rule at $V_T = \frac{V_0 R_2}{R_1+R_2}$

Case-1):- $V_{in} > V_T$

$V_{id} = V_T - V_{in}$

$V_{id} = -Ve$

$V_0 = -Ve$

$V_0 = -V_{sat}$

case (ii) :- $V_{in} < V_T$

$V_{id} = V_T - V_{in}$

$V_{id} = +ve$

$V_0 = +ve$

$V_0 = +V_{sat}$

→ If $V_0 = +V_{sat}$ then ~~theriold~~ thersold voltage is called as upper thersold potential.

$V_0 = +V_{sat}$

$$V_T = \frac{R_2}{R_1+R_2}(+V_{sat})$$

$$V_{UTP} = \frac{R_2}{R_1+R_2}(+V_{sat})$$

→ If $V_0 = -V_{sat}$ then thersold voltage is called as lower thesold potential.

$V_0 = -V_{sat}$

$$V_T = \frac{R_2}{R_1+R_2}(-V_{sat})$$

$$V_{LTP} = \frac{R_2}{R_1+R_2}(-V_{sat})$$

→ the difference between the upper thersold potential and lower thersold potential is called as Hystensis

$$V_H = V_{UTP} - V_{LTP}$$

$$V_H = \frac{R_2}{R_1+R_2}(+V_{sat}) - \frac{R_2}{R_1+R_2}(-V_{sat})$$

$$V_H = \frac{R_2}{R_1+R_2}(2V_{sat})$$

(i) $V_{in} > V_{UTP}$; $V_o = -V_{sat}$

(ii) $V_{in} < V_{UTP}$; $V_o = +V_{sat}$

(iii) $V_{in} > V_{LTP}$; $V_o = +V_{sat}$

(iv) $V_{in} < V_{LTP}$; $V_o = -V_{sat}$.

<u>Example</u> :- (iii) $V_{in} = -5$ and $V_{LTP} = -3$

NOW $V_{id} = V_{LTP} - V_{in}$

$= -3 - (-5)$

$= +2$