Semester: III						
FOUNDATIONS OF COMPUTER SYSTEMS DESIGN (Theory and Practice)						
Course Code	:	21CS34		**CIE**	:	100+50 Marks
Credits: L:T:P	:	3:0:1		**SEE**	:	100+50 Marks
Total Hours	:	45L+30P		**SEE Duration**	:	3Hours + 3Hours

Unit-I	**8 Hrs**
Introduction-Perspectives **Business Domains & Applications:** Semiconductors as an essential component of electronic devices and its advances in **communications, computing, healthcare, military systems, transportation, clean energy**, and countless other applications. Arithmetic and Logic Design Using Combinational Circuits **Arithmetic:** Addition and Subtraction of Signed Numbers, Multiplication of Unsigned Numbers, Multiplication of Signed Numbers, Fast Multiplication, Bit-Pair Recoding of Multipliers, Integer Division, Floating-Point Numbers and their single and double precision representation. **Logic Design with MSI Components**: Karnaugh Maps to obtain minimal Expressions for Complete Boolean and Incomplete Boolean Expressions, Binary Adders, Subtracters, Comparators, Decoders, Encoders, Multiplexers	
Unit – II	**10 Hrs**
Logic Design Using Sequential Circuits **Flip-Flops and Applications**: The Basic Bistable Elements, Latches, Timing Considerations, Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops), Edge – Triggered Flip-Flops, Characteristic Equations, Registers - SISO, SIPO, PISO, PIPO and Universal Shift Register. **Counters:** Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous Counters and Self-Correcting Counters	
Unit –III	**10 Hrs**
Study and design of Synchronous Sequential Networks **Synchronous Sequential Networks**: Structure and operation of Clocked synchronous Sequential Networks, Analysis of Clocked Synchronous Sequential Networks, Modelling clocked synchronous sequential network behavior, State Table Reduction, The State Assignment, Completing the design of clocked synchronous sequential networks.	
Unit –IV	**10 Hrs**
Structure of Computers and Instruction Set Architecture **Basic Structure of Computers**: Functional Units, Basic Operational Concepts, Performance – Technology and Parallelism. **Instruction Set Architecture**: Memory Locations and Addresses, Memory Operations, Instructions and Instruction Sequencing, Addressing Modes, Assembly Language- Assembler Directives, Assembly and Execution of Programs. Stacks, Subroutines- Subroutine Nesting and the Processor Stack, Parameter Passing, The Stack Frame.	
Unit –V	**7 Hrs**
Memory System & Basic Processing Unit **The Memory System**: Basic Concepts, Semiconductor RAM Memories, Cache Memories- Mapping Functions, Examples of Mapping Techniques, Performance Considerations. **Basic Processing Unit**: Fundamental Concepts, Instruction Execution, Hardware Components, Instruction Fetch and Execution Steps, Multiple-Bus Organization, Control Signals, Hardwired Control, Basic organization of a Microprogrammed Control Unit.	

Course Outcomes: After completing the course, the students will be able to:-	
CO 1	Apply design requirements for digital systems and Computer organization
CO 2	Analyse the models used for designing various combinational and sequential circuits
CO3	Design optimized modern processors and memories for given specifications
CO 4	Develop applications of synchronous sequential networks using flip flop and registers.
CO5	Investigate techniques of digital system design for building industry relevant real-world systems using electronic components and modern tools
CO6	Indulge in developing novel interdisciplinary projects with effective oral and written communication skills

Reference Books	
1.	Computer Organization and Embedded Systems , Carl Hamacher, ZvonkoVranesic, SafwatZaky, NaraigManjikian, Mc Graw Hill, 6th Edition, 2012, ISBN-13: 978-0-07-338065-0
2.	Digital Principles and Design, Donald D.Givone, Tata McGraw-Hill, 2003 , ISBN-13: 0-07- 252503-7
3.	Computer Organization and Design, David A. Patterson and John L. Hennessy, Elsevier, 5th Edition, 2014, ISBN-13: 978-0-12-407726-3.
4.	Digital Principles and Applications, Donald P Leach, Malvoni, GautamSaha Tata McGraw Hill, 7th Edition 2010, ISBN-13: 978-0070141704.

Laboratory Component

PART A (Design & Construction of Combinational & Sequential Circuits)

1A. Realization of Excess-3 Code converter with Parallel Adder and Subtractor using 4-bit adder, using the IC – 74283.

B. Realization of Binary to Gray Code Converter using decoders, using the IC 74139.

2. Realization of Full Adder and Full Subtract or using Multiplexers, using IC 74153.

3. Design and realization One Bit and Two-Bit Magnitude Comparator using logic Gates.

4A. Realization of single digit Seven segment display using the BCD to seven segment decoders, using the IC–7447.

B. Realization of Priority Encoder using IC–74147.

5. Design and Realization of Master-Slave JK Flip Flop using only NAND Gates.

6A. Realization of Synchronous Up-Down programmable counter using IC 74192.

B. Realization of Asynchronous decade counter and its variations using IC 7490.

7A. Realization of Ring counter and Johnson counter using IC 7495.

B. Design and realization of sequence generator using IC 7495.

8. Design of Mod-N Synchronous Up counters using IC 74112.

Note: Experiments & ICs indicated can be changed based on the availability and relevance

PART B - Innovative Experiments (IE) / Open Ended Experiments

Design a 4/8-bit CPU using the LOGISIM simulator, for the following specifications.

- Program Counter (Assume 256 program/code memory)
- Instruction Register (Assume instruction size as 16 bit)
- General Purpose Registers (RISC type-R0-R7): Use Harvard & Multiple Bus Architecture
- ALU (to support 4-bit integer arithmetic operations & 4-bit logical operations)
- Memory – 1024 ROM (to store instructions of size 16 bit) and 256 RAM (to store 4-bit data)
- Implement the following instructions namely: MOV, ADD, SUB, LOAD, STORE, AND, XOR, NOT, BRANCH, BRANCH ON CONDITION.
- Result to be displayed on 7-segment displays / reg tab of LOGISIM

ASSESSMENT AND EVALUATION PATTERN		
	CIE	**SEE**
WEIGHTAGE	**50%**	**50%**
QUIZZES		
Quiz-I	Each quiz is evaluated for 10 marks adding up to **20 MARKS.**	
Quiz-II		
THEORY COURSE (Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analysing, Evaluating, and Creating)		
Test – I	Each test will be conducted for 50 Marks adding upto 100 marks. Final test marks will be reduced to **40 MARKS**	
Test – II		
EXPERIENTIAL LEARNING	**40**	
Case Study-based Teaching-Learning (Study & Dissemination of Published articles related to state of the art work in the fields of semiconductors, computer architecture, memories etc)	**10**	
Building Prototypes: Students to design & demonstrate prototypes of Smart Systems, IoT Applications etc, which involves integration of Hardware & Software.	**20**	
Participation and winning in Hackathons / Paper Presentations /Journal Publications / Course Material Preparation-Videos/Animations/AR-VR tools	**10**	
MAXIMUM MARKS FOR THE THEORY	**100 MARKS**	**100 MARKS**
PRACTICALS	**50***	**50***
TOTAL MARKS FOR THE COURSE	**150**	**150**

Guidelines for Conducting CIE Laboratory / Practical's:

Sl.No	Contents	Marks
1	Write-Up, Conduction of Experiment & Record Writing	30
2	Design a 4/8-bit CPU using the LOGISIM/any other simulator	10
3	Lab Exam (WriteUp-2M, Conduction-6M, Viva-2M)	10
	Total:	**50**

Guidelines for Conducting SEE Lab Exam:

Sl.No	Contents	Marks
1	Write-Up and Conduction of Part A Experiment	30
2	Demonstration of CPU design on Logisim simulator & Viva.	20
	Total:	**50**