KLS GOGTE INSTITUTE OF TECHNOLOGY BELAGAVI-08

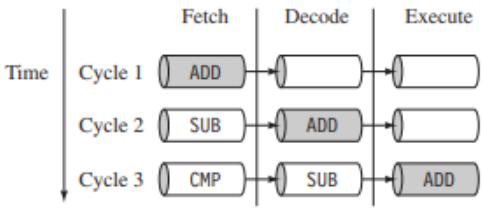
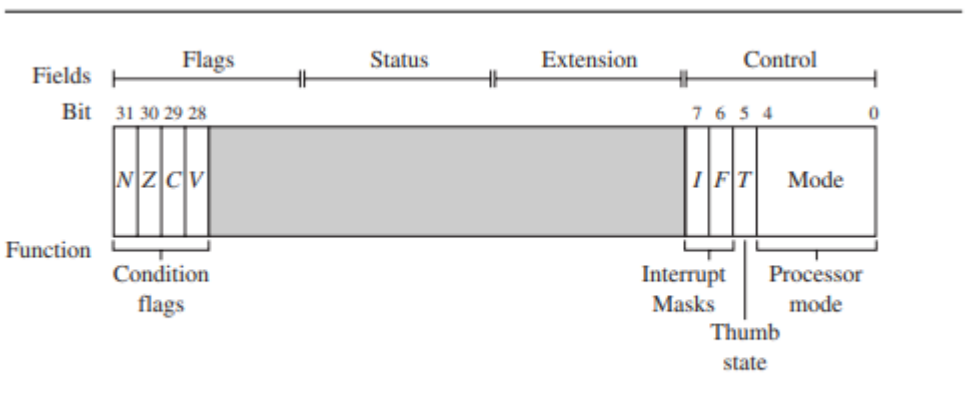
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

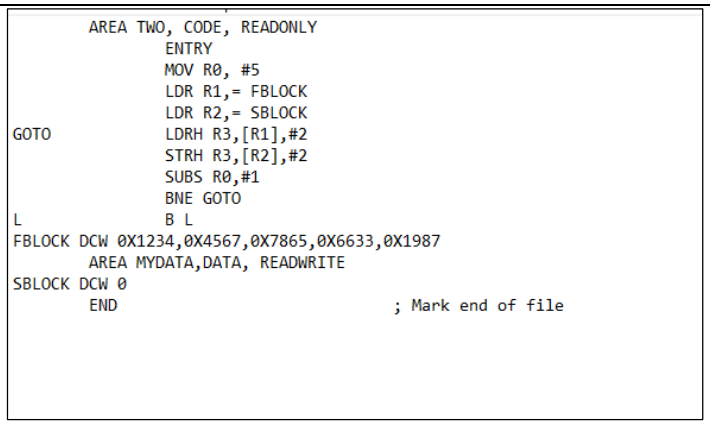
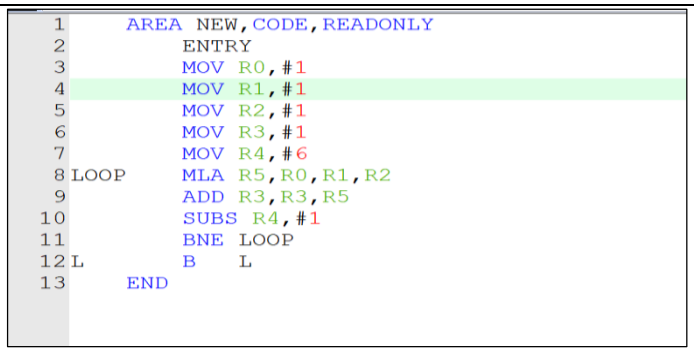
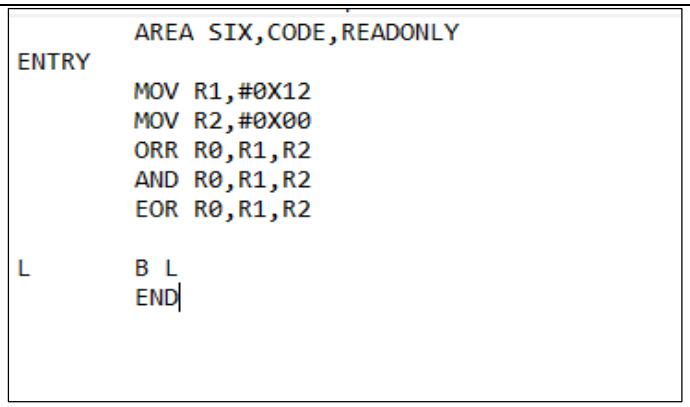
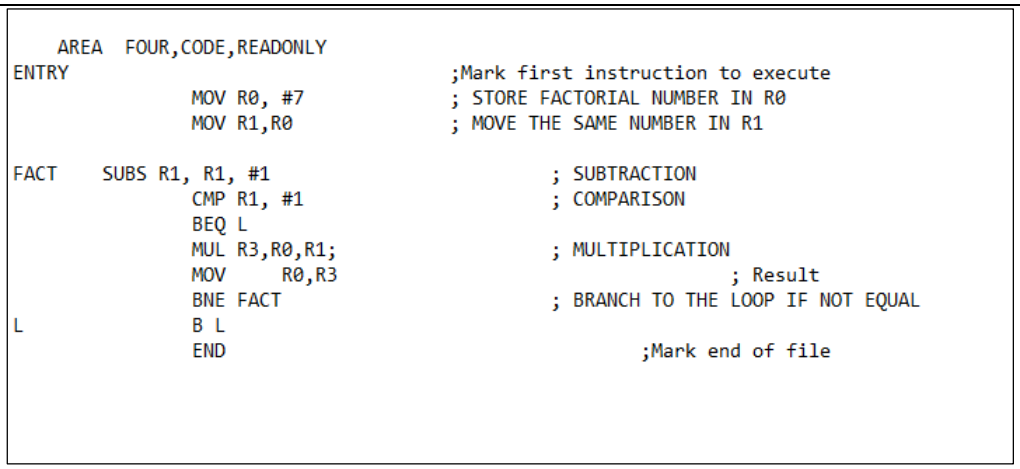
**IA TEST SCHEME OF EVALUATION**

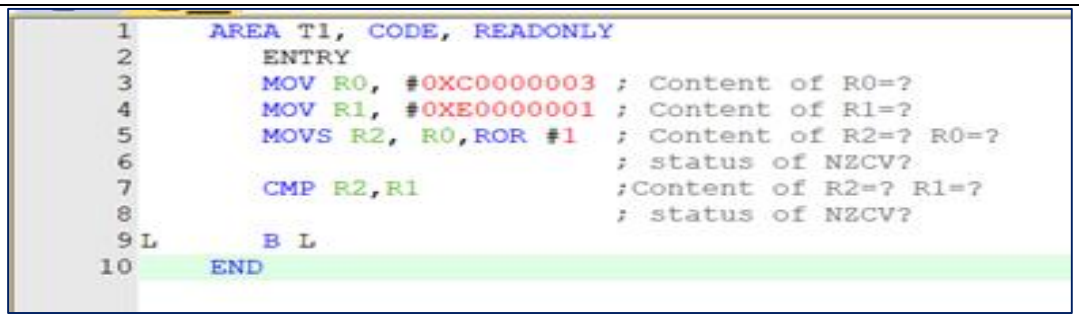
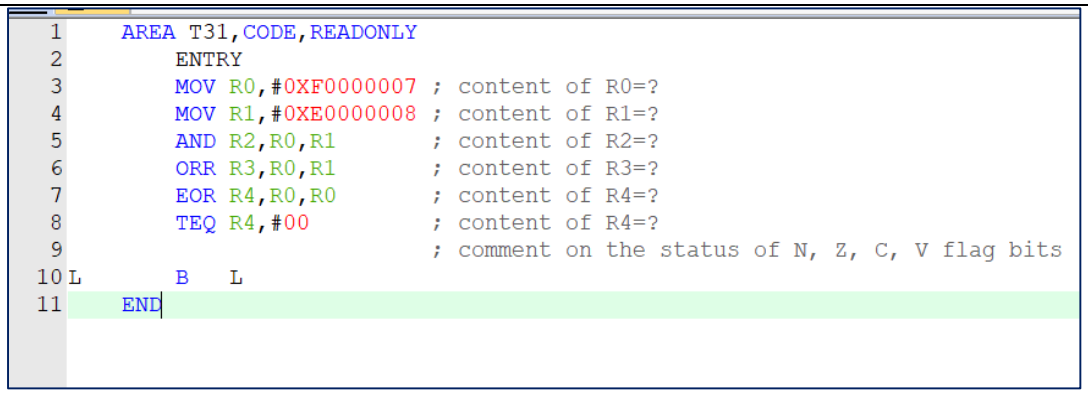
**ACADEMIC YEAR 2023-24**

| | | |
|---|---|---|
| **DATE: 05/12/2023** | **IA TEST: I** | **MARKS** |
| **SUBJECT: MICROCONTROLLERS AND EMBEDDED SYSTEMS** | | |
| **SUBJECT CODE: 21CS53** | | |

**PART A**

| | | |
|---|---|---|
| **1.** | A pipeline is the mechanism a RISC processor uses to execute instructions. Using a pipeline speeds up execution by fetching the next instruction while other instructions are being decoded and executed. | **1 M** |
| |  Figure 2.8 Pipelined instruction sequence. | **2 M** |
| | **Explanation** | **2M** |
| **2.** |  A generic program status register (*psr*). | **3 M** |
| | a. SUBS R0, R1, R1; Zero flag is affected as R1-R1 is zero<br>b. CMP R2, R3; R2=0x20 and R3=0x50; Negative flag is affected as R2-R3 is | **1M+1M** |

| | | |
|---|---|---|
| | negative | |
| | **PART B** | |
| **3.** |  | **5 M** |
| **4.** |  | **5 M** |
| **5.** |  | **5 M** |
| **6.** |  | **5 M** |

| PART C | | |
|---|---|---|
| **7.** |  <br>**R0=0XC0000003**<br>**R1=0XE0000001**<br>**R2=0XE0000001, R0=0XC0000003, N=1, Z=0, C=1, V=0**<br>**R2=0XE0000001, R1=0XE0000001, N=0, Z=1, C=1,V=0** | **0.5 M**<br>**0.5 M**<br>**2 M**<br>**2 M** |
| **8.** |  <br>**R0= 0XF0000007**<br>**R1=0XE0000008**<br>**R2=0XE0000000**<br>**R3=0XF000000F**<br>**R4=0X00000000**<br>**R4=0X00000000, N=0,Z=1,C=0,V=0** | **0.5 M**<br>**0.5 M**<br>**0.5 M**<br>**0.5 M**<br>**0.5 M**<br>**2.5 M** |

```
1     AREA T1, CODE, READONLY
2         ENTRY
3         MOV R0, #0XC0000003 ; Content of R0=?
4         MOV R1, #0XE0000001 ; Content of R1=?
5         MOVS R2, R0,ROR #1  ; Content of R2=? R0=?
6                             ; status of NZCV?
7         CMP R2,R1           ;Content of R2=? R1=?
8                             ; status of NZCV?
9 L       B L
10    END
```

```
1     AREA T31,CODE,READONLY
2         ENTRY
3         MOV R0,#0XF0000007 ; content of R0=?
4         MOV R1,#0XE0000008 ; content of R1=?
5         AND R2,R0,R1       ; content of R2=?
6         ORR R3,R0,R1       ; content of R3=?
7         EOR R4,R0,R0       ; content of R4=?
8         TEQ R4,#00         ; content of R4=?
9                            ; comment on the status of N, Z, C, V flag bits
10 L      B   L
11    END
```