Perform the following procedure for initializing the SPI

- Reset the SPI by clearing the RESET bit in the SPI global control register 0 (SPIGCR0) to 0.
- Take the SPI out of reset by setting SPIGCR0.RESET to 1.
- Configure the SPI for master mode by configuring the CLKMOD and MASTER bits in the SPI global control register 1 (SPIGCR1).
- Configure the SPI for 3-pin or 4-pin with chip select mode by configuring the SPI pin control register 0 (SPIPC0).
- Choose the SPI data format register n (SPIFMTn) to be used by configuring the DFSEL bit in the SPI transmit data register (SPIDAT1).
- Configure the SPI data rate, character length, shift direction, phase, polarity and other format options using SPIFMTn.
- In master mode, configure the master delay options using the SPI delay register (SPIDELAY).
- Select the error interrupt notifications by configuring the SPI interrupt register (SPIINT0) and the SPI interrupt level register (SPILVL).
- Enable the SPI communication by setting the SPIGCR1.ENABLE to 1.
- Setup and enable the DMA for SPI data handling and then enable the DMA servicing for the SPI data requests by setting the SPIINT0.DMAREQEN to 1.
- Handle SPI data transfer requests using DMA and service any SPI error conditions using the interrupt service routine.

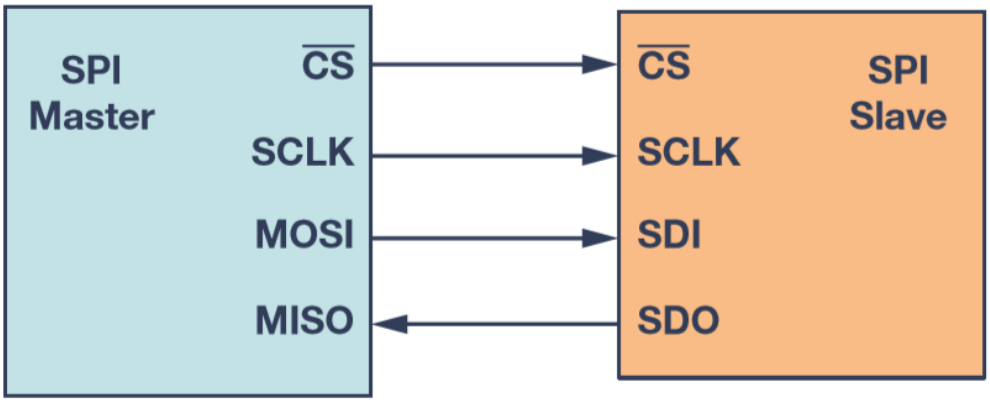

Figure SPI configuration with master and a slave.

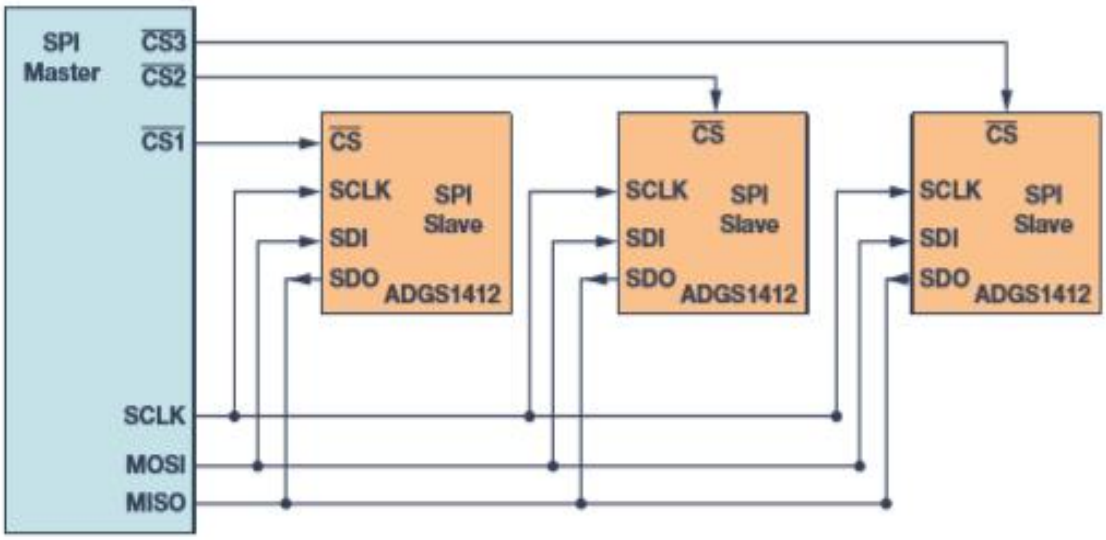

Figure . Multislave SPI configuration.

Table SPI Modes with CPOL and CPHA

SPI Mode	CPOL	CPHA	Clock Polarity in Idle State	Clock Phase Used to Sample and/or Shift the Data
0	0	0	Logic low	Data sampled on rising edge and shifted out on the falling edge
1	0	1	Logic low	Data sampled on the falling edge and shifted out on the rising edge
2	1	1	Logic high	Data sampled on the falling edge and shifted out on the rising edge
3	1	0	Logic high	Data sampled on the rising edge and shifted out on the falling edge

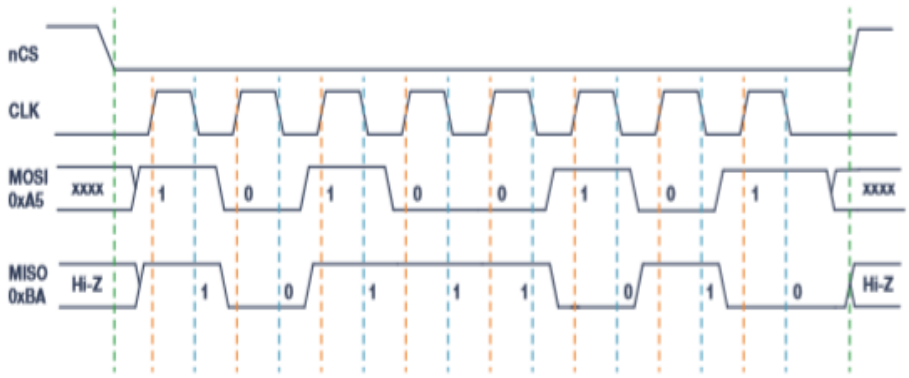

Figure 2. SPI Mode 0, CPOL = 0, CPHA = 0: CLK idle state = low, data sampled on rising edge and shifted on falling edge.

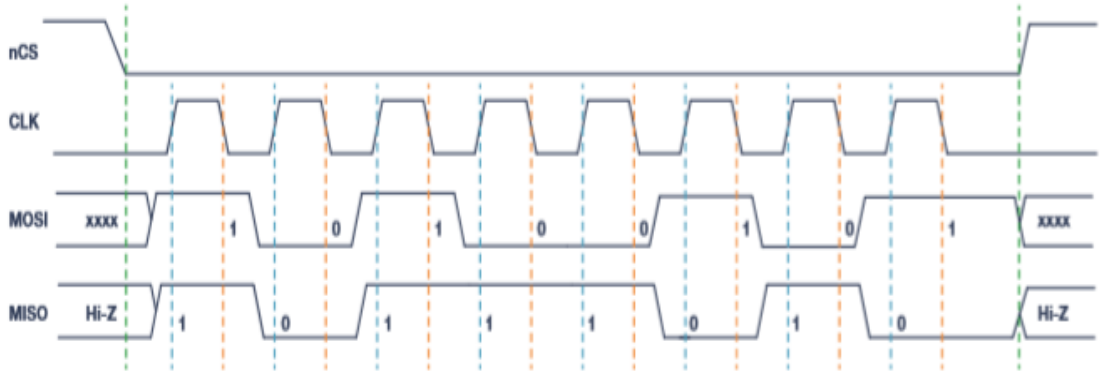

Figure 3. SPI Mode 1, CPOL = 0, CPHA = 1: CLK idle state = low, data sampled on the falling edge and shifted on the rising edge.

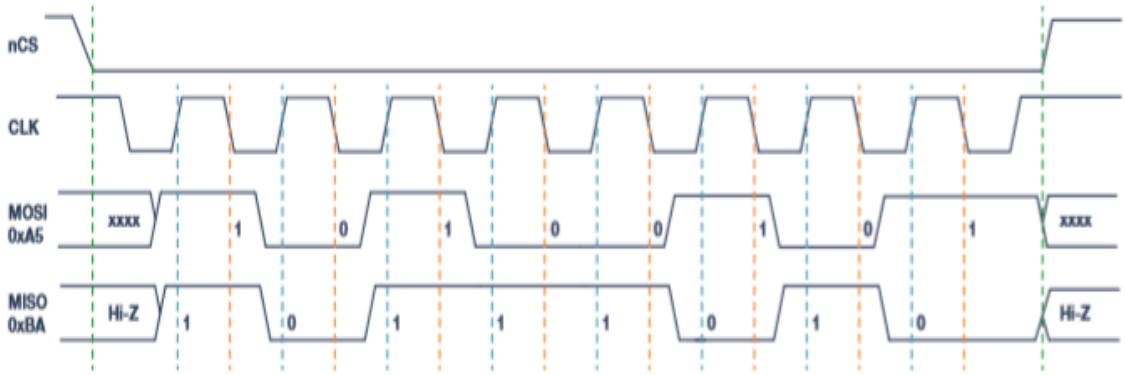

Figure 4. SPI Mode 2, CPOL = 1, CPHA = 1: CLK idle state = high, data sampled on the falling edge and shifted on the rising edge.

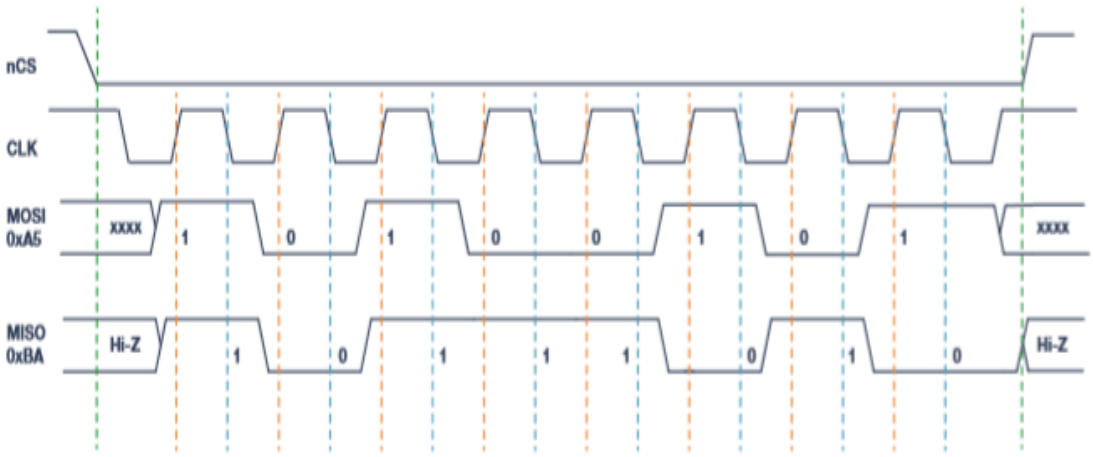

Figure 5. SPI Mode 3, CPOL = 1, CPHA = 0: CLK idle state = high, data sampled on the rising edge and shifted on the falling edge.