TRANSITIONING Si4430/31 FROM REV A0 TO REV B

1. Purpose and Overview

The purpose of this document is to describe the changes between Revisions A0 and B to assist in the transition to the new revision. Pinout, TX/RX matching, register modifications, and overall performance improvements are discussed in this document.

The Si4431 Revision B addresses the errata items associated with Revision A0 and improves the synthesizer spurious performance. All errata items for Revision A0 are solved with the exception of some sensitivity desense on frequencies that are multiples of 30 MHz and a required register modification for data rates higher than 100 kbps. Both of these items are covered in the Rev B data sheet.

2. Pinout Changes

The pinout changes from A0 to B are minor and do not require a PCB board modification to transition to the new revision. Figure 1 illustrates the changed pins highlighted in red. Pin 5 previously required an external 1 µF decoupling capacitor. This capacitor has been integrated, and the pin is not bonded to the device; so, connecting to Pin 5 will have no effect. Pin 6 is added to provide a control signal for a TX/RX switch to conserve the GPIO for other uses. Ant1 is a hardwired digital output equivalent to GPIO setting 10111, Antenna 1 Switch.

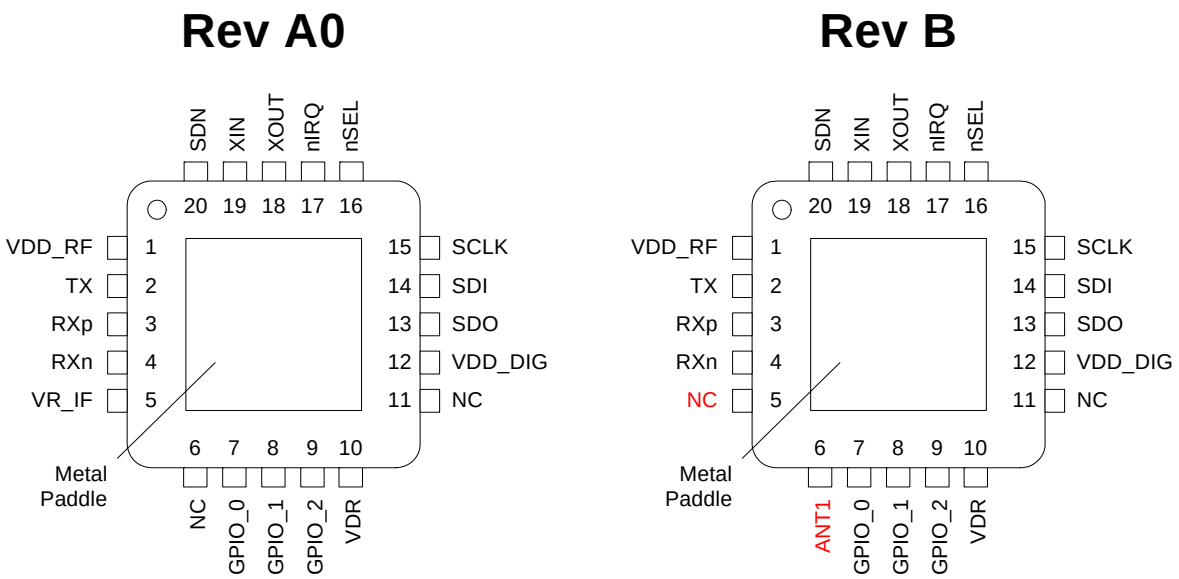

Figure 1. Pinout Changes

3. TX and RX Matching Components

The same matching structure and component values may be used for the Revision B receive match.

The same transmit match structure recommended in the Si4431 data sheet may still be used, but a change in component values is required. For a complete PA matching discussion, see “AN436: Si4030/4031/4430/4431 PA Matching.”

4. Register Changes

The Revision A0 errata specified that register value changes were required for registers 57h, 59h, and 5Ah. In Revision B, the default values of these registers have been changed and should no longer be altered.

All RX modem settings should be configured per the register calculator specific to Revision B, Si443x Register Settings_Rev B1-Vx.xls. The latest calculator may be downloaded from the Silicon Labs website: www.silabs.com. Table 1 highlights the modified registers. The calculator provides proper settings for all new or modified registers.

Table 1. Modified Registers from V2 to B

Add	R/W	Function/ Description	Data								POR Default
1E	R/W	AFC Timing Control	swant_ timer[1]	swant_ timer[0]	shwait[2]	shwait[1]	shwait[0]	anwait[2]	anwait[1]	anwait[0]	0Ah
21	R/W	Clock Recovery Offset 2	rxosr [10]	rxosr[9]	rxosr[8]	stallctrl	ncoff[19]	ncoff[18]	ncoff[17]	ncoff[16]	01h
24	R/W	Clock Recovery Timing Loop Gain 1				rxncocomp	cgainx2	crgain[10]	crgain[9]	crgain[8]	02h
30	R/W	Data Access Control	enpacrx	lsbfrst	crcdonly	skip2ph	enpactx	encrc	crc[1]	crc[0]	8Dh
33	R/W	Header Control 2	skipsync	hdlen[2]	hdlen[1]	hdlen[0]	fixpklen	synclen[1]	synclen[0]	prealen[8]	22h
69	R/W	AGC Override 1	Reserved	SGI	aggcen	lnagain	pga[3]	pga[2]	pga[1]	pga[0]	20h
6D	R/W	TX Power	papeakval	papeaken	papeaklvl[1]	papeaklvl[0]	lna_sw	txpow[2]	txpow[1]	txpow[0]	18h

Document Change List

Revision 0.1 to Revision 0.2

- Updated title on page 1.

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