LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT8618SX

Low Power HDMI1.4 Transmitter

Datasheet

1. Features

- **RGB Input**
  - Support 24-bit RGB，YUV and BT656/BT601/ BT1120 Input
  - Support both SDR and DDR Data Sampling
  - Programmable Rising/Falling Edge Clock Input
  - Support up to 148.5MHz DDR or 297MHz SDR Clock Input
  - Support both 1.8V and 3.3V Input Voltage Level
- **HDMI Transmitter**
  - Compliant with HDMI1.4 and HDCP1.4
  - Resolution Up to 4K 30Hz
  - Programmable output swing and pre-emphasis
  - Fully hardware-controlled or optional software-controlled HDCP operations
  - Pre-programmed HDCP key sets or external EEPROM stored key sets
  - Integrated CEC controller
  - Integrated EDID shadow RAM and embedded EDID
  - 5V tolerance DDC/HPD I/Os
- **Miscellaneous**
  - 1.8V and 3.3V Power Supply
  - Support 100KHz and 400KHz I2C slave
  - Support up to 8-channel Audio Input
  - Temperature Range: -40°C ~ +85°C
  - Pin compatible with Sil9030，ANX9030 and CAT6612
  - Packaged in QFN64 7.5mm x 7.5mm，QFP80 12mm x 12mm and QFN64 9mm x 9mm

2. General Description

The LT8618SX is Lontium's low power version HDMI transmitter based on ClearEdge™ technology. It supports the 24-bit color depth HDMI 1.4 (High Definition Multimedia Interface) specification. They are fully backwoard compatible with Lontium's first generation HDMI transmitter LT8618EX, and also pin compatible with Sil9030 and ANX9030 transmitters.

LT8618SX is a high performance, low power part that are specifically designed for HD-Digital cameras, HD-Digital Video Cameras, HD-PMP/MP4 Players, Cell phones, etc. The normal operation power is less than 100mA playing 24bit 1080P content, and the standby power is less than 2mA.

3. Applications

- DVD, BD
- Car Video Recorder
- PTV Box
- HD Source

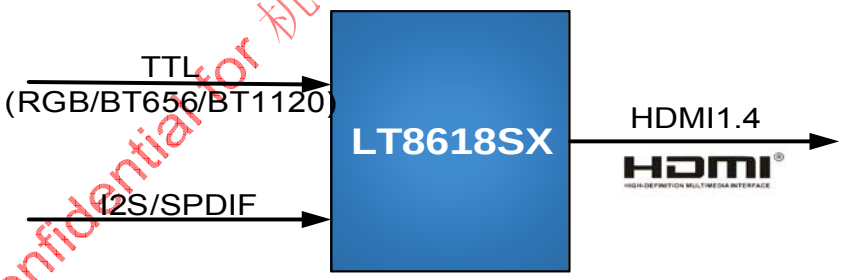

Figure 3.1 LT8618SX Typical Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT8618SXA	-40℃ to 85℃	LQFP80 (12*12)	
LT8618SXB	-40℃ to 85℃	QFN64 (9*9)	

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5. Revision History

Version	Owner	Content	Date
R1.0	Y C	Initial datasheet creation	04/05/2017
R1.1	Y C	1. Change Pin description； 2. Delete QFN64 7.5mmx7.5mm package information.	09/26/2017
R1.2	Y C	1. Add power consumption information； 2. Add ESD information.	10/27/2017
R1.3	Y C	Delete Embeded EEPROM description	02/27/2018

6. Pinning Information

6.1 Pin Configuration

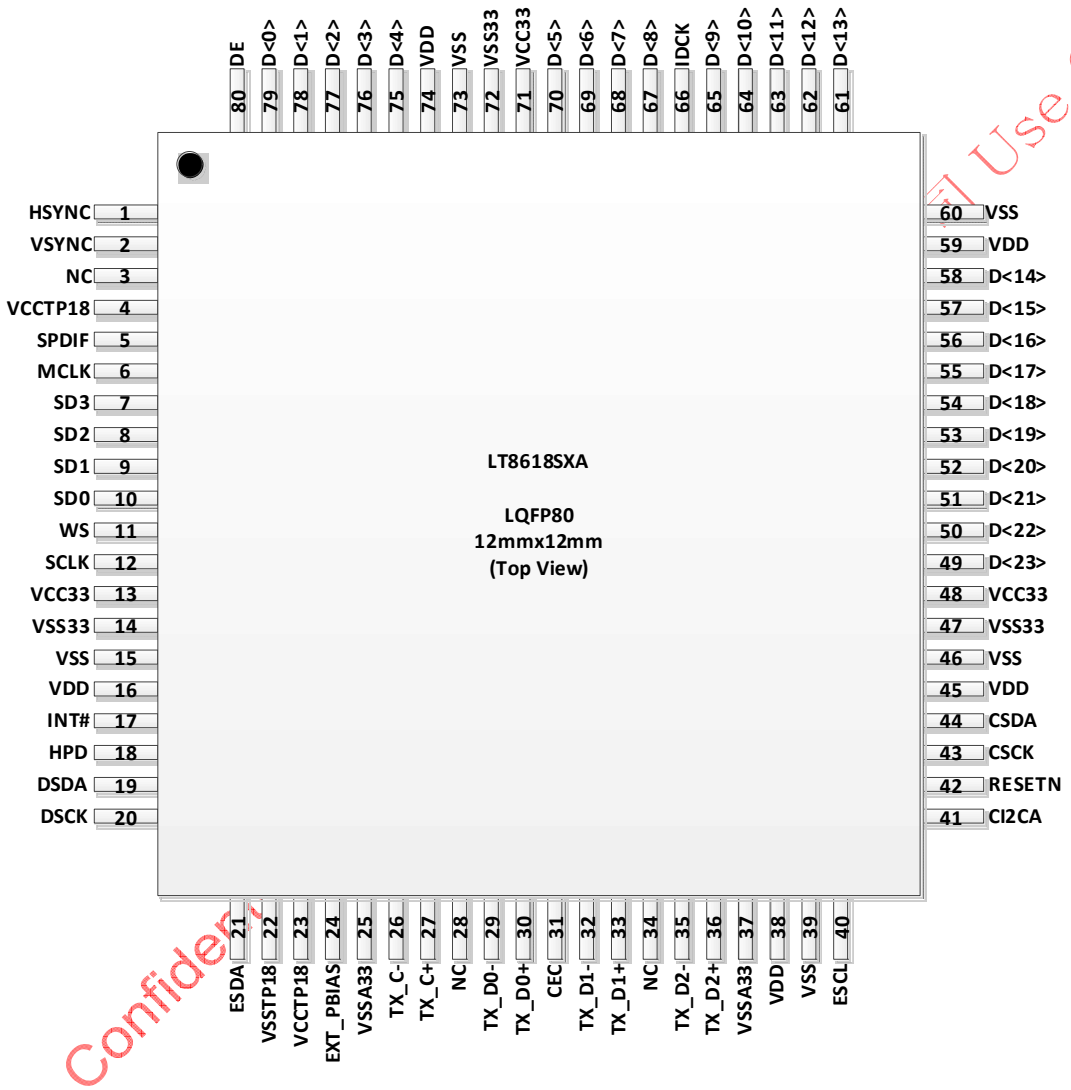


Figure 6.1.1 LT8618SXA Pin Configuration

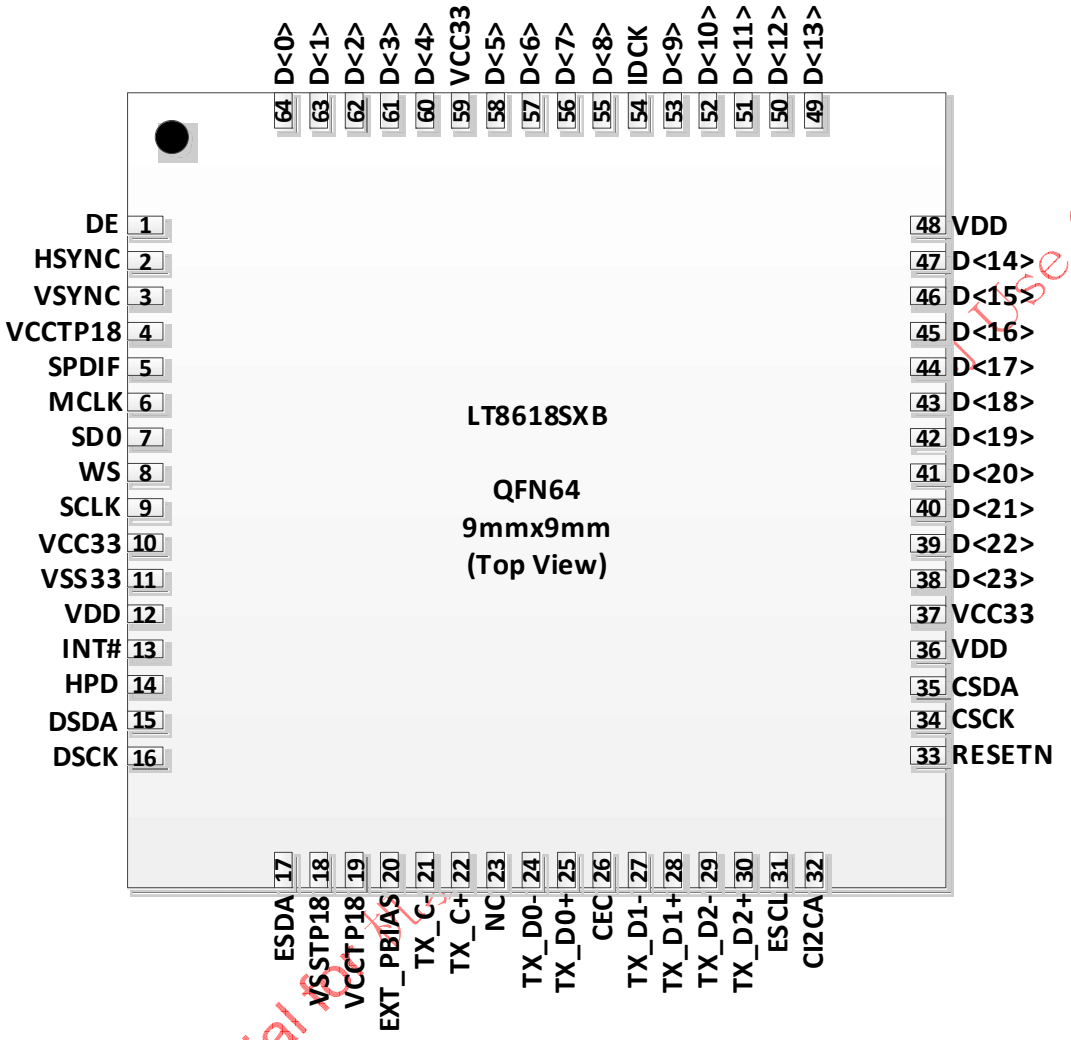


Figure 6.1.2 LT8618SXB Pin Configuration

To minimize the power supply noise floor, at least one 0.1μF and one 0.01μF decoupling capacitor is recommended to be installed near all the LT8618SX 1.8V/3.3V power pins. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power input pins must be minimized.

6.2 Pin Description

Table 6.2.1 LT8618SXA Pin Description

PIN#	PIN NAME	I/O	DESCRIPTION
1	HSYNC	I	Horizontal Sync input control signal.
2	VSYNC	I	Vertical Sync input control signal.
3	NC	---	
4	VCCTP18	AP	TMDS PLL power. Connect to 1.8V supply.
5	SPDIF	I	S/PDIF Audio Input or master clock input for IIS master mode.
6	MCLK	I	Audio Input Master Clock for IIS slave mode.
7	SD3	I	I2S Serial Data.
8	SD2	I	I2S Serial Data.
9	SD1	I	I2S Serial Data.
10	SD0	I	I2S Serial Data.
11	WS	IO	I2S Word Select Input (IIS slave mode) or Output (IIS master mode).
12	SCLK	IO	I2S Serial Clock Input (IIS slave mode) or Output (IIS master mode).
13	VCC33	P	I/O pin VCC33. Connect to 3.3V supply.
14	VSS33	G	I/O pin GND.
15	VSS	G	Digital Core GND.
16	VDD	P	Digital Core VDD. Connect to 1.8V supply.
17	INT#	O	Interrupt output. Configurable by resistor setting. To be either push-pull output or open-drain output.
18	HPD	I	Hot Plug Detect input.
19	DSDA	IO	DDC Data (open drain output).
20	DSCK	I	DDC Clock.
21	ESDA	IO	EEPROM I2C Port. This port is dedicated to loading HDCP Key Sets.
22	VSSTP18	AG	TMDS PLL GND.
23	VCCTP18	AP	TMDS PLL power. Connect to 1.8V supply.
24	EXT_PBIAS	IO	Connecting this pin through a 2k resistor (±1%) to VSSA33 is recommended.
25	VSSA33	AG	Analog GND.
26	TX_C-	O	TMDS output clock pairs.
27	TX_C+	O	TMDS output clock pairs.
28	NC	---	
29	TX_D0-	O	TMDS output data pairs.
30	TX_D0+	O	TMDS output data pairs.
31	CEC	IO	CEC data bus.
32	TX_D1-	O	TMDS output data pairs.
33	TX_D1+	O	TMDS output data pairs.
34	NC	---	
35	TX_D2-	O	TMDS output data pairs.
36	TX_D2+	O	TMDS output data pairs.
37	VSSA33	AG	Analog GND.
38	VDD	P	Digital Core VDD. Connect to 1.8V supply.

PIN#	PIN NAME	I/O	DESCRIPTION
39	VSS	G	Digital Core GND.
40	ESCL	IO	EEPROM I2C Port. This port is dedicated to loading HDCP Key Sets.
41	CI2CA	I	I2C device address select.
42	RESETN	I	Reset pin (Active Low), must be controlled by a dependent I/O pin from MCU. (3.3V IO)
43	CSCK	I	Config I2C clock.
44	CSDA	IO	Config I2C data.
45	VDD	P	Digital Core VDD. Connect to 1.8V supply.
46	VSS	G	Digital Core GND.
47	VSS33	G	I/O pin GND.
48	VCC33	P	I/O pin VCC33. Connect to 3.3V supply.
49	D[23]	I	These pins are used only in 24-bit single-edge mode. In 12-bit dual-edge mode these pins should be tied to ground.
50	D[22]	I	
51	D[21]	I	
52	D[20]	I	
53	D[19]	I	
54	D[18]	I	
55	D[17]	I	
56	D[16]	I	
57	D[15]	I	
58	D[14]	I	
59	VDD	P	Digital Core VDD. Connect to 1.8V supply.
60	VSS	G	Digital Core GND.
61	D[13]	I	These pins are used only in 24-bit single-edge mode. In 12-bit dual-edge mode these pins should be tied to ground.
62	D[12]	I	
63	D[11]	I	These pins are used in 12-bit dual-edge mode and in 24-bit mode single-edge mode.
64	D[10]	I	
65	D[9]	I	
66	IDCK	I	Input data capture clock.
67	D[8]	I	These pins are used in 12-bit dual-edge mode and in 24-bit mode single-edge mode.
68	D[7]	I	
69	D[6]	I	
70	D[5]	I	
71	VCC33	P	I/O pin VCC33. Connect to 3.3V supply.
72	VSS33	G	I/O pin GND.
73	VSS	G	Digital Core GND.
74	VDD	P	Digital Core VDD. Connect to 1.8V supply.
75	D[4]	I	These pins are used in 12-bit dual-edge mode and in 24-bit mode single-edge mode.
76	D[3]	I	
77	D[2]	I	
78	D[1]	I	

PIN#	PIN NAME	I/O	DESCRIPTION
79	D[0]	I	
80	DE	I	Input data enable.

Table 6.2.2 LT8618SXB Pin Description

PIN#	PIN NAME	I/O	DESCRIPTION
1	DE	I	Input data enable.
2	HSYNC	I	Horizontal Sync input control signal.
3	VSYNC	I	Vertical Sync input control signal.
4	VCCTP18	AP	TMDS PLL power. Connect to 1.8V supply.
5	SPDIF	I	S/PDIF Audio Input or master clock input for IIS master mode.
6	MCLK	I	Audio Input Master Clock for IIS slave mode.
7	SD3	I	I2S Serial Data.
8	WS	IO	I2S Word Select Input(IIS slave mode) or Output(IIS master mode).
9	SCLK	IO	I2S Serial Clock Input(IIS slave mode) or Output(IIS master mode).
10	VCC33	P	I/O pin VCC33. Connect to 3.3V supply.
11	VSS33	G	I/O pin GND.
12	VDD	P	Digital Core VDD. Connect to 1.8V supply.
13	INT#	O	Interrupt output. Configurable by resistor setting. To be either push-pull output or open-drain output.
14	HPD	I	Hot Plug Detect input.
15	DSDA	IO	DDC Data (open drain output).
16	DSCK	I	DDC Clock.
17	ESDA	IO	EEPROM I2C Port. This port is dedicated to loading HDCP Key Sets.
18	VSSTP18	AG	TMDS PLL GND.
19	VCCTP18	AP	TMDS PLL power. Connect to 1.8V supply.
20	EXT_PBIAS	IO	Connecting this pin through a 2k resistor (±1%) to VSSA33 is recommended.
21	TX_C-	O	TMDS output clock pairs.
22	TX_C+	O	TMDS output clock pairs.
23	NC	---	
24	TX_D0-	O	TMDS output data pairs.
25	TX_D0+	O	TMDS output data pairs.
26	CEC	IO	CEC data bus.
27	TX_D1-	O	TMDS output data pairs.
28	TX_D1+	O	TMDS output data pairs.
29	TX_D2-	O	TMDS output data pairs.
30	TX_D2+	O	TMDS output data pairs.
31	ESCL	IO	EEPROM I2C Port. This port is dedicated to loading HDCP Key Sets.
32	CI2CA	I	I2C device address select.
33	RESETN	I	Reset pin (Active Low). (3.3V IO)
34	CSCK	I	Config I2C clock.

PIN#	PIN NAME	I/O	DESCRIPTION
35	CSDA	IO	Config I2C data.
36	VDD	P	Digital Core VDD. Connect to 1.8V supply.
37	VCC33	P	I/O pin VCC33. Connect to 3.3V supply.
38	D[23]	I	These pins are used only in 24-bit single-edge mode. In 12-bit dual-edge mode these pins should be tied to ground.
39	D[22]	I	
40	D[21]	I	
41	D[20]	I	
42	D[19]	I	
43	D[18]	I	
44	D[17]	I	
45	D[16]	I	
46	D[15]	I	
47	D[14]	I	
48	VDD	P	Digital Core VDD. Connect to 1.8V supply.
49	D[13]	I	These pins are used only in 24-bit single-edge mode. In 12-bit dual-edge mode these pins should be tied to ground.
50	D[12]	I	
51	D[11]	I	These pins are used in 12-bit dual-edge mode and in 24-bit mode single-edge mode.
52	D[10]	I	
53	D[9]	I	
54	IDCK	I	Input data capture clock.
55	D[8]	I	These pins are used in 12-bit dual-edge mode and in 24-bit mode single-edge mode.
56	D[7]	I	
57	D[6]	I	
58	D[5]	I	
59	VCC33	P	I/O pin VCC33. Connect to 3.3V supply.
60	D[4]	I	These pins are used in 12-bit dual-edge mode and in 24-bit mode single-edge mode.
61	D[3]	I	
62	D[2]	I	
63	D[1]	I	
64	D[0]	I	

7. Function Description

7.1 Function Block Diagram

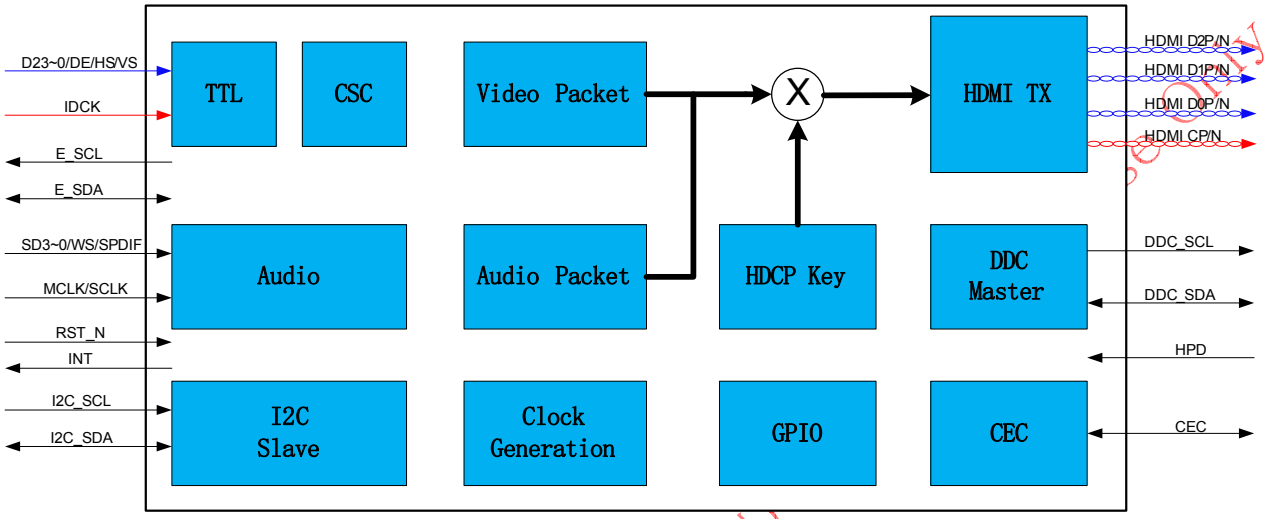


Figure 7.1.1 Function Block Diagram

7.2 Detailed Description

7.2.1 Data Bus Mappings

The LT8618SX supports multiple input data mappings. Some have explicit control signals. Some have embedded control signals. The selection of data mapping mode should be consistent at the pins and in the corresponding register settings.

The video capture logic receives the video data from the 24-bit video interface. The interface is configured by registers to set the bus width and format as well as rising and falling edge latching. Several video input formats are supported; these and their respective pixel bit mapping are listed in the following figures.

Table 7.2.1.1 RGB and YCbCr 4:4:4 Formats with Separate Syncs

Pin Name	24-bit RGB	24-bit YCbCr
D0	B0	Cb0
D1	B1	Cb1
D2	B2	Cb2
D3	B3	Cb3
D4	B4	Cb4
D5	B5	Cb5
D6	B6	Cb6
D7	B7	Cb7
D8	G0	Y0
D9	G1	Y1
D10	G2	Y2
D11	G3	Y3
D12	G4	Y4
D13	G5	Y5
D14	G6	Y6
D15	G7	Y7
D16	R0	Cr0
D17	R1	Cr1
D18	R2	Cr2
D19	R3	Cr3
D20	R4	Cr4
D21	R5	Cr5
D22	R6	Cr6
D23	R7	Cr7
HS	HSYNC	HSYNC
VS	VSYNC	VSYNC
DE	DE	DE

Table 7.2.1.2 YCbCr 4:2:2 Formats with separate sync

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel0	Pixel1	Pixel0	Pixel1	Pixel0	Pixel1
D0	GND	GND	GND	GND	GND	GND
D1	GND	GND	GND	GND	GND	GND
D2	GND	GND	Y0	Y0	Y2	Y2
D3	GND	GND	Y1	Y1	Y3	Y3
D4	GND	GND	GND	GND	Cb0	Cr0
D5	GND	GND	GND	GND	Cb1	Cr1
D6	GND	GND	Cb0	Cr0	Cb2	Cr2
D7	GND	GND	Cb1	Cr1	Cb3	Cr3
D8	Y0	Y0	Y2	Y2	Y4	Y4
D9	Y1	Y1	Y3	Y3	Y5	Y5
D10	Y2	Y2	Y4	Y4	Y6	Y6
D11	Y3	Y3	Y5	Y5	Y7	Y7
D12	Y4	Y4	Y6	Y6	Y8	Y8
D13	Y5	Y5	Y7	Y7	Y9	Y9
D14	Y6	Y6	Y8	Y8	Y10	Y10
D15	Y7	Y7	Y9	Y9	Y11	Y11
D16	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
D17	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
D18	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
D19	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
D20	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
D21	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
D22	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
D23	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HS	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VS	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 7.2.1.3 YCbCr 4:2:2 Formats with embbedded sync

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel 0	Pixel 1	Pixel 0	Pixel 1	Pixel 0	Pixel 1
D0	GND	GND	GND	GND	Y0	Y0
D1	GND	GND	GND	GND	Y1	Y1
D2	GND	GND	Y0	Y0	Y2	Y2
D3	GND	GND	Y1	Y1	Y3	Y3
D4	GND	GND	GND	GND	Cb0	Cr0
D5	GND	GND	GND	GND	Cb1	Cr1
D6	GND	GND	Cb0	Cr0	Cb2	Cr2
D7	GND	GND	Cb1	Cr1	Cb3	Cr3
D8	Y0	Y0	Y2	Y2	Y4	Y4
D9	Y1	Y1	Y3	Y3	Y5	Y5
D10	Y2	Y2	Y4	Y4	Y6	Y6
D11	Y3	Y3	Y5	Y5	Y7	Y7
D12	Y4	Y4	Y6	Y6	Y8	Y8
D13	Y5	Y5	Y7	Y7	Y9	Y9
D14	Y6	Y6	Y8	Y8	Y10	Y10
D15	Y7	Y7	Y9	Y9	Y11	Y11
D16	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
D17	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
D18	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
D19	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
D20	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
D21	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
D22	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
D23	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HS	GND	GND	GND	GND	GND	GND
VS	GND	GND	GND	GND	GND	GND
DE	GND	GND	GND	GND	GND	GND

Table 7.2.1.4 YC Mux 4:2:2 Formats with separate sync

Pin Name	8-bit YC		10-bit YC		12-bit YC	
	1st clk	2nd clk	1st clk	2nd clk	1st clk	2nd clk
D0	GND	GND	GND	GND	C0	Y0
D1	GND	GND	GND	GND	C1	Y1
D2	GND	GND	C0	Y0	C2	Y2
D3	GND	GND	C1	Y1	C3	Y3
D4	GND	GND	GND	GND	GND	GND
D5	GND	GND	GND	GND	GND	GND
D6	GND	GND	GND	GND	GND	GND
D7	GND	GND	GND	GND	GND	GND
D8	C0	Y0	C2	Y2	C4	Y4
D9	C1	Y1	C3	Y3	C5	Y5
D10	C2	Y2	C4	Y4	C6	Y6
D11	C3	Y3	C5	Y5	C7	Y7
D12	C4	Y4	C6	Y6	C8	Y8
D13	C5	Y5	C7	Y7	C9	Y9
D14	C6	Y6	C8	Y8	C10	Y10
D15	C7	Y7	C9	Y9	C11	Y11
D16	GND	GND	GND	GND	GND	GND
D17	GND	GND	GND	GND	GND	GND
D18	GND	GND	GND	GND	GND	GND
D19	GND	GND	GND	GND	GND	GND
D20	GND	GND	GND	GND	GND	GND
D21	GND	GND	GND	GND	GND	GND
D22	GND	GND	GND	GND	GND	GND
D23	GND	GND	GND	GND	GND	GND
HS	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VS	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 7.2.1.5 YC Mux 4:2:2 Formats with embbedded sync

Pin Name	8-bit YC		10-bit YC		12-bit YC	
	1st clk	2nd clk	1st clk	2nd clk	1st clk	2nd clk
D0	GND	GND	GND	GND	C0	Y0
D1	GND	GND	GND	GND	C1	Y1
D2	GND	GND	C0	Y0	C2	Y2
D3	GND	GND	C1	Y1	C3	Y3
D4	GND	GND	GND	GND	GND	GND
D5	GND	GND	GND	GND	GND	GND
D6	GND	GND	GND	GND	GND	GND
D7	GND	GND	GND	GND	GND	GND
D8	C0	Y0	C2	Y2	C4	Y4
D9	C1	Y1	C3	Y3	C5	Y5
D10	C2	Y2	C4	Y4	C6	Y6
D11	C3	Y3	C5	Y5	C7	Y7
D12	C4	Y4	C6	Y6	C8	Y8
D13	C5	Y5	C7	Y7	C9	Y9
D14	C6	Y6	C8	Y8	C10	Y10
D15	C7	Y7	C9	Y9	C11	Y11
D16	GND	GND	GND	GND	GND	GND
D17	GND	GND	GND	GND	GND	GND
D18	GND	GND	GND	GND	GND	GND
D19	GND	GND	GND	GND	GND	GND
D20	GND	GND	GND	GND	GND	GND
D21	GND	GND	GND	GND	GND	GND
D22	GND	GND	GND	GND	GND	GND
D23	GND	GND	GND	GND	GND	GND
HS	GND	GND	GND	GND	GND	GND
VS	GND	GND	GND	GND	GND	GND
DE	GND	GND	GND	GND	GND	GND

Table 7.2.1.6 12-bit RGB and YCbCr 4:4:4 DDR (d) Format with Separate Sync

Pin Name	12-bit RGB		12-bit YCbCr	
	1st edge	2nd edge	1st edge	2nd edge
D0	B0	G4	Cb0	Y4
D1	B1	G5	Cb1	Y5
D2	B2	G6	Cb2	Y6
D3	B3	G7	Cb3	Y7
D4	B4	R0	Cb4	Cr0
D5	B5	R1	Cb5	Cr1
D6	B6	R2	Cb6	Cr2
D7	B7	R3	Cb7	Cr3
D8	G0	R4	Y0	Cr4
D9	G1	R5	Y1	Cr5
D10	G2	R6	Y2	Cr6
D11	G3	R7	Y3	Cr7
HS	HSYNC		HSYNC	
VS	VSYNC		VSYNC	
DE	DE		DE	

7.2.2 Color Space Conversion (YCbCr to RGB)

Many video decoders only offer YCbCr outputs, while DVI 1.0 supports only RGB color space. In order to offer full compatibility between various Source and Sink combination, this block offers YCbCr to RGB color space conversion (CSC). This provides maximum flexibility.

RGB - YCbCr Equations: SDTV
The basic equations to convert between 8-bit digital R′G′B′ data with a 16–235 nominal range (Studio RGB) and YCbCr are:

Y = 0.299R′ + 0.587G′ + 0.114B′
Cb = –0.172R′ – 0.339G′ + 0.511B′ + 128
Cr = 0.511R′ – 0.428G′ – 0.083B′ + 128
R′ = Y + 1.371(Cr – 128)
G′ = Y – 0.698(Cr – 128) – 0.336(Cb – 128)
B′ = Y + 1.732(Cb – 128)

RGB - YCbCr Equations: HDTV
The basic equations to convert between 8-bit digital R′G′B′ data with a 16–235 nominal range (Studio RGB) and YCbCr are:

Y = 0.213R′ + 0.715G′ + 0.072B′
Cb = –0.117R′ – 0.394G′ + 0.511B′ + 128
Cr = 0.511R′ – 0.464G′ – 0.047B′ + 128
R′ = Y + 1.540(Cr – 128)
G′ = Y – 0.459(Cr – 128) – 0.183(Cb – 128)
B′ = Y + 1.816(Cb – 128)

7.2.3 Pixel Repetition

Video formats with native pixel rates below 25 Mpixels/sec require pixel-repetition in order to be carried across a TMDS link. 720x480i and 720x576i video format timings shall always be pixel-repeated. The HDMI Source indicates the use of pixel-repetition with the Pixel Repetition (PR0:PR3) field in the AVI InfoFrame.

This field indicates to the HDMI Sink how many repetitions of each unique pixel are transmitted. In non-repeated formats, this value is zero.

For pixel-repeated formats, this value indicates the number of pixels that may be discarded by the Sink without losing real image content.

The Source shall always accurately indicate the pixel repetition count being used. The use of the Pixel Repetition field is optional for HDMI Sink.

During pixel-doubling (TR_PIXEL_RPT = 1), all of the data sent across during the first pixel period will be repeated during the second pixel period. The third pixel period will then represent the second actual pixel and so on.

7.2.4 Audio Data Processing Flow

The LT9611 supports two to eight audio channels through four I2S inputs as well as one S/PDIF input of audio data. The SPDIF stream is processed by a separate SPDIF processing block. The SPDIF processing block consists of SPDIF Frame sync detection and data decode block, FIFOs to store the received data, validity, parity, user's data and channel status bits for both the left and right channels. It also has a single bit FIFO which is used to store the information regarding the first frame detection. A depth of 16 for each of FIFOs is sufficient. The SPDIF sync detection, data decoding and loading of the decoded data are done synchronous to the SPDIF clock. The SDPIF clock is twice the SPDIF bit-rate. This selection is done to ease the implementation of the sync detection and data decoding. The reading of the data is done by the TMDS clock. The TMDS clock and SPDIF clock are assumed to be asynchronous with each other. To ensure that the write pointer of the FIFO is not corrupted when mapped from SPDIF to TMDS clock domain, the write pointer is grey coded. It is also mandatory to double re-time the write pointer in the TMDS clock domain.

In addition to the SPDIF processing block, the audio data paketization also has a header byte generation block. This block is responsible for generation of the header bytes for the audio packet.

The four I2S inputs allow transmission of 8-channel uncompressed audio data at up to 192 kHz sample rate. Four FIFOs are to store the received data.

The appropriate registers must be configured to describe the format of audio being input into the LT9611. This information is passed over the HDMI link in the CEA-861B Audio Info (AI) packets.

Four I2S inputs also allow transmission of DVD-Audio and decoded Dolby Digital to A/V Receivers and high-end displays. The interface supports up to 2-channel 192 kHz or 8-channel 96 kHz. The I2S pins must also be 'coherent' with MCLK.

MCLK frequencies support various audio sample rates as shown in Table 7.2.5.1.

Table 7.2.4.1 Supported MCLK Frequencies

	Audio Sample Rate, Fs						
	8-Channel I2S and 2-Channel S/PDIF Supported Rates						
	2-Channel I2S Supported Rates						
Multiple of Fs	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
192	6.144 MHz	8.467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.869 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.869 MHz	33.864 MHz	67.738 MHz	73.728 MHz
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz		
768	18.432 MHz	16.394 MHz	12.288 MHz	67.738 MHz	73.728 MHz		
1024	24.576 MHz	45.158 MHz	49.152 MHz				
1152	36.864 MHz	50.803 MHz	55.296 MHz				

Audio data carried across the HDMI link, which is driven by a TMDS (video) clock only, does not retain the original audio sample clock. The task of recreating this clock at the Sink is called Audio Clock Regeneration.

In many video source devices, the audio and video clocks are generated from a common clock

(coherent clocks). In this situation, there exists a rational (integer divided by integer) relationship between these two clocks. The HDMI clock regeneration architecture can take advantage of this rational relationship and can also work in an environment where there is no such relationship between these two clocks, that is, where the two clocks are truly asynchronous or where their relationship is unknown.

The Source shall determine the fractional relationship between the video clock and an audio reference clock.

The exact relationship between the two clocks will be:

$$128*fs = f_{TMDS\_CLK} * N / CTS.$$

The CTS value generated by the HDMI source is used by the HDMI sync to re-generate the audio sample clock. The CTS is generated according to the equation 128*FS = pixel clock*N/CTS, where FS is the audio sample clock. In other words the CTS is generated by counting the number of pix clocks in 128*fs/N duration. This can be implemented using simple counters. The CTS counter has to be a 20bit counter and is initialized (to zero) after every 128*FS/N clocks.

The 128*fs and pixel clock have to be treated as asynchronous with respect to each other and appropriate care is to be taken during synchronization.

7.2.5 HDCP

The LT8618SX includes HDCP 1.4(High - Bandwidth Digital Content Protection) circuitry. The HDCP protocol ensures protection from unauthorized duplication of copyrighted media content.

The LT8618SX employs a HDCP encryption engine. It contains the encryption logic for all HDMI data (audio, video, and control). Hardware - implemented HDCP authentication and encryption for audio and video reduce external micro - controller

overhead. HDCP encryption and authentication may be performed following device initialization. When using the LT9611, system manufacturers need to provide external key sets through a memory device, for example an EEPROM.

The HDCP encryption engine contains all the necessary logic to encrypt the incoming audio and video data. The encryption process is entirely controlled by the system microcontroller/microprocessor through a set sequence of register reads and writes. HDCP keys and Key Selector Value (KSV) stored in the external memory are used in the encryption process. A resulting calculated value is applied to an XOR mask during each clock cycle to encrypt the audio/video data.

8. Specification

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCC18_RX, VCC18_TXPLL VDD	1.8V Power Supply Voltage	-0.3		2.0	V
VCC33	3.3V Power Supply Voltage	-0.3		3.63	V
V_I	CMOS Terminal Input Voltage Range	-0.3		2.0	V
V_O	CMOS Terminal Output Voltage Range	-0.3		2.0	V
T_S	Storage Temperature	-55		125	℃
ESD	HBM Elastrostatic Discharge Level		4K		V

Notes:
1.Permanent device damage may occur if absolute maximum conditions are exceeded.
2.Function operation should be restricted to the conditions described under Normal Operating Conditions.

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCC18_RX, VCC18_TX VDD	1.8V Power Supplay Voltage	1.62	1.8	1.98	V
VCC33	3.3V Power Supply Voltage	2.97	3.3	3.63	V
VCC_N	Power Supply Voltage Noise			50	mV
T_A	Operating Free-air Temperature	-40	27	85	℃

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

DIGITAL I/Os DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIH	Input High-level Voltage	1.62		3.63	V
VIL	Input Low-level Voltage			500	mV
VTH+	Low to High Threshold Voltage		1.28		V
VTH-	High to Low Threshold Voltage		0.8		V
Duty Cycle	Input Pixel Clock Duty Cycle	40%	50%	60%	
VOH	Output High-level Voltage	2.4			V
VOL	Output Low-level Voltage			0.4	V
HDMI Transmitter DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VOFF	Single-ended standby (off) output voltage	AVCC-10		AVCC+10	mV
VH	Single-ended output high level voltage	AVCC-200		AVCC+10	mV
VL	Single-ended output low level voltage	AVCC-700		AVCC-400	mV
VSWING	Single-ended output data swing	400		600	mV

RTERM	AC couple single-ended impedance	40		60	Ω

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

HDMI Transmitter AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
T_Intra_Pair_Skew	Intra-pair skew			0.15 Tbit	ps
T_Inter_Pair_Skew	Inter-pair skew			0.2 Tcharactor	ns
Tr/Tf	Rise time / fall time	75			ps
DUTY	TMDS clock duty cycle	40	50	60	%
T_jitter	Maximum TMDS clock jitter			0.25Tbit	ps
Video AC Timing Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
TCIP	IDCK Period,one pixel per clock	3.3		40	ps
FCIP	IDCK Frequency,one pixel per clock	25		300	MHz
TCIP12	IDCK Period,dual-edge clock	6.6		40	ps
FCIP12	IDCK Frequency, dual-edge clock	25		150	MHz
T_{DUTY}	IDCK Duty Cycle	40%		60%	
T_{SIDF}	Setup Time to IDCK falling edge in SDR mode	1.5			ns
T_{HIDF}	Hold Time to IDCK falling edge in SDR mode	0.5			ns
T_{SIDR}	Setup Time to IDCK rising edge in SDR mode	0.7			ns
T_{HIDR}	Hold Time to IDCK rising edge in SDR mode	1.1			ns
T_{SIDD}	Setup Time to IDCK edge in DDR mode	1.3			ns
T_{HIDD}	Hold Time to IDCK edge in DDR mode	0.8			ns
Audio AC Timing Specifications					
F_{S_I2S}	I2S Sample Rate	32		192	kHz
T_{SCKCYC}	I2S Cycle Time			1.0	UI
$T_{SCKDUTY}$	I2S Duty Cycle	90%		110%	
T_{I2SSU}	I2S Setup Time	15			ns
T_{I2SHD}	I2S Hold Time	0			ns
F_{S_SPDIF}	SPDIF Sample Rate	32		96	kHz
T_{SPCYC}	SPDIF Cycle Time			1.0	UI
T_{SPDUTY}	SPDIF Duty Cycle	90%		110%	
$F_{MCLKCYC}$	MCLK Cycle Time			75	MHz
$T_{MCLKDUTY}$	MCLK Duty Cycle	40%		60%	
T_{AUDDLY}	Audio Pipeline Delay		30	70	us

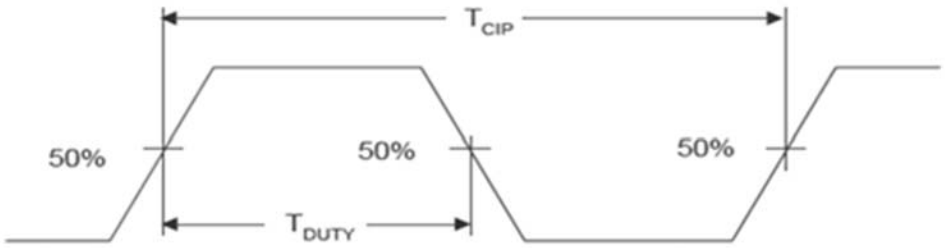


Figure 8.4.1 IDCK Clock Cycle/High/Low Times

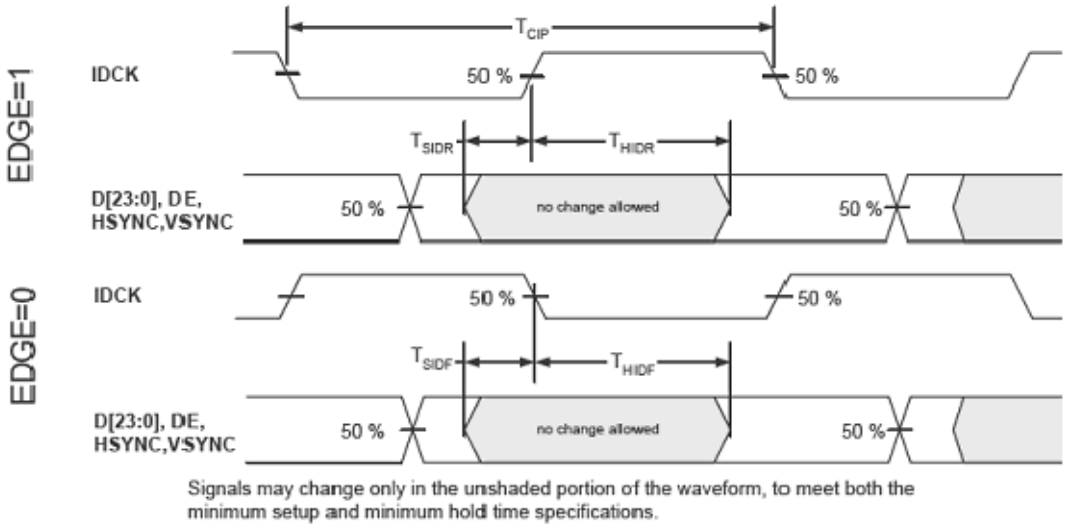


Figure 8.4.2 Control and Data Signal-Edge Setup/Hold Times to IDCK

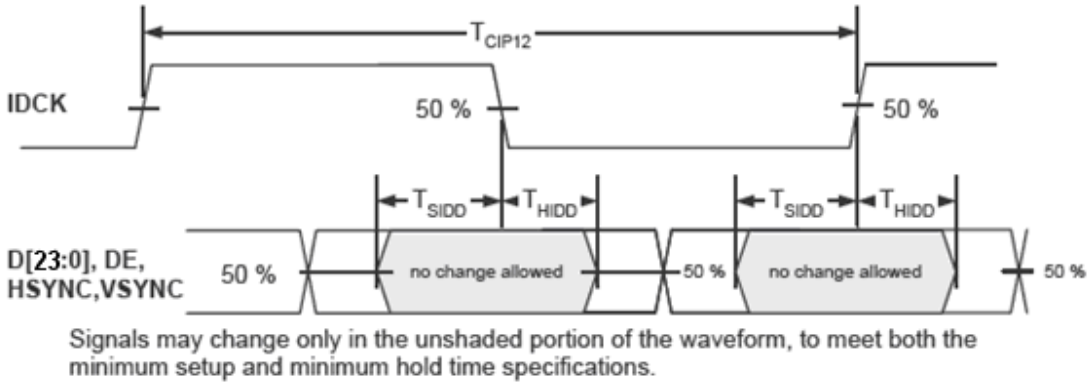


Figure 8.4.3 Dual-Edge Setup/Hold Times to IDCK

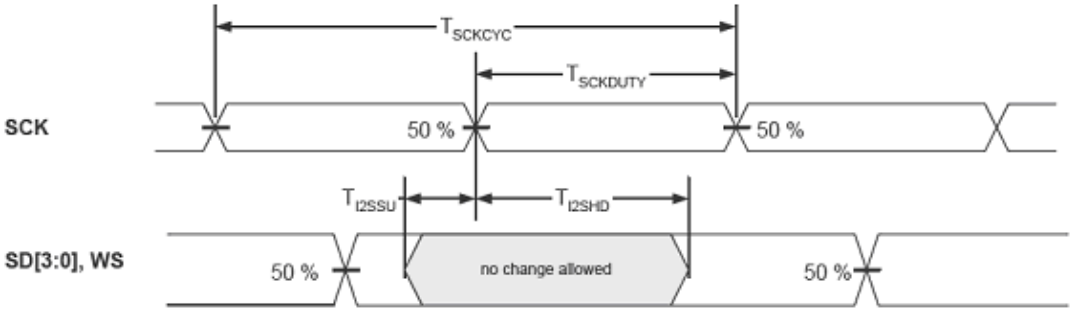


Figure 8.4.4 I2S Input Timings

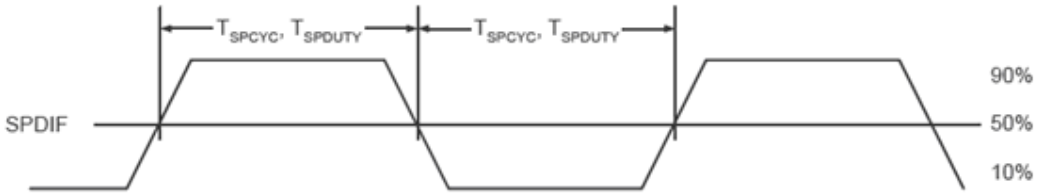


Figure 8.4.5 S/PDIF Input Timings

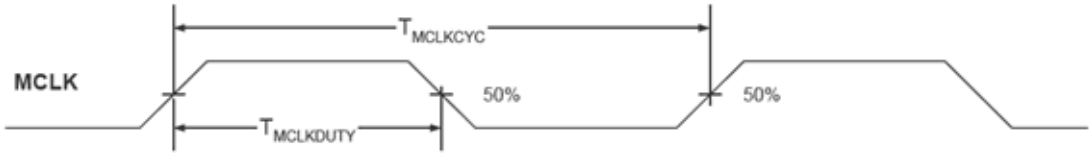


Figure 8.4.6 MCLK Timings

8.5 Power Consumption

Table 8.5.1 Power Consumption

Symbol	Test Condition	Power Consumption	Unit
I_{VCC18}	24bit TTL to HDMI 4K30Hz	180	mA
I_{VCC33}		9	mA
I_{VCC18}	24bit TTL to HDMI 1080P	100	mA
I_{VCC33}		6	mA

8.6 Power-up and Reset Sequence

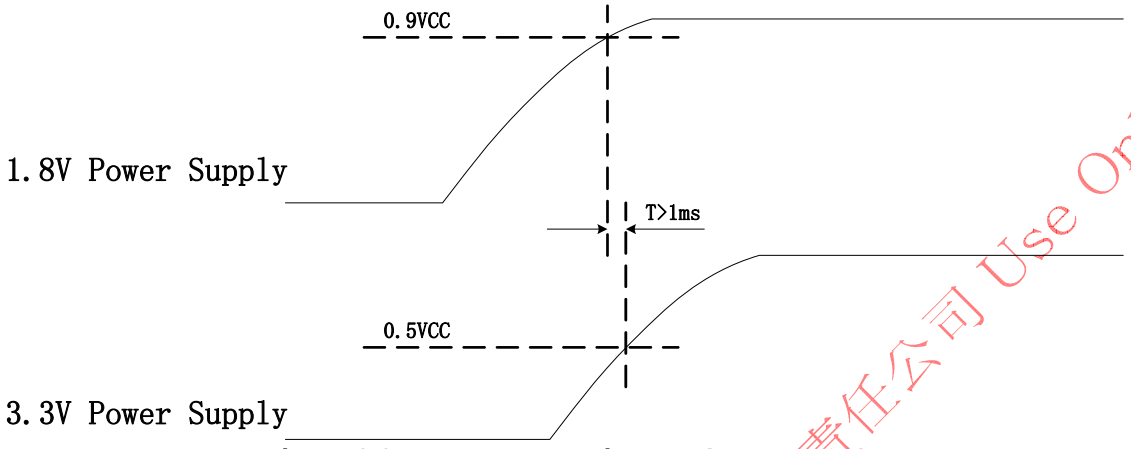


Figure 8.6.1 Power-up and Reset Sequence

9. Package Information

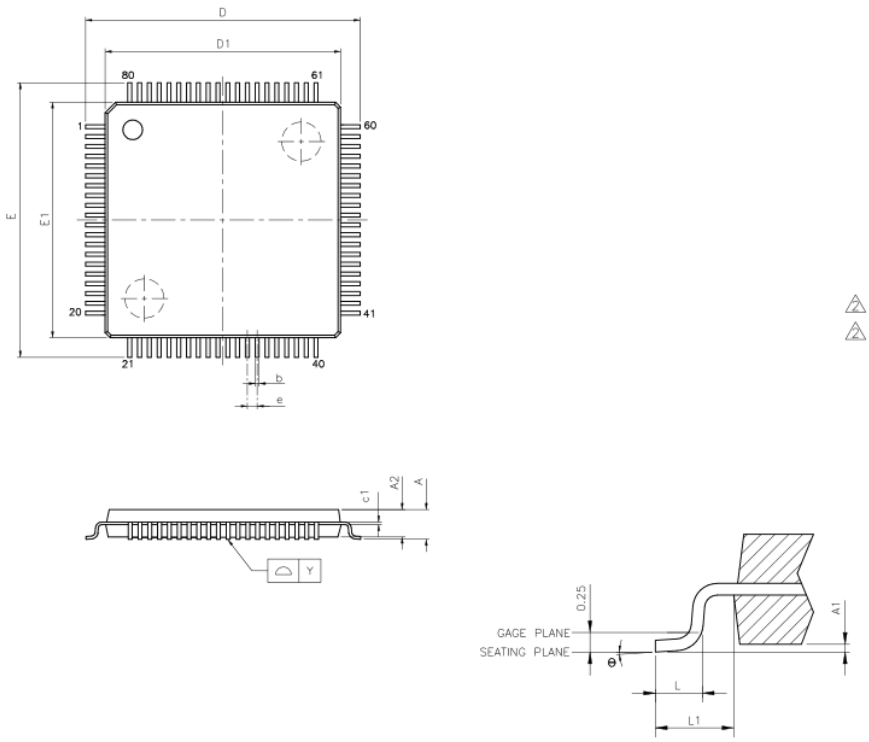
9.1 ePad Enhancement

The LT8618SXA is packaged in a 80-lead LQFP .
The LT8618SXB is packaged in a 64-lead QFN package with ePad.
The LT8618SX is packaged in a 64-lead QFN package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

9.2 Package Dimensions

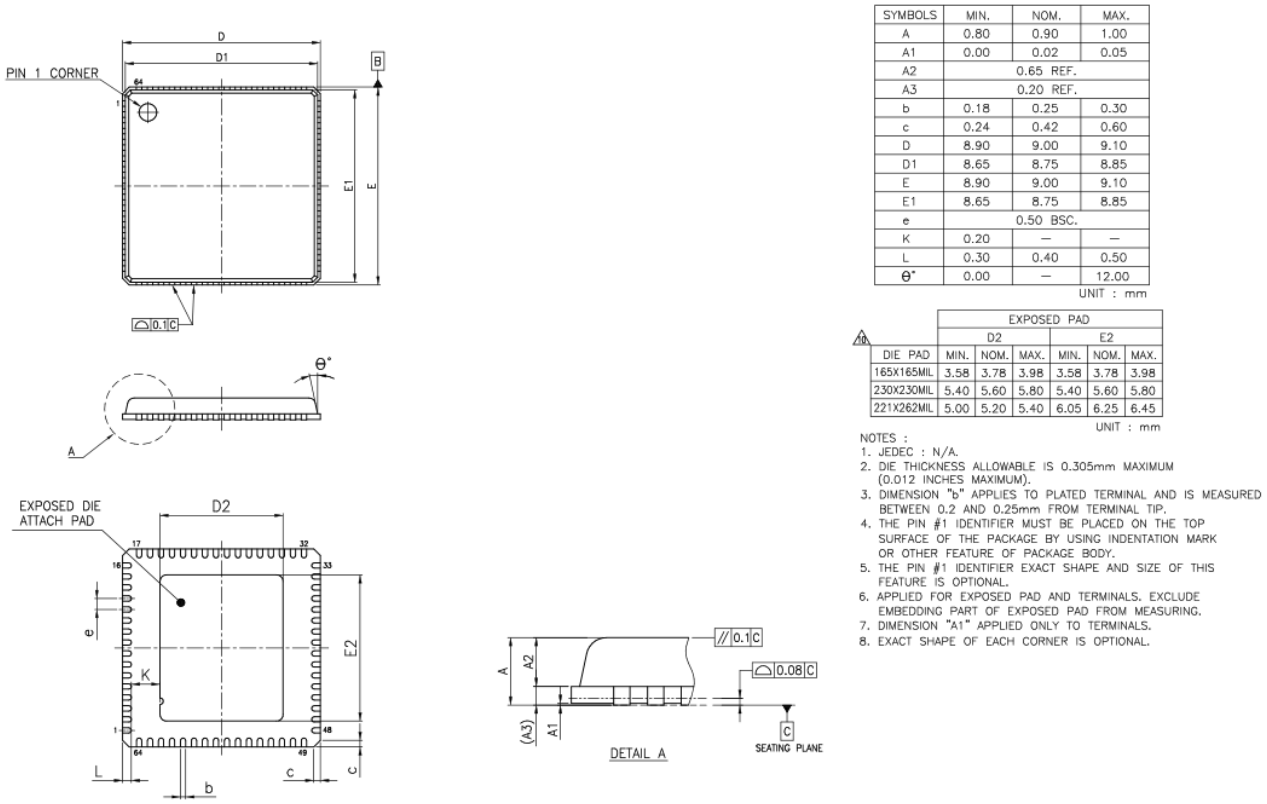


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	14 BSC	
D1	12 BSC	
E	14 BSC	
E1	12 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	
Y	—	0.08
θ	0°	7°

NOTES:
1.JEDEC OUTLINE:MS-026 BDD
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

Figure 9.2.1 LT8618SXA Package Dimensions



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.20 REF.	
b	0.18	0.25	0.30
c	0.24	0.42	0.60
D	8.90	9.00	9.10
D1	8.65	8.75	8.85
E	8.90	9.00	9.10
E1	8.65	8.75	8.85
e		0.50 BSC.	
K	0.20	–	–
L	0.30	0.40	0.50
θ°	0.00	–	12.00

UNIT : mm

	EXPOSED PAD					
	D2			E2		
DIE PAD	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
165X165MIL	3.58	3.78	3.98	3.58	3.78	3.98
230X230MIL	5.40	5.60	5.80	5.40	5.60	5.80
221X262MIL	5.00	5.20	5.40	6.05	6.25	6.45

UNIT : mm

NOTES :
1. JEDEC : N/A.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

Figure 9.2.2 LT8618SXB Package Dimensions

Visit our corporate web page at: www.lontiumsemi.com
Technical support: support@lontium.com
Sales: sales@lontium.com