AP0200_100vFBGA_Adapter

Rev	Who	Date	Description
Rev 0.0	gmudhuguri	03/18/2014	Initial.
Rev 0.1	gmudhuguri	04/22/2014	1) Removed the TRST_N Jtag Connection. 2) Changed the Hearders to a smaller package 3) Added Pull down to all config and GPIO headers.
Rev 0.2	gmudhuguri	04/30/2014	1) Removed the Potentiometers for the power page. 2) Removed the Voltage Shift IC for beagle SPI
Rev 0.3	gmudhuguri	05/05/2014	1) Replaced VDDIO regulator to track the IO from the ethernet PHY board.
Rev 0.4	gmudhuguri	05/07/2014	1) Replaced the IO Expander. 2) Removed decaps on the power to headboard
Rev 0.5	gmudhuguri	05/14/2014	1) Replace 2x10 JTAG with 2x5 JTAG connector
Rev 1.0	gmudhuguri	06/12/2014	1) Interchanged the Connections from the IO expander to have a sequence 2) Connected S-SP0 pin from the baseboard connector to Stanby pin 3) Removed the gpio1 led circuitary 4) Added Pull-ups to I2C lines 5) Connected un-used S_SP pins of the two connectors 6) Replaced the 10 pin JTAG header with 20 pin. 7) Added a Diag-Display circuit adding a level translator and a 8 pin header 8) Removed the headers for the confid of gpios 2 to 6.
Rev 1.1	gmudhuguri	06/27/2014	1) Replace 2x10 JTAG TSW with 2x10 JTAG TST connector
Rev 1.2	aralex	08/20/2015	Made R101 as DNP becase the Demo3 and Sensor Trigger should not be shorted
Rev 1.3	aralex	10/13/2015	Made R84 as DNP in OrCAD to reflect in BOM. Earlier it was a text only

Aptina IMAGING

Title: TITLE PAGE		
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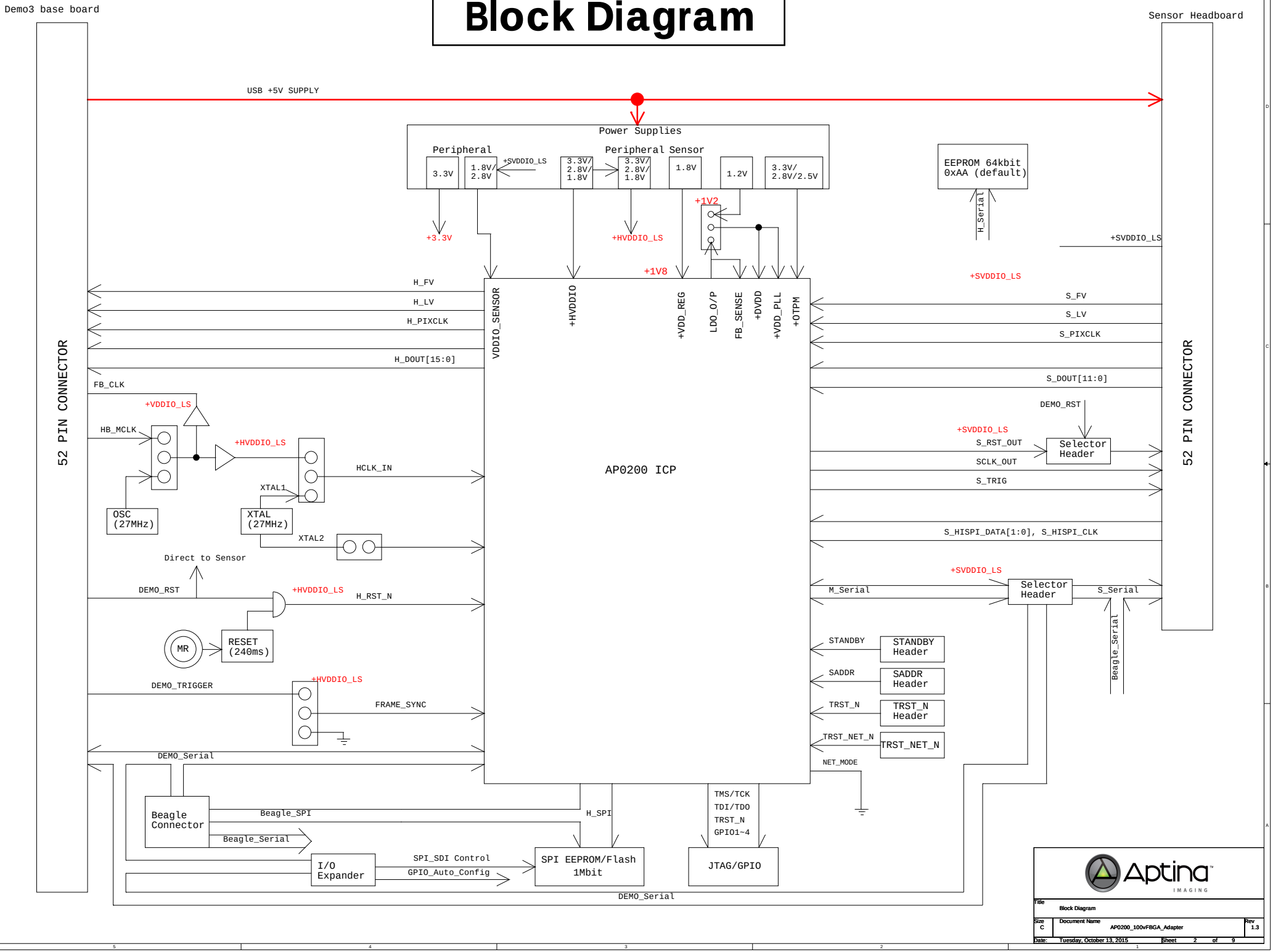
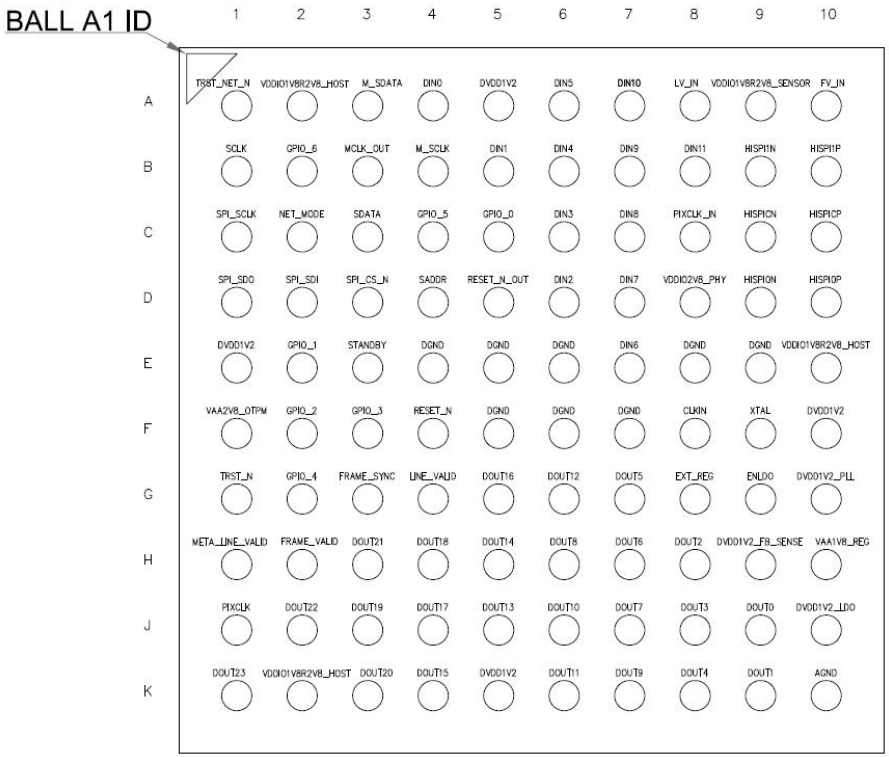
Block Diagram



PINOUT



Aptina IMAGING

Title: PINOUT		
Size: C	Document Name: AP0200_100vFBGA_Adapter	Rev: 1.3
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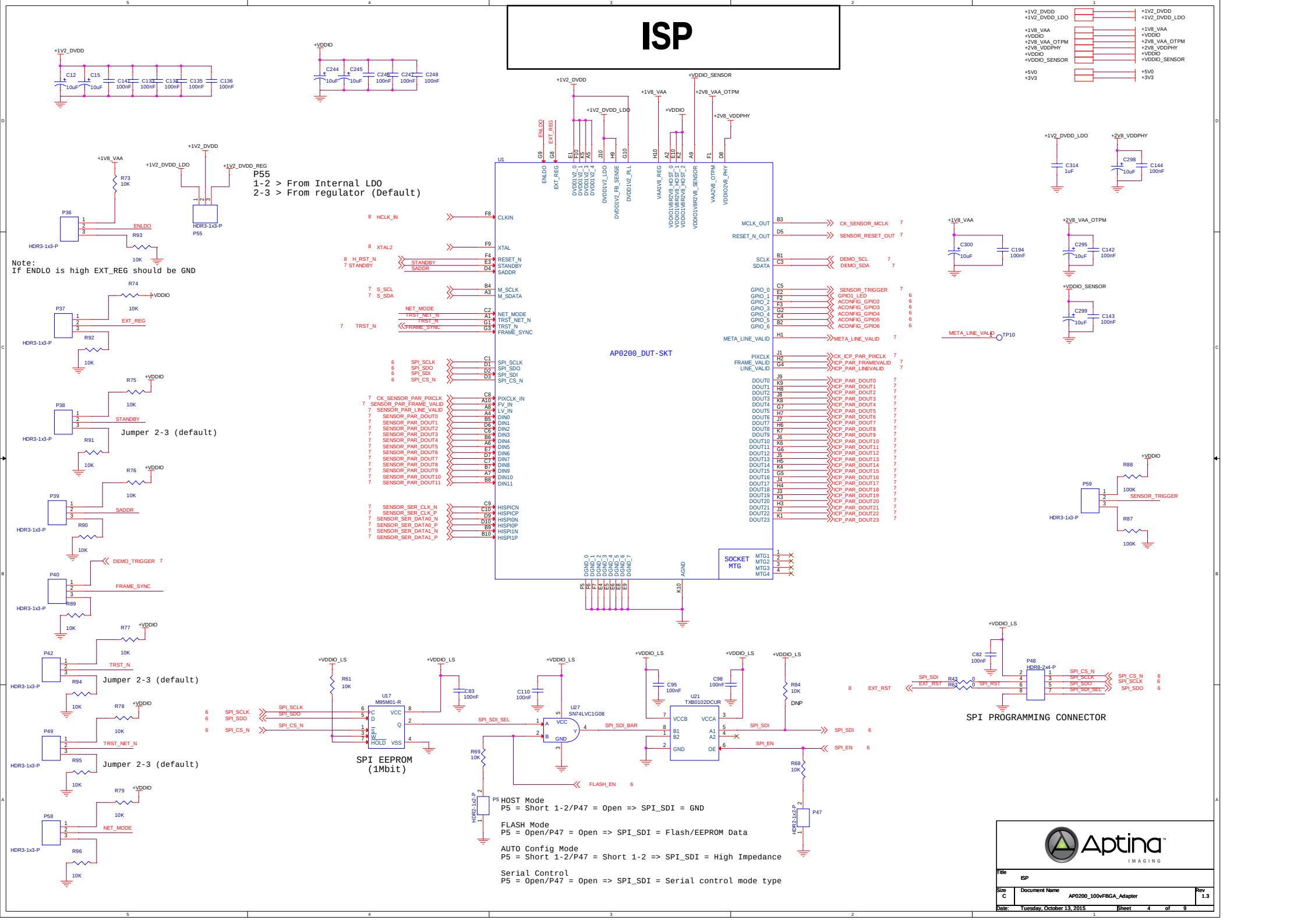
ISP


+1V2_DVDD
C12 10uF
C15 10uF
C141 100nF
C133 100nF
C134 100nF
C135 100nF
C136 100nF
+VDDIO
C244 10uF
C245 10uF
C246 100nF
C247 100nF
C248 100nF
+1V2_DVDD
+1V2_DVDD_LDO
+1V2_DVDD_REG
+1V8_VAA
R73 10K
P36
ENLDO
R93 10K
HDR3-1x3-P
P55
HDR3-1x3-P
P55
1-2 > From Internal LDO
2-3 > From regulator (Default)
Note:
If ENDLO is high EXT_REG should be GND
R74 10K
+VDDIO
P37
EXT_REG
R92 10K
HDR3-1x3-P
R75 10K
+VDDIO
P38
STANDBY
R91 10K
HDR3-1x3-P
Jumper 2-3 (default)
R76 10K
+VDDIO
P39
SADDR
R90 10K
HDR3-1x3-P
DEMO_TRIGGER 7
P40
FRAME_SYNC
R89 10K
HDR3-1x3-P
R77 10K
+VDDIO
P42
TRST_N
R94 10K
HDR3-1x3-P
Jumper 2-3 (default)
R78 10K
+VDDIO
P49
TRST_NET_N
R95 10K
HDR3-1x3-P
Jumper 2-3 (default)
R79 10K
+VDDIO
P58
NET_MODE
R96 10K
HDR3-1x3-P
U1
AP0200_DUT-SKT
ENLDO
EXT_REG
DVDD1V2_0
DVDD1V2_1
DVDD1V2_3
DVDD1V2_4
DVDD1V2_LDO
DVDD1V2_FB_SENSE
DVDD1V2_PLL
VAA1V8_REG
VDDIO1V8R2V8_HOST_0
VDDIO1V8R2V8_HOST_1
VDDIO1V8R2V8_HOST_2
VDDIO1V8R2V8_SENSOR
VAA2V8_OTPM
VDDIO2V8_PHY
8 HCLK_IN
CLKIN
8 XTAL2
XTAL
8 H_RST_N
7 STANDBY
STANDBY
SADDR
RESET_N
STANDBY
SADDR
7 S_SCL
7 S_SDA
M_SCLK
M_SDATA
NET_MODE
TRST_NET_N
7 TRST_N
TRST_N
FRAME_SYNC
6 SPI_SCLK
6 SPI_SDO
6 SPI_SDI
6 SPI_CS_N
SPI_SCLK
SPI_SDO
SPI_SDI
SPI_CS_N
7 CK_SENSOR_PAR_PIXCLK
7 SENSOR_PAR_FRAME_VALID
7 SENSOR_PAR_LINE_VALID
7 SENSOR_PAR_DOUT0
7 SENSOR_PAR_DOUT1
7 SENSOR_PAR_DOUT2
7 SENSOR_PAR_DOUT3
7 SENSOR_PAR_DOUT4
7 SENSOR_PAR_DOUT5
7 SENSOR_PAR_DOUT6
7 SENSOR_PAR_DOUT7
7 SENSOR_PAR_DOUT8
7 SENSOR_PAR_DOUT9
7 SENSOR_PAR_DOUT10
7 SENSOR_PAR_DOUT11
PIXCLK_IN
FV_IN
LV_IN
DIN0
DIN1
DIN2
DIN3
DIN4
DIN5
DIN6
DIN7
DIN8
DIN9
DIN10
DIN11
7 SENSOR_SER_CLK_N
7 SENSOR_SER_CLK_P
7 SENSOR_SER_DATA0_N
7 SENSOR_SER_DATA0_P
7 SENSOR_SER_DATA1_N
7 SENSOR_SER_DATA1_P
HISPICN
HISPICP
HISPI0N
HISPI0P
HISPI1N
HISPI1P
DGND_0
DGND_1
DGND_2
DGND_3
DGND_4
DGND_5
DGND_6
DGND_7
AGND
SOCKET MTG
MTG1
MTG2
MTG3
MTG4
MCLK_OUT
RESET_N_OUT
CK_SENSOR_MCLK 7
SENSOR_RESET_OUT 7
SCLK
SDATA
DEMO_SCL 7
DEMO_SDA 7
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
SENSOR_TRIGGER 7
GPIO1_LED 6
ACONFIG_GPIO2 6
ACONFIG_GPIO3 6
ACONFIG_GPIO4 6
ACONFIG_GPIO5 6
ACONFIG_GPIO6 6
META_LINE_VALID
META_LINE_VALID 7
PIXCLK
FRAME_VALID
LINE_VALID
CK_ICP_PAR_PIXCLK 7
ICP_PAR_FRAMEVALID 7
ICP_PAR_LINEVALID 7
DOUT0
DOUT1
DOUT2
DOUT3
DOUT4
DOUT5
DOUT6
DOUT7
DOUT8
DOUT9
DOUT10
DOUT11
DOUT12
DOUT13
DOUT14
DOUT15
DOUT16
DOUT17
DOUT18
DOUT19
DOUT20
DOUT21
DOUT22
DOUT23
ICP_PAR_DOUT0
ICP_PAR_DOUT1
ICP_PAR_DOUT2
ICP_PAR_DOUT3
ICP_PAR_DOUT4
ICP_PAR_DOUT5
ICP_PAR_DOUT6
ICP_PAR_DOUT7
ICP_PAR_DOUT8
ICP_PAR_DOUT9
ICP_PAR_DOUT10
ICP_PAR_DOUT11
ICP_PAR_DOUT12
ICP_PAR_DOUT13
ICP_PAR_DOUT14
ICP_PAR_DOUT15
ICP_PAR_DOUT16
ICP_PAR_DOUT17
ICP_PAR_DOUT18
ICP_PAR_DOUT19
ICP_PAR_DOUT20
ICP_PAR_DOUT21
ICP_PAR_DOUT22
ICP_PAR_DOUT23
+1V2_DVDD_LDO
C314 1uF
+2V8_VDDPHY
C298 10uF
C144 100nF
+1V8_VAA
C300 10uF
C194 100nF
+2V8_VAA_OTPM
C295 10uF
C142 100nF
+VDDIO_SENSOR
C299 10uF
C143 100nF
META_LINE_VALID
TP10
+VDDIO
R88 100K
P59
SENSOR_TRIGGER
R87 100K
HDR3-1x3-P
+VDDIO_LS
R61 10K
U17
M95M01-R
SPI EEPROM
(1Mbit)
C83 100nF
C110 100nF
U27
SN74LVC1G08
SPI_SDI_SEL
SPI_SDI_BAR
R69 10K
P5
HDR2-1x2-P
FLASH_EN 6
C95 100nF
C98 100nF
U21
TXB0102DCUR
VCCB
VCCA
B1
B2
A1
A2
GND
OE
SPI_SDI
SPI_EN
R84 10K
DNP
R68 10K
P47
HDR2-1x2-P
8 EXT_RST
C82 100nF
P48
HDR8-2x4-P
SPI_SDI
EXT_RST
R43 0
R62 0
SPI_RST
SPI_CS_N
SPI_SCLK
SPI_SDO
SPI_SDI_SEL
SPI PROGRAMMING CONNECTOR
HOST Mode
P5 = Short 1-2/P47 = Open => SPI_SDI = GND
FLASH Mode
P5 = Open/P47 = Open => SPI_SDI = Flash/EEPROM Data
AUTO Config Mode
P5 = Short 1-2/P47 = Short 1-2 => SPI_SDI = High Impedance
Serial Control
P5 = Open/P47 = Open => SPI_SDI = Serial control mode type
Aptina IMAGING
Title
ISP
Size C
Document Name
AP0200_100vFBGA_Adapter
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Date: Tuesday, October 13, 2015
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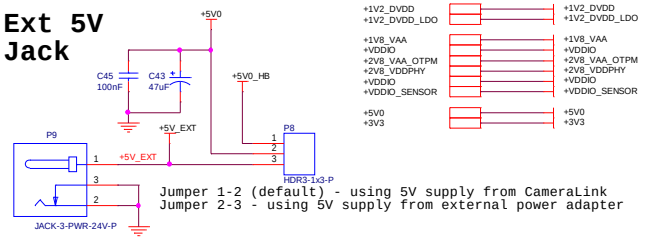
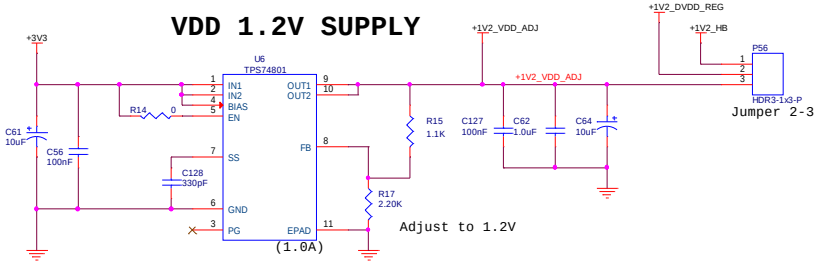
POWER

Ext 5V Jack



Jumper 1-2 (default) - using 5V supply from CameraLink
Jumper 2-3 - using 5V supply from external power adapter

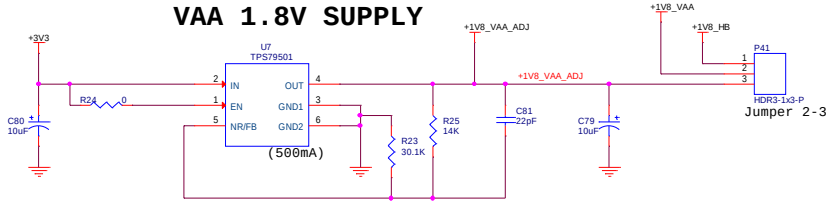
VDD 1.2V SUPPLY



Jumper 2-3

Adjust to 1.2V

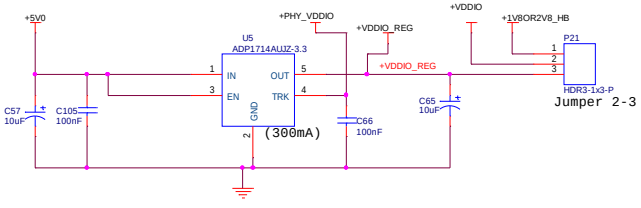
VAA 1.8V SUPPLY



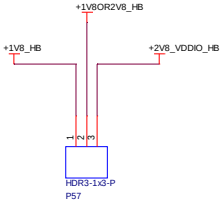
Jumper 2-3

Adjust to 1.8V

VDDIO SUPPLY

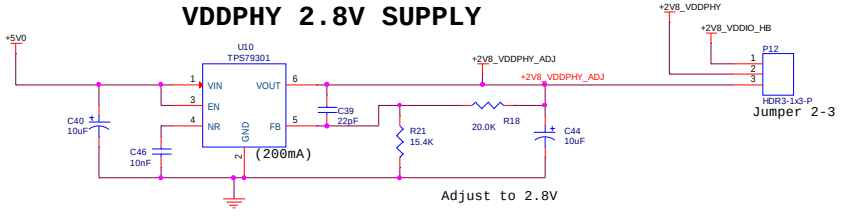


Jumper 2-3



P57
1-2 > 1.8 V from Baseboard to P21 (default)
2-3 > 2.8 V from Baseboard to P21

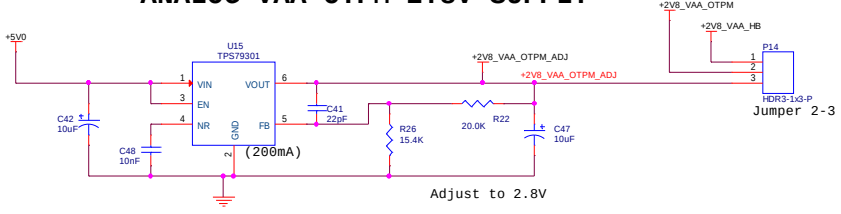
VDDPHY 2.8V SUPPLY



Jumper 2-3

Adjust to 2.8V

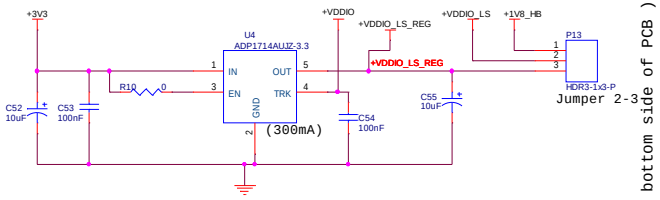
ANALOG VAA OTPM 2.8V SUPPLY



Jumper 2-3

Adjust to 2.8V

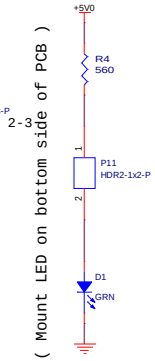
PERIPHERAL VDDIO_LS SUPPLY



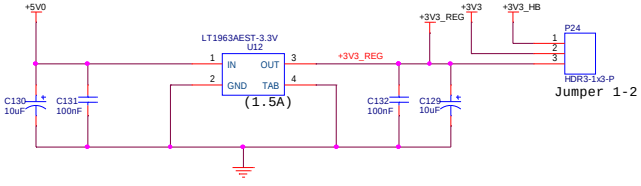
Jumper 2-3

5V LED

(Mount LED on bottom side of PCB)

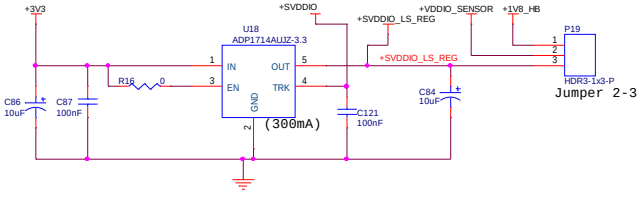


PERIPHERAL 3.3V SUPPLY



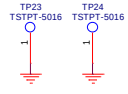
Jumper 1-2

VDDIO_SENSOR SUPPLY



Jumper 2-3

Ground Testpoint



Aptina IMAGING

Title	POWER	
Size C	Document Name AP0200_100vFBGA_Adapter	Rev 1.3
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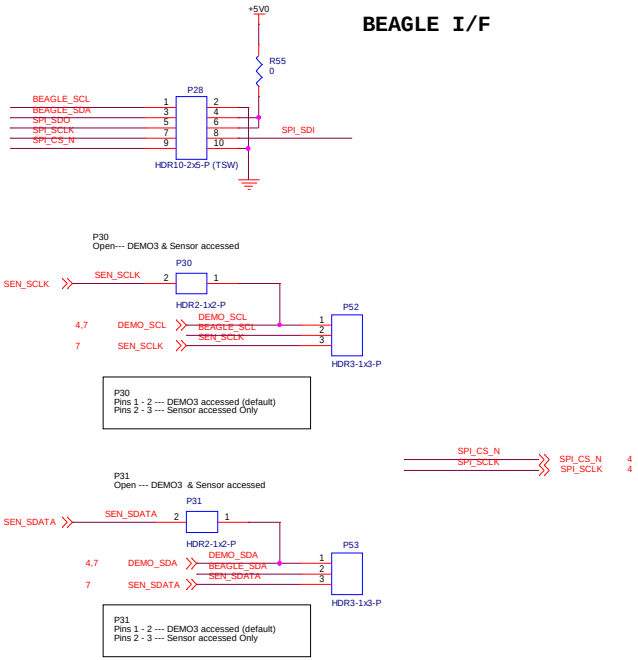
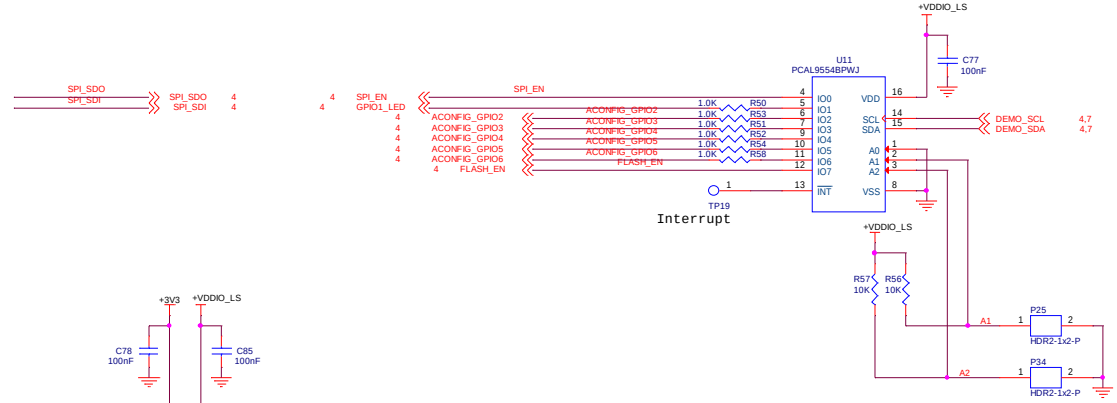
Auto-Config/BEAGLE Interface

BEAGLE I/F

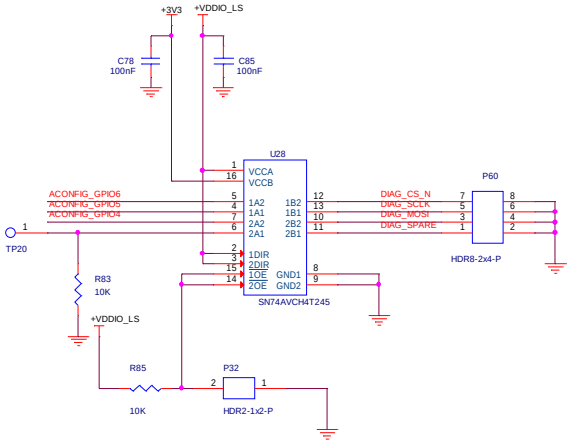


Auto Config Circuit

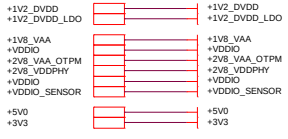


I2C GPIO Address Settings:

```
A2 = HIGH, A1 = LOW;  Address => 0x48 (default)
A2 = HIGH, A1 = HIGH; Address => 0x4C
A2 = LOW,  A1 = HIGH; Address => 0x44
A2 = LOW,  A1 = LOW;  Address => 0x40
```



1-2 ---> for DIAG Operation



Aptina IMAGING

Title: Beagle/Auto Config		
Size: C	Document Name: AP0200_100vFBGA_Adapter	Rev: 1.3
Date: Tuesday, October 13, 2015	Sheet 6 of 9	

External Interface

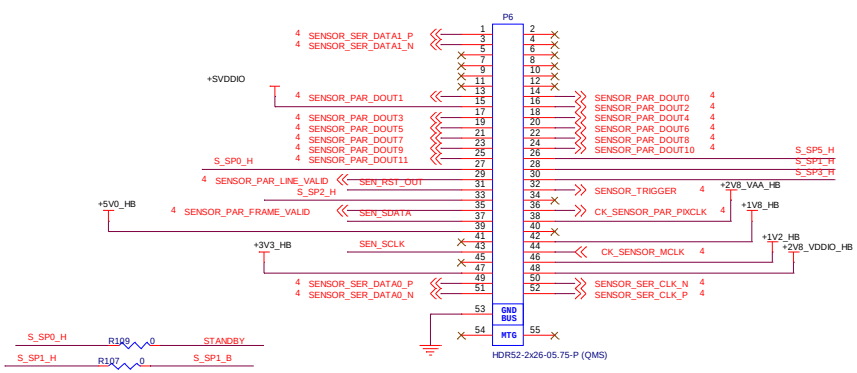
HEADBOARD CONNECTOR

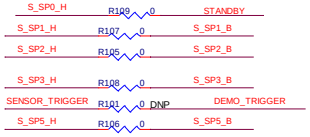
SP0 ---> NO-CONNECT
SP1 ---> CONNECTED TO SP1 OF BASEBOARD CONNECTOR
SP2 ---> CONNECTED TO SP2 OF BASEBOARD CONNECTOR
SP3 ---> CONNECTED TO SP3 OF BASEBOARD CONNECTOR
SP4 ---> GPIO9 PIN OF AP0200
SP5 ---> CONNECTED TO SP5 OF BASEBOARD CONNECTOR

BASEBOARD CONNECTOR

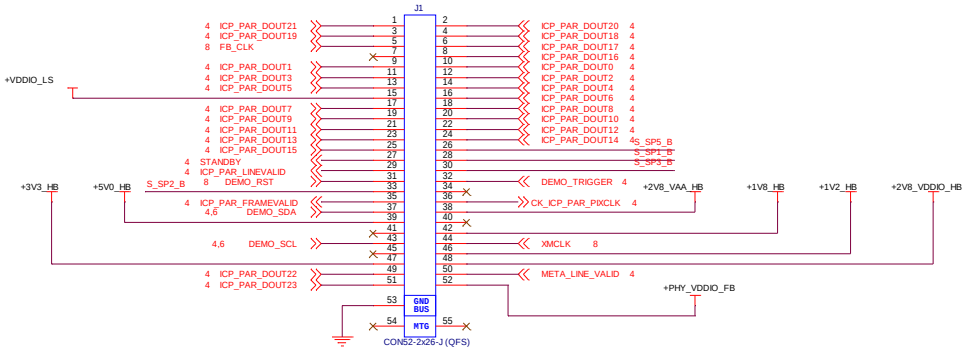
SP0 ---> STANDBY of AP0200
SP1 ---> CONNECTED TO SP1 OF HEADBOARD CONNECTOR
SP2 ---> CONNECTED TO SP2 OF HEADBOARD CONNECTOR
SP3 ---> CONNECTED TO SP3 OF HEADBOARD CONNECTOR
SP4 ---> DEMO_TRIGGER CONNECTED TO FRAME-SYNC PIN OF AP0200
SP5 ---> CONNECTED TO SP5 OF HEADBOARD CONNECTOR

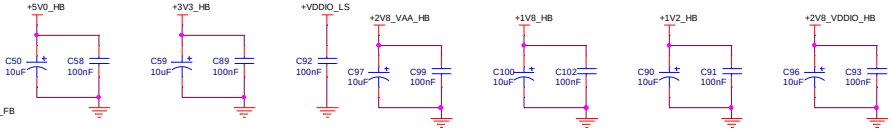
Demo Headboard Connector

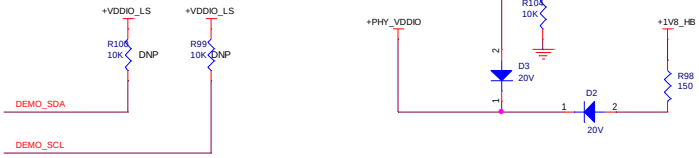


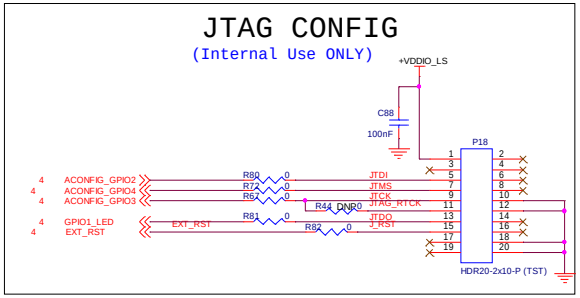


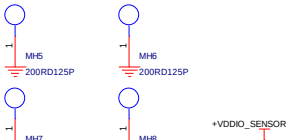
Demo Baseboard Connector

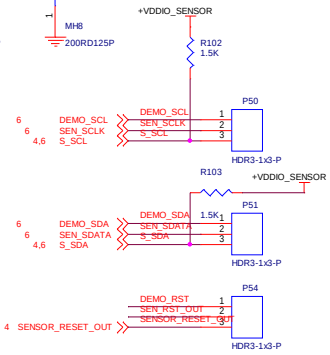




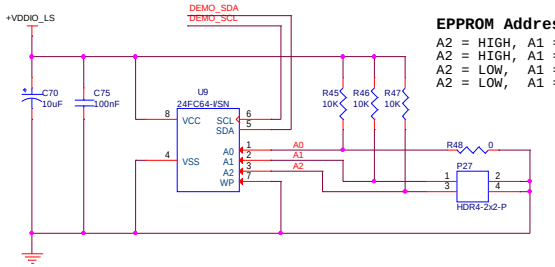






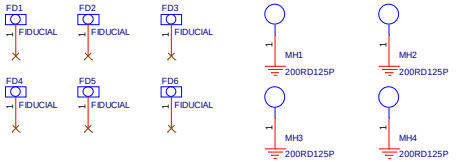


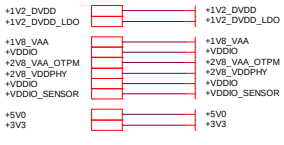
LENS CORRECTION EEPROM



EPPROM Address Switch Settings:

A2 = HIGH, A1 = LOW, A0 = LOW; Address => 0xA8 (default)
A2 = HIGH, A1 = HIGH, A0 = LOW; Address => 0xAC
A2 = LOW, A1 = HIGH, A0 = LOW; Address => 0xA4
A2 = LOW, A1 = LOW, A0 = LOW; Address => 0xA0





Aptina IMAGING

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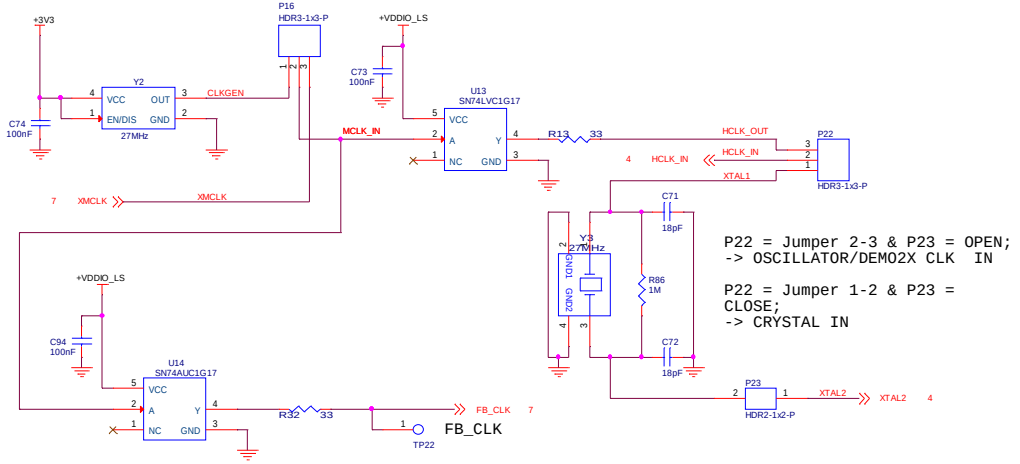
Clock/Reset

+1V2_DVDD
+1V2_DVDD_LDO
+1V8_VAA
+VDDIO
+2V8_VAA_OTPM
+2V8_VDDPHY
+VDDIO
+VDDIO_SENSOR
+5V0
+3V3

User Note: P16
Jumper (1-2) : OSC CLK
Jumper (2-3) : DEMO3 CLK

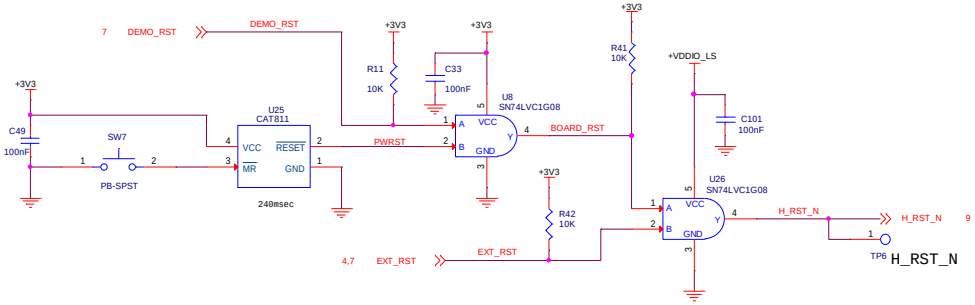
CLOCK CIRCUIT



P22 = Jumper 2-3 & P23 = OPEN;
-> OSCILLATOR/DEMO2X CLK IN

P22 = Jumper 1-2 & P23 =
CLOSE;
-> CRYSTAL IN

RESET CIRCUIT



Title	CLOCK AND RESET		
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