AR0143AT

Product Preview

1/4-Inch 1.3 Mp Digital Image Sensor

ON Semiconductor®

www.onsemi.com

General Description

ON Semiconductor's AR0143AT is a 1/4−inch CMOS digital image sensor with a 1344Hx968V active−pixel array. It captures images in either linear, high dynamic range, or LFM modes, with a rolling−shutter readout. The LFM mode eliminates high frequency LED flicker in the image allowing Traffic Sign Reading (TSR) algorithms to operate in all lighting conditions. It includes sophisticated camera functions such as in−pixel binning, windowing and both video and single frame modes. It is designed for both low light and high dynamic range scene performance, with sensor fault detection features that can enable ASIL B compliance for the camera system. It is programmable through a simple two−wire serial interface. The AR0143AT produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including automotive ADAS, automotive scene viewing, and 720p HDR video.

Features

- Key Technologies:
  - Automotive grade Backside Illuminated Pixel
  - LED Flicker Mitigation mode
  - Sensor Fault Detection for ASIL−B Compliance
  - Up to 4−exposure HDR at 1344x968 and 40 fps or 3−exposure HDR at 1344x968 and 60 fps
- Latest 3.0 μm Back Side Illuminated (BSI) pixel with
- ON Semiconductor DR−Pix™ technology
- Data interfaces: up to 4−lane MIPI CSI−2, Parallel, or up to 4−lane high speed pixel interface (HiSPi) serial interface (SLVS and HiVCM)
- Advanced HDR with flexible exposure ratio control
- LED Flicker Mitigation (LFM) mode
- Selectable automatic or user controlled black level control
- Frame to frame switching among up to 4 contexts to enable multi−function systems
- Spread−spectrum input clock support
- Multi−Camera synchronization support

Applications

- Automotive ADAS
- High dynamic range imaging
- Mirror Replacement
- ADAS + Viewing Fusion

Table 1. KEY PARAMETERS

Parameter	Value
Optical format	1/4 inch
Maximum resolution	1344 x 968 (1.3 Mp)
Shutter type	Electronic Rolling Shutter (ERS)
Pixel size	3 μm
Pixel output interfaces	Up to 4−lane HiSPi with SLVS and HiVCM MIPI CSI−2 12−bit parallel
Output formats	12−bit Uncompressed Linear 20−bit Uncompressed HDR 10−bit Companded Linear 16−bit, 14−bit, or 12−bit Compounded HDR
Control interface	2−wire, Serial Control 100 kHz/1 MHz
Input clock range	6−48MHz in PLL mode
Maximum frame rate	Up to 60fps at 1344x968 (3−exposures)
Output pixel clock maximum	99.43 MHz
Responsivity	TBD
SNRmax	TBD
Max Dynamic Range	>120 dB
Packaging options	9 mm x 9 mm iBGA Bare die
Operating temp. range	−40°C to 110°C Ambient −40°C to 125°C Junction
Supply voltage	I/O 1.8 V or 2.8 V Digital 1.2 V Analog 2.8 V HiSPi 0.4 V or 1.8 V
Power consumption	~ 450 mW typical (1344 x 968, 3exp HDR, 60 fps, serial)

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

Table 2. ORDERING INFORMATION

Part Number	Product Description	Orderable Product Attribute Description
AR0143ATSC00XUEA0-DPBR-E	RGB, 0deg CRA, iBGA	Dry pack with protective film, Double side BBAR glass
AR0143ATSC00XUEA0-DRBR−E	RGB, 0deg CRA, iBGA	Dry pack without protective film, Double side BBAR glass
AR0143ATSC00XUEA0-TPBR−E	RGB, 0deg CRA, iBGA	Tape & reel with protective film, Double side BBAR glass
AR0143ATSC00XUEA0-TRBR-E	RGB, 0deg CRA, iBGA	Tape & reel without protective film, Double side BBAR glass
AR0143ATSC00XUD20-E	RGB, 0deg CRA, Recon Die	
AR0143ATSC00XUEAH3-GEVB	RGB, 0deg CRA, iBGA, Demo3 Headboard	
AR0143ATSC00XUEAD3-GEVK	RGB, 0deg CRA, iBGA, Demo3 Demokit	
MARS1−AR0143ATS−GEVB	MARS AR0143AT, RGB, iBGA Headboard	

NOTE: Contact the ON Semiconductor sales or marketing representative to discuss your specific requirements.

Table of Contents

GENERAL DESCRIPTION

The ON Semiconductor AR0143AT can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 720p−resolution image at 60 frames per second (fps) in 3−exposure HDR mode and 40 fps in 4− exposure HDR mode through the serial output ports. In linear mode, it outputs 12−bit uncompressed or 10−bit compressed raw data, using either the parallel or serial output ports. In high dynamic range (HDR) mode, it outputs 12, 14, or 16−bit compressed data, or 20−bit linearized data using either the parallel or serial output ports. The device may be operated in video (master) mode or in single frame trigger mode. The LFM mode is used to minimize the impact of LED flicker for applications where there is dynamic LED lighting, such as TSR, and is output in linear mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock in parallel mode.

The AR0143AT has additional ASIL features, including but not limited to: two on-board independent temperature sensor, start−up tests, memory BIST, analog and digital CRC, and test patterns. Optional register information and histogram statistic information can be embedded in the first and last 2 lines of the image frame.

The sensor is designed to operate in a wide junction temperature range (−40°C to + 125°C).

FUNCTIONAL OVERVIEW

The AR0143AT is a 1/4 inch progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase-locked loop (PLL) that can be option− ally enabled to generate all internal clocks from a single master input clock running between 6 and 48 MHz. The maximum output pixel rate is 750 Mb/s in serial modes, and 99.43 Mp/s in parallel modes, corresponding to a clock rate of 99.43 MHz. Figure 1 shows a block diagram of the sensor.

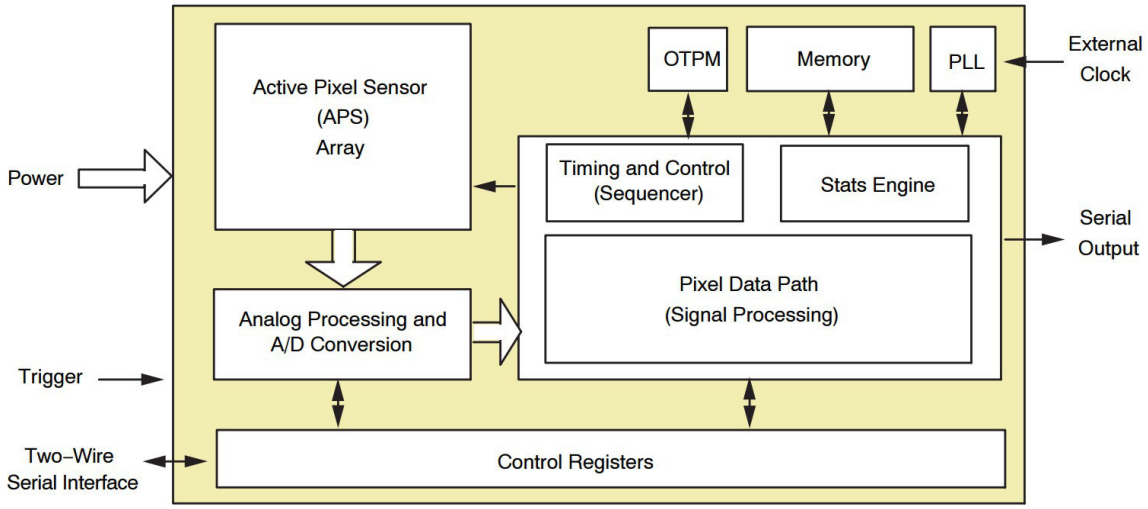

Figure 1. Block Diagram

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.3 Mp BSI Active−Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row inte− grate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog−to−digital converter (ADC). The output from the ADC is a 13−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where multiple images are combined on−chip to produce a single image at 20−bit per pixel value. A compressing mode is further offered to allow this 20−bit pixel value to be transmitted to the host system as a 12− or 14− or 16−bit value with close to zero loss in image quality.

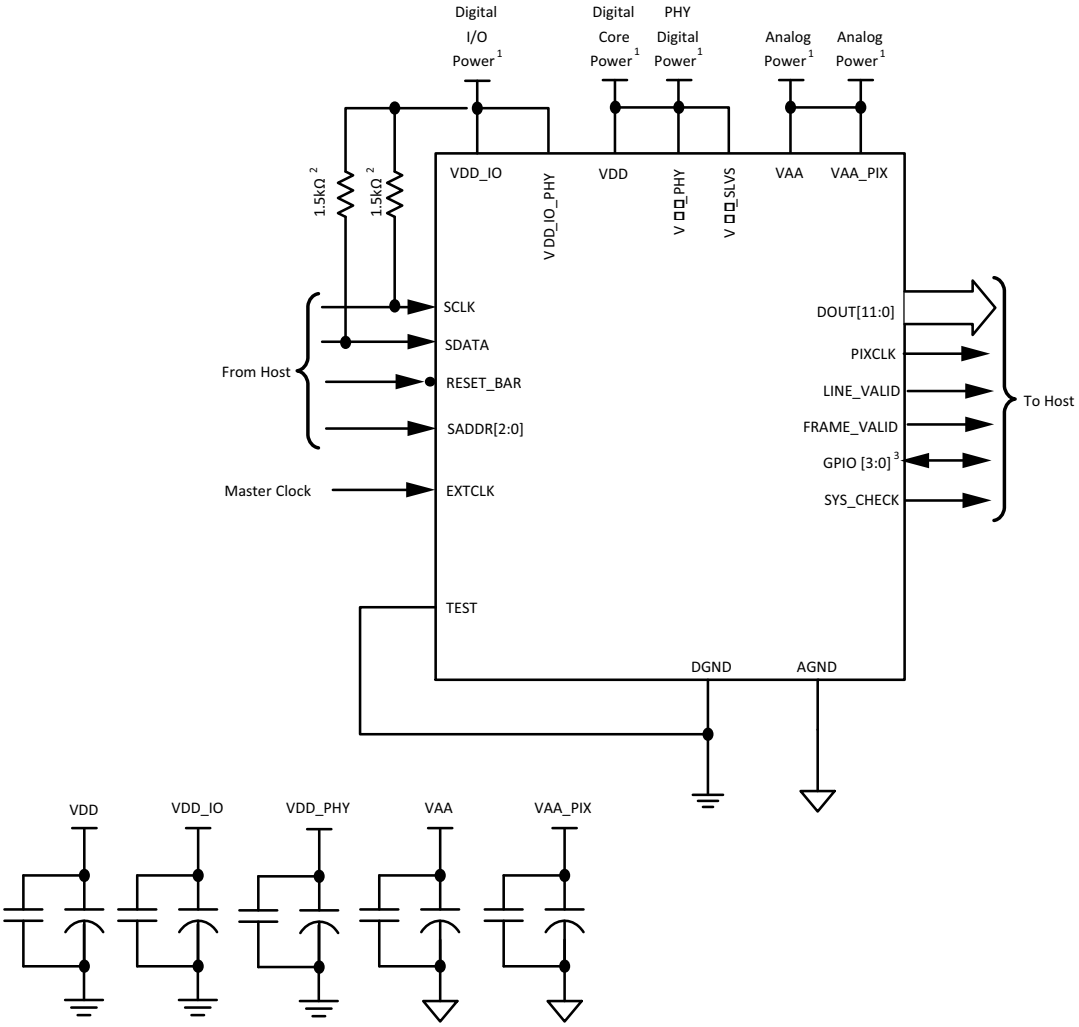

Figure 2. Typical Configuration, Parallel

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
4. The serial output data interface pads can be left unconnected when the parallel output interface is used. The serial output data supply pads should remain connected and powered appropriately.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on lay− out and design considerations. Refer to the AR0143AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.

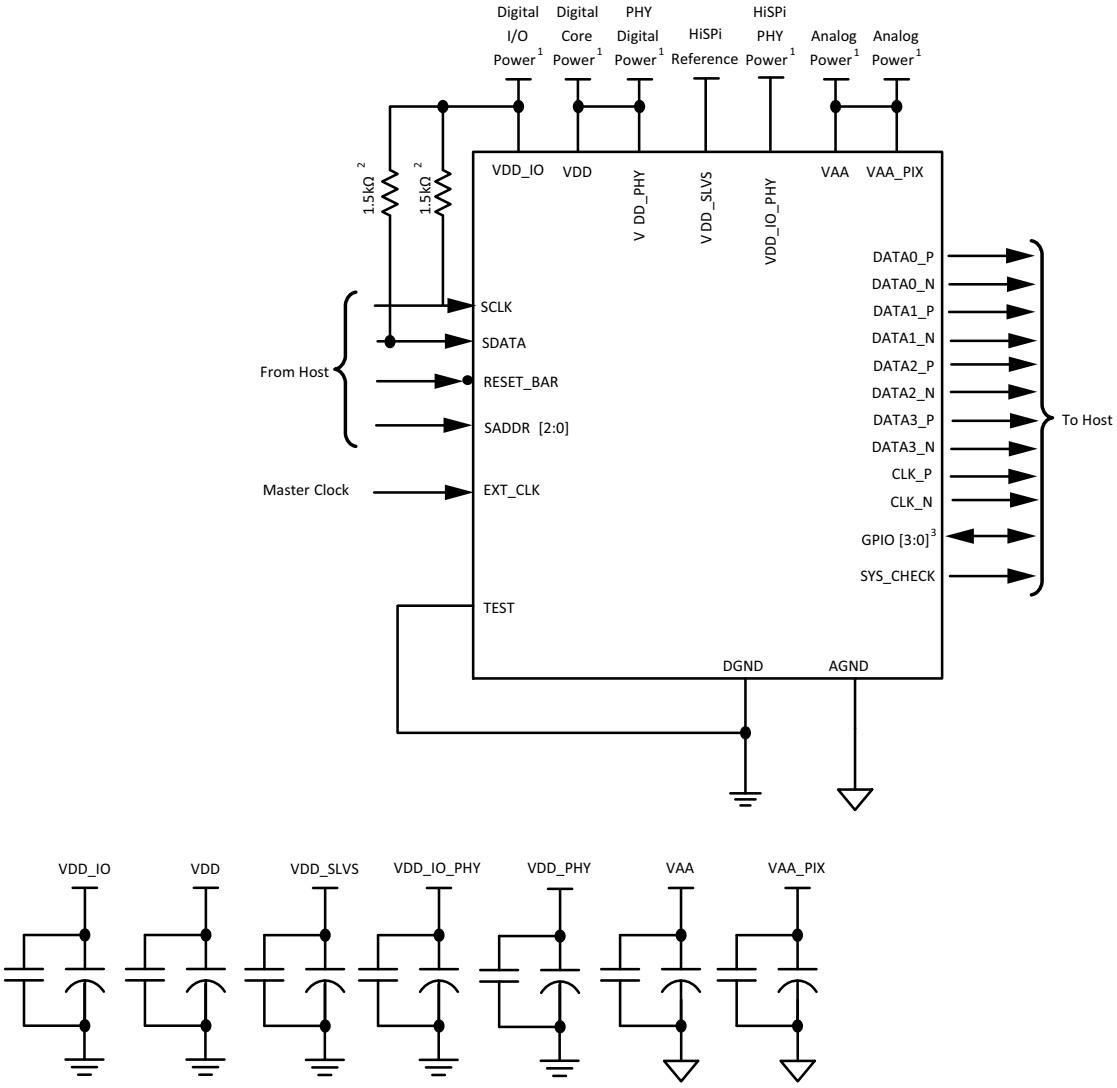

Figure 3. Typical Configuration, 4−Lane HiSPi

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
4. The parallel interface output pads can be left unconnected when the serial output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on lay− out and design considerations. Refer to the AR0143AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.

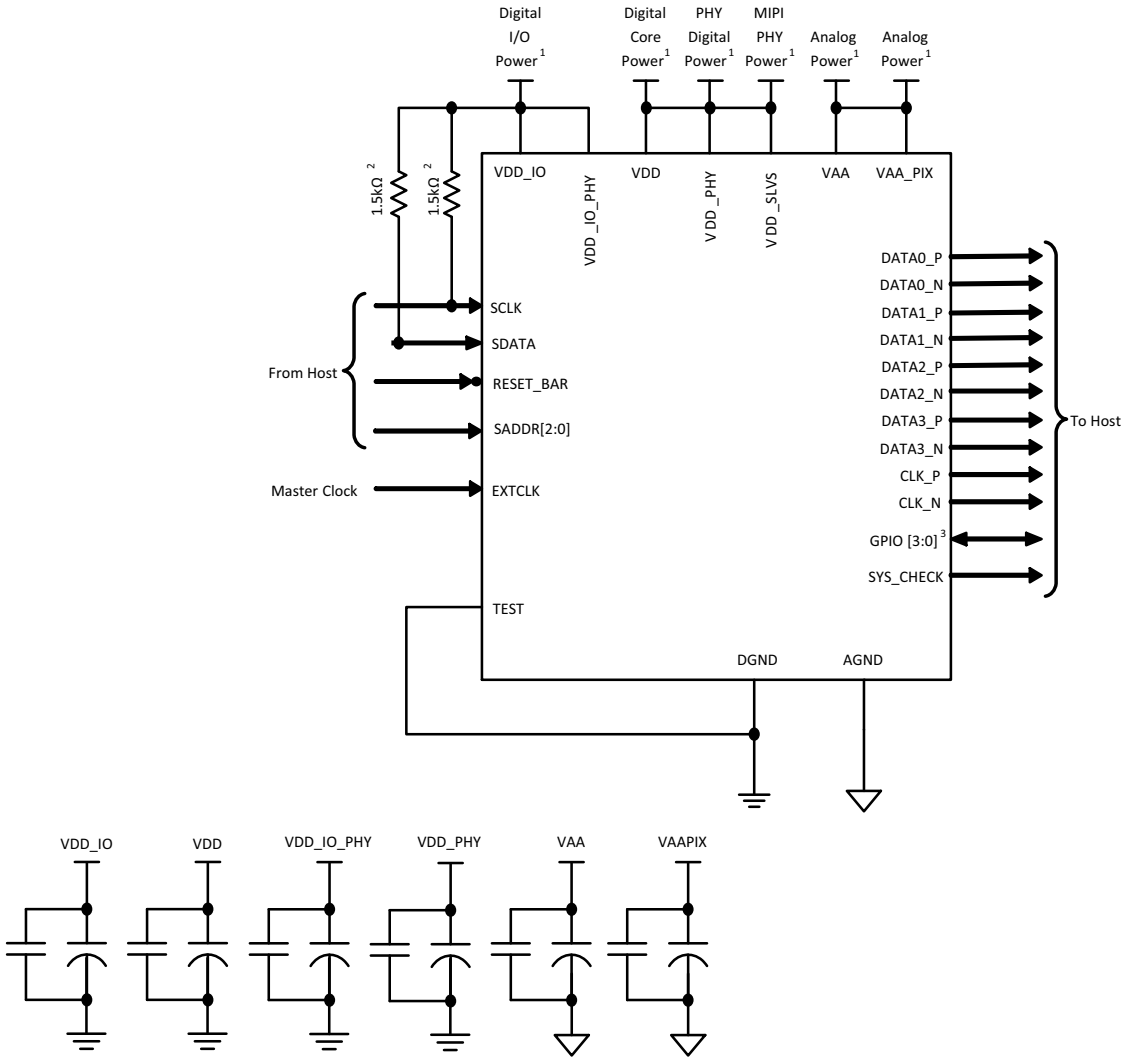

Figure 4. Typical Configuration, 4−Lane MIPI

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on lay− out and design considerations. Refer to the AR0143AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. 1/0 signals voltage must be configured to match VDD_10 voltage to minimize any leakage currents.

PIXEL DATA FORMAT

Pixel Array Structure

While the sensor's format is 1344x968, additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for mono− chrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

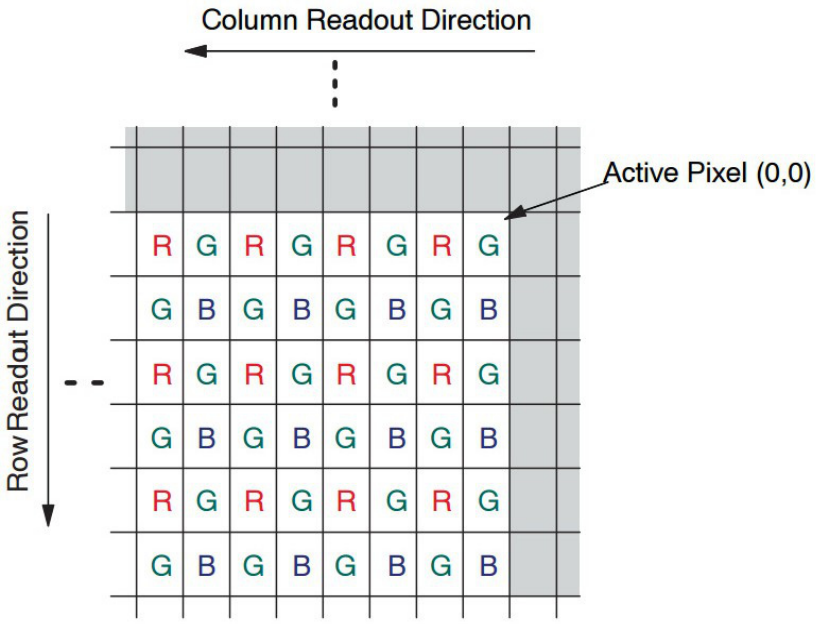

Figure 5. Pixel Color Pattern Detail (Top Right Corner)

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 5). This reflects the actual layout of the array on the die. Also, the first readable pixel location of the sensor in default condition is that of physical pixel address (256, 6). This first readable pixel location corresponds to the register X_ADDR_START_ (R0x3004)=0x0000 and the register Y_ADDR_START_ (R0x3002)=0x0000.

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 6. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 6.

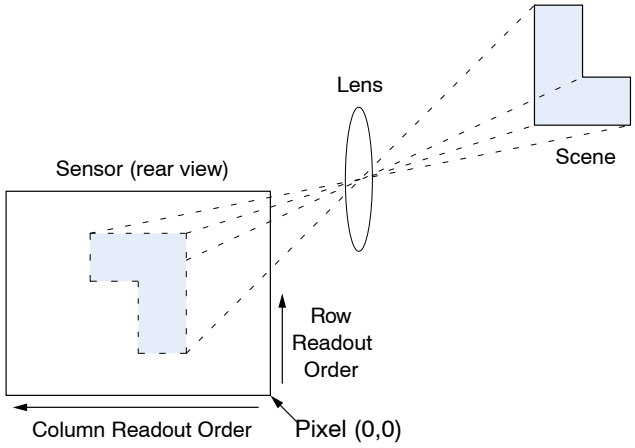

Figure 6. Imaging a Scene

OPERATING MODES AND FEATURES

For a complete description, recommendations, and usage guidelines for product features, refer to the AR0143AT Developer Guide.

3.0 μm Dual Conversion Gain Pixel

To improve the low light performance and keep the high dynamic range, a large (3.0 μm) dual conversion gain pixel is implemented for better image optimization. With a dual conversion gain pixel, the conversion gain of the pixel may be dynamically changed to better adapt the pixel response based on dynamic range of the scene. This gain can be switched manually or automatically by an external auto exposure control module.

Dual conversion gain can also be controlled independently for each exposure in HDR mode, allowing a mixture of high conversion gain (HCG) and low conversion gain (LCG) across multiple exposures.

Resolution

The active array supports a maximum of 1344 x 968 pixels to support 720p resolution. Utilizing a 3.0 μm pixel will result in an optical format of 1/4−inch.

Frame Rate

At full resolution, the AR0143AT is capable of running up to 60 fps in parallel, MIPI, and HiSPi modes, depending on the number of exposures. The AR0143AT has a maximum frame rate of 60fps at full resolution in 3−exposure HDR, 2−exposure HDR and linear modes.

High Dynamic Range

The AR0143AT can operate in an HDR mode to acquire video data using ON Semiconductor's multi−exposure technology. This allows the sensor to handle >120 dB of intrascene dynamic range. The sensor also features a linear or standard dynamic range (SDR) mode where a single image is captured. In HDR mode, the sensor sequentially captures up to four exposures by maintaining separate read and reset pointers that are inter− leaved within the rolling shutter readout. The intermediate pixel values are stored in line buffers while waiting for all the exposure values to be present. As soon as all exposure values are available, they are combined to create a linearized 20−bit value for each pixel's response. This 20−bit value may be output directly or optionally companded to 16, 14 or 12-bits before output.

The exposure ratios may be set to 2x, 4x, 8x, 16x, or 32x, or can be individually controlled per exposure to allow a wide range of flexible exposure ratios. The individual exposure ratio control for T1, T2, T3, and T4 is limited by the number of line buffers allocated to each exposure.

Options to output each individual exposures only, or pixel interleaved data are also available. Individual exposures may be read out in a line interleaved mode as described in the Line Interleaved Mode section.

Motion Compensation and Linearization

In typical multi−exposure HDR systems, motion artifacts can be created when objects move during the integration time of the exposures used to construct the image. When this happens, edge artifacts can potentially be visible and might look like a tearing or ghosting effect. To correct for this issue, the AR0143AT incorporates both motion compensation and improved digital lateral overflow (DLO2) algorithm, but with the addition of individual color knee points as well as an additional knee point for the fourth exposure.

LED Flicker Mitigation (LFM)

LED sign flicker causes traffic signs to be incorrectly read in bright daylight conditions as the LEDs may be illuminated when the sensor is not integrating. The AR0143AT includes a new mode, LFM, for reading these signs. In LFM mode, the effective sensitivity of the pixel can be controlled and reduced, enabling exposure times to be extended. On AR0143AT variants with color CFAs, color will be maintained in the sensor output to aid in sign discrimination.

Multi−camera Synchronization

AR0143AT supports multi−camera synchronization Slave modes. The Slave modes support synchronization of multiple cameras within 8 pixel clocks from the beginning of FRAME_VALID/LINE_VALID from sensors without reducing the maximum frame rate. This feature saves the line memory buffer at the host system to combine a multiple of video input streams from the sensors.

Slave Mode

The slave mode feature of the AR0143AT supports triggering the start of a frame readout from an input signal that is supplied from an external ASIC. The slave mode signal allows for precise control of frame rate and register change updates.

Context Switching and Register Updates

The user has the option of using the highly configurable context memory, or a simplified implementation in which only a subset of registers is available for switching. The AR0143AT supports a highly configurable context switching RAM of size 256 x 16. Within this Context Memory, changes to registers within the chip may be stored. The register set for each context must be the same, but the number of contexts and registers per context are limited only by the size of the context memory.

Alternatively, the user may switch between two predefined register sets A and B by writing to a context switch change bit. When the context switch is configured to context A the sensor will reference the context A registers. If the context switch is changed from A to B during the readout of frame n, the sensor will then reference the context

B coarse_integration_time registers in frame n+1 and all other context B registers at the beginning of reading frame n+2. The sensor will show the same behavior when changing from context B to context A. The following registers are context switchable:

Table 3. LIST OF CONFIGURABLE REGISTERS FOR CONTEXT A AND CONTEXT B

Context A Register Description	Context B Register Description
coarse_integration_time	coarse_integration_time_cb
coarse_integration_time2	coarse_integration_time2_cb
coarse_integration_time3	coarse_integration_time3_cb
coarse_integration_time4	coarse_integration_time4_cb
fine_integration_time	fine_integration_time_cb
fine_integration_time2	fine_integration_time2_cb
fine_integration_time3	fine_integration_time3_cb
fine_integration_time4	fine_integration_time4_cb
exposure_ratio	exposure_ratio_cb
line_length_pck	line_length_pck_cb
frame_length_lines	frame_length_lines_cb
row_bin	row_bin_cb
col_bin	col_bin_cb
fine_gain	fine_gain_cb
coarse_gain	coarse_gain_cb
x_addr_start	x_addr_start_cb
y_addr_start	y_addr_start_cb
x_addr_end	x_addr_end_cb
y_addr_end	y_addr_end_cb
y_odd_inc	y_odd_inc_cb
x_odd_inc	x_odd_inc_cb
green1_gain	green1_gain_cb
blue_gain	blue_gain_cb
red_gain	red_gain_cb
green2_gain	green2_gain_cb
global_gain	global_gain_cb
operation_mode_ctrl	operation_mode_ctrl_cb
bypass_pix_comb	bypass_pix_comb_cb

Embedded Data and Statistics

The AR0143AT has the capability to output image data and statistics within the frame timing. There are two types of information embedded within the frame readout.

Embedded data can be enabled on two rows before the active image pixels are displayed, and shows the current settings for the part.

Embedded statistics can be enabled on the two rows after the active image pixels are displayed, and include frame identifiers and histogram information for that image. This can be used by off−chip auto−exposure blocks to make decisions about exposure adjustment.

Histograms for up to two independent regions of interest (ROIs) can be tracked per frame, with programmable registers determining their size and location. Two compression methods are available for the histogram data, with one being a new logarithmic compression scheme that enables more detailed data for dark portions of the image. Note that histogram information can be output for only one pixel plane at a time.

In addition to histograms, the output image frame can be split into a virtual grid of up to 16 ROIs that can each provide the average pixel value for that region. The grid for ROIs is defined by four offset pointers for each axis (X and Y), as shown in Figure 8. Each of these averages can be included with the statistics embedded in the output image, allowing a simple exposure metric for each region to be generated.

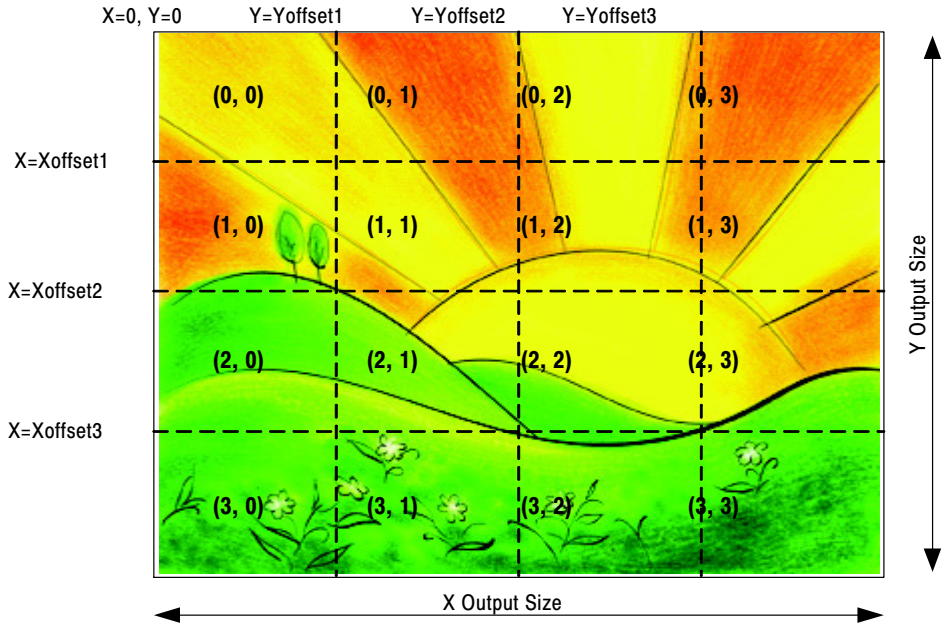

Figure 7. Grid−ROI, Configuration 1; x_grid_status=0x3; y_grid_status=0x3

Black Level Control/Correction

Black level correction can optionally be automatically controlled by the AR0143AT; the default setting is for automatic black level calibration to be enabled. The automatic black level correction measures the average value of pixels from a set of optically black pixel rows in the image sensor. The pixels are averaged as if they were light sensitive and passed through the appropriate gain. This line average is then digitally low−pass filtered over many frames to remove temporal noise and random instabilities associated with this measurement. The optically black lines may be read out, bypassing the datapath, for off−chip analysis. The automatic black level correction can be disabled and the black level set manually via register settings. Manual black level settings are frame synchronized to the next start of frame.

Row and Column Correction

Row and column noise correction is applied automatically by the image sensor on a frame by frame basis. Re−triggering of correction circuits due to settings or temperature changes are not necessary. The digital gain can be applied before HDR linearization for white balancing, and after HDR linearization for increasing scene brightness.

Defective Pixel Tracking/Correction

Defective Pixel Correction (DPC) is intended to compensate or tag defective pixels by replacing their value with a value based on the surrounding pixels, or tagging them by assigning them a ‘0’ value. The defect pixel correction feature supports up to 200 defects. The locations of defective pixels are stored in a table on chip during the manufacturing process; this table is accessible through the two−wire serial interface. There is no provision for later augmenting the defect table entries. The DPC algorithm is one−dimensional, calculating the resulting averaged pixel value based on nearby pixels within a row. The algorithm distinguishes between color and monochrome parts; for color parts, the algorithm uses nearest neighbor in the same color plane. The defect pixel correction algorithm may be disabled. (Note that the outgoing defect specification for the AR0143AT assumes the defect correction is disabled). The defect pixels identified during manufacture can be read from on−chip ROM via the 2−wire control interface.

Analog/Digital Gains

A programmable analog gain of 0.125x to 8x applied simultaneously to all color channels will be featured along with a digital gain of 1x to 16x that may be configured on a per color channel basis. Future releases will have an option to separate the digital gain for use as an AWB function and as a global gain.

Skipping/Binning Modes

The AR0143AT supports subsampling. Subsampling allows the sensor to read out a smaller set of active pixels by either skipping, binning, or summing pixels within the readout window. Horizontal binning is achieved in the digital readout. The sensor will sample the combined two adjacent pixels within the same color plane. Vertical row binning is applied in the pixel readout. Row binning can be configured as two rows within the same color plane. Pixel skipping can be configured up to two in both the x− direction and y−direction. Skipping pixels in the x−direction will not reduce the row time. Skipping pixels in the y direction will reduce the number of rows from the sensor effectively reducing the frame time. Skipping will introduce image artifacts from aliasing. The AR0143AT supports row wise vertical binning. Row wise vertical summing is not supported.

ASIL / ISO26262 Support Features

The AR0143AT incorporates many features to assist ASIL−B system compliance to be achieved by a system that integrates it. Please refer to the AR0143AT Safety Manual for more information.

SYSTEM INTERFACES

This section describes the AR0143AT interfaces. Note that all output port options may not be available on all packaging options.

HiSPi Pixel Output Port

The AR0143AT provides a 4−lane HiSPi pixel output port with support for SLVS and HiVCM modes. Supported configurations are described in Table 4. Additional information is provided in the ON Semiconductor HiSPi Protocol and Physical Layer documents.

Table 4. HiSPi PROTOCOL SUPPORT

Lanes	Width	Data type	Protocols	Max. Mbps/lane	Notes
1, 2, or 4	20-bit	Bayer/RAW	SP-packetized SP-streaming Streaming−S	750 Mbps	HDR output mode (uncompressed)
1, 2, or 4	16-bit	Bayer/RAW	SP-packetized SP-streaming Streaming−S	750 Mbps	HDR output mode (compressed)
1, 2, or 4	14-bit	Bayer/RAW	SP-packetized SP-streaming Streaming−S	750 Mbps	HDR output mode (compressed)
1, 2, or 4	12-bit	Bayer/RAW	SP-packetized SP-streaming Streaming−S	750 Mbps	SDR (linear) mode

MIPI CSI−2 Pixel Output Port

The AR0143AT provides a 4−lane MIPI CSI-2 pixel output port. The data protocol support is per Table 5. Please contact ON Semiconductor for additional information.

Table 5. MIPI PROTOCOL SUPPORT

Lanes	Width	Data type	Protocols	Max. Mbps/lane	Notes
1, 2, or 4	20−bit	Bayer/RAW	SP−packetized SP−streaming	750 Mbps	HDR output mode (uncompressed)
1, 2, or 4	16-bit	Bayer/RAW	SP−packetized SP−streaming	750 Mbps	HDR output mode (compressed)
1, 2, or 4	14-bit	Bayer/RAW	SP-packetized SP-streaming	750 Mbps	HDR output mode (compressed)
1, 2, or 4	12-bit	Bayer/RAW	SP-packetized SP-streaming	750 Mbps	SDR (linear) mode

Parallel Pixel Output Port

The AR0143AT provides a 12−bit data pixel output port with frame and line valid signals. HDR data is companded to 12−bit, and 12−bit SDR (non-HDR) data may be output via this port.

Note that the parallel port cannot be used to output combinations of individual T1/T2/ T3/T4 exposures on a per frame basis.

Line Interleaved Output

The AR0143AT will have the capability to output the T1, T2, T3, and T4 exposures separately, in a line interleaved format. The purpose of this is to enable off chip HDR linear combination and processing.

Embedded data and statistics are also supported in line interleaved mode. See the AR0143AT Developer Guide for more information.

Two−Wire Sensor Control Interface

The two−wire serial interface bus enables read/write access to control and status registers within the AR0143AT. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off−chip by a 1.5 kΩ resistor. Either the slave or master device can drive SDATA LOW−the interface protocol determines which device is allowed to drive SDATA at any given time. The protocols described in the two−wire serial interface specification allow the slave device to drive SCLK LOW; the AR0143AT uses SCLK as an input only and therefore never drives it LOW.

ELECTRICAL SPECIFICATIONS

Table 6. ELECTRICAL SPECIFICATIONS

Symbol	Definition	Min	Nominal	Max	Unit
VDD	Core digital voltage	1.14	1.2	1.26	V
VDD_IO	I/O digital voltage	1.7/2.6	1.8/2.8	1.9/3.0	V
VAA	Analog voltage	2.6	2.8	3.0	V
VAA_PIX	Pixel supply voltage	2.6	2.8	3.0	V
VDD_PHY	PHY supply voltage	1.14	1.2	2.16	V
VDD_IO_PHY	Serial PHY supply voltage	1.7 /2.6	1.8/2.8	1.9/3.0	V
VDD_SLVS	HiSPi supply voltage (SLVS)	0.3	0.4	0.6	V
VDD_SLVS	HiSPi supply voltage (HiVCM)	1.14	1.2	2.16	V

NOTE: VAA_PIX must always be equal to VAA.

Power Up

For controlled power up, RESET_BAR pin must be asserted (low) before supplies can be sequenced up in any order (except VPP, which should be left unconnected). Once all supplies are valid, RESET_BAR is de−asserted (high), the part will begin boot−up on EXTCLK.

Power Down

For controlled power down, streaming must be first disabled. The RESET_BAR pin must be asserted (low) before any external supplies are removed. Then the supplies are allowed to be sequenced off in any order.

Typical Power Down Sequence:

1. De−assert Streaming: Set software standby mode (mode_select = 0) register.
2. Wait till the end of the current frame (or end−of−line if so configured).
3. Configure I/O for “hold” if desired. “Hold” state requires maintaining VDD_IO; however.
4. Set RESET_BAR = 0. (Hard Standby, low−leakage state)
5. Wait t0 power−down delay.
6. Power off supplies in any order. For “hold” I/O state, do not power off VDD_IO supply.

Two−Wire Serial Register Interface

The electrical characteristics of the two−wire serial register interface (SCLK, SDATA) are shown in Figure 8 and Table 7.

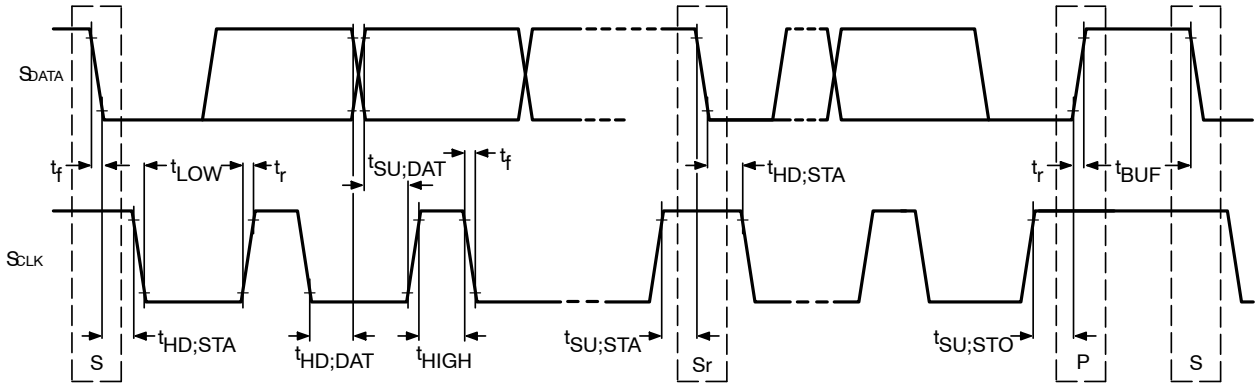

Figure 8. Two−Wire Serial Bus Timing Parameters

NOTE: Read sequence: For an 8−bit READ, read waveforms start after WRITE command and register address are issued.

Table 7. TWO−WIRE SERIAL BUS CHARACTERISTICS
fEXTCLK = 27 MHz; VDD = 1.2 V; VDD_IO = 2.8 V; VAA = 2.8 V; VAA_PIX = 2.8 V; T_A = 25°C

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Clock Frequency	fSCL	0	100	0	400	0	1000	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	4.0	–	0.6	–	0.26	–	μs
LOW period of the SCLK clock	tLOW	4.7	–	1.2	–	0.5	–	μs
HIGH period of the SCLK clock	tHIGH	4.0	–	0.6	–	0.26	–	μs
Set−up time for a repeated START condition	tSU;STA	4.7	–	0.6	–	0.26	–	μs
Data hold time	tHD;DAT	2 (Note 4)	3.45 (Note 5)	0 (Note 6)	0.9 (Note 5)	0 (Note 6)	–	μs
Data set-up time	tSU;DAT	250	–	100 (Note 6)	–	50 (Note 6)	–	ns
Rise time of both SDATA and SCLK signals	tr	–	1000	20 + 0.1Cb (Note 7)	300	20 + 0.1Cb (Note 7)	120	ns
Fall time of both SDATA and SCLK signals	tf	–	300	20 + 0.1Cb (Note 7)	300	20 + 0.1Cb (Note 7)	120	ns
Set−up time for STOP condition	tSU;STO	4.0	–	0.6	–	0.26	–	μs
Bus free time between a STOP and START condition	tBUF	4.7	–	1.3	–	0.5	–	μs
Capacitive load for each bus line	Cb	–	400	–	400	–	500	pF
Serial interface input pin capacitance	CIN_SI	–	3.3	–	3.3	–	3.3	pF
SDATA max load capacitance	CLOAD_SD	–	30	–	30	–	30	pF
SDATA pull−up resistor	RSD	1.5	4.7	1.5	4.7	1.5	4.7	kΩ

1. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.
2. Two−wire control is I²C−compatible.
3. All values referred to V_{IHmin} = 0.9 VDD and V_{ILmax} = 0.1 VDD levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
5. The maximum ^{t}HD;DAT has only to be met if the device does not stretch the LOW period (^{t}LOW) of the SCLK signal.
6. A Fast−mode I²C−bus device can be used in a Standard−mode I²C−bus system, but the requirement tSU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line ^{t}r max + ^{t}SU;DAT = 1000 + 250 = 1250 ns (according to the Standard−mode I²C−bus specification) before the SCLK line is released.
7. Cb = total capacitance of one bus line in pF.

I/O Timing

By default, the AR0143AT launches pixel data, FV, and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV, and LV using the rising edge of PIXCLK.

See Figure 9 below and Table 8 on page 15 for I/O timing (AC) characteristics.

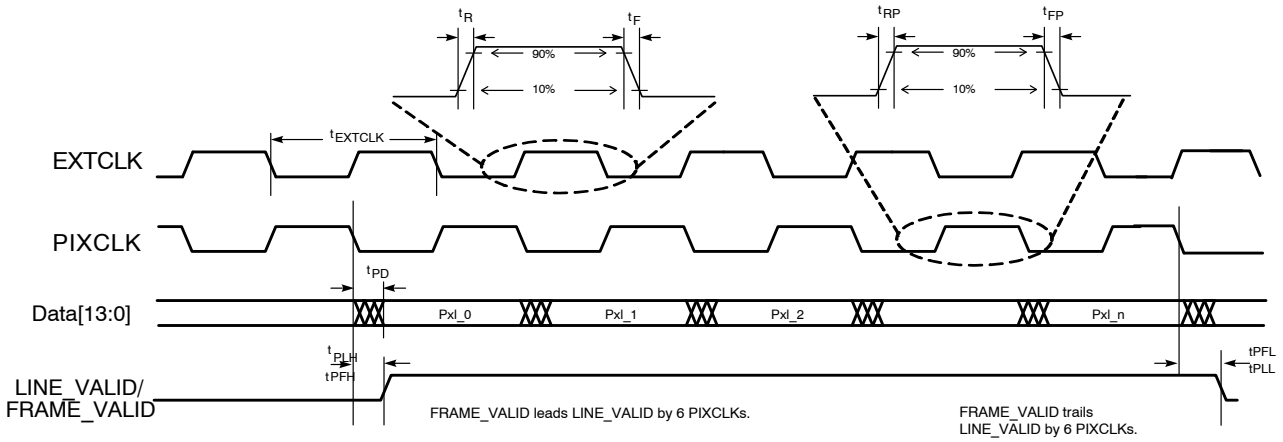

Figure 9. I/O Timing Diagram

Table 8. I/O TIMING CHARACTERISTICS (Note 8)

Symbol	Definition	Condition	Min	Typ	Max	Unit
fEXTCLK1	Input clock frequency	PLL Enabled	6 (Note 9)	–	48	MHz
tEXTCLK1	Input clock period	PLL Enabled	15.6	–	166	ns
t_R	Input clock rise time		–	TBD	–	ns
t_F	Input clock fall time		–	TBD	–	ns
tRP	Pixclk rise time		–	TBD	–	ns
tFP	Pixclk fall time		–	TBD	–	ns
	Clock duty cycle	PLL Enabled	40	50	60	%
tPIX JITTER	Jitter on PIXCLK		–	TBD		ns
tCP	EXTCLK to PIXCLK propagation delay	Nominal voltages, PLL Disabled	–	TBD	–	ns
fPIXCLK	PIXCLK frequency	Default, Nominal Voltages	6		99.43	MHz
tPD	PIXCLK to data valid	Default, Nominal Voltages	–	TBD	–	ns
tPFH	PIXCLK to FV HIGH	Default, Nominal Voltages	–	TBD	–	ns
tPLH	PIXCLK to LV HIGH	Default, Nominal Voltages	–	TBD	–	ns
tPFL	PIXCLK to FV LOW	Default, Nominal Voltages	–	TBD	–	ns
tPLL	PIXCLK to LV LOW	Default, Nominal Voltages	–	TBD	–	ns
CLOAD	Output load capacitance		–	<10	–	pF
CIN	Input pin capacitance		–	2.5	–	pF

8. I/O timing characteristics are measured under the following conditions:
   a. Temperature is 25°C ambient
   b. 10 pF load
   c. 1.8 V I/O supply voltage
9. When using a 1 MHz two−wire interface clock, the minimum clock frequency is 16 MHz.

HiSPi Electrical Specifications

The ON Semiconductor AR0143AT sensor supports both SLVS and HiVCM HiSPi modes. Please refer to the High−Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The VDD_SLVS supply in this datasheet corresponds to VDD_TX in the HiSPi Physical Layer Specification. Similarly, VDD is equivalent to VDD_HiSPi as referenced in the specification. The DLL as implemented on AR0143AT is limited in the number of available delay steps and differs from the HiSPi specification as described in this section.

Table 9. CHANNEL SKEW

Measurement Conditions: VDD_HiSPi = 1.8 V;VDD_HiSPi_TX = 0.4 V; Data Rate = 480 Mbps; DLL set to 0

Data Lane Skew in Reference to Clock	tCHSKEW1PHY	−150	ps

POWER−ON RESET AND STANDBY TIMING

Power−Up Sequence

A typical power−up sequence:

1. Set RESET_BAR low
2. Power up supplies (except VPP, which should be left unconnected).
3. Wait for current to be applied on t0, t1, t2, controlled by external supply slew rate (See Figure 10).
4. When external supplies valid, set RESET_BAR high.
5. HOST config through IIC.
6. Set STREAMING bit.
7. PLL internally enables and locks.
8. AR0143AT enters streaming mode.

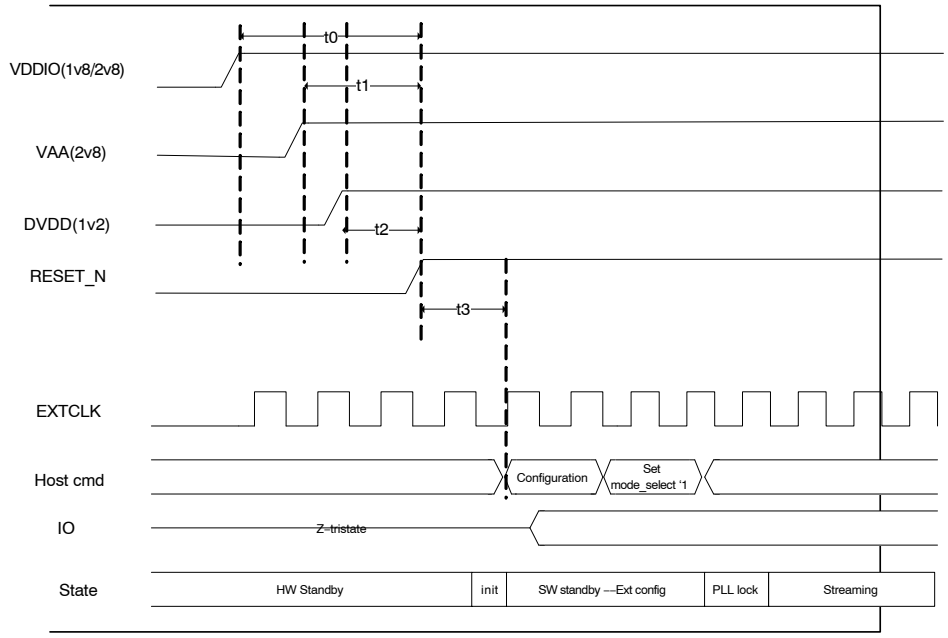

Figure 10. Initial Power−Up Sequence

Table 10. AR0143AT PIN LIST

PIN Name	iBGA Pin	Type	Descriptions	Comments
EXTCLK	H2	Input	Master input clock. PLL input clock.	Connect to clock source. Min and Max frequency depends upon output port and clocking method.
RESET_BAR	H8	Input	Asynchronous active−low reset.	Connect to host.
SCLK	C5	Input	CCI clock for access to control and status registers.	Connect to host.
SDATA	D7	Input/Output	CCI data for reads from and writes to control and status registers.	Connect to host.
SADDR0	C7	Input	CCI interface device address select bit 0.	Selects CCI address. 000b sets the address to 0x20/0x21. 001b sets the address to 0x30/0x31. Connect to VDD_IO or DGND accordingly.
SADDR1	C6	Input	CCI interface device address select bit 1.	
SADDR2	D8	Input	CCI interface device address select bit 2.	
PIXCLK	H5	Output	Parallel data output pixel clock. Used to qualify the LINE_VALID, FRAME_VALID and DOUT11 to DOUT0 outputs.	Connect to host/receiver or can be left floating if not used. Use DOUT[11:0] for 12−bit parallel configuration.
FRAME_VALID	H7	Output	Parallel data output FRAME_VALID output. Qualified by PIXCLK.	
LINE_VALID	G7	Output	Parallel data output LINE_VALID output. Qualified by PIXCLK.	
DOUT11	G6	Output	Parallel data output pixel data bit 11. Qualified by PIXCLK.	Connect to host/receiver or can be left floating if not used. Use DOUT[11:0] for 12−bit parallel configuration.
DOUT10	F6	Output	Parallel data output pixel data bit 10. Qualified by PIXCLK.	
DOUT9	G5	Output	Parallel data output pixel data bit 9. Qualified by PIXCLK.	
DOUT8	F5	Output	Parallel data output pixel data bit 8. Qualified by PIXCLK.	
DOUT7	E5	Output	Parallel data output pixel data bit 7. Qualified by PIXCLK.	
DOUT6	D5	Output	Parallel data output pixel data bit 6. Qualified by PIXCLK.	
DOUT5	H4	Output	Parallel data output pixel data bit 5. Qualified by PIXCLK.	
DOUT4	G4	Output	Parallel data output pixel data bit 4. Qualified by PIXCLK.	
DOUT3	F4	Output	Parallel data output pixel data bit 3. Qualified by PIXCLK.	
DOUT2	E4	Output	Parallel data output pixel data bit 2. Qualified by PIXCLK.	
DOUT1	D4	Output	Parallel data output pixel data bit 1. Qualified by PIXCLK.	
DOUT0	H3	Output	Parallel data output pixel data bit 0. Qualified by PIXCLK.	Connect to host/receiver or can be left floating if not used. Use DOUT[11:0] for 12−bit parallel configuration.

Table 10. AR0143AT PIN LIST

PIN Name	iBGA Pin	Type	Descriptions	Comments
CLK_P	E1	Output	Differential Mipi/HiSpi serial clock.	Connect to host/receiver or can be left floating if not used. Use DATA0 for 1 lane configuration or DATA0 and DATA1 for 2 lane configuration.
CLK_N	E2	Output	Differential Mipi/HiSpi serial clock.	
DATA3_P	C1	Output	Differential Mipi/HiSpi serial data lane 3.	
DATA3_N	C2	Output	Differential Mipi/HiSpi serial data lane 3.	
DATA2_P	D1	Output	Differential Mipi/HiSpi serial data lane 2.	
DATA2_N	D2	Output	Differential Mipi/HiSpi serial data lane 2.	
DATA1_P	F1	Output	Differential Mipi/HiSpi serial data lane 1.	
DATA1_N	F2	Output	Differential Mipi/HiSpi serial data lane 1.	
DATA0_P	G1	Output	Differential Mipi/HiSpi serial data lane 0.	
DATA0_N	G2	Output	Differential Mipi/HiSpi serial data lane 0.	
TEST	D6	Input	Enable manufacturing test modes.	Tie to DGND.
ATEST1	B7	Input/Output	Analog manufacturing test access	Leave unconnected.
ATEST2	B6	Input/Output	Analog manufacturing test access	
ATEST3	B5	Input/Output	Analog manufacturing test access	
ATEST4	B4	Input/Output	Analog manufacturing test access	
GPIO0	F7	Input/Output	GPIO Pin 0	GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
GPIO1	E8	Input/Output	GPIO Pin 1	
GPIO2	E7	Input/Output	GPIO Pin 2	
GPIO3	E6	Input/Output	GPIO Pin 3	
SYS_CHECK	G8	Output	Combined OR of error flags	Leave unconnected if not used.
TEMP_FLAG	H6	Output	Temperature monitoring flag	Leave unconnected if not used.
DGND	J1, B3, E3, G3, A4, C4, J5, A7, C8, F8, A9, J9	Power	Digital ground.	
VDD	B1, J2, J4, A5, J7, F9, H9	Power	Core Digital power.	
VDD_PHY	D3	Power	PHY Digital power.	Connect to VDD
VDD_IO	H1, B2, J3, A6, J6, J8, E9, G9	Power	Digital I/O power.	
AGND	A3, B8	Power	Analog ground.	
VAA	A2, A8, C9	Power	Analog power.	
VAA_PIX	B9	Power	Analog pixel array power.	Connect to VAA
VDD_IO_PHY	C3	Power	Power to MIPI and HiSPi PHYs.	Use 1.8 V nominal for HiSPi HiVCM or Sub−LVDS. Use 1.8 V or 2.8 V nominal for MIPI or HiSPi SLVS. Tie to VDD_IO when Parallel interface is used.
VDD_SLVS	F3	Power	Reference voltage for HiSPi serial interface.	Set according to desired HiSPi output common mode voltage. Use 0.4 V nominal for HiSPi SLVS, otherwise use 1.2 V nominal. Tie to VDD when MIPI is being used
VPP	D9	Power	High voltage supply for programming OTPM.	Leave unconnected.

PACKAGE DIMENSIONS

TBD
CASE TBD
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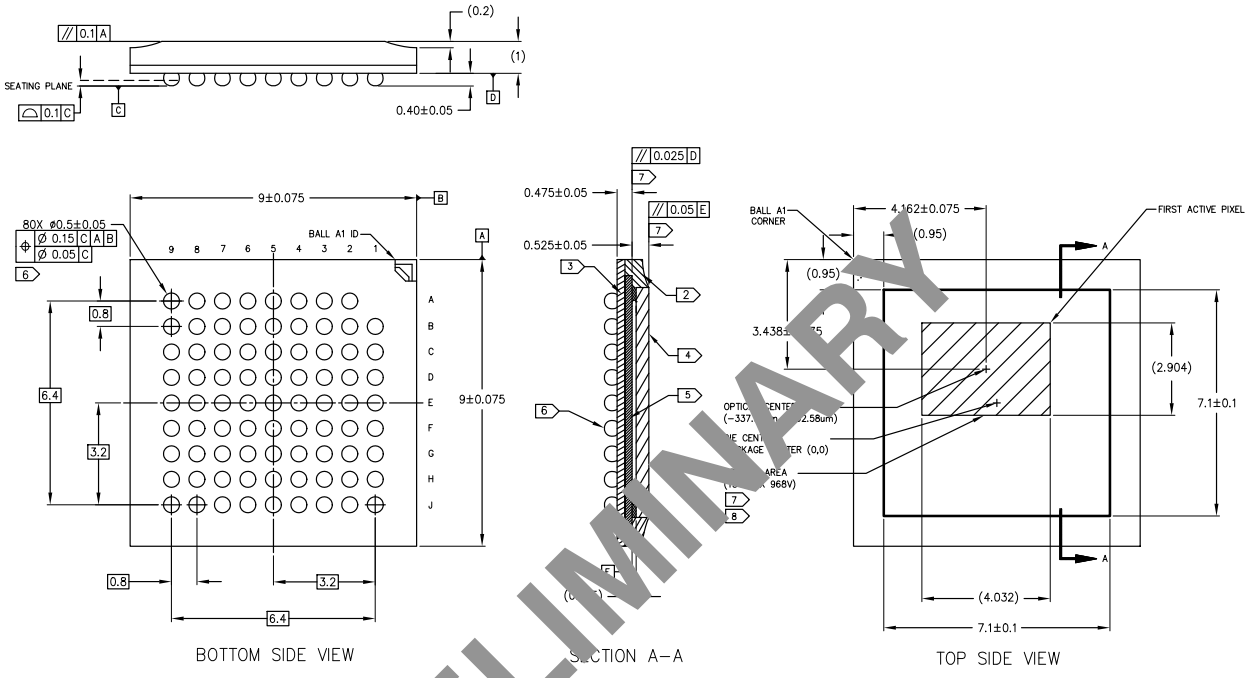

	1	2	3	4	5	6	7	8	9
A		VAA2V8	[illegible]ND	DGND	DVDD1V2	VDDIO2V8R1V8	DGND	VAA2V8	DGND
B	DVDD1V2	VDDIO2V8R1V8	DG[illegible]	ATEST4	ATEST3	ATEST2	ATEST1	AGND	VAA2V8_PIX
C	DATA3P	DATA3N	[illegible]1V8R1V2_PHY	DGND	SCL	SADDR1	SADDR0	DGND	VAA2V8
D	DATA2P	DATA2N	[illegible]VDD1V2_PHY	DOUT1	DOUT6	TEST	SDA	SADDR2	VAAHV_NPIX
E	CLKP	CLKN	DGND	DOUT2	DOUT7	GPIO_3	GPIO_2	GPIO_1	VDDIO2V8R1V8
F	DATA1P	DATA1N	DVDD1V2R0V4_SLVS_PHY	DOUT3	DOUT8	DOUT10	GPIO_0	DGND	DVDD1V2
G	DATA0P	DATA0N	DGND	DOUT4	DOUT9	DOUT11	LINE_VALID	SYS_CHECK	VDDIO2V8R1V8
H	VDDIO2V8R1V8	EXTCLK	DOUT0	DOUT5	PIXCLK	TEMP_FLAG	FRAME_VALID	RESET_N	DVDD1V2
J	DGND	DVDD1V2	VDDIO2V8R1V8	DVDD1V2	DGND	VDDIO2V8R1V8	DVDD1V2	VDDIO2V8R1V8	DGND

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