TLV755P 500-mA, Low I_Q, Small Size, Low Dropout Regulator

1 Features

- Input Voltage Range: 1.44 V to 5.5 V
- Available in Fixed-Output Voltages:
  - 0.6 V to 5 V (50-mV Steps)
- Low I_Q: 25 µA (Typical)
- Low Dropout:
  - 220 mV (Maximum) at 500 mA (3.3 V_{OUT})
- Output Accuracy: 1% (Typical)
- Built-In Soft-Start With Monotonic V_{OUT} Rise
- Foldback Current Limit
- Active Output Discharge
- High PSRR: 45 dB at 100 kHz
- Stable With a 1-µF Ceramic Output Capacitor
- Packages:
  - 2.9-mm × 1.6-mm SOT-23-5
  - 1-mm x 1-mm X2SON-4
  - 2 mm × 2 mm WSON-6

2 Applications

- Set-Top Boxes, TV, and Gaming Consoles
- Portable and Battery-Powered Equipment
- Desktop, Notebooks, and Ultrabooks
- Tablets and Remote Controls
- White Goods and Appliances
- Grid Infrastructure and Protection Relays
- Camera Modules and Image Sensors

3 Description

The TLV755P low-dropout regulator (LDO) device is an ultra-small, low quiescent current LDO that sources 500 mA with good line and load transient performance. The TLV755P is optimized for a wide variety of applications by supporting an input voltage range from 1.44 V to 5.5 V. To minimize cost and solution size, the device is offered in fixed output voltages ranging from 0.6 V to 5 V to support the lower core voltages of modern microcontroller (MCUs). Additionally, the TLV755 has a low I_Q with enable functionality to minimize standby power. This device features an internal soft-start to lower inrush current, thus providing a controlled voltage to the load and minimizing the input voltage drop during start up. When shutdown, the device actively pulls down the output to quickly discharge the outputs and ensure a known start-up state.

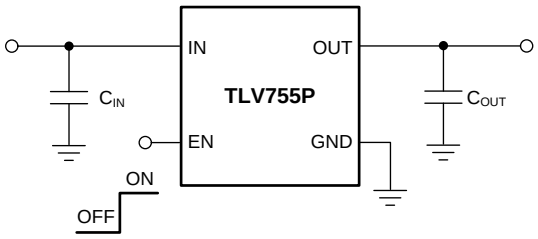
The TLV755P is stable with small ceramic output capacitors allowing for a small overall solution size. A precision band-gap and error amplifier provides a typical accuracy of 1%. All device versions have integrated thermal shutdown, current limit, and undervoltage lockout (UVLO). The TLV755P has an internal foldback current limit that helps reduce the thermal dissipation during short-circuit events.

Device Information(1)

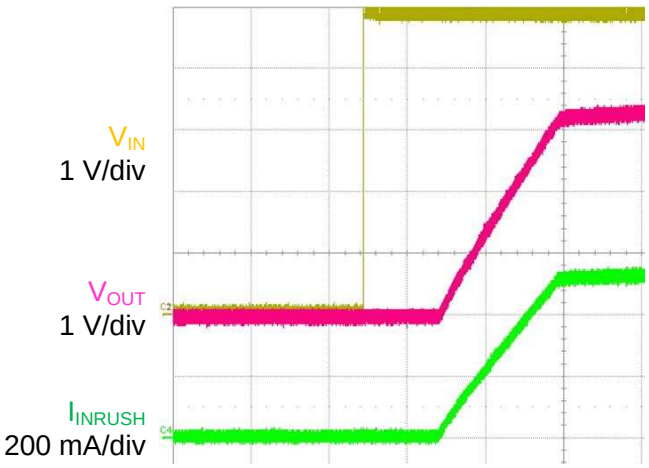
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV755P	X2SON (4)	1.00 mm × 1.00 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	SON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Startup Waveform



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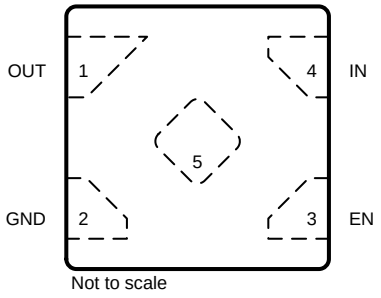
4 Revision History

DATE	REVISION	NOTES
November 2017	*	Initial release.

5 Pin Configuration and Functions

DQN Package
6-Pin X2SON
Top View



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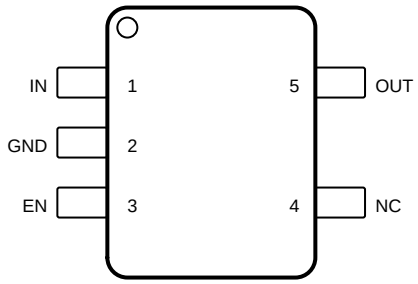
DBV Package
5-Pin SOT-23
Top View



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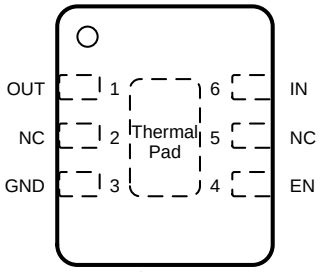
DRV Package
6-Pin WSON With Exposed Thermal Pad
Top View



Not to scale

NC = no internal connection.

Pin Functions

PIN				I/O	DESCRIPTION
NAME	DQN	DBV	DRV		
EN	3	3	4	I	Enable pin. Drive EN greater than V_{HI} to turn on the regulator. Drive EN less than V_{LO} to place the LDO into shutdown mode.
GND	2	2	3	—	Ground pin.
IN	4	1	6	I	Input pin. A capacitor with a value of 1 µF or larger is required from this pin to ground(1). See the *Input and Output Capacitor Selection* section for more information.
NC	—	4	2, 5	—	No internal connection.
OUT	1	5	1	O	Regulated output voltage pin. A capacitor with a value of 1 µF or larger is required from this pin to ground(1). See the *Input and Output Capacitor Selection* section for more information.
Thermal pad	—	—	Pad	—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

(1) The nominal input and output capacitance must be greater than 0.47 µF; throughout this document the nominal derating on these capacitors is 50%. Take care to ensure that the effective capacitance at the pin is greater than 0.47 µF.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	6	
	Output, V_{OUT}	–0.3	V_{IN} + 0.3(2)	
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 6 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
C_{IN}	Input capacitor	1			µF
C_{OUT}	Output capacitor	1		200	µF
V_{IN}	Input voltage	1.44		5.5	V
V_{OUT}	Output voltage	0.6		5	V
I_{OUT}	Output current	0		500	mA
V_{EN}	Enable voltage	0		5.5	V
f_{EN}	Enable toggle frequency			10	kHz
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV755P			UNIT
		DQN (X2SON)	DBV (SOT-23)	DRV (WSON)	
		4 Pins	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	168.4	231.1	100.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	139.1	118.4	108.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.4	64.4	64.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.6	28.4	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	101.7	63.8	64.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	88.4	N/A	34.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT} + 0.5 V or 1.44 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.44		5.5	V
V_{OUT}	Output voltage			0.6		5	V
	Output accuracy	T_J = 25°C		–1%		1%	
		–40°C ≤ T_J ≤ +85°C, V_{OUT} ≥ 1 V		–1%		1%	
		–40°C ≤ T_J ≤ +85°C, 0.6 V ≤ V_{OUT} < 1 V		–10		10	mV
		V_{OUT} ≥ 1 V		–1.5%		1.5%	
		0.6 V ≤ V_{OUT} < 1 V		–15		15	mV
$(\Delta_{VOUT})_{\Delta VIN}$/ V_{OUT}	Line regulation	V_{OUT} + 0.5 V(1) ≤ V_{IN} ≤ 5.5 V	V_{OUT} > 1.5 V		0.01%		
ΔV_{OUT}/ ΔI_{OUT}	Load regulation	0.1 mA ≤ I_{OUT} ≤ 500 mA, V_{IN} ≥ 2.4 V	DQN package		0.018		V/A
			DBV package		0.030		
			DRV package		0.022		
I_{GND}	Ground current	T_J = 25°C, I_{OUT} = 0 mA		14	25	31	µA
		–40°C ≤ T_J ≤ +85°C, I_{OUT} = 0 mA				33	
		–40°C ≤ T_J ≤ +125°C, I_{OUT} = 0 mA				40	
I_{SHDN}	Shutdown current	V_{EN}= 0 V, 1.44 V ≤ V_{IN} ≤ 5.5 V, –40°C ≤ T_J ≤ +125°C			0.1	1	µA
I_{CL}	Output current limit	V_{IN} = V_{OUT} + $V_{DO(MAX)}$ + 0.25 V	V_{OUT} = V_{OUT} – 0.2 V, V_{OUT} ≤ 1.5 V	600	720	865	mA
			V_{OUT} = 0.9 × V_{OUT}, 1.5 V < V_{OUT} ≤ 4.5 V	600	720	865	
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V			355		mA
V_{DO}	Dropout voltage(2)	I_{OUT} = 500 mA, –40°C ≤ T_J ≤ +85°C	0.6 V ≤ V_{OUT} < 0.8 V		675	700	mV
			0.8 V ≤ V_{OUT} < 1 V		600	650	
			1 V ≤ V_{OUT} < 1.2 V		550	575	
			1.2 V ≤ V_{OUT} < 1.5 V		500	525	
			1.5 V ≤ V_{OUT} < 1.8 V		350	400	
			1.8 V ≤ V_{OUT} < 2.5 V		325	375	
			2.5 V ≤ V_{OUT} < 3.3 V		250	300	
			3.3 V ≤ V_{OUT} ≤ 5.0 V		150	212	
		I_{OUT} = 500 mA, –40°C ≤ T_J ≤ +125°C	0.6 V ≤ V_{OUT} < 0.8 V			725	
			0.8 V ≤ V_{OUT} < 1 V			675	
			1 V ≤ V_{OUT} < 1.2 V			600	
			1.2 V ≤ V_{OUT} < 1.5 V			550	
			1.5 V ≤ V_{OUT} < 1.8 V			425	
			1.8 V ≤ V_{OUT} < 2.5 V			400	
			2.5 V ≤ V_{OUT} < 3.3 V			325	
			3.3 V ≤ V_{OUT} ≤ 5.0 V			238	
PSRR	Power-supply rejection ratio	f = 1 kHz, V_{IN} = V_{OUT} + 1 V, I_{OUT} = 50 mA			52		dB
		f = 100 kHz, V_{IN} = V_{OUT} + 1 V, I_{OUT} = 50 mA			46		
		f = 1 MHz, V_{IN} = V_{OUT} + 1 V, I_{OUT} = 50 mA			52		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 1.2 V, I_{OUT} = 50 mA			71.5		μV_{RMS}
V_{UVLO}	Undervoltage lockout	V_{IN} rising		1.21	1.3	1.44	V
$V_{UVLO, HYST}$	Undervoltage lockout hysteresis	V_{IN} falling			40		mV

(1) V_{IN} = 1.44 V for V_{OUT} < 0.9 V.
(2) Dropout is measured when V_{OUT} is 5% below $V_{OUT(NOM)}$.

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Electrical Characteristics (continued)

over operating free-air temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT} + 0.5 V or 1.44 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Startup time	Time from EN assertion to 0.95 × V_{OUT}		400		µs
V_{HI}	EN pin high voltage (enabled)		0.9			V
V_{LO}	EN pin low voltage (enabled)				0.4	V
I_{EN}	Enable pin current	EN = 5.5 V, V_{IN} = 5.5 V		10		nA
$R_{PULLDOWN}$	Pulldown resistance	V_{IN} = 3.3 V		120		Ω
T_{SD}	Thermal shutdown	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		155		

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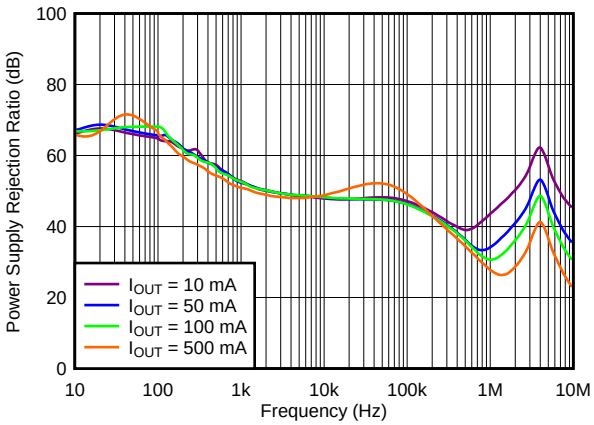
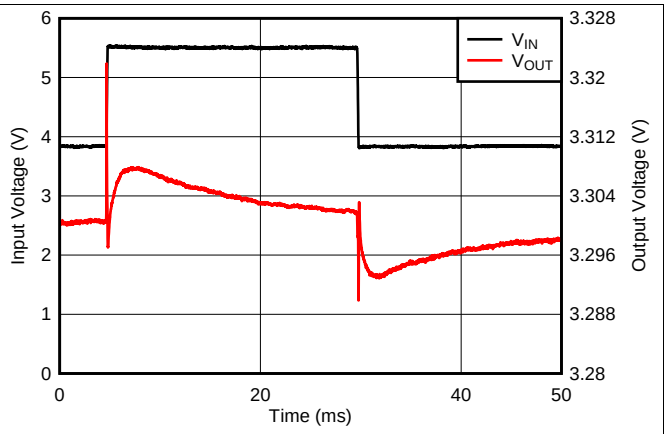
6.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.4 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



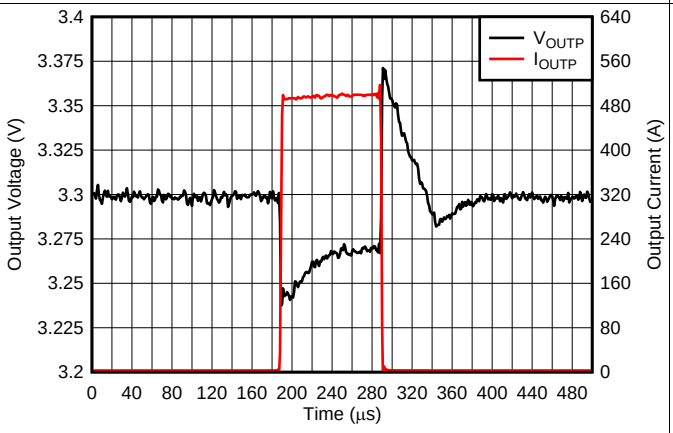
V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF

Figure 1. PSRR vs Frequency and I_{OUT}



V_{OUT} = 3.3 V, C_{OUT} = 1 µF, V_{IN} slew rate = 1 V/µs

Figure 2. Line Transient



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF, I_{OUT} slew rate = 1 A/µs

Figure 3. 1-mA to 500-mA Load Transient

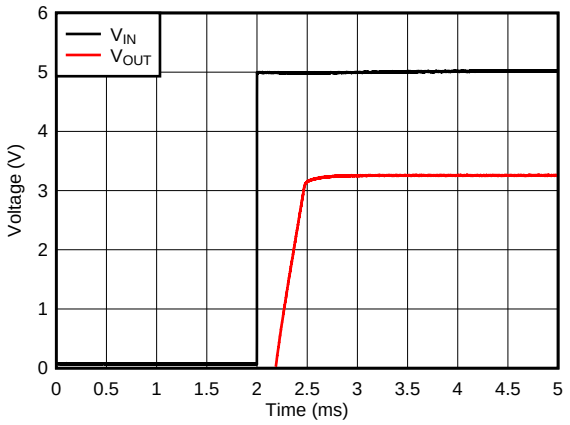


Figure 4. V_{IN} = V_{EN} Power-Up

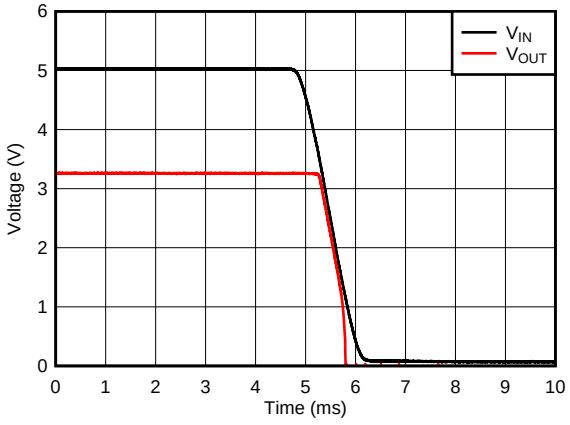


Figure 5. V_{IN} = V_{EN} Shutdown

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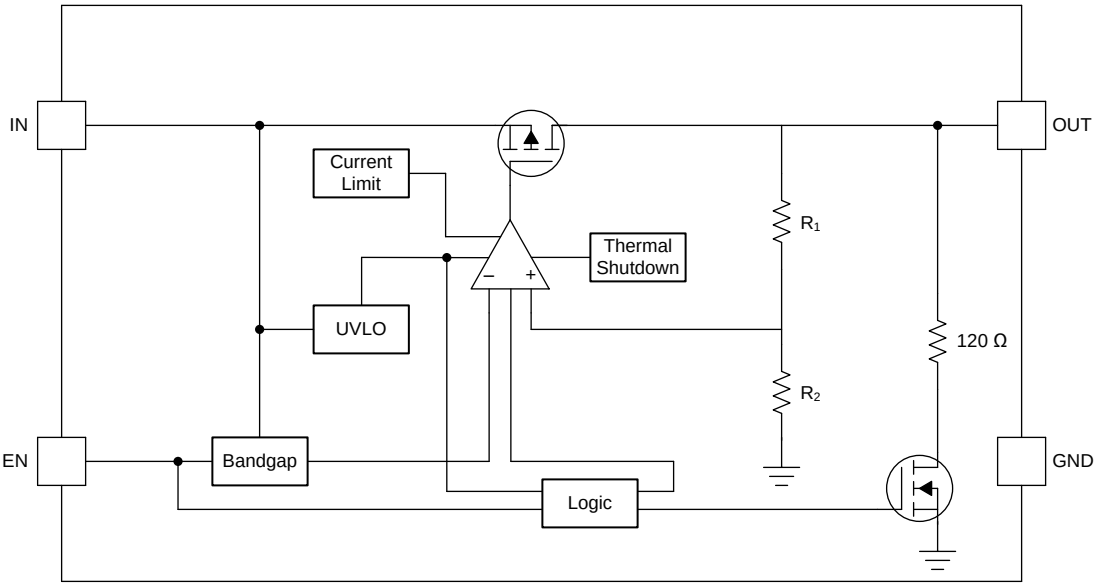
7 Detailed Description

7.1 Overview

The TLV755P belongs to a family of next-generation, low-dropout regulators (LDOs). This device consumes low quiescent current and delivers excellent line and load transient performance. The TLV755P is optimized for a wide variety of applications by supporting an input voltage range from 1.4 V to 5.5 V. To minimize cost and solution size, the device is offered in fixed output voltages ranging from 0.6 V to 5 V to support the lower core voltages of modern MCUs.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature is –40°C to +125°C.

7.2 Functional Block Diagram



NOTE: $R_1 + R_2$ = TBD.

7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit disables the output until the input voltage is greater than the rising UVLO voltage (V_{UVLO}). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When V_{IN} is less than V_{UVLO}, the output is connected to ground with a 120-Ω pulldown resistor.

7.3.2 Enable (EN)

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed V_{HI}. Turn off the device by forcing the EN pin below V_{LO}. If shutdown capability is not required, connect EN to IN.

The device has an internal pulldown resistor that connects a 120-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. Equation 1 calculates the time constant τ:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

Feature Description (continued)

7.3.3 Internal Foldback Current Limit

The TLV755P has an internal current limit that protects the regulator during fault conditions. The current limit is a hybrid brick-wall scheme until the output voltage is less than 0.4 × $V_{OUT(NOM)}$. When the voltage drops below 0.4 × $V_{OUT(NOM)}$, a foldback current limit is implemented that scales back the current as the output voltage approaches GND. When the output shorts, the LDO supplies a typical current of I_{SC}. The output voltage is not regulated when the device is in current limit. In this condition, the output voltage is the product of the regulated current and the load resistance. When the device output shorts, the PMOS pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}] until thermal shutdown is triggered and the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown.

The foldback current-limit circuit limits the current that is allowed through the device to current levels lower than the minimum current limit at nominal V_{OUT} current limit (I_{CL}) during start up. Figure 6 shows typical current limit values. If the output is loaded by a constant-current load during start up, or if the output voltage is negative when the device is enabled, then the load current demanded by the load may exceed the foldback current limit and the device may not rise to the full output voltage. For constant-current loads, disable the output load until the output rises to the nominal voltage.

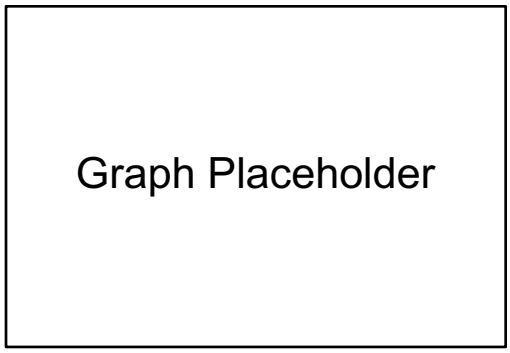


Figure 6. TLV755 Current Limit vs V_{OUT}

7.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 165°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation and protects the circuit from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the device into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

Table 1 lists a comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal(1)	$V_{IN} > V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{HI}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout(1)	$V_{IN} < V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{HI}$	—	$T_J < T_{SD}$
Disabled(2)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{LO}$	—	$T_J > T_{SD}$

(1) All table conditions must be met.
(2) The device is disabled when any condition is met.

7.4.1 Normal Operation

The device regulates to the nominal output voltage when all following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device degrades because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, right after being in a normal regulation state, but not during startup), the pass-FET is driven as hard as possible when the control loop is out of balance. During the normal time required for the device to regain regulation, $V_{IN} \geq V_{OUT(NOM)} + V_{DO}$, V_{OUT} can overshoot $V_{OUT(NOM)}$ during fast transients.

7.4.3 Disabled

The output is shut down by forcing the enable pin below V_{LO}. When disabled, the pass device is turned off, internal circuits are shut down, and the output voltage is actively discharged to ground by an internal switch from the output to ground. The active pulldown resistor is on when sufficient input voltage is provided.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Selection

The TLV755P requires an output capacitance of 0.47 µF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in capacitance value and equivalent series resistance (ESR) over temperature. When selecting a capacitor for a specific application, consider the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. As a general rule, ceramic capacitors must be derated by 50%. For best performance, TI recommends a maximum output capacitance value of 200 µF.

Place a 1-µF capacitor on the input pin of the LDO. Some input supplies have a high impedance, which places the input capacitor on the input supply and reduces the input impedance. This capacitor counteracts reactive input sources and improves transient response and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors are used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are expected, or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

Use a PMOS pass transistor achieves low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales linearly with the output current because the PMOS device functions like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation. Figure 7 shows typical dropout values.

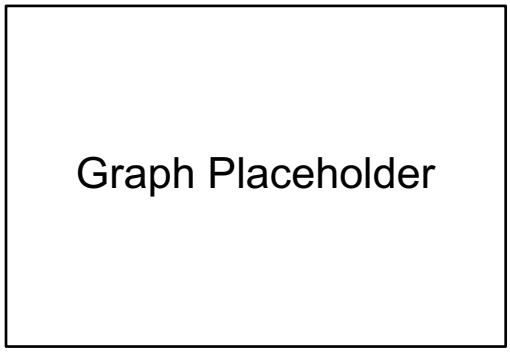


Figure 7. Dropout vs V_{IN}

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Application Information (continued)

8.1.3 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} for start-up. As with other LDOs, the output overshoots on recovery from these conditions. Figure 8 shows that a ramping input supply causes an LDO to overshoot on start-up when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

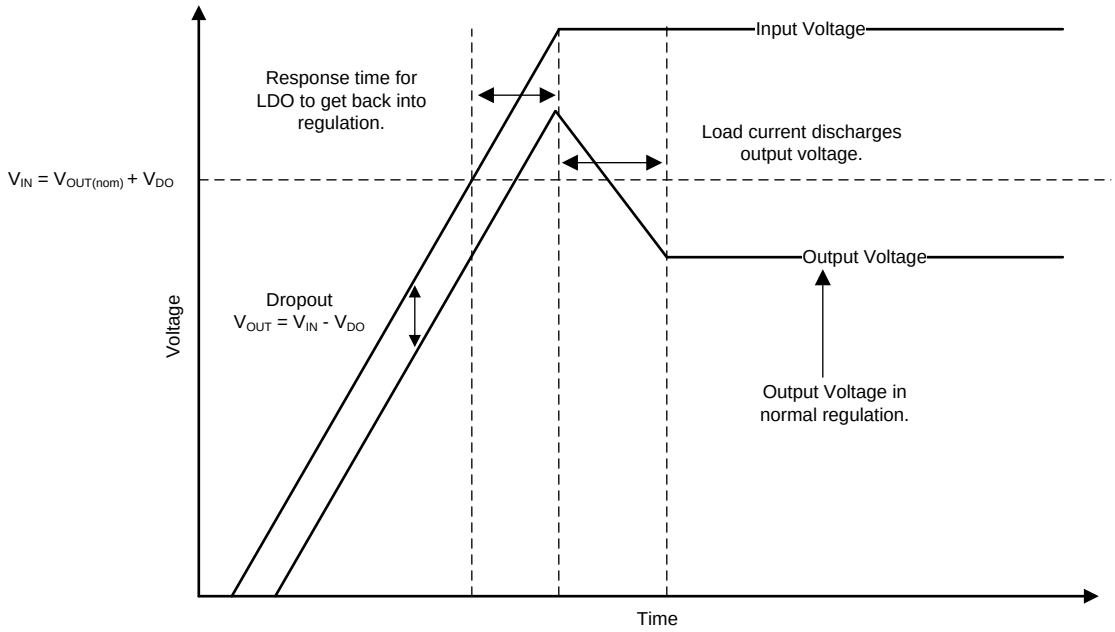

Figure 8. Startup Into Dropout

8.1.4 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

ADVANCE INFORMATION

Application Information (continued)

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection must be used to protect the device. Figure 9 shows one approach of protecting the device.

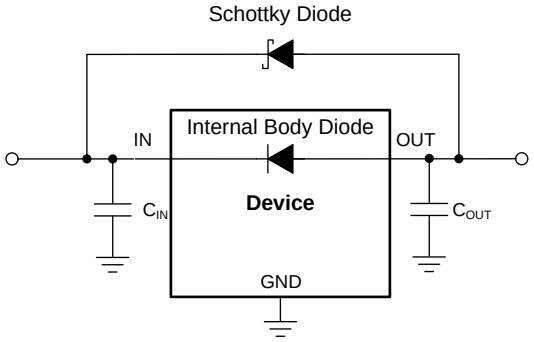

Figure 9. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free of other heat-generating devices as possible that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use Equation 2 to approximate P_D:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation must be minimized to achieve greater efficiency. This minimizing process is achieved by selecting the correct system voltage rails. Proper selection helps obtain the minimum input-to-output voltage differential. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to Equation 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB, device package, and the temperature of the ambient air (T_A).

$$T_J = T_A + R_{\theta JA} \times P_D \quad (3)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ value recorded in the table is determined by the JEDEC standard, PCB, and copper-spreading area. The $R_{\theta JA}$ value is only used as a relative measure of package thermal performance. $R_{\theta JA}$ is the sum of the DRV package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

ADVANCE INFORMATION

Application Information (continued)

8.1.5.1 Estimating Junction Temperature

The JEDEC standard recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not thermal resistances, but offer practical and relative means of estimating junction temperatures. These psi metrics are independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 4 and are given in the table.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as described in Equation 2
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

(4)

8.2 Typical Application

This application shows a typical use case for the TLV755, where the device converts from 2.5 V to 1.8 V for a common MCU core rail.

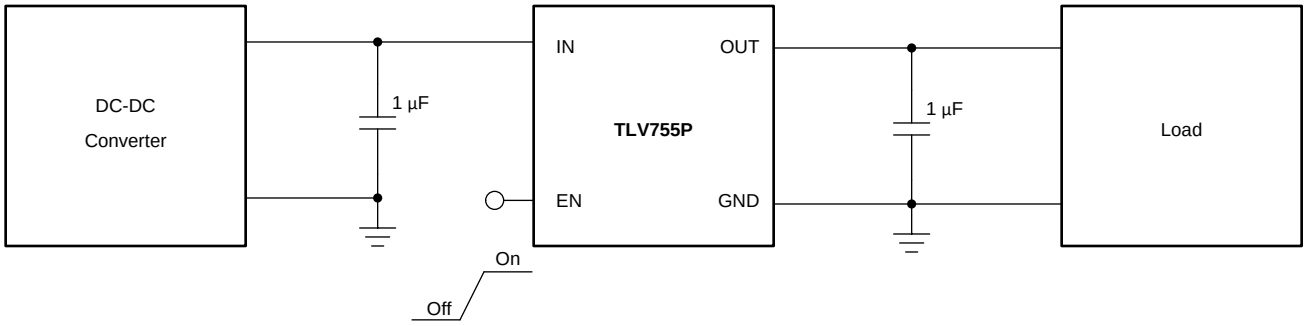

Figure 10. TLV755P Typical Application

8.2.1 Design Requirements

Table 2 lists the design requirements for this application.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	2.5 V
Output voltage	1.8 V
Input current	400 mA (maximum)
Output load	300-mA dc
Maximum ambient temperature	85°C

ADVANCE INFORMATION

8.2.2 Detailed Design Procedure

8.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During startup, the input current is higher as a result of the inrush current charging the output capacitor. Use Equation 5 to calculate the current through the input.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right]$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turnon ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance (5)

8.2.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use Equation 6 to calculate the power dissipation. As Equation 7 shows, multiply P_D by $R_{\theta JA}$ and add the ambient temperature (T_A) to calculate the junction temperature (T_J).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (6)$$

$$T_J = R_{\theta JA} \times P_D + T_A \quad (7)$$

If the ($T_{J(MAX)}$) value does not exceed 125°C, use Equation 8 to calculate the maximum ambient temperature. Equation 9 calculates the maximum ambient temperature with a value of 103.39°C.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (8)$$

$$T_{A(MAX)} = 125°C - 102.9 \times (2.5\ V - 1.8\ V) \times (0.3\ A) = 103.39°C \quad (9)$$

9 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV755P. If the input source is reactive, consider using multiple input capacitors in parallel with the 1-µF input capacitor to lower the input supply impedance over frequency.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close as possible to the device
- Use copper planes for device connections to optimize thermal performance
- Place thermal vias around the device to distribute the heat

ADVANCE INFORMATION

10.2 Layout Examples

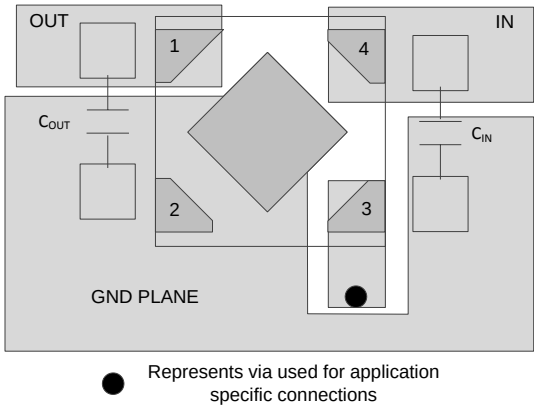

Figure 11. Layout Example: DQN Package

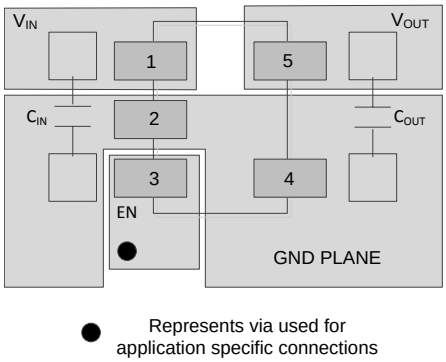

Figure 12. Layout Example: DBV Package

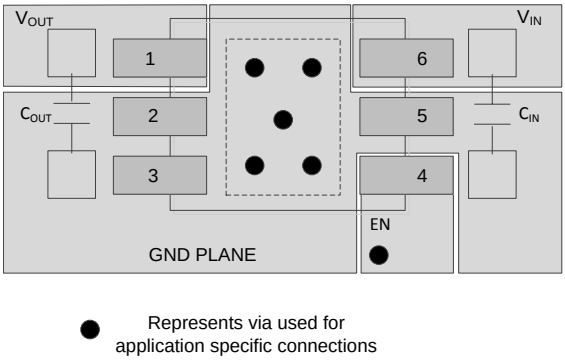

Figure 13. Layout Example: DRV Package

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Table 3. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TLV755**xx(x)Pyyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **P** indicates an active output discharge feature. All members of the TLV755 family will actively discharge the output when the device is disabled. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.6 V to 5 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV75507PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75509PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75510PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75510PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75512PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75512PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75515PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75515PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75518PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75518PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75519PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75519PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75525PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75525PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75528PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75528PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75529PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75530PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75530PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV75533PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV75533PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

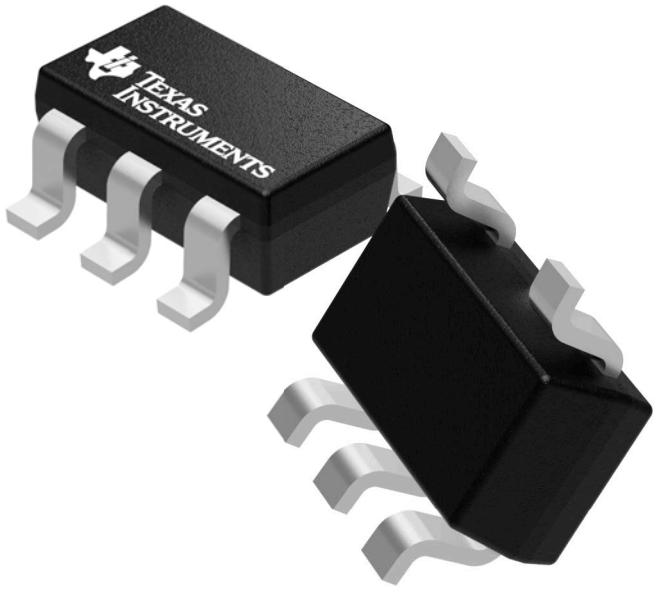
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



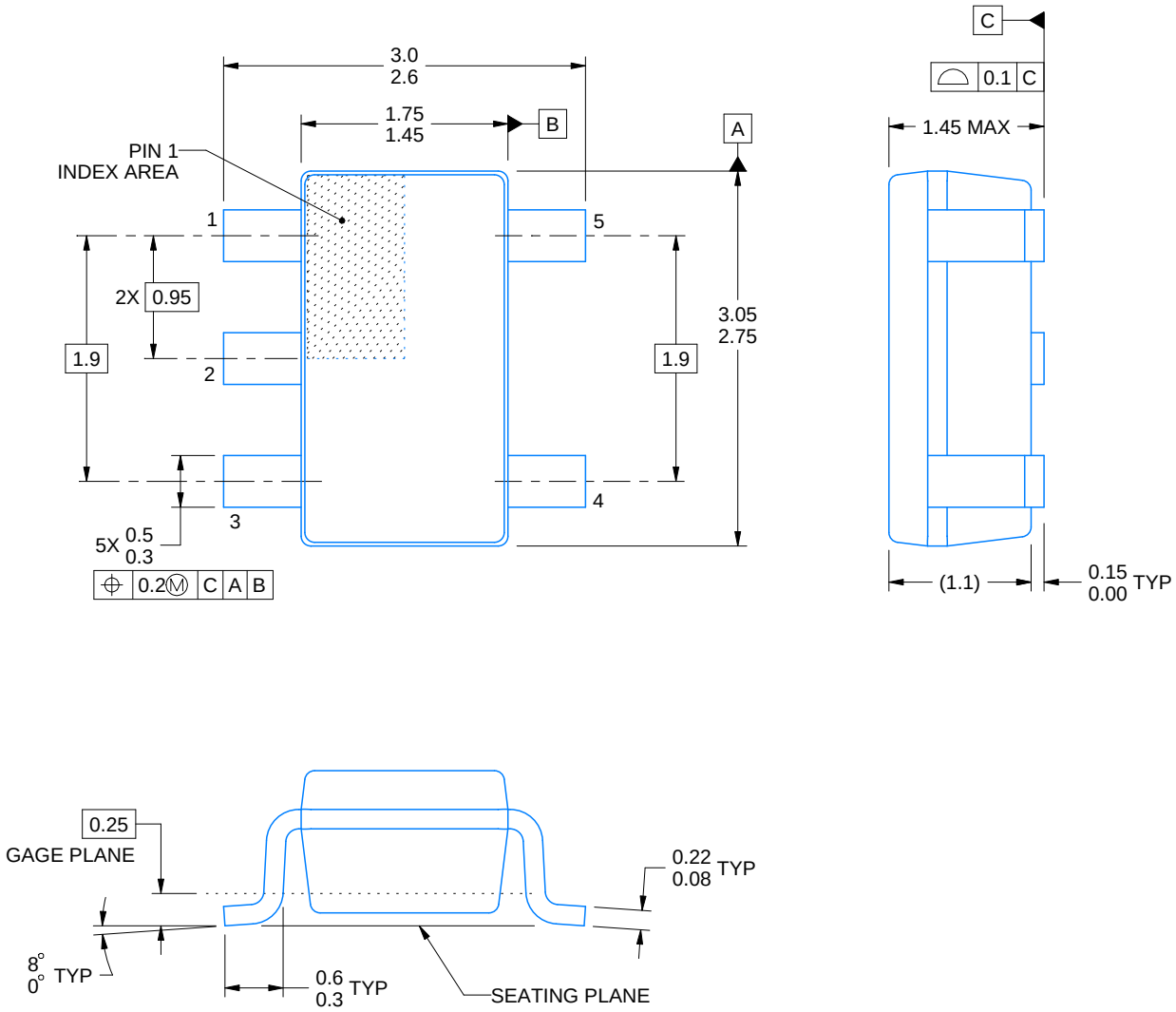
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

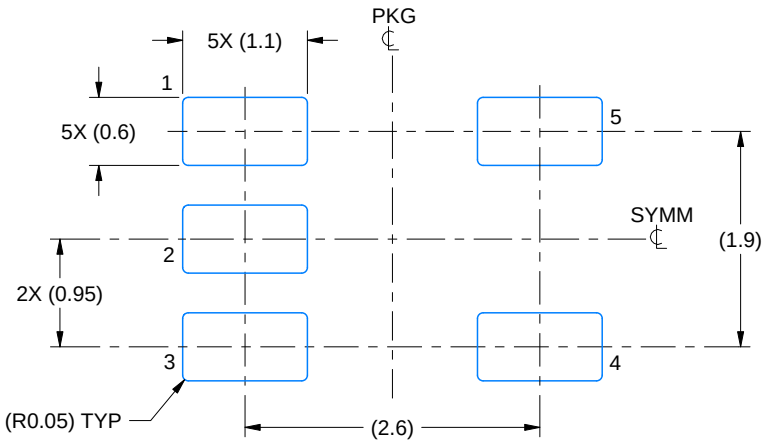
SMALL OUTLINE TRANSISTOR



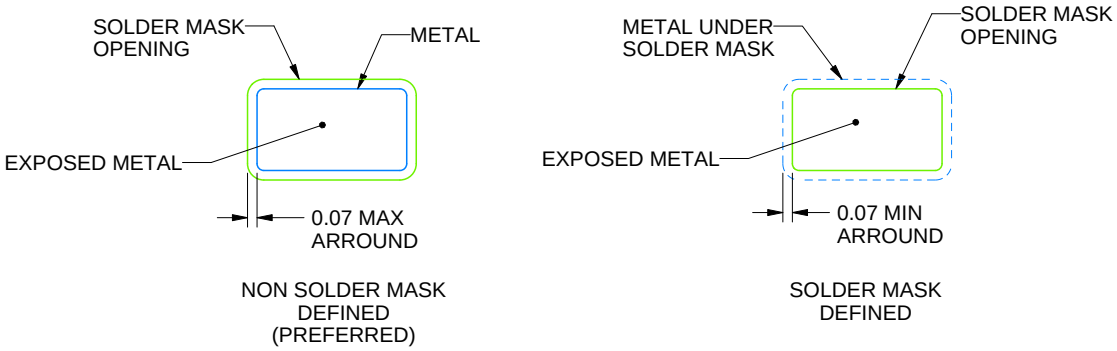
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

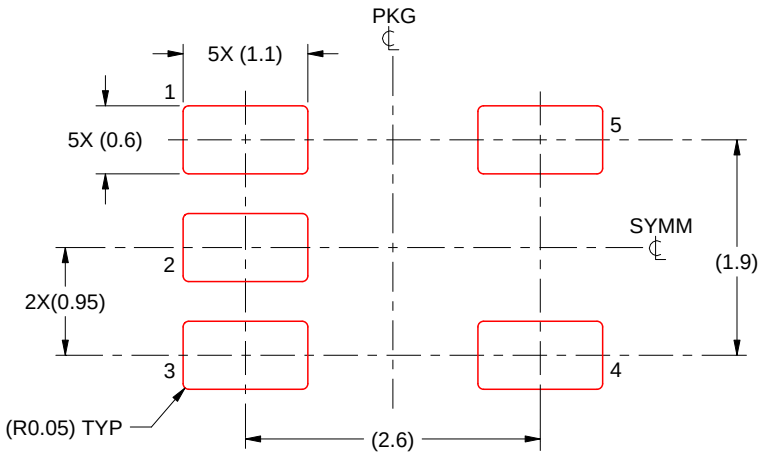


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

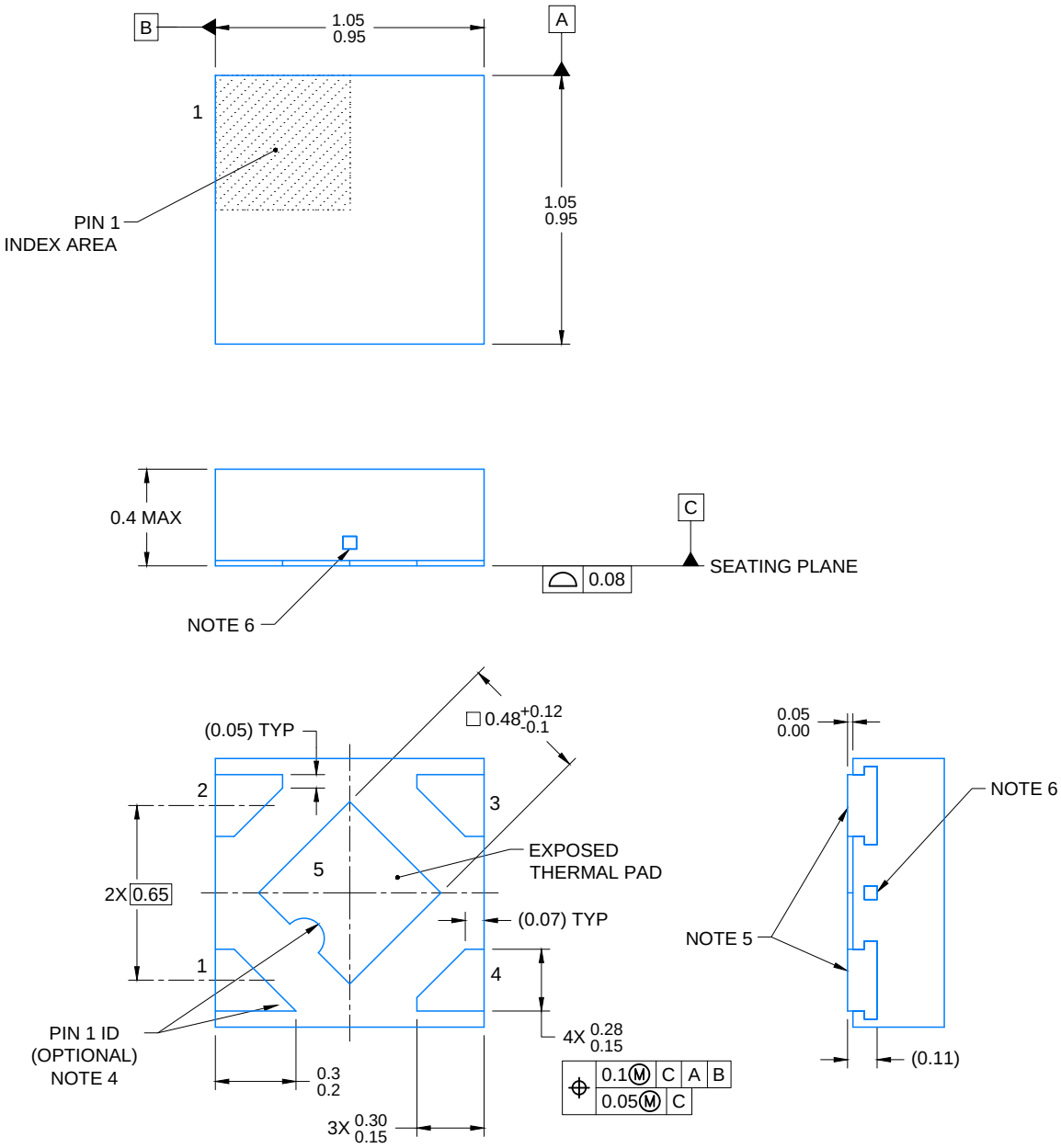
4210367/F

PACKAGE OUTLINE

DQN0004A

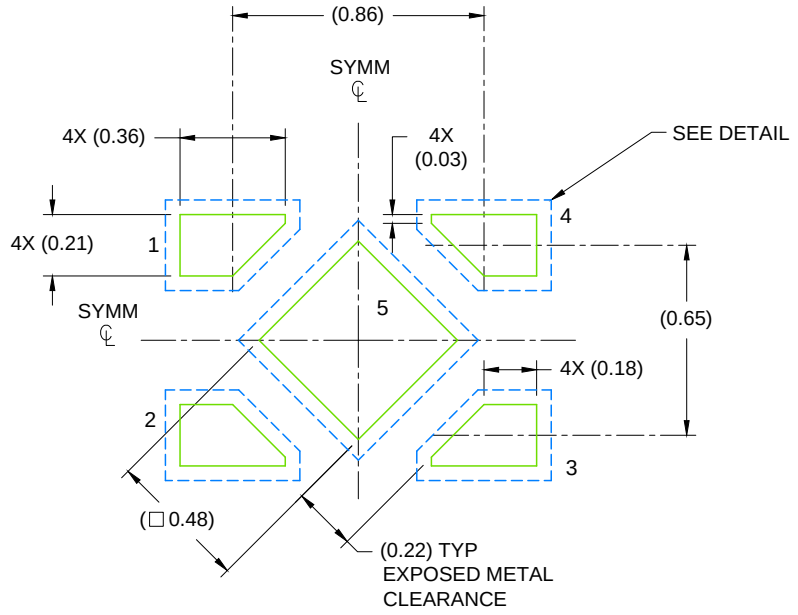
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



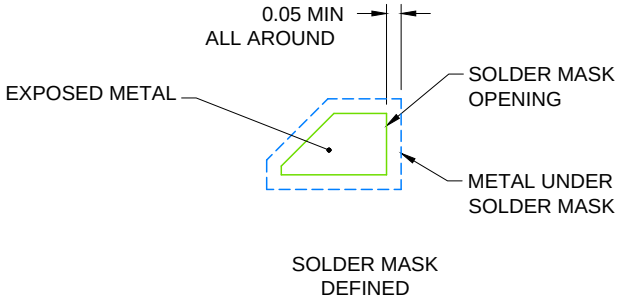
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X

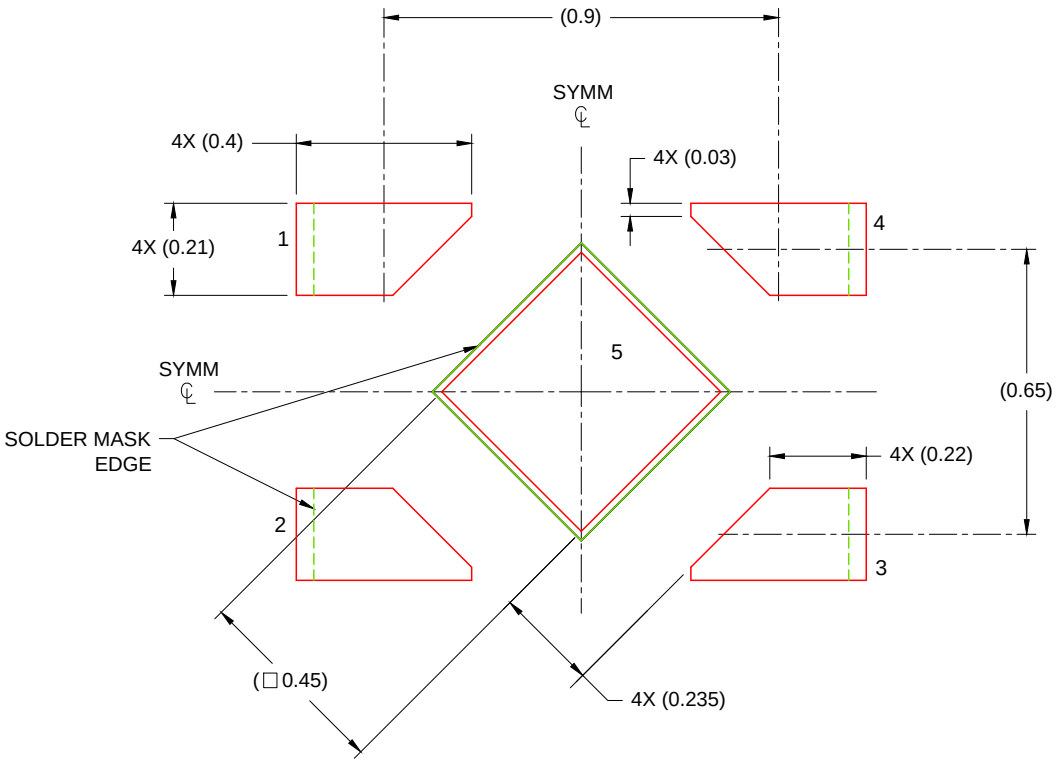


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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