NVIDIA JETSON TX2 USB2.0 TUNING GUIDE

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Application Note

DOCUMENT CHANGE HISTORY

DA-08689-001_v1.0

Version	Date	Description of Change
1.0	August 15, 2017	Initial Release

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

OVERVIEW

This application note describes the registers and steps needed to tune the USB2.0 high speed eye diagram for NVIDIA® Jetson™ TX2. USB-IF provides complete test specification and instructions on their website for high speed host and device mode testing. NVIDIA typically uses Tektronix oscilloscopes for USB characterization. The following test procedures are for Tektronix oscilloscopes.

- Host Mode Testing
  - Procedure for using Tektronix TDS694C: http://www.usb.org/developers/docs/Host_HS_Test.pdf
  - Procedure for using other Tektronix scopes: http://www.usb.org/developers/docs/Host_test_procedure.pdf
- Device Mode Testing
  - Procedure for using Tektronix TDS694C: http://www.usb.org/developers/compliance/Device_HS_Test.pdf
  - Procedure for using other Tektronix scopes: http://www.usb.org/developers/docs/DeviceTestProcedure.pdf

Customers are free to use oscilloscopes from other vendors to do USB characterization.

Note: Jetson TX2 utilizes NVIDIA® Tegra® X2 which is a Parker series SoC.

REQUIRED EQUIPMENT

- Tektronix TDS694C or faster digital sampling oscilloscope
- Tektronix P6247 or P6248 or equivalent differential probe * 1
- High-speed USB Electrical Test Fixture
- Oscilloscope USB test Software
- Tool to access register/memory space in Tegra or build a special image to force USB Test mode enabled

REGISTERS FOR HOST MODE TESTING

Figure 1 shows the relationship between the USB ports and the xUSB controllers.

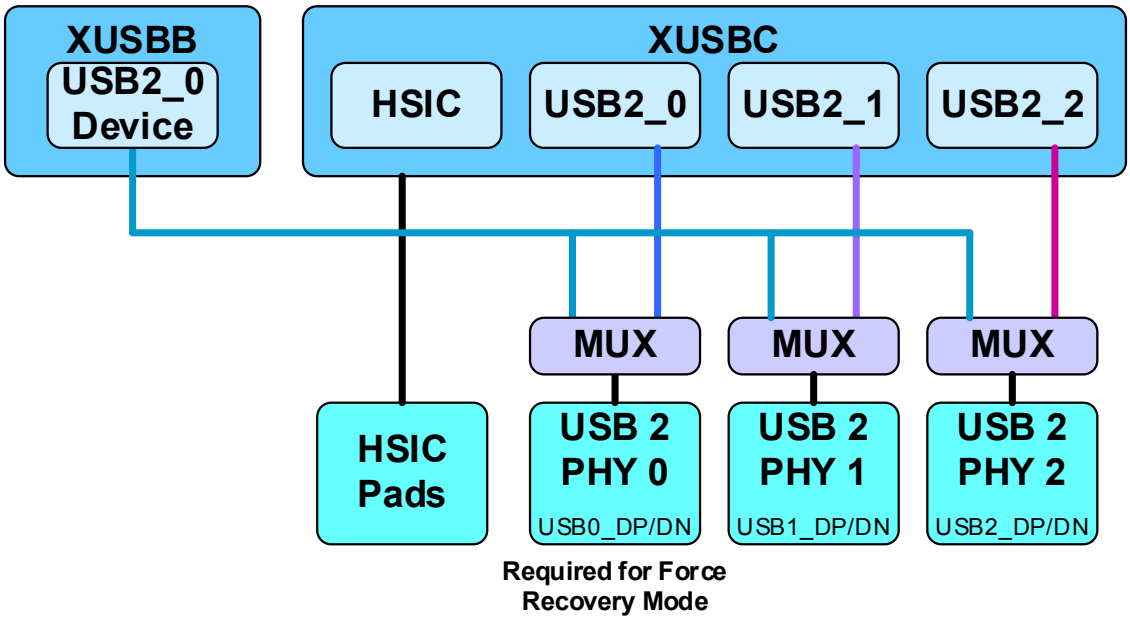

Figure 1. Tegra X2 USB Controllers and Interfaces Routing Map

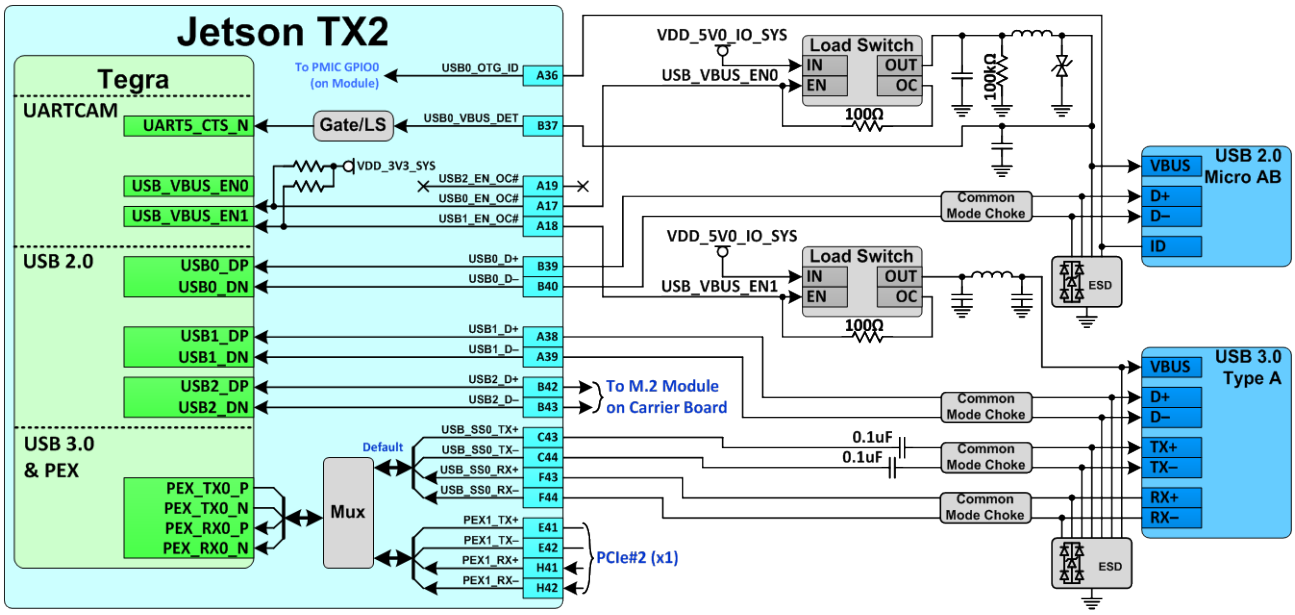

Figure 2. Jetson TX2 Connection Example

Toggle the Jetson TX2 USB registers listed in Table 1 to force Test J, Test K, Test SE0 NAK, and Test Packet on the respective USB port.

Table 1. xUSB USB2.0 Port Test Control Registers

Descriptions	Register Name and Setting
Normal Operations (default)	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] = 0000b
Test J	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] = 0001b
Test K	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] = 0010b
Test SE0 NAK	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] = 0011b
Test Packet	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] = 0100b
Force enable	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] = 0101b

xUSB USB2.0 Port Registers Address:

- USB0: 0x3530454: XUSB_XHCI_OP_PORTPMSCHS_3
- USB1: 0x3530464: XUSB_XHCI_OP_PORTPMSCHS_4
- USB2: 0x3530474: XUSB_XHCI_OP_PORTPMSCHS_5

TEST MODE PROGRAMMING SEQUENCE

The programming sequence for enabling USB2.0 test mode is as follows:

1. Disable the auto-suspend for the controllers:
   a) For example: the following command under Linux Kernel.

   echo on > /sys/bus/usb/devices/usb1/power/control

> **Note:** The "usb1" here is the XHCI USB2 controller; it may map to "usb2" if there is another USB controller on the board. The XHCI bus number can be found under /sys/devices/3530000.xhci/.

2. Set PP (Port Power) in Disabled state by XUSB_XHCI_OP_PORTSC* bit [9] = 0.

   USB0: 0x3530450: XUSB_XHCI_OP_PORTSC_3

   USB1: 0x3530460: XUSB_XHCI_OP_PORTSC_4

   USB2: 0x3530470: XUSB_XHCI_OP_PORTSC_5

3. Set RS (Run/Stop) bit in the XUSB_XHCI_OP_USBCMD_0 bit [0] = 0.

   0x3530020: XUSB_XHCI_OP_USBCMD_0

4. Wait for the HCHalted (HCH) bit in the XUSB_XHCI_OP_USBSTS_0 bit [0] = 1.

   0x3530024: XUSB_XHCI_OP_USBSTS_0

5. Set the xUSB Port Test Control registers in PORTPMSCHS register (see Section "Registers for Host Mode Testing").

6. Disable Pad PD (power down) by clearing the XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0 bit [26] = 0.

   USB0: 0x3520088: XUSB_PADCTL_USB2_OTG_PAD0_CTL_0_0

   USB1: 0x35200c8: XUSB_PADCTL_USB2_OTG_PAD1_CTL_0_0

   USB2: 0x3520108: XUSB_PADCTL_USB2_OTG_PAD2_CTL_0_0

7. Plug in the test fixture to start USB2.0 eye diagram test.

Note: In Steps 2, 5, and 6, USB0 is USB0_D+/D- (B39/B40), USB1 is USB1_D+/D- (A38/A39), and USB2 is USB2_D+/D- (B42/B43).

REGISTERS TO ADJUST HIGH SPEED USB2.0 EYE DIAGRAM

The following are Jetson TX2 USB registers that may be needed to tune the USB2.0 eye diagram. The following "Tuning Procedure" section discusses how to use these registers during characterization.

Table 2. xUSB Registers

Register Name	Bit Fields	Description
XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0: Address 0x03520088 for USB0, 0x035200C8 for USB1, and 0x03520108 for USB2		
HS_SLEW (See Note 1)	8:6	HS slew rate control
HS_CURR_LEVEL (See Note 2)	5:0	HS driver output setup control
XUSB_PADCTL_USB2_OTG_PADx_CTL_1_0: Address 0x0352008C for USB0, 0x035200CC for USB1, and 0x0352010C for USB2		
TERM_RANGE_ADJ	6:3	HS termination control
XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0: Address 0x03520284		
HS_SQUELCH_LEVEL (See Note 3)	2:0	HS SQUELCH control for device RX testing
XUSB_PADCTL_USB2_OTG_PADx_CTL_3_0: Address 0x03520094 for USB0, 0x035200D4 for USB1, 0x03520114 for USB2		
HS_RXEQ	8:6	HS_RXEQ (device RX testing)
HS_TXEQ	3:1	HS_TXEQ (device TX testing)

Notes:

1. HS_SLEW where 0'b000 = slowest and 0'b111 = fastest
2. HS_CURR_LEVEL where 0'b000000 = highest current level and 0'b111111 = lowest current level
3. HS_SQUELCH_LEVEL where 0'b000 = lowest and 0'b111 = highest

The USBx is based on the module pin name, so USB0 is USB0_D+/D- (B39/B40), USB1 is USB1_D+/D- (A38/A39), and USB2 is USB2_D+/D1 (B42/B43).

TUNING PROCEDURE

During manufacturing chip production, each NVIDIA Tegra device is calibrated and the fuses corresponding to USB drive strength (HS_CURR_LEVEL), HS termination (TERM_RANGE_ADJ), and 15K host pull down (RPD_CTRL) are burnt on each chip.

Before making any USB measurements, ensure that the values programmed during manufacturing are loaded for HS_CURR_LEVEL, TERM_RANGE_ADJ and RPD_CTRL values into the pad configuration inputs.

To find out the default drive strength and HS termination value, read from FUSE_USB_CALIB_0 fuse. USB_CALIB bit [5:0] represents the fused HS_CURR_LEVEL value for USB0 port and USB_CALIB bit [10:7] represents the TERM_RANGE_ADJ value for all the ports. USB_CALIB [16:11] is HS_CURR_LEVEL for USB1 port, USB_CALIB [22:17] is HS_CURR_LEVEL for USB2 port. FUSE_USB_CALIB_EXT_0[4:0] represents the RPD_CTRL (host pull-down) for all ports. See Table "FUSE_USB Registers" below for details.

Table 3. FUSE_USB Registers

Register Name	Bit Field	Description
FUSE_USB_CALIB_0 (Address 0x038201F0)		
USB_CALIB	22:17	HS_CURR_LEVEL for USB2
USB_CALIB	16:11	HS_CURR_LEVEL for USB1
USB_CALIB	10:7	TERM_RANGE_ADJ for all USB ports
USB_CALIB	5:0	HS_CURR_LEVEL for USB 0
FUSE_USB_CALIB_EXT_0 (Address 0x03820350)		
USB_CALIB_EXT	4:0	RPD_CTRL for all USB ports

During the characterization stage, manually adjusting the HS_CURR_LEVEL value should be enough to fulfill compliance requirements. It is possible to try and increase termination as a last resort.

Note: NVIDIA does not recommend customers adjusting termination values. Do note that if the TERM_RANGE_ADJ needs to be adjusted, it may result in an impedance mismatch on the board and further attention may be needed.

It must be emphasized that if any HS_CURR_LEVEL modification is needed, it must be done as an offset to the default fused value since each device may have a different HS_CURR_LEVEL default value.

Do not apply a global overwrite HS_CURR_LEVEL value for all silicon. There is a mechanism provided in software to read fused USB drive strength and add an offset to it.

Pre-emphasis (EQ function) can also be tweaked for certain channel designs in addition to tweaking HS_CURR_LEVEL. EQ function can also help with long cable loss. To modify the EQ, write directly to XUSB_PADCTL_USB2_OTG_PADx_CTL_3_0 bits [8:6] for HS_RXEQ and [3:1] for HS_TXEQ.

Table 4. EQ Function

HS_TXEQ[2:0]	AC Gain	HS_RXEQ[2:0]	SQ Level
00	+0 dB (default)	00	-0 dB (default)
01	+1.3 dB	01	-1.2 dB
10	+2.5 dB	10	-2.0 dB
11	+3.5 dB	11	-3.5 dB

Squelch is used to tune the RX sensitivity level - higher DCR loss will require a lower squelch level. To modify the squelch level, write directly to XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0 bits [2:0].

Lastly, the slew rate can be modified by writing directly to XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0 bits [8:6].

HS_CURR_LEVEL OFFSET APPLY PROCEDURE

If the default value does not fit customer design, please adjust the HS_CURR_LEVEL register in order to pass USB HS eye diagram. Follow these steps for tuning:

1. Obtain default value; read reg. "FUSE_USB_CALIB_0"(Address: 0x38201F0) :
   a) USB_CALIB [5:0]: USB pad HS_CURR_LEVEL[5:0] for USB0
   b) USB_CALIB [16:11]: USB pad HS_CURR_LEVEL[5:0] for USB1
   c) USB_CALIB [22:17]: USB pad HS_CURR_LEVEL[5:0] for USB2
2. Calculate offset from fused HS_CURR_LEVEL value and desired value to pass eye mask.
   a) For example, if default value as 0x20, and desired value as 0x1C, where offset = -4
   b) For example, if default value as 0x10, and desired value as 0x14, where offset = +4
3. Adjust HS_CURR_LEVEL register as described in the "Tuning Procedure" section.
   a) Maximum allowable offset: ±6 steps
4. Provide the "tuned offset steps" to software team.

SOFTWARE VERIFICATION

A functional check is recommended. Connect the DUT to USB hosts and devices to perform a check on functionality.

To check if software implements the tuned offset step properly, load new software with offset included into another DUT and check to ensure:

HS_CURR_LEVEL = USB_CALIB + tuned offset steps

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