AN12088

Application hints for TJA1100 Automotive Ethernet PHY

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Document information

Information	Content
Keywords	Automotive Ethernet, 100BASE-T1, PHY, TJA1100
Abstract	The TJA1100 is an 100BASE-T1 Single-port PHY optimized for automotive use cases. The device provides 100 Mbps transmit and receive capability over a single unshielded twisted pair cable, supporting a cable length of at least 15 m. Optimized for automotive use cases like IP camera links, driver assistance systems and back-bone networks, the TJA1100 has been designed for low power consumption and minimum system costs, while still providing the robustness needed in the automotive world. This document describes the application aspects of the TJA1100 in more detail.

Revision history

Rev	Date	Description
1	2017-11-13	• Initial version

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1. Introduction

1.1 Product description

The TJA1100 is an IEEE Std 802.3bw™-2015 (100BASE-T1) [1] compliant Ethernet PHY optimized for automotive use cases. The device provides 100 Mbps transmit and receive capability over a single unshielded twisted pair cable, supporting a cable length of at least 15 m. Optimized for automotive use cases such as IP camera links, driver assistance systems and back-bone networks, the TJA1100 has been designed to minimize power consumption and system costs, while still providing the robustness required for automotive use cases.

1.2 Features

Optimized for automotive use cases

- Transmitter optimized for capacitive coupling to unshielded twisted-pair cable
- Enhanced integrated PAM-3 pulse shaping for low RF emission
- Adaptive receive equalizer optimized for automotive cable length of at least 15 m
- Reduced power consumption through configurable transmitter pulse amplitude adapted to cable length[1]
- Dedicated PHY enable/disable input pin to minimize power consumption
- Low Power Sleep mode with local wake-up support
- Robust remote wake-up via Ethernet
- Gap-free supply under-voltage detection with fail-silent behavior
- EMC optimized output driver strength for Media Independent Interface (MII) and Reduced MII (RMII)
- Diagnosis of cabling errors (shorts and opens)
- Small HVQFN-36 package for PCB space-constrained applications
- MDI pins protected against ESD ±6 kV HBM and ±6 kV IEC61000-4-2
- MDI pins protected against transients in automotive environment
- Automotive-grade temperature range -40 …+125 °C
- Automotive product qualification in accordance with AEC-Q100

Miscellaneous

- MII as well as RMII standard compliant interface
- Reverse MII mode for back-to-back connection of two PHYs
- 3V3 single supply operation with on-chip 1.8 V LDO regulators
- On-chip termination resistors for balanced UTP cable
- Jumbo frame support up to 16 kB

[1] Conformance test, interoperability test and EMC test are done with 1V default amplitude

- Internal, external and remote loopback mode for diagnosis
- LED control output for link diagnosis

1.3 Pinning

The pinning diagram is shown in Fig 1. In general, it consists of power supply interface, the MII/RMII, the SMI, the MDI related pins TRX_P/TRX_M and the oscillator input pins. As 100BASE-T1 provides a full-duplex bi-directional communication, the standard MII signals COL and CRS are not needed.

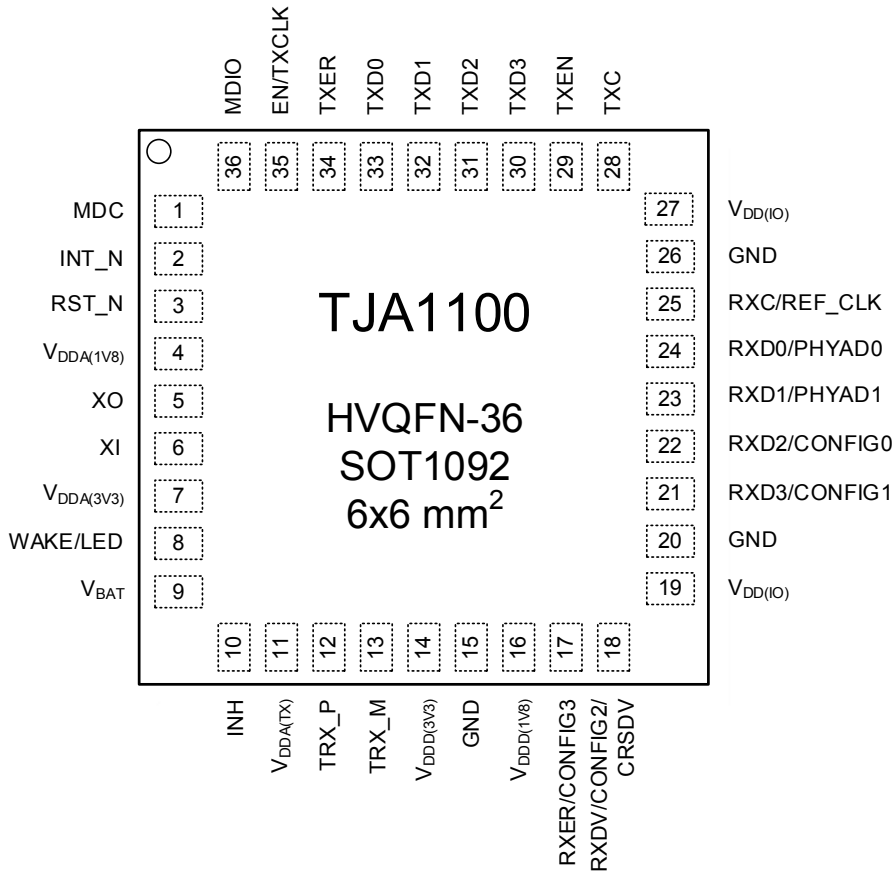


Fig 1. Pinning diagram

Table 1. TJA1100 pinning and signal

Symbol	Pin	I/O	Description
MDC	1	I	Serial Management Interface clock input (very weak pull-down)
INT_N	2	O	Interrupt output (active Low, open-drain output) Can be left open if not used
RST_N	3	I	Reset input (active Low, weak pull-up)
$V_{DDA(1V8)}$	4	P	1.8 V supply voltage for analog (internally generated supply voltage)
XO	5	AO	Crystal feedback This pin is used in MII/RMII mode when a 25 MHz crystal is utilized. Can be left open if not used
XI	6	AI	Crystal input This pin is used in MII/RMII mode when a 25 MHz crystal is utilized. Should be shorted to GND to avoid noise input if not used
$V_{DDA(3V3)}$	7	P	3.3 V analog supply voltage
LED	8	AO	LED open-drain output (when enabled by configuration)
WAKE	8	AI	Local wakeup input (when LED output disabled) Shall be left open or shorted to GND via a series resistor and configured as WAKE input if not used
VBAT	9	P	Battery supply voltage
INH	10	AO	Inhibit output for voltage regulator control (VBAT related, active High) Can be left open if not used
$V_{DDA(TX)}$	11	P	3.3 V supply voltage for transmitter
TRX_P	12	AIO	Plus terminal of transmit/receive signal
TRX_M	13	AIO	Minus terminal of transmit/receive signal
$V_{DDD(3V3)}$	14	P	3.3 V digital supply voltage
GND	15	G	Reference ground
$V_{DDD(1V8)}$	16	P	1.8 V supply voltage for digital (internally generated supply voltage)
RXER	17	O	MII/RMII: Receive Error output Can be left open if not used
CONFIG3	17	I	Pin strapping configuration input 3
RXDV	18	O	MII Mode: Receive Data Valid output
CONFIG2	18	I	Pin strapping configuration input 2
CRSDV	18	O	RMII Mode: Carrier Sense/Receive Data Valid output
$V_{DD(IO)}$	19	P	3.3 V digital I/O supply voltage
GND	20	G	Reference ground
RXD3	21	O	MII Mode: Receive Data output, bit 3 of RXD[3:0] nibble Can be left open in RMII Mode

Symbol	Pin	I/O	Description
CONFIG1	21	I	Pin strapping configuration input 1
RXD2	22	O	MII Mode: Receive Data output, bit 2 of RXD[3:0] nibble Can be left open in RMII Mode
CONFIG0	22	I	Pin strapping configuration input 0
RXD1	23	O	MII Mode: Receive Data output, bit 1 of RXD[3:0] nibble RMII Mode: Receive Data output, bit 1 of RXD[1:0] nibble
PHYAD1	23	I	Pin strapping configuration input for bit 1 of the PHY address used for the SMI address/Cipher scrambler
RXD0	24	O	MII Mode: Receive Data output, bit 0 of RXD[3:0] nibble RMII Mode: Receive Data output, bit 0 of RXD[1:0] nibble
PHYAD0	24	I	Pin strapping configuration input for bit 0 of the PHY address used for the SMI address/Cipher scrambler
RXC	25	O	MII mode: 25 MHz Receive Clock output
		I	Reverse MII mode: 25 MHz Receive Clock input
REF_CLK	25	O	RMII mode: interface reference clock output (in case of 25 MHz crystal at PHY)
		I	RMII mode: interface reference clock input (in case of 50 MHz external oscillator)
GND	26	G	Reference ground
$V_{DD(IO)}$	27	P	3.3 V digital I/O supply voltage
TXC	28	O	MII Mode: 25 MHz Transmit Clock output Can be left open in RMII Mode
		I	MII Reverse Mode: 25 MHz Transmit Clock input Can be left open in RMII Mode
TXEN	29	I	MII/RMII: Transmit Enable input (active High, weak pull-down)
TXD3	30	I	MII Mode: Transmit Data input, bit 3 of TXD[3:0] nibble (weak pull-down) Can be left open in RMII Mode
TXD2	31	I	MII Mode: Transmit Data input, bit 2 of TXD[3:0] nibble (weak pull-down) Can be left open in RMII Mode
TXD1	32	I	MII Mode: Transmit Data input, bit 1 of TXD[3:0] nibble RMII Mode: Transmit Data input, bit 1 of TXD[1:0] nibble (weak pull-down)
TXD0	33	I	MII Mode: Transmit Data input, bit 0 of TXD[3:0] nibble RMII Mode: Transmit Data input, bit 0 of TXD[1:0] nibble (weak pull-down)
TXER	34	I	MII/RMII: Transmit Error input (weak pull-down) Shall be shorted to GND if not used
EN	35	I	PHY enable input (active High, weak pull-down))
TXCLK	35	O	transmit clock output in test mode and during slave jitter test
MDIO	36	IO	Serial Management Interface data I/O (weak pull-up)

AIO : Analog Input/Output
AO : Analog Output
AI : Analog Input
I : Digital Input (VDDIO related)
O : Digital Output (VDDIO related)
IO : Digital Input/output
P : Power supply
G : Ground

1.4 Block diagram

The block diagram of the TJA1100 is shown in Fig 2. The blocks in green color are the functional blocks covered by the 100BASE-T1 specification, consisting of the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) both for the transmit and receive signal path. The MII/RMII interface (including the Serial Management Interface (SMI)) conforms to IEEE802.3 clause 22. Additional blocks are defined for mode control, register configuration, interrupt control, system configuration, reset control, LED control and local wake-up. Configuration Control allows for some hardware configuration during power-on (e.g. master or slave configuration). Functional blocks related to the power supply of the device (blue) include the internal 1.8 V regulator for the digital core, the VLP supply in Sleep mode, the Reset circuit and the supply monitoring.

The clock signals needed for the operation of the PHY are generated in the PLL block, derived from an external crystal or an oscillator input signal.

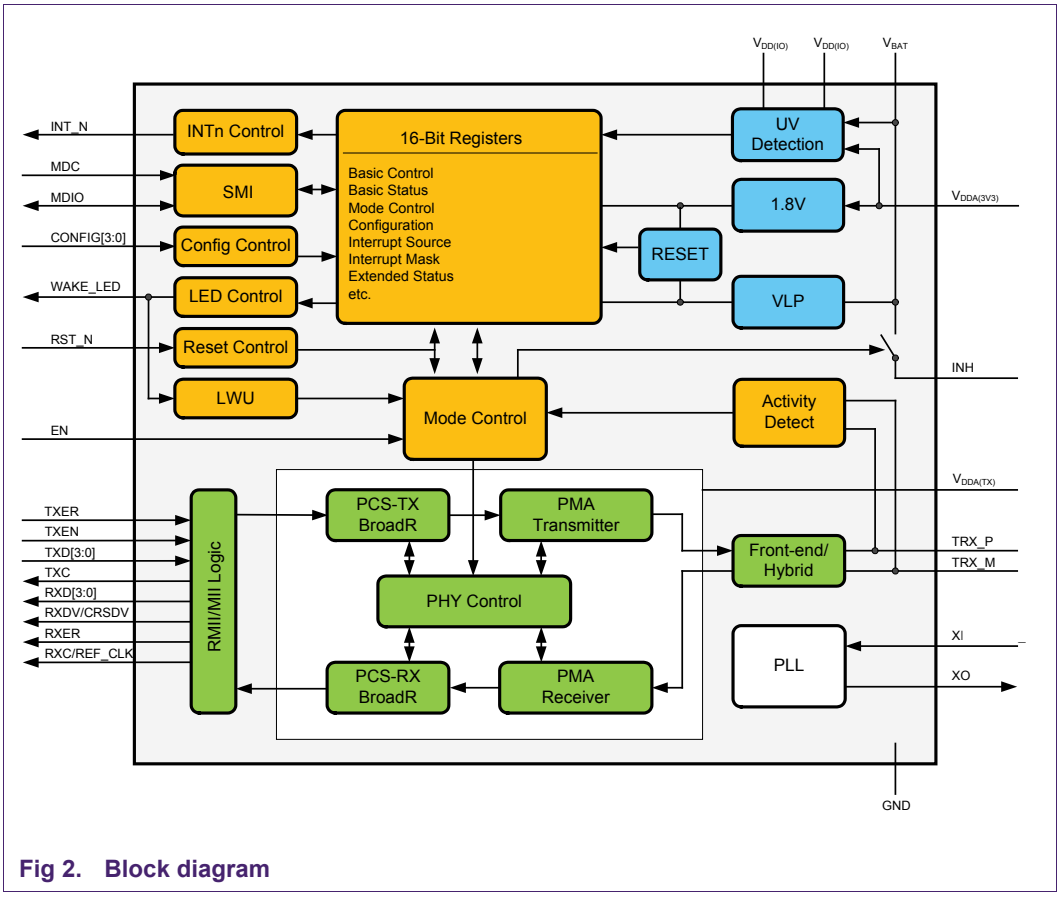


Fig 2. Block diagram

2. 100BASE-T1 Basics

2.1 System diagram

As an 100BASE-T1 compliant Ethernet PHY, the TJA1100 provides 100 Mbit/s transmit and receive capability over a single unshielded twisted pair cable, supporting a cable length of at least 15 m with a Bit Error Rate (BER) less than or equal to 1E-10. It is optimized for capacitive signal coupling to the twisted pair lines. To comply with automotive EMC requirements [2], [3], common mode chokes, ESD elements and low pass filters as well as a common mode termination network is inserted between Ethernet PHY and connector. The connection to the Media Access Control (MAC) unit is realized either by the standard MII or the RMII.

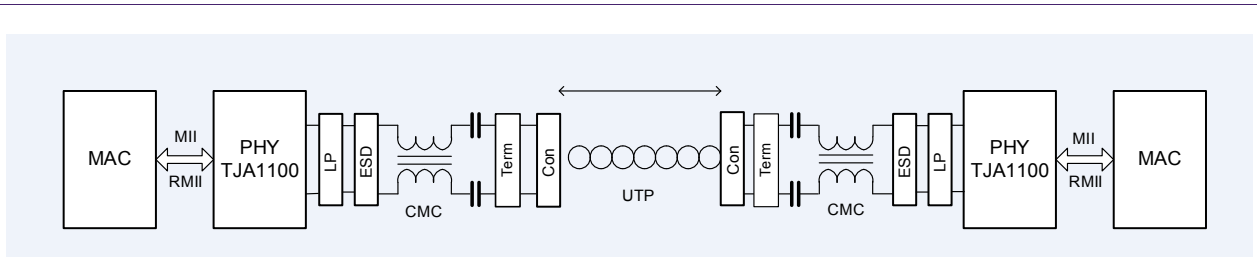


Fig 3. System diagram

2.2 Link startup

The link startup is governed by the PHY Control state machine in the 100BASE-T1 and is shown in Fig 4.

The LINK_CONTROL bit must be set before a link will be established. This holds for both the Master and Slave PHY. Once this bit is set, the Master PHY initiates the training phase by sending Idle (tx_mode=SEND_I). As soon as the receiver of the Slave PHY has been synchronized to the Idle sequence, it also enters the training state and starts sending Idle. Upon expiration of the minwait_timer the Slave PHY switches to Send_Idle state. Now the Master PHY receives an Idle sequence from the Slave PHY. As soon as the receiver of the Master PHY has been synchronized (loc_rcvr_status=OK & rem_rcvr_status=OK), it enters the Send Idle or Data state. Once the Slave PHY detects that the receiver status of the Master PHY is OK (rem_rcvr_status=OK), it finally enters the Send Idle or Data state too. From that point onwards the bi-directional link is established and normal data communication is possible.

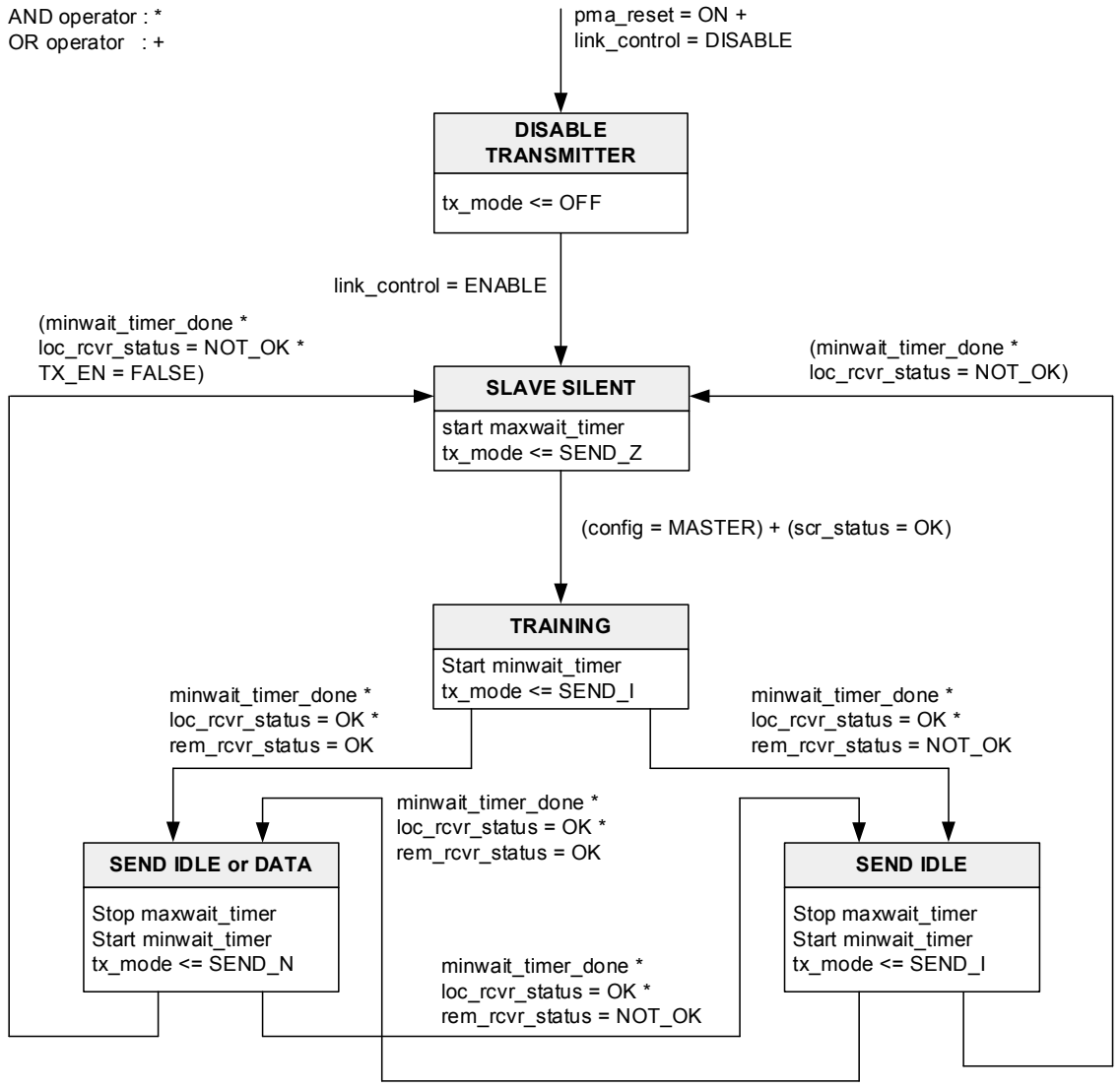


Fig 4. PHY Control state machine from IEEE Std 802.3bw™-2015 specification [1]

3. Hardware application

3.1 Overview

A typical application circuit for the TJA1100 can be seen in Fig 5. The shown use case assumes a capacitive coupling to the twisted-pair wires. To comply with EMC requirements a common mode choke should be inserted into the signal path. It is recommended to place the DC blocking capacitors between common mode choke and connector. Further supply filter recommendations can be found in section 3.5.

While the differential signal termination is integrated into the PHY, it is recommended to apply a common mode termination to the twisted-pair lines to avoid a floating behavior on the cable.

In case battery-enabled wake-up functionality is not required, a typical application circuit may look like in Fig 6. Here the V_{BAT} pin can be supplied from 3.3 V and the INH pin can be left open. Small buffer capacitors which are commonly applied to supply pins are not explicitly shown here. More detailed application information will be given in the following chapters.

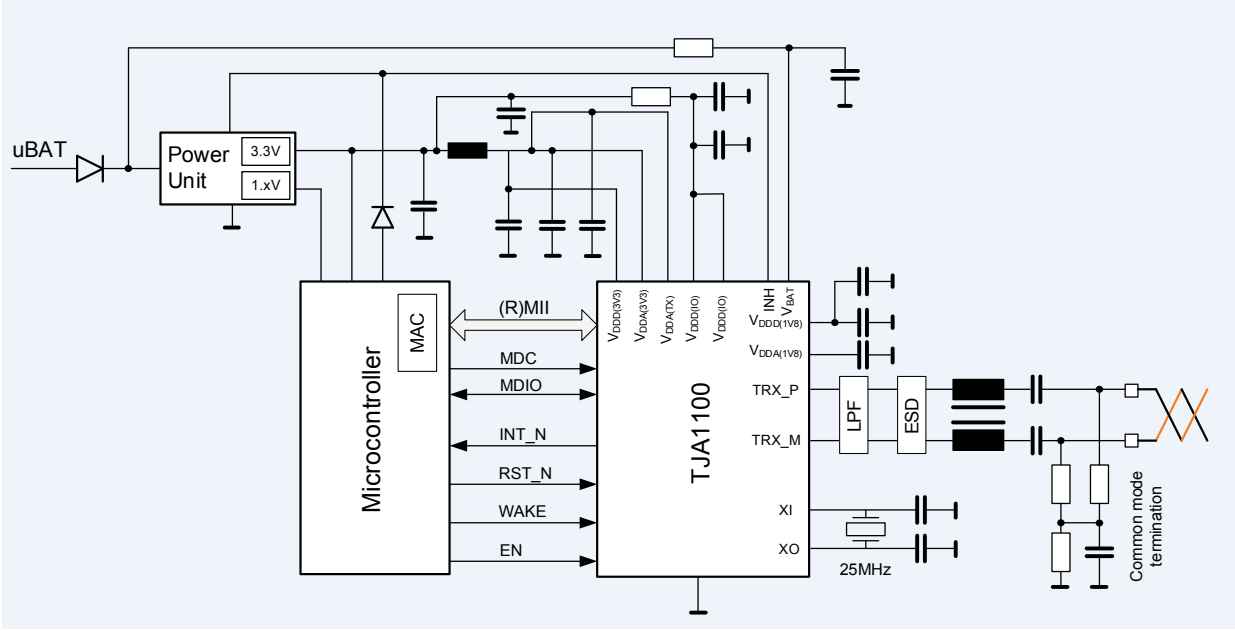


Fig 5. Typical application circuit for the TJA1100 with sleep support

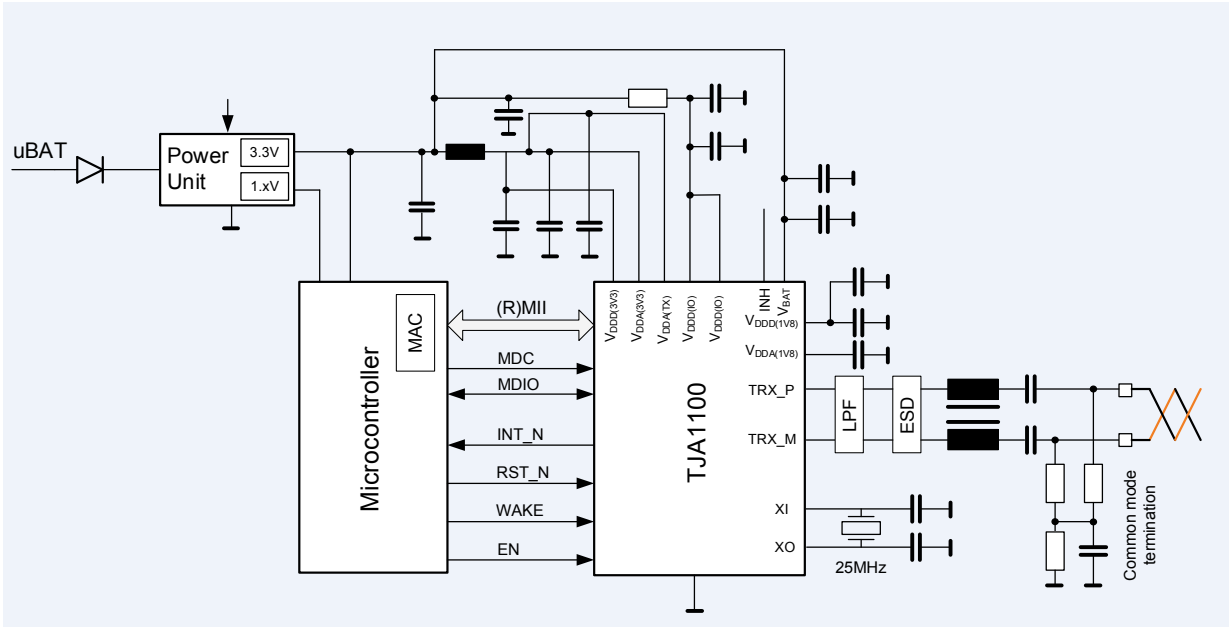


Fig 6. Typical application circuit for the TJA1100 without sleep support

3.2 MII/RMII interface

Fig 7 shows the MII interface between PHY and MAC in more detail. Transmit and receive data is exchanged via 4-bit wide data nibbles TXD[3:0] and RXD[3:0], which are conveyed synchronously to the transmit and receive clock TXC and RXC, respectively. Both clock signals are provided by the PHY and are typically derived from an external crystal running at nominal 25 MHz (±100 ppm). Normal data transmission is initiated with a High level at TXEN, while a High level at RXDV indicates normal data reception.

Figure 8 shows the RMII interface between PHY and MAC in more detail. Transmit and receive data is exchanged via 2-bit wide data nibbles TXD[1:0] and RXD[1:0]. To achieve the same data rate the interface is clocked with nominal 50 MHz. There is only one clock signal REF_CLK provided by the PHY both for the transmit and receive data. This clock signal is typically derived from an external 25 MHz crystal (±100 ppm) as shown in Fig 8. For this use case it is recommended to double check the RMII requirements of the MAC controller device as far as it concerns the clock requirements.

As before normal data transmission is initiated with a High level at TXEN, while a High level at CRSDV indicates normal data reception.

The trace length between PHY and MAC shall be kept short to ensure a capacitive load at the fast switching pins (input capacitance of MAC plus PCB trace) of less than 15 pF. The PCB trace impedance should be at least 50 Ω with a line delay of less than 1 ns. To allow for further EMC fine tuning, additional series resistors of around 20 Ω can be considered.

In case the capacitive load can be kept below 15 pF and the connection between PHY and MAC is short, the MII and RMII output driver slew rate may be reduced for improved

EME behavior by setting the MII_DRIVER configuration bit to ‘1’. It is expected to check the timing for this setting with the available IBIS model or in measurements.

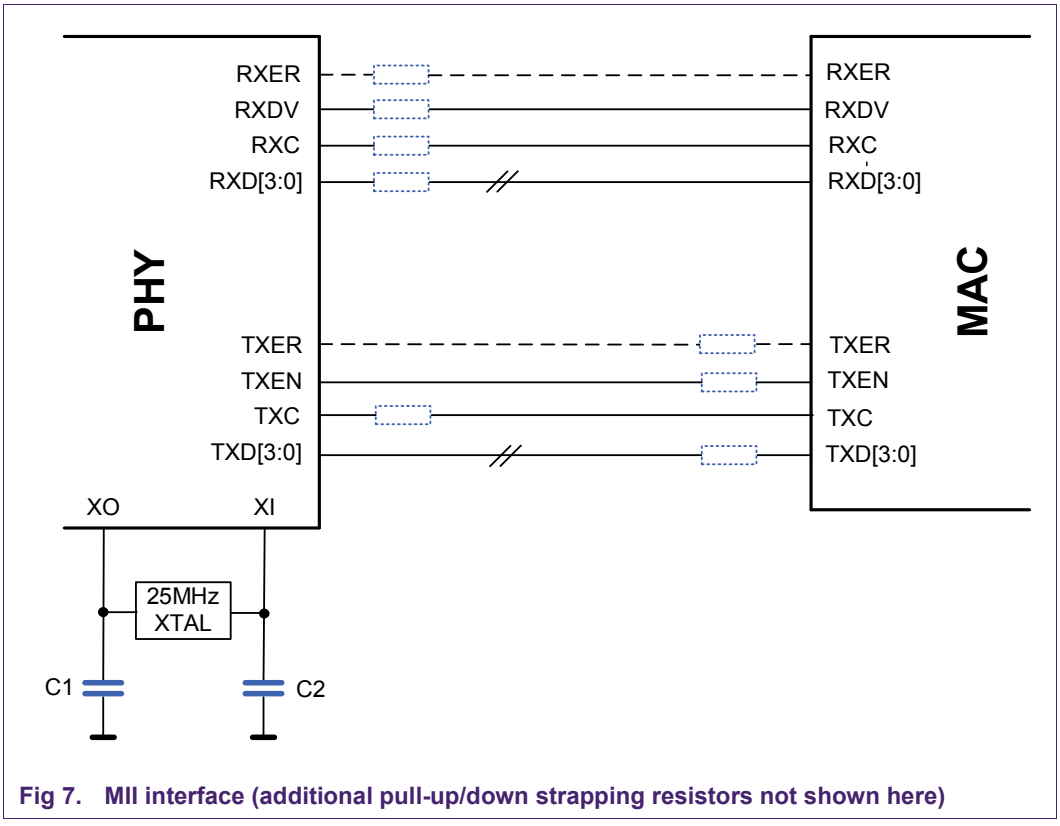


Fig 7. MII interface (additional pull-up/down strapping resistors not shown here)

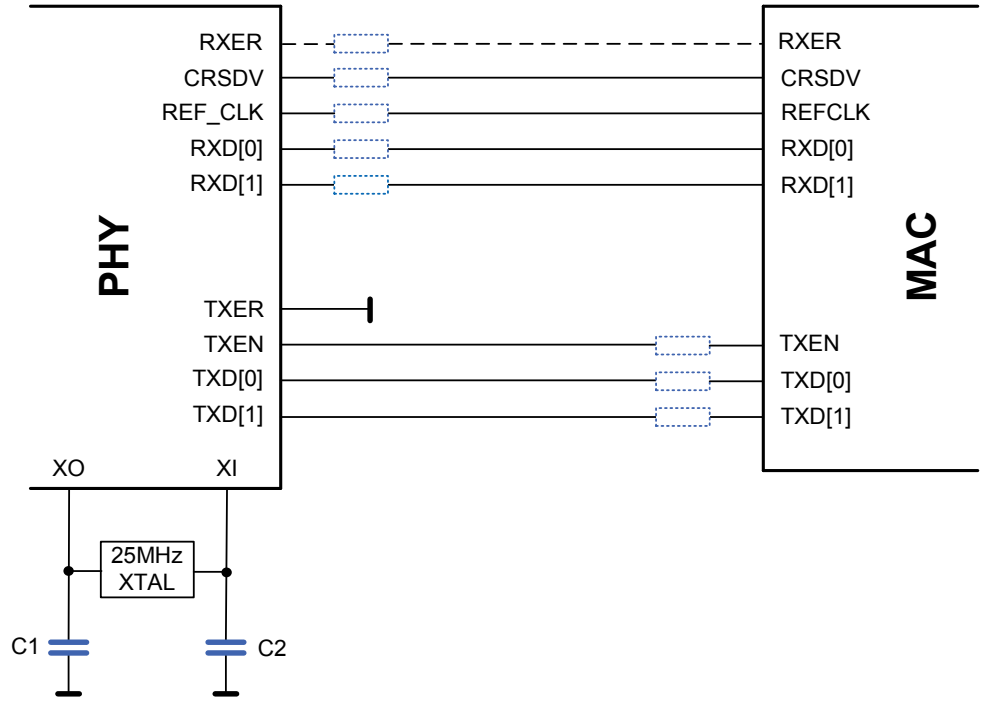


Fig 8. RMII interface (additional pull-up/down strapping resistors not shown here)

Fig 9 shows the RMII in case a 50 MHz external oscillator is used to provide the clock signal to the PHY and MAC. Note the frequency tolerance of the external oscillator must be within ±50 ppm. The pin XI shall be connected to ground and the pin XO shall be left open in this case.

The ±50 ppm frequency tolerance of external 50 MHz clock input is necessary since it will be used as the recovered clock in the TJA1100, and there will be a ppm difference between the 50 MHz REF_CLK received from the MAC and the recovered clock.

Other pins such as TXC and TXD[2], TXD[3], RXD[2] and RXD[3] are left open for RMII configuration.

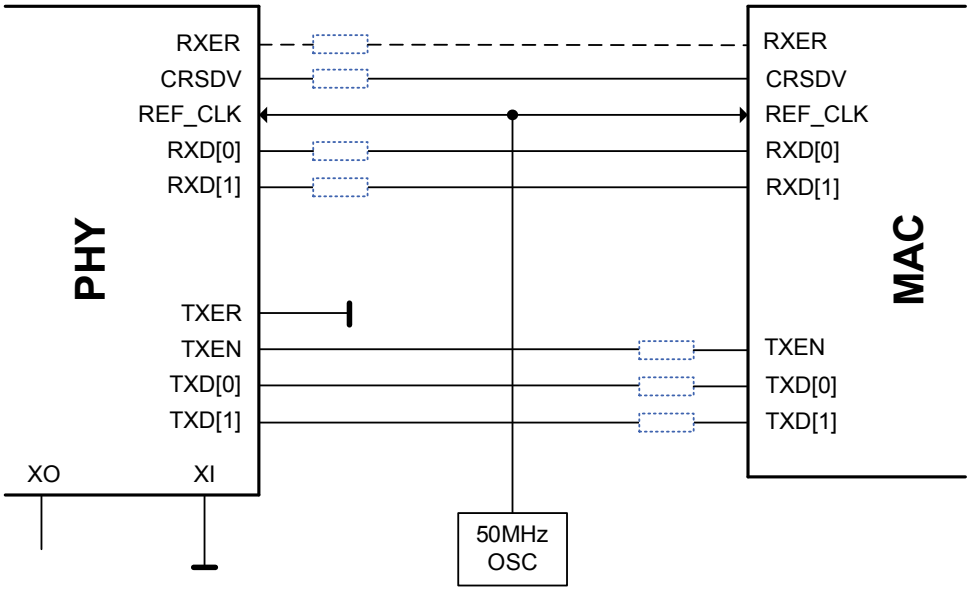


Fig 9. RMII interface with external clock

3.3 SMI interface

The SMI (Serial Management Interface) is a series bus defined in IEEE802.3 clause 22 standards, providing access to the various control and status registers for management and service purpose.

3.3.1 Functionality of the SMI pins

The SMI interface is implemented by two signals:

- MDC (Management Data Clock): Driven by the MAC to the PHY. The MDC can be clocked up to 2.5 MHz corresponding to a minimum clock period of 400 ns.
- MDIO (Management Data Input/Output): Bidirectional, driven by the MAC to the PHY during a write transaction. For a read transaction, the PHY takes over the MDIO line during the turnaround bit times, supplies the MAC with the register data requested, then releases the MDIO line.

To allow for further EMC fine tuning an additional series resistor of around 50 Ω can be considered for the MDC signal line. The MDIO requires a specific pull-up resistor (about 10 kΩ) to $V_{DD(IO)}$. The pull-up can be also within the MAC. Make sure the 10 kΩ pull-up resistor is available only once at the same MDIO bus.

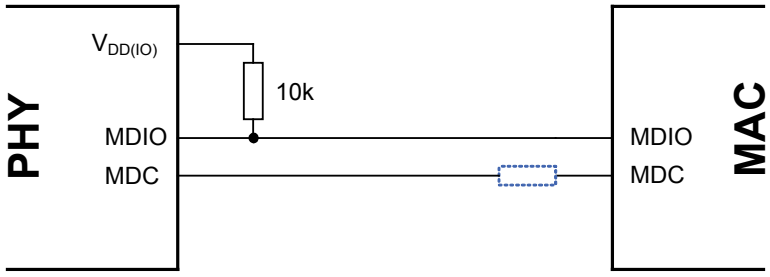


Fig 10. SMI diagram

3.3.2 SMI frame structure & bus timing

The SMI interface supports a single MAC as the master, and can have up to 32 PHY slaves. Frames transmitted on the SMI interface shall have the frame structure shown in Table 2. The order of bit transmission shall be from left to right.

Table 2. SMI frame format

	SMI frame fields							
	Preamble	Start of frame	Operation code	PHY address	Register address	Turn around	Data	Idle
Read	1…1	01	10	AAAAA	RRRRR	Z0	D…D	Z
Write	1…1	01	01	AAAAA	RRRRR	10	D…D	Z

Preamble: At the beginning of each transaction, the MAC shall send a sequence of 32 contiguous logic “1” bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can use to establish synchronization.

Start of frame: The start of frame is indicated by a <01> pattern.

Operation code: For a read transaction is <10>, while for a write operation is <01>.

PHY address: The PHY address is 5 bits. The 1st PHY address bit transmitted and received is the MSB of the address. Please refer to bits PHYAD[4:0] in Configuration register 2 for the TJA1100 PHY address.

Register address: The Register address is 5 bits. The 1st register address bit transmitted and received is the MSB of the address.

Turnaround: The turnaround time is a 2 bit time spacing between Register address and data field.

Data: The data field is 16 bits.

Idle: The idle condition on MDIO is a high-impedance state. The pull-up resistor pulls the MDIO line to a logic “1”.

Fig 11 shows the example of SMI write/read transaction. Bit sampling is performed on the rising edge of the clock MDC.

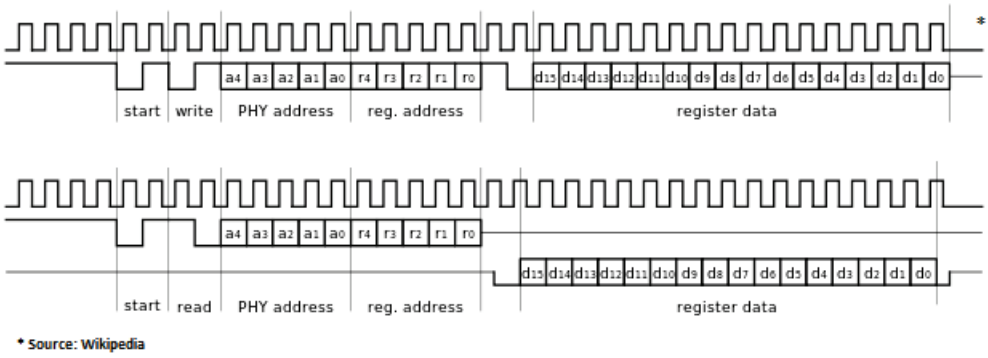


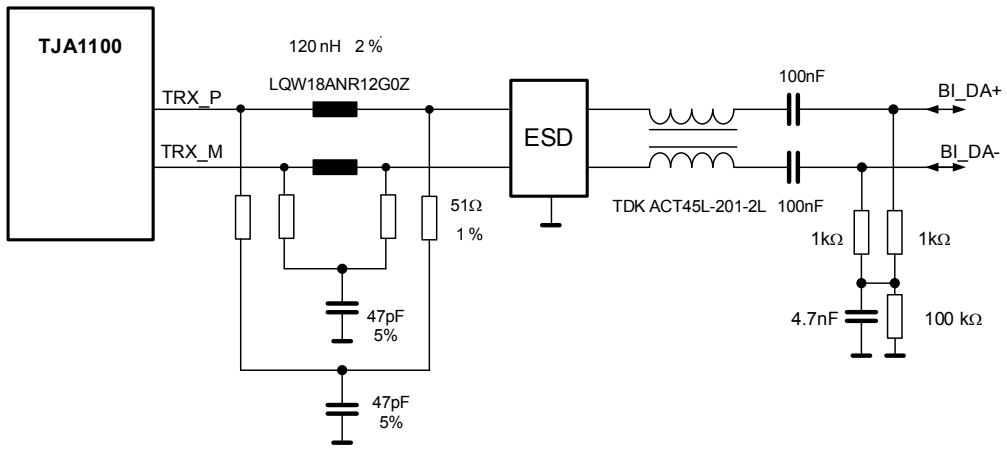
Fig 11. Example of SMI write/read timing

3.4 MDI interface

The MDI interface connects the PHY to the twisted pair cable and consists of the following mandatory elements (from left to right) shown in Fig 12:

- Low-pass filter
- ESD protection diode
- Common mode choke
- Capacitive coupling
- Common mode termination (optional, requested by some OEMs)
- Head/Plug of connector

Below, the elements and their requirements are discussed in more detail. While the capacitive coupling and common mode termination can be viewed as PHY independent, the choice of common mode choke and low-pass filter design are typically PHY specific. The below statements therefore apply to the TJA1100 only. As the MDI interface acts as termination for the transmission line of the balanced 100 Ω cable, any deviation from the nominal 100 Ω at the MDI interface will give rise to reflection of some portion of the incoming signal. The amount of reflected signal is measured by the Return Loss parameter (over frequency) and must be kept within the limits specified in the 100BASE-T1 document.



(1) = $R_{S(max)}$ = maximum series resistance; f_{SR} = self-resonant frequency

Fig 12. MDI application diagram

3.4.1 Common mode choke

The common mode choke provides common mode rejection needed to handle typical common mode noise in an automotive environment. While it helps to get rid of common mode noise over a broad frequency range, the choke may appear to be a major source of differential noise due to common to differential mode conversion. Therefore, only high quality symmetrical chokes shall be used. The most important requirements for chokes have been defined in [2] and are repeated in Table 3.

Table 3. Performance requirements for common mode chokes

S-Parameter	Value	Description
Sdd-21	>-0.5 dB @ 1 MHz >-0.5 dB @ 10 MHz >-0.7 dB @ 33 MHz >-1.0 dB @ 66 MHz	Differential mode attenuation (IL)
Scc-21	<-25 dB @ 1 MHz <-45 dB @ 10 MHz <-45 dB @ 80 MHz <-23 dB @ 1000 MHz	Common mode rejection
Sds-21/Sds-12 Ssd-21/Ssd-12	<-70 dB @ 1 MHz <-70 dB @ 10 MHz <-50 dB @ 100 MHz <-34 dB @ 300 MHz <-24 dB @ 1000 MHz	Differential to common mode rejection Common to differential mode rejection
Sdd-11 Sdd-22	<-27 dB @ 1 MHz <-27 dB @ 10 MHz <-19 dB @ 66 MHz	Return Loss

3.4.2 AC coupling

In Fig 12 AC coupling is realized by using 100 nF DC blocking capacitors forming a high-pass filter together with the termination of 50 Ω for each line. The tolerance of the capacitors shall be within ±10 % with max rating ≥ 50 V.

3.4.3 Low-pass filter

Next to the internal pulse shaping, it is recommended to use an external low-pass filter as shown in Fig 12. For symmetry reasons the tolerance of the components should be within ±1 % for the resistors, ±2 % for the coils and ±5 % for the capacitors. As mainly the matching between the bus lines is relevant, the absolute value for the resistor is more relaxed (it can be between 49 Ω and 51 Ω with 1 % accuracy).

3.4.4 ESD protection

The TJA1100 already provides a high level of ESD robustness (see [1]). Nevertheless, the PESD2ETH-X or -AX diode is mandatory for higher robustness also in case of independent power supplies of the link partners (e.g. mains adapters) or a short of the bus lines to voltages higher 5 V. The supply terminal of the diode shall be connected to a 3.3 V supply rail, which is sufficiently buffered. The layout for the diode should be symmetrically, Fig 13 shows a possible routing.

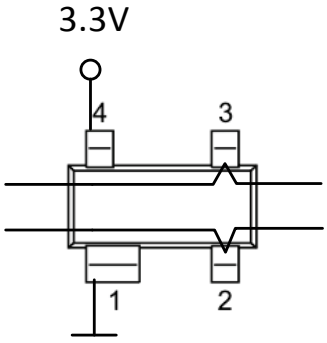


Fig 13. Recommended ESD diode trace routing

3.4.5 Common mode termination

To provide some common mode termination of the channel, a split termination consisting of two resistors and a capacitor can be optionally connected to the signal lines between the DC blocking capacitors and the connector. For symmetry reasons the tolerance of the two resistors shall be within ±1 %. The power rating of the resistors should be higher than 0.4 W, depending on expected RF power in the actual application. Please check with the end customer (OEM) on the details of the implementation and their requirements.

3.4.6 Differential signal layout

The differential signal pair TRX_P/TRX_M shall be routed close together with a controlled impedance of 100 Ω. Since the symmetry is most critical for the EMC performance, keep both traces of the differential pair as identical as possible. To increase the effectiveness of the choke or transformer for higher frequencies and to

minimize parasitic capacitances, consider also a cut-out of the ground plane beneath the differential signal path from the PHY to the connector. The choke shall be placed close to the PHY.

The insertion loss for the path from the PHY to the connector shall be smaller than 2 dB for all frequencies from 1 MHz to 66 MHz. The return loss limit is given in the 100BASE-T1 specification.

It should be noted that the symmetry requirement for MDI mode conversion must stay within the limits as defined in the 100BASE-T1.

Please note that all the min., typ. and max. values of the integrated termination resistor $R_{term(TRX\_P)}$ and $R_{term(TRX\_M)}$ should be used in the PCB simulation.

3.4.7 Communication channel

The used channel needs to fulfill the channel requirements as described in [1]. Furthermore, it is recommended to use a channel with a total cable propagation delay of lower than 85 ns to ensure echo will be fully cancelled.

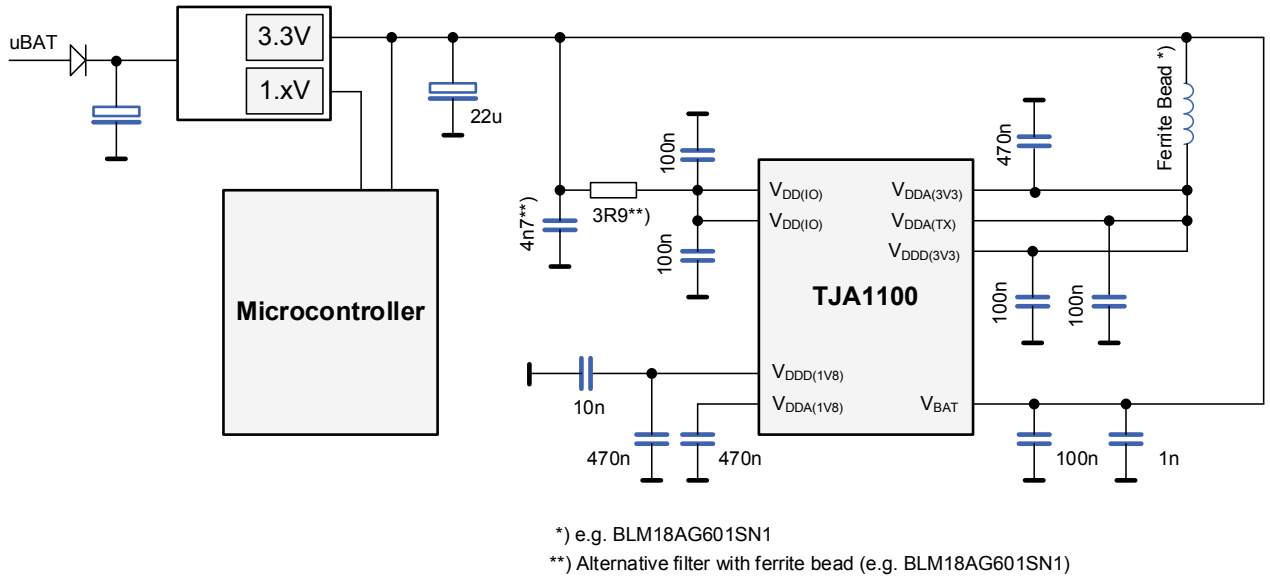
3.5 Supply

The supply schematic is shown in Fig 14. As can be seen in Fig 14 two landing places for buffering capacitors are recommended for $V_{DDA(3V3)}$ and $V_{DDD(1V8)}$ pins. As usual the buffer capacitors shall be placed as close as possible to the pins. The PCB should provide the possibility to apply ferrite beads to $V_{DDA(TX)}$,$V_{DDA(3V3)}$ and $V_{DDD(3V3)}$. For $V_{DDA(IO)}$ a landing spot for an R-C filter or a ferrite bead is recommended. For first investigations, they can be equipped with 0 Ω resistors. To what extend these ferrite beads are really needed depends on the EMC results. The shown electrolytic capacitor of 22 µF at the voltage regulator output reflects the buffering needs of the PHY only. A higher value may be needed when also considering the buffering needs of the microcontroller or any other components that are supplied through this voltage rail.

The additional 10 nF at $V_{DDD(1V8)}$ and 1nF at V_{BAT} are not necessarily needed but would further improve the emission on those supply lines.

As shown in Fig 15, V_{BAT} can also be supplied by the battery directly. It's recommended to place a series resistor of e.g. 1 kΩ into the battery supply line of the PHY for enhanced protection against automotive transients. In addition, a capacitor of e.g. 100 nF, closely connected to V_{BAT} and forming a low-pass filter in conjunction with the series resistor, can be used for enhanced transient protection.

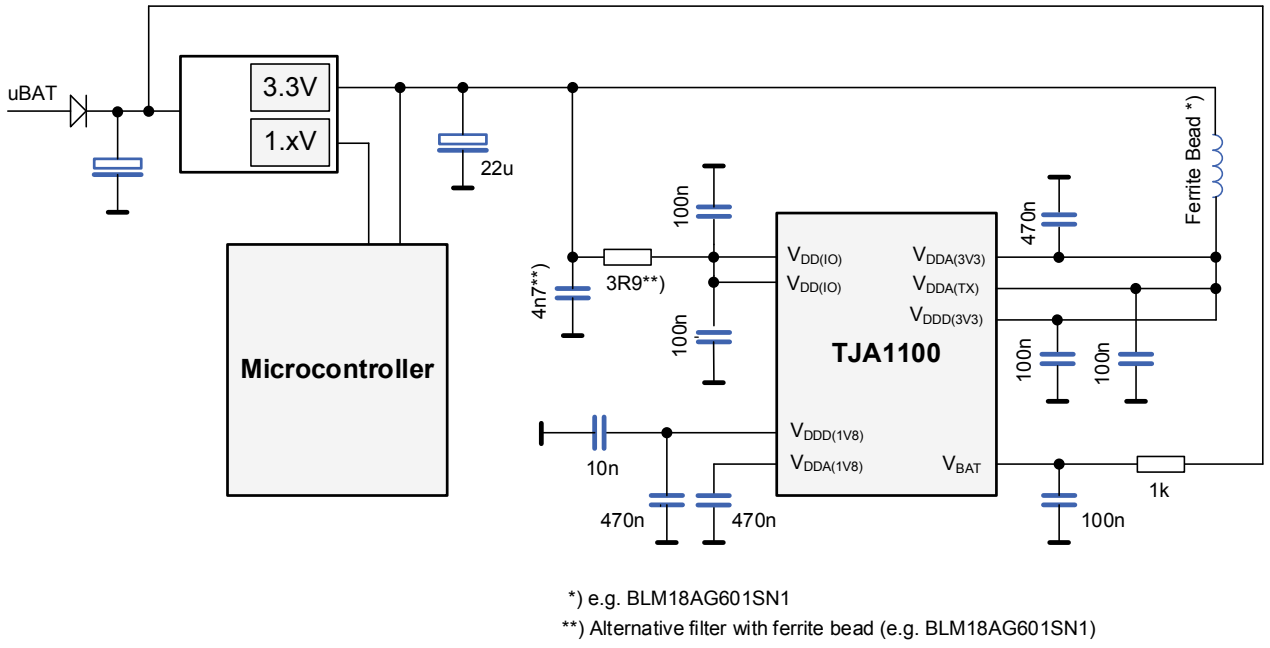
Note that the maximum allowed slew rate on BAT supply should be limited below 10 V/µs for rising edge and 1 V/µs for falling edge above 2 Vpp amplitude.



*) e.g. BLM18AG601SN1

**) Alternative filter with ferrite bead (e.g. BLM18AG601SN1)

Fig 14. Supply schematic (V_{BAT} pin supplied out of 3.3 V regulator)



*) e.g. BLM18AG601SN1

**) Alternative filter with ferrite bead (e.g. BLM18AG601SN1)

Fig 15. Supply schematic (V_{BAT} pin supplied out of the battery)

The filtering in the supply is mainly intended for blocking emission from the IC. Nevertheless, it will also filter disturbance from supply towards the IC. The ripple at the output of an external 3.3 V voltage regulator shall not exceed the limit of 50 mVpp in the range between 1 MHz and 66 MHz.

3.6 Host Interface (RST_N, INT_N, EN)

RST_N and EN are input signals to the PHY and typically driven by GPIO pins of the microcontroller, while INT_N is an input signal to the microcontroller.

INT_N is an open collector output, allowing to use several PHYs in parallel to one interrupt input of the microcontroller. Therefore, an external pull up (approx. 10 kΩ) is needed. No further components are needed.

For EN and RST_N a pull-up or pull-down can be applied in case a certain level is expected as default (EN has weak pull down internally, RST_N has weak pull up internally). The value (e.g. 10 kΩ) should be chosen such that a proper high/low level is ensured (considering also other resistances at this line, e.g. in the microcontroller).

If the EN pin or RST_N pin is not used, it shall be connected to $V_{DD(IO)}$. INT_N can be left open if not used.

Note that a series jumper shall be considered for the EN pin since this pin will be reconfigured as output and signals the TX_TCLK clock signal in test mode. See section 6.4 for further information.

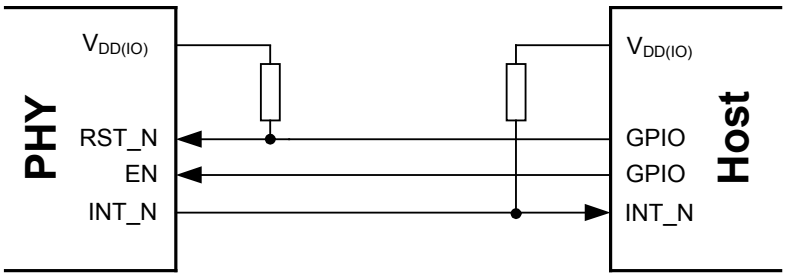


Fig 16. Example Host interface

Note that the EN is only checked when the PHY is initiated. At a startup with EN low the PHY will first enter Standby and will react after this to the EN low to enter Disable mode.

3.7 WAKE/LED pin

The functionality of pin #8 can be configured by the configuration bit 18.3. In case this bit is set to ‘1’ pin #8 provides a LED output, while per default pin #8 is configured as a wake input. Fig 17 shows a typical application circuit in case pin #8 is used as LED output. The following signals can be indicated at the LED output depending on configuration: link status, frame reception, symbol error, CRS signal.

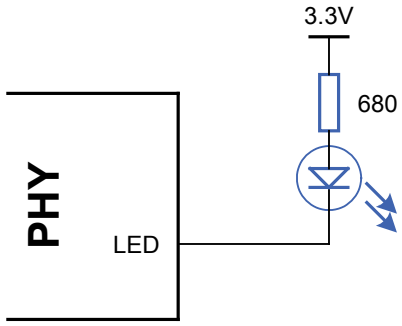


Fig 17. LED application circuit

In case pin #8 is used to receive a wakeup from the microcontroller the WAKE pin is simply connected to a corresponding GPIO of the microcontroller. A $V_{DD(IO)}$ ratiometric input threshold for pin WAKE has to be configured by configuration bit 18.2. Notice that only a falling edge will trigger a local wakeup. Fig 18 shows an example with a simple switch as wake-up source.

If the WAKE input should be able to receive wakeup signals from different sources e.g. from the microcontroller and another high-active wakeup pulse, the application circuit for the WAKE pin may look like in Fig 19.

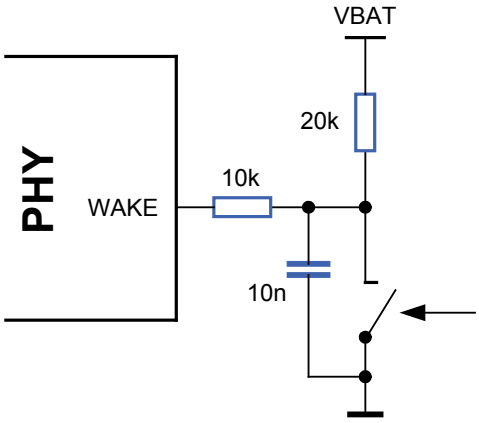


Fig 18. Wake application with external switch

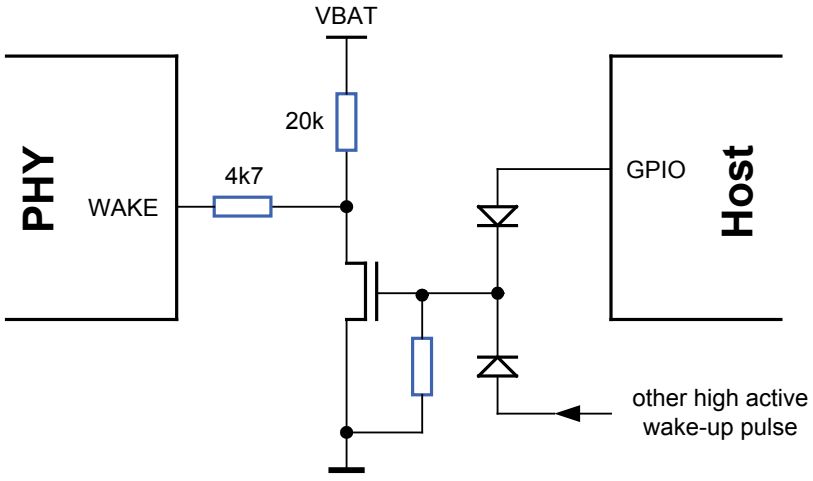


Fig 19. Wake application circuit with two different wakeup sources

3.8 Pin strapping

The TJA1100 allows for some hardware configuration via pin-strapping during power-on at the pins #22, #21, #18, #17. A pull-up is coded as logic '1', while a pull-down is coded as logic '0'. The pull-up/down resistors shall have a value of around 5 kΩ to 20 kΩ. It should be as high as possible to have low impact to the data signal, but needs to be small enough to have the correct pin strapping value (e.g. to overrule reset behavior of µC pins).

Table 4. Hardware configuration

Bit/Pin	Register Name
CONFIG0/ Pin 22	1 = PHY configured as Master 0 = PHY configured as Slave
CONFIG1/ Pin 21	1 = Autonomous operation 0 = Managed operation
CONFIG3-2/ Pin 17, 18	00 = Normal MII mode 01 = RMII mode (external 50 MHz oscillator) 10 = RMII mode (external 25 MHz crystal) 11 = Reverse MII mode

In the same way, the two [1:0] bits of the PHY address can be modified via pin-strapping at the pins #23 and #24, respectively.

Pin-strapping by means of pull-up/down resistors will not work if the microcontroller in reset drives a fixed level on these pins during power-on. In this case the microcontroller is recommended to hold the PHY in reset (RST_N pin Low) during power-on. Once the microcontroller is initialized, the software can drive the strapping pins to the required levels and then release the PHY reset.

Fig 20 shows when the EN pin, the RST_N pin and the pin-strapping pins are sampled during power-on and hardware reset phase. Standby init is an intermediate state between from Power-on/Reset mode to Standby mode.

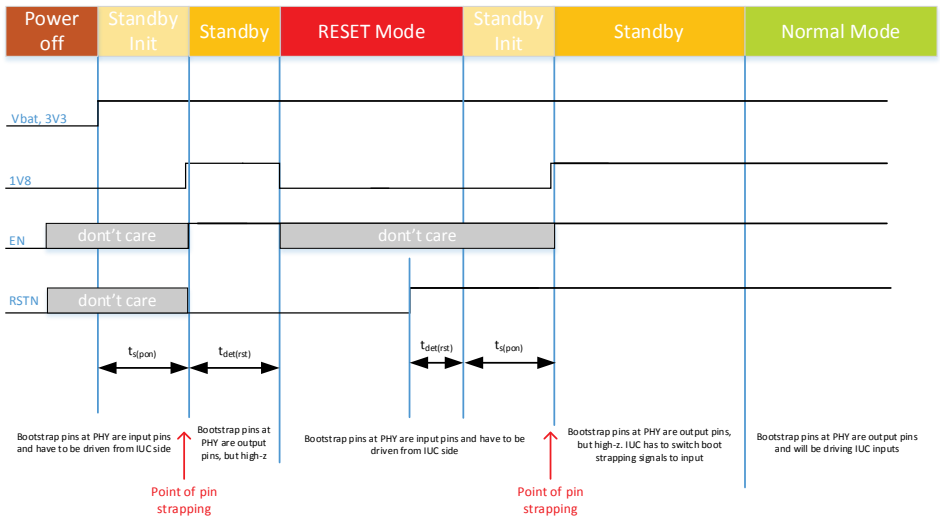


Fig 20. EN/RST_N/Pin-strapping sample time during power-on/reset phase

3.9 Clocking (XTAL)

For clocking the TJA1100, a 25 MHz XTAL can be used and in RMII alternatively a 50 MHz clock on REF_CLK. In case a XTAL is used, it should fulfill the requirements as given in below.

Table 5. XTAL requirements

Name	requirement
Frequency	25 MHz
Tolerance	MII/RMII: 100 ppm **Note:** This is including all influencing effects (e.g. aging, temperature, …)
ESR	max. 100 Ω, typ. 40 to 60 Ω
Load capacitance	Around 10, see description below
Drive level	< 100 µW

3.9.1 Load capacitance

For the calculation of the load capacitance, the trimming of the XTAL needs to be taken into account. This information will be given by the XTAL supplier and the resulting capacitor on the PCB should match with this requirement to reach the ppm requirements. The XO has typically 2 pF, XI 3.5 pF capacitance.
Please note that XI is an input for crystal usages only. This pin shall not be used as a general clock input pin.

4. Power-up/down

The TJA1100 has been designed in a way that no dedicated supply sequence is necessary. It does not matter whether first the 3.3 V pins will be supplied and then the V_{BAT} pin or vice versa. Being optimized for automotive use cases the TJA1100 can also handle a wide range of slow and fast ramping supply conditions.

5. Basic control & basic status

5.1 Basic control

For basic PHY applications the TJA1100 provides some basic control features like Reset, Loopback, Powerdown, Isolate, and Unidirectional-Enable. These features can be accessed by the standard Basic Control Register (register address 0x00) defined in clause 22 of IEEE802.3. Notice the control bits #13, #12, #9, #8, #7, #6 are not applicable to an 100BASE-T1 PHY and therefore are without function in the TJA1100.

5.1.1 Reset

The PHY part (including the communication status register) of the TJA1100 can be reset by setting bit #15 (RESET) in the Basic Control register. Upon completion of the reset process, which may take up to 1ms, this bit is automatically cleared. Any register access should be avoided during the reset process. Resetting the PHY part may be helpful when facing difficulties to get a link up and running.

5.1.2 Loopback

Loopback operation can be advantageously used for diagnosis purposes, especially to locate potential error sources. In principle Ethernet frames are sent by the MAC and reflected back at some point of the signal path, forming a closed loop. If the loop is error-free, the MAC will receive the same frames as sent out before.

In accordance with the IEEE specifications, the TJA1100 provides three loopback modes with different reflection points: internal, external and remote loopback. In case of internal loopback, the reflection point is after the PCS block, thus checking proper operation of the internal PCS part. In case of external loopback, the reflection point is after the PMA block, thus checking proper operation of both the internal PCS and PMA part. The remote loopback finally spans the entire loop from one PHY to the other PHY and back to the first PHY, thus includes the entire channel. The loopback mode can be selected by the bits [4:3] in the Extended Control register. To activate and deactivate the loopback operation the below sequence should be followed:

- Select loopback mode (and Normal mode) in Extended Control register
- Enable loopback operation in Basic Control register
- Enable LINK_CONTROL in Extended Control register
- (Loopback operation is active now)
- Disable LINK_CONTROL in Extended Control register
- Disable loopback operation in Basic Control register

5.1.3 Powerdown

By setting the bit #11 (POWER_DOWN) in the Basic Control register the TJA1100 is forced into the Standby mode (see chapter 7.1). Any power mode change in the Extended Control register, while POWER_DOWN is enabled will be ignored and will trigger a CONTROL_ERROR interrupt. When this bit is reset, the TJA1100 continues in Standby mode until another mode control command is given in the Extended Control register.

5.1.4 Isolate

If bit #10 (ISOLATE) is set, the PHY is isolated from the MII/RMII, that means any transmit request from the MAC is ignored and output pins like RXD[3:0], RXDV, RXER, RXC, TXC are switched to high-impedance. Isolate operation is needed when a MAC shall have the possibility to access two or more PHYs on the same board in a time division manner.

5.1.5 Unidirectional-Enable

Before normal communication can take place, a link must be established between the two partners. With setting bit #5 (UNIDIRECT_EN) the TJA1100 is forced to process any transmit request from the MII/RMII regardless of whether a valid link has been established before. The transmission process in unidirectional mode will always use its own local clock as time base regardless of the configuration as Master or Slave.

5.2 Basic status

The TJA1100 also provides some basic status like Remote fault, Link status and Jabber detect. This status can be accessed by the standard Basic Status Register (register address 0x01) defined in clause 22 of IEEE802.3. Note that the status bits #15, #14, #13, #12, #11, #10, #9, #8, #7, #6, #5, #3, #0 are not applicable to OABR PHY.

5.2.1 Remote fault

When bit #4 (REMOTE_FAULT) read as “1”, it indicates that a remote fault condition has been detected. This bit will be set if the remote receiver is not OK in the TJA1100.

5.2.2 Link status

When bit #2 (LINK_STATUS) read as “1”, it indicates that the TJA1100 receiver synchronizes to the data stream of the link partner. It only means the LOC_RCVR_STATUS (bit #12 in Communication Status Register) has been OK for a certain time. It doesn’t mean a valid link has been established.

LINK_UP (bit #15 in Communication Status Register) is combining LOC_RCVR_STATUS, REM_RCVR_STATUS, SCR_LOCKED and SQI=OK (i.e. SQI higher than defined SQI_FAILLIMIT). Thus, the link is established when LINK_UP is set.

5.2.3 Jabber detect

When bit #1 (JABBER_DETECT) read as “1”, it indicates that a jabber condition has been detected. A detailed description can be found in the TJA1100 datasheet [5].

6. Extended control

The Extended Control register allows access to TJA1100 specific control features beyond that of the basic control features described in the chapter before. These extended control features are described in detail in the following.

6.1 Link control

In managed operation (see chapter 8.1) the LINK_CONTROL bit must be set before a link will be established. This holds for both the Master and Slave PHY. Once this bit is set the Master PHY starts initiating the training phase by sending Idle. As soon as the Slave PHY has been synchronized, it will respond by sending Idle too. To disable a link, the LINK_CONTROL bit must be reset. A mode transition from Normal to Standby, Disable or Reset mode will automatically reset the LINK_CONTROL bit.

In autonomous operation, the LINK_CONTROL bit will be automatically set with entering the Normal mode. As a result, a link startup will be performed automatically after power-on. LINK_CONTROL should not be changed per SMI when in autonomous mode.

6.2 Power modes

The TJA1100 provides three main power modes: Normal, Standby, Sleep (Request), which can be controlled by the bits [14:11] in the Extended Control register, provided that the POWER_DOWN bit in the Basic Control register is reset. The power modes are described in detail in chapter 7.

6.3 Training restart

In case the receiver cannot be synchronized within a certain time (no LINK_UP) during training, the TJA1100 aborts the current training phase. After reset of the complete receiver a new training phase will be started. A failed training phase will be indicated in the interrupt source register.

6.4 Test modes

According to the 100BASE-T1 specification, the TJA1100 provides five different test modes which can be selected by the extended control bits [8:6]. The test modes are needed for compliance testing against 100BASE-T1 specification and for ECU level tests as described in [4]. A detailed description can also be found in the data sheet of the TJA1100. To run a test mode, the TJA1100 must be in Normal mode and LINK_CONTROL must be disabled. In test modes 1-4 the EN pin is reconfigured as output and signals the TX_TCLK clock signal. A jumper may be used to allow TX_TCLK signal for PMA measurements on ECU level and disconnecting the EN function. The PHY shall be configured as slave for return loss measurement in the PMA test.

6.5 Cable test

The TJA1100 is able to detect open and short circuits between the twisted pair bus lines. Note that a short circuit between the bus line (TRX_P/TRX_M) and ground or power supply can’t be detected by cable test.

When bit #5 (CABLE_TEST) is set, test pulses are transmitted onto the cable with a repetition rate of 666.6 kHz. The TJA1100 evaluates the reflected signals and uses

impedance mismatch data along the channel to determine the quality of the link. The cable test is completed within maximum 100 µs. The result can then be read from the External Status register. Please make sure that the cable is terminated with the link partner or a dedicated 100 Ω resistor. This TDR-based measurement is confined to detecting open and short circuits in and between the cable wires. Shorts between a single wire and the battery voltage or ground may not be detected.

To trigger the cable test, the TJA1100 must be in Normal mode, the communication shall be stopped completely and the LINK_CONTROL bit must be disabled. In case a faulty SMI command simultaneously commands test mode and cable test, the latter would prevail. Once the cable test expires (bit is self-clearing), the TJA1100 would switch to test mode operation.

Note: When cable tests are started and the link partner is configured as Master there can be an ambiguity in the cable tests results. If the line is properly terminated, then for this particular case both Open and Short flags will be indicated.

6.6 Loopback mode

The TJA1100 supports internal, external and remote loopback. The loopback mode can be selected by bits [4:3] of the Extended Control register.

6.7 Configuration register access

Writing to the configuration registers is disabled by default for safety reasons. To change the configuration, configuration register writing must be enabled before by setting bit #2 (CONFIG_EN) in the Extended Control register. The configuration is expected to happen after power-on as part of the initialization routine; however, re-configuration of the PHY is possible at any later time. Before re-configuration it is recommended to stop the link first and to enter Standby mode. After changing the configuration, it is recommended to disable write access again.

6.8 INH control in Disable mode

The behavior of the INH output in Disable mode can be controlled by bit #1 (CONFIG_INH) in the Extended Control register. A `0` switches INH off, while a `1` switches INH on in Disable mode. This allows selecting the INH behavior according to application needs.

6.9 Wake request

A link in Sleep must be activated before a link can be re-established. For this reason, the node requesting the link can issue a wake request by sending Idle onto the link. The link partner will detect the Idle activity and will wake up subsequently.

To request a link wake-up, bit #0 (WAKE_REQUEST) in the Extended Control register shall be set, while the TJA1100 is in Normal mode and LINK_CONTROL is disabled. The wake request phase shall last at least 5 ms to ensure a reliable wake-up. The TJA1100 stops the wake request and stops sending Idle with resetting bit #0 or with enabling LINK_CONTROL.

7. Power Modes

One of the features of the TJA1100 is the possibility to put a link and the associated node into the Sleep state, while the node can be still woken up with activity on the Ethernet wires. In this way, nodes whose functionality is temporarily not needed can be switched to the Sleep state with minimum power consumption.

7.1 Standby mode

After power-on (no under-voltage on pin V_{BAT}) the TJA1100 will enter Standby mode and the INH control output (pin #10) is activated. This battery related control signal may be used to activate the main voltage supply of the ECU. Once the 3.3 V supply voltage is available, the internal 1.8 V regulator is activated and pin strapping is done at the corresponding configuration and PHY address pins. No SMI access shall take place during this initialization period of max. 2 ms duration.

From operation point of view the Standby mode corresponds to the IEEE802.3 Power-Down mode, with transmit and receive functions disabled. The Standby mode also acts as a fail-silent mode and is entered when an under-voltage condition at the pin $V_{DDA(3V3)}$ or pin $V_{DD(IO)}$ occurs.

7.2 Normal mode

To establish a communication link, the TJA1100 must be brought into Normal mode via SMI command before. With entering the Normal mode, the internal PLL starts running and the transmit and receive functions will be enabled. After a stabilization time of 2 ms the TJA1100 is ready to set up a link. Once the LINK_CONTROL bit is set to ‘ENABLE’, the PHY configured as Master initiates the training sequence by sending Idle pulses (see chapter 2.2 for the link startup process).

While this procedure is valid for host controlled operation (AUTO_OP=’0’ in configuration 1 register), in case of autonomous operation (AUTO_OP=’1’) the TJA1100 will automatically enter Normal mode and activate the link upon power-on.

7.3 Sleep mode

If the ECU or network management in a node decides to withdraw from the network because the functions of the node are temporarily not needed, it may power down the entire ECU, while the TJA1100 resides in Sleep mode and keeps partly supplied from the battery terminal. In Sleep mode, all internal functions are switched off except the WAKE input and the activity detection.

By releasing the INH output, the ECU is allowed to switch off its main power supply unit. Typically, the entire ECU is powered down. The TJA1100 is kept partly alive by the permanent battery terminal and can still react to activity on the Ethernet lines or WAKE pin. Once Ethernet Idle pulses or frames are detected on the lines or there is a falling edge on the WAKE pin, the TJA1100 wakes up, switching on the main power unit via the INH control signal. As soon as the supply voltages become stable within their operating ranges, the TJA1100 can be switched to Normal mode via an SMI command and the communication link to the partner can be re-established.

The Sleep mode can be entered from Normal mode via the intermediate Sleep Request mode as well as from Standby mode. It should be noted that the configuration register settings are maintained during Sleep mode.

7.4 Sleep request mode

The Sleep Request mode is an intermediate state to introduce the transition to Sleep mode. The Sleep Request timer starts when the TJA1100 enters Sleep Request mode. This timer determines how long the PHY remains in Sleep Request mode. When the timer expires, the PHY switches to Sleep mode and INH is switched off. The PHY does not expect to receive Ethernet frames in Sleep Request mode. So, if any Ethernet frame is received at MDI or MII, the PHY will return to Normal mode and trigger a wake-up interrupt. The transition to Sleep mode will also be aborted with a Normal mode command.

Link should be terminated before entering sleep mode to ensure no activity anymore once sleep is entered.

7.5 Disable mode

Whenever the Ethernet interface is not in use or needs to be disabled for fail-safe reasons, the PHY can be switched off by pulling pin EN LOW. In Disable mode, the PHY is switched off completely, including the internal 1.8 V regulator, thus minimizing power consumption. The configuration register settings are maintained. To exit Disable mode, pin EN needs to be forced HIGH to activate the PHY. The Disable mode will also be left if there is an under-voltage condition on $V_{DD(IO)}$.

7.6 Reset

The complete device can be reset with asserting the RST_N pin for at least 1 ms (Low active). All registers (including configuration) will be set back to their default values. In contrast a software reset only resets the PHY part of the device.

7.7 Mode transitions

7.7.1 Link wake-up from Sleep mode

The procedure for waking up and reactivating a link from Sleep is illustrated in Fig 21. Assume as a starting point that both link partners are in Sleep mode. An end node (here the left side) may have received a wake-up from the CAN or LIN interface and now requests Ethernet communication. The management software initiates the wake-up process by switching PHY1 to Normal mode and reactivates the link by issuing a wake-up request to the PHY.

As a result, the PHY starts transmitting Idle codes (tx_mode=SEND_I). The activity on the twisted-pair lines will be detected by the partner PHY, which in turn switches via Sleep to Standby mode and activates its ECU via the INH signal. The microcontroller can configure the PHY to Normal mode then trigger the training phase by enabling link control (LINK_CONTROL=1) after activation.

A WU interrupt signals a remote wake-up event to the management and the wake-up source can be read from the PHY registers. Upon a remote wake-up the link control will be enabled and the training phase can start immediately. As soon as the link is ready,

signaled by a LINK_UP interrupt, the network management can start with sending NM messages.

Since a dedicated wake-up phase has been introduced, the described procedure is the same as whether a Master PHY or Slave PHY initiates the link wake-up.

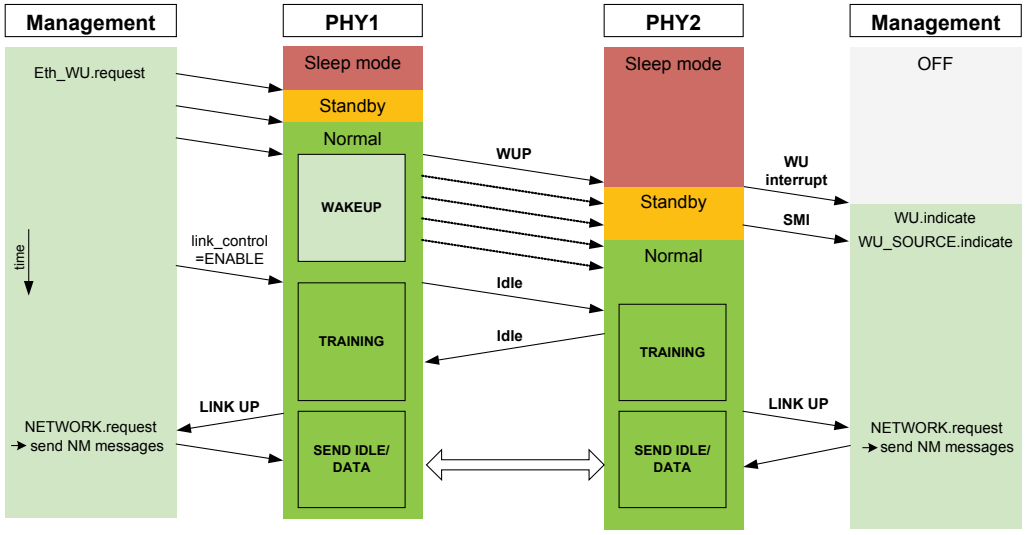


Fig 21. Wake-up from Sleep

8. Software aspects

This chapter introduces the software aspects of the TJA1100 and illustrates the different operations between “Power-on” and “Power-off”. Therefore, the Fig 22 provides a quick overview about:

- Different kind of operations
- Order of the operations
- Subchapter, where the operation is discussed in more detail

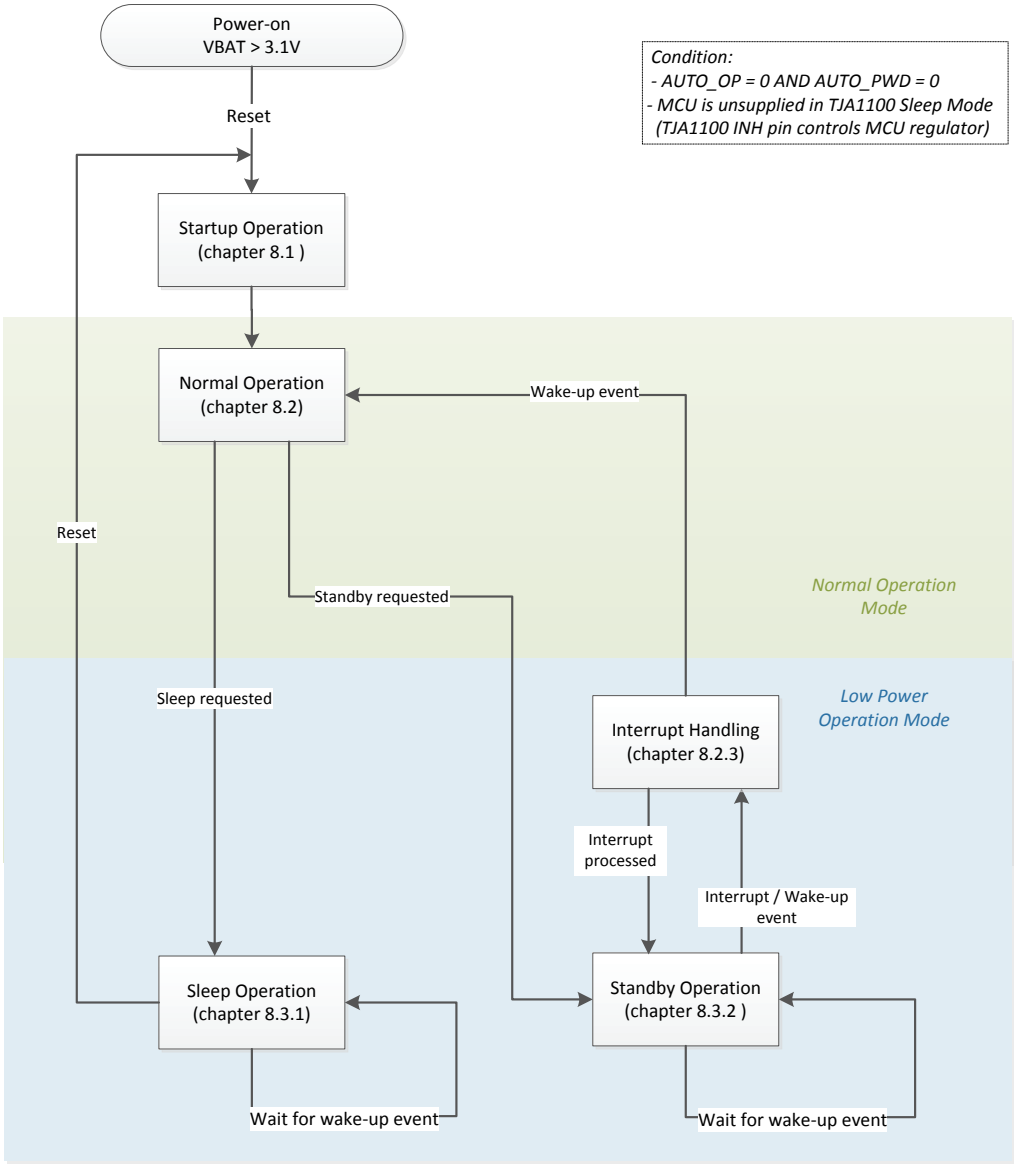


Fig 22. Abstract view of Software Flow (if AUTO_OP = AUTO_PWD = 0)

For the illustration of the software flow in the following chapters, it is assumed that the TJA1100 PHY is controlled externally by the microcontroller and does not change its modes automatically (AUTO_OP = AUTO_PWD = 0). Furthermore, the PHY is running in Normal Operation, thus POWER_DOWN in the Basic Control Register is initialized with 0. Additionally, following chapters assume that the voltage regulator of the microcontroller is controlled by the TJA1100 INH. This means, the microcontroller is unsupplied in TJA1100 Sleep Mode.

Fig 23 below shows the simplified state diagram of the TJA1100 from software perspective. This state diagram will be used in the following subchapters to establish the link between the different software operations and the related TJA1100 operating modes.

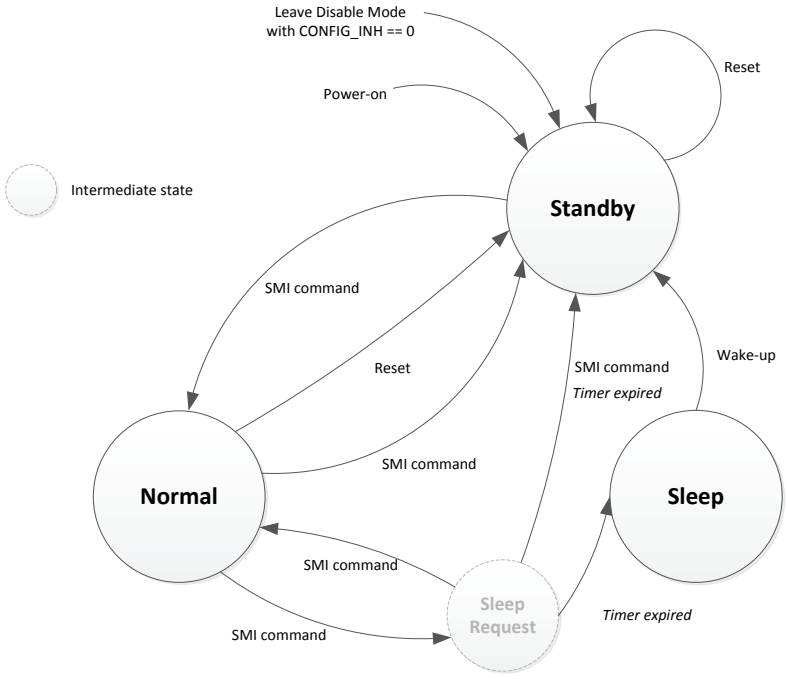


Fig 23. Simplified TJA1100 mode diagram from SW perspective

8.1 Startup operation

This section introduces the software operations, which are related to the startup of the application. The Startup Operation takes place in Standby Mode of the TJA1100 (see picture Fig 24). The figure below shows the different hardware events that trigger the execution of the Startup Operation. All kinds of resets (e.g. external reset, leave Disable Mode with INH off) trigger the execution of the Startup Operation. Furthermore, “Power-on” and “Wake-up” events trigger the Startup Operation as well. At the end of the Startup Operation a transition to Normal Operation Mode is performed via the related SMI command.

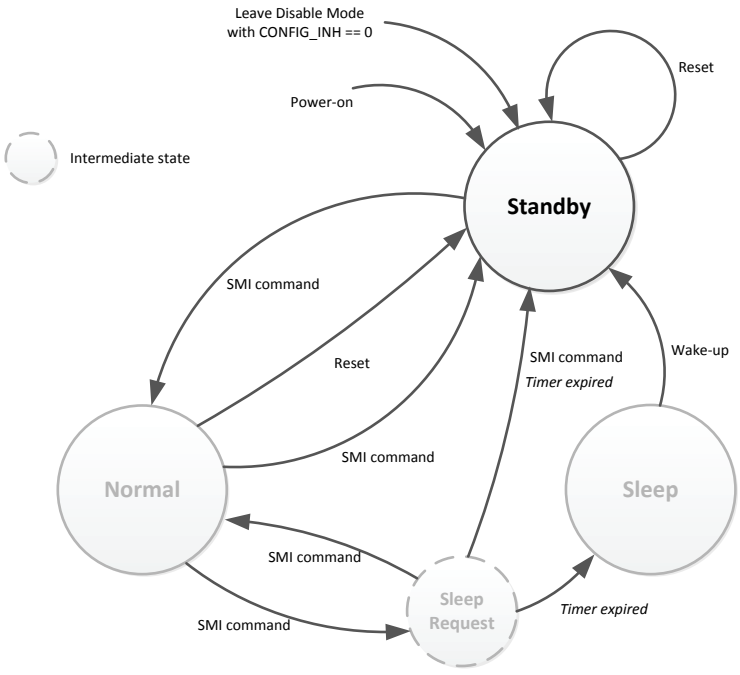


Fig 24. Simplified mode diagram with focus on Startup Operation

The Startup Operation typically consists of the following parts:

- Microcontroller initialization
- Application initialization
- Check of device identification
- Reset / Wake-up Source Detection incl. PHY initialization, if Power-On has been detected
- Startup interrupt handling
- Transition to Normal Operation Mode

Fig 25 shows the complete flow of the Startup Operation with its different parts. Moreover, it guides to the related subchapter for a detailed explanation.

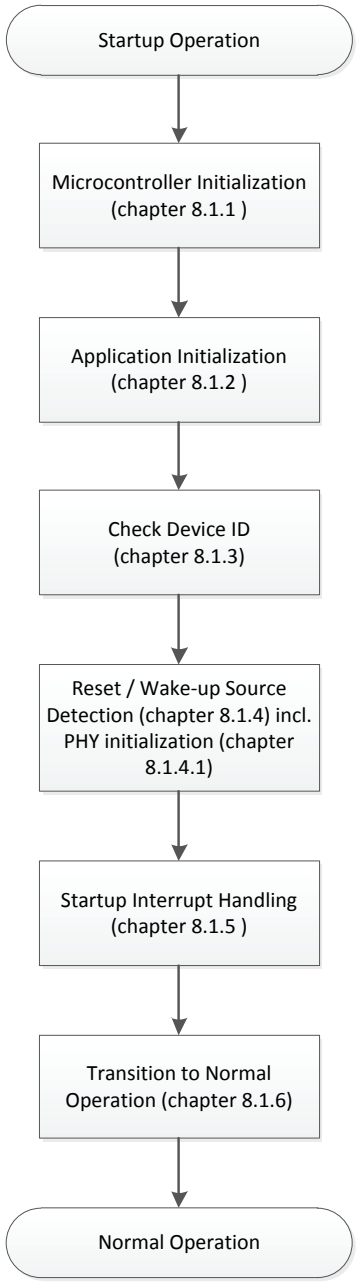


Fig 25. Startup Operation Software Flow

8.1.1 Microcontroller initialization

The microcontroller initialization is always the first part of the startup routine. It is a microcontroller specific routine that configures the microcontroller and its periphery. With respect to the TJA1100 PHY, at least the pins needed for the Serial Management Interface (SMI; containing of Management Data Clock (MDC) and Management Data Input / Output (MDIO)) must be configured to ensure that the SMI of the microcontroller is

working properly after the initialization. Otherwise no communication with the TJA1100 can take place.

Additionally, it must be ensured that the bits, configured by pin strapping, are not overruled by the microcontroller pin configuration during initialization. This can easily be achieved, if

- The according microcontroller pins are high-ohmic during initialization phase (recommended),
- The relevant pins are configured as specified by pin strapping or
- The RST_N pin is not released until the relevant microcontroller pins are configured (high-ohmic).

This is valid for the TJA1100 pins CONFIG0, CONFIG1, CONFIG2, CONFIG3, PHYAD0 and PHYAD1 or rather the register bits MASTER_SLAVE, AUTO_OP, MII_Mode and PHYAD.

8.1.2 Application initialization

The application initialization is also necessary at the beginning of the startup routine. It is an application specific routine that initializes the global application specific variables and is completely independent from TJA1100 hardware.

8.1.3 Check device identification

In order to check, if the running application software is used for the correct device, the PHY Identification Registers (SMI addresses: 0x2, 0x3) are read and the ID is checked. This is required to ensure that the software runs with the correct device.

Sometimes the intermediate version of the PHY may be used, so the application software can check the type number and revision number (the PHY Identification Register 2, SMI address: 0x3) to distinguish the intermediate version (MRA2, MRA3) and the final version (MRA4).

Table 6. Type/revision number of MRA2/MRA3/MRA4

PHY version	Type number (binary)	Revision number (binary)
MRA2	000110	0000
MRA3	000100	1000
MRA4	000100	0001

8.1.4 Reset / Wake-up source detection

The next step in the Startup Operation is the reset or wake-up source detection, respectively. Fig 26 illustrates the software flow for the Reset and Wake-up Source Detection. The flow is divided into a status check of the TJA1100 and the detection itself.

To ensure that no error has occurred during PHY initialization, at first the PHY Init status is checked. Therefore, the Interrupt Status Register (SMI address: 0x15) is read (and thus also cleared; data are processed afterwards, see chapter 8.1.5) and the

PHY_INIT_FAIL bit is evaluated. In case there was no PHY hardware initialization error, this bit is 0 and the Reset and Wake-up Source Detection can be started.

If PHY_INIT_FAIL is set to 1, a PHY hardware initialization error has been detected and a PHY Software Reset should be asserted. This is done by a SMI write access to the Basic Control Register (SMI address: 0x0) with RESET bit set to 1. After that, this register is polled until the RESET bit is 0 again. If PHY_INIT_FAIL does not become 0 after several PHY RESETs, a hardware error can be assumed.

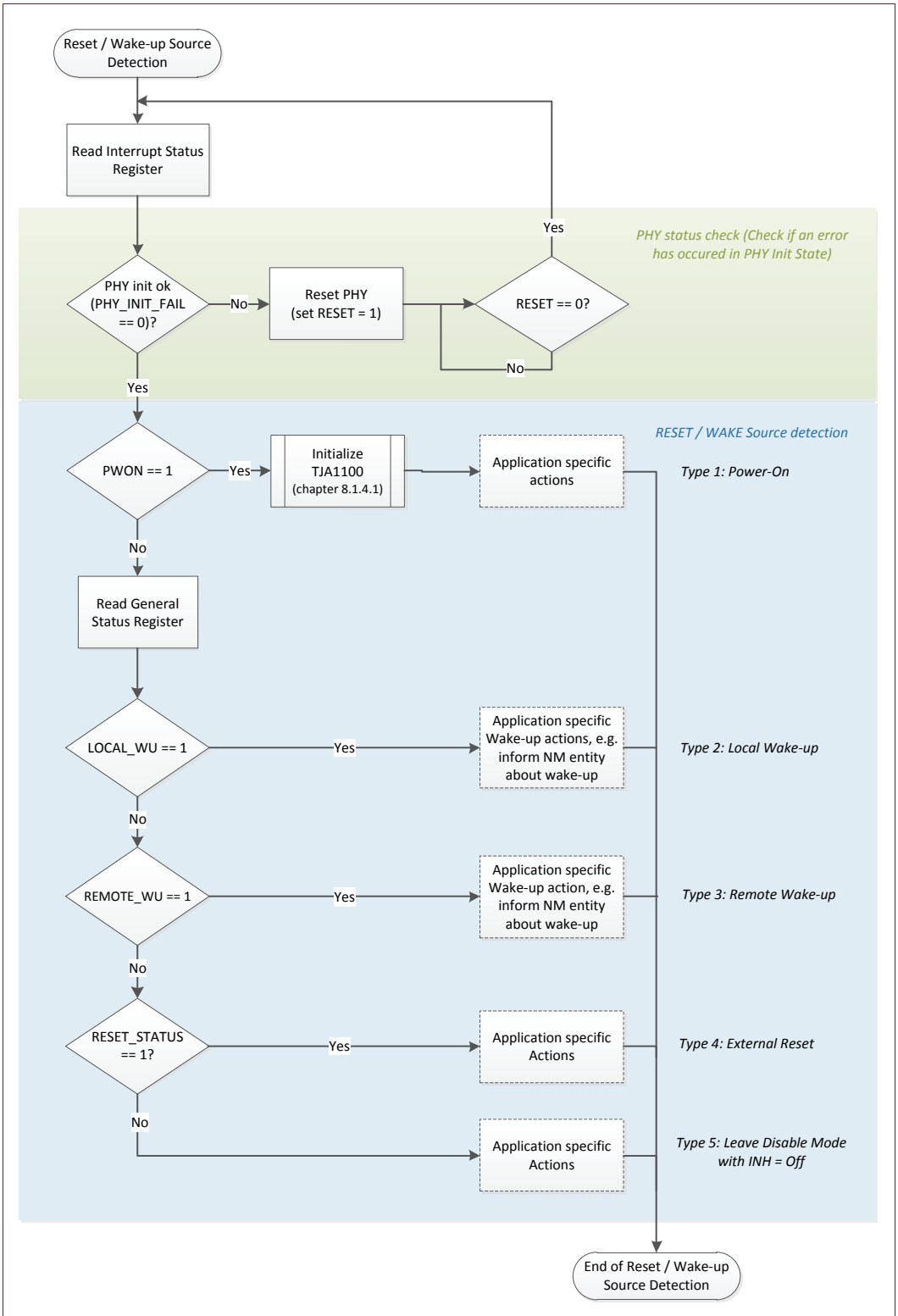


Fig 26. Reset / Wake-up Source Detection

8.1.4.1 PHY initialization

In case the reason for the reset was a power-on the TJA1100 must be initialized. This contains SMI write accesses to:

- The Extended Control Register (SMI address: 0x11) with CONFIG_EN = 1 in order to enabled write accesses to Configuration Registers
- The Configuration registers (Configuration 1 Register (SMI address: 0x12), Configuration 2 Register (SMI address: 0x13) in order to configure the TJA1100
- The Interrupt Enable Register in order to enable or mask the interrupts. In order to be informed quickly about any error during communication and to get an interrupt after a wake-up, it is recommended to enable all interrupts (SMI Address: 0x16, SMI data: 0Xffff).

See Fig 27 for illustration of the flow.

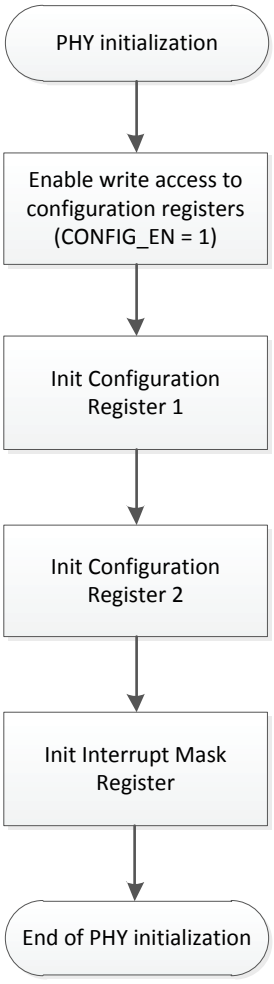


Fig 27. PHY initialization

8.1.5 Startup interrupt handling

Due to the SMI read access of the Interrupt Status Register (SMI address: 0x15) during the Reset and Wake-up Source Detection, the Interrupt Status Register is cleared. Nevertheless, all pending interrupts should be handled. Therefore, the read value of the Interrupt Status Register has to be stored in a variable.

As Power-On (PWON), Wake-Up (WAKEUP) and PHY initialization fail (PHY_INIT_FAIL) are already handled during Reset and Wake-up Source detection, only following interrupts are handled during Startup Interrupt Handling:

- SMI Control Error (CONTROL_ERROR)
- Undervoltage detection on $V_{DD(IO)}$, $V_{DDA(1V8)}$, $V_{DDD(1V8)}$, $V_{DDA(3V3)}$ (UV_ERROR)
- Undervoltage Recovery (UV_RECOVERY)
- Over temperature (TEMP_ERROR)

8.1.6 Transition to Normal mode

TJA1100 Normal Mode is entered by a SMI write access (POWER_MODE = 0x3) to the Extended Control Register (SMI address: 0x11). It is recommended to disable the write access to Configuration Registers during Normal Operation. Therefore, the CONFIG_EN bit should be set to 0 in this SMI write command.

As Normal Mode can only be entered if no under voltage or over temperature is pending, it should be ensured that none of these events is present, when sending the Normal Mode command.

8.2 Normal operation

This section introduces the software operations which are associated to Normal Operation of the application. Normal Operation is related to the Normal Mode of the TJA1100. This mode should only be entered after a successful startup operation. Therefore, the beginning of Normal Operation is a transition from Standby to Normal Mode caused by the related SMI command.

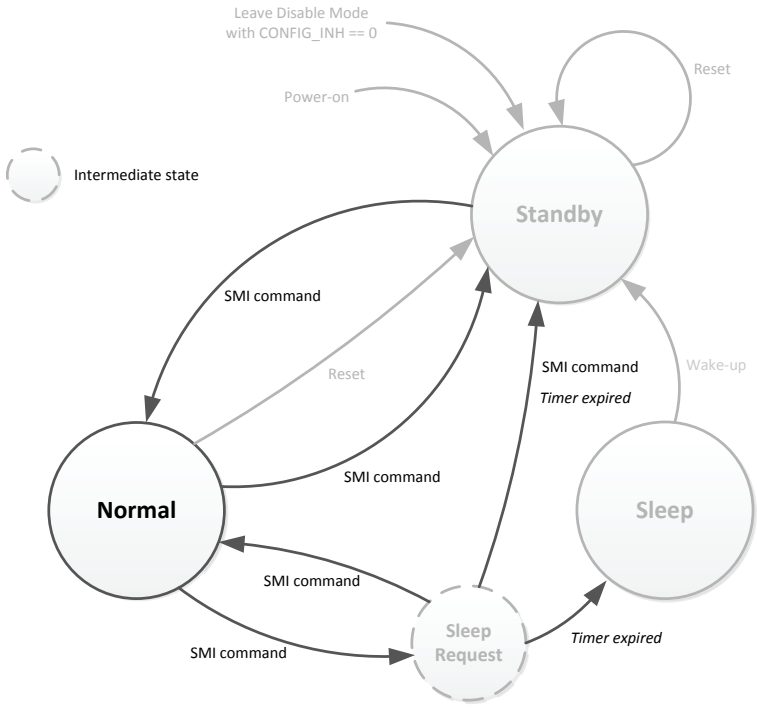


Fig 28. Simplified mode diagram with focus on Normal Operation

The most important operations of the Normal Operation are link startup, PHY status polling and interrupt handling. At the end of the Normal Operation a transition to Low Power Operation (Standby, Sleep) is performed via the related SPI command.

Hence, this chapter consists of:

- Enter Normal Operation
- Link Startup (chapter 8.2.1)
- Status polling (chapter 8.2.2)
- Interrupt Handling (chapter 8.2.3)
- Run default application (chapter 8.2.4)
- Transition to Low Power Operation (Standby, Sleep) (chapter 8.2.5)

8.2.1 Link startup

The next step after the transition to Normal Mode is the startup of the PHY link. After a small timeout of 2 ms the link must be enabled by setting LINK_CONTROL to 1 in the Extended Control Register (SMI address: 0x11). As the Link Startup (training sequence) takes some time, it should be checked whether the link is stable (LINK_UP = 1).

Fig 29 illustrates this Link Startup flow using the polling mechanism. The LINK stable check includes the four status bits of the communication status register (LOC_RCVR_STATUS ok, REM_LOC_STATUS ok, SCR_LOCKED, LINK_UP). LINK stable status can be polled, while using a loop (can be adapted to the application need) until a link could be established and communication can be started.

If no link could be established within 100 ms timeout after enabling the LINK_CONTROL bit, the link diagnosis process could be started to check whether an open or short in the Ethernet channel etc. Timing could be adapted if Master and Slave have different startup timings and it is expected to have a longer startup time when waiting for the link partner.

In case the TRAINING_FAILED interrupt occurs (see chapter 8.2.3) and this interrupt has been enabled before, Link Startup should be tried again. Restarting the Link means, disabling Link Control, waiting 100 µs and enabling the Link Control again, see Fig 30.

When configured as Slave and depending on the needs of the application, additionally the POLARITY_DETECT bit could be read to be informed whenever an MDI polarity inversion has been detected and corrected.

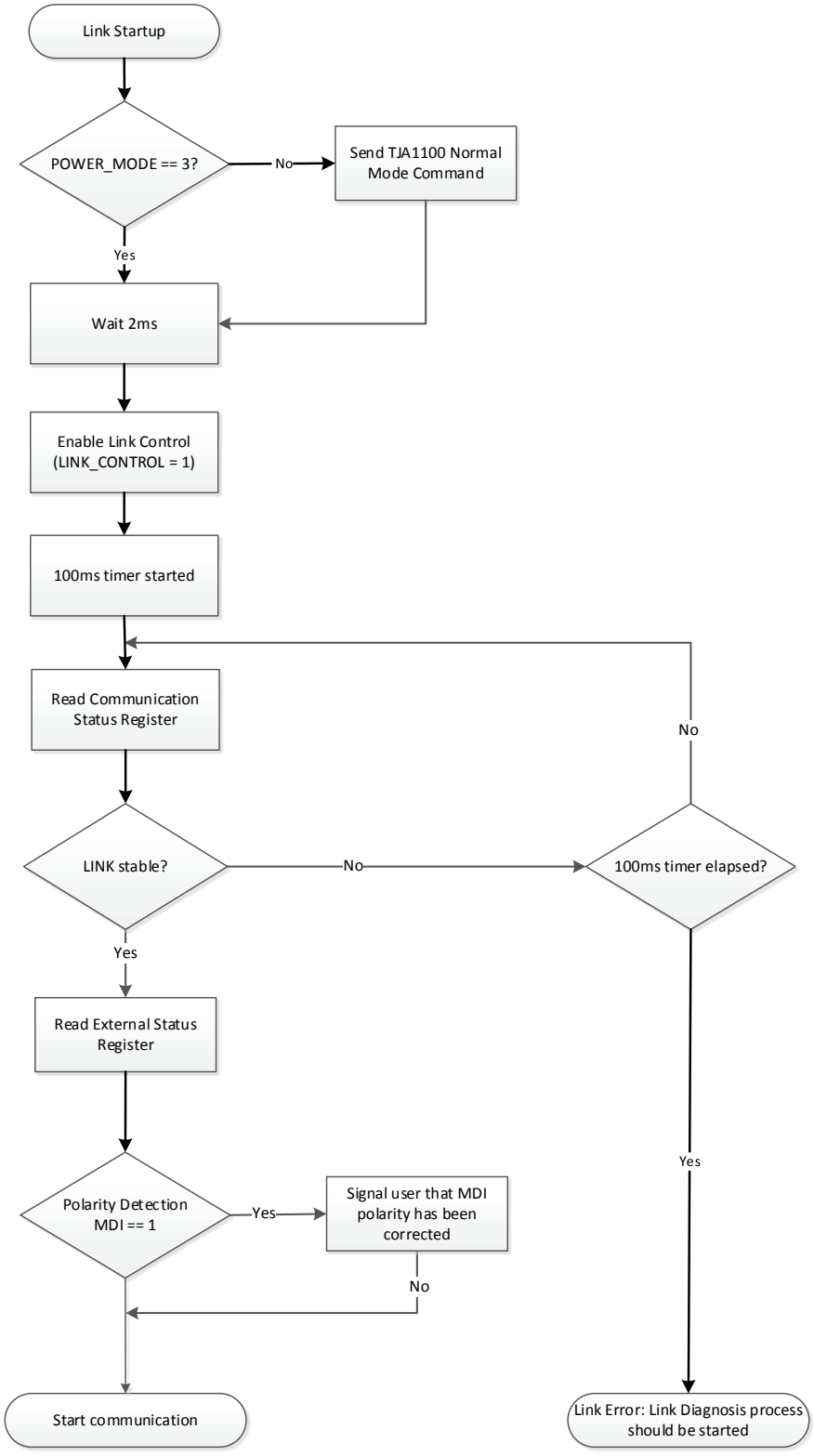


Fig 29. Link Startup (alternative 1 polling the Communication Status Register)

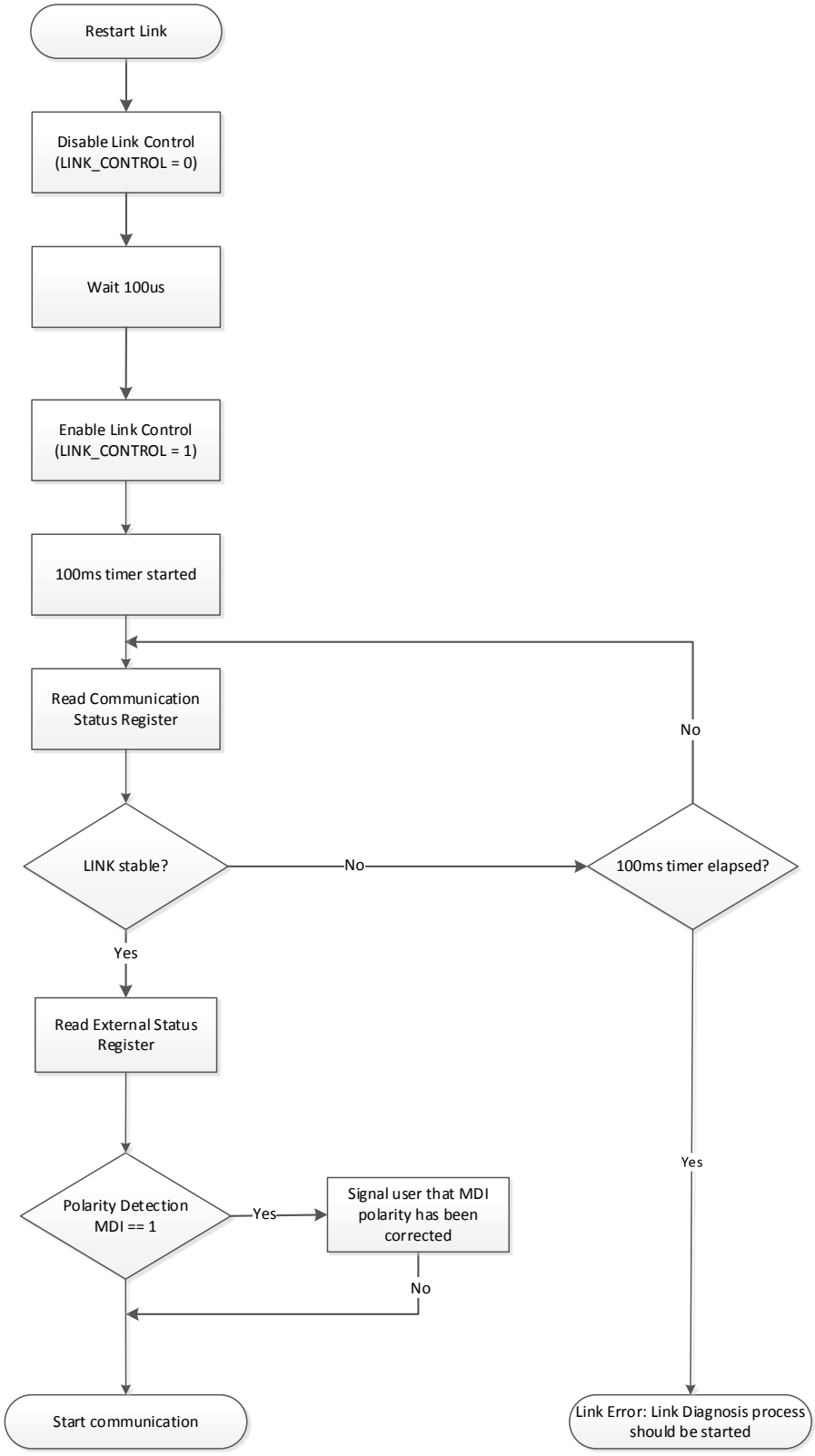


Fig 30. Restart Link

8.2.2 Status polling

If the link is up (see 8.2.1), the communication can be started. To monitor the Link Status all the time, the Communication Status Register (SMI address: 0x23) and the Basic Status Register (SMI address: 0x01) can be read periodically. As some status bits changes are signaled by interrupts (assumption: no interrupt is masked), for the status check of the PHY only following bits are relevant, if all interrupts are enabled:

Communication Status Register:

- TX_MODE (bit #14-13)
- LOC_RCVR_STATUS (bit #12)
- REM_RCVR_STATUS (bit #11)
- SSD_ERROR (bit #9)
- ESD_ERROR (bit #8)
- SQI (bit #7-5)
- RECEIVE_ERROR (bit #4)
- TRANSMIT_ERROR (bit #3)
- PHY_STATE (bit #2-0)

Basic Status Register:

- JABBER_DETECT (bit #1)

More detailed information is given in Fig 31 and Fig 32. These flow charts give an overview of what needs to be done in case an error is indicated by a status bit.

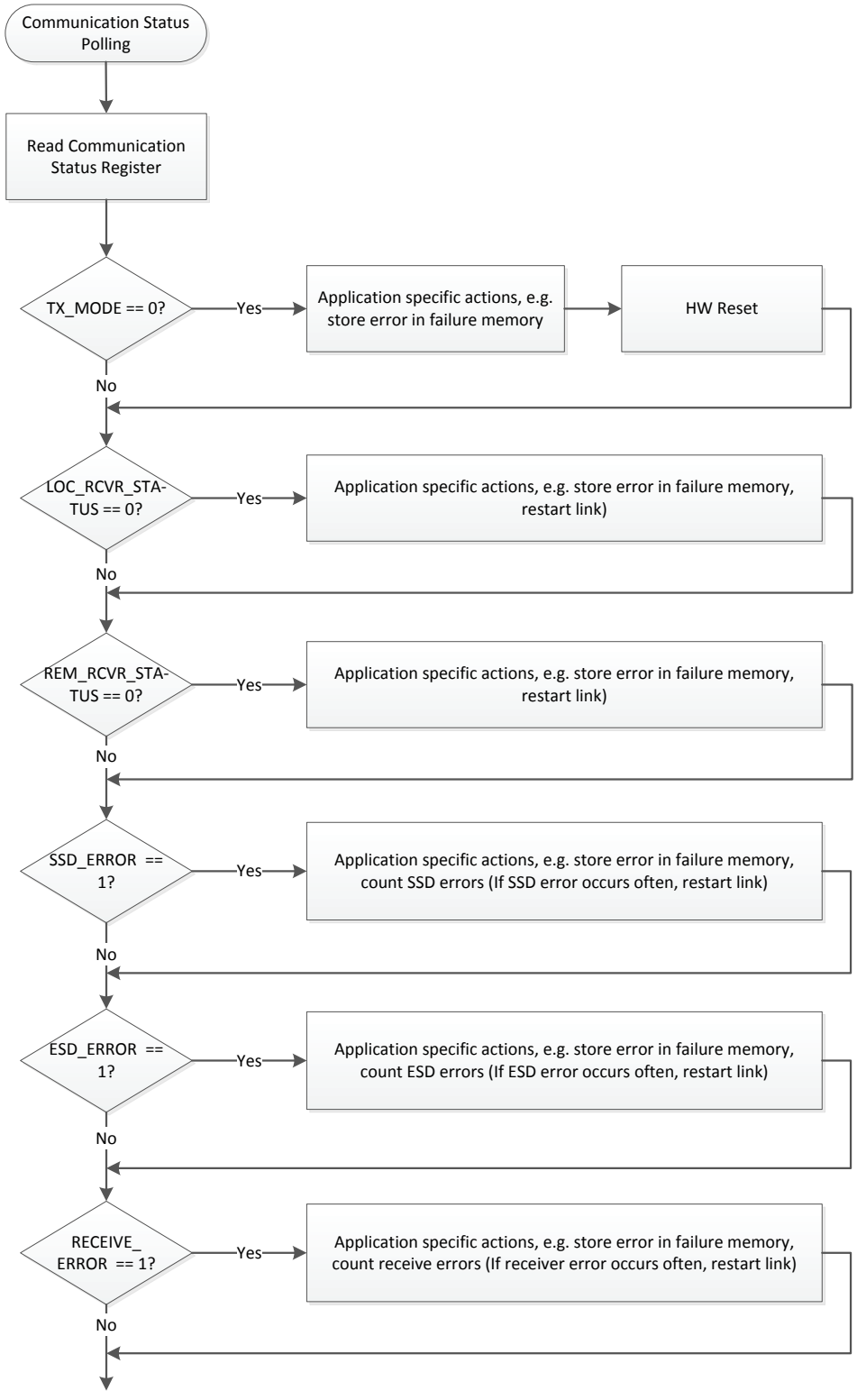


Fig 31. Status Polling in Normal Operation Mode (1)

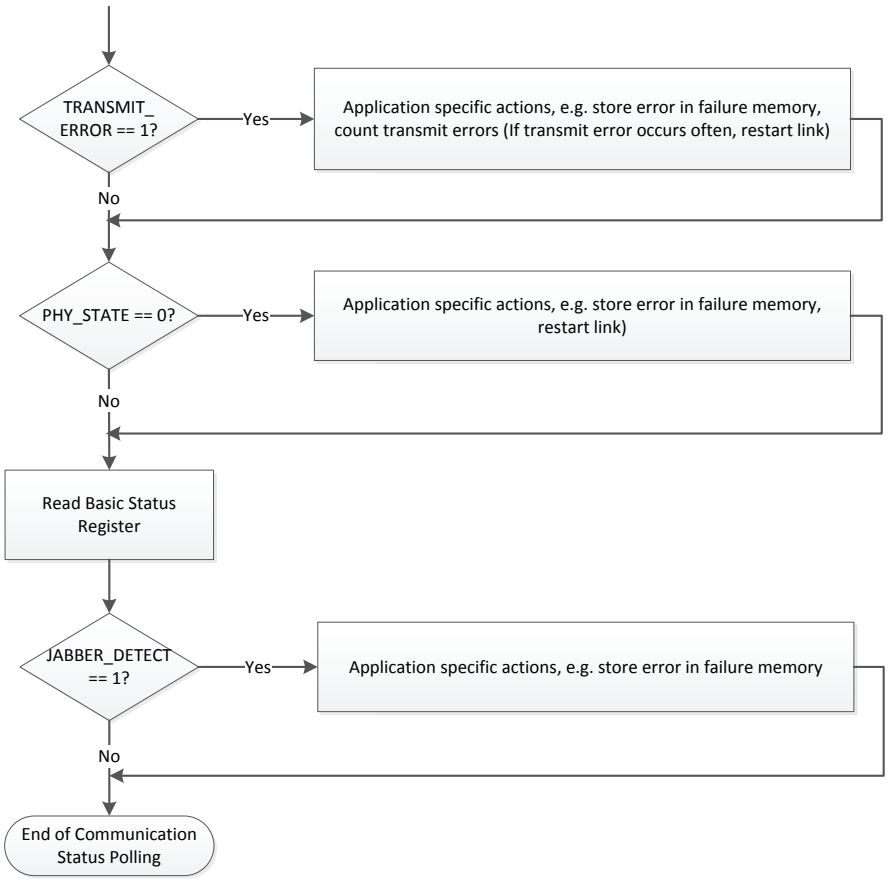


Fig 32. Status Polling in Normal Operation Mode (2)

Not shown in the diagram is the handling of SQI (Signal Quality Indication). The SQI value gives information on the actual channel quality. The higher the value, the better the signal quality. The SQI can be grouped in the following quality indications and signal quality classification:

Table 7. Link quality mapping

SQI value	Description
0	worse than class A SQI (unstable link)
1	Class A SQI (unstable link)
2	Class B SQI (unstable link)
3	Class C SQI (good link)
4	Class D SQI (good link; bit error rate < 1E–10)
5	Class E SQI (good link)
6	Class F SQI (very good link)
7	Class G SQI (very good link)

Note: The Basic status register also provides the REMOTE_FAULT bit (bit #4) according to IEEE. This bit does not need to be checked, as it reflects the same information as REM_RCVR_STATUS. Both bits are latched, therefore they can show different values depending on their readout status.

8.2.3 Interrupt handling

The TJA1100 has a dedicated INT_N pin that signals interrupts to the microcontroller. When any kind of interrupt is pending, and enabled, the INT_N pin goes low.

The interrupt service can be implemented with an external interrupt to the microcontroller through the INT_N pin (active low) or by reading the Interrupt Status Register (SMI address: 0x15) on a regular basis (polling). Please note that the Interrupt Status Bits are always set if an event occurs, but the INT_N pin is only driven low, if the according interrupt has been enabled in the Interrupt Enable Register.

The Interrupt Status Register gives a summary of all possible kinds of interrupts. Please note that reading out the Interrupt Status Register also clears all interrupts status bits. An interrupt is pending when a bit is set in the Interrupt Status Register and the according interrupt enable bit is set in the Interrupt Enable Register. Upon determination of a pending interrupt, the related interrupt handler is called. The interrupt handlers are application specific functions and depend on the need of the application, see Fig 33, Fig 34 and Fig 35.

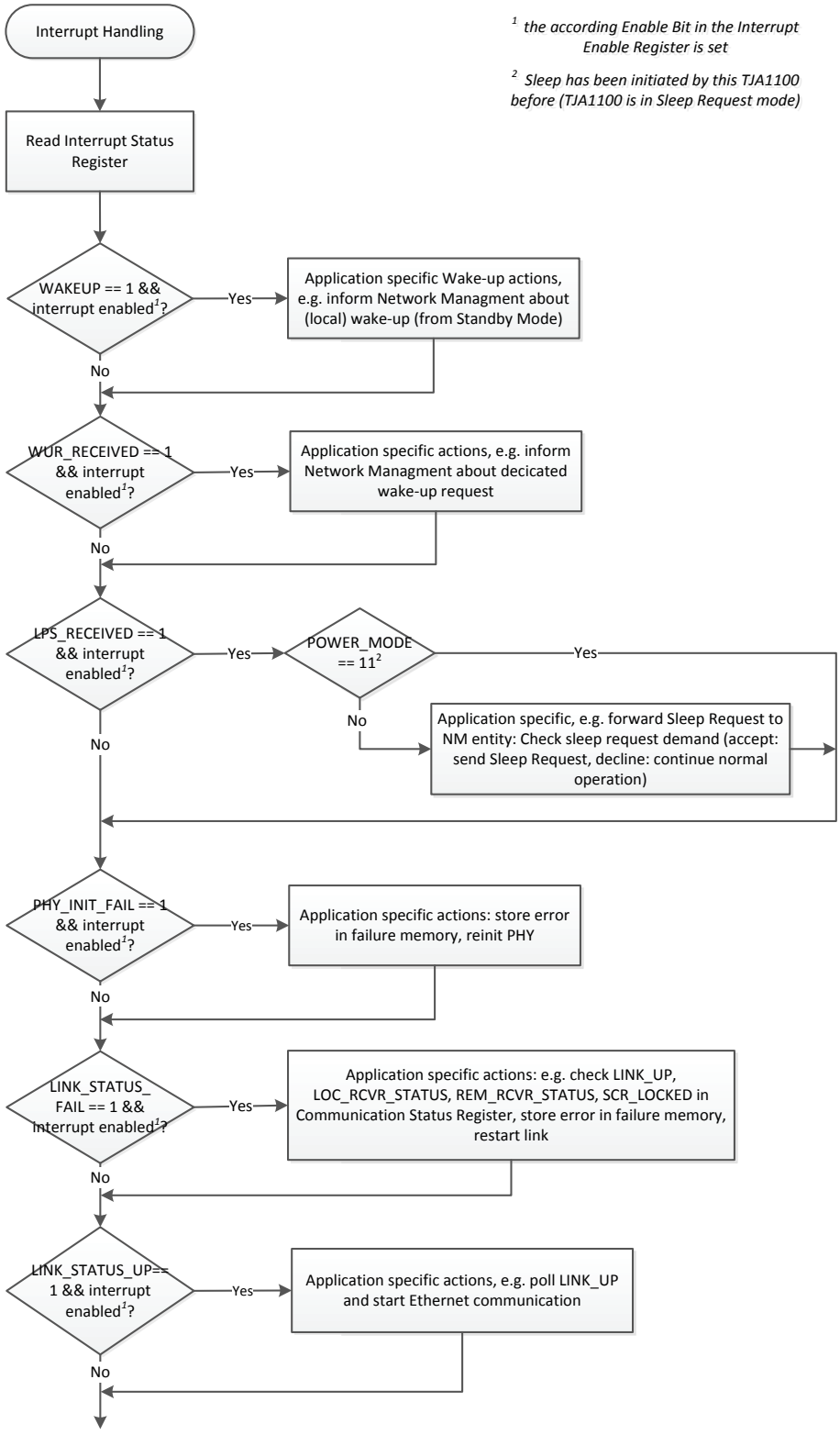


Fig 33. Interrupt Handling (1)

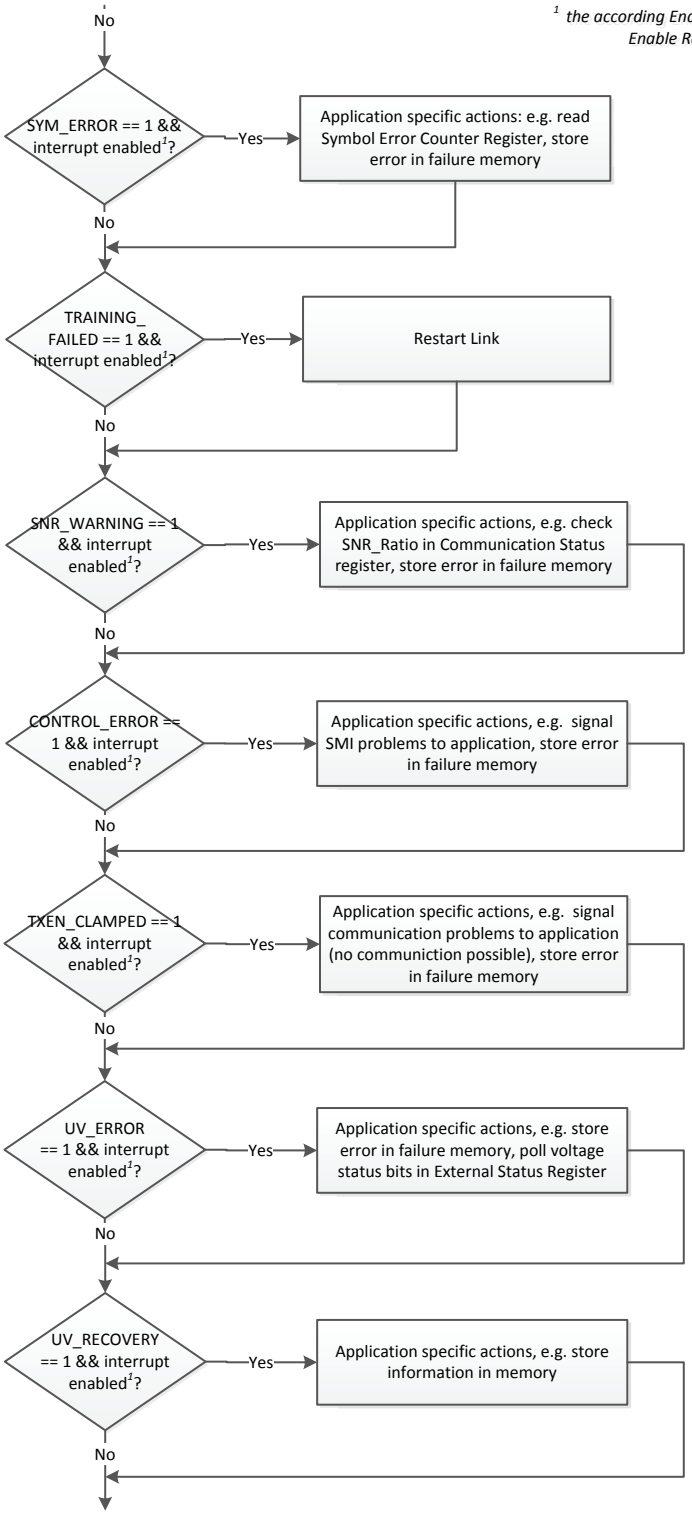


Fig 34. Interrupt Handling (2)

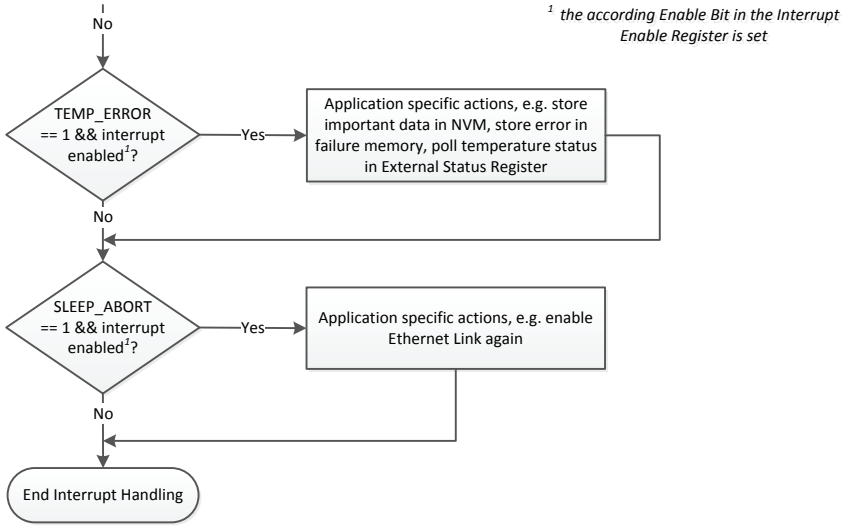


Fig 35. Interrupt Handling (3)

For further information of the Wake-up interrupt handling refer to chapter 8.3.3.

The Interrupt Handler is called whenever an interrupt has occurred in Normal and Standby Mode. As in TJA1100 Standby Mode no link is built, only WAKEUP, CONTROL_ERROR, UV_ERROR, UV_RECOVERY and TEMP_ERROR may occur, while in Normal Mode all interrupts except for WAKEUP are possible.

8.2.4 Run default application

The execution of the application can e.g. include Ethernet packets routing, periodic microcontroller input pin polling, periodic event handling. From TJA1100 perspective it is important to stop the Ethernet communication in case of a failure.

8.2.5 Transition to Low Power operation

Low Power Mode of the PHY is requested by an SMI write access to the Extended Control Register (SMI address: 0x11).

For entering sleep mode, the link should be terminated by both link partners to have silent on the channel. The TJA1100 will enter Sleep Mode after a Sleep Request Command (POWER_MODE set to 0Xb) and Sleep timeout.

To enter Standby Mode (POWER_MODE = 0Xc) only a SMI write access to the Extended Control Register (SMI address: 0x11) is necessary, see 8.3.2.

8.3 Low power operation

This section introduces the software operations, which are associated to Low Power Operation of the application. It is related to the Standby and Sleep Mode of TJA1100. The difference between both modes is the amount of power that can be saved. The Sleep Mode has the lowest current consumption, especially if the microcontroller is

unsupplied, which applies if the microcontroller voltage regulator is controlled by the TJA1100 INH. In Standby Mode the current consumption is higher compared to Sleep mode, as the microcontroller is still powered. In both low power modes the TJA1100 can be woken up either locally by the WAKE pin or remotely by Ethernet Idle pulses on the lines. The following subchapters discuss the Standby and Sleep Mode in more details.

As illustrated in Fig 36, Low Power Operation can be entered from Normal Mode, via SMI commands.

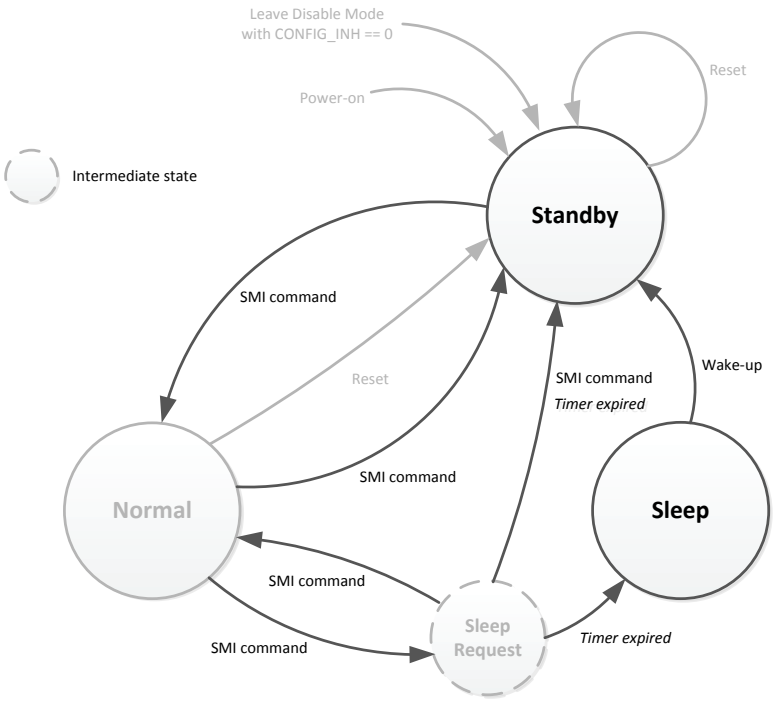


Fig 36. Simplified mode diagram with focus on Low Power Operation

8.3.1 Sleep operation mode

Sleep Mode is a special kind of Low Power Operation. It can be entered from Normal Mode via the Sleep Request command, which is a write access to the Extended Control Register (SMI address: 0x11).

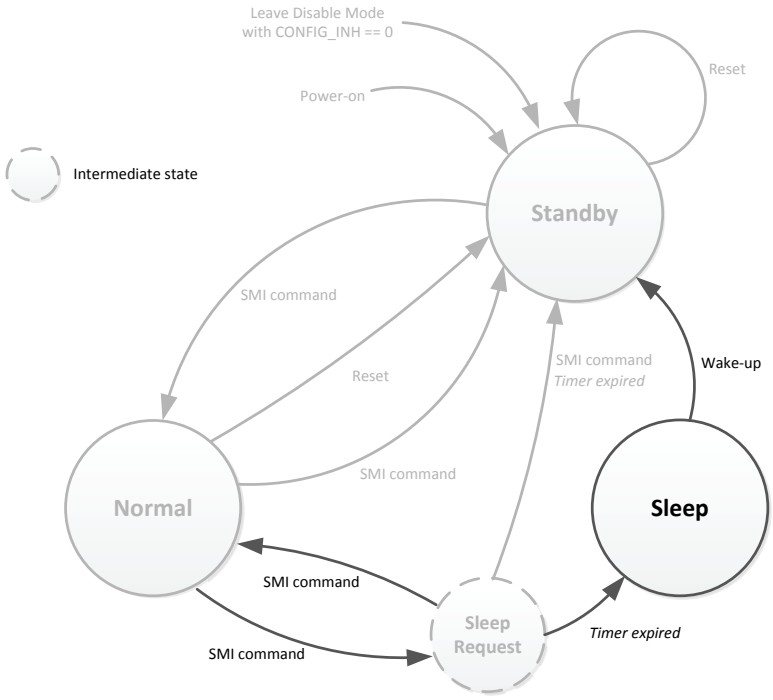


Fig 37. Simplified mode diagram with focus on Low Power Operation (Sleep Mode)

The software flow of the go-to-sleep process is summarized in Fig 38. The first action during Sleep Mode preparation is to check if the TJA1100 is in Normal Mode. If the TJA1100 is in Normal Mode, transmission is stopped and the sleep request command (POWER_MODE = 0Xb) is sent to the TJA1100.

If the TJA1100 receives a Normal Mode Command (POWER_MODE = 0x3) via SMI when the Sleep Request Timer runs, transition to Low Power Sleep Mode is aborted and Normal Mode is entered again.

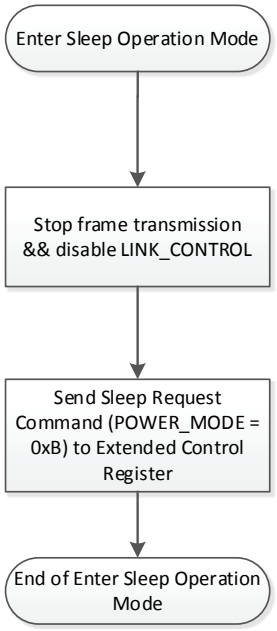


Fig 38. Transition to Sleep Mode software flow

8.3.2 Standby operation mode

A different kind of Low Power Operation is the so-called Stop or Sub Clock operation. This operation is related to the Standby Mode of the TJA1100 because it requires a supplied microcontroller. Stop or Sub Clock operation is a low power feature of the microcontroller itself. A wake-up from Stop/Sub Clock operation will not lead to mode changes of the TJA1100.

The TJA1100 simply enters Standby Mode, if the according SMI write access to the Extended Control Register (POWER_MODE = 0Xc) is sent.

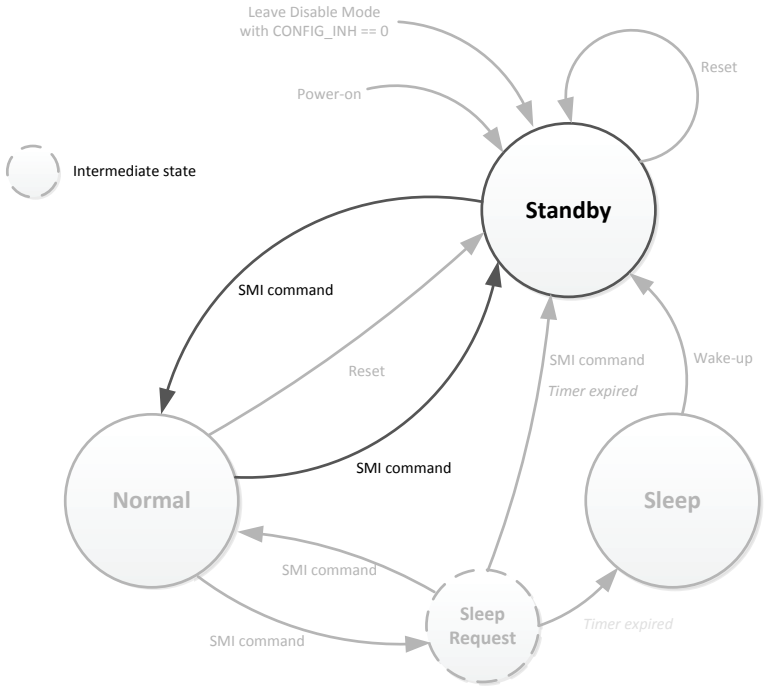


Fig 39. Simplified mode diagram with focus on Low Power Operation (Standby Mode)

In order to save additional power, in TJA1100 Standby Mode the Stop/Sub Clock operation of the microcontroller can be entered by disabling the oscillator completely or switching to a lower clock frequency.

Fig 40 illustrates the required actions before entering Stop Mode. The first part of the Stop Operation is to stop frame transmission (if still enabled) and configure the interrupts/wake-up sources for Standby Mode by a write access to the Interrupt Enable Register. When the interrupts are configured properly, Standby Mode Request can be sent to the TJA1100. Afterwards if no interrupt is pending, the Stop/Sub Clock operation of the microcontroller can be entered by disabling the oscillator completely or switching to a lower clock frequency. Otherwise, an event has occurred and stop mode transition must be aborted.

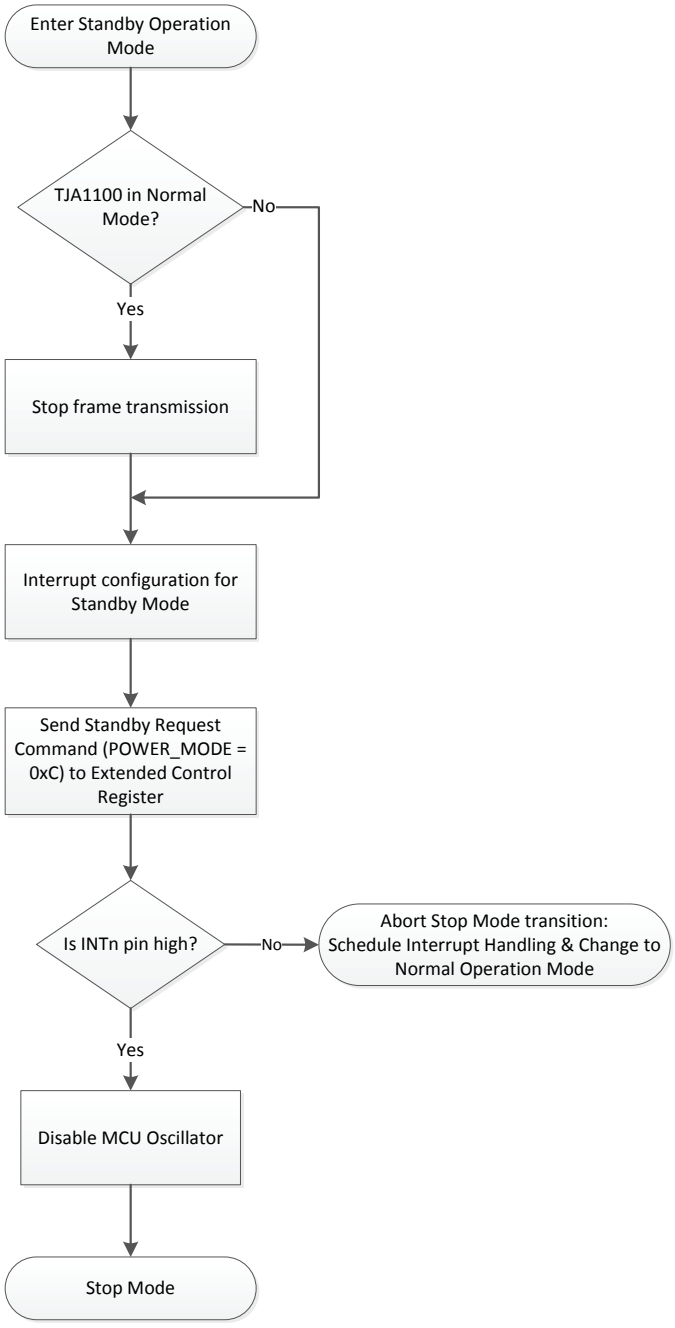


Fig 40. Transition to MCU Stop Mode (TJA1100 Standby Mode) software flow

8.3.3 Wake-Up handling – link wakeup

The procedure for waking up and reactivating a link from Sleep is illustrated in Fig 21. Assume as a starting point that both link partners are in Sleep mode, the microcontroller is switched off and the PHY is configured as remote wake-up detection. When a local or remote wake-up event is detected, the PHY switches to Standby mode automatically and activates the ECU via the INH signal (typically the entire ECU is unpowered in TJA1100 Sleep Mode). Hence, Startup Operation is started. It detects the wake-up source of the PHY and informs the management entity, which can decide whether to reactivate the link or not. For detailed information on the flow during the Startup Operation refer to chapter 8.1.

The procedure for waking up and reactivating a link from Standby Mode is different. When a local or remote wake-up is detected and the according interrupt has been enabled before, the wake-up is signaled to the microcontroller by the INT_N pin and the interrupt handler is started immediately. The interrupt handler detects the wake-up and informs the management entity, which can decide whether to reactivate the link or not. For further information on the interrupt handler refer to chapter 8.2.3.

Fig 41 illustrates Wake-up Handling from software perspective.

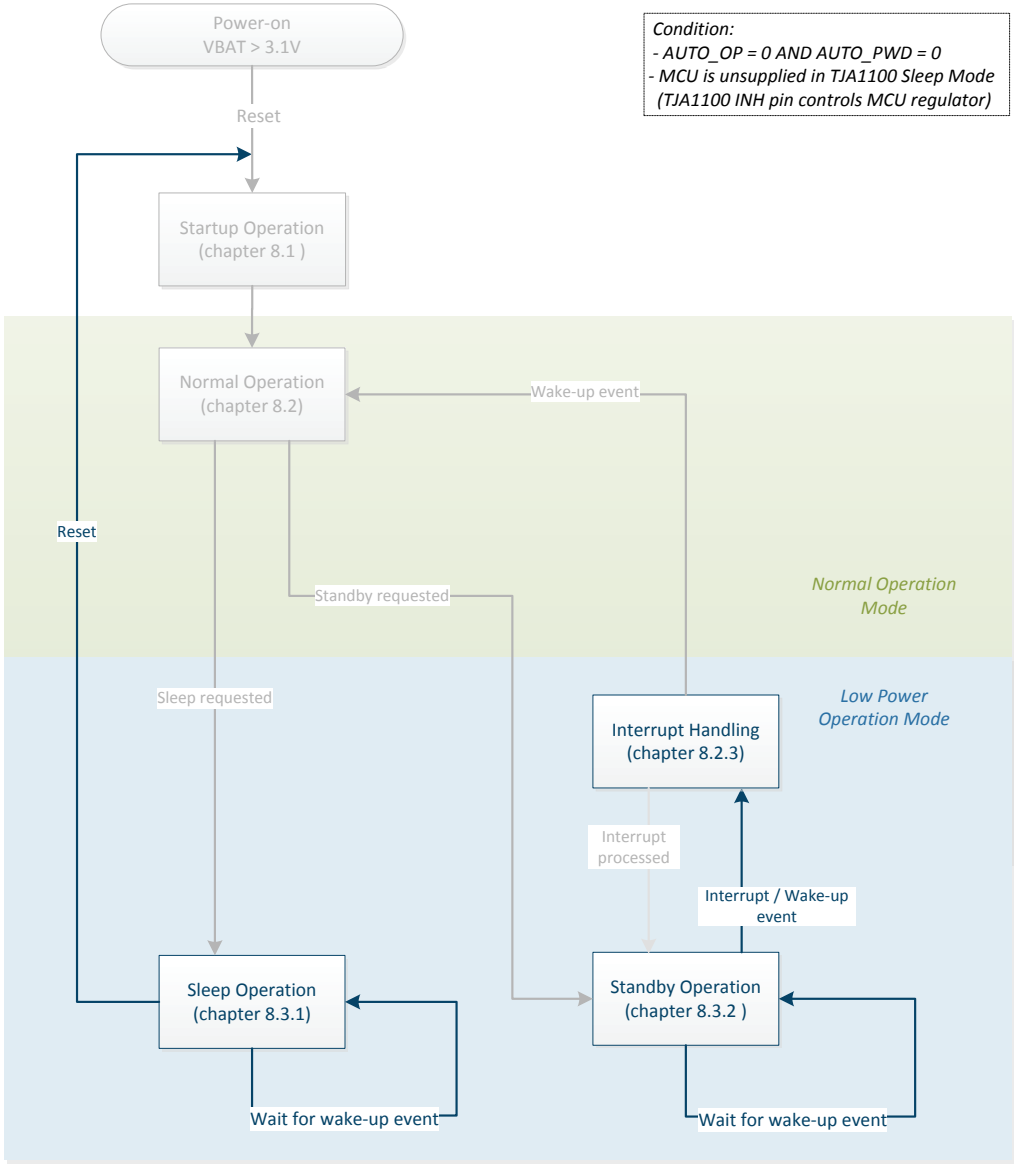


Fig 41. WAKE handling in Sleep and Standby Mode

8.4 Latching function

In the TJA1100 datasheet some register bits marked as LL (Latched LOW) or LH (Latched HIGH), which indicates these bits are implemented with a latching function. It means the occurrence of a fault/event will cause the relevant bit to become clear (LL) or set (LH), and remain clear or set even the fault/event has been disappeared already until this bit is read or a reset. As a consequence, the latched bits need to be read a 2nd time to get the actual status.

Note that latched bits in the Basic Status Register and the Communication Status Register are not latched if link control is disabled (bit LINK_CONTROL = 0).

9. Printed Circuit Board Checklist

No.	Pin-name	Pin-number	TJA1100 Requirements
1	all	all	Check pinning and correct pin numbers. Refer to the datasheet
2	MDC	1	Connect to MDC pin of the µC; A series resistor can be reserved to improve EMC performance but not necessary. Note that the impedance of the series resistor plus the output impedance of the MDC driver shall match the impedance of the PCB trace.
3			If more than one TJA1100 on the same board use the same MDC clock, note that PCB branches and stubs to distribute the MDC clock to multiple TJA1100 shall be as short as possible.
4	INT_N	2	If connected to the µC it needs a pull-up resistor of about 10 kΩ to VDD(IO); the pull-up can be also within the µC; The value of the pull-up resistor should be chosen such that a proper high/low level is ensured.
5			If not used, it can be left open.
6	RST_N	3	RST_N shall be connected to GPIO or port pin of the uC. A pull-up resistor of about 10 kΩ to VDD(IO) possible but not necessary
7	VDDA(1V8)	4	It's recommended to connect one 470 nF ceramic capacitor between this pin and GND. The capacitor should be located close to this pin.
8	XO	5	If 25 MHz external crystal (±100 ppm) is used, it's recommended to use one 15 pF ceramic capacitor connected to XO or any other recommended value provided by the crystal supplier; If this pin is not used it can be left open
9	XI	6	If 25 MHz external crystal (±100 ppm) is used, it's recommended to use one 15 pF ceramic capacitor connected to XI or any other recommended value provided by the crystal supplier. If this pin is not used, it should be shorted to GND to avoid noise input
10			The 25 MHz crystal shall fulfill below requirements: tolerance < 100 ppm (including all influencing effects), max. ESR: 100 Ω, load capacitance: around 10 pF, drive level: < 100 µW.
11			Note that the equivalent load capacitance of the two series capacitors at the XI/XO pin shall be ≤ 8 pF. The max. ESR

			of the capacitor shall be < 60 Ω.
12	VDDA(3V3), VDDA(TX), VDDD(3V3)	7, 11, 14	It is recommended to connect one 470 nF ceramic capacitor between the VDDA(3V3) pin and GND.
13			It is recommended to connect one 100 nF ceramic capacitor between the VDDA(TX) pin and GND.
14			It is recommended to connect one 100 nF ceramic capacitor between the VDDD(3V3) pin and GND.
15			A series ferrite bead (600 Ω ± 25 % @ 100 MHz) is recommended, and the assembly depends on the EMC results. At least the footprint of the ferrite bead should be reserved.
16			The capacitor should be located close to the pin.
17			It is recommended to implement short loop between these pins and GND.
18			The voltage regulator output should be sufficiently buffered (e.g. 22 µF)
19	LED/WAKE	8	If used as a LED output (open-drain output), a series current limiting resistor to 3.3 V is needed.
20			If used as a WAKE input, note that only a falling edge can trigger a local wake up.
21			If not used the pin shall be left open or shorted to GND via a series resistor and pin shall not be configured as LED output.
22	VBAT	9	This pin can be connected to battery supply via a reverse polarity protection diode in case the wake-up function or wake up source is needed.
23			This pin can be connected to 3.3 V power supply instead of battery supply in case the wake-up function is not needed
24			It is recommended to use a ceramic capacitor of 100 nF as noise filter. The capacitor shall have a voltage robustness of 50 V if this pin is connected to battery supply.
25			One 1 nF paralleled ceramic capacitor is optional to improve the EMC performance.
26	INH	10	Note that the max. voltage drop of this pin is 1 V in case the output current is 1 mA. Double check load on INH pin.
27			If not used the pin shall be left open.
28	TRX_P,	12,13	The recommended circuit (default filter) can be found in the

	TRX_M		datasheet. Note that the tolerance of the series 100 nF capacitor shall be within 10 % with max rating ≥ 50 V.
29			It's recommended to use a PESD2ETH diode for higher robustness also in case of independent power supplies of the link partners (e.g. mains adapters) or a short of the bus lines to voltages higher 5 V. The supply terminal of the diode should be connected to VDDA(TX). The layout for the diode should be symmetrically.
30			It's recommended to connect a split termination consisting of two resistors and a capacitor to the signal lines between the DC blocking capacitors and the connector. For symmetry reasons the tolerance of the two resistors shall be within ±1 %. The power rating of the resistors should be higher than 0.4 W, depending on expected RF power in the actual application.
31			The PCB tracks should be routed close together in a symmetrical way.
32			The recommended impedance of the PCB trace is 100 Ω.
33	GND	15, 20, 26	The GND pins shall be soldered to board GND with short trace.
34	VDDD(1V8)	16	It is recommended to connect one 10 nF (optional) and one 470 nF ceramic capacitor between this pin and GND.
35	RXER/ CONFIG3	17	MII/RMII mode: connect to the RXER pin of the MAC; 20 Ω series resistor can be considered to improve EMC performance. If not used, it should be left open.
36	RXDV/ CONFIG2/ CRSDV	18	MII mode: connect to the RXDV pin of the MAC; RMII mode: connect to the CRSDV pin of the MAC; 20 Ω series resistor can be considered to improve EMC performance
37	VDD(IO)	19, 27	It is recommended to connect one 100 nF ceramic capacitor between this pin and GND. The capacitor should be located close to this pin.
38			It's recommended to add a 4.7 nF capacitor and 3.9 Ω resistor to form a low-pass filter or add a series ferrite bead as a filter. NXP only evaluated the ferrite bead BLM18AG601SN1. Any other type can be taken according to the EMC measurement on ECU level.
39			The power supply of the VDDA(3V3) and VDD(IO) pin should be connected to make sure these pins are powered

			at the same time.
40	RXD3/ CONFIG1, RXD2/ CONFIG0	21,22	MII mode: connect to the RXD3/RXD2 pin of the MAC; 20 Ω series resistor can be considered to improve EMC performance; RMII mode: can be left open
41	RXD1/ PHYAD1, RXD0/ PHYAD0	23, 24	MII/RMII mode: connect to the RXD1/RXD0 pin of the MAC; 20 Ω series resistor can be considered to improve EMC performance.
42	RXC/ REF_CLK	25	MII mode: connect to the RXC pin of the MAC; RMII mode: connect to the REF_CLK pin of the MAC; A series resistor can be considered to improve EMC performance in MII mode and RMII mode without external clock; Note that the impedance of the series resistor plus the output impedance of the clock driver shall match the impedance of the PCB trace. A 50 MHz external oscillator (±50 ppm) can be connected to this pin if configured as RMII mode with external clock.
43	TXC	28	MII mode: connect to the TXC pin of the MAC; A series resistor can be considered to improve EMC performance; Note that the impedance of the series resistor plus the output impedance of the clock driver shall match the impedance of the PCB trace. RMII mode: can be left open
44	TXEN	29	Connect to the TXEN pin of the MAC; 20 Ω series resistor can be considered to improve EMC performance.
45	TXD3, TXD2	30, 31	MII mode: connect to the TXD3/TXD2 pin of the MAC; 20 Ω series resistor can be considered to improve EMC performance; RMII mode: can be left open
46	TXD1, TXD0	32, 33	MII/RMII mode: connect to the TXD1/TXD0 pin of the MAC; 20 Ω series resistor can be considered to improve EMC performance.
47	TXER	34	MII mode: connect to the TXER pin of the MAC; If not used, it shall be connected to GND.
48			For the RXD0/1/2/3 and TXD0/1/2/3 pin, the trace length between PHY and MAC shall be kept short to ensure a capacitive load of less than 15 pF. The PCB trace impedance should be at least 50 Ω with a line delay of less than 1 ns.

49	EN	35	This pin is typically connected to a GPIO pin of a uC or permanently connected to VDD(IO). A series jumper shall be considered since this pin will be reconfigured as output and signals the TX_TCLK clock signal in test mode.
50	MDIO	36	Connect to MDIO pin of µC with a pull-up resistor of about 10 kΩ to VDD(IO) , the pull-up can be also within the µC. Make sure the 10 kΩ pull-up resistor is available only once at the same MDIO bus.
51	CONFIG3, CONFIG2, CONFIG1, CONFIG0, PHYAD1, PHYAD0	17, 18, 21, 22, 23, 24	If pin strapping is used, the pull-up/down resistors shall have a value of around 5 kΩ to 20 kΩ. Make sure the input voltage < 0.8 V (Low) or > 2.0 V (High).
52	exposed die pad		The exposed die pad shall be soldered to GND.

10. Abbreviations

ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
HBM	Human Body Model
IEC	International Electrotechnical Commission
INH	Inhibit
MAC	Medium Access Controller
MDI	Medium Dependent Interface
MII	Medium Independent Interface
OABR	OPEN Alliance BroadR-Reach
PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PMA	Physical Medium Attachment
RMII	Reduced Medium Independent Interface
SMI	Serial Management Interface
SPI	Serial Peripheral Interface
WU	Wake-up
WUP	Wake-up Pattern

11. References

[1] 100BASE-T1 Specification, IEEE Std 802.3bw™-2015

[2] OPEN Alliance, EMC Test Specification for BroadR-Reach™ Common Mode Chokes, Version 2.0, December 19, 2014, FTZ Zwickau

[3] OPEN Alliance, EMC Test Specification for BroadR-Reach™ Transceivers, Version 2.0, December 19, 2014, FTZ Zwickau

[4] OPEN Alliance, Automotive Ethernet ECU Test Specification, Version 1.0, January 15, 2016, OPEN Alliance

[5] TJA1100 – 100Base-T1 PHY for Automotive Ethernet, Product data sheet, Rev. 2.30 – 2017, NXP Semiconductors

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