DEVKIT-MPC5748G

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Caution:

These schematics are provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

Revision Information

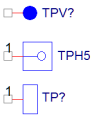
Rev	Date	Designer	Comments
X1	23 Sep 2015	Catalin Neacsu	Initial release
X2	24 Sep 2015	Catalin Neacsu	Further changes. Decreased component size where possible.
X3	29 Sep 2015	Catalin Neacsu	Changed ethernet page. Changed caps around Q50 Rearranged GPIOs on page 15. Added more LEDs on page 14
X4	02 Oct 2015	Catalin Neacsu	Changed U50, USB connectors, ETH Connector, BOM optimization
X5	05 Oct 2015	Catalin Neacsu	Changed PN of U11 and C23
X6	07 Oct 2015	Catalin Neacsu	Small visual updates
X7	08 Oct 2015	Catalin Neacsu	Add separation resistors for USB interface, U50
X8	12 Oct 2015	Catalin Neacsu	Changed 3V3 converter, minor BOM optimization
X9	14 Oct 2015	Catalin Neacsu	Changed 3V3 converter, minor BOM optimization, better cost
X10	21 Oct 2015	Catalin Neacsu	Updated IO connections per Jesus Sanchez's request Added TP on page 3 per Ruiz Ricardo's request
X11	27 Oct 2015	Catalin Neacsu	Changed Power Supply page Added one user led
X12	28 Oct 2015	Catalin Neacsu	Changed PN for P2 and P7
X13	30 Oct 2015	Catalin Neacsu	Changed Power Supply page to allow supply selection
X14	02 Nov 2015	Catalin Neacsu	BOM Optimization
X15	03 Nov 2015	Catalin Neacsu	PN change for L1
X16	23 Dec 2015	Catalin Neacsu	Added Open SDA block Implemented other feedback
X17	06 Jan 2016	Catalin Neacsu	Implemented OpenSDA feedback
X18	08 Jan 2016	Catalin Neacsu	Changed some ICs to their NXP equivalent
X19	15 Jan 2016	Catalin Neacsu	P12, Y50 add GND connections. JTAG connector 14 pins
A	26 Jan 2016	Catalin Neacsu	Protoype Release
A1	13 Jun 2016	Jun Qiao	Update with Flexray, OpenSDA, Ethernet, LED, Buttons, GPIO.
A2	20 Jun 2016	Jun Qiao	Update with OpenSDA, GPIO connectors.
B	24 Jun 2016	Jun Qiao	Pilot Release

3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hile Pad Large (for standard 0.1" header).
Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop



Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
  2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

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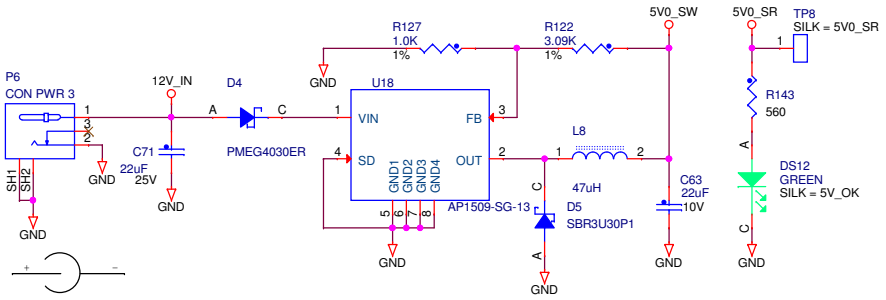
Designer: C Neacsu	Drawing Title: DEVKIT-MPC5748G	
Drawn by: C Neacsu	Page Title: Index and Title Page	
Approved: Pesses Philip	Size B	Document Number SCH-29030 PDF: SPF-29030 Rev B
	Date: Thursday, July 21, 2016	Sheet 1 of 15

Power Input and Voltage Regulators

12V Power Supply Input

5V Switching Regulator

Input Voltage 12V, Output 5V at 1800mA

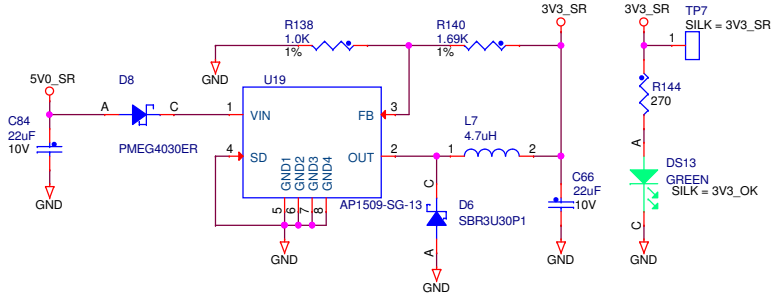


LAYOUT NOTE:
ADD Graphical silk:

Layout note: follow IC datasheet recommandations for PCB layout and thermal dissipation

3.3V Switching Regulator

Input Voltage 5V, Output 3.3V at 1600mA

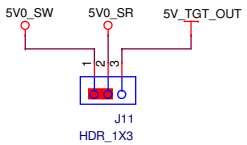


Layout note: follow IC datasheet recommandations for PCB layout and thermal dissipation

Board supply selection

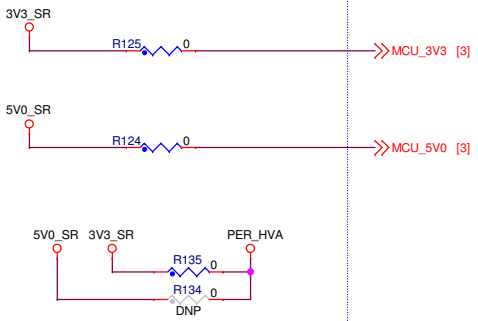
Select between USB and external 12V

1-2 -> external 12V
2-3 -> USB/UART connector

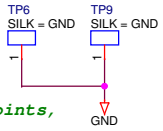


Power Control

Jumpers can be fitted to facilitate power measurements



Test and reference points



GND Test Points, Top Side

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Calypso MCU Power Connections

Power Supply Contraints:

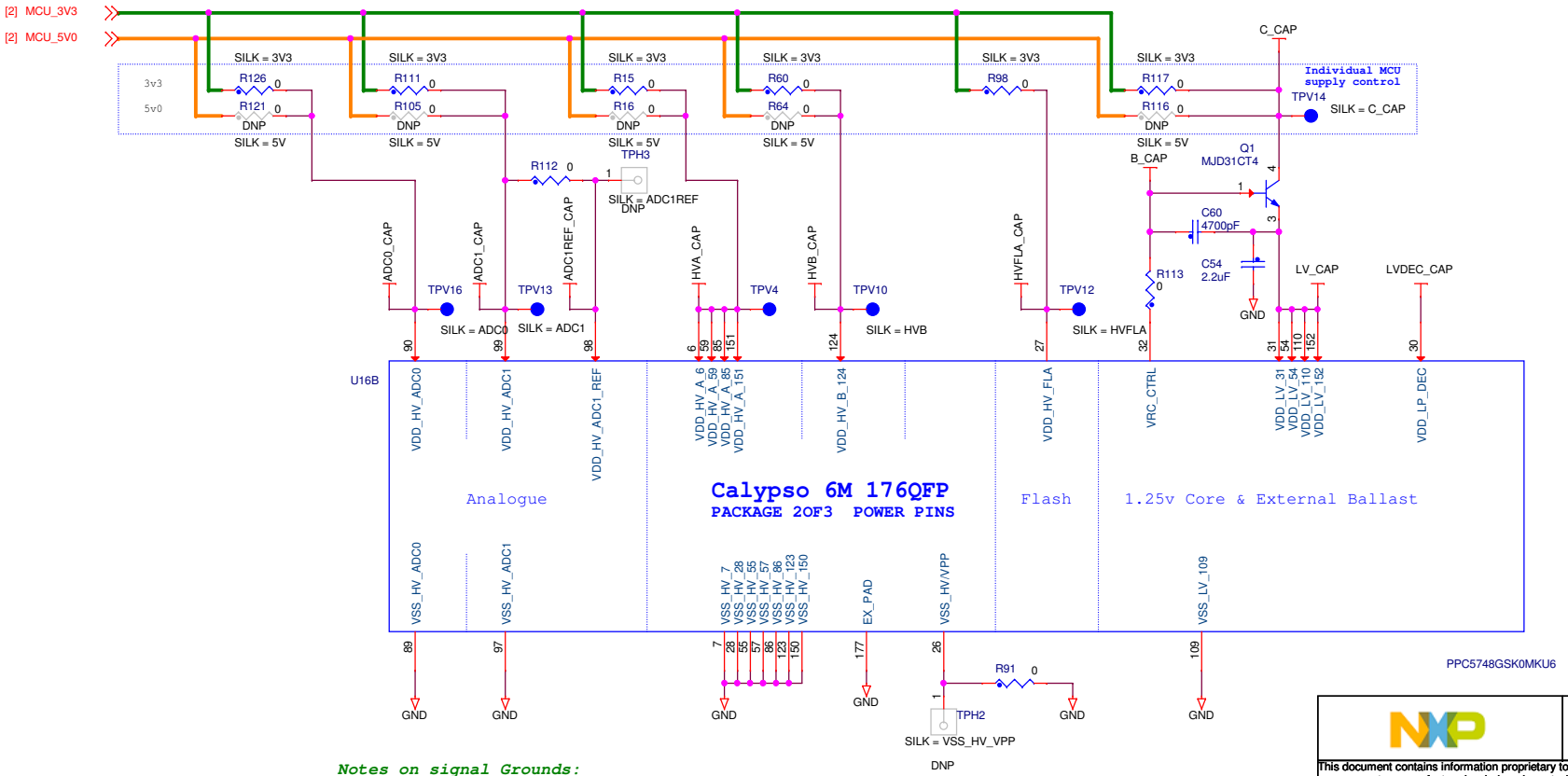
- If VDD_HV_A is driven from 3.3V, VDD_HV_FLA must also be supplied from 3.3V
- If VDD_HV_A is driven from 5V, the VDD_HV_FLA pin must be disconnected from 3.3V

- Don't attempt to over drive an analogue pad to 5V when the digital VDD_HV_x supply is set to 3.3V. This will trigger the ESD protection on that pad. For example if VDD_HV_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD_HV_A domain

Default Configuration:

- ALL MCU supply voltages are set to 3.3V (ADC0, ADC1, VDD_HV_A, VDD_HV_B, VDD_HV_C, VBallast)
- VDD_HV_FLA = External 3.3V supplied (jumper fitted)

The analogue pins can only be driven to the same voltage as the VDD_HV_x domain they are situated in (ie max 3.3V) so makes sense for the analogue supply and reference to be 3.3V



Notes on signal Grounds:

- The scheme shown has the analogue and digital grounds connected to the same plane
- This results in better ADC performance than using an analogue grond plane with single entry point (or ferrite) to digital ground plane.

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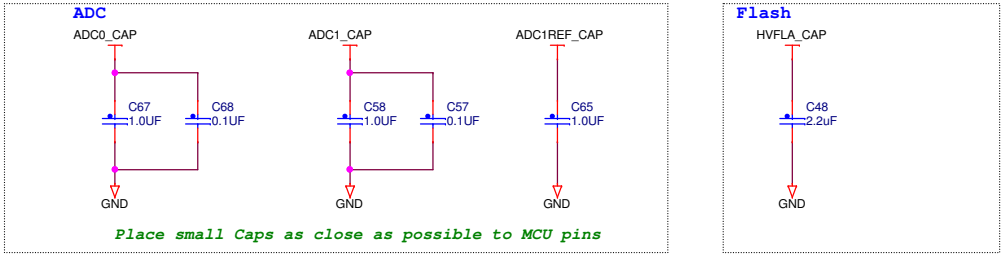
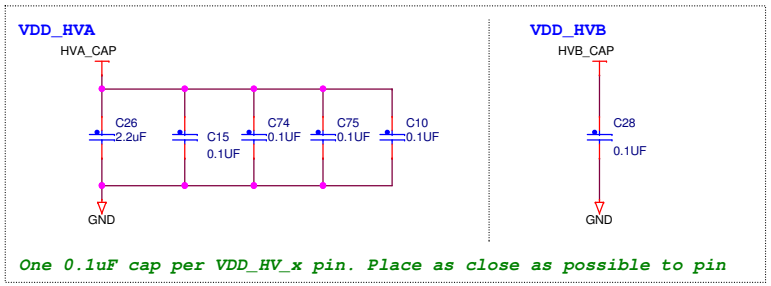
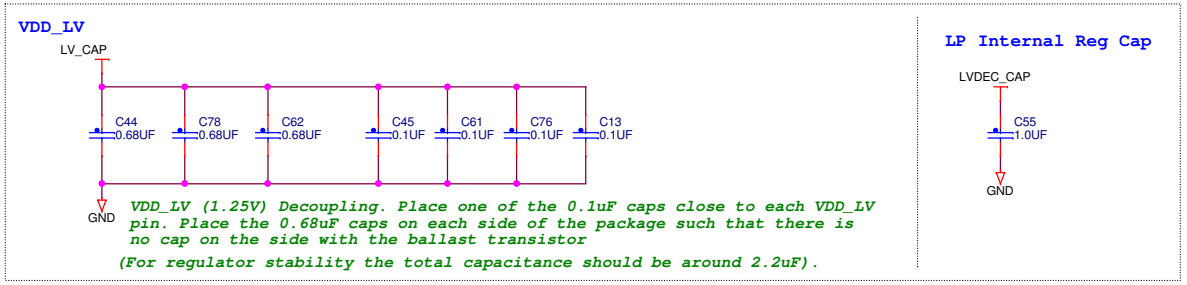
Approved:	Size	Document Number SCH-29030 PDF: SPF-29030	Rev B
	Date: Thursday, July 21, 2016	Sheet 3 of 15	

Calypso MCU Decoupling and bulk storage







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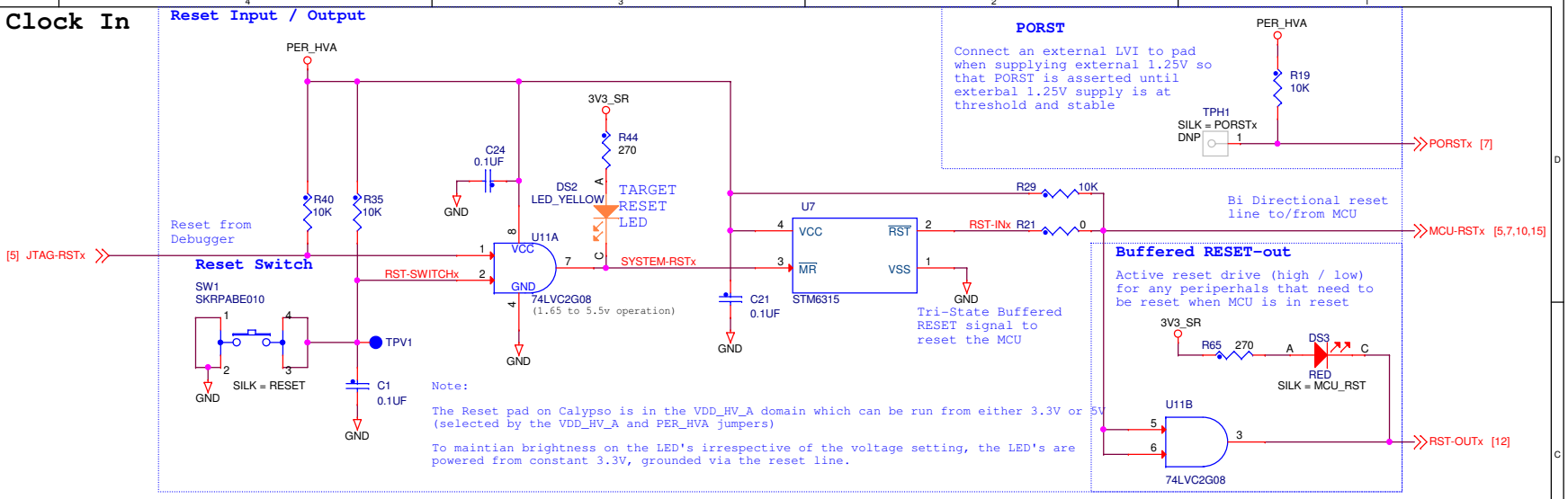
Reset and External Clock In

Reset is in the VDD_HVA domain.



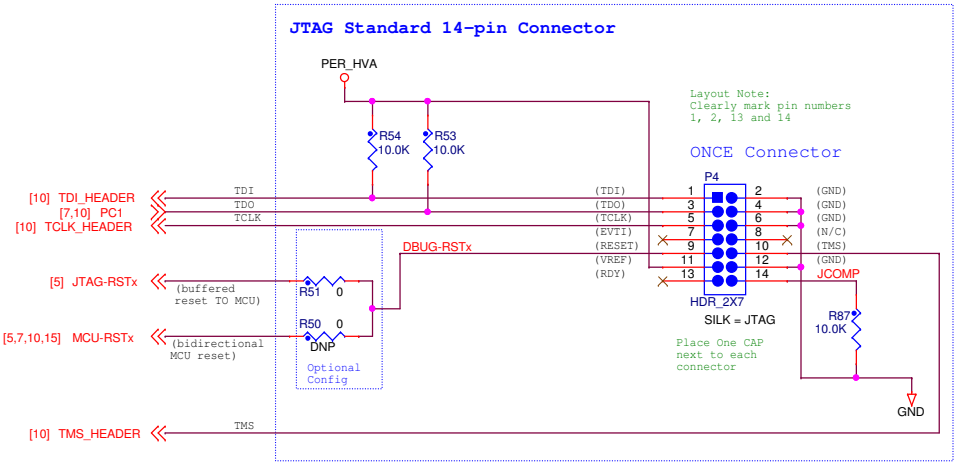


Table 13-3. Functional terminal state during power-up and reset

TERMINAL TYPE[1]	POWERUP pad state[2]	RESET pad state	DEFAULT pad state[3]	Comments
RESET	strong pull-down	strong pull-down	weak pull-up	functional reset pad.
PORST[4]	Weak pull down	Weak pull up	weak pull-up	power on reset pad.
GPIO	high impedance	high impedance	high impedance	by default, but configurable for STANDBY exit
ANALOG	high impedance	high impedance	high impedance	-
EOUT0, EOUT1	high impedance	high impedance	high impedance	
TCK	high impedance	weak pull-up	weak pull-up	-
TMS	high impedance	weak pull-up	weak pull-up	-
TDI	high impedance	weak pull-up	weak pull-up	-
TDO	high impedance	high impedance	high impedance	-
TCK_ALT	high impedance	weak pull-up	weak pull-up	-
TMS_ALT	high impedance	weak pull-up	weak pull-up	-
TDI_ALT	high impedance	weak pull-up	weak pull-up	-
TDO_ALT	high impedance	high impedance	high impedance	-

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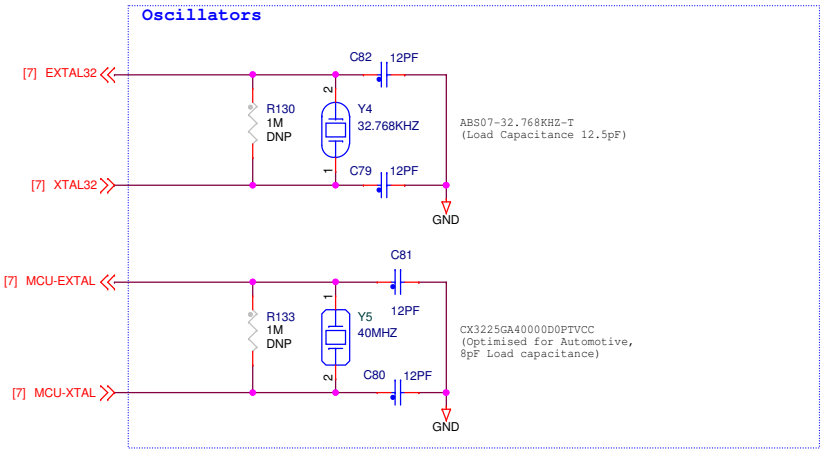
Clocks



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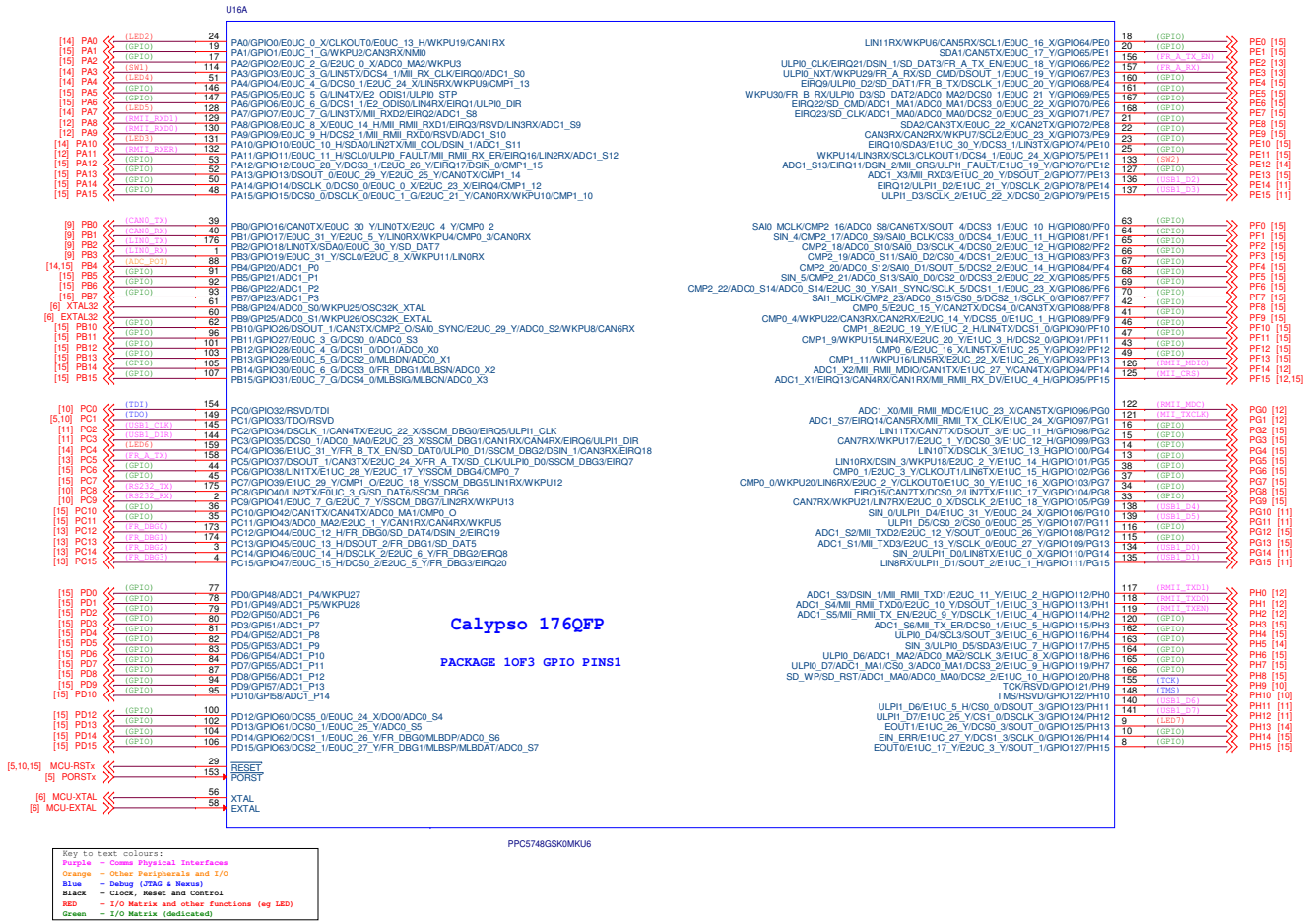
Calypso GPIO 1 of 2



Key to text colours:

- Purple – Comms Physical Interfaces
- Orange – Other Peripherals and I/O
- Blue – Debug (JTAG & Nexus)
- Black – Clock, Reset and Control
- RED – I/O Matrix and other functions (eg LED)
- Green – I/O Matrix (dedicated)

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Calypso GPIO 2 of 2

Key to text colours:
Purple – Comms Physical Interfaces
Orange – Other Peripherals and I/O
Blue – Debug (JTAG & Nexus)
Black – Clock, Reset and Control
RED – I/O Matrix and other functions (eg LED)
Green – I/O Matrix (dedicated)

U16C

Calypso 176QFP

PACKAGE 3OF3 GPIO PINS2

[15] PI0	(GPIO)	PI0	172	PI0/GPIO128/E0UC_28_Y/LIN8TX/SDA1/SD_DAT3
[15] PI1	(GPIO)	PI1	171	PI1/GPIO129/E0UC_29_Y/SCL1/SD_DAT2/WKPU24/LIN8RX
[15] PI2	(GPIO)	PI2	170	PI2/GPIO130/E0UC_30_Y/LIN9TX/SDA2/SD_DAT1
[15] PI3	(GPIO)	PI3	169	PI3/GPIO131/E0UC_31_Y/SCL2/SD_DAT0/WKPU23/LIN9RX
[11] PI4	(USB1_STP)	PI4	143	PI4/GPIO132/E1UC_28_Y/SOUT_0/ULPI1_STP
[11] PI5	(USB1_NXT)	PI5	142	PI5/GPIO133/E1UC_29_Y/SCLK_0/CS2_1/CS2_2/ULPI1_NXT
[15] PI6	(GPIO)	PI6	11	PI6/GPIO134/E1UC_30_Y/CS0_0/CS0_1/CS0_2
[11,15] PI7	(USB1_RST)	PI7	12	PI7/GPIO135/E1UC_31_Y/CS1_0/CS1_1/CS1_2
[15] PI8	(GPIO)	PI8	108	PI8/GPIO136/E2UC_15_Y/MLBCP/MLBCLK/ADC0_S16
[12,15] PI11	(ENET_RST)	PI11	111	PI11/GPIO139/E2UC_14_Y/ADC0_S19/DSIN_3
[15] PI12	(GPIO)	PI12	112	PI12/GPIO140/DCS0_3/DCS0_2/ADC0_S20
[15] PI13	(GPIO)	PI13	113	PI13/GPIO141/DCS1_3/DCS1_2/ADC0_S21
[15] PI14	(GPIO)	PI14	76	PI14/GPIO142/SAI2_D0/E0_ODIS0/E1_ODIS0/ADC0_S22/SIN_0
[15] PI15	(GPIO)	PI15	75	PI15/GPIO143/CS0_0/DCS2_2/E0_ODIS1/E1_ODIS1/ADC0_S23/SAI2_MCLK
	(GPIO)		74	
[15] PJ0	(GPIO)		73	PJ0/GPIO144/CS1_0/DCS3_2/SAI2_SYNC/E2UC_19_Y/E0_ODIS2/E1_ODIS2/ADC0_S24
[15] PJ1	(GPIO)		72	PJ1/GPIO145/SOUT_0/SAI2_BCLK/E0_ODIS3/E1_ODIS3/ADC0_S25/SIN_1
[15] PJ2	(GPIO)		71	PJ2/GPIO146/CS0_1/CS0_2/CS0_3/SAI1_D0/ADC0_S26
[15] PJ3	(GPIO)			PJ3/GPIO147/CS1_1/CS1_2/CS1_3/SAI1_BCLK/ADC0_S27
[14] PJ4	(LED1)		5	PJ4/GPIO148/SCLK_1/E1UC_18_Y/E2UC_4_Y

PPC5748GSK0MKU6

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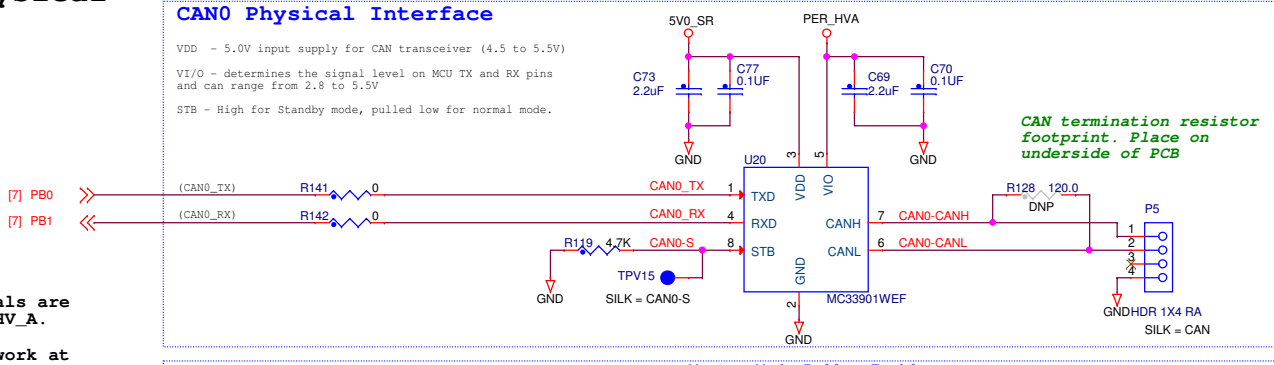
CAN & LIN Physical

CAN0 Physical Interface

VDD – 5.0V input supply for CAN transceiver (4.5 to 5.5V)

VI/O – determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V

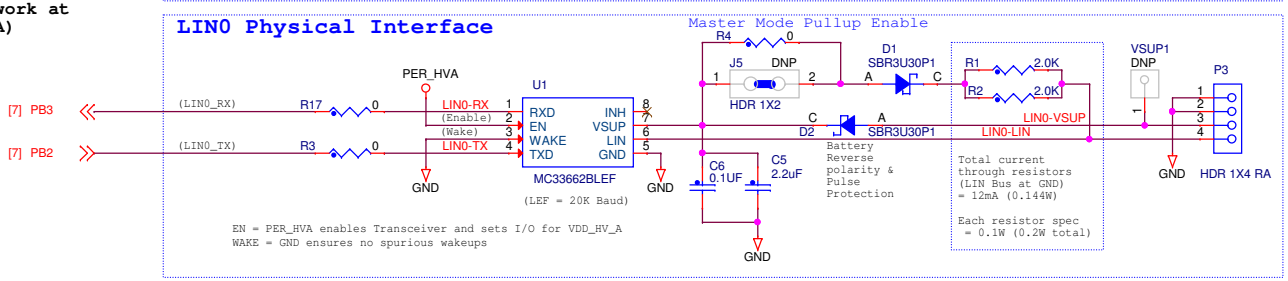
STB – High for Standby mode, pulled low for normal mode.



All CAN and LIN signals are in power domain VDD_HV_A.

All interfaces will work at 3.3V or 5.0V (PER_HVA)

LIN0 Physical Interface



MC33662LEF LIN transceiver is newer version of 33661 offering:

- Full LIN compliance (33661 no longer compliant)
- Improved ESD protection on LIN pin up to 15KV
- Improved ESD on Wake and VSUP Pins
- Other EMC and performance improvements

See freescale.com for more details

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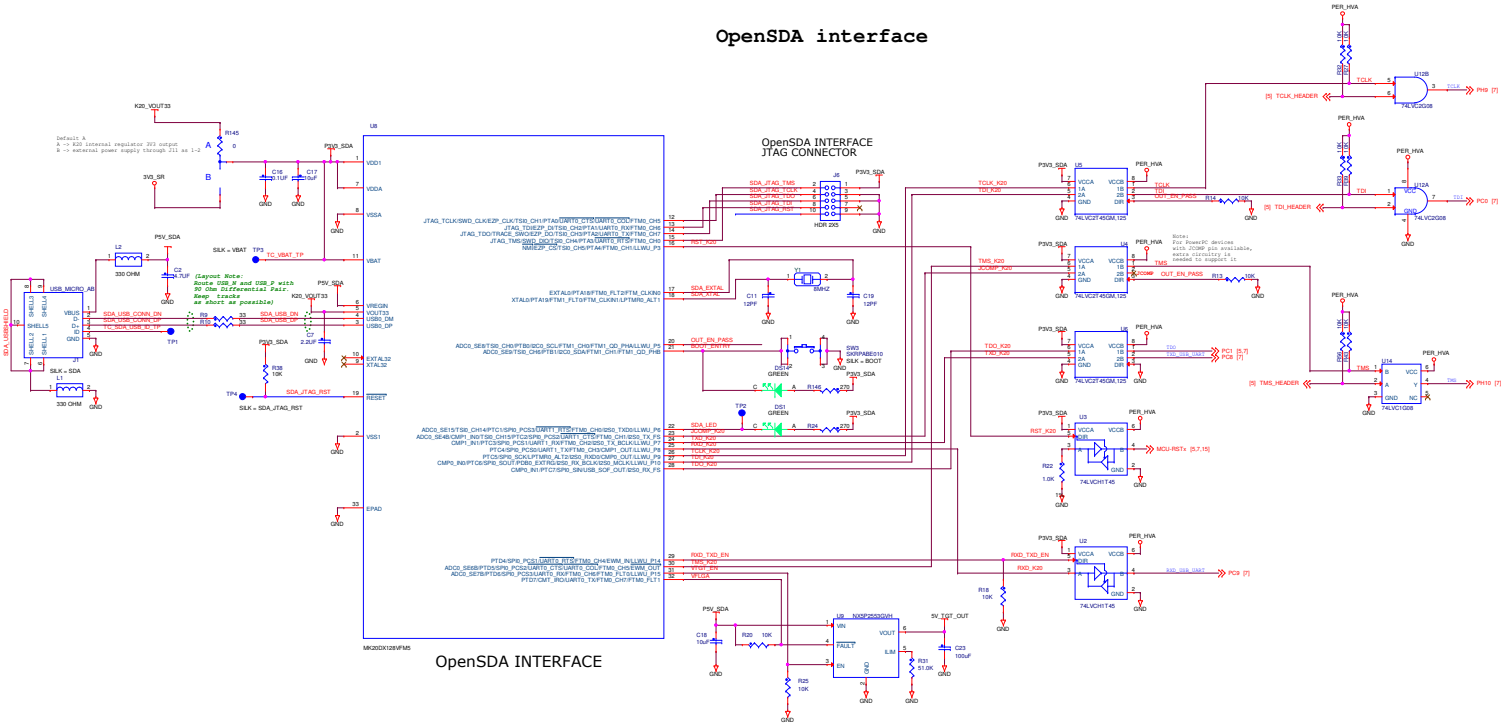
OpenSDA interface



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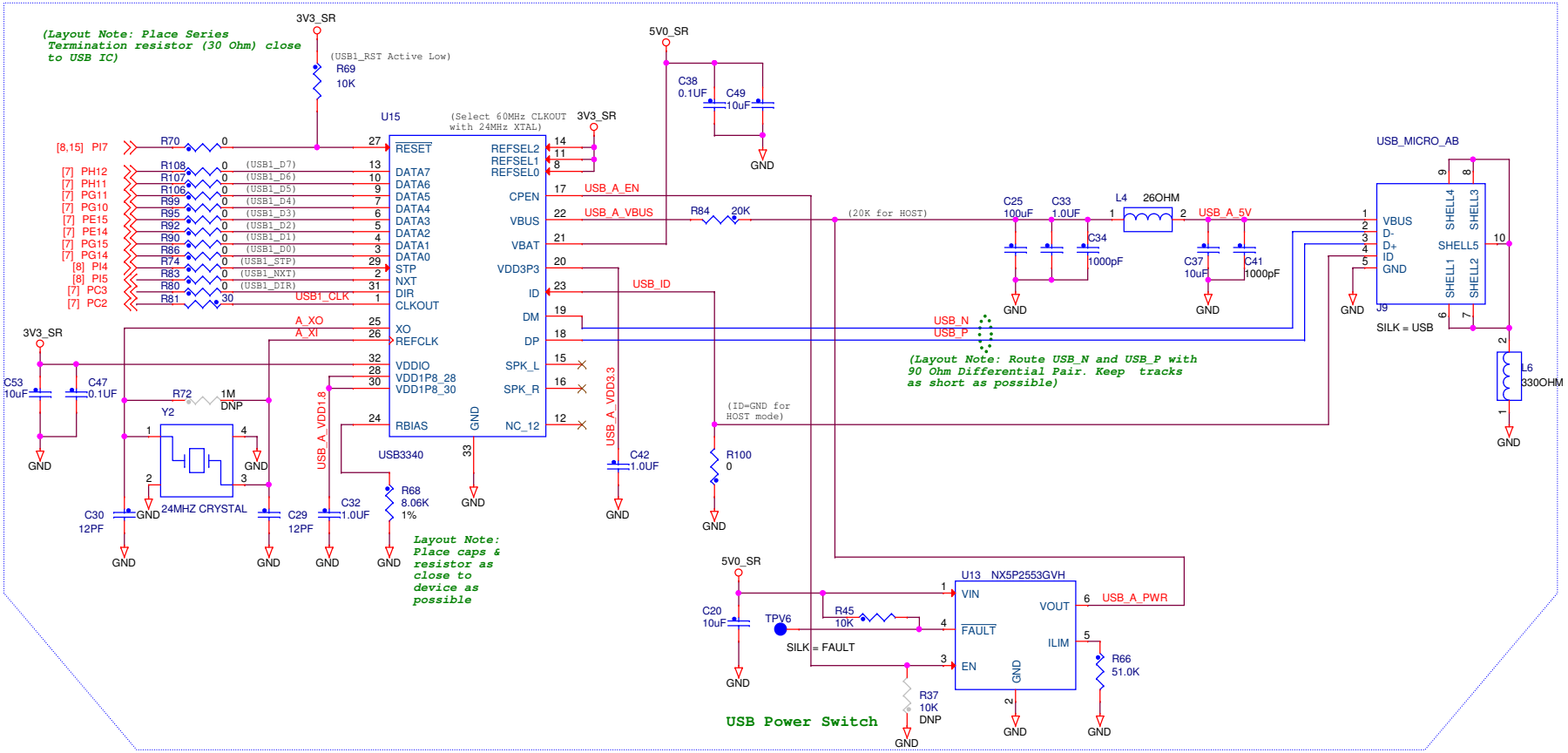
USB (Type A Host and Type AB OTG)

USB Signals are in power domain VDD_HV_A

The USB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, USB MCU pads must be left as tri-state with no pullups or series resistors to be removed



General Layout Note. Recommendation is to keep all tracks between MCU and USB PHI less than 3"

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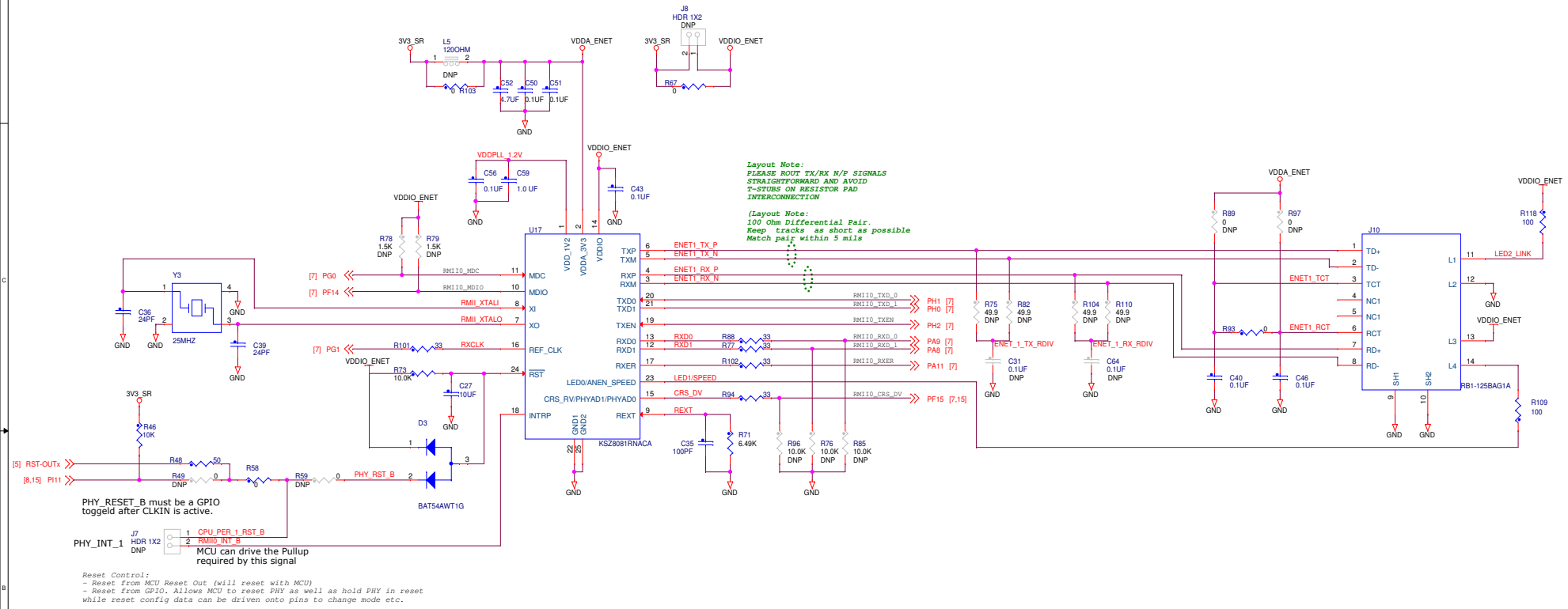
Ethernet Physical Interface



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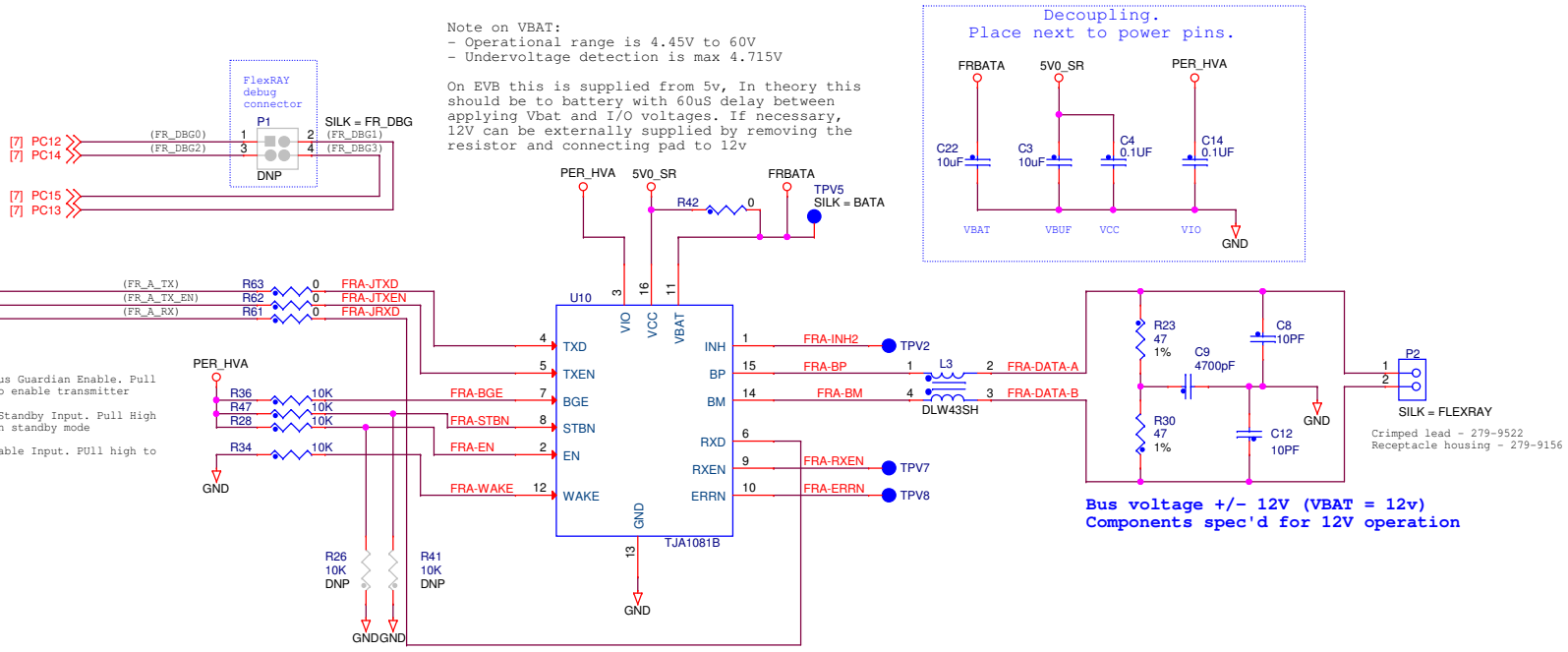
FlexRAY Physical Interface

All Signals are in power domain VDD_HV_A.

FlexRAY interface will work at 3.3V or 5.0V (PER_HVA)



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ICAP Classification: CP: IUO: PUBI: X

Designer:	Drawing Title: **DEVKIT-MPC5748G**		
Brawn by:	Page Title: **FlexRAY Physical Interface**		
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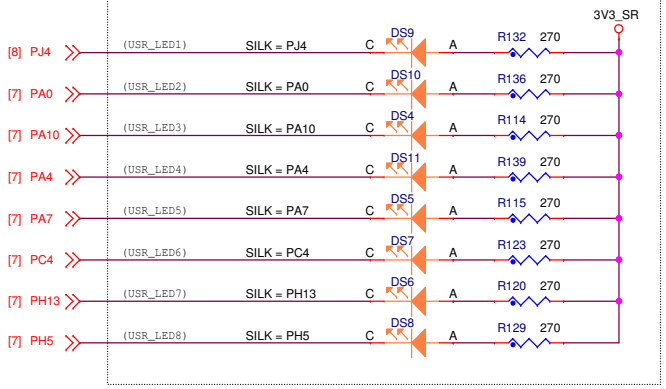
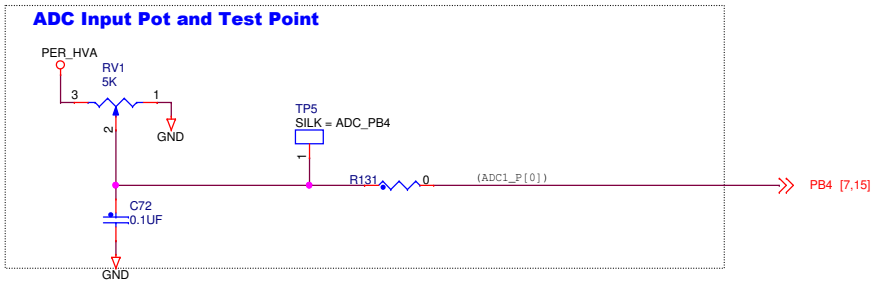
User Peripherals (Led's, Switches and ADC Pot)

Switches are hard wired to 3.3V rather than 5V so it's not possible to drive 5V into a 3.3V pad (which would cause damage)
Similarly, the LED's are active low with 3.3v supply so can be safely coupled to pads on either 3.3V or 5V domains
The ADC input is limited to 3.3V, again to prevent driving 5V into a 3.3V pad which would cause damage

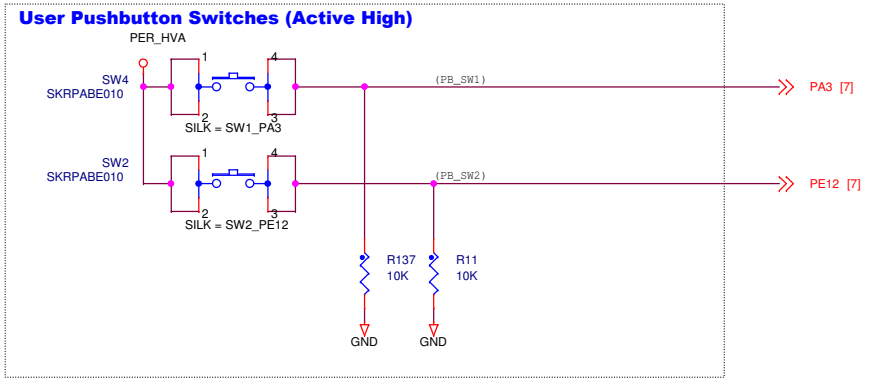
User LED's (Active Low)



ADC Input Pot and Test Point



User Pushbutton Switches (Active High)



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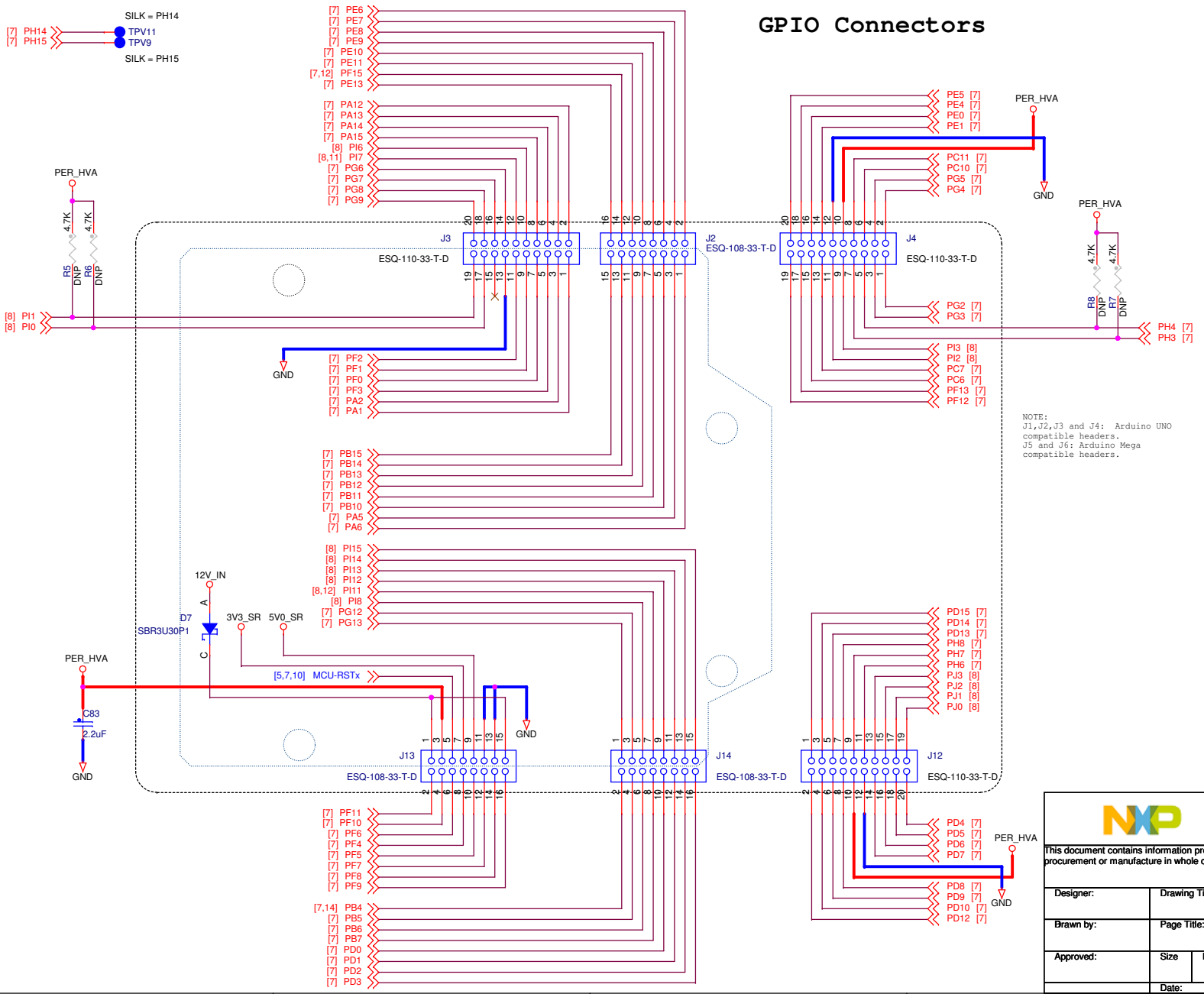
GPIO Connectors



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