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Revisions

Rev	Description	Date	Approved
X1	PPL Relealse. SCH still under development	20-Aug-15	Andrew Robertson
X2	Update new AFE caps and added RGMII Mode	22-Aug-15	Andrew Robertson
X3	MCU changed to BGA. Power nets fixes	03-Nov-15	Neacsu Catalin
X4	Add 5.0v Reg and CAN PHY	05-Nov-15	Andrew Robertson
X5	Synced parts with CIS, changed decoupling to 0201	05-Nov-15	Andrew Robertson
X6	Fixed pullup voltage for R32, R33, change PN for J6	07-Jan-16	Andrew Robertson
A	Release to Agile	08-Jan-16	Andrew Robertson
A1	Removed connection to SD_ADC0	08-Jan-16	Andrew Robertson

S32R274-RADAR

Automotive Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: Andrew Robertson	Drawing Title: S32R274-RADAR	
Drawn by: Andrew Robertson	Page Title: TITLE, TOC & REV	
Approved: Andrew Robertson	Size C / Document Number SCH-29022 PDF: SPF-29022	Rev A1
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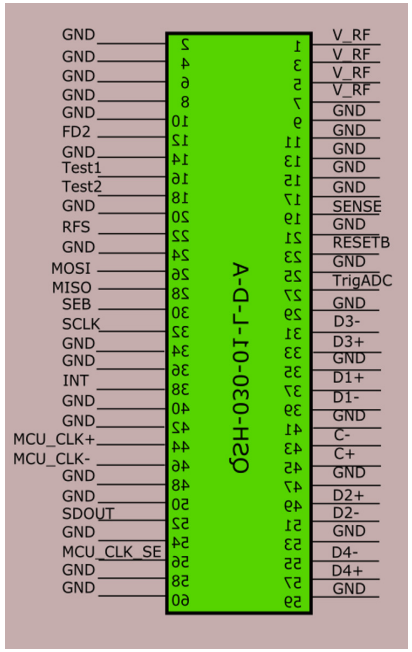
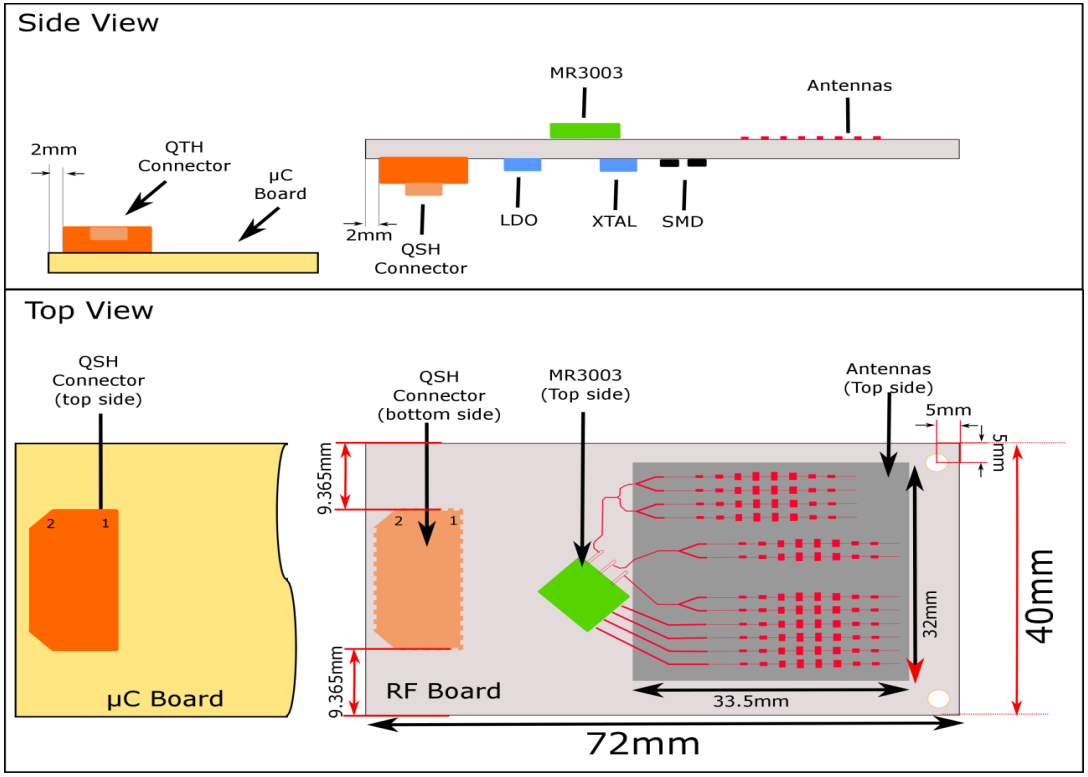
Eagle Connector Pinout



Eagle Board Connector Diagram



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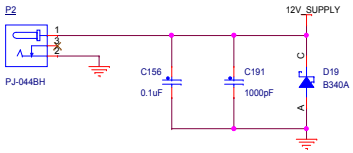
Power supply input

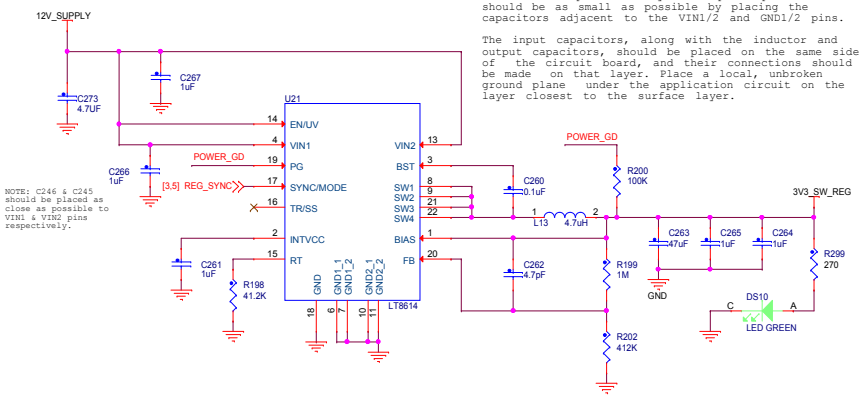
Main Power-In
2.1mm Barrel
PWR JACK PLUG VERT TH Connector



S32R274 SWITCHING REG - 4A, 3.3V

NOTE: The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the VIN1/2 and GND1/2 pins.

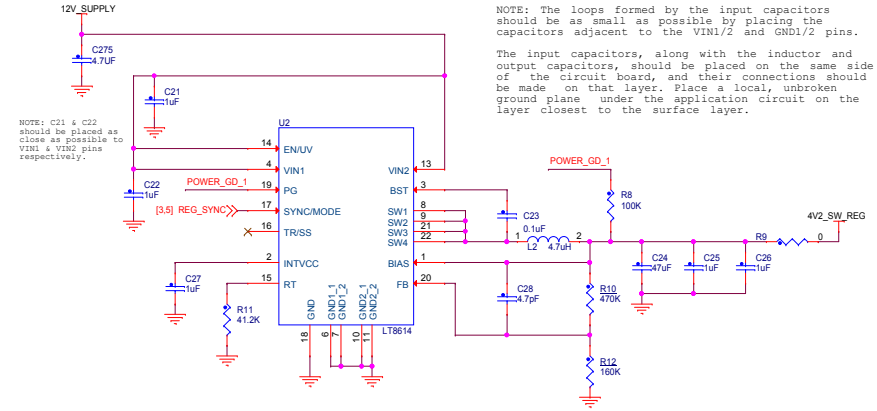
The input capacitors, along with the inductor and output capacitors, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer.



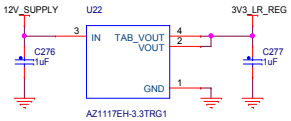
Eagle Supply Switching Reg - 4A, 4.2V

NOTE: The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the VIN1/2 and GND1/2 pins.

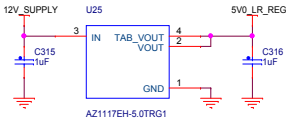
The input capacitors, along with the inductor and output capacitors, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer.



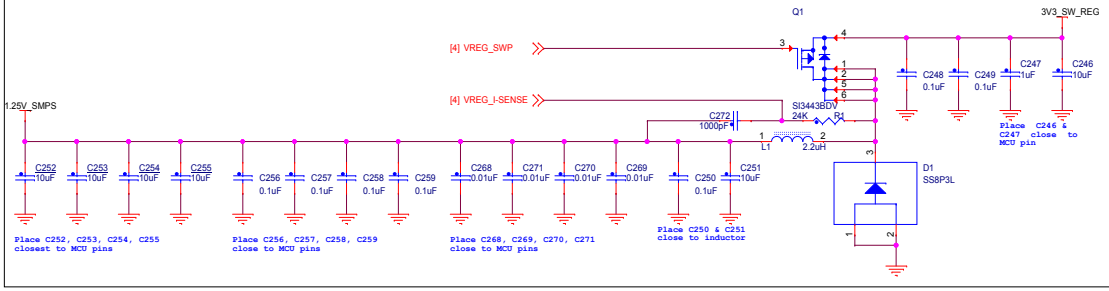
3.3v Linear Regulation



5.0v Regulation



Internal SMPS Circuit



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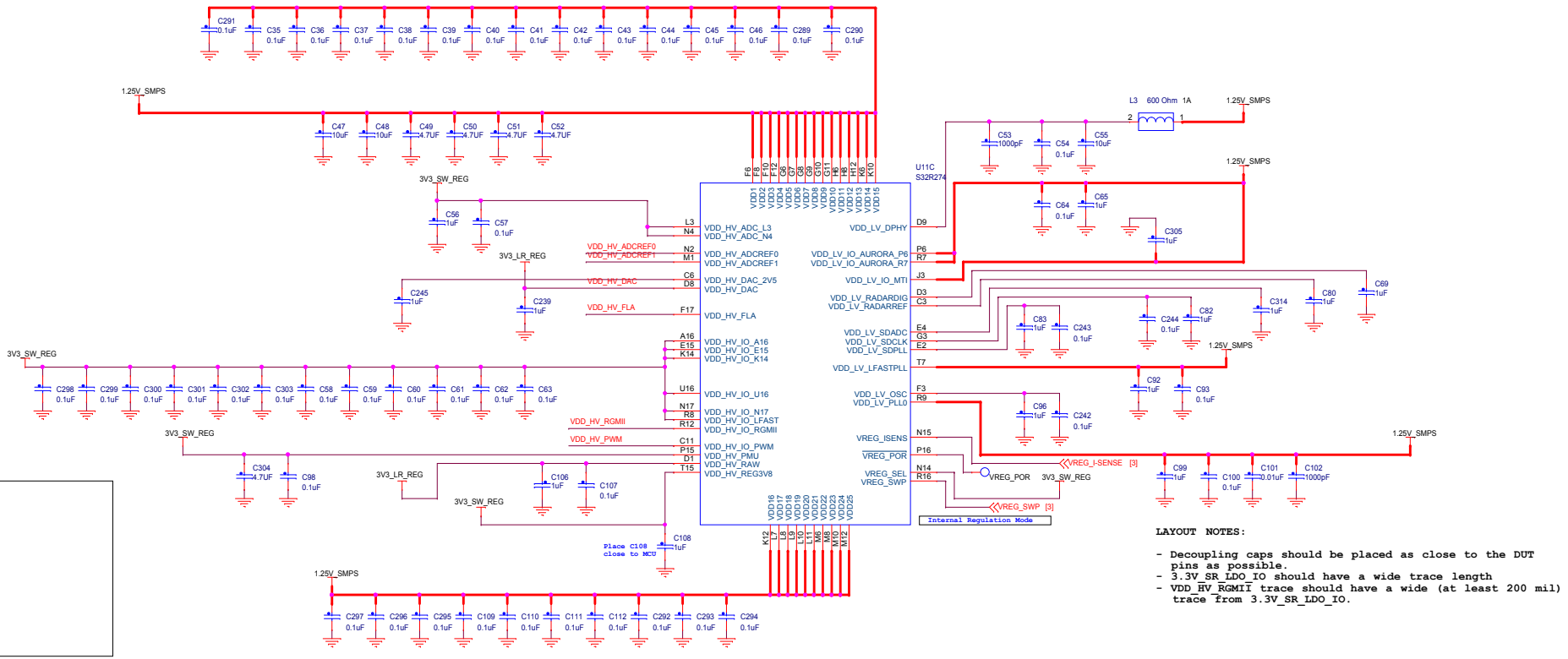
MCU Power Connections and Decoupling

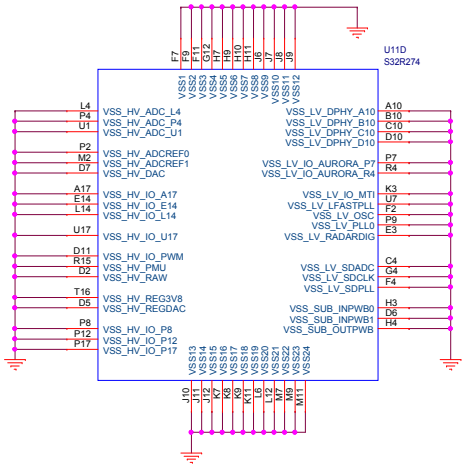


GND Test Points

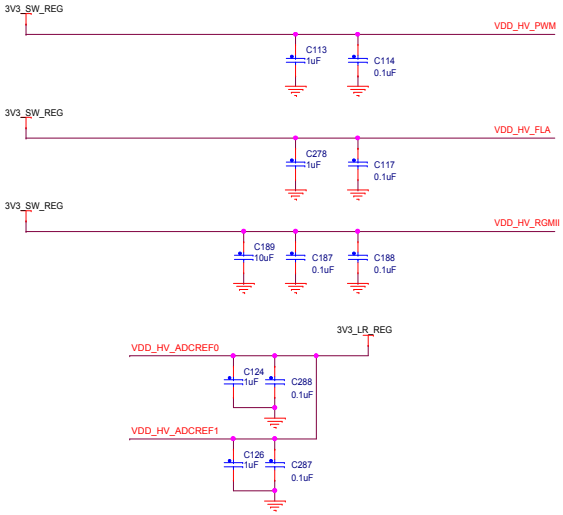
LAYOUT NOTES:

- Decoupling caps should be placed as close to the DUT pins as possible.
- 3.3V_SR_LDO_IO should have a wide trace length
- VDD_HV_RGMII trace should have a wide (at least 200 mil) trace from 3.3V_SR_LDO_IO.

MCU Grounds



Supply Decoupling



Reset Circuit

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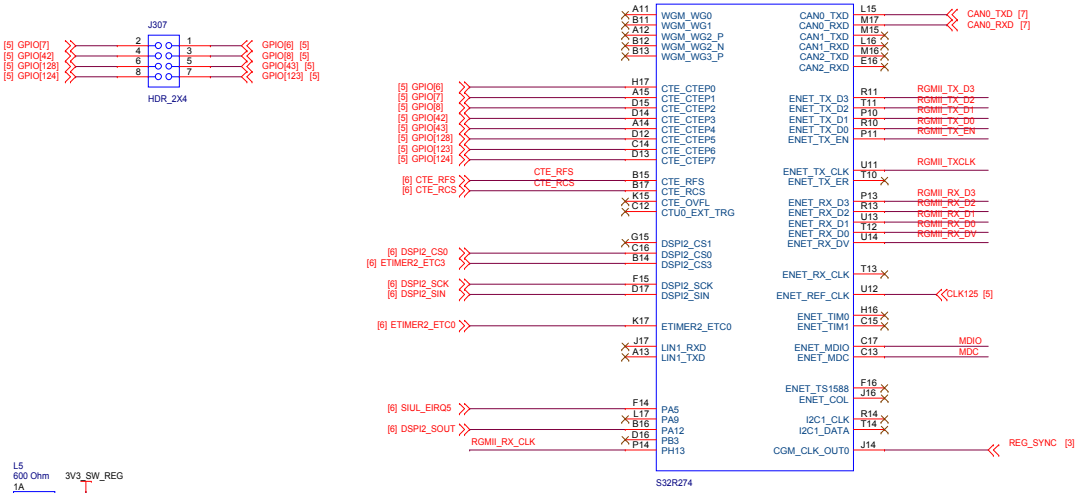
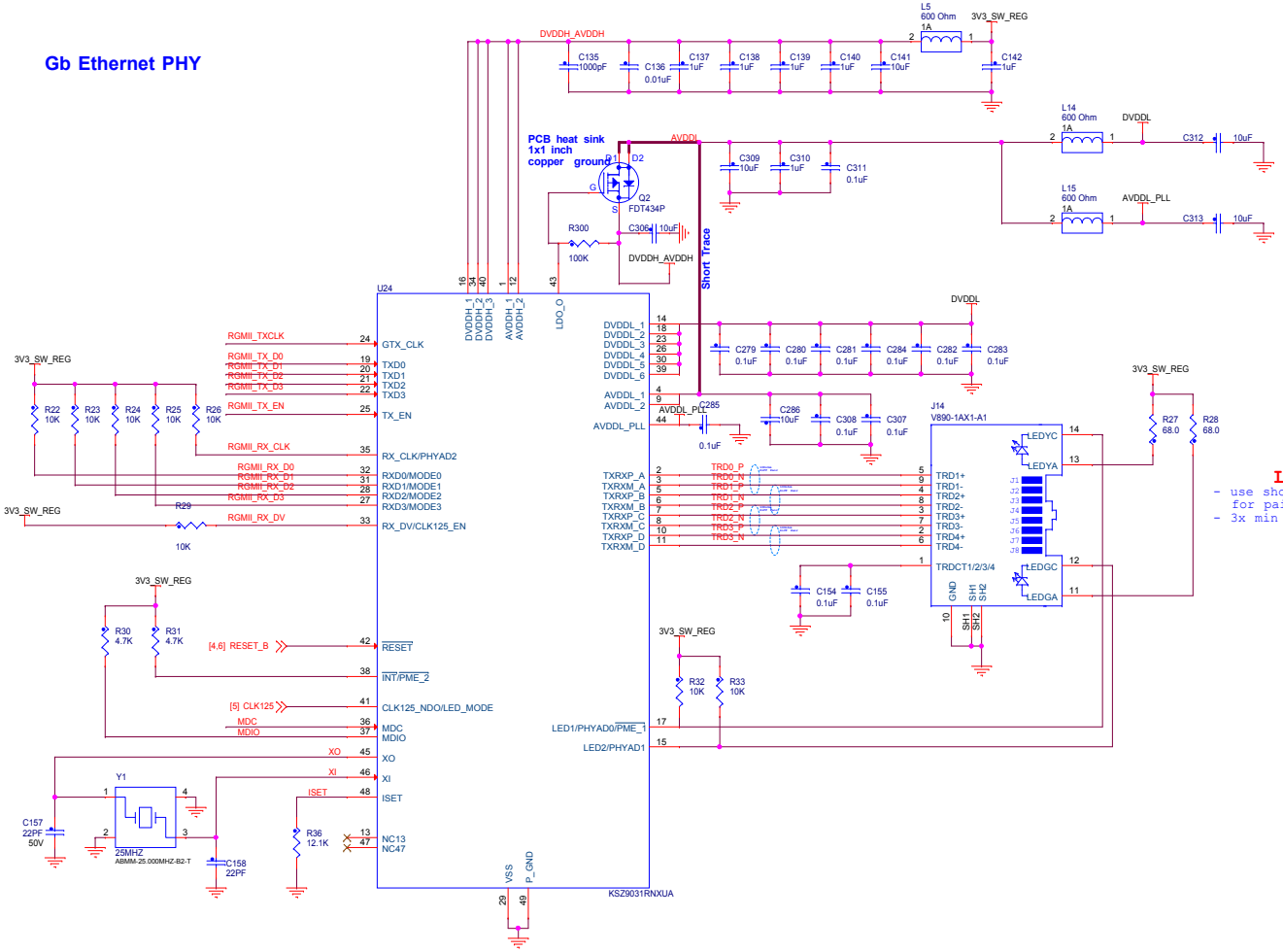
RRU Connections



Gb Ethernet PHY



LAYOUT CRITICAL!

- use short parallel traces with same length for pairs. 3x min distance between pairs.
- 3x min distance to other signals inlc. GND

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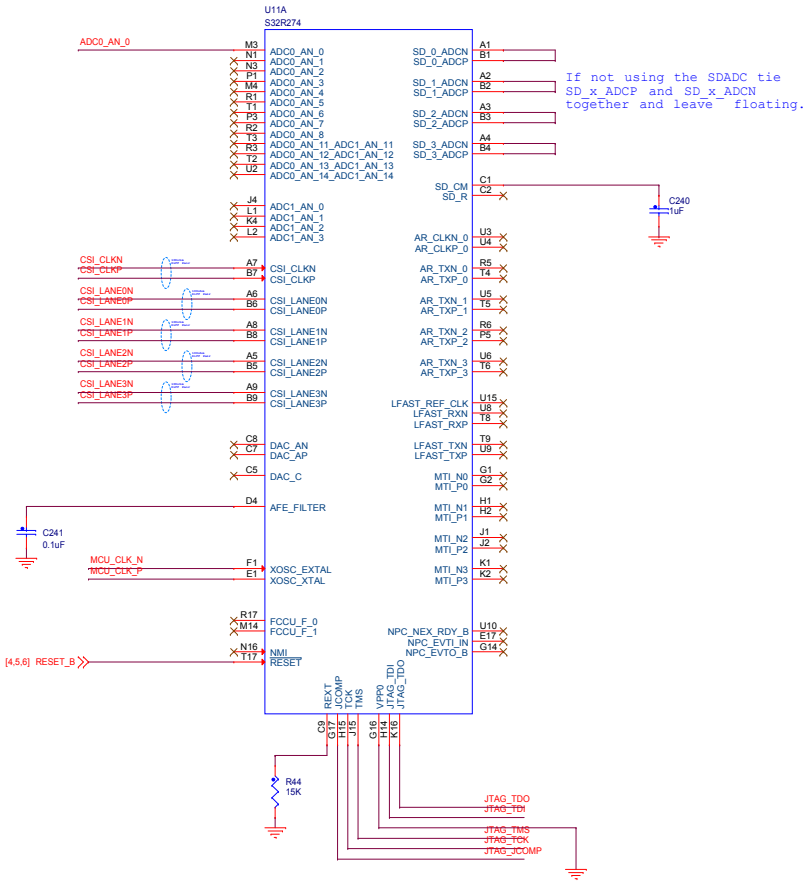
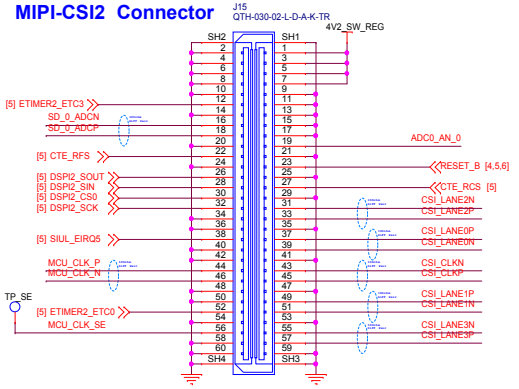


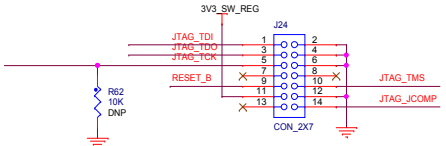
MIPI-CSI2 Connector



LAYOUT CRITICAL!

- Use short parallel traces with same length for pairs. 3x min distance between pairs.
- 3x min distance to other signals inlc. GND
- Avoid vias where possible but if required ensure they are matched for all signal lines, with 50ohm controlled impedance.
- Ensure all pairs have matched trace lengths, including CLK lines.
- Ensure no tracks run parallel to diff pairs to minimise crosstalk.

JTAG



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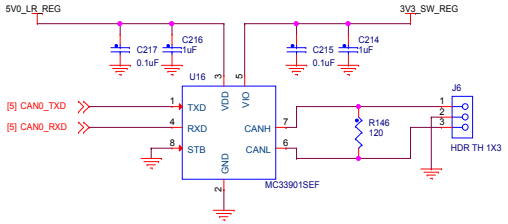
CAN PHY



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