

MUN5313DW1, NSBC144EPDXV6, NSBC144EPDP6

Complementary Bias Resistor Transistors R1 = 47 kΩ, R2 = 47 kΩ

NPN and PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

(T_A = 25°C both polarities Q₁ (PNP) & Q₂ (NPN), unless otherwise noted)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V _{CBO}	50	Vdc
Collector-Emitter Voltage	V _{CEO}	50	Vdc
Collector Current – Continuous	I _C	100	mAdc
Input Forward Voltage	V _{IN(fwd)}	40	Vdc
Input Reverse Voltage	V _{IN(rev)}	10	Vdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
MUN5313DW1T1G, SMUN5313DW1T1G*	SOT-363	3,000/Tape & Reel
SMUN5313DW1T3G*	SOT-363	10,000/Tape & Reel
NSBC144EPDXV6T1G NSVBC144EPDXV6T1G*	SOT-563	4,000/Tape & Reel
NSBC144EPDXV6T5G	SOT-563	8,000/Tape & Reel
NSBC144EPDP6T5G	SOT-963	8,000/Tape & Reel

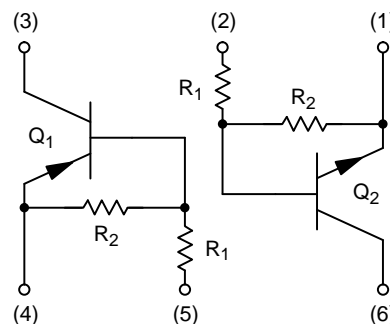
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



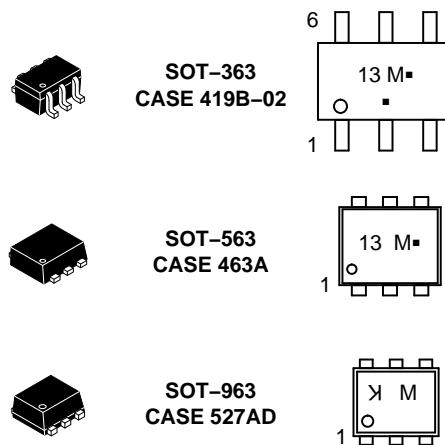
ON Semiconductor®

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PIN CONNECTIONS



MARKING DIAGRAMS



13/K = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
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MUN5313DW1 (SOT-363) ONE JUNCTION HEATED

Total Device Dissipation T _A = 25°C (Note 1) (Note 2) Derate above 25°C (Note 1) (Note 2)	P _D	187 256 1.5 2.0	mW mW/°C
Thermal Resistance, Junction to Ambient (Note 1) (Note 2)	R _{θJA}	670 490	°C/W

MUN5313DW1 (SOT-363) BOTH JUNCTION HEATED (Note 3)

Total Device Dissipation T _A = 25°C (Note 1) (Note 2) Derate above 25°C (Note 1) (Note 2)	P _D	250 385 2.0 3.0	mW mW/°C
Thermal Resistance, Junction to Ambient (Note 1) (Note 2)	R _{θJA}	493 325	°C/W
Thermal Resistance, Junction to Lead (Note 1) (Note 2)	R _{θJL}	188 208	°C/W
Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C

NSBC144EPDXV6 (SOT-563) ONE JUNCTION HEATED

Total Device Dissipation T _A = 25°C (Note 1) Derate above 25°C (Note 1)	P _D	357 2.9	mW mW/°C
Thermal Resistance, Junction to Ambient (Note 1)	R _{θJA}	350	°C/W

NSBC144EPDXV6 (SOT-563) BOTH JUNCTION HEATED (Note 3)

Total Device Dissipation T _A = 25°C (Note 1) Derate above 25°C (Note 1)	P _D	500 4.0	mW mW/°C
Thermal Resistance, Junction to Ambient (Note 1)	R _{θJA}	250	°C/W
Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C

NSBC144EPDP6 (SOT-963) ONE JUNCTION HEATED

Total Device Dissipation T _A = 25°C (Note 4) (Note 5) Derate above 25°C (Note 4) (Note 5)	P _D	231 269 1.9 2.2	MW mW/°C
Thermal Resistance, Junction to Ambient (Note 4) (Note 5)	R _{θJA}	540 464	°C/W

NSBC144EPDP6 (SOT-963) BOTH JUNCTION HEATED (Note 3)

Total Device Dissipation T _A = 25°C (Note 4) (Note 5) Derate above 25°C (Note 4) (Note 5)	P _D	339 408 2.7 3.3	MW mW/°C
Thermal Resistance, Junction to Ambient (Note 4) (Note 5)	R _{θJA}	369 306	°C/W
Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C

- FR-4 @ Minimum Pad.
- FR-4 @ 1.0 × 1.0 Inch Pad.
- Both junction heated values assume total power is sum of two equally powered channels.
- FR-4 @ 100 mm², 1 oz. copper traces, still air.
- FR-4 @ 500 mm², 1 oz. copper traces, still air.

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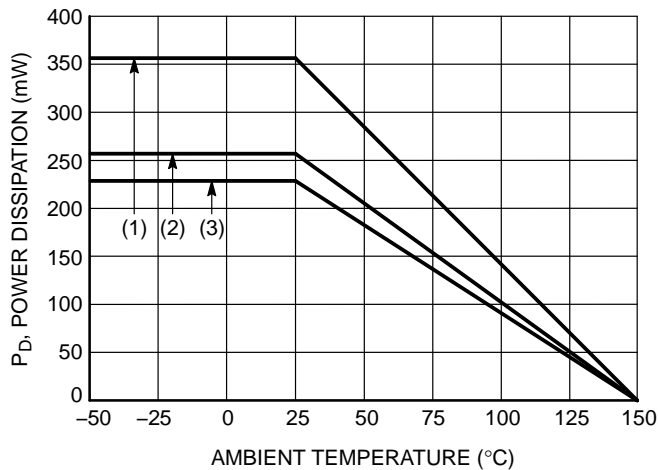
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ both polarities Q_1 (PNP) & Q_2 (NPN), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current ($V_{CB} = 50\text{ V}$, $I_E = 0$)	I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current ($V_{CE} = 50\text{ V}$, $I_B = 0$)	I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current ($V_{EB} = 6.0\text{ V}$, $I_C = 0$)	I_{EBO}	–	–	0.1	mAdc
Collector-Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 6) ($I_C = 2.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	50	–	–	Vdc

ON CHARACTERISTICS

DC Current Gain (Note 6) ($I_C = 5.0\text{ mA}$, $V_{CE} = 10\text{ V}$)	h_{FE}	80	140	–	
Collector-Emitter Saturation Voltage (Note 6) ($I_C = 10\text{ mA}$, $I_B = 0.3\text{ mA}$)	$V_{CE(sat)}$	–	–	0.25	V
Input Voltage (Off) ($V_{CE} = 5.0\text{ V}$, $I_C = 100\text{ }\mu\text{A}$) (NPN) ($V_{CE} = 5.0\text{ V}$, $I_C = 100\text{ }\mu\text{A}$) (PNP)	$V_{i(off)}$	– –	1.2 1.2	– –	Vdc
Input Voltage (On) ($V_{CE} = 0.2\text{ V}$, $I_C = 3.0\text{ mA}$) (NPN) ($V_{CE} = 0.2\text{ V}$, $I_C = 3.0\text{ mA}$) (PNP)	$V_{i(on)}$	– –	1.9 2.0	– –	Vdc
Output Voltage (On) ($V_{CC} = 5.0\text{ V}$, $V_B = 3.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OL}	–	–	0.2	Vdc
Output Voltage (Off) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OH}	4.9	–	–	Vdc
Input Resistor	R_1	32.9	47	61.1	k Ω
Resistor Ratio	R_1/R_2	0.8	1.0	1.2	

6. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle $\leq 2\%$.



- (1) SOT-363; 1.0 x 1.0 Inch Pad
- (2) SOT-563; Minimum Pad
- (3) SOT-963; 100 mm², 1 oz. Copper Trace

Figure 1. Derating Curve

TYPICAL CHARACTERISTICS – NPN TRANSISTOR
MUN5313DW1, NSBC144EPDXV6

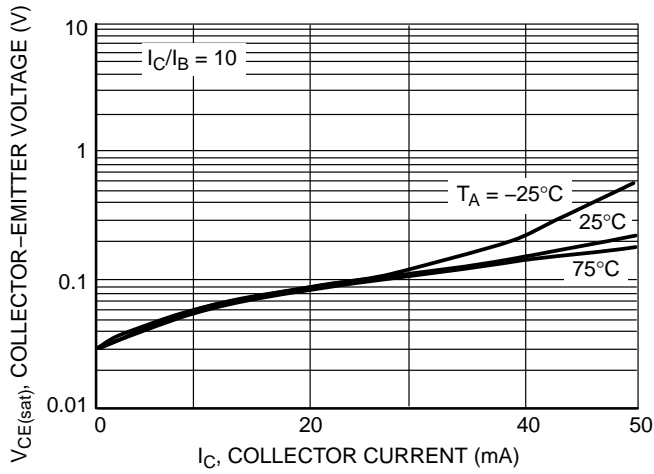


Figure 2. $V_{CE(sat)}$ vs. I_C

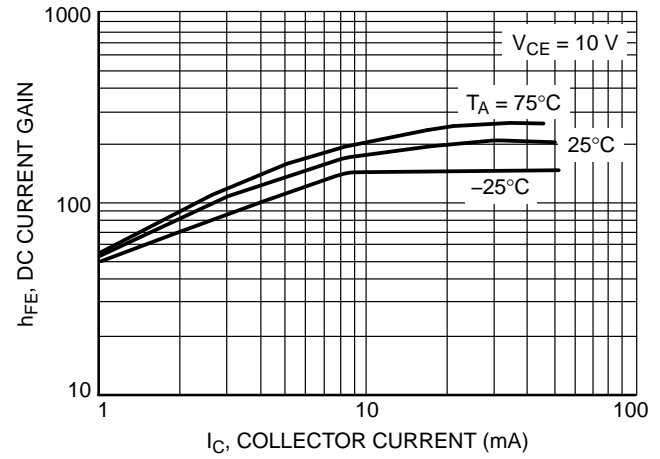


Figure 3. DC Current Gain

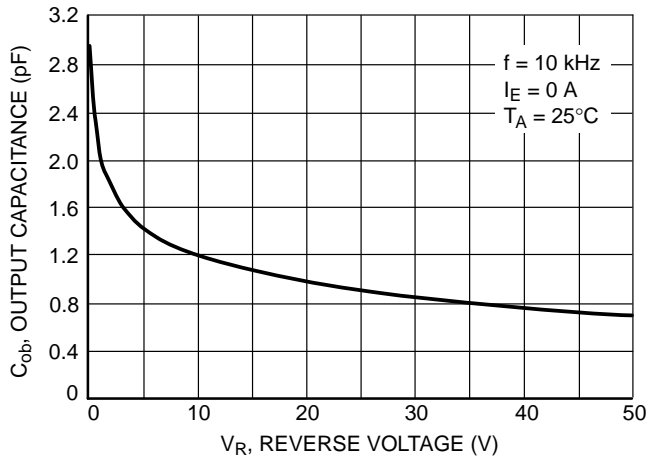


Figure 4. Output Capacitance

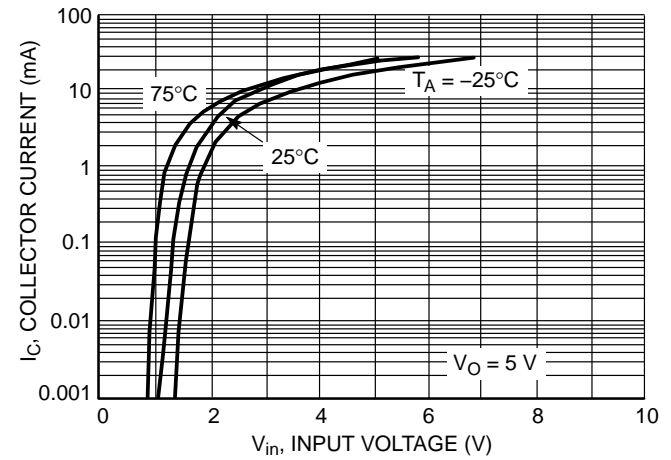


Figure 5. Output Current vs. Input Voltage

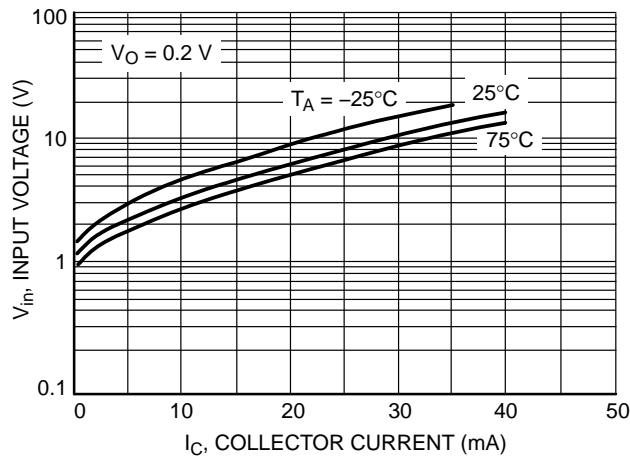


Figure 6. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – PNP TRANSISTOR
MUN5313DW1, NSBC144EPDXV6

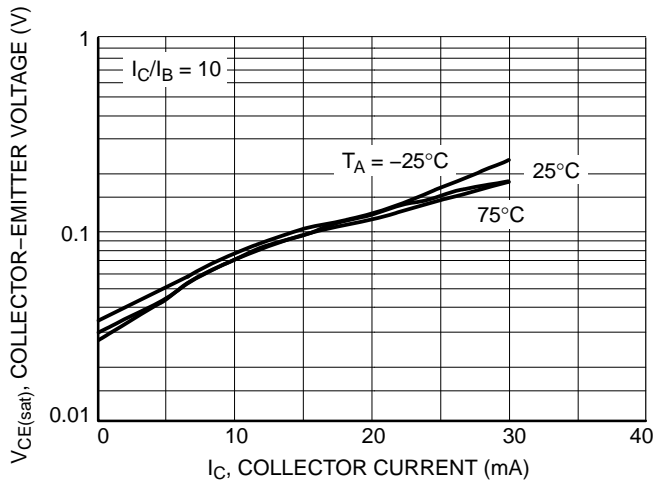


Figure 7. $V_{CE(sat)}$ vs. I_C

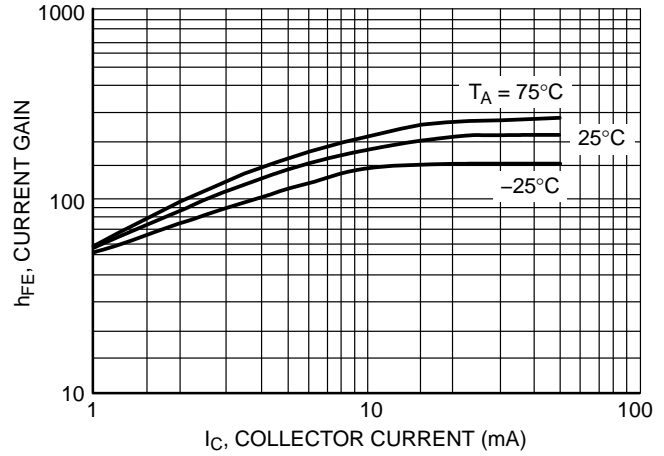


Figure 8. DC Current Gain

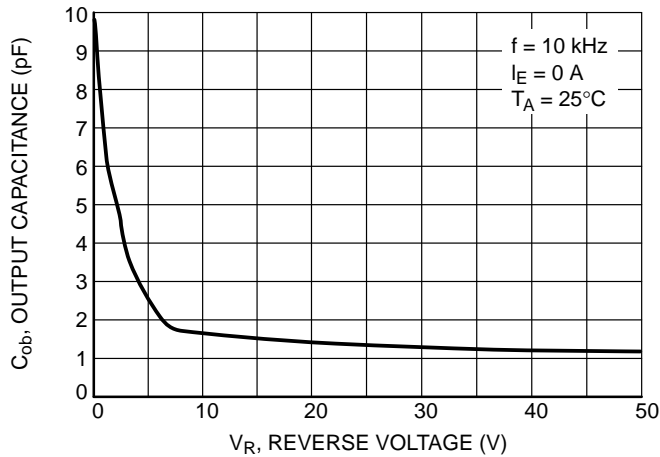


Figure 9. Output Capacitance

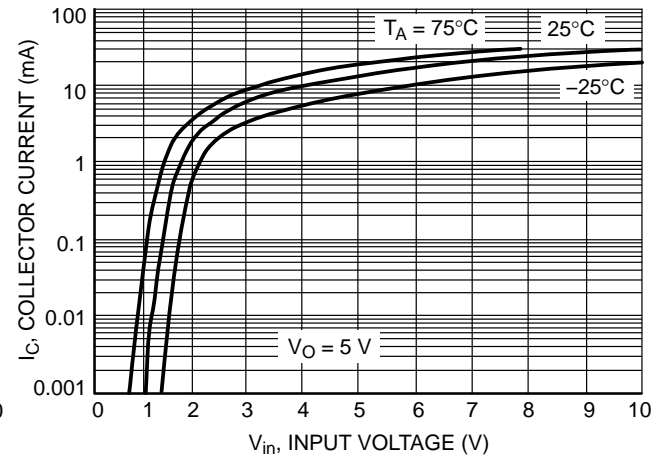


Figure 10. Output Current vs. Input Voltage

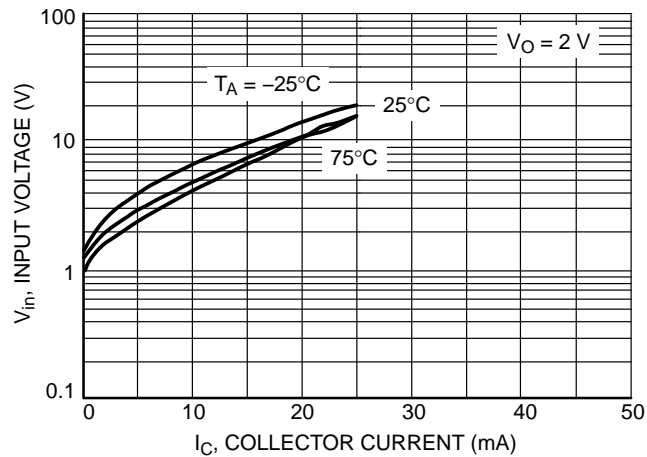


Figure 11. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – NPN TRANSISTOR
NSBC144EPDP6

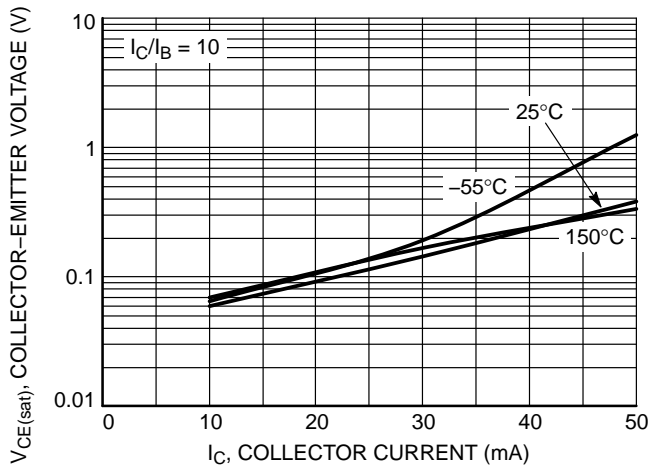


Figure 12. $V_{CE(sat)}$ vs. I_C

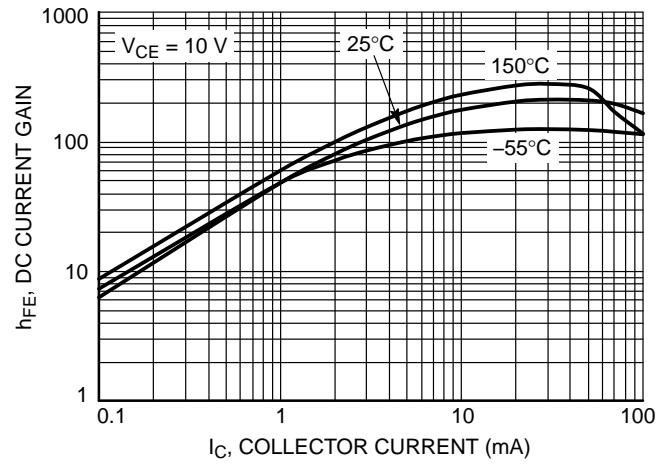


Figure 13. DC Current Gain

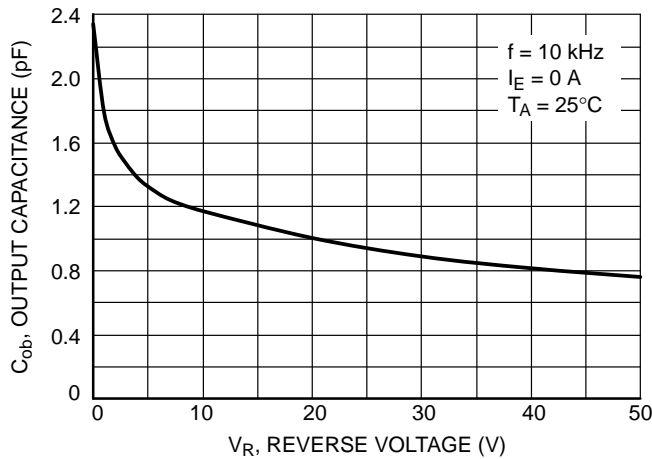


Figure 14. Output Capacitance

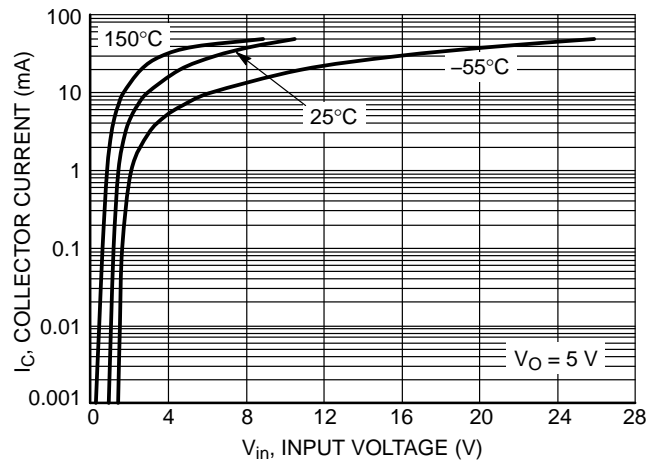


Figure 15. Output Current vs. Input Voltage

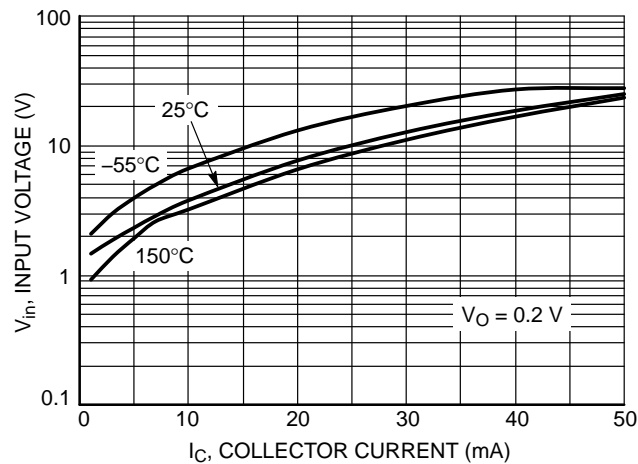


Figure 16. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – PNP TRANSISTOR
NSBC144EPDP6

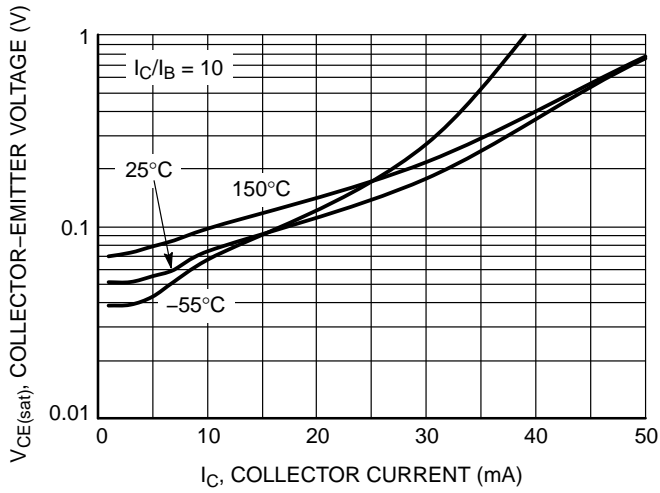


Figure 17. $V_{CE(sat)}$ vs. I_C

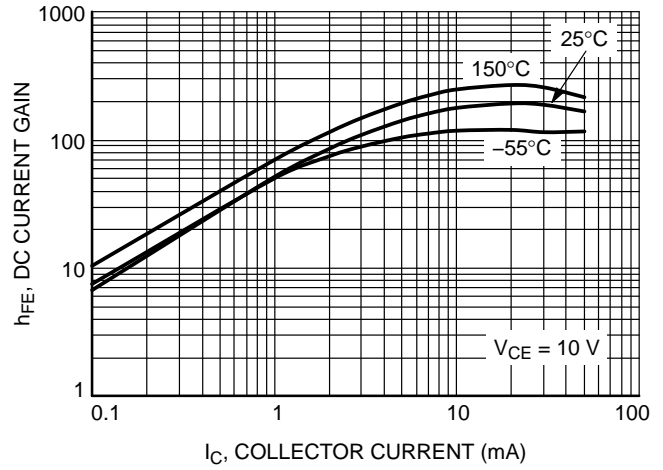


Figure 18. DC Current Gain

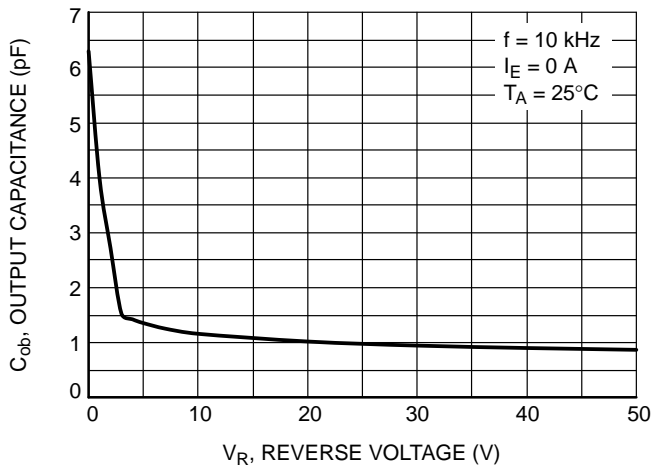


Figure 19. Output Capacitance

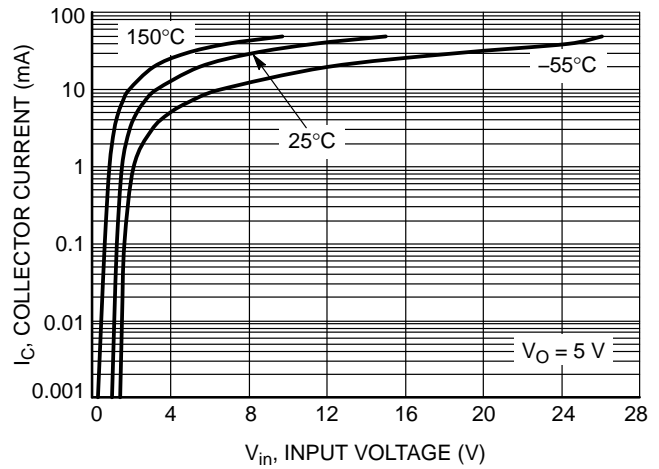


Figure 20. Output Current vs. Input Voltage

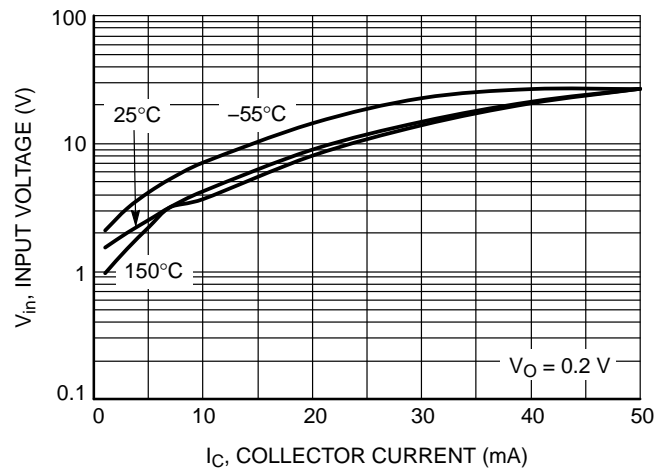
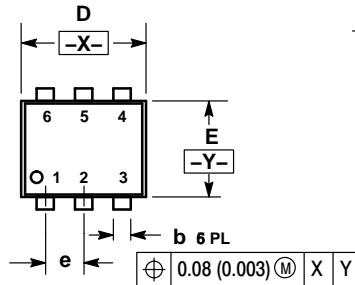


Figure 21. Input Voltage vs. Output Current

PACKAGE DIMENSIONS

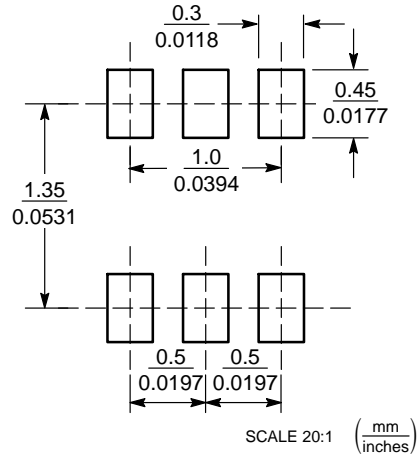
SOT-563, 6 LEAD
CASE 463A
ISSUE G

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

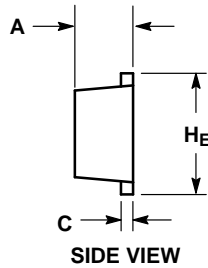
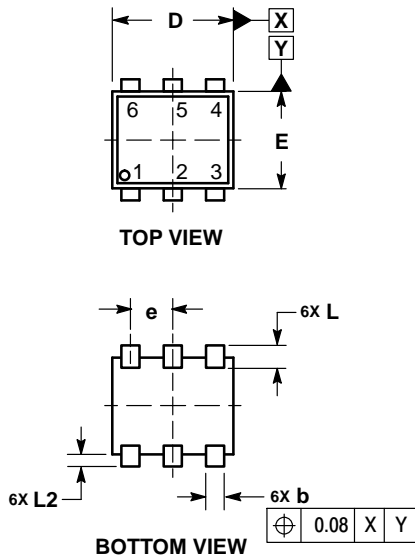
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H _E	1.50	1.60	1.70	0.059	0.062	0.066

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

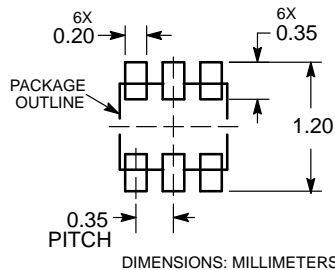
PACKAGE DIMENSIONS

SOT-963
CASE 527AD
ISSUE E

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H _E	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15

RECOMMENDED
MOUNTING FOOTPRINT*

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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