NVIDIA JETSON TX2 PIN AND FUNCTION NAMES GUIDE

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Application Note

DOCUMENT CHANGE HISTORY

DA-08707-001_v1.0

Version	Date	Description of Change
1.0	August 28, 2017	Initial Release

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INTRODUCTION

The NVIDIA® Jetson™ TX2 is a System on Module (SOM) built around the NVIDIA® Tegra® X2 System on Chip (SoC). Jetson TX2 documentation often refers to names of interfaces, pins, functions, etc., from an SOM perspective, but other documentation (for example, the TRM) will necessarily take a SoC perspective. Some documentation will reference both SOM and SoC naming. It is important to understand whether a given document is using pin names/numbers, interface names/instances, and function names/instances with reference to the SOM or to the SoC.

Various documents are provided to help customers design, lay out, build, and configure NVIDIA Jetson module based designs. Table 1 lists the main documents that are focused on the hardware, or contain references to hardware features.

Table 1. Hardware References and Features Documentation

Document Category	Document Name for Jetson TX2 Designs	Description
Data Sheet	Jetson TX2 Module Data Sheet	•Module overview •Power and system management •Interface and signal description •Electrical, package, and thermal specifications
Technical Reference Manual	Tegra X2 (SoC) Technical Reference Manual	•Address map •Chapters per block (functional description, programming guidelines, and registers)
Product OEM Design Guide	Jetson TX2 OEM Product Design Guide	•Power •Interface chapters (connection figures and tables, and routing guidelines)
Carrier Board Specification	Jetson TX1/TX2 Developer Kit Carrier Board Specification	•Developer Kit features and description •Expansion connector and interface descriptions •Power allocation

Document Category	Document Name for Jetson TX2 Designs	Description
Pinmux	Jetson TX2 Module Pinmux	•Module pin name and number, Tegra ball name •SFIO and GPIO options •Wakes, straps, POR state
Design files	Jetson TX1/TX2 Developer Kit Carrier Board Design Files	•Schematics, layout, bill of materials (BOM) •Misc (Assy drawing, stack-up, gerbers, etc)

PIN AND FUNCTION NAMES

The documentation, references names of interfaces, pins, functions, etc. There are different pin and interface names in many cases on the module vs. chip. Some documents are based on the chip, such as the TRM, while others are based on the module, or may have both chip and module terms and names. This can lead to confusion. It is important to use the right document and to understand whether a term or name is associated with a chip or module pin name or number, an interface name or instance, or function name or instance.

PINMUX

The Jetson TX2 Module Pinmux has the module pin names and pin numbers in the first two columns, and the Tegra ball name in the 3rd column. The GPIOs and SFIO functions are covered in the pin muxing area. The portion of the Pinmux in Table 2 includes one of the I2S interfaces.

Table 2. Jetson TX2 Pin Muxing

		MPIO	Pin Muxing				
Signal Name	**Pin #**	**IC Ball Name**	**GPIO**	**SFIO0**	**SFIO1**	**SFIO2**	**SFIO3**
I2S0_CLK	G2	DAP1_SCLK	GPIO3_PJ.00	I2S1_SCLK			
I2S0_SDOUT	H2	DAP1_DOUT	GPIO3_PJ.01	I2S1_SDATA_OUT			
I2S0_SDIN	G1	DAP1_DIN	GPIO3_PJ.02	I2S1_SDATA_IN			
I2S0_LRCLK	H1	DAP1_FS	GPIO3_PJ.03	I2S1_LRCK			
AUDIO_MCLK	F1	AUD_MCLK	GPIO3_PJ.04	AUD_MCLK			
GPIO20/AUD_INT	H3	GPIO_AUD0	GPIO3_PJ.05				
GPIO19/AUD_RST	F2	GPIO_AUD1	GPIO3_PJ.06				
DSPK_OUT_DAT	H4	GPIO_AUD2	GPIO3_PJ.07		DSPK1_DAT	SPDIF_IN	
DSPK_OUT_CLK	G4	GPIO_AUD3	GPIO3_PK.00		DSPK1_CLK	SPDIF_OUT	

In the case shown in Table 2, for one of the I2S interfaces that are available on the module pins, the following pin/function names exist:

- Module signal names: I2S0_xxx
- Tegra chip pin names: DAP1_xxx
- SFIO 0 function names: I2S1_xxx

This shows that the module pin names, chip pin names, and function names can be fairly different. When referring to the various documents, it is important to understand which name form is applicable. For instance, if the TRM is accessed for information on how to configure the pins or functions, it is necessary to know that the TRM is chip-focused. It will have Tegra pin names when referring to the pins, such as in the Pinmux register section, or function names if the function is being configured. In the case of the module data sheet, the module pin names are relevant. See the following "TRM" and "Data Sheet" sections for details.

DATA SHEET

The module data sheet only uses the module pin names. If a programmer needed to know what Tegra function to configure, it would be necessary to look at either the Pinmux spreadsheet or OEM product design guide to know what Tegra function is associated with that module pin.

Table 3. I2S Signal Descriptions

Signal Name	Type	Description
I2S[3:0]_LRCK	I/O	Frame Sync/Word Select. Supports I2S/PCM audio. Interface can be master or slave
I2S[3:0]_CLK	I/O	Serial Clock/Bit Clock. Supports I2S/PCM audio. Interface can be master or slave
I2S[3:0]_SDIN	I	Data In. Supports I2S/PCM audio. Interface can be master or slave.
I2S[3:0]_SDOUT	I/O	Data Out. Supports I2S/PCM audio. Interface can be master or slave.

Table 4. Pin List

Audio					
F1	AUDIO_MCLK	Audio Codec Master Clock	Output	CMOS – 1.8V	ST
F2	GPIO19_AUD_RST	Audio Codec Reset or GPIO	Output	CMOS – 1.8V	ST
H3	GPIO20_AUD_INT	Audio Codec Interrupt or GPIO	Input	CMOS – 1.8V	ST
G2	I2S0_CLK	Digital Audio Port 1 Clock	Bidirectional	CMOS – 1.8V	ST
H1	I2S0_LRCLK	I2S Audio Port 0 Left/Right Clock	Bidirectional	CMOS – 1.8V	ST
G1	I2S0_SDIN	Digital Audio Port 1 Data In	Input	CMOS – 1.8V	ST
H2	I2S0_SDOUT	I2S Audio Port 0 Data Out	Bidirectional	CMOS – 1.8V	ST

TECHNICAL REFERENCE MANUAL

The Technical Reference Manual (TRM) is based on the chip (for example, Tegra X2). References to pin names (such as DAP1) will be chip pin names. There are also references to functions (such as I2S1). These should match the names of functions in the Pinmux spreadsheet or OEM product design guide. In order to know what pin on the module a Tegra X2 pin is associated with, the Pinmux spreadsheet is the best cross reference, although the OEM product design guide has that information as well.

8.31.7.17 PADCTL_AUDIO_DAP1_SCLK_0

Offset: 0x40 | Read/Write: R/W | SCR Protection: SCR_DAP1_SCLK_0 | Reset: 0x00000454

1:0	I2S1	PM: 0 = I2S1 1 = RSVD1 2 = RSVD2 3 = RSVD3

OEM PRODUCT DESIGN GUIDE

The OEM product design guide focuses on the module, but many of the figures and pin description tables also include the Tegra X2 signal associated with a module pin where applicable. The partial table (Table 5) contains the same I2S interface used as the example in the earlier document sections. Both the module (Jetson TX2) and chip (Tegra X2) pin names are shown.

Table 5. Jetson TX2 Audio Pin Descriptions

Pin #	Jetson TX2 Pin Name	Tegra Signal	Usage/Description	Usage on the Carrier Board	Direction	Pin Type
F1	AUDIO_MCLK	AUDIO_MCLK	Audio Codec Master Clock	Audio	Output	CMOS – 1.8V
G2	I2SO_CLK	DAP1_SCLK	Digital Audio Port 1 Clock	Audio	Bidirectional	CMOS – 1.8V
H1	I2SO_LRCLK	DAP1_FS	I2S Audio Port 0 Field Select	Audio	Bidirectional	CMOS – 1.8V
G1	I2SO_SDIN	DAP1_DIN	Digital Audio Port 1 Data In	Audio	Input	CMOS – 1.8V
H2	I2SO_SDOUT	DAP1_DOUT	I2S Audio Port 0 Data Out	Audio	Bidirectional	CMOS – 1.8V

Figure 1 also shows the I2S interface and includes the chip and module pin names. In addition, the reference schematic net names are used outside the module. The net names may match the form used for the chip pin names, as in the following example, but not in all cases.

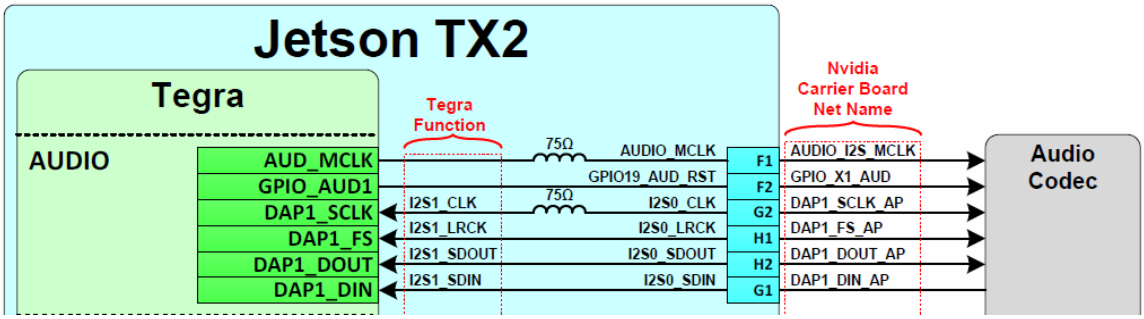

Figure 1. I2S Interface

The following audio connections table contains only the module pin names.

Table 6. Audio Signal Connections

Jetson TX2 Pin Name	Type	Termination	Description
I2S[3:0]-SCLK	I/O	**I2S[2,0]_CLK** have 75Ω beads and **I2S3_CLK** has a 120Ω Bead in series (on Jetson TX2).	**I2S Serial Clock:** Connect to I2S/PCM **CLK** pin of audio device.
I2S[3:0]-LRCK	I/O		**I2S Left/Right Clock:** Connect to Left/Right Clock pin of audio device.
I2S[3:0]-SDATA_OUT	I/O		**I2S Data Output:** Connect to Data Input pin of audio device.
I2S[3:0]-SDATA_IN	I		**I2S Data Input:** Connect to Data Output pin of audio device.
AUD_MCLK	O	75Ω Beads in series (on Jetson TX2).	**Audio Codec Master Clock:** Connect to clock pin of Audio Codec.
GPIO19_AUD_RST	O		**Audio Reset:** Connect to reset pin of Audio Codec.
GPIO20_AUD_INT	I		**Audio Interrupt:** Connect to interrupt pin of Audio Codec.

DEVELOPER KIT CARRIER BOARD SPECIFICATION

The Developer Kit specification uses module (Jetson TX1/TX2) pin names and net names from the carrier board reference design. If it is necessary to know the corresponding chip (Tegra X2) name or function, the Pinmux should be referenced (the OEM product design guide also contains this information).

Table 7. Developer Kit Specification

Pin No.	Signal Name	Jetson TX1/TX2 Pin Name	Usage and Description	Type and Direction
12	AUDIO_I2S_SRCLK_3V3	I2S0_SCLK	Audio I2S #0 Clock	Bidirectional
35	AUDIO_I2S_SFSYNC_3V3	I2S0_LRCLK	Audio I2S #0 Left/Right Clock	Bidirectional
38	AUDIO_I2S_SIN_3V3	I2S0_SDIN	Audio I2S #0 Data In	Input
40	AUDIO_I2S_SOUT_3V3	I2S0_SDOUT	Audio I2S #0 Data Out	Output

DESIGN FILES

The design files (schematics, layout, etc.) also contain only module pin names and net names. Look to the Pinmux or OEM design guide if it is necessary to know which chip pin is associated with a particular module pin name.

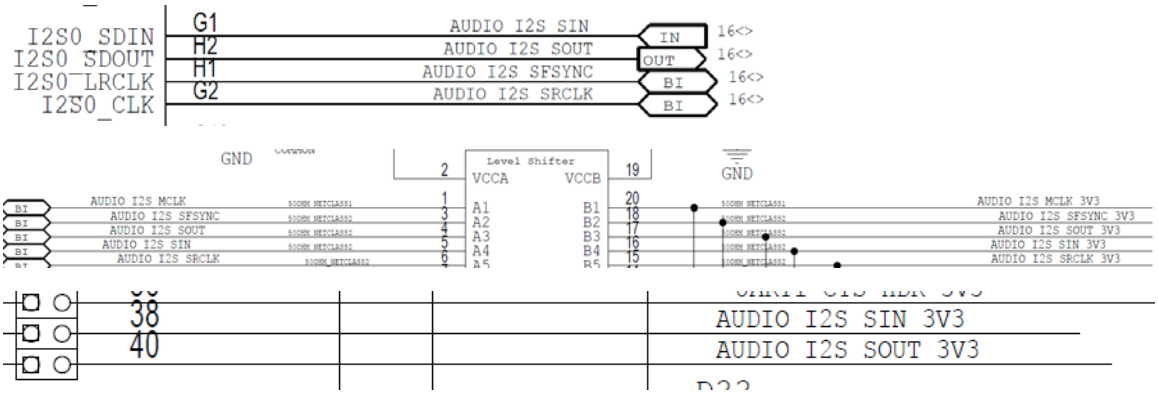

Figure 2. Design Schematics

CHIP, MODULE, AND CARRIER BOARD PIN NAMES AND NUMBERS

The information provided in the following table can be found in various hardware documentation (as described within this application note). Table 8 provides a consolidation of this information for your convenience.

Table 8. Chip, Module, and Carrier Board Pinout

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	Tegra X2 Pin Name
A1	VDD_IN	VDD_MOD	–
A2	VDD_IN	VDD_MOD	–
A3	GND	GND	–
A4	GND	GND	–
A5	RSVD	RSVD1	–
A6	I2C_PM_CLK	I2C_PM_CLK	GEN8_I2C_SCL
A7	CHARGING#	CHARGING	(PMIC GPIO5)
A8	GPIO14_AP_WAKE_MDM	AP_WAKE_MDM_1V8	UFS0_RST
A9	GPIO15_AP2MDM_READY	AP2MDM_READY	UFS0_REF_CLK
A10	GPIO16_MDM_WAKE_AP	MDM_WAKE_AP_1V8	GPIO_MDM2
A11	JTAG_GP1 (RSVD)	NVJTAG_SEL	NVJTAG_SEL
A12	JTAG_TMS	JTAG_AP_TMS	JTAG_TMS
A13	JTAG_TDO	JTAG_AP_TDO	JTAG_TD0
A14	JTAG_RTCK	JTAG_AP_RTCK	–
A15	UART2_CTS#	UART2_CTS	UART2_CTS
A16	UART2_RTS#	UART2_RTS	UART2_RTS
A17	USB0_EN_OC#	USB_VBUS_EN0	USB_VBUS_EN0

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	Tegra X2 Pin Name
A18	USB1_EN_OC#	USB_VBUS_EN1	USB_VBUS_EN1
A19	USB2_EN_OC#	USB_VBUS_EN2	–
A20	I2C_GP1_DAT	I2C_GP1_DAT_3V3	GEN1_I2C_SDA
A21	I2C_GP1_CLK	I2C_GP1_CLK_3V3	GEN1_I2C_SCL
A22	GPIO_EXP1_INT	GPIO_EXP1_INT	GPIO_MDM7
A23	GPIO_EXP0_INT	GPIO_EXP0_INT	GPIO_MDM1
A24	LCD1_BKLT_PWM	LCD1_BKLT_PWM	GPIO_DIS5
A25	LCD_TE	LCD_TE	GPIO_DIS1
A26	GSYNC_HSYNC	GS_H	GPIO_DIS4
A27	GSYNC_VSYNC	GS_V	GPIO_DIS2
A28	GND	GND	–
A29	SDIO_RST#	WIFI2_EN	GPIO_WAN3
A30	SDIO_D3	SDIO_D3	–
A31	SDIO_D2	SDIO_D2	–
A32	SDIO_D1	SDIO_D1	–
A33	DP1_HPD	HDMI_HPD	DP_AUX_CH1_HPD
A34	DP1_AUX_CH-	HDMI_DDC_SDA_POL	DP_AUX_CH1_N
A35	DP1_AUX_CH+	HDMI_DDC_SCL_POL	DP_AUX_CH1_P
A36	USB0_OTG_ID	USB0_ID_IO_CONN	(PMIC GPIO0)
A37	GND	GND	–
A38	USB1_D+	USB1_D_P	USB1_DP
A39	USB1_D-	USB1_D_N	USB1_DN
A40	GND	GND	–
A41	PEX2_REFCLK+	PEX2_REFCLK_P	PEX_CLK2P
A42	PEX2_REFCLK-	PEX2_REFCLK_N	PEX_CLK2N
A43	GND	GND	–
A44	PEX0_REFCLK+	PEX_CLK0_P	PEX_CLK1P
A45	PEX0_REFCLK-	PEX_CLK0_N	PEX_CLK1N
A46	RESET_OUT#	RESET_OUT_L	SYS_RESET_N
A47	RESET_IN#	RESET_IN_L	(PMIC NRST_IO)
A48	CARRIER_PWR_ON	CARRIER_PWR_ON	–
A49	CHARGER_PRSNT#	ACOK	–
A50	VDD_RTC	BBAT	(PMIC BBATT)
B1	VDD_IN	VDD_MOD	–
B2	VDD_IN	VDD_MOD	–
B3	GND	GND	–
B4	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	Tegra X2 Pin Name
B5	RSVD	RSVD2	–
B6	I2C_PM_DAT	I2C_PM_DAT	GEN8_I2C_SDA
B7	CARRIER_STBY#	SOC_PWR_REQ	SOC_PWR_REQ
B8	VIN_PWR_BAD#	VIN_PWR_BAD_L	–
B9	GPIO17_MDM2AP_READY	MDM2AP_READY_1V8	GPIO_PQ7
B10	GPIO18_MDM_COLDBOOT	MDM_COLDBOOT_1V8	GPIO_PQ6
B11	JTAG_TCK	JTAG_AP_TCK	JTAG_TCK
B12	JTAG_TDI	JTAG_AP_TDI	JTAG_TDI
B13	JTAG_GP0	JTAG_AP_TRST_L	JTAG_TRST_N
B14	GND	GND	–
B15	UART2_RX	UART2_RXD	UART2_RX
B16	UART2_TX	UART2_TXD	UART2_TX
B17	FAN_TACH	FAN_TACH	UART5_TX
B18	GNSS_PPS (RSVD)	GNSS_PPS	–
B19	GPIO11_AP_WAKE_BT	AP_WAKE_BT	GPIO_PQ5
B20	GPIO10_WIFI_WAKE_AP	WIFI2_WAKE_AP_L	GPIO_WAN4
B21	GPIO12_BT_EN	BT2_EN	MCU_PWR_REQ
B22	GPIO13_BT_WAKE_AP	BT2_WAKE_AP_L	GPIO_WAN2
B23	GPIO7_TOUCH_RST	TOUCH_RST	SAFE_STATE
B24	TOUCH_CLK	TOUCH_CLK	TOUCH_CLK
B25	GPIO6_TOUCH_INT	TOUCH_INT	CAN_GPIO7
B26	LCD_VDD_EN	LCD_EN	GPIO_EDP0
B27	LCD0_BKLT_PWM	LCD_BL_PWM	GPIO_DIS0
B28	LCD_BKLT_EN	LCD_BL_EN	GPIO_DIS3
B29	SDIO_CMD	SDIO_CMD	–
B30	SDIO_CLK	SDIO_CLK	–
B31	GND	GND	–
B32	SDIO_D0	SDIO_D0	–
B33	HDMI_CEC	HDMI_CEC	HDMI_CEC
B34	DP0_AUX_CH-	EDP_AUX_CH0_N	DP_AUX_CH0_N
B35	DP0_AUX_CH+	EDP_AUX_CH0_P	DP_AUX_CH0_P
B36	DP0_HPD	DP_HPD0_AP	DP_AUX_CH0_HPD
B37	USB0_VBUS_DET	VDD_VBUS	UART5_CTS
B38	GND	GND	–
B39	USB0_D+	USB0_IO_CONN_D_P	USB0_DP
B40	USB0_D-	USB0_IO_CONN_D_N	USB0_DN
B41	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	Tegra X2 Pin Name
B42	USB2_D+	USB2_D_P	USB2_DP
B43	USB2_D-	USB2_D_N	USB2_DN
B44	GND	GND	–
B45	PEX1_REFCLK+	PEX_CLK1_P	PEX_CLK3P
B46	PEX1_REFCLK-	PEX_CLK1_N	PEX_CLK3N
B47	GND	GND	–
B48	RSVD	RSVD3	–
B49	RSVD	RSVD4	–
B50	POWER_BTN#	POWER_BTN	POWER_ON / (PMIC EN0)
C1	VDD_IN	VDD_MOD	–
C2	VDD_IN	VDD_MOD	–
C3	GND	GND	–
C4	GND	GND	–
C5	RSVD	RSVD5	–
C6	I2C_CAM_CLK	CAM_I2C_SCL	CAM_I2C_SCL
C7	BATLOW#	LOW_BAT	(PMIC_GPIO6)
C8	RSVD	CHG_OC_L	BATT_OC
C9	WDT_TIME_OUT#	WDT_TIME_OUT_L	GPIO_SEN7
C10	I2C_GP2_DAT	I2C_GP2_DAT	GEN7_I2C_SDA
C11	I2C_GP2_CLK	I2C_GP2_CLK	GEN7_I2C_SCL
C12	I2C_GP3_CLK	I2C_GP3_CLK	GEN9_I2C_SCL
C13	I2C_GP3_DAT	I2C_GP3_DAT	GEN9_I2C_SDA
C14	I2S1_SDIN	I2S1_SDIN	DAP2_DIN
C15	I2S1_CLK	I2S1_CLK	DAP2_SCLK
C16	FAN_PWM	FAN_PWM	GPIO_SEN6
C17	CAN1_STBY	CAN1_STBY	CAN_GPIO6
C18	CAN1_TX	CAN1_TX	CAN1_DOUT
C19	CAN1_ERR	CAN1_ERR	CAN_GPIO3
C20	CAN_WAKE	CAN_WAKE	CAN_GPIO4
C21	GND	GND	–
C22	CSI5_D0-	CON_CSI_F_D0_N	CSI_F_D0_N
C23	CSI5_D0+	CON_CSI_F_D0_P	CSI_F_D0_P
C24	GND	GND	–
C25	CSI3_D0-	CON_CSI_D_D0_N	CSI_D_D0_N
C26	CSI3_D0+	CON_CSI_D_D0_P	CSI_D_D0_P
C27	GND	GND	–
C28	CSI1_D0-	CON_CSI_B_D0_N	CSI_B_D0_N

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	Tegra X2 Pin Name
C29	CSI1_D0+	CON_CSI_B_D0_P	CSI_B_D0_P
C30	GND	GND	–
C31	DSI3_D0+	CON_DSI_B_D2_P	DSI_D_D0_P
C32	DSI3_D0-	CON_DSI_B_D2_N	DSI_D_D0_N
C33	GND	GND	–
C34	DSI1_D0+	CON_DSI_A_D2_P	DSI_B_D0_P
C35	DSI1_D0-	CON_DSI_A_D2_N	DSI_B_D0_N
C36	GND	GND	–
C37	DP1_TX1-	DP1_TXD1_N	HDMI_DP1_TXDN1
C38	DP1_TX1+	DP1_TXD1_P	HDMI_DP1_TXDP1
C39	GND	GND	–
C40	PEX2_TX+	PEX_TX2_P	PEX_TX3P
C41	PEX2_TX-	PEX_TX2_N	PEX_TX3N
C42	GND	GND	–
C43	USB_SS0_TX+	USB3_TX1_P	PEX_TX0P
C44	USB_SS0_TX-	USB3_TX1_N	PEX_TX0N
C45	GND	GND	–
C46	PEX2_CLKREQ#	PEX2_CKREQ_L	PEX_L1_CLKREQ_N
C47	PEX1_CLKREQ#	PCIE_L1_CLKREQ	PEX_L2_CLKREQ_N
C48	PEX0_CLKREQ#	PCIE0_L0_CLKREQ	PEX_L0_CLKREQ_N
C49	PEX0_RST#	PCIE0_L0_RST	PEX_L0_RST_N
C50	RSVD	RSVD7	–
D1	RSVD	RSVD8	–
D2	RSVD	RSVD9	–
D3	RSVD	RSVD10	–
D4	RSVD	RSVD11	–
D5	RSVD	UART4_RX	UART7_RX
D6	I2C_CAM_DAT	CAM_I2C_SDA	CAM_I2C_SDA
D7	GPIO5_CAM_FLASH_EN	FLASH_EN	UART5_RTS_N
D8	RSVD	UART4_TX	UART7_TX
D9	UART1_TX	UART1_TXD	UART3_TX
D10	UART1_RX	UART1_RXD	UART3_RX
D11	DIRECTDC_OUT2 (RSVD)	DIRECTDC_OUT2	–
D12	DIRECTDC_OUT3 (RSVD)	DIRECTDC_OUT3	–
D13	I2S1_LRCLK	I2S1_LRCLK	DAP2_FS
D14	I2S1_SDOUT	I2S1_SDOUT	DAP2_DOUT
D15	I2C_GP0_DAT	I2C_GP0_DAT_1V8	GPIO_SEN9

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	Tegra X2 Pin Name
D16	AO_DMIC_IN_DAT	AO_DMIC_IN_DAT	CAN_GPIO0
D17	CAN1_RX	CAN1_RX	CAN1_DIN
D18	CAN0_RX	CAN0_RX	CAN0_DIN
D19	CAN0_TX	CAN0_TX	CAN0_DOUT
D20	GND	GND	–
D21	CSI5_CLK-	CON_CSI_F_CLK_N	CSI_F_CLK_N
D22	CSI5_CLK+	CON_CSI_F_CLK_P	CSI_F_CLK_P
D23	GND	GND	–
D24	CSI3_CLK-	CON_CSI_D_CLK_N	CSI_D_CLK_N
D25	CSI3_CLK+	CON_CSI_D_CLK_P	CSI_D_CLK_P
D26	GND	GND	–
D27	CSI1_CLK-	CON_CSI_B_CLK_N	CSI_B_CLK_N
D28	CSI1_CLK+	CON_CSI_B_CLK_P	CSI_B_CLK_P
D29	GND	GND	–
D30	DSI3_CLK+	CON_DSI4_CLK_P	DSI_D_CLK_P
D31	DSI3_CLK-	CON_DSI4_CLK_N	DSI_D_CLK_N
D32	GND	GND	–
D33	DSI1_CLK+	CON_DSI3_CLK_P	DSI_B_CLK_P
D34	DSI1_CLK-	CON_DSI3_CLK_N	DSI_B_CLK_N
D35	GND	GND	–
D36	DP1_TX2-	DP1_TXD2_N	HDMI_DP1_TXDN0
D37	DP1_TX2+	DP1_TXD2_P	HDMI_DP1_TXDP0
D38	GND	GND	–
D39	PEX_RFU_TX+	PEX_TX1_P	PEX_TX1P
D40	PEX_RFU_TX-	PEX_TX1_N	PEX_TX1N
D41	GND	GND	–
D42	USB_SS1_TX+	PEX_TX3_P	PEX_TX2P
D43	USB_SS1_TX-	PEX_TX3_N	PEX_TX2N
D44	GND	GND	–
D45	SATA_TX+	SATA_TX_P	PEX_TX5P
D46	SATA_TX-	SATA_TX_N	PEX_TX5N
D47	SATA_DEV_SLP	SATA_DEV_SLP	PEX_L2_CLKREQ_N
D48	PEX_WAKE#	PCIE_WAKE_L	PEX_WAKE_N
D49	PEX2_RST#	PEX2_RST_L	PEX_L1_RST_N
D50	RSVD	RSVD14	–
E1	FORCE_RECOV#	FORCE_RECOVERY_L	GPIO_SW1
E2	SLEEP#	SLEEP	GPIO_SW2

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	Tegra X2 Pin Name
E3	SPI0_CLK	SPI0_CLK	GPIO_SEN1
E4	SPI0_MISO	SPI0_MISO	GPIO_SEN2
E5	I2S3_SDIN	I2S3_SDIN	DAP4_DIN
E6	I2S3_CLK	I2S3_CLK	DAP4_SCLK
E7	CAM2_MCLK (RSVD)	CAM2_MCLK	GPIO_CAM2
E8	CAM_VSYNC (RSVD)	CAM_VSYNC	QSPI_IO1
E9	UART1_RTS#	UART1_RTS	UART3_RTS
E10	UART1_CTS#	UART1_CTS	UART3_CTS
E11	DIRECTDC_OUT0 (RSVD)	DIRECTDC_OUT0	–
E12	DIRECTDC_OUT1 (RSVD)	DIRECTDC_OUT1	–
E13	SPI1_CS1# (RSVD)	SPI1_CS1	–
E14	SPI1_CS0#	SPI1_CS0	GPIO_CAM7
E15	I2C_GP0_CLK	I2C_GP0_CLK_1V8	GPIO_SEN8
E16	AO_DMIC_IN_CLK	AO_DMIC_IN_CLK	CAN_GPIO1
E17	CAN0_STBY (RSVD)	CAN0_STBY	–
E18	CAN0_ERR	CAN0_ERR	CAN_GPIO5
E19	GND	GND	–
E20	CSI5_D1-	CON_CSI_F_D1_N	CSI_F_D1_N
E21	CSI5_D1+	CON_CSI_F_D1_P	CSI_F_D1_P
E22	GND	GND	–
E23	CSI3_D1-	CON_CSI_D_D1_N	CSI_D_D1_N
E24	CSI3_D1+	CON_CSI_D_D1_P	CSI_D_D1_P
E25	GND	GND	–
E26	CSI1_D1-	CON_CSI_B_D1_N	CSI_B_D1_N
E27	CSI1_D1+	CON_CSI_B_D1_P	CSI_B_D1_P
E28	GND	GND	–
E29	DSI3_D1+	CON_DSI_B_D3_P	DSI_D_D1_P
E30	DSI3_D1-	CON_DSI_B_D3_N	DSI_D_D1_N
E31	GND	GND	–
E32	DSI1_D1+	CON_DSI_A_D3_P	DSI_B_D1_P
E33	DSI1_D1-	CON_DSI_A_D3_N	DSI_B_D1_N
E34	GND	GND	–
E35	DP1_TX3-	DP1_TXD3_N	HDMI_DP1_TXDN3
E36	DP1_TX3+	DP1_TXD3_P	HDMI_DP1_TXDP3
E37	GND	GND	–
E38	DP1_TX0-	DP1_TXD0_N	HDMI_DP1_TXDN2
E39	DP1_TX0+	DP1_TXD0_P	HDMI_DP1_TXDP2

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	Tegra X2 Pin Name
E40	GND	GND	–
E41	PEX1_TX+	PEX_TX0_AP_P	PEX_TX0P
E42	PEX1_TX-	PEX_TX0_AP_N	PEX_TX0N
E43	GND	GND	–
E44	PEX0_TX+	PEX_TX4_P	PEX_TX4P
E45	PEX0_TX-	PEX_TX4_N	PEX_TX4N
E46	GND	GND	–
E47	GBE_LINK_ACT#	GBE_LED0_SPICSB	–
E48	GBE_MDI0+	GBE_MDI0_P	–
E49	GBE_MDI0-	GBE_MDI0_N	–
E50	PEX1_RST#	PCIE_L1_RST	PEX_L2_RST_N
F1	AUDIO_MCLK	AUDIO_I2S_MCLK_R	AUD_MCLK
F2	GPIO19_AUD_RST	AUD_RST	GPIO_AUD1
F3	SPI0_CS0#	SPI0_CS0	GPIO_SEN4
F4	SPI0_MOSI	SPI0_MOSI	GPIO_SEN3
F5	I2S3_LRCLK	I2S3_LRCLK	DAP4_FS
F6	I2S3_SDOUT	I2S3_SDOUT	DAP4_DOUT
F7	GPIO1_CAM1_PWR#	CAM1_PWDN	GPIO_CAM3
F8	CAM1_MCLK	CAM1_MCLK	EXTPERIPH2_CLK
F9	CAM0_MCLK	CAM0_MCLK	EXTPERIPH1_CLK
F10	GND	GND	–
F11	DIRECTDC_IN (RSVD)	DIRECTDC_IN	–
F12	DIRECTDC_CLK (RSVD)	DIRECTDC_CLK	–
F13	SPI1_MOSI	SPI1_MOSI	GPIO_CAM6
F14	SPI1_MISO	SPI1_MISO	GPIO_CAM5
F15	GND	GND	–
F16	SPI2_CS1#	SPI2_CS1	GPIO_MDM4
F17	SDCARD_CD#	SDCARD_CD_L	GPIO_EDP2
F18	SDCARD_D3	SDCARD_DAT3_POL	SDMMC1_DAT3
F19	SDCARD_D2	SDCARD_DAT2_POL	SDMMC1_DAT2
F20	SDCARD_WP	SDCARD_WP	GPIO_EDP1
F21	GND	GND	–
F22	CSI4_D0-	CON_CSI_E_D0_N	CSI_E_D0_N
F23	CSI4_D0+	CON_CSI_E_D0_P	CSI_E_D0_P
F24	GND	GND	–
F25	CSI2_D0-	CON_CSI_C_D0_N	CSI_C_D0_N
F26	CSI2_D0+	CON_CSI_C_D0_P	CSI_C_D0_P

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	Tegra X2 Pin Name
F27	GND	GND	–
F28	CSI0_D0-	CON_CSI_A_D0_N	CSI_A_D0_N
F29	CSI0_D0+	CON_CSI_A_D0_P	CSI_A_D0_P
F30	GND	GND	–
F31	DSI2_D0+	CON_DSI_B_D0_P	DSI_C_D0_P
F32	DSI2_D0-	CON_DSI_B_D0_N	DSI_C_D0_N
F33	GND	GND	–
F34	DSI0_D0+	CON_DSI_A_D0_P	DSI_A_D0_P
F35	DSI0_D0-	CON_DSI_A_D0_N	DSI_A_D0_N
F36	GND	GND	–
F37	DP0_TX1-	EDP_TXD1_N	HDMI_DP0_TXDN1
F38	DP0_TX1+	EDP_TXD1_P	HDMI_DP0_TXDP1
F39	GND	GND	–
F40	PEX2_RX+	PEX_RX2_P	PEX_RX3P
F41	PEX2_RX-	PEX_RX2_N	PEX_RX3N
F42	GND	GND	–
F43	USB_SS0_RX+	USB3_RX1_P	PEX_RX0P
F44	USB_SS0_RX-	USB3_RX1_N	PEX_RX0N
F45	GND	GND	–
F46	GBE_LINK1000#	GBE_LED2	–
F47	GBE_MDI1+	GBE_MDI1_P	–
F48	GBE_MDI1-	GBE_MDI1_N	–
F49	GND	GND	–
F50	GBE_LINK100#	GBE_LED1_SPISCK	–
G1	I2S0_SDIN	AUDIO_I2S_SIN	DAP1_DIN
G2	I2S0_CLK	AUDIO_I2S_SRCLK	DAP1_SCLK
G3	GND	GND	–
G4	DSPK_OUT_CLK	DSPK_OUT_CLK	GPIO_AUD3
G5	I2S2_CLK	I2S2_CLK	DMIC2_DAT
G6	I2S2_SDIN	I2S2_SDIN	DMIC1_DAT
G7	GPIO4_CAM_STROBE	FLASH_STROBE	GPIO_SEN5
G8	GPIO0_CAM0_PWR#	CAM0_PWDN	QSPI_SCK
G9	UART3_CTS#	UART3_CTS	UART4_CTS_N (via mux)
G10	UART3_RTS#	UART3_RTS	UART4_RTS_N (via mux)
G11	UART0_RTS#	UART0_RTS	UART1_RTS
G12	UART0_RX	UART0_RXD	UART1_RX
G13	SPI1_CLK	SPI1_SCK	GPIO_CAM4

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	Tegra X2 Pin Name
G14	GPIO9_MOTION_INT	MOTION_INT_AP_L	CAN_GPIO2
G15	SPI2_MOSI	SPI2_MOSI	GPIO_WAN7
G16	SPI2_CS0#	SPI2_CS0	GPIO_WAN8
G17	GND	GND	–
G18	SDCARD_CLK	SDCARD_CLK_POL	SDMMC1_CLK
G19	SDCARD_CMD	SDCARD_CMD_POL	SDMMC1_CMD
G20	GND	GND	–
G21	CSI4_CLK-	CON_CSI_E_CLK_N	CSI_E_CLK_N
G22	CSI4_CLK+	CON_CSI_E_CLK_P	CSI_E_CLK_P
G23	GND	GND	–
G24	CSI2_CLK-	CON_CSI_C_CLK_N	CSI_C_CLK_N
G25	CSI2_CLK+	CON_CSI_C_CLK_P	CSI_C_CLK_P
G26	GND	GND	–
G27	CSI0_CLK-	CON_CSI_A_CLK_N	CSI_A_CLK_N
G28	CSI0_CLK+	CON_CSI_A_CLK_P	CSI_A_CLK_P
G29	GND	GND	–
G30	DSI2_CLK+	CON_DSI_B_CLK_P	DSI_C_CLK_P
G31	DSI2_CLK-	CON_DSI_B_CLK_N	DSI_C_CLK_N
G32	GND	GND	–
G33	DSI0_CLK+	CON_DSI_A_CLK_P	DSI_A_CLK_P
G34	DSI0_CLK-	CON_DSI_A_CLK_N	DSI_A_CLK_N
G35	GND	GND	–
G36	DP0_TX2-	EDP_TXD2_N	HDMI_DP0_TXDN0
G37	DP0_TX2+	EDP_TXD2_P	HDMI_DP0_TXDP0
G38	GND	GND	–
G39	PEX_RFU_RX+	PEX_RX1_P	PEX_RX1P
G40	PEX_RFU_RX-	PEX_RX1_N	PEX_RX1N
G41	GND	GND	–
G42	USB_SS1_RX+	PEX_RX3_P	PEX_RX2P
G43	USB_SS1_RX-	PEX_RX3_N	PEX_RX2N
G44	GND	GND	–
G45	SATA_RX+	SATA_RX_P	PEX_RX5P
G46	SATA_RX-	SATA_RX_N	PEX_RX5N
G47	GND	GND	–
G48	GBE_MDI2+	GBE_MDI2_P	–
G49	GBE_MDI2-	GBE_MDI2_N	–
G50	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	Tegra X2 Pin Name
H1	I2S0_LRCLK	AUDIO_I2S_SFSYNC	DAP1_FS
H2	I2S0_SDOUT	AUDIO_I2S_SOUT	DAP1_DOUT
H3	GPIO20_AUD_INT	AUDIO_CDC_IRQ	GPIO_AUD0
H4	DSPK_OUT_DAT	DSPK_OUT_DAT	GPIO_AUD2
H5	I2S2_LRCLK	I2S2_LRCLK	DMIC1_CLK
H6	I2S2_SDOUT	I2S2_SDOUT	DMIC2_CLK
H7	GPIO3_CAM1_RST#	CAM1_RST_L	QSPI_IO0
H8	GPIO2_CAM0_RST#	CAM0_RST_L	QSPI_CS_N
H9	UART3_RX	UART3_RXD	UART4_RX (via mux)
H10	UART3_TX	UART3_TXD	UART4_TX (via mux)
H11	UART0_CTS#	UART0_CTS	UART1_CTS
H12	UART0_TX	UART0_TXD	UART1_TX
H13	GPIO8_ALS_PROX_INT	SAR_TOUT	GPIO_PQ4
H14	SPI2_CLK	SPI2_SCK	GPIO_WAN5
H15	SPI2_MISO	SPI2_MISO	GPIO_WAN6
H16	SDCARD_PWR_EN	SDCARD_VDD_EN	GPIO_EDP3
H17	SDCARD_D1	SDCARD_DAT1_POL	SDMMC1_DAT1
H18	SDCARD_D0	SDCARD_DAT0_POL	SDMMC1_DAT0
H19	GND	GND	–
H20	CSI4_D1-	CON_CSI_E_D1_N	CSI_E_D1_N
H21	CSI4_D1+	CON_CSI_E_D1_P	CSI_E_D1_P
H22	GND	GND	–
H23	CSI2_D1-	CON_CSI_C_D1_N	CSI_C_D1_N
H24	CSI2_D1+	CON_CSI_C_D1_P	CSI_C_D1_P
H25	GND	GND	–
H26	CSI0_D1-	CON_CSI_A_D1_N	CSI_A_D1_N
H27	CSI0_D1+	CON_CSI_A_D1_P	CSI_A_D1_P
H28	GND	GND	–
H29	DSI2_D1+	CON_DSI_B_D1_P	DSI_C_D1_P
H30	DSI2_D1-	CON_DSI_B_D1_N	DSI_C_D1_N
H31	GND	GND	–
H32	DSI0_D1+	CON_DSI_A_D1_P	DSI_A_D1_P
H33	DSI0_D1-	CON_DSI_A_D1_N	DSI_A_D1_N
H34	GND	GND	–
H35	DP0_TX3-	EDP_TXD3_N	HDMI_DP0_TXDN3
H36	DP0_TX3+	EDP_TXD3_P	HDMI_DP0_TXDP3
H37	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	Tegra X2 Pin Name
H38	DP0_TX0-	EDP_TXD0_N	HDMI_DP0_TXDN2
H39	DP0_TX0+	EDP_TXD0_P	HDMI_DP0_TXDP2
H40	GND	GND	–
H41	PEX1_RX+	PEX_RX0_AP_P	PEX_RX0P
H42	PEX1_RX-	PEX_RX0_AP_N	PEX_RX0N
H43	GND	GND	–
H44	PEX0_RX+	PEX_RX4_P	PEX_RX4P
H45	PEX0_RX-	PEX_RX4_N	PEX_RX4N
H46	GND	GND	–
H47	GBE_MDI3+	GBE_MDI3_P	–
H48	GBE_MDI3-	GBE_MDI3_N	–
H49	GND	GND	–
H50	GBE_CTREF (RSVD)	GBE_CTREF	–