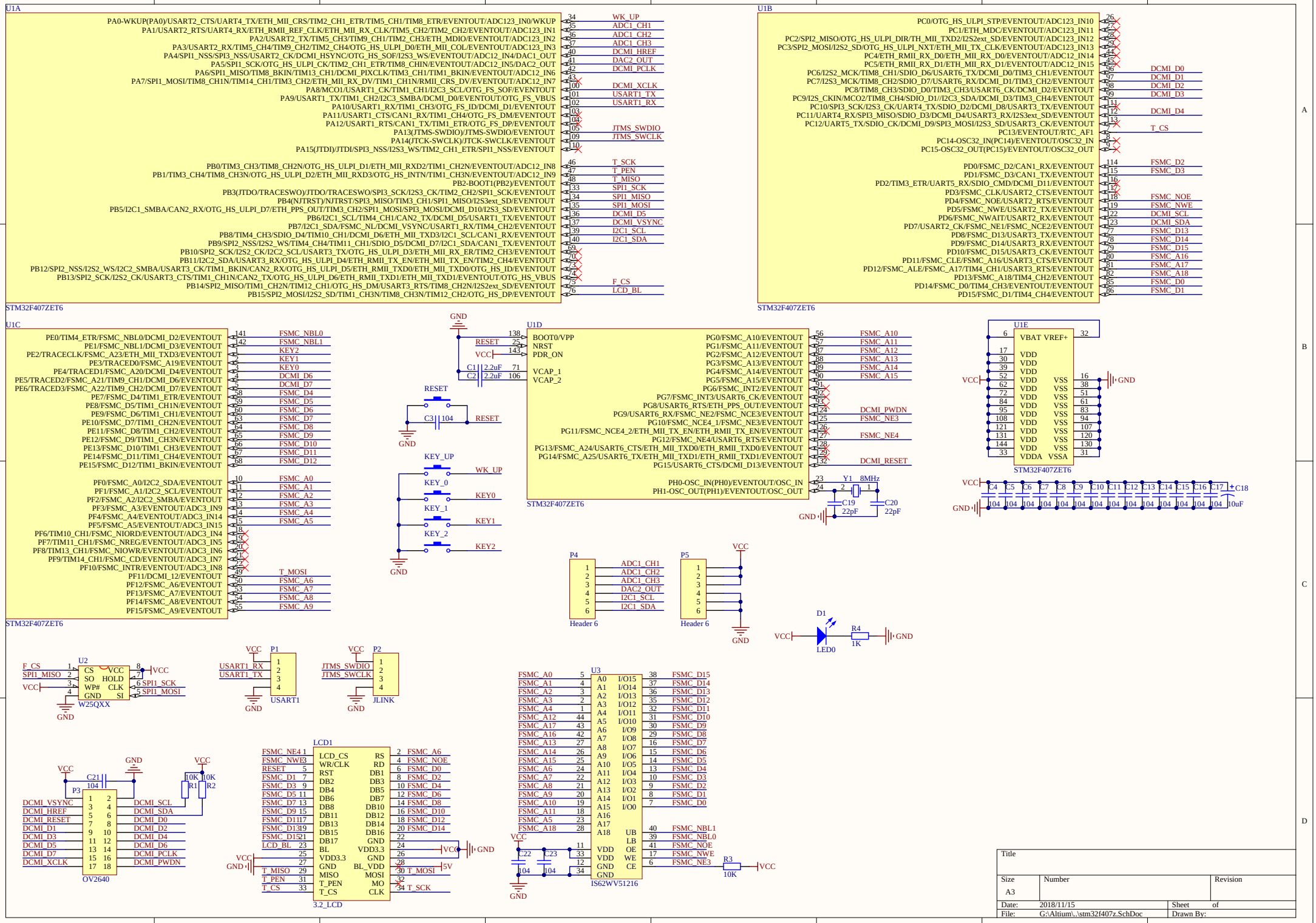
U1A
PA0-WKUP(PA0)/USART2_CTS/UART4_TX/ETH_MII_CRS/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR/EVENTOUT/ADC123_IN0/WKUP
PA1/USART2_RTS/UART4_RX/ETH_RMII_REF_CLK/ETH_MII_RX_CLK/TIM5_CH2/TIM2_CH2/EVENTOUT/ADC123_IN1
PA2/USART2_TX/TIM5_CH3/TIM9_CH1/TIM2_CH3/ETH_MDIO/EVENTOUT/ADC123_IN2
PA3/USART2_RX/TIM5_CH4/TIM9_CH2/TIM2_CH4/OTG_HS_ULPI_D0/ETH_MII_COL/EVENTOUT/ADC123_IN3
PA4/SPI1_NSS/SPI3_NSS/USART2_CK/DCMI_HSYNC/OTG_HS_SOF/I2S3_WS/EVENTOUT/ADC12_IN4/DAC1_OUT
PA5/SPI1_SCK/OTG_HS_ULPI_CK/TIM2_CH1_ETR/TIM8_CHIN/EVENTOUT/ADC12_IN5/DAC2_OUT
PA6/SPI1_MISO/TIM8_BKIN/TIM13_CH1/DCMI_PIXCLK/TIM3_CH1/TIM1_BKIN/EVENTOUT/ADC12_IN6
PA7/SPI1_MOSI/TIM8_CH1N/TIM14_CH1/TIM3_CH2/ETH_MII_RX_DV/TIM1_CH1N/RMII_CRS_DV/EVENTOUT/ADC12_IN7
PA8/MCO1/USART1_CK/TIM1_CH1/I2C3_SCL/OTG_FS_SOF/EVENTOUT
PA9/USART1_TX/TIM1_CH2/I2C3_SMBA/DCMI_D0/EVENTOUT/OTG_FS_VBUS
PA10/USART1_RX/TIM1_CH3/OTG_FS_ID/DCMI_D1/EVENTOUT
PA11/USART1_CTS/CAN1_RX/TIM1_CH4/OTG_FS_DM/EVENTOUT
PA12/USART1_RTS/CAN1_TX/TIM1_ETR/OTG_FS_DP/EVENTOUT
PA13(JTMS-SWDIO)/JTMS-SWDIO/EVENTOUT
PA14(JTCK-SWCLK)/JTCK-SWCLK/EVENTOUT
PA15(JTDI)/JTDI/SPI3_NSS/I2S3_WS/TIM2_CH1_ETR/SPI1_NSS/EVENTOUT
PB0/TIM3_CH3/TIM8_CH2N/OTG_HS_ULPI_D1/ETH_MII_RXD2/TIM1_CH2N/EVENTOUT/ADC12_IN8
PB1/TIM3_CH4/TIM8_CH3N/OTG_HS_ULPI_D2/ETH_MII_RXD3/OTG_HS_INTN/TIM1_CH3N/EVENTOUT/ADC12_IN9
PB2-BOOT1(PB2)/EVENTOUT
PB3(JTDO/TRACESWO)/JTDO/TRACESWO/SPI3_SCK/I2S3_CK/TIM2_CH2/SPI1_SCK/EVENTOUT
PB4(NJTRST)/NJTRST/SPI3_MISO/TIM3_CH1/SPI1_MISO/I2S3ext_SD/EVENTOUT
PB5/I2C1_SMBA/CAN2_RX/OTG_HS_ULPI_D7/ETH_PPS_OUT/TIM3_CH2/SPI1_MOSI/SPI3_MOSI/DCMI_D10/I2S3_SD/EVENTOUT
PB6/I2C1_SCL/TIM4_CH1/CAN2_TX/DCMI_D5/USART1_TX/EVENTOUT
PB7/I2C1_SDA/FSMC_NL/DCMI_VSYNC/USART1_RX/TIM4_CH2/EVENTOUT
PB8/TIM4_CH3/SDIO_D4/TIM10_CH1/DCMI_D6/ETH_MII_TXD3/I2C1_SCL/CAN1_RX/EVENTOUT
PB9/SPI2_NSS/I2S2_WS/TIM4_CH4/TIM11_CH1/SDIO_D5/DCMI_D7/I2C1_SDA/CAN1_TX/EVENTOUT
PB10/SPI2_SCK/I2S2_CK/I2C2_SCL/USART3_TX/OTG_HS_ULPI_D3/ETH_MII_RX_ER/TIM2_CH3/EVENTOUT
PB11/I2C2_SDA/USART3_RX/OTG_HS_ULPI_D4/ETH_RMII_TX_EN/ETH_MII_TX_EN/TIM2_CH4/EVENTOUT
PB12/SPI2_NSS/I2S2_WS/I2C2_SMBA/USART3_CK/TIM1_BKIN/CAN2_RX/OTG_HS_ULPI_D5/ETH_RMII_TXD0/ETH_MII_TXD0/OTG_HS_ID/EVENTOUT
PB13/SPI2_SCK/I2S2_CK/USART3_CTS/TIM1_CH1N/CAN2_TX/OTG_HS_ULPI_D6/ETH_RMII_TXD1/ETH_MII_TXD1/EVENTOUT/OTG_HS_VBUS
PB14/SPI2_MISO/TIM1_CH2N/TIM12_CH1/OTG_HS_DM/USART3_RTS/TIM8_CH2N/I2S2ext_SD/EVENTOUT
PB15/SPI2_MOSI/I2S2_SD/TIM1_CH3N/TIM8_CH3N/TIM12_CH2/OTG_HS_DP/EVENTOUT
WK_UP
ADC1_CH1
ADC1_CH2
ADC1_CH3
DCMI_HREF
DAC2_OUT
DCMI_PCLK
DCMI_XCLK
USART1_TX
USART1_RX
JTMS_SWDIO
JTMS_SWCLK
T_SCK
T_PEN
T_MISO
SPI1_SCK
SPI1_MISO
SPI1_MOSI
DCMI_D5
DCMI_VSYNC
I2C1_SCL
I2C1_SDA
F_CS
LCD_BL
STM32F407ZET6
U1B
PC0/OTG_HS_ULPI_STP/EVENTOUT/ADC123_IN10
PC1/ETH_MDC/EVENTOUT/ADC123_IN11
PC2/SPI2_MISO/OTG_HS_ULPI_DIR/TH_MII_TXD2/I2S2ext_SD/EVENTOUT/ADC123_IN12
PC3/SPI2_MOSI/I2S2_SD/OTG_HS_ULPI_NXT/ETH_MII_TX_CLK/EVENTOUT/ADC123_IN13
PC4/ETH_RMII_RX_D0/ETH_MII_RX_D0/EVENTOUT/ADC12_IN14
PC5/ETH_RMII_RX_D1/ETH_MII_RX_D1/EVENTOUT/ADC12_IN15
PC6/I2S2_MCK/TIM8_CH1/SDIO_D6/USART6_TX/DCMI_D0/TIM3_CH1/EVENTOUT
PC7/I2S3_MCK/TIM8_CH2/SDIO_D7/USART6_RX/DCMI_D1/TIM3_CH2/EVENTOUT
PC8/TIM8_CH3/SDIO_D0/TIM3_CH3/USART6_CK/DCMI_D2/EVENTOUT
PC9/I2S_CKIN/MCO2/TIM8_CH4/SDIO_D1/I2C3_SDA/DCMI_D3/TIM3_CH4/EVENTOUT
PC10/SPI3_SCK/I2S3_CK/UART4_TX/SDIO_D2/DCMI_D8/USART3_TX/EVENTOUT
PC11/UART4_RX/SPI3_MISO/SDIO_D3/DCMI_D4/USART3_RX/I2S3ext_SD/EVENTOUT
PC12/UART5_TX/SDIO_CK/DCMI_D9/SPI3_MOSI/I2S3_SD/USART3_CK/EVENTOUT
PC13/EVENTOUT/RTC_AF1
PC14-OSC32_IN(PC14)/EVENTOUT/OSC32_IN
PC15-OSC32_OUT(PC15)/EVENTOUT/OSC32_OUT
PD0/FSMC_D2/CAN1_RX/EVENTOUT
PD1/FSMC_D3/CAN1_TX/EVENTOUT
PD2/TIM3_ETR/UART5_RX/SDIO_CMD/DCMI_D11/EVENTOUT
PD3/FSMC_CLK/USART2_CTS/EVENTOUT
PD4/FSMC_NOE/USART2_RTS/EVENTOUT
PD5/FSMC_NWE/USART2_TX/EVENTOUT
PD6/FSMC_NWAIT/USART2_RX/EVENTOUT
PD7/USART2_CK/FSMC_NE1/FSMC_NCE2/EVENTOUT
PD8/FSMC_D13/USART3_TX/EVENTOUT
PD9/FSMC_D14/USART3_RX/EVENTOUT
PD10/FSMC_D15/USART3_CK/EVENTOUT
PD11/FSMC_CLE/FSMC_A16/USART3_CTS/EVENTOUT
PD12/FSMC_ALE/FSMC_A17/TIM4_CH1/USART3_RTS/EVENTOUT
PD13/FSMC_A18/TIM4_CH2/EVENTOUT
PD14/FSMC_D0/TIM4_CH3/EVENTOUT
PD15/FSMC_D1/TIM4_CH4/EVENTOUT
DCMI_D0
DCMI_D1
DCMI_D2
DCMI_D3
DCMI_D4
T_CS
FSMC_D2
FSMC_D3
FSMC_NOE
FSMC_NWE
DCMI_SCL
DCMI_SDA
FSMC_D13
FSMC_D14
FSMC_D15
FSMC_A16
FSMC_A17
FSMC_A18
FSMC_D0
FSMC_D1
STM32F407ZET6
U1C
PE0/TIM4_ETR/FSMC_NBL0/DCMI_D2/EVENTOUT
PE1/FSMC_NBL1/DCMI_D3/EVENTOUT
PE2/TRACECLK/FSMC_A23/ETH_MII_TXD3/EVENTOUT
PE3/TRACED0/FSMC_A19/EVENTOUT
PE4/TRACED1/FSMC_A20/DCMI_D4/EVENTOUT
PE5/TRACED2/FSMC_A21/TIM9_CH1/DCMI_D6/EVENTOUT
PE6/TRACED3/FSMC_A22/TIM9_CH2/DCMI_D7/EVENTOUT
PE7/FSMC_D4/TIM1_ETR/EVENTOUT
PE8/FSMC_D5/TIM1_CH1N/EVENTOUT
PE9/FSMC_D6/TIM1_CH1/EVENTOUT
PE10/FSMC_D7/TIM1_CH2N/EVENTOUT
PE11/FSMC_D8/TIM1_CH2/EVENTOUT
PE12/FSMC_D9/TIM1_CH3N/EVENTOUT
PE13/FSMC_D10/TIM1_CH3/EVENTOUT
PE14/FSMC_D11/TIM1_CH4/EVENTOUT
PE15/FSMC_D12/TIM1_BKIN/EVENTOUT
PF0/FSMC_A0/I2C2_SDA/EVENTOUT
PF1/FSMC_A1/I2C2_SCL/EVENTOUT
PF2/FSMC_A2/I2C2_SMBA/EVENTOUT
PF3/FSMC_A3/EVENTOUT/ADC3_IN9
PF4/FSMC_A4/EVENTOUT/ADC3_IN14
PF5/FSMC_A5/EVENTOUT/ADC3_IN15
PF6/TIM10_CH1/FSMC_NIORD/EVENTOUT/ADC3_IN4
PF7/TIM11_CH1/FSMC_NREG/EVENTOUT/ADC3_IN5
PF8/TIM13_CH1/FSMC_NIOWR/EVENTOUT/ADC3_IN6
PF9/TIM14_CH1/FSMC_CD/EVENTOUT/ADC3_IN7
PF10/FSMC_INTR/EVENTOUT/ADC3_IN8
PF11/DCMI_12/EVENTOUT
PF12/FSMC_A6/EVENTOUT
PF13/FSMC_A7/EVENTOUT
PF14/FSMC_A8/EVENTOUT
PF15/FSMC_A9/EVENTOUT
FSMC_NBL0
FSMC_NBL1
KEY2
KEY1
KEY0
DCMI_D6
DCMI_D7
FSMC_D4
FSMC_D5
FSMC_D6
FSMC_D7
FSMC_D8
FSMC_D9
FSMC_D10
FSMC_D11
FSMC_D12
FSMC_A0
FSMC_A1
FSMC_A2
FSMC_A3
FSMC_A4
FSMC_A5
T_MOSI
FSMC_A6
FSMC_A7
FSMC_A8
FSMC_A9
STM32F407ZET6
U1D
BOOT0/VPP
NRST
PDR_ON
VCAP_1
VCAP_2
PG0/FSMC_A10/EVENTOUT
PG1/FSMC_A11/EVENTOUT
PG2/FSMC_A12/EVENTOUT
PG3/FSMC_A13/EVENTOUT
PG4/FSMC_A14/EVENTOUT
PG5/FSMC_A15/EVENTOUT
PG6/FSMC_INT2/EVENTOUT
PG7/FSMC_INT3/USART6_CK/EVENTOUT
PG8/USART6_RTS/ETH_PPS_OUT/EVENTOUT
PG9/USART6_RX/FSMC_NE2/FSMC_NCE3/EVENTOUT
PG10/FSMC_NCE4_1/FSMC_NE3/EVENTOUT
PG11/FSMC_NCE4_2/ETH_MII_TX_EN/ETH_RMII_TX_EN/EVENTOUT
PG12/FSMC_NE4/USART6_RTS/EVENTOUT
PG13/FSMC_A24/USART6_CTS/ETH_MII_TXD0/ETH_RMII_TXD0/EVENTOUT
PG14/FSMC_A25/USART6_TX/ETH_MII_TXD1/ETH_RMII_TXD1/EVENTOUT
PG15/USART6_CTS/DCMI_D13/EVENTOUT
PH0-OSC_IN(PH0)/EVENTOUT/OSC_IN
PH1-OSC_OUT(PH1)/EVENTOUT/OSC_OUT
FSMC_A10
FSMC_A11
FSMC_A12
FSMC_A13
FSMC_A14
FSMC_A15
DCMI_PWDN
FSMC_NE3
FSMC_NE4
DCMI_RESET
Y1 8MHz
C19 22pF
C20 22pF
STM32F407ZET6
U1E
VBAT VREF+
VDD VSS VDDA VSSA
STM32F407ZET6
C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18
104 10uF
RESET
C1 2.2uF
C2 2.2uF
C3 104
KEY_UP
KEY_0
KEY_1
KEY_2
WK_UP
P4
ADC1_CH1
ADC1_CH2
ADC1_CH3
DAC2_OUT
I2C1_SCL
I2C1_SDA
Header 6
P5
Header 6
D1
LED0
R4 1K
U2
CS SO WP# GND VCC HOLD CLK SI
F_CS
SPI1_MISO
SPI1_SCK
SPI1_MOSI
W25QXX
P1
USART1_RX
USART1_TX
USART1
P2
JTMS_SWDIO
JTMS_SWCLK
JLINK
P3
C21 104
10K R1
10K R2
DCMI_VSYNC
DCMI_HREF
DCMI_RESET
DCMI_D1
DCMI_D3
DCMI_D5
DCMI_D7
DCMI_XCLK
DCMI_SCL
DCMI_SDA
DCMI_D0
DCMI_D2
DCMI_D4
DCMI_D6
DCMI_PCLK
DCMI_PWDN
OV2640
LCD1
LCD_CS WR/CLK RST DB2 DB4 DB6 DB8 DB11 DB13 DB15 DB17 BL VDD3.3 GND MISO T_PEN T_CS
RS RD DB1 DB3 DB5 DB7 DB10 DB12 DB14 DB16 GND VDD3.3 GND BL_VDD MOSI MO CLK
FSMC_NE4
FSMC_NWE
RESET
FSMC_D1
FSMC_D3
FSMC_D5
FSMC_D7
FSMC_D9
FSMC_D11
FSMC_D13
FSMC_D15
LCD_BL
T_MISO
T_PEN
T_CS
FSMC_A6
FSMC_NOE
FSMC_D0
FSMC_D2
FSMC_D4
FSMC_D6
FSMC_D8
FSMC_D10
FSMC_D12
FSMC_D14
T_MOSI
T_SCK
5V
3.2_LCD
U3
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 VDD VDD GND GND
I/O15 I/O14 I/O13 I/O12 I/O11 I/O10 I/O9 I/O8 I/O7 I/O6 I/O5 I/O4 I/O3 I/O2 I/O1 I/O0 UB LB OE WE CE
FSMC_A0
FSMC_A1
FSMC_A2
FSMC_A3
FSMC_A4
FSMC_A12
FSMC_A17
FSMC_A16
FSMC_A13
FSMC_A14
FSMC_A15
FSMC_A6
FSMC_A7
FSMC_A8
FSMC_A9
FSMC_A10
FSMC_A11
FSMC_A5
FSMC_A18
FSMC_D15
FSMC_D14
FSMC_D13
FSMC_D12
FSMC_D11
FSMC_D10
FSMC_D9
FSMC_D8
FSMC_D7
FSMC_D6
FSMC_D5
FSMC_D4
FSMC_D3
FSMC_D2
FSMC_D1
FSMC_D0
FSMC_NBL1
FSMC_NBL0
FSMC_NOE
FSMC_NWE
FSMC_NE3
C22 104
C23 104
R3 10K
IS62WV51216
Title
Size A3
Number
Revision
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