Velicharla
Gokul Kumar

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As an experienced Front-End Chip Design Engineer, I specialize in digital circuit design and development for FPGA and ASIC projects. I have designed and implemented efficient RTL solutions, focusing on building robust, scalable hardware architectures that meet project goals.

Skills

- **HDL** - *Proficient in Verilog, SystemVerilog.*
- **Tools** - *Skilled in Vivado, Vitis HLS, Vitis, Quartus, QuestaSim and MATLAB.*
- **RTL Design***: Familiar with design trade-offs related to throughput, latency, and power optimization; skilled in linting for code quality*
- **Timing Analysis & CDC** - *Knowledge of Static Timing Analysis (STA), constraint development, Clock Domain Crossing (CDC) techniques, and clock synchronization strategies*
- **SoC Architecture** - *Strong understanding of ARM-based SoC architectures, including CPU/memory subsystems, interconnects, boot processes, and board bring-up*
- **Interconnect Protocols** - *Proficient in AXI-Stream; familiar with AXI4, AXI4-Lite, and APB protocols.*
- **SerDes** - *Design Experience with Ethernet IP and Ethernet protocol domain.*
- **Interface IPs** - *Design Experience with DDR4 controllers, DMA and related interface IP blocks.*
- **Scripting** - *Skilled in python, Shell Scripting.*
- **Debugging & Problem Solving** - *Strong debugging skills and a collaborative team player.*

Experience

- 5G Testbed R&D Lab, Indian Institute of Technology Hyderabad — *TS*, India
  RTL and SoC System Design Engineer — *Dec 2023 - present*
  - Integrated hardware modules into the Ethernet debug framework, contributing to the micro-architecture for testing 25G SFP link between RU and DU in ORAN Massive MIMO system.
  - Developed fundamental hardware modules for the 5G NR UE PHY Baseband subsystem, with a focus on the Synchronization Signal Block (SSB) channel.
  - Designed an automated testing framework to validate 1,000 unique test dumps for the SSB.
  - Implemented moderate-level C code for L1 control on the PS, ensuring seamless handoff and alignment with hardware requirements by working closely with cross-functional teams.

- 5G Testbed R&D Lab, Indian Institute of Technology Hyderabad — *TS*, India
  Research Project Intern — *Dec 2022 - Nov 2023*
  - Assisted in developing fundamental DSP modules with fixed-point implementation in HDL, focusing on synthesis and optimization.
  - Reviewed and adhered to user guides for soft-core IPs, ensuring proper configuration.
  - Developed Make, Tcl, and Python scripts to automate EDA tool flows and performed unit testing with Cocotb for developer sanity checks.
  - Integrated Jenkins with Docker container agents to enable scalable and automated CI/CD pipelines for build and testing processes.

- Indian Institute of Technology Hyderabad — *TS*, India
  Future Wireless Communications Intern — *Aug 2022 - Nov 2022*
  - Designed and implemented basic DSP modules using high-level synthesis (HLS).
  - Applied matrix analysis and optimization techniques (cvxpy, gradient ascent, and descent) in Python.
  - Developed digital logics with platformIO, Arduino, and IDF frameworks in Verilog, Assembly, and Avr-gcc.

Education

- Vignan's Foundation for Science Technology and Research — AP, India
  B.Tech in Electronics and Communication Engineering; — *2019 – 2023*
  CGPA: 9.52/10.0
- Sri Chaitanya jr. College — AP, India
  MPC; CGPA: *9.88/10.0* — *2017 – 2019*
- Sri Chaitanya Techno School — AP, India
  SSC; GPA: *9.8/10.0* — *2017*

Academic Projects

- **Elderly Fall Detection and Location Tracing System**:
  Duration: *4-months*
- **IoT Based Smart Water Governing System**:
  Duration: 4-months

Volunteer Experience

- IEEE Student Branch Secretary. *-6 Months*
- Class Representative *-6 Months*
- Student Coordinator *-3 Days*
  -CIRH International Conference.

Certifications

- Problem Solving Through Programming in C,
  NPTEL
- Programming, Data Structures and Algorithms Using
  Python, NPTEL
- Programming For Everybody (Getting Started with
  Python), Coursera
- Programming In Java,
  NPTEL
- Business English Certificate Vantage
  Overall score:159 CEFR Level: B1
- DevOps and Building Automation using
  Python, Coursera

Awards & Honors

- **Merit Certificate**: Certificate of academic excellence (2020,2021)

Extra-Curricular Activities

- **Sports**: Badminton, Volleyball