Velicharla
Gokul Kumar

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Education

- Vignan's Foundation for Science Technology and Research — AP, India — *2019 – 2023*
  B.Tech in Electronics and Communication Engineering; CGPA: 9.52/10.0
- Sri Chaitanya jr. College — AP, India — *2017 – 2019*
  MPC; CGPA: 9.88/10.0
- Sri Chaitanya Techno School — AP, India — *2017*
  SSC; GPA: 9.8/10.0

Skills

- HDL - *Proficient in Verilog, SystemVerilog.*
- Tools - *Skilled in Vivado, Vitis HLS, Vitis, Quartus, QuestaSim and MATLAB.*
- RTL Design*: Familiar with design trade-offs related to throughput, latency, and power optimization; skilled in linting for code quality*
- Timing Analysis & CDC - *Familiar with Static Timing Analysis (STA), constraint development, clock domain crossing (CDC) techniques, and clock synchronization strategies.*
- SoC Architecture - *Familiar with ARM-based SoC architectures, including boot processes and board bring up.*
- Interconnect Protocols - *Proficient in AXI-Stream; familiar with AXI4, AXI4-Lite, and APB protocols.*

Experience

- 5G Testbed R&D Lab, Indian Institute of Technology Hyderabad — *TS*, India
  RTL and SoC System Design Engineer — *Dec 2023 - present*
  - Developed fundamental hardware modules for the 5G NR PHY Baseband subsystem, with a focus on the Synchronization Signal Block (SSB) channel.
  - Implemented moderate-level C code for L1 control on the PS, ensuring seamless handoff and alignment with hardware requirements.
  - Worked with AXI bridges and interconnects between PS and PL, specifically targeting Intel FPGA.
  - Designed an automated testing framework to validate 1,000 unique test dumps for the SSB.
- 5G Testbed R&D Lab, Indian Institute of Technology Hyderabad — *TS*, India
  Research Project Intern — *Dec 2022 - Nov 2023*
  - Assisted in developing fundamental DSP modules with fixed-point implementation in HDL, focusing on synthesis and optimization.
  - Reviewed and adhered to user guides for soft-core IPs, ensuring proper configuration.
  - Contributed to the development of Make, Tcl, and Python scripts to automate and streamline EDA tool compilation processes.
  - Integrated Jenkins with Docker container agents to enable scalable and automated CI/CD pipelines for build and testing processes.
- Indian Institute of Technology Hyderabad — *TS*, India
  Future Wireless Communications Intern — *Aug 2022 - Nov 2022*
  - Designed and implemented basic DSP modules using Vivado, Vitis HLS, and MATLAB for high-level synthesis.
  - Applied matrix analysis and optimization techniques (cvxpy, gradient ascent, and descent) in Python.
  - Developed digital logics with platformIO, Arduino, and IDF frameworks in Verilog, Assembly, and Avr-gcc.

Academic Projects

- **Elderly Fall Detection and Location Tracing System**:
  Duration: *4-months*
- **IoT Based Smart Water Governing System**:
  Duration: 4-months

Volunteer Experience

- IEEE Student Branch Secretary. *-6 Months*
- Class Representative *-6 Months*
- Student Coordinator *-3 Days*
  -CIRH International Conference.

Certifications

- Problem Solving Through Programming in C,
  NPTEL
- Programming, Data Structures and Algorithms Using
  Python, NPTEL
- Programming For Everybody (Getting Started with
  Python), Coursera
- Programming In Java,
  NPTEL
- Business English Certificate Vantage
  Overall score:159 CEFR Level: B1
- DevOps and Building Automation using
  Python, Coursera

Awards & Honors

- **Merit Certificate**: Certificate of academic excellence (2020,2021)

Extra-Curricular Activities

- **Sports**: Volleyball, Badminton