# Velicharla
# Gokul Kumar

| +91 9573465257 | gokul.velicharla@gmail.com | Hyderabad


As an experienced Front-End Chip Design Engineer, I specialize in digital circuit design and development for FPGA and ASIC projects. I have designed and implemented efficient RTL solutions, focusing on building robust, scalable hardware architectures that meet project goals.

## Skills

- **HDL** - Proficient in Verilog and SystemVerilog.
- **Tools & Simulation** - Experienced with Vivado, Vitis, Vitis HLS, Quartus, QuestaSim, and MATLAB.
- **RTL Design** - Familiar with design trade-offs related to throughput, latency, and power optimization; skilled in code linting and quality checks.
- **Timing & CDC** - Solid understanding of Static Timing Analysis (STA), constraint development, Clock Domain Crossing (CDC) techniques, and synchronization strategies.
- **SoC Architecture** - Familiar with ARM-based SoC designs, including CPU/memory subsystems, interconnects, boot processes, and board bring-up.
- **Protocols & Interfaces** - Hands on experience with AXI4, APB and AHB protocols.
- **SerDes** - Design Experience with Ethernet IP and Ethernet protocol domain.
- **Scripting & Automation** - Proficient in Python and Shell scripting; experienced with automation tools like Jenkins and Docker.
- **Debugging & Problem Solving** - Strong debugging skills and a collaborative team player.

## Experience

- 5G Testbed R&D Lab, Indian Institute of Technology Hyderabad — *TS*, India
  *RTL and SoC System Design Engineer* — *Dec 2023 - present*
  - Integrated hardware modules into the Ethernet debug framework, contributing to the micro-architecture for testing 25G SFP Fronthaul link between RU and DU in ORAN Massive MIMO system.
  - Designed a packet client to separate control-plane (C-plane) and user-plane (U-plane) data from serial input received via the Ethernet IP, and route it to the ULPI IP.
  - Developed and optimized fundamental hardware modules for the 5G NR UE PHY Baseband subsystem, with a focus on the Synchronization Signal Block (SSB) channel.
- 5G Testbed R&D Lab, Indian Institute of Technology Hyderabad — *TS*, India
  *Research Project Trainee* — *Dec 2022 - Nov 2023*
  - Assisted in developing fundamental DSP modules with fixed-point implementation in HDL, focusing on synthesis and optimization and code linting.
  - Reviewed and adhered to user guides for soft-core IPs, ensuring proper configuration.
  - Integrated interface IPs such as DDR4 controllers and DMA to support required system functionality.
  - Developed Make, Tcl, and Python scripts to automate EDA tool flows and performed unit testing with Cocotb for developer sanity checks.
- Indian Institute of Technology Hyderabad — *TS*, India
  *Future Wireless Communications Intern* — *Aug 2022 - Nov 2022*
  - Designed and implemented basic DSP modules using high-level synthesis (HLS).
  - Applied matrix analysis and optimization techniques (cvxpy, gradient ascent, and descent) in Python.
  - Developed digital logics with platformIO, Arduino, and IDF frameworks in Verilog, Assembly, and Avr-gcc.

## Education

- Vignan's Foundation for Science Technology and Research — AP, India
  *B.Tech in Electronics and Communication Engineering;* — *2019 – 2023*
  *CGPA: 9.52/10.0*
- Sri Chaitanya jr. College — AP, India
  *MPC;* CGPA: *9.88/10.0* — *2017 – 2019*
- Sri Chaitanya Techno School — AP, India
  *SSC;* GPA: *9.8/10.0* — *2017*

## Academic Projects & Personal Projects

- **Memory Tester System Design:**
  *Duration***:** *2-months*
- **Elderly Fall Detection and Location Tracing System**:
  *Duration*: *4-months*
- **IoT Based Smart Water Governing System**:
  *Duration: 4-months*

## Volunteer Experience

- IEEE Student Branch Secretary. *-6 Months*
- Class Representative *-6 Months*
- Student Coordinator *-3 Days*
  *-CIRH International Conference.*

## Certifications

- Problem Solving Through Programming in C,
  NPTEL
- Programming, Data Structures and Algorithms Using
  Python, NPTEL
- Programming For Everybody (Getting Started with
  Python), Coursera
- Programming In Java,
  NPTEL
- Business English Certificate Vantage
  Overall score:159 CEFR Level: B1
- DevOps and Building Automation using
  Python, Coursera

## Awards & Honors

- **Merit Certificate**: Certificate of academic excellence (2020,2021)

## Extra-Curricular Activities

- **Sports**: Badminton, Volleyball