Velicharla
Gokul Kumar

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Education

- Vignan's Foundation for Science Technology and Research — AP, India
  2019 – 2023
  B.Tech in Electronics and Communication Engineering; CGPA: 9.52/10.0
- Sri Chaitanya jr. College — AP, India
  2017 – 2019
  MPC; CGPA: 9.88/10.0
- Sri Chaitanya Techno School — AP, India
  2017
  SSC; GPA: 9.8/10.0

Skills

- HDL - *Proficient in Verilog, SystemVerilog.*
- Tools - *Skilled in Vivado, Vivado HLS, Vitis, Quartus, QuestaSim and MATLAB.*
- RTL Design - *Strong understanding of design trade-offs, including throughput, latency, area, and power.*
- *Timing Analysis & Linting - In-depth knowledge of Static Timing Analysis (STA), constraint development, linting.*
- *Clocking & CDC - Expertise in clock domain crossing (CDC) techniques, and clock synchronization strategies.*
- SoC Architecture - *Familiar with ARM-based SoC architectures, including boot processes and board bring up.*
- Interconnect Protocols - *Proficient in AXI4, AXI4-Lite, AXI -Stream.*
- Debugging & Problem Solving - *Strong analytical and debugging skills.*

Experience

- 5G Testbed R&D Lab, Indian Institute of Technology Hyderabad — *TS*, India
  RTL and SoC System Design Engineer — *Dec 2023 - present*
  - Developed fundamental hardware modules for the 5G NR PHY Baseband subsystem, focusing on the Synchronization Signal Block (SSB) channel.
  - Moderate-level C code developing for L1 controlling on PS, ensuring smooth hand-off and alignment with hardware requirements.
  - Worked with AXI bridges and interconnects between PS and PL, specifically in Intel FPGA.
  - Designed an automated framework to conduct testing for 1,000 different test dumps in the SSB channel.

- 5G Testbed R&D Lab, Indian Institute of Technology Hyderabad — *TS*, India
  Research Project Intern — *Dec 2022 - Nov 2023*
  - Reviewed and adhered to user guides for soft-core IPs, ensuring effective configuration.
  - Digital Design - *Fixed-point implementation of signal processing techniques in HDL.*
  - Jenkins, Docker - *integrating Jenkins with docker container agents for build & Automated Testing.*
  - Scripting - *Make, Tcl, Shell, Python wrappers for the compiling flow of EDA tools.*

- Indian Institute of Technology Hyderabad — *TS*, India
  Future Wireless Communications Intern — *Aug 2022 - Nov 2022*
  - Synthesis, High level synthesis - *Digital design of basic communication modules using Vivado, Vitis, Vitis HLS, MATLAB*
  - Communications, Signal processing, Random variables -*basics.*
  - Configuring FPGA, ARM using Termux - *on Vaman board.*
  - Matrix Analysis in python, Optimization - *using cvxpy, gradient ascent & descent.*
  - *Digital Design -using platformIO, Arduino, IDF frameworks in Assembly, Avr-gcc level on Arduino board.*

Academic Projects

- **Elderly Fall Detection and Location Tracing System**:
  Duration: *4-months*
- **IoT Based Smart Water Governing System**:
  Duration: 4-months

Volunteer Experience

- IEEE Student Branch Secretary. *-6 Months*
- Class Representative *-6 Months*
- Student Coordinator *-3 Days*
  -CIRH International Conference.

Certifications

- Problem Solving Through Programming in C,
  NPTEL
- Programming, Data Structures and Algorithms Using
  Python, NPTEL
- Programming For Everybody (Getting Started with
  Python), Coursera
- Programming In Java,
  NPTEL
- Business English Certificate Vantage
  Overall score:159 CEFR Level: B1
- DevOps and Building Automation using
  Python, Coursera

Awards & Honors

- **Merit Certificate**: Certificate of academic excellence (2020,2021)

Extra-Curricular Activities

- **Sports**: Volleyball, Badminton