V.GOKUL KUMAR
Wisig Trainee
Indian Institute of Technology Hyderabad
Email: velicharla@outlook.com

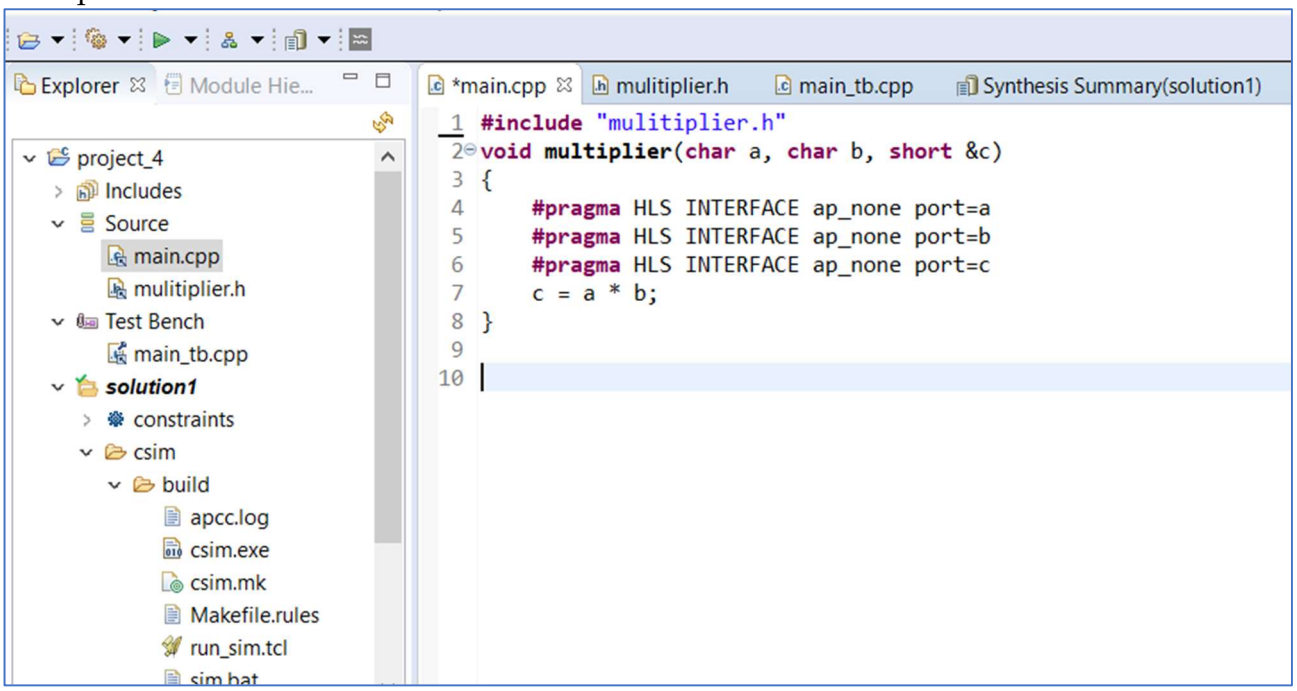
Date:15-03-2023

Hls ASSIGNMENT-1

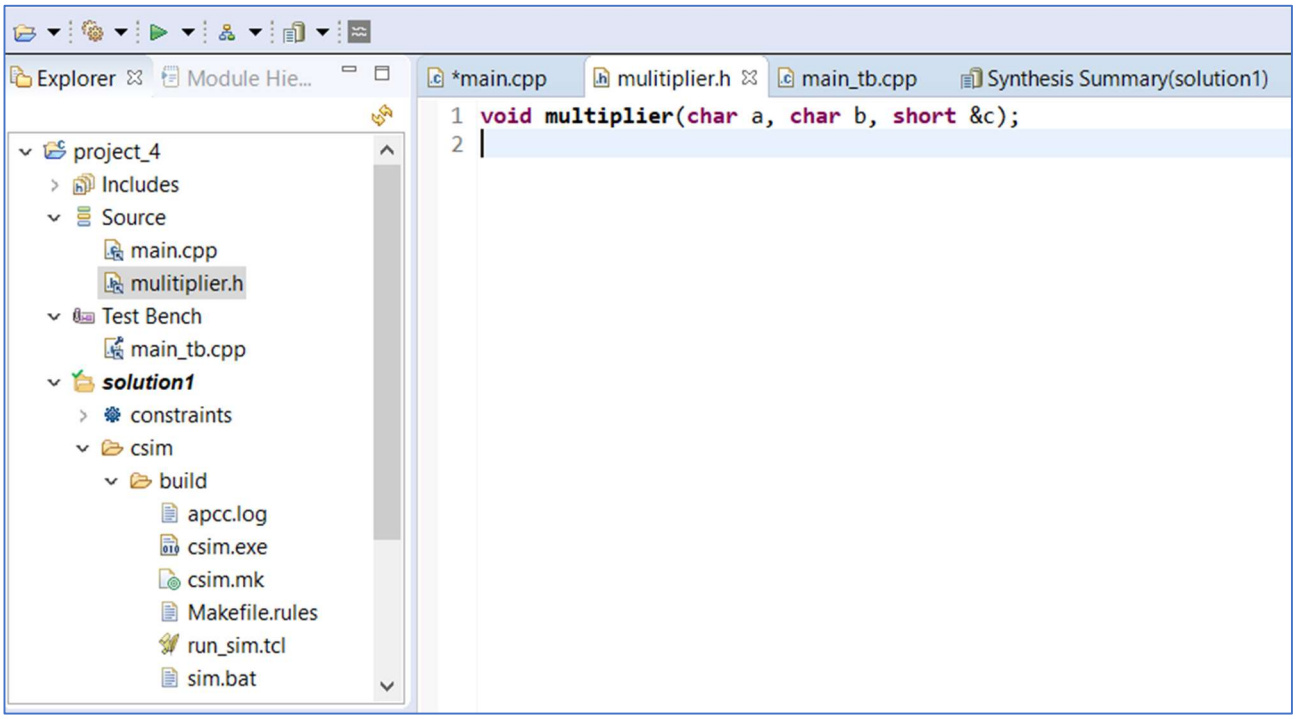
Design an 8bit * 8bit multiplier using HLS. There will be two 8bit inputs (use char data type) and one 16bit output (use short data type). Use ap_none interface for the port interfaces. Write an HLS testbench to verify the output of the design. Pass 10 pair of input values to design and collect the output, and display inputs and outputs as part of the testbench. Verify if your design is working using C simulation first. Run HLS synthesis. Now, verify the design again using C/RTL co-simulation. Report your design and tb code, C simulation printed outputs, HLS resource consumption, HLS timing report, and C/RTL cosimulation printed outputs and report, in one document

Design:

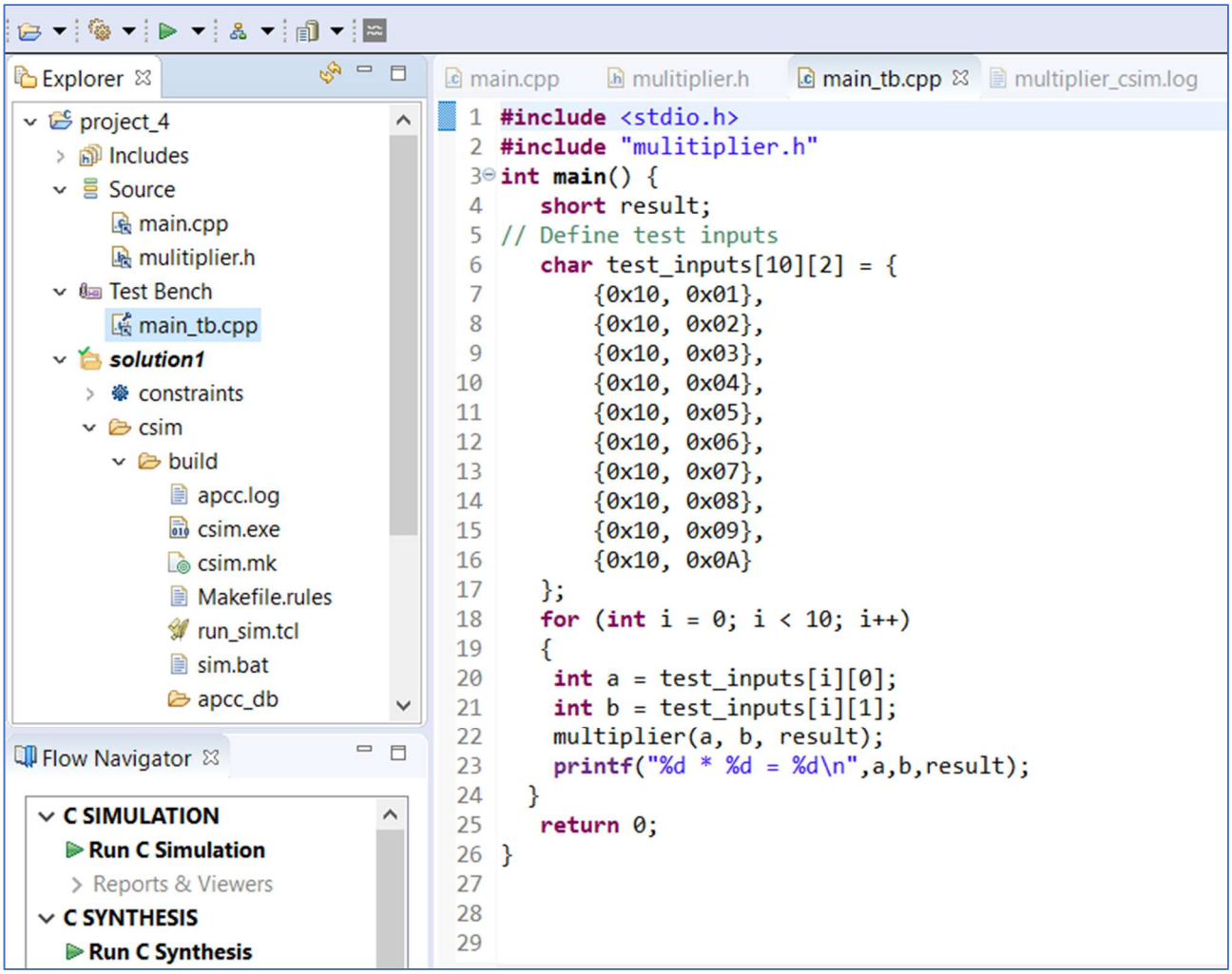
Multiplier function:



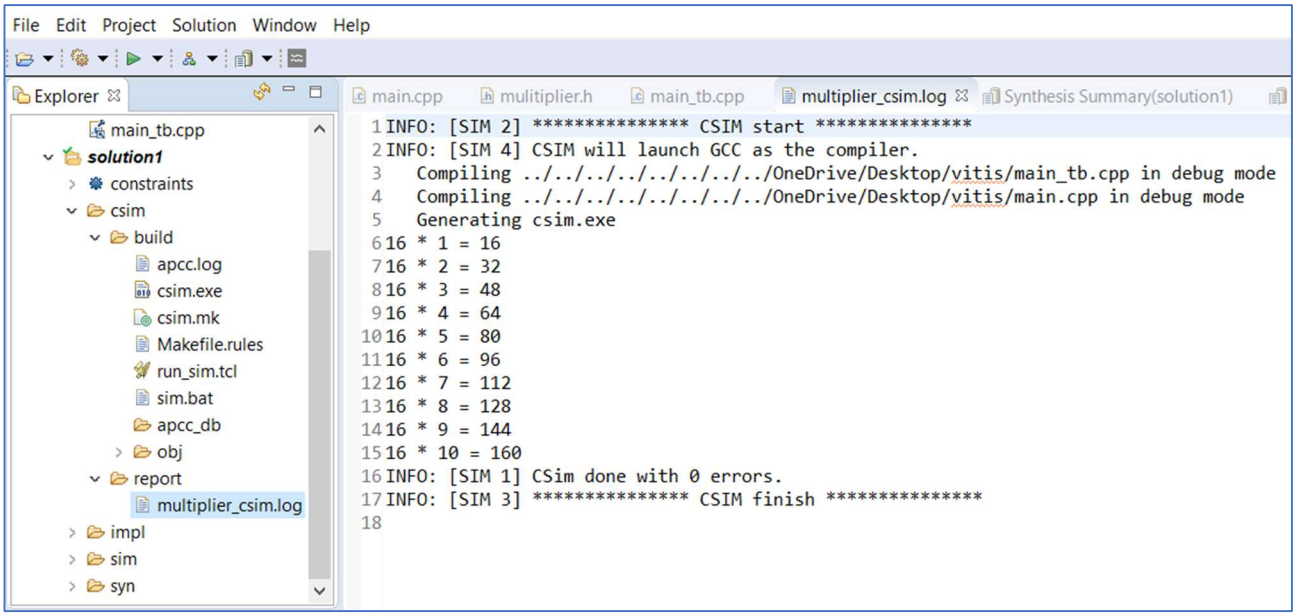
Header file:



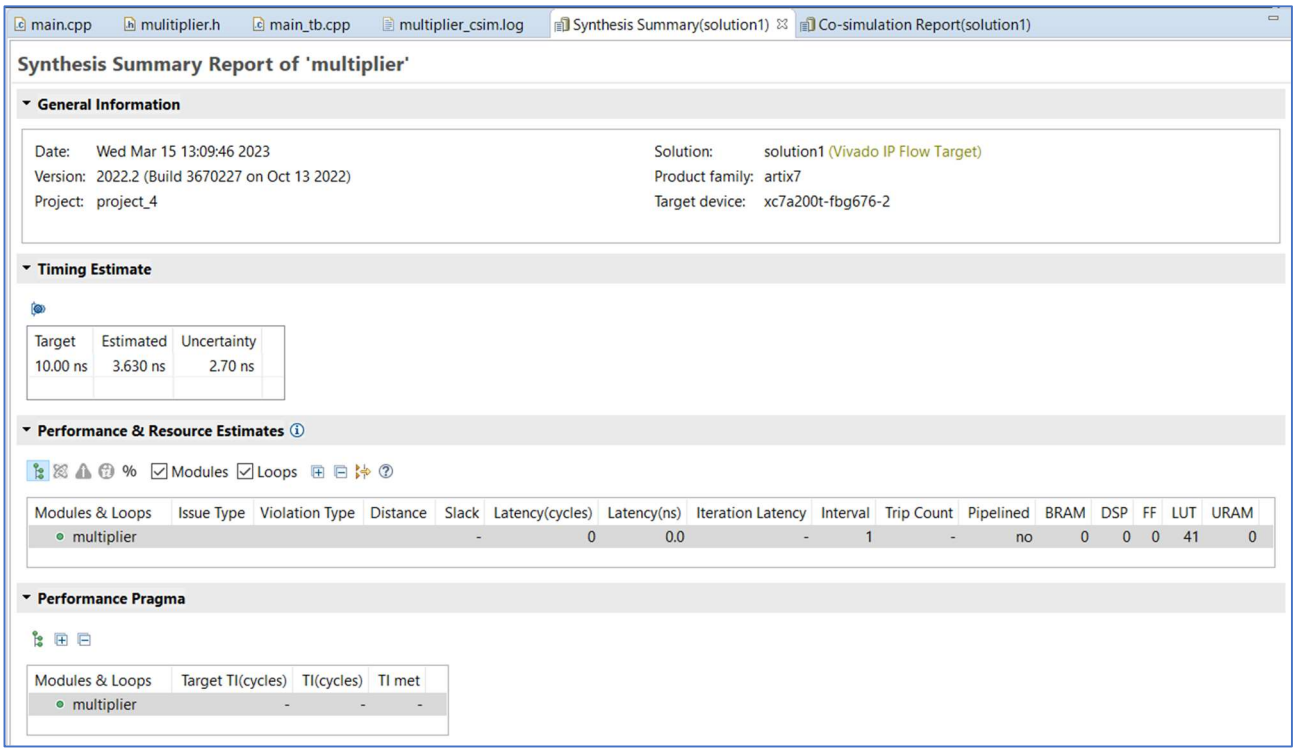
Test Bench:



C simulation printed output:



Synthesis Report:



HW Interfaces

Other Ports

Interface	Mode	Bitwidth
a	ap_none	8
b	ap_none	8
c	ap_none	16

TOP LEVEL CONTROL

Interface	Type	Ports
ap_ctrl	ap_ctrl_hs	ap_done ap_idle ap_ready ap_start

SW I/O Information

Top Function Arguments

Argument	Direction	Datatype
a	in	char
b	in	char
c	out	short&

SW-to-HW Mapping

Argument	HW Interface	HW Type
a	a	port
b	b	port
c	c	port

Pragma Report

Valid Pragma Syntax

Bind Op Report

No filter settings

Name	DSP	Pragma	Variable	Op	Impl	Latency
multiplier	-					
mul_8s_8s_16_1_1_U1	-		mul_ln7	mul	auto	0

No user config_op information

Bind Storage Report

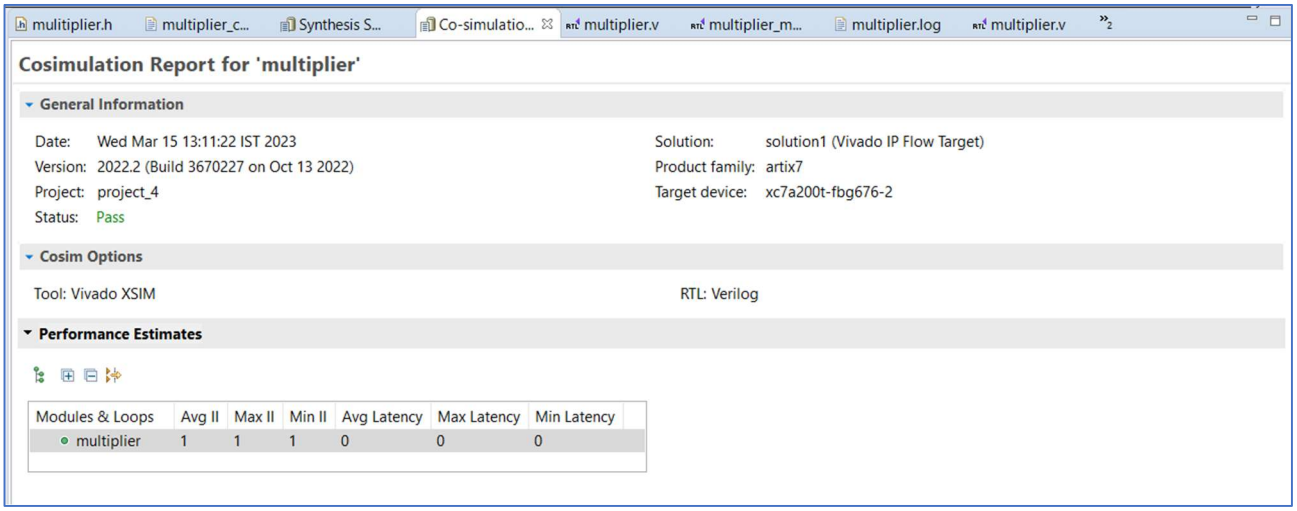
No bind storage, config_storage information

Cosimulation printed output:

```
## quit
INFO: [Common 17-206] Exiting xsim at Wed Mar 15 13:11:17 2023...
16 * 1 = 16
16 * 2 = 32
16 * 3 = 48
16 * 4 = 64
16 * 5 = 80
16 * 6 = 96
16 * 7 = 112
16 * 8 = 128
16 * 9 = 144
16 * 10 = 160
INFO: [COSIM-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [COSIM-210] Design is translated to an combinational logic. II and Latency will be marked as all 0.

```

Cosimulation Report:



Github:

https://github.com/velicharlagokulkumar/vitis-hls/tree/main/project_4