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RTL ASSIGNMENT-1

Design an 8-bit down counter. The count value is loaded from 'in' input on a positive clock edge when 'latch' input is high. Count value is decremented by 1 on a positive clock edge while 'dec' input is high. Stop decrementing at 0 and raise 'zero' flag output active high whenever count value is 0. 'latch' input has priority over 'dec' input. Whenever 'divide-by-two' input is high and 'latch' input is low and 'dec' input is low (both dec and divide-by-two will never be high at the same time), divide the current contents of the counter by 2.

Module code:

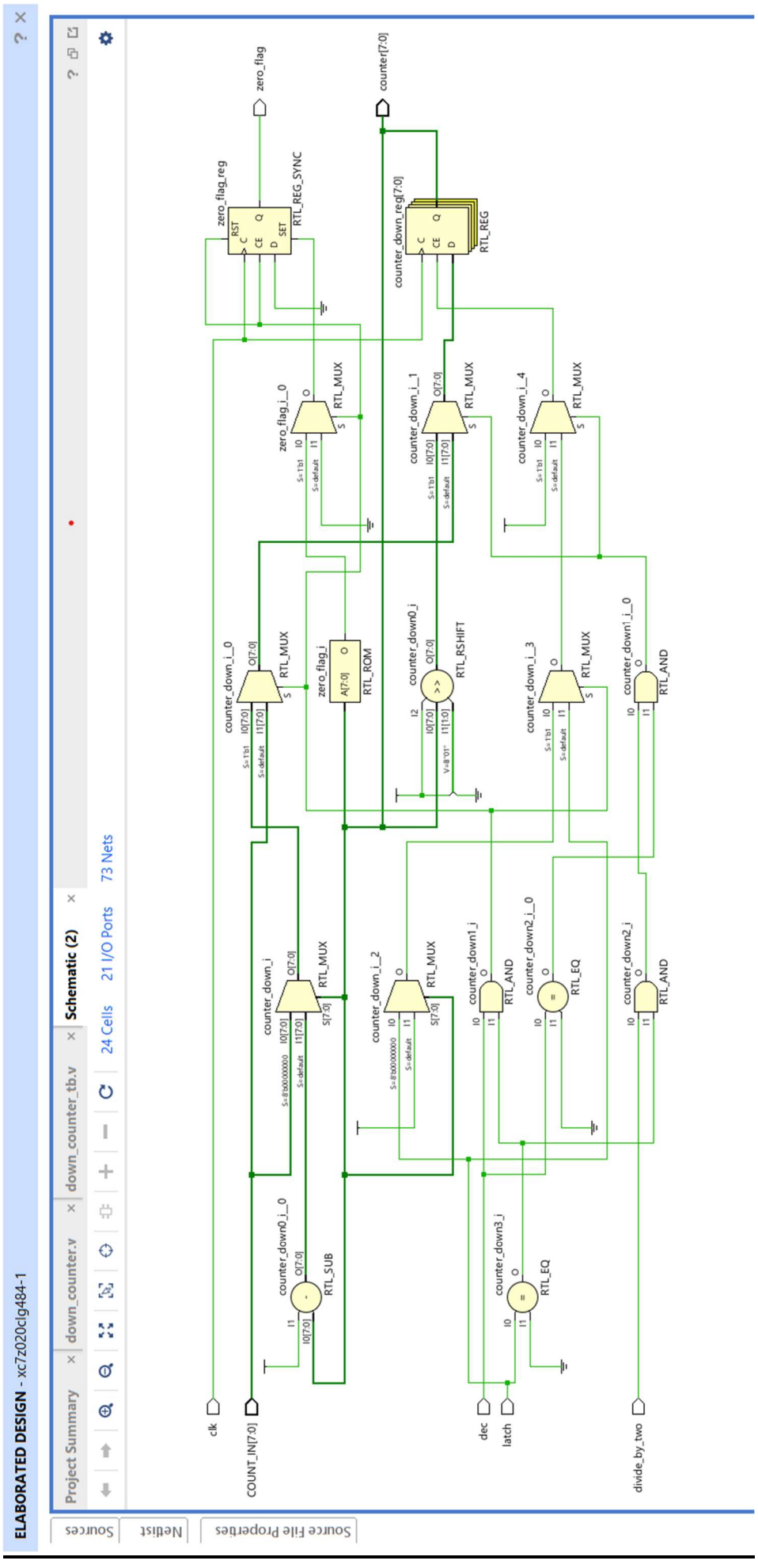
```
1  `timescale 1ns / 1ps
2  module down_counter(counter,zero_flag,clk,COUNT_IN,latch,dec,divide_by_two);
3  input clk,latch,dec,divide_by_two;
4  input [7:0] COUNT_IN;
5  output [7:0] counter;
6  output reg zero_flag=0;
7  reg [7:0] counter_down=0;
8
9  always @(posedge clk)
10 begin
11
12 if(latch)
13 counter_down <= COUNT_IN;
14
15 if(dec&latch==0)
16 if(counter_down==0)
17 begin
18 zero_flag=1;
19 end
20 else
21 begin
22 counter_down <= counter_down-1;
23 zero_flag=0;
24 end
25
26 if(divide_by_two&latch==0&dec==0)
27 counter_down <= counter_down/2;
28 end
29
30 assign counter = counter_down;
31 endmodule
```

Test Bench code:

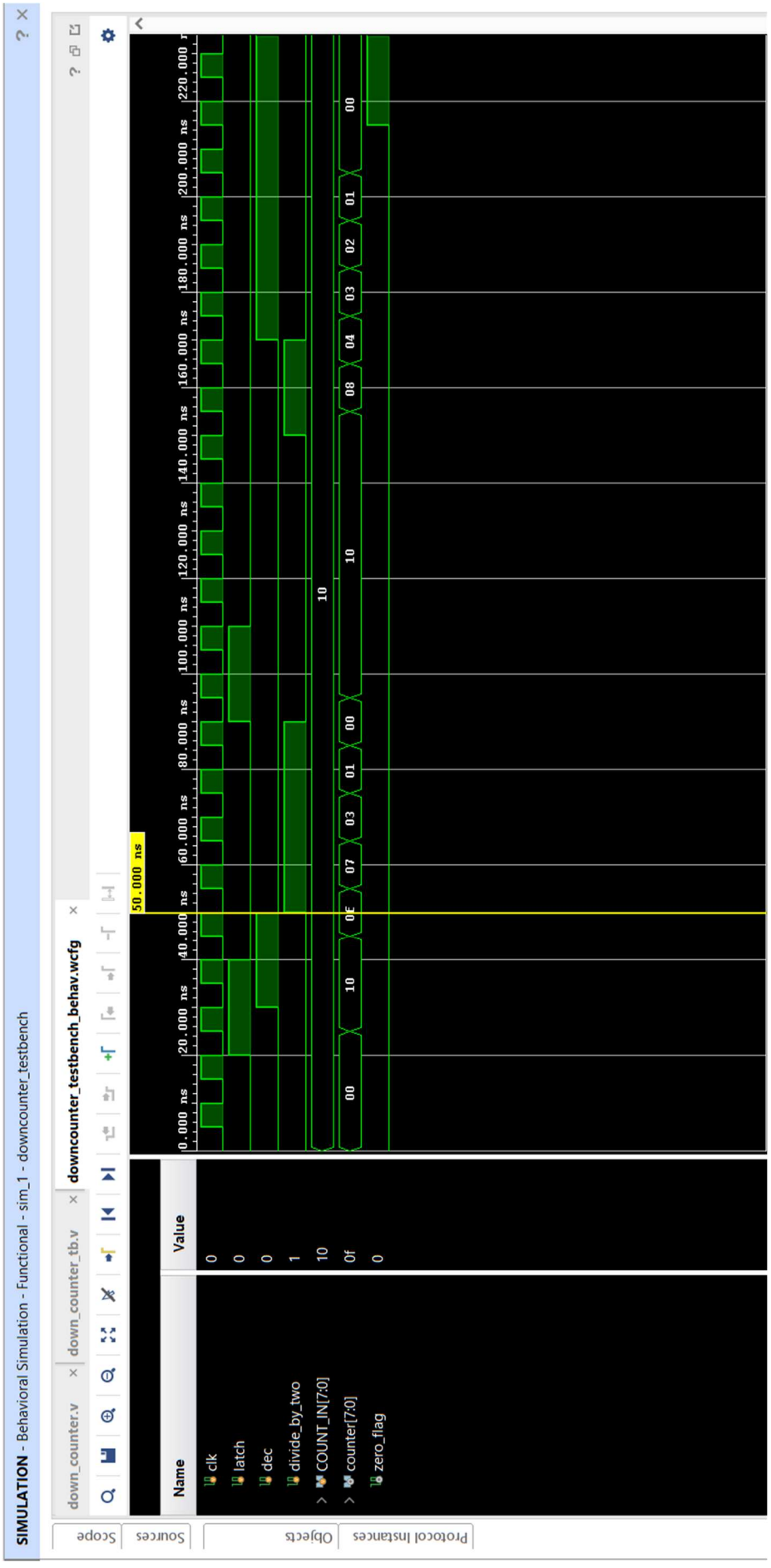
```
module downcounter_testbench();
reg clk,latch,dec,divide_by_two;
reg [7:0]COUNT_IN;
wire [7:0] counter;
wire zero_flag;
down_counter dut(counter,zero_flag,clk,COUNT_IN,latch,dec,divide_by_two);

initial begin
COUNT_IN=16;
clk=0;
forever #5 clk=~clk;
end

initial begin
latch=0;
#20;
latch=1;
#20;
latch=0;
#50
latch=1;
#20
latch=0;
#200
latch=1;
#20
latch=0;
end

initial begin
dec=0;
divide_by_two =0;
#30
dec=1;
#20
dec=0;
divide_by_two=1;
#40
divide_by_two=0;
#60
divide_by_two=1;
#20
divide_by_two=0;
dec=1;
end

endmodule
```

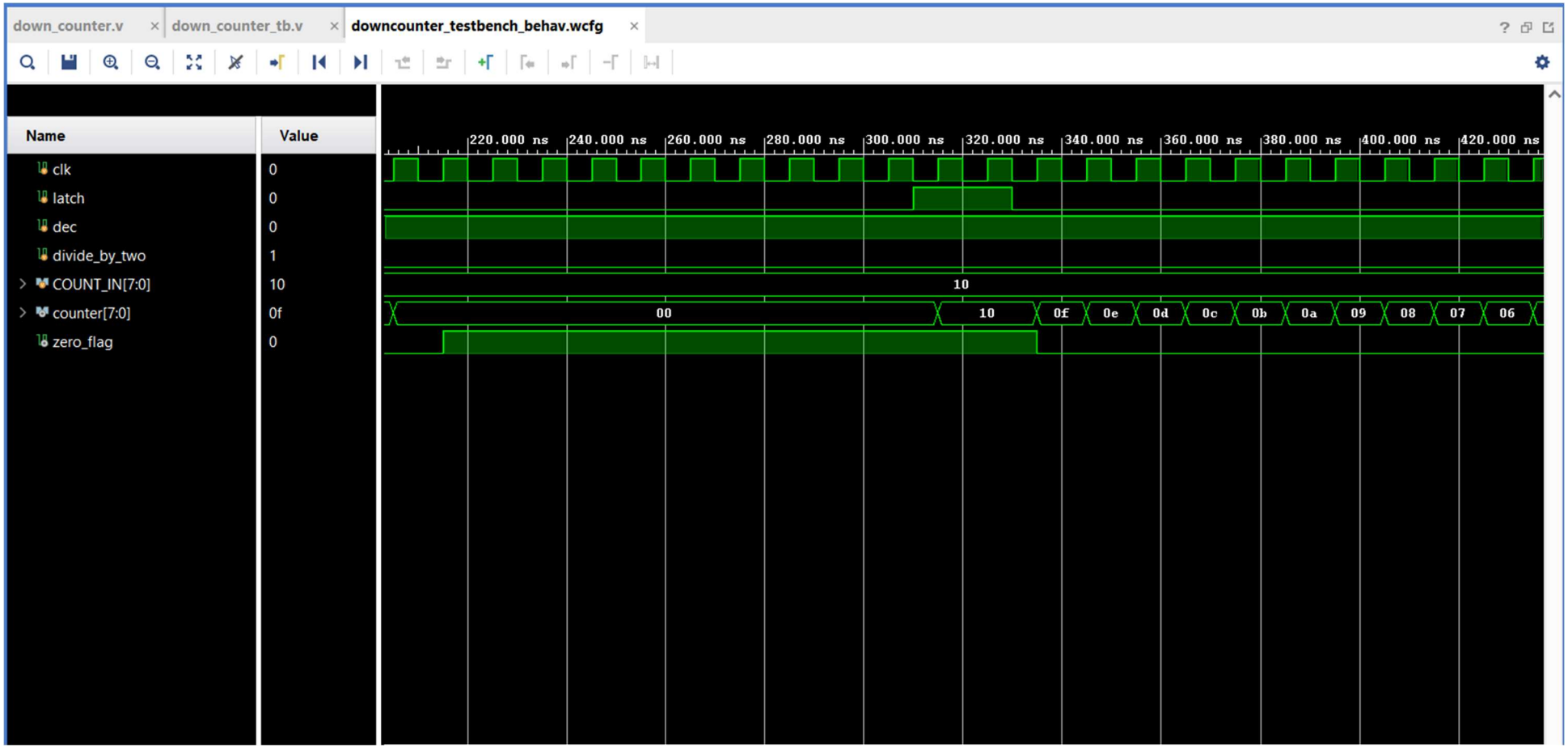
Github link for codes:
https://github.com/velicharlagokulkumar/vivado/tree/main/Assignment_1

Schematic Diagram:



Timing Diagram:




down_counter.v
down_counter_tb.v
downcounter_testbench_behav.wcfg
Name
Value
clk
0
latch
0
dec
0
divide_by_two
1
COUNT_IN[7:0]
10
counter[7:0]
0f
zero_flag
0
220.000 ns
240.000 ns
260.000 ns
280.000 ns
300.000 ns
320.000 ns
340.000 ns
360.000 ns
380.000 ns
400.000 ns
420.000 ns
10
00
10
0f
0e
0d
0c
0b
0a
09
08
07
06