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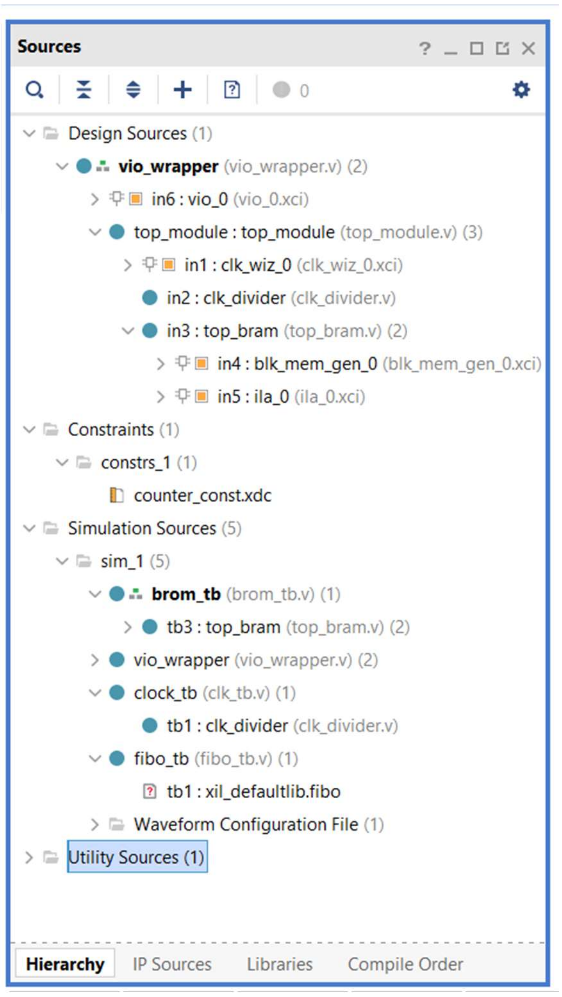
Date:10-12-2022

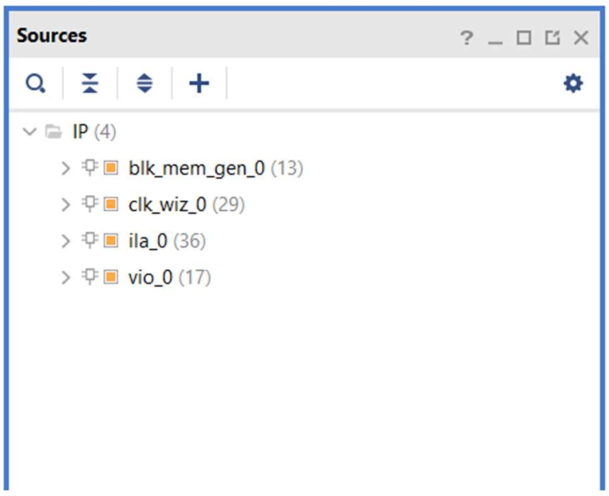
RTL ASSIGNMENT-2

The assignment is to generate Fibonacci sequence using addition and store it in a true dual port standalone block memory generator IP from Xilinx. The flow should be such that you generate an entry in the Fibonacci sequence and then you store it in the memory one after another. The memory can be treated as cyclic, i.e., once you have used the entire memory, you can wrap around and start writing from 0th address again. Use appropriate clock (using Xilinx clocking wizard IP, and use the clock available on the FPGA as source clock for the clocking wizard) frequency so that the memory doesn't get filled too quickly. Try to implement a pipelined module. Simulate and verify the functionality. Now, connect system ILA IP to the block memory generator ports to observe the working on the board. Synthesize, implement and generate the bitstream for a board that is available for use. Run it on the board and see if you're able to observe data being written to the memory.

Module code:

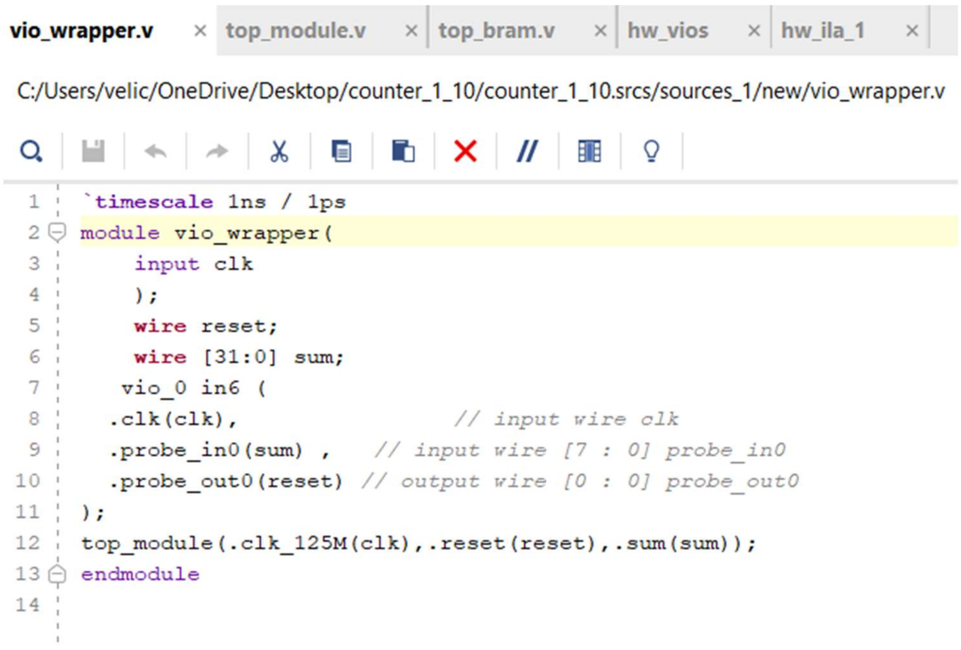


```
Design Sources (1)
  vio_wrapper (vio_wrapper.v) (2)
    in6 : vio_0 (vio_0.xci)
    top_module : top_module (top_module.v) (3)
      in1 : clk_wiz_0 (clk_wiz_0.xci)
      in2 : clk_divider (clk_divider.v)
      in3 : top_bram (top_bram.v) (2)
        in4 : blk_mem_gen_0 (blk_mem_gen_0.xci)
        in5 : ila_0 (ila_0.xci)
Constraints (1)
  constrs_1 (1)
    counter_const.xdc
Simulation Sources (5)
  sim_1 (5)
    brom_tb (brom_tb.v) (1)
      tb3 : top_bram (top_bram.v) (2)
    vio_wrapper (vio_wrapper.v) (2)
    clock_tb (clk_tb.v) (1)
      tb1 : clk_divider (clk_divider.v)
    fibo_tb (fibo_tb.v) (1)
      tb1 : xil_defaultlib.fibo
    Waveform Configuration File (1)
Utility Sources (1)
```



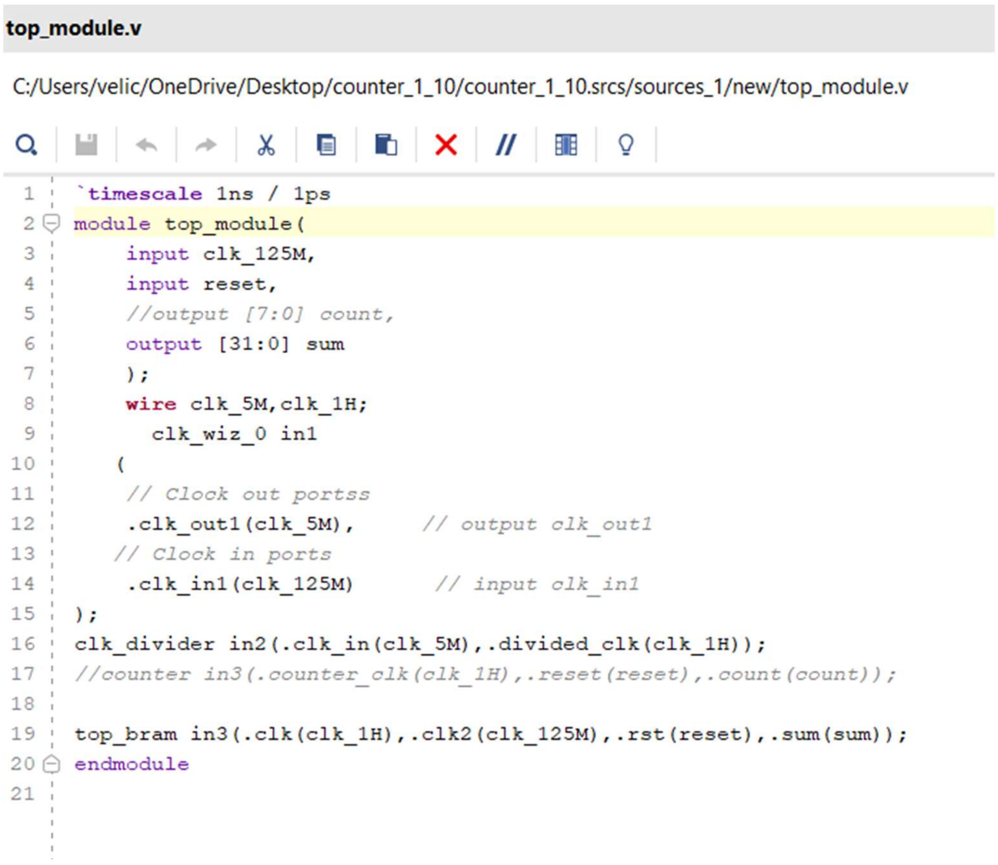
```
IP (4)
  blk_mem_gen_0 (13)
  clk_wiz_0 (29)
  ila_0 (36)
  vio_0 (17)
```

Hierarchy   IP Sources



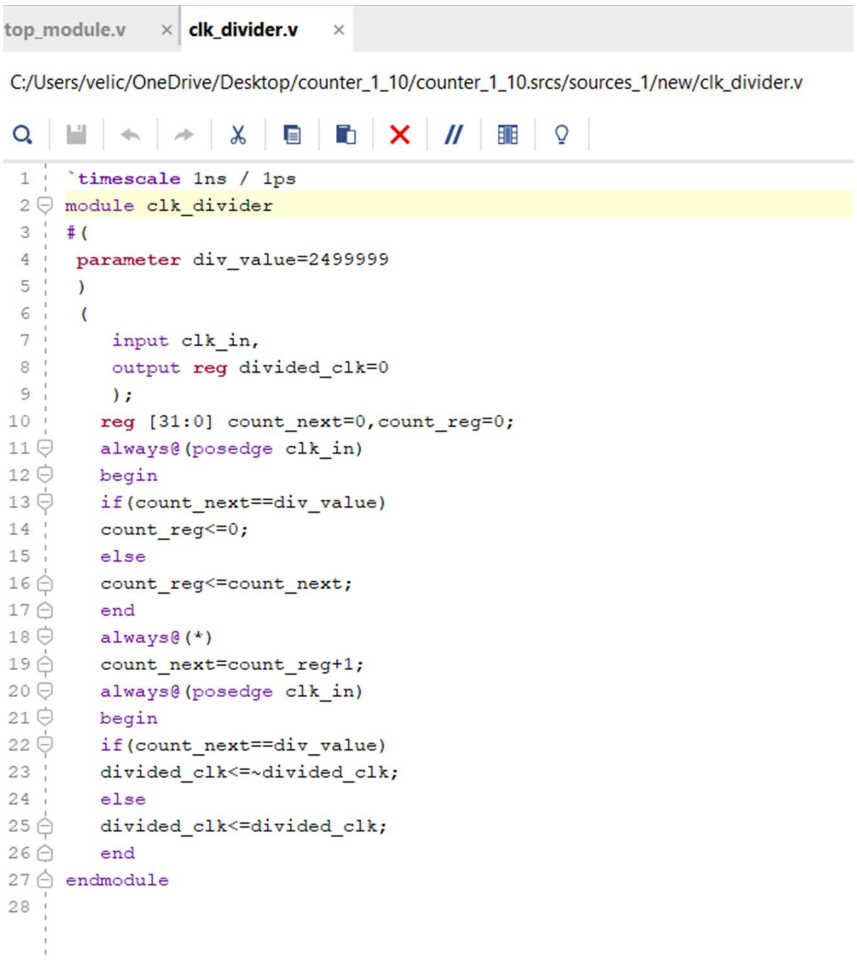
C:/Users/velic/OneDrive/Desktop/counter_1_10/counter_1_10.srcs/sources_1/new/vio_wrapper.v

```
`timescale 1ns / 1ps
module vio_wrapper(
    input clk
    );
    wire reset;
    wire [31:0] sum;
   vio_0 in6 (
  .clk(clk),                // input wire clk
  .probe_in0(sum) ,    // input wire [7 : 0] probe_in0
  .probe_out0(reset) // output wire [0 : 0] probe_out0
);
top_module(.clk_125M(clk),.reset(reset),.sum(sum));
endmodule
```



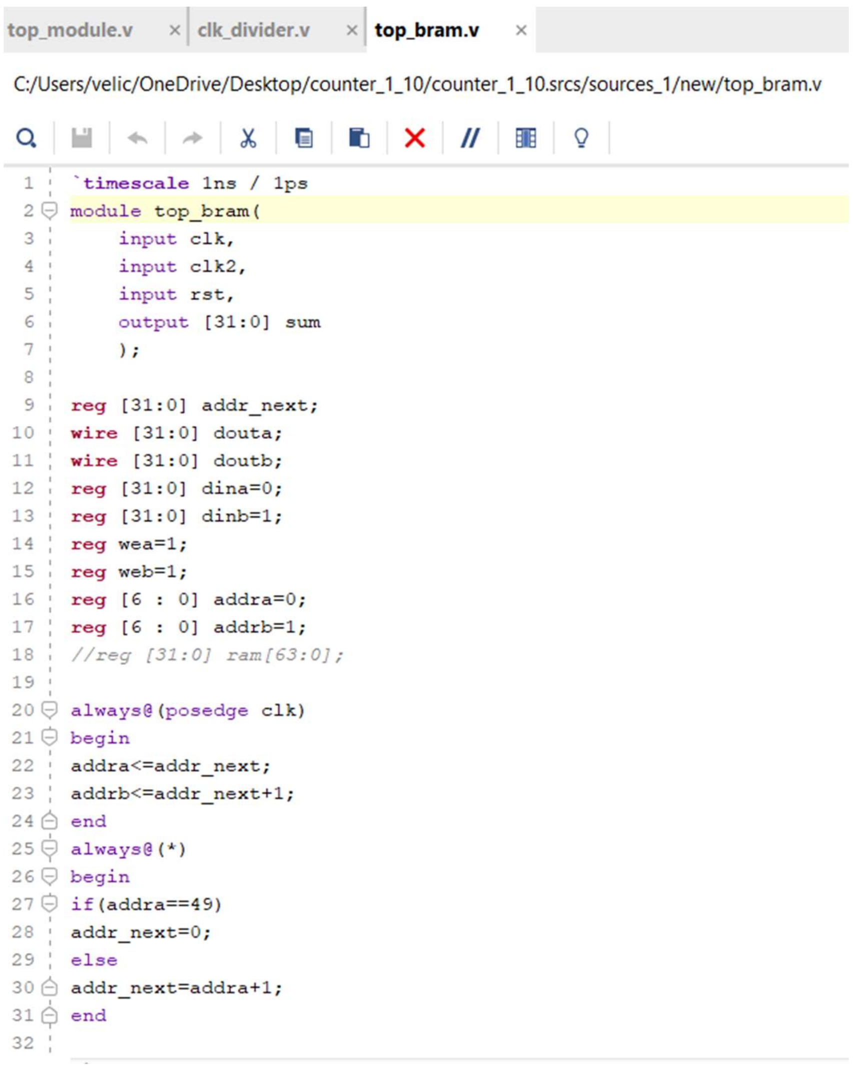
C:/Users/velic/OneDrive/Desktop/counter_1_10/counter_1_10.srcs/sources_1/new/top_module.v

```
`timescale 1ns / 1ps
module top_module(
    input clk_125M,
    input reset,
    //output [7:0] count,
    output [31:0] sum
    );
    wire clk_5M,clk_1H;
      clk_wiz_0 in1
   (
    // Clock out portss
    .clk_out1(clk_5M),     // output clk_out1
   // Clock in ports
    .clk_in1(clk_125M)      // input clk_in1
);
clk_divider in2(.clk_in(clk_5M),.divided_clk(clk_1H));
//counter in3(.counter_clk(clk_1H),.reset(reset),.count(count));

top_bram in3(.clk(clk_1H),.clk2(clk_125M),.rst(reset),.sum(sum));
endmodule
```



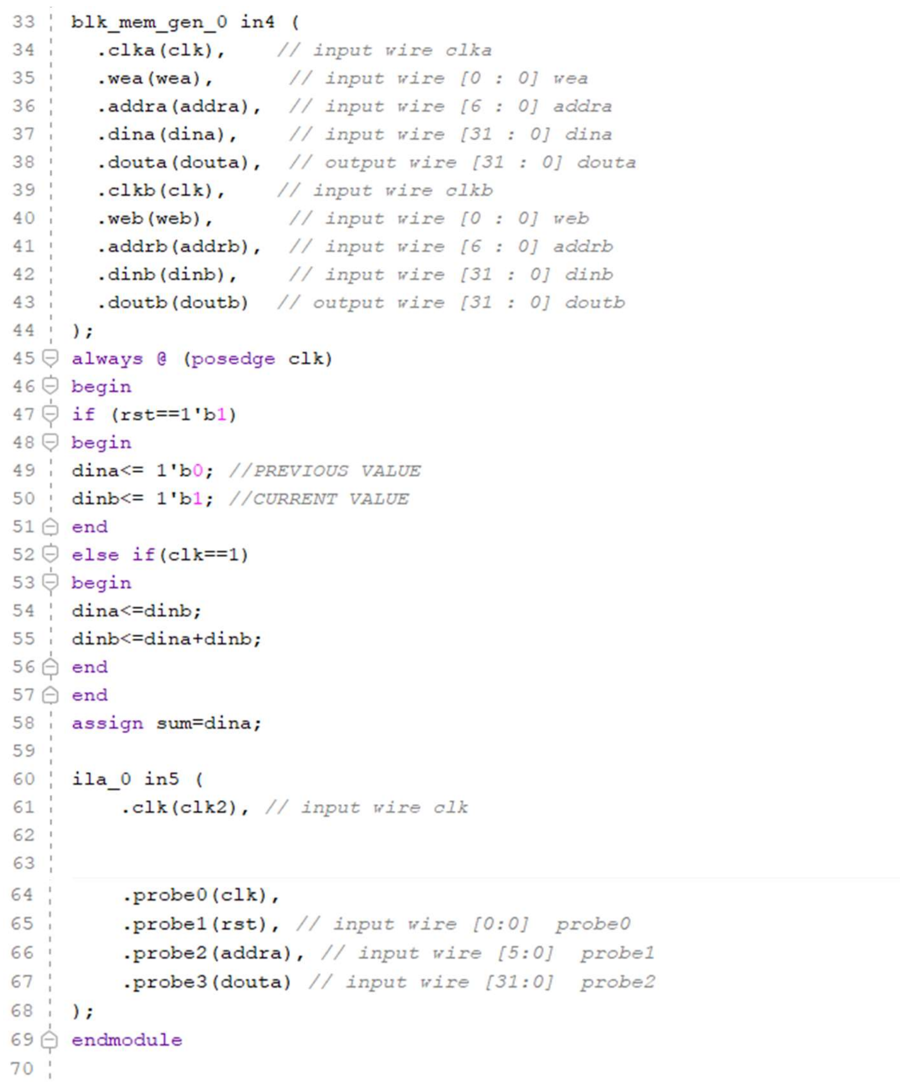
C:/Users/velic/OneDrive/Desktop/counter_1_10/counter_1_10.srcs/sources_1/new/clk_divider.v

```verilog
`timescale 1ns / 1ps
module clk_divider
#(
 parameter div_value=2499999
 )
 (
    input clk_in,
    output reg divided_clk=0
    );
   reg [31:0] count_next=0,count_reg=0;
   always@(posedge clk_in)
   begin
   if(count_next==div_value)
   count_reg<=0;
   else
   count_reg<=count_next;
   end
   always@(*)
   count_next=count_reg+1;
   always@(posedge clk_in)
   begin
   if(count_next==div_value)
   divided_clk<=~divided_clk;
   else
   divided_clk<=divided_clk;
   end
endmodule

```



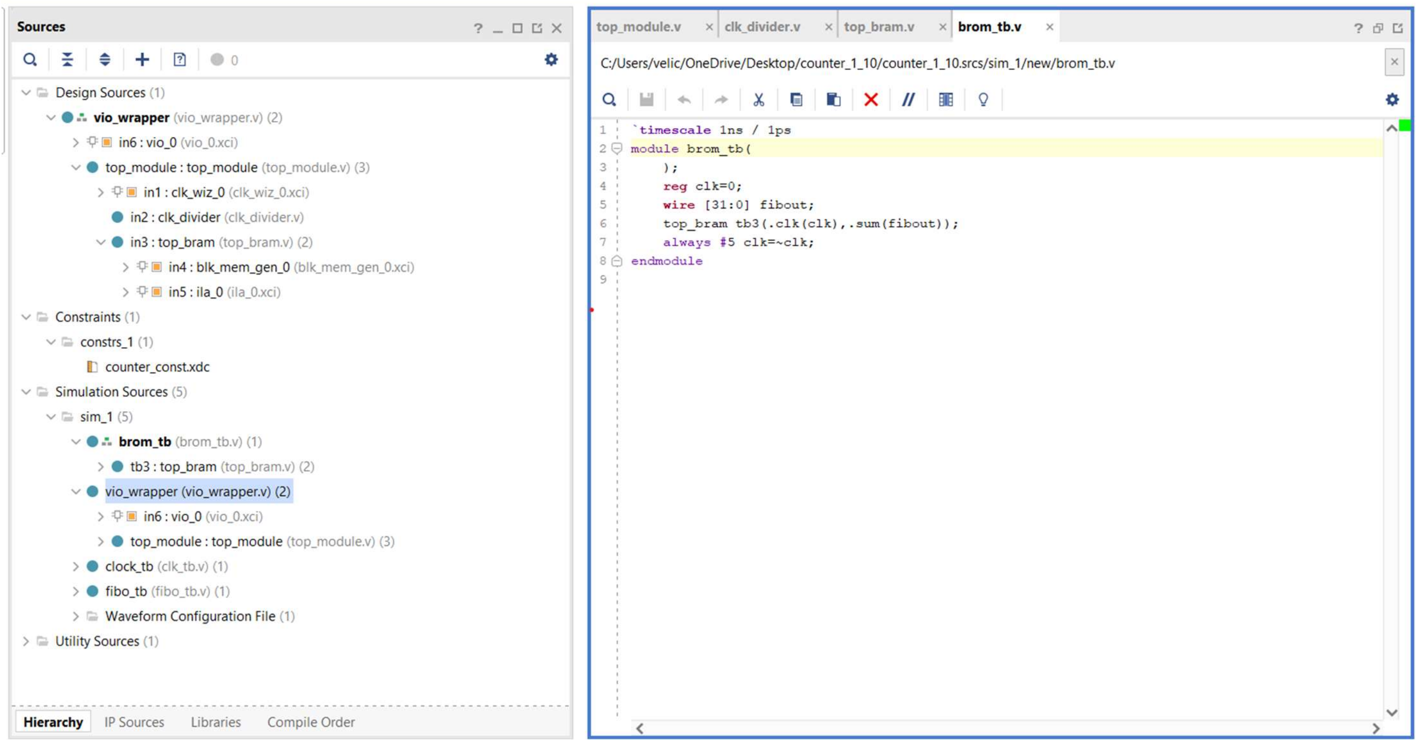
C:/Users/velic/OneDrive/Desktop/counter_1_10/counter_1_10.srcs/sources_1/new/top_bram.v

```verilog
`timescale 1ns / 1ps
module top_bram(
    input clk,
    input clk2,
    input rst,
    output [31:0] sum
    );

reg [31:0] addr_next;
wire [31:0] douta;
wire [31:0] doutb;
reg [31:0] dina=0;
reg [31:0] dinb=1;
reg wea=1;
reg web=1;
reg [6 : 0] addra=0;
reg [6 : 0] addrb=1;
//reg [31:0] ram[63:0];

always@(posedge clk)
begin
addra<=addr_next;
addrb<=addr_next+1;
end
always@(*)
begin
if(addra==49)
addr_next=0;
else
addr_next=addra+1;
end

```



```verilog
blk_mem_gen_0 in4 (
  .clka(clk),    // input wire clka
  .wea(wea),      // input wire [0 : 0] wea
  .addra(addra),  // input wire [6 : 0] addra
  .dina(dina),    // input wire [31 : 0] dina
  .douta(douta),  // output wire [31 : 0] douta
  .clkb(clk),    // input wire clkb
  .web(web),      // input wire [0 : 0] web
  .addrb(addrb),  // input wire [6 : 0] addrb
  .dinb(dinb),    // input wire [31 : 0] dinb
  .doutb(doutb)  // output wire [31 : 0] doutb
);
always @ (posedge clk)
begin
if (rst==1'b1)
begin
dina<= 1'b0; //PREVIOUS VALUE
dinb<= 1'b1; //CURRENT VALUE
end
else if(clk==1)
begin
dina<=dinb;
dinb<=dina+dinb;
end
end
assign sum=dina;

ila_0 in5 (
    .clk(clk2), // input wire clk


    .probe0(clk),
    .probe1(rst), // input wire [0:0]  probe0
    .probe2(addra), // input wire [5:0]  probe1
    .probe3(douta) // input wire [31:0]  probe2
);
endmodule

```

Test Bench code:



Sources

Design Sources (1)
- vio_wrapper (vio_wrapper.v) (2)
  - in6 : vio_0 (vio_0.xci)
  - top_module : top_module (top_module.v) (3)
    - in1 : clk_wiz_0 (clk_wiz_0.xci)
    - in2 : clk_divider (clk_divider.v)
    - in3 : top_bram (top_bram.v) (2)
      - in4 : blk_mem_gen_0 (blk_mem_gen_0.xci)
      - in5 : ila_0 (ila_0.xci)

Constraints (1)
- constrs_1 (1)
  - counter_const.xdc

Simulation Sources (5)
- sim_1 (5)
  - brom_tb (brom_tb.v) (1)
    - tb3 : top_bram (top_bram.v) (2)
  - vio_wrapper (vio_wrapper.v) (2)
    - in6 : vio_0 (vio_0.xci)
    - top_module : top_module (top_module.v) (3)
  - clock_tb (clk_tb.v) (1)
  - fibo_tb (fibo_tb.v) (1)
  - Waveform Configuration File (1)

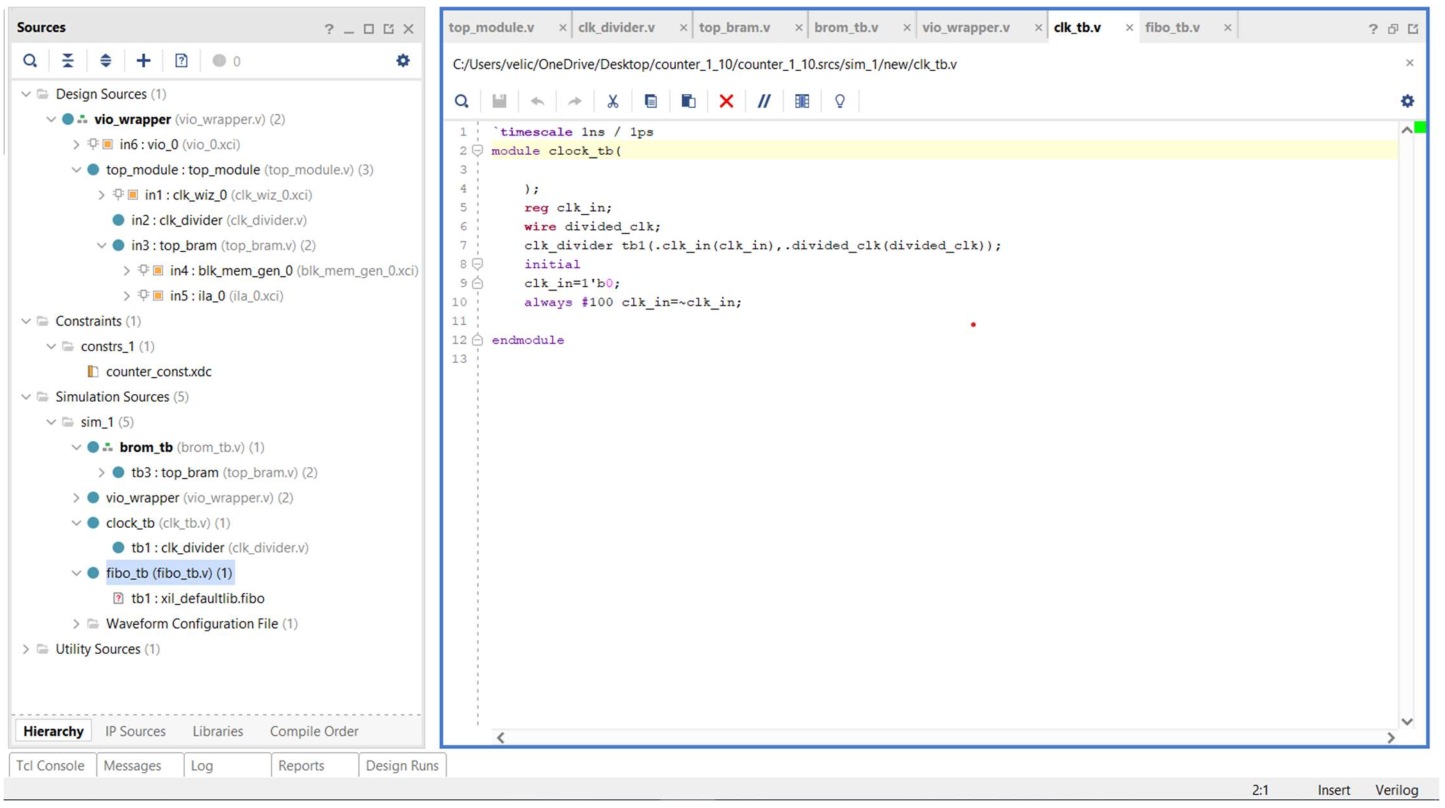
Utility Sources (1)

Hierarchy | IP Sources | Libraries | Compile Order

top_module.v | clk_divider.v | top_bram.v | brom_tb.v

C:/Users/velic/OneDrive/Desktop/counter_1_10/counter_1_10.srcs/sim_1/new/brom_tb.v

```verilog
`timescale 1ns / 1ps
module brom_tb(
    );
    reg clk=0;
    wire [31:0] fibout;
    top_bram tb3(.clk(clk),.sum(fibout));
    always #5 clk=~clk;
endmodule
```



Sources

Design Sources (1)
- vio_wrapper (vio_wrapper.v) (2)
  - in6 : vio_0 (vio_0.xci)
  - top_module : top_module (top_module.v) (3)
    - in1 : clk_wiz_0 (clk_wiz_0.xci)
    - in2 : clk_divider (clk_divider.v)
    - in3 : top_bram (top_bram.v) (2)
      - in4 : blk_mem_gen_0 (blk_mem_gen_0.xci)
      - in5 : ila_0 (ila_0.xci)

Constraints (1)
- constrs_1 (1)
  - counter_const.xdc

Simulation Sources (5)
- sim_1 (5)
  - brom_tb (brom_tb.v) (1)
    - tb3 : top_bram (top_bram.v) (2)
  - vio_wrapper (vio_wrapper.v) (2)
  - clock_tb (clk_tb.v) (1)
    - tb1 : clk_divider (clk_divider.v)
  - fibo_tb (fibo_tb.v) (1)
    - tb1 : xil_defaultlib.fibo
  - Waveform Configuration File (1)

Utility Sources (1)

Hierarchy | IP Sources | Libraries | Compile Order

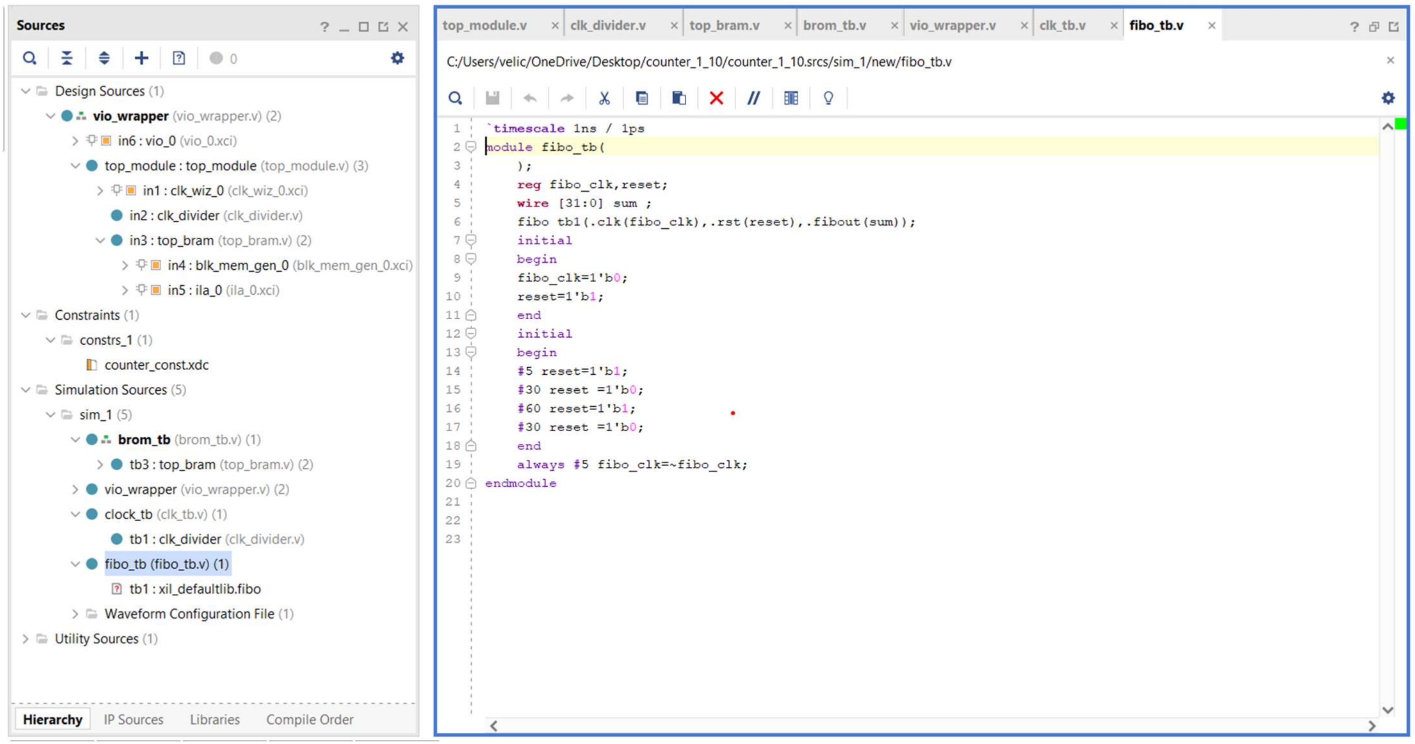
top_module.v | clk_divider.v | top_bram.v | brom_tb.v | vio_wrapper.v | clk_tb.v | fibo_tb.v

C:/Users/velic/OneDrive/Desktop/counter_1_10/counter_1_10.srcs/sim_1/new/clk_tb.v

```verilog
`timescale 1ns / 1ps
module clock_tb(

    );
    reg clk_in;
    wire divided_clk;
    clk_divider tb1(.clk_in(clk_in),.divided_clk(divided_clk));
    initial
    clk_in=1'b0;
    always #100 clk_in=~clk_in;

endmodule
```

Tcl Console | Messages | Log | Reports | Design Runs

2:1 Insert Verilog



Sources

- Design Sources (1)
  - vio_wrapper (vio_wrapper.v) (2)
    - in6 : vio_0 (vio_0.xci)
    - top_module : top_module (top_module.v) (3)
      - in1 : clk_wiz_0 (clk_wiz_0.xci)
      - in2 : clk_divider (clk_divider.v)
      - in3 : top_bram (top_bram.v) (2)
        - in4 : blk_mem_gen_0 (blk_mem_gen_0.xci)
        - in5 : ila_0 (ila_0.xci)
- Constraints (1)
  - constrs_1 (1)
    - counter_const.xdc
- Simulation Sources (5)
  - sim_1 (5)
    - brom_tb (brom_tb.v) (1)
      - tb3 : top_bram (top_bram.v) (2)
    - vio_wrapper (vio_wrapper.v) (2)
    - clock_tb (clk_tb.v) (1)
      - tb1 : clk_divider (clk_divider.v)
    - fibo_tb (fibo_tb.v) (1)
      - tb1 : xil_defaultlib.fibo
    - Waveform Configuration File (1)
- Utility Sources (1)

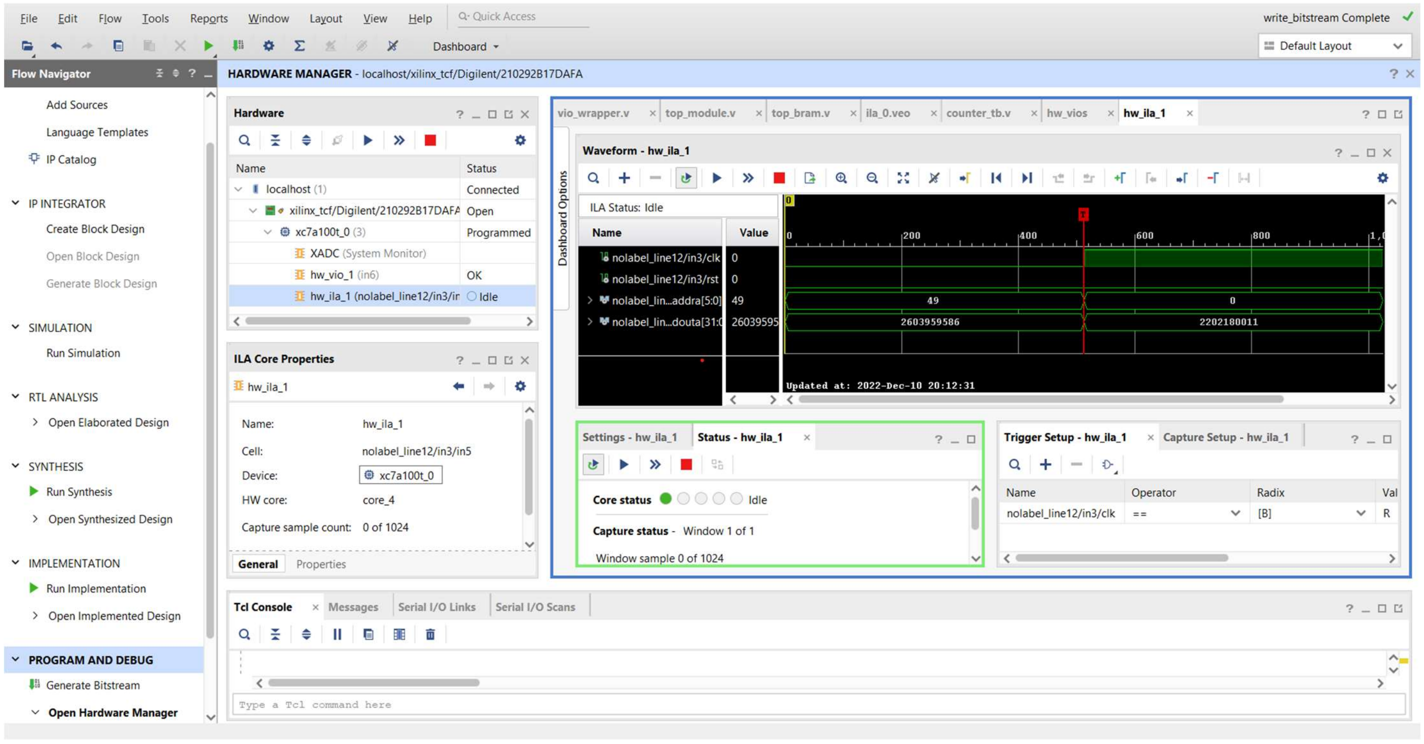
Hierarchy | IP Sources | Libraries | Compile Order

top_module.v | clk_divider.v | top_bram.v | brom_tb.v | vio_wrapper.v | clk_tb.v | fibo_tb.v

C:/Users/velic/OneDrive/Desktop/counter_1_10/counter_1_10.srcs/sim_1/new/fibo_tb.v

```verilog
`timescale 1ns / 1ps
module fibo_tb(
    );
    reg fibo_clk,reset;
    wire [31:0] sum ;
    fibo tb1(.clk(fibo_clk),.rst(reset),.fibout(sum));
    initial
    begin
    fibo_clk=1'b0;
    reset=1'b1;
    end
    initial
    begin
    #5 reset=1'b1;
    #30 reset =1'b0;
    #60 reset=1'b1;
    #30 reset =1'b0;
    end
    always #5 fibo_clk=~fibo_clk;
endmodule
```

Internal Logic Analyzer (ILA):



write_bitstream Complete

HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210292B17DAFA

Hardware

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/210292B17DAFA	Open
xc7a100t_0 (3)	Programmed
XADC (System Monitor)	
hw_vio_1 (in6)	OK
hw_ila_1 (nolabel_line12/in3/in	Idle

ILA Core Properties

hw_ila_1

Name:	hw_ila_1
Cell:	nolabel_line12/in3/in5
Device:	xc7a100t_0
HW core:	core_4
Capture sample count:	0 of 1024

General | Properties

vio_wrapper.v | top_module.v | top_bram.v | ila_0.veo | counter_tb.v | hw_vios | hw_ila_1

Waveform - hw_ila_1

ILA Status: Idle

Name	Value
nolabel_line12/in3/clk	0
nolabel_line12/in3/rst	0
nolabel_lin...addra[5:0]	49
nolabel_lin...douta[31:0	26039595

0 200 400 600 800 1,0

addra: 49 → 0

douta: 2603959586 → 2202180011

Updated at: 2022-Dec-10 20:12:31

Settings - hw_ila_1 | Status - hw_ila_1

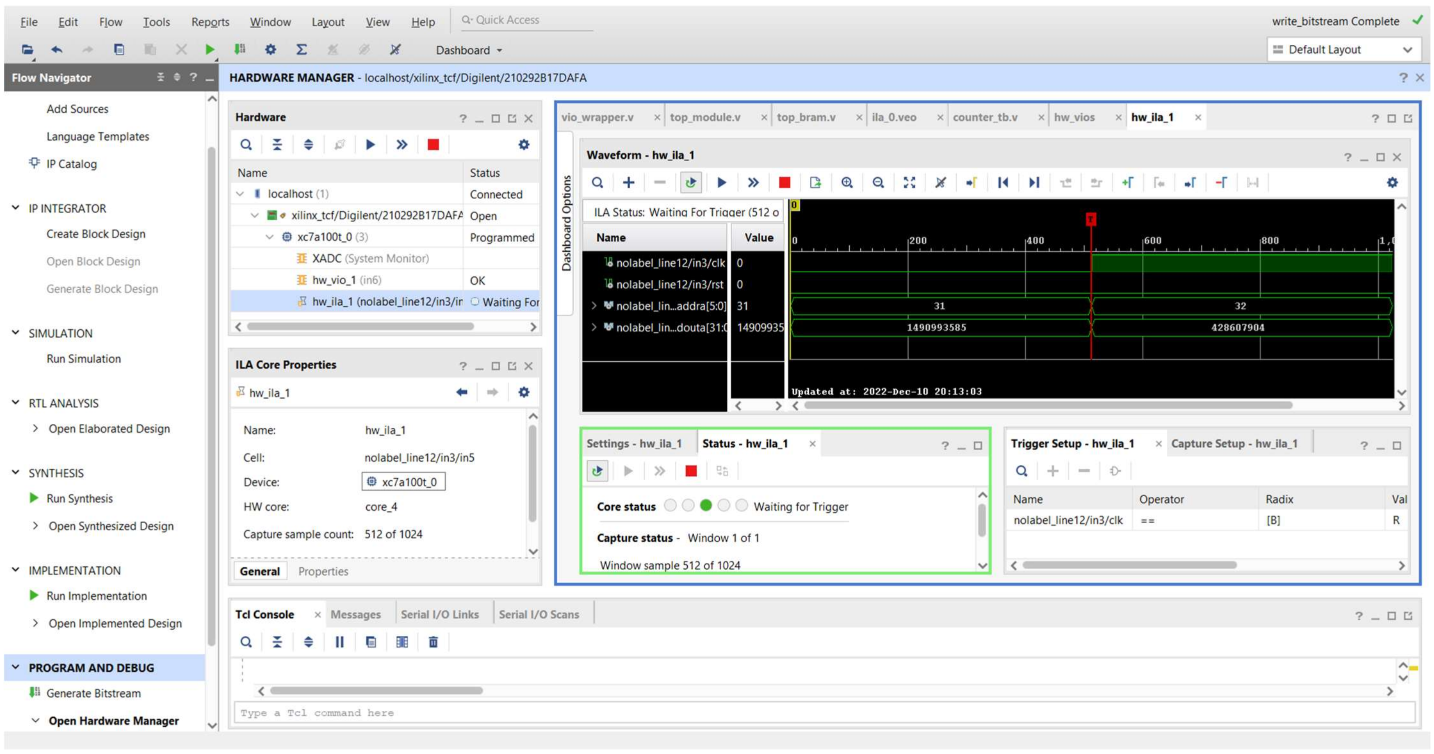
Core status ● ○ ○ ○ ○ Idle

Capture status - Window 1 of 1

Window sample 0 of 1024

Trigger Setup - hw_ila_1 | Capture Setup - hw_ila_1

Name	Operator	Radix	Val
nolabel_line12/in3/clk	==	[B]	R



HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210292B17DAFA

Hardware

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/210292B17DAFA	Open
xc7a100t_0 (3)	Programmed
XADC (System Monitor)	
hw_vio_1 (in6)	OK
hw_ila_1 (nolabel_line12/in3/ir	Waiting For

ILA Core Properties

hw_ila_1

Name:	hw_ila_1
Cell:	nolabel_line12/in3/in5
Device:	xc7a100t_0
HW core:	core_4
Capture sample count:	512 of 1024

General Properties

Waveform - hw_ila_1

ILA Status: Waiting For Trigger (512 o

Name	Value
nolabel_line12/in3/clk	0
nolabel_line12/in3/rst	0
nolabel_lin...addra[5:0]	31
nolabel_lin...douta[31:0]	14909935

0 200 400 600 800 1,0

31 32

1490993585 428607904

Updated at: 2022-Dec-10 20:13:03

Settings - hw_ila_1 | Status - hw_ila_1

Core status: Waiting for Trigger

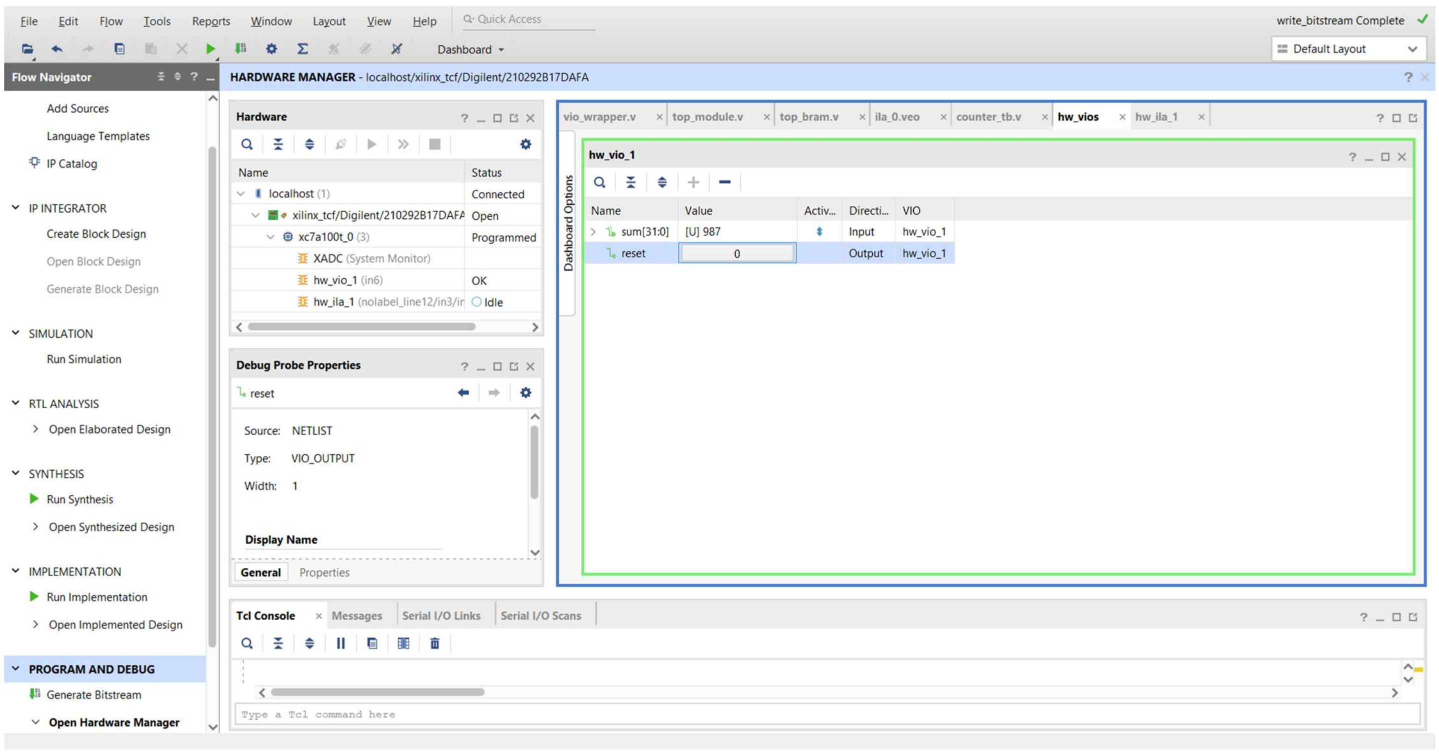
Capture status - Window 1 of 1

Window sample 512 of 1024

Trigger Setup - hw_ila_1 | Capture Setup - hw_ila_1

Name	Operator	Radix	Val
nolabel_line12/in3/clk	==	[B]	R

Virtual Input Output (VIO):



HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210292B17DAFA

Hardware

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/210292B17DAFA	Open
xc7a100t_0 (3)	Programmed
XADC (System Monitor)	
hw_vio_1 (in6)	OK
hw_ila_1 (nolabel_line12/in3/ir	Idle

Debug Probe Properties

reset

Source:	NETLIST
Type:	VIO_OUTPUT
Width:	1

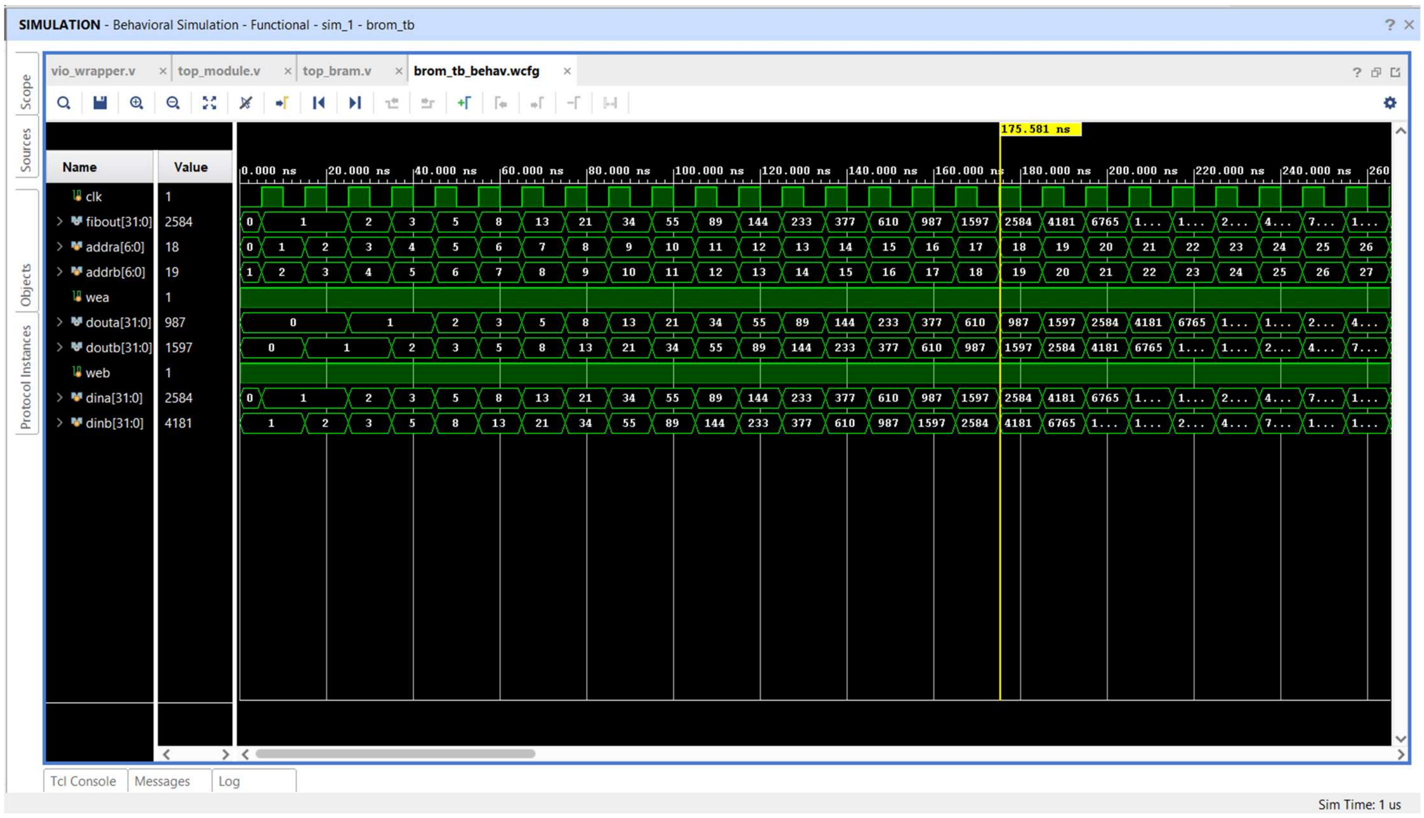
Display Name

General Properties

hw_vio_1

Name	Value	Activ...	Directi...	VIO
sum[31:0]	[U] 987		Input	hw_vio_1
reset	0		Output	hw_vio_1

Simulation (brom_tb):



SIMULATION - Behavioral Simulation - Functional - sim_1 - brom_tb

vio_wrapper.v | top_module.v | top_bram.v | brom_tb_behav.wcfg

```
175.581 ns
0.000 ns  20.000 ns  40.000 ns  60.000 ns  80.000 ns  100.000 ns  120.000 ns  140.000 ns  160.000 ns  180.000 ns  200.000 ns  220.000 ns  240.000 ns  260

Name           Value
clk            1
fibout[31:0]   2584   0 1 2 3 5 8 13 21 34 55 89 144 233 377 610 987 1597 2584 4181 6765 1... 1... 2... 4... 7... 1...
addra[6:0]     18     0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
addrb[6:0]     19     1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
wea            1
douta[31:0]    987    0 1 2 3 5 8 13 21 34 55 89 144 233 377 610 987 1597 2584 4181 6765 1... 1... 2... 4...
doutb[31:0]    1597   0 1 2 3 5 8 13 21 34 55 89 144 233 377 610 987 1597 2584 4181 6765 1... 1... 2... 4... 7...
web            1
dina[31:0]     2584   0 1 2 3 5 8 13 21 34 55 89 144 233 377 610 987 1597 2584 4181 6765 1... 1... 2... 4... 7... 1...
dinb[31:0]     4181   1 2 3 5 8 13 21 34 55 89 144 233 377 610 987 1597 2584 4181 6765 1... 1... 2... 4... 7... 1... 1...
```

Tcl Console | Messages | Log

Sim Time: 1 us

Github link for codes:
https://github.com/velicharlagokulkumar/vivado/tree/main/Assignment_2